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DAQ

DAQPad™-6507/6508 User Manual

Digital I/O Devices for USB

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About This Manual

This manual describes the mechanical and electrical aspects of the DAQPad-6507 and DAQPad-6508 and contains information concerning their operation and programming.

The DAQPad-6507 and DAQPad-6508 are digital I/O devices for USB-compatible computers. These devices are designed for high-performance data acquisition and control for applications in laboratory testing, production testing, and industrial process monitoring and control.

Organization of This Manual

The *DAQPad-6507/6508 User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the DAQPad-6507 and DAQPad-6508; lists what you need to get started; describes software programming choices, optional equipment, and custom cables; and explains how to unpack the DAQPad-6507 and DAQPad-6508.
- Chapter 2, *Installation and Configuration*, describes how to install and configure the DAQPad-6507 and DAQPad-6508 devices.
- Chapter 3, *Signal Connections*, includes timing specifications and signal connection instructions for the DAQPad-6507 and 6508 I/O connectors.
- Chapter 4, *Theory of Operation*, contains a functional overview of the DAQPad-6507/6508 devices and explains the operation of each functional unit making up the DAQPad-6507 or DAQPad-6508.
- Appendix A, *Specifications*, lists the specifications of the DAQPad-6507/6508 devices.
- Appendix B, *OKI 82C55A Data Sheet*, contains the manufacturer data sheet for the OKI 82C55A (OKI Semiconductor) CMOS programmable peripheral interface. This interface is used on the DAQPad-6507/6508 devices.
- Appendix C, *Common Questions*, contains a list of commonly asked questions and their answers relating to usage and special features of your DAQPad-6507/6508 devices.

- Appendix D, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* alphabetically lists the topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual:

☞	This icon to the left of bold italicized text denotes a note, which alerts you to important information.
⚠	This icon to the left of bold italicized text denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.
82C55A	82C55A refers to the OKI 82C55A (OKI Semiconductor) CMOS programmable peripheral interface.
< >	Angle brackets containing numbers separated by an ellipses represent a range of values associated with a bit or signal name (for example, ACH<0..7>).
bold italic	Bold italic text denotes a note, caution, or warning.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
`monospace`	Text in this font denotes text or characters that you should literally enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and for statements and comments taken from programs.
NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles unless otherwise noted.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ devices.

National Instruments Documentation

The *DAQPad-6507/6508 User Manual* is one piece of the documentation set for your data acquisition (DAQ) system. You could have any of several types of manuals, depending on the hardware and software in your system. Use the different types of manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.
- Software documentation—Examples of software documentation you may have are the LabVIEW, LabWindows/CVI, and NI-DAQ documentation sets. After you set up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) documentation or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure your hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides or accessory device user manuals. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.
- *SCXI Chassis User Manual*—If you are using SCXI, read this manual for maintenance information on the chassis and installation instructions.

Related Documentation

If you are a register-level programmer, the following documents contain information that you may find helpful as you read this manual:

- Your computer technical reference manual
- USB Specification, Revision 1.1

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix D, *Customer Communication*, at the end of this manual.

Chapter 1

Introduction

This chapter describes the DAQPad-6507 and DAQPad-6508; lists what you need to get started; describes software programming choices, optional equipment, and custom cables; and explains how to unpack the DAQPad-6507 and DAQPad-6508.

About the DAQPad-6507 and DAQPad-6508 Devices

Thank you for purchasing the National Instruments DAQPad-6507 or DAQPad-6508. Your DAQPad device is a 96-bit, parallel, digital I/O interface for computers with USB ports. Four 82C55A programmable peripheral interface (PPI) chips control the 96 bits of digital I/O. The 82C55A can operate in either a unidirectional or bidirectional mode and can generate interrupt requests to the host computer. You can program the 82C55A for almost any 8-bit or 16-bit digital I/O application. All communication is through a standard, 100-pin, female connector for the DAQPad-6508 or 100-screw terminals with a strain-relief clamp for the DAQPad-6507.

Your DAQPad device has a wide input voltage range, and can be powered from any 9 to 30 VDC power supply.

You can use your DAQPad device in a wide range of digital I/O applications. With the DAQPad-6507 and DAQPad-6508 devices, you can interface any PC to any of the following:

- Other computers:
  - Another PC with a National Instruments PC-DIO-96/PnP, PC-DIO-24/PnP, AT-DIO-32F, DAQPad-6507, or DAQPad-6508
  - Any other computer with an 8-bit or 16-bit parallel interface
- Centronics-compatible printers and plotters
- Panel meters
- Instruments and test equipment with BCD readouts and/or controls
- Optically isolated, solid-state relays and I/O module mounting racks

Note ***Your DAQPad device cannot sink sufficient current to drive the SSR-OAC-5 and SSR-OAC-5A output modules. However, it can drive the SSR-ODC-5 output module and all SSR input modules available from National Instruments.***

If you need to drive an SSR-OAC-5 or SSR-OAC-5A, you can either use a non-inverting digital buffer chip between your DAQPad device and the SSR backplane, or you can use an MIO series device with appropriate connections (for example, an SC-205X and cables).

With a DAQPad-6507or DAQPad-6508, your computer can serve as a digital I/O system controller for laboratory testing, production testing, and industrial process monitoring and control.

Detailed specifications of the DAQPad-6507 and DAQPad-6508 devices are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your DAQPad-6507 or DAQPad-6508, you will need the following:

- ❑ DAQPad-6507 or DAQPad-6508 device
- ❑ DAQPad-6507/6508 User Manual
- ❑ One of the following software packages and documentation:
  - NI-DAQ for PC Compatibles
  - LabVIEW for Windows
  - LabWindows/CVI
  - ComponentWorks
  - VirtualBench
- ❑ Your computer

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use LabVIEW, LabWindows/CVI, ComponentWorks, VirtualBench, NI-DAQ, or register-level programming.

National Instruments Application Software

LabVIEW and LabWindows/CVI are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows/CVI enhances traditional programming languages. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

ComponentWorks contains tools for data acquisition and instrument control built on NI-DAQ driver software. ComponentWorks provides a higher-level programming interface for building virtual instruments through standard OLE controls and DLLs. With ComponentWorks, you can use all of the configuration tools, resource management utilities, and interactive control utilities included with NI-DAQ.

VirtualBench features virtual instruments that combine DAQ products, software, and your computer to create a stand-alone instrument with the added benefit of the processing, display, and storage capabilities of your computer. VirtualBench instruments load and save waveform data to disk in the same forms that can be used in popular spreadsheet programs and word processors.

Using LabVIEW, LabWindows/CVI, ComponentWorks, or VirtualBench software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages or NI-DAQ software, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

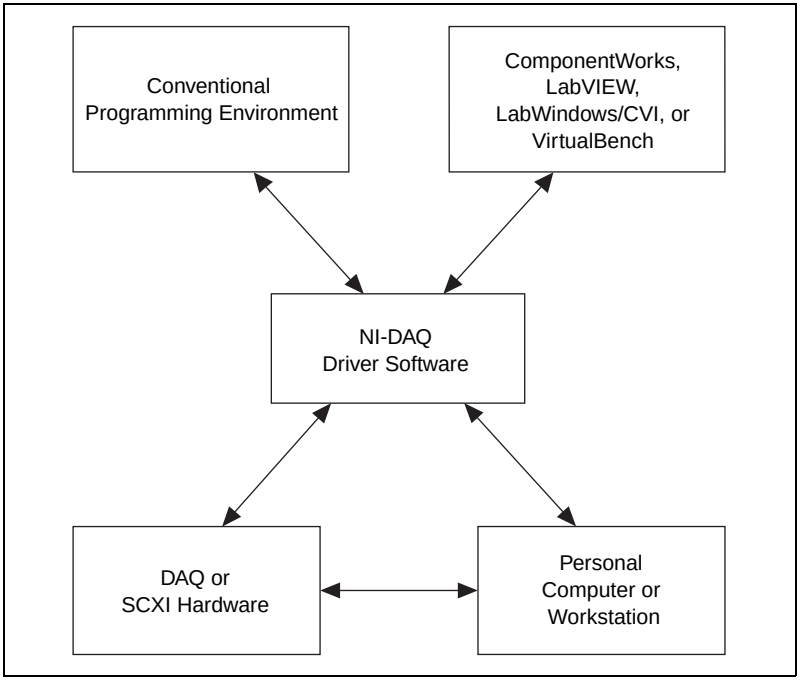


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Optional Equipment

National Instruments offers a variety of products to use with your DAQPad-6508 device, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies
- Connector blocks and unshielded 50-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals—from up to 3,072 channels—for relays and analog output
- Low channel count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For more specific information about these products, refer to your National Instruments catalogue or website, or call the office nearest you.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

You can connect the DAQPad-6508 device to a wide range of printers, plotters, test instruments, I/O racks and modules, screw terminal panels, and almost any device with a parallel interface. The DAQPad-6508 digital I/O connector is a standard, 100-pin header connector. Adapters for this header connector expand the interface to four 50-pin ribbon cables, each of which has the pinout of a PC-DIO-24. The pin assignments of the expansion cables are compatible with the standard 24-channel I/O module mounting racks (such as those manufactured by Opto 22 and Gordos).

The CB-100 cable termination accessory is available from National Instruments for use with your DAQPad device. This accessory includes two 50-conductor, flat-ribbon cables and a connector block. You can attach signal input and output wires to screw terminals on the connector block and, therefore, connect signals to your DAQPad device I/O connector.

You can use the CB-100 for initial prototyping of an application or in situations in which your DAQPad device interconnections are frequently changed. When a final field wiring scheme has been developed, you might want to develop your own cable.

If you want to develop your own cable, the mating connector for the DAQPad-6508 is a 100-position, right-angle receptacle without board locks. Recommended manufacturer part numbers for this mating connector are as follows:

- AMP Corporation (part number 749076-9)
- Honda Corporation (part number PCS-XE100LFD-HS)

Unpacking

Your DAQPad-6507 or DAQPad-6508 device is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge can damage several components on the device. To avoid such damage in handling the device, *never* touch the exposed pins of connectors.

Installation and Configuration

Chapter 2

This chapter describes how to install and configure the DAQPad-6507 and DAQPad-6508 devices.

Software Installation

You should install your software before you install your DAQPad-6507 or DAQPad-6508. If you are using LabVIEW, LabWindows/CVI, ComponentWorks, or VirtualBench, install this software before installing NI-DAQ driver software. Refer to your software release notes for your software for installation instructions.

☞ **Note** ***The DAQPad-6507/6508 devices require NI-DAQ 6.0 or 6.1 for Windows 95, or NI-DAQ 6.5 or later for Windows 98 (strongly recommended with USB). To ensure that you have the latest version of NI-DAQ, install it from the CD that ships with your device.***

To install NI-DAQ, refer to your NI-DAQ release notes. Find the installation section for your operating system and follow the instructions given there.

Hardware Installation

You can connect your DAQPad-6507 or DAQPad-6508 to any available USB socket. The following are general installation instructions, but consult your computer user manual or technical reference manual for specific instructions and warnings. Refer to Figure 2-1 to learn more about making connections for DAQPad-6507/6508 device.

The following are general installation instructions, but consult your personal computer user manual or technical reference manual for specific instructions and warnings.

☞ **Note** ***To ensure proper operation of your DAQPad device, follow the instructions in the sequence shown below. Otherwise, your DAQPad might not initialize properly, and***

you will need to turn off the DAQPad rocker switch and restart your DAQPad device again.

1. Connect the USB cable from the computer port or from any hub to the port on your DAQPad device. Refer to Figure 2-1 for more information on connections.

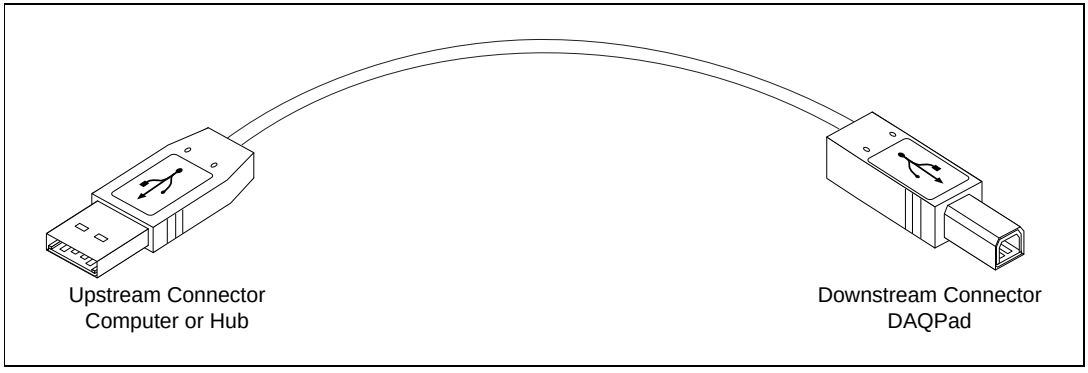


Figure 2-1. Connection between Your Computer or USB Hub and Your DAQPad Device

2. Flip the rocker switch to turn the power on for the DAQPad-6507 or DAQPad-6508. Your computer should detect your DAQPad device immediately, and when the computer recognizes your DAQPad device, the LED on the front panel blinks or lights up, depending on the status of your device.
3. If the LED comes on after the DAQPad is powered and connected to the host, it is functioning properly. Refer to Table 2-1 for LED pattern descriptions for your DAQPad device.
4. Configure your DAQPad device and any accessories with the NI-DAQ Configuration Utility.

When the LED blinks, it turns on and off for one second each for as many times as necessary, then waits three seconds before repeating the cycle.

Table 2-1. LED Patterns for DAQPad-6507/6508 States

LED	DAQPad-6507/6508 State	Description
Off	Off or in the low power, suspend mode	Your DAQPad device is turned off or in the low power, suspend mode.
2 blinks	Addressed state	This pattern is displayed if the host computer detects your DAQPad device but cannot configure it because there are no system resources available. If your DAQPad remains in this state, check your software installation.
3 blinks	Power supply failure	This pattern is displayed if you try to draw too much power from the USB. You must attach the external power supply.
4 blinks	General error state	If this pattern is displayed, contact National Instruments.
On	Configured state	Your DAQPad device is configured.

Note ***The DAQPad-6507/6508 devices use 100 kΩ resistors for polarity selection. These signals are controlled by a switch on the back of your DAQPad. For more information, see the Digital I/O State Selection section in Chapter 3, Signal Connections.***

Your DAQPad-6507/6508 device is now installed. Refer to Figure 2-2 to learn more about upstream and downstream connections between the host computer and the DAQPad-6507/6508 devices.

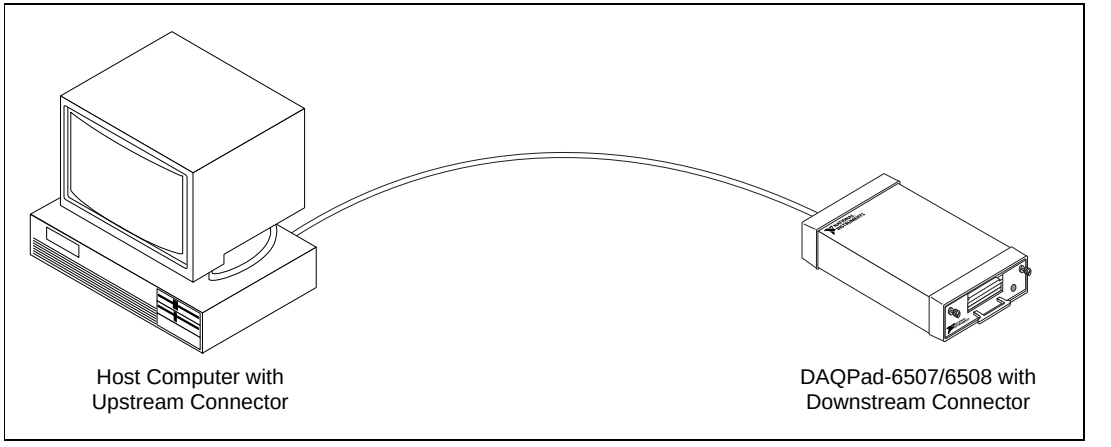


Figure 2-2. Upstream and Downstream Connections between the Host Computer and the DAQPad-6507 or DAQPad-6508

Configuration

The DAQPad-6507/6508 devices are completely software-configurable, hot Plug and Play instruments. The Plug and Play services query the instrument and allocate the required resources. The operating system enables the instrument for operation. Refer to your software documentation for more information.

Power Considerations

The DAQPad device remains powered up only when the USB cable connects it to the host computer and the computer is powered up. The host computer has the ability to go into a power-saving suspend mode. During this time, your DAQPad device can also go into a low-power mode, and the I/O signals remain in a fully powered, static state. The advantage of the low-power mode is that it conserves power. This mode is important if you are using a battery pack, even though all of the analog circuitry and digital I/O is powered off and the +5 V supply on the I/O connector is turned off in this state.

When the DAQPad exits the suspend mode, NI-DAQ will reinitialize your DAQPad device and all I/O signals to their default state, regardless of whether your DAQPad device is in low power mode or static mode. This action might change the current I/O states and gain if your DAQPad device is the low powered, static mode.

The default behavior of your DAQPad device is to go into powered, static state when the computer enters its suspend mode.

In the powered static state of your DAQPad device, you can draw current from the +5 V pin on the connector and all digital I/O lines and analog output channels will be static at a fixed voltage.

☞ **Note** ***Refer to the*** `Set_DAQ_Device_Info` ***function in the*** *NI-DAQ Function Reference Manual* ***to change the settings that determine the behavior of your DAQPad device during the suspend state.***

If low-power consumption is a concern, the recommended way to turn off your DAQPad device is with the rocker switch located on the rear panel. This switch turns your DAQPad device on and off by disconnecting both the external power supply and the USB supply.

It is also possible to turn off your DAQPad device by detaching the USB cable while leaving the external supply attached; however, several milliamperes are continually drawn from the external supply in this case, although no power is drawn from the USB supply. If you are using a battery pack, such as the BP-1, it is best to use the rocker switch on the back panel to prolong the charge of the battery.

Chapter 3

Signal Connections

This chapter includes timing specifications and signal connection instructions for the DAQPad-6507 and DAQPad-6508 I/O connectors.

Caution ***Connections that exceed any of the maximum ratings of input or output signals on the DAQPad-6507/6508 devices can damage the device and the computer. The description of each signal in this section includes information about maximum input ratings. National Instruments is not liable for any damages resulting from any inaccurate signal connections.***

To learn more about screw terminal assignments on the DAQPad-6507, refer to Figure 3-1.

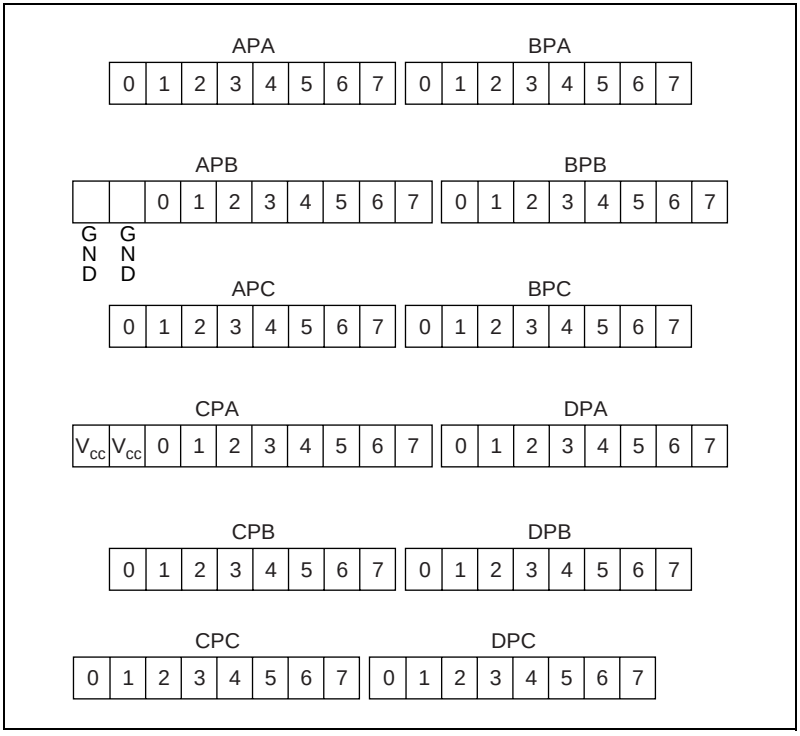
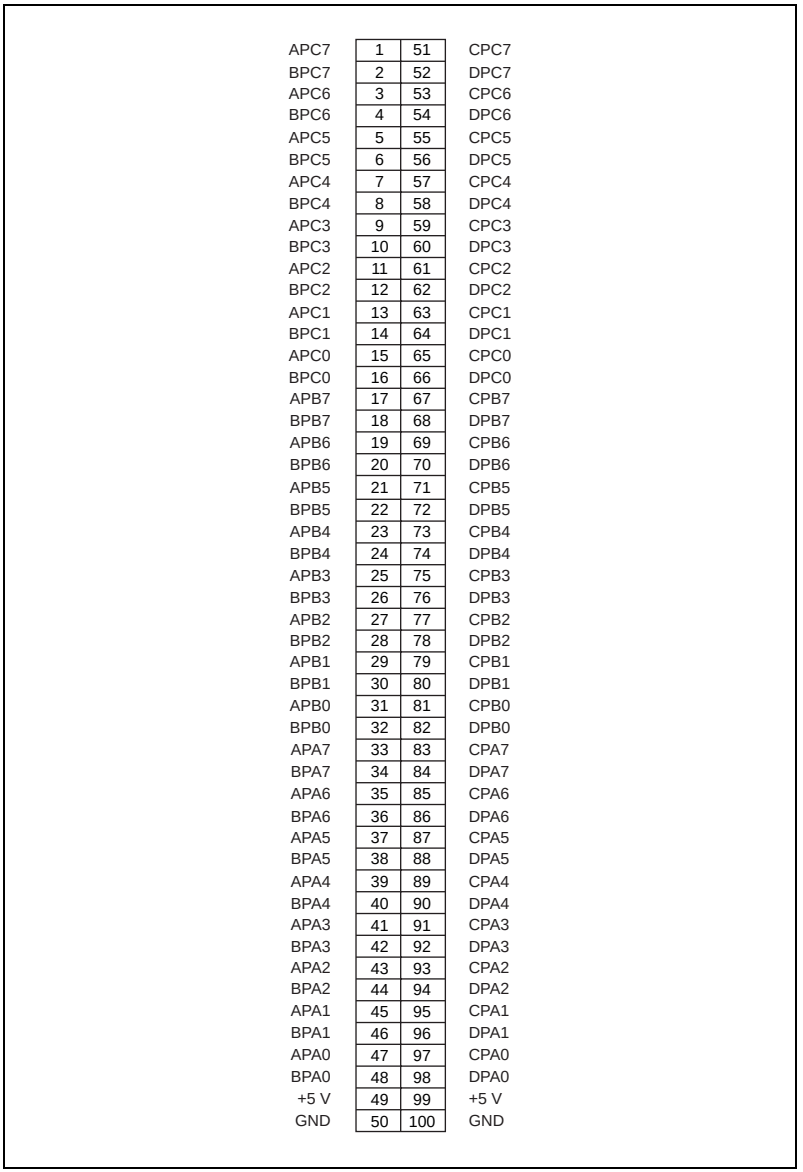


Figure 3-1. Screw Terminal Assignments for the DAQPad-6507

I/O Connector Pin Description

Figure 3-2 shows the pin assignments for the DAQPad-6507/6508 digital I/O connector.



APC7	1	51	CPC7
BPC7	2	52	DPC7
APC6	3	53	CPC6
BPC6	4	54	DPC6
APC5	5	55	CPC5
BPC5	6	56	DPC5
APC4	7	57	CPC4
BPC4	8	58	DPC4
APC3	9	59	CPC3
BPC3	10	60	DPC3
APC2	11	61	CPC2
BPC2	12	62	DPC2
APC1	13	63	CPC1
BPC1	14	64	DPC1
APC0	15	65	CPC0
BPC0	16	66	DPC0
APB7	17	67	CPB7
BPB7	18	68	DPB7
APB6	19	69	CPB6
BPB6	20	70	DPB6
APB5	21	71	CPB5
BPB5	22	72	DPB5
APB4	23	73	CPB4
BPB4	24	74	DPB4
APB3	25	75	CPB3
BPB3	26	76	DPB3
APB2	27	77	CPB2
BPB2	28	78	DPB2
APB1	29	79	CPB1
BPB1	30	80	DPB1
APB0	31	81	CPB0
BPB0	32	82	DPB0
APA7	33	83	CPA7
BPA7	34	84	DPA7
APA6	35	85	CPA6
BPA6	36	86	DPA6
APA5	37	87	CPA5
BPA5	38	88	DPA5
APA4	39	89	CPA4
BPA4	40	90	DPA4
APA3	41	91	CPA3
BPA3	42	92	DPA3
APA2	43	93	CPA2
BPA2	44	94	DPA2
APA1	45	95	CPA1
BPA1	46	96	DPA1
APA0	47	97	CPA0
BPA0	48	98	DPA0
+5 V	49	99	+5 V
GND	50	100	GND

Figure 3-2. Digital I/O Connector Pin Assignments for the DAQPad-6508

I/O Connector Signal Connection Descriptions

Refer to Table 3-1 for pin assignments for the DAQPad-6508.

Table 3-1. Pin Assignments for the DAQPad-6508

Pin	Signal Name	Description
1, 3, 5, 7, 9, 11, 13, 15	APC<7..0>	Bidirectional Data Lines for Port C of PPI A—APC7 is the MSB, APC0 the LSB.
17, 19, 21, 23, 25, 27, 29, 31	APB<7..0>	Bidirectional Data Lines for Port B of PPI A—APB7 is the MSB, APB0 the LSB.
33, 35, 37, 39, 41, 43, 45, 47	APA<7..0>	Bidirectional Data Lines for Port A of PPI A—APA7 is the MSB, APA0 the LSB.
2, 4, 6, 8, 10, 12, 14, 16	BPC<7..0>	Bidirectional Data Lines for Port C of PPI B—BPC7 is the MSB, BPC0 the LSB.
18, 20, 22, 24, 26, 28, 30, 32	BPB<7..0>	Bidirectional Data Lines for Port B of PPI B—BPB7 is the MSB, BPB0 the LSB.
34, 36, 38, 40, 42, 44, 46, 48	BPA<7..0>	Bidirectional Data Lines for Port A of PPI B—BPA7 is the MSB, BPA0 the LSB.
51, 53, 55, 57, 59, 61, 63, 65	CPC<7..0>	Bidirectional Data Lines for Port C of PPI C—CPC7 is the MSB, CPC0 the LSB.
67, 69, 71, 73, 75, 77, 79, 81	CPB<7..0>	Bidirectional Data Lines for Port B of PPI C—CPB7 is the MSB, CPB0 the LSB.
83, 85, 87, 89, 91, 93, 95, 97	CPA<7..0>	Bidirectional Data Lines for Port A of PPI C—CPA7 is the MSB, CPA0 the LSB.
52, 54, 56, 58, 60, 62, 64, 66	DPC<7..0>	Bidirectional Data Lines for Port C of PPI D—DPC7 is the MSB, DPC0 the LSB.
68, 70, 72, 74, 76, 78, 80, 82	DPB<7..0>	Bidirectional Data Lines for Port B of PPI D—DPB7 is the MSB, DPB0 the LSB.
84, 86, 88, 90, 92, 94, 96, 98	DPA<7..0>	Bidirectional Data Lines for Port A of PPI D—DPA7 is the MSB, DPA0 the LSB.
49, 99	+5 V	+5 V—These pins are connected to the DAQPad's +5 VDC supply.
50, 100	GND	Ground—These pins are connected to the computer's ground signal.
Note: Pins 49 and 99 are connected to the +5 V PC power supply via a 1 A self-resetting fuse.		

Port C Pin Assignments

The signals assigned to port C depend on the mode in which the 82C55A is programmed in your application software. In mode 0, port C is considered as two 4-bit I/O ports. In modes 1 and 2, port C is used for status and handshaking signals with zero, two, or three lines available for general-purpose input/output. Table 3-2 summarizes the signal assignments of port C for each programmable mode.

Caution ***During programming, be aware that each time a port is configured, output ports A and C are reset to 0, and output port B is undefined.***

Table 3-2. Port C Signal Assignments

Programming Mode	Group A					Group B		
	PC7	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O
* Indicates that the signal is active low; refer to Table 3-3 for signal name definitions.								

Cable Assembly Connectors

The cable assembly referred to in the *Optional Equipment* section in Chapter 1, *Introduction*, is an assembly of two 50-pin cables and three connectors. Both cables are joined to a single connector on one end and to individual connectors on the free ends. The 100-pin connector that joins the two cables plugs into the I/O connector of the DAQPad-6508. The other two connectors are 50-pin connectors, one of which is connected to pins 1 through 50, and the other is connected to pins 51 through 100 of the DAQPad-6508 I/O connector. The cables are labelled Position 1-50 and 51-100, respectively. Figures 3-3 and 3-4 show the pin assignments for the 50-pin connectors on the cable assembly.

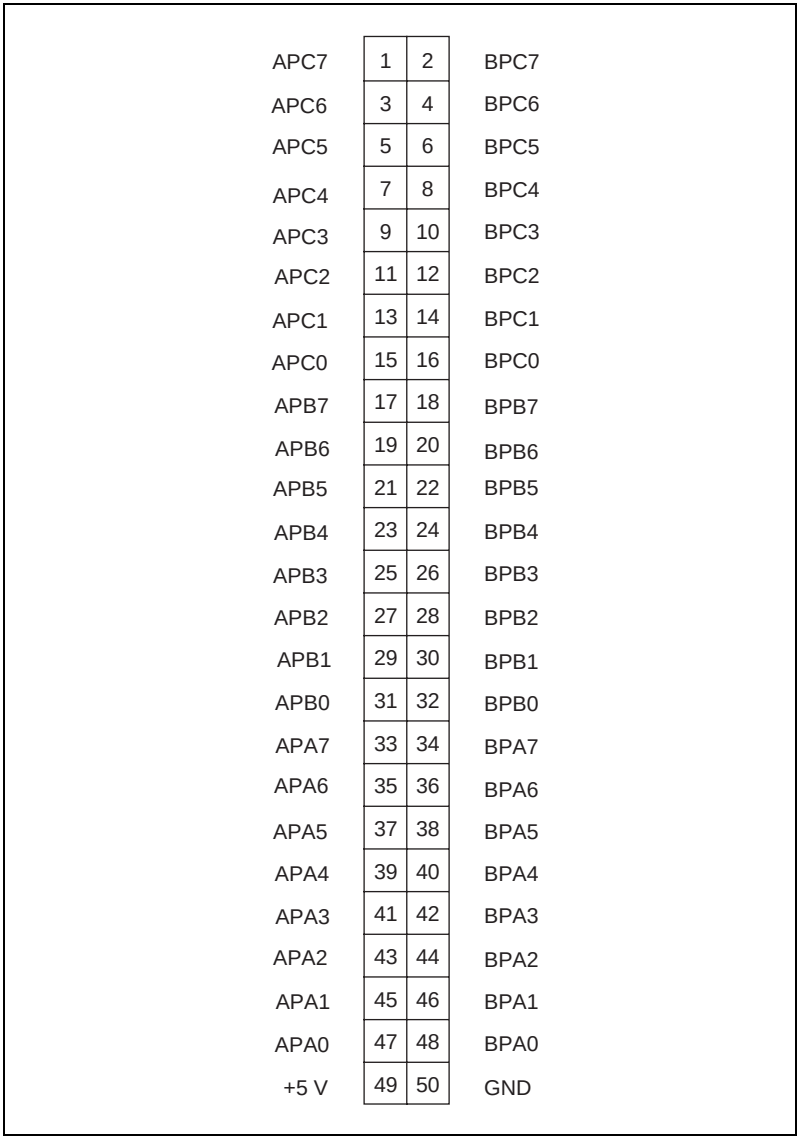
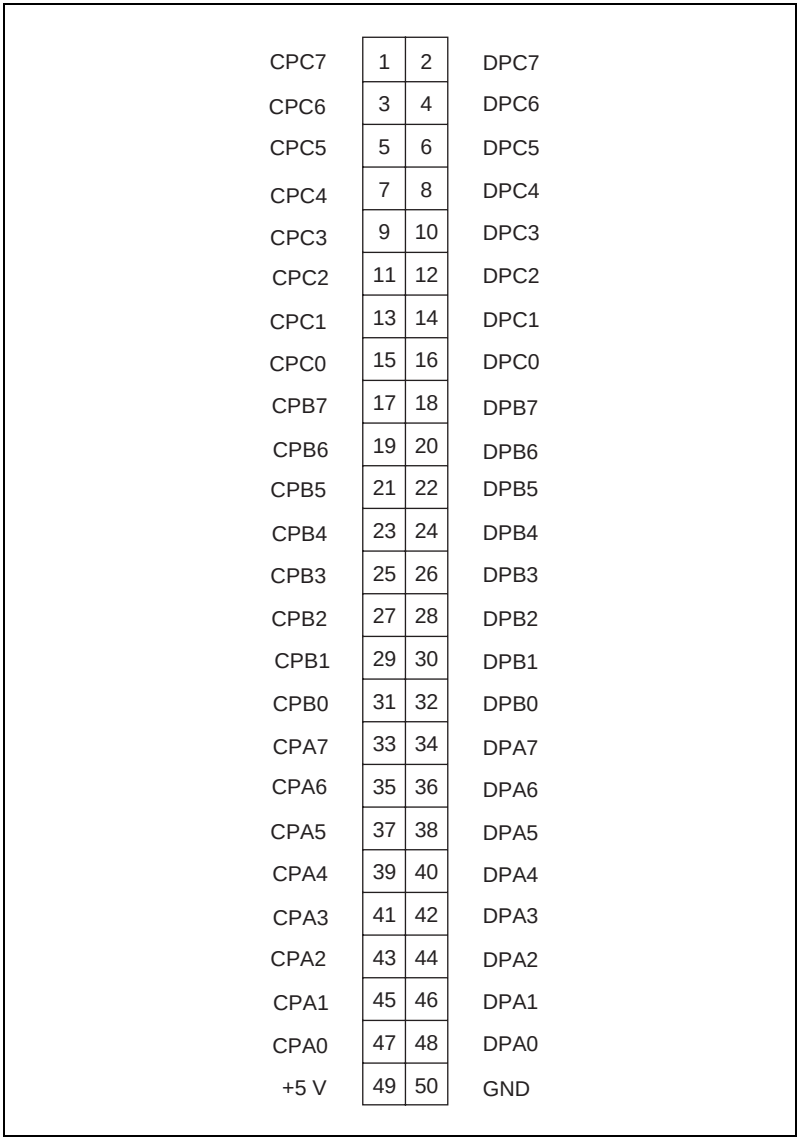


Figure 3-3. Cable Assembly Connector Pin Assignments for Pins 1 through 50 of the DAQPad-6508 I/O Connector



CPC7	1	2	DPC7
CPC6	3	4	DPC6
CPC5	5	6	DPC5
CPC4	7	8	DPC4
CPC3	9	10	DPC3
CPC2	11	12	DPC2
CPC1	13	14	DPC1
CPC0	15	16	DPC0
CPB7	17	18	DPB7
CPB6	19	20	DPB6
CPB5	21	22	DPB5
CPB4	23	24	DPB4
CPB3	25	26	DPB3
CPB2	27	28	DPB2
CPB1	29	30	DPB1
CPB0	31	32	DPB0
CPA7	33	34	DPA7
CPA6	35	36	DPA6
CPA5	37	38	DPA5
CPA4	39	40	DPA4
CPA3	41	42	DPA3
CPA2	43	44	DPA2
CPA1	45	46	DPA1
CPA0	47	48	DPA0
+5 V	49	50	GND

Figure 3-4. Cable Assembly Connector Pin Assignments for Pins 51 through 100 of the DAQPad-6508 I/O Connector

Digital I/O Signal Connections

Pins 1 through 48 and pins 51 through 98 of the I/O connector are digital I/O signal pins. Figure 3-5 depicts signal connections for three typical digital I/O applications.

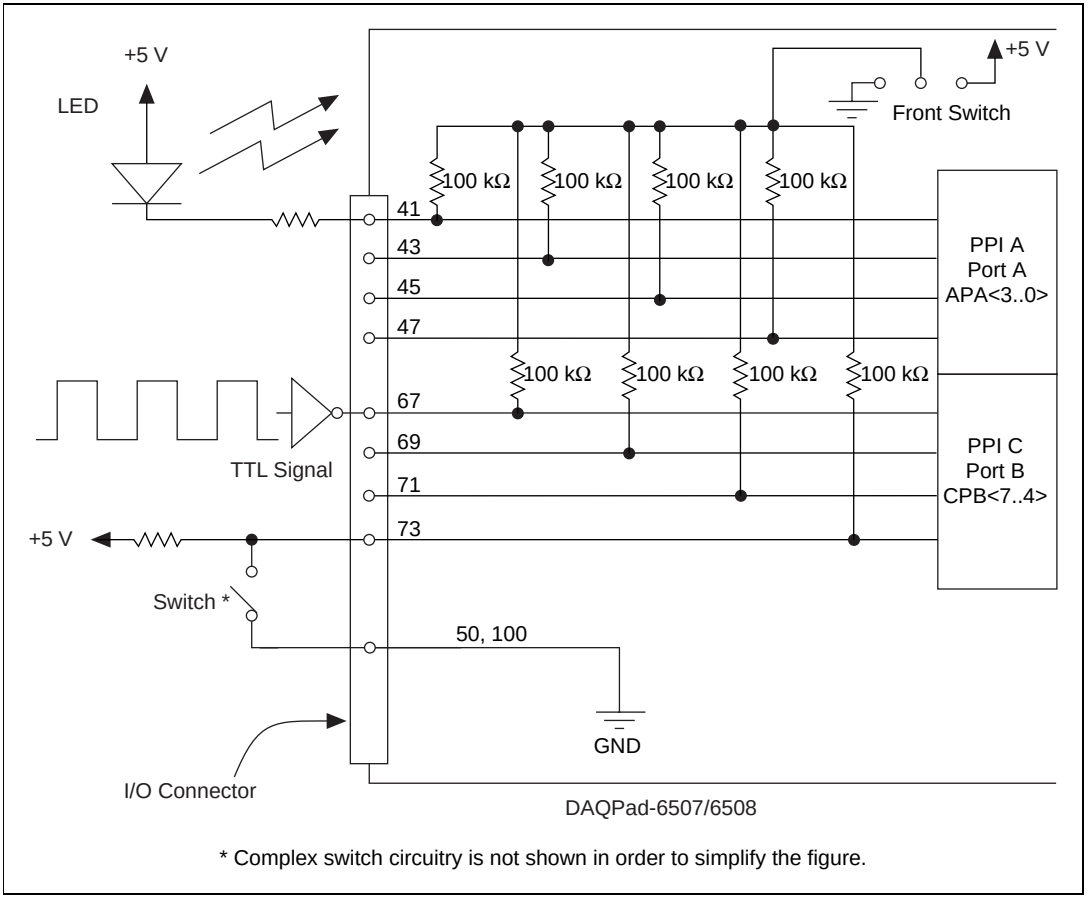


Figure 3-5. Digital I/O Connections

In Figure 3-5, PPI A, port A is configured for digital output, and PPI C, port B is configured for digital input. Digital input applications include receiving TTL signals and sensing external device states, such as the state of the switch in Figure 3-5. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 3-5.

Power Connections

Two pins on the I/0 connector supply +5 V from your DAQPad device's power supply through a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. These two pins are referenced to DGND and can be used to power external digital circuitry.The power rating is indicated below.

Power rating: +4.65 VDC to +5.25 VDC at 1 A combined total for both pins

Caution ***Never connect the +5 V power pins (pins 49 and 99) directly to analog or digital ground or to any other voltage source on your DAQPad device or any other device. Doing so can damage your DAQPad device and the computer. National Instruments is*** *not* ***liable for damages resulting from such a connection.***

Pins 49 and 99 of the I/O connector are connected to the +5 V supply of the DAQPad-6507/6508 devices. You can power the DAQPad-6507 or DAQPad-6508 from either USB power or an external source. The DAQPad uses USB power when the external source is not plugged in. USB power limits any device from using more than 0.5 A. If you are running from USB power (that is, if your external power source is not plugged in), you have only 150 mA to drive signals and supply power for your circuitry. If you require more power than 150 mA, attach the external power source. Also, your host computer might turn off power to your DAQPad device if no activity is detected. This cuts the power to any external circuitry powered by your DAQPad device if you are not using an external power source. Refer to *Power Considerations*, in Chapter 2, *Installation and Configuration*, of this manual.

Connecting Power Sources to Digital I/O Lines

Caution ***Always turn your DAQPad on before applying external power to the digital I/O (DIO) lines. If your DAQPad is off and external power is applied to the DIO lines, your DAQPad may be damaged. National Instruments is*** *not* ***liable for damage caused by incorrect power sequencing.***

When supplying power to DIO lines, we strongly recommend you use the +5 V source from the DAQPad. If you must use an external power source, it is important to sequence the power correctly—DAQPad first, then external power—to prevent damage to the CMOS circuits. Because of a trait common to all CMOS circuits, applying external power first may cause current to flow incorrectly, damaging the circuit.

Digital I/O State Selection

You can power up the digital I/O lines for the DAQPad-6507/6508 devices in a user-defined state. The DAQPad-6507/6508 devices facilitate user-configurable pull-up or pull-down tasks. Each DIO channel is connected to a 100 kΩ resistor and can be pulled high or low using the front panel switch. You can use this switch to pull all 96 DIO lines high or low, or you can allow the lines to float. However, if all lines are high, you might want to pull some lines low. To do this properly, you must understand the nature of the drive current on those lines and adhere to TTL logic levels, or you can let the lines float and tie them all high or low as necessary.

High DIO State

If you select the pulled-high mode, each DIO line will be pulled to V_{CC} (+5 VDC) with a 100 kΩ resistor. To pull a specific line low, connect between that line and ground and use a pull-down resistor (R_L) whose value will give you a maximum of 0.4 VDC. The DIO lines provide a maximum of 2.5 mA at 3.7 V in the high state. Use the largest possible resistor so that you do not use more current than necessary to perform the pull-down task.

Also, make sure the resistor value is not so large that leakage current from the DIO line along with the current from the 100 kΩ pull-up resistor drives the voltage at the resistor above a TTL low level of 0.4 VDC.

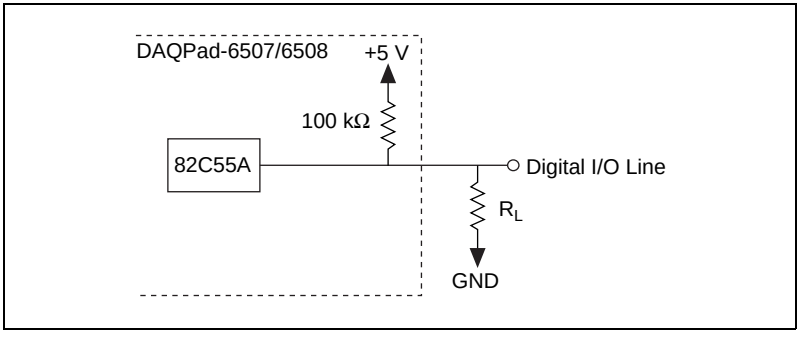


Figure 3-6. DIO Channel Configured for High DIO State with External Load

Example:
At power up, the device is configured for input and, by default, all DIO lines are high. To pull one channel low, follow these steps:

1. Install a load (R_L). Remember that the smaller the resistance, the greater the current consumption and the lower the voltage (V).
2. Using the following formula, calculate the largest possible load to maintain a logic low level of 0.4 V and supply the maximum driving current (I).

   $V = I * R_L \Rightarrow R_L = V / I$, where:

   V= 0.4 V is the voltage across R_L

   I = 46 µA + 10 µA is the 4.6 V across the 100 kΩ pull-up resistor and 10 µA from 82C55 leakage current

   Therefore:

   R_L = 7.1 kΩ is the 0.4 V / 56 µA

This resistor value, 7.1 kΩ, provides a maximum of 0.4 V on the DIO line at power up. You can substitute smaller resistor values, but they will draw more current, leaving less drive current for other circuitry connected to this line. The 7.1 kΩ resistor reduces the amount of a logic high source current by 0.4 mA with a 2.8 V output.

Low DIO State

If you select pulled-low mode, each DIO line will be pulled to GND (0 VDC) using a 100 kΩ resistor. If you want to pull a specific line high, connect a pull-up resistor that gives you a minimum of 2.8 VDC. The DIO lines are capable of sinking a maximum of 2.5 mA at 0.4 V in the low state. Use the largest possible resistance value so that you do not use more current than necessary to perform the pull-up task.

Also, make sure the pull-up resistor value is not so large that leakage current from the DIO line along with the current from the 100 kΩ pull-down resistor brings the voltage at the resistor below a TTL-high level of 2.8 VDC.

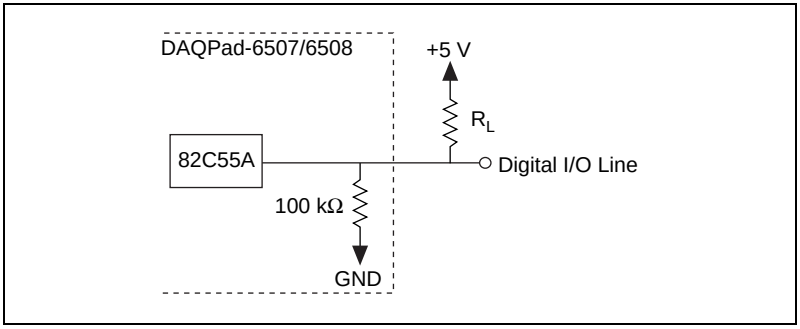


Figure 3-7. DIO Channel Configured for Low DIO State with External Load

Example:
The switch is set in the low DIO state, which means all DIO lines are pulled low. If you want to pull one channel high, follow these steps:

1. Install a load (R_L). Remember that the smaller the resistance, the greater the current consumption and the lower the voltage (V).
2. Using the following formula, calculate the largest possible load to maintain a logic high level of 2.8 V and supply the maximum sink current (I).

   $V = I * R_L \Rightarrow R_L = V / I$, where:

   $V = 2.2$ V is the voltage across R_L

   $I = 28\ \mu A + 10\ \mu A$ is the 2.8 V across the 100 kΩ pull-up resistor and 10 μA from 82C55A leakage current

   Therefore:

   $R_L = 5.7$ kΩ is the 2.2 V / 38 μA

This resistor value, 5.7 kΩ, provides a minimum of 2.8 V on the DIO line at power up. You can substitute smaller resistor values but they draw more current, leaving less sink current for other circuitry connected to this line. The 5.7 kΩ resistor reduces the amount of a logic low sink current by 0.8 mA with a 0.4 V output.

Floating DIO State

The DIO lines are not pulled high or low by your DAQPad device in this configuration. Use an external 100 kΩ resistor to pull the line to the state you want.

Timing Specifications

This section lists the timing specifications for handshaking with the DAQPad-6507/6508 devices. The handshaking lines STB* and IBF synchronize input transfers. The handshaking lines OBF* and ACK* synchronize output transfers.

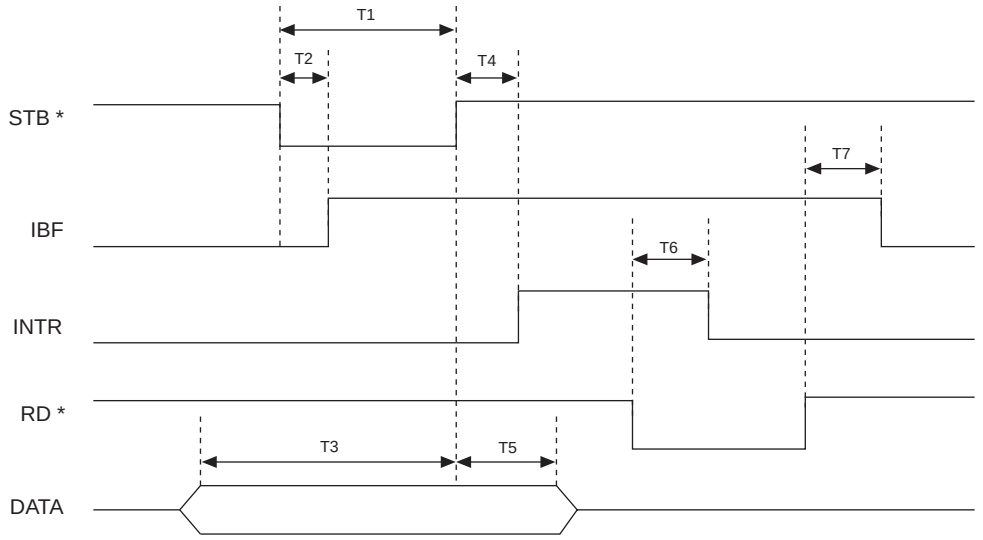
The signals in Table 3-3 are used in the timing diagrams later in this chapter.

Table 3-3. Timing Signal Descriptions

Name	Type	Description
STB*	Input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. This is an input acknowledge signal.
ACK*	Input	Acknowledge Input—A low signal on this handshaking line indicates that the data written to the port has been accepted. This signal is a response from the external device indicating that it has received the data from the DAQPad-6507/6508 devices.
OBF*	Output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written to the port.
INTR	Output	Interrupt Request—This signal becomes high when the 82C55A requests service during a data transfer. The appropriate interrupt enable bits must be set to generate this signal.
RD*	Internal	Read Signal—This signal is the read signal generated from the control lines of the computer I/O expansion bus.
WR*	Internal	Write Signal—This signal is the write signal generated from the control lines of the computer I/O expansion bus.
DATA	Bidirectional	Data Lines at the Specified Port—This signal indicates the availability of data on the data lines at a port that is in the output mode. If the port is in the input mode, this signal indicates when the data on the data lines should be valid.

Mode 1 Input Timing

The following figure illustrates the timing specifications for an input transfer in mode 1.

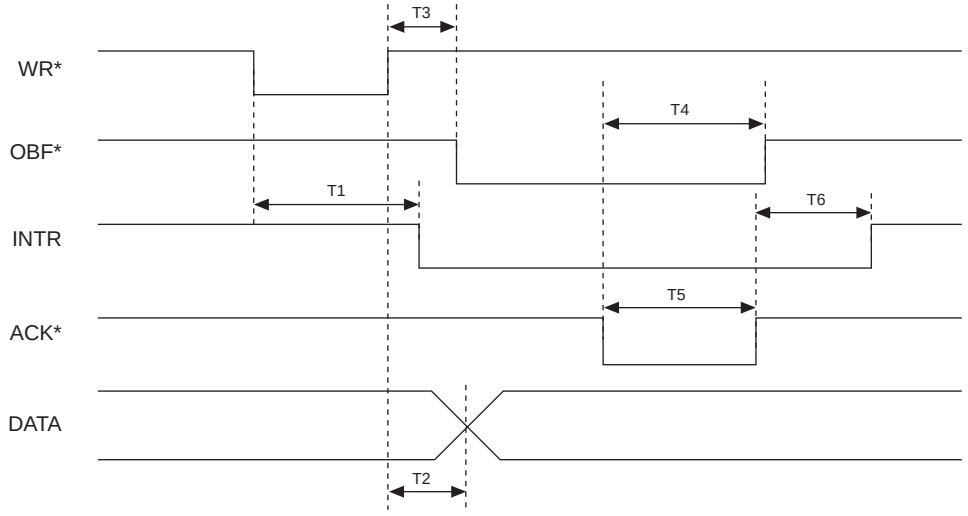


Name	Description	Minimum	Maximum
T1	STB* pulse width	100	—
T2	STB* = 0 to IBF = 1	—	150
T3	Data before STB* = 1	20	—
T4	STB* = 1 to INTR = 1	—	150
T5	Data after STB* = 1	50	—
T6	RD* = 0 to INTR = 0	—	200
T7	RD* = 1 to IBF = 0	—	150

All timing values are in nanoseconds.

Mode 1 Output Timing

The following figure illustrates the timing specifications for an output transfer in mode 1.

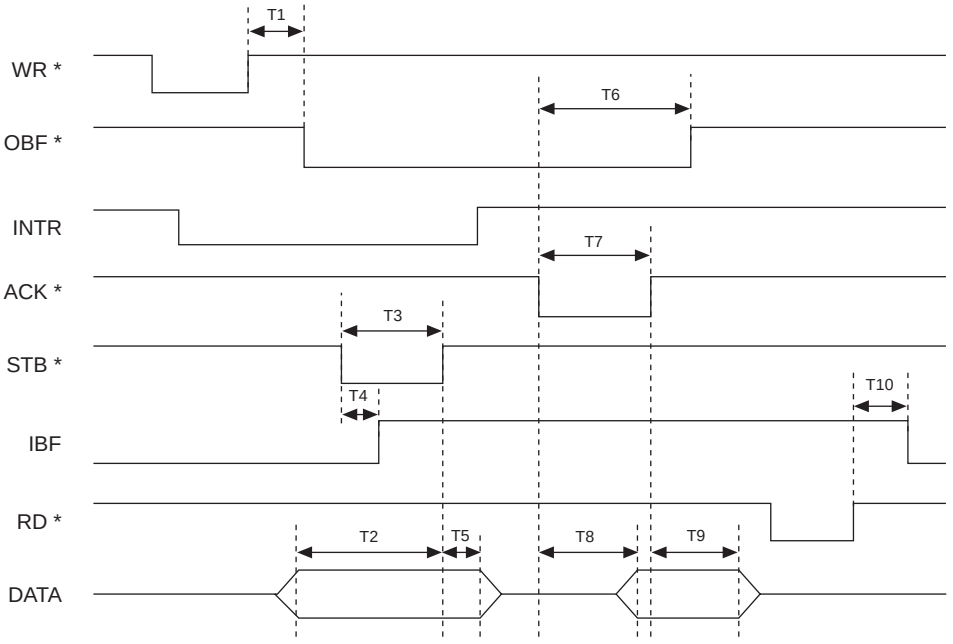


Name	Description	Minimum	Maximum
T1	WR* = 0 to INTR = 0	—	250
T2	WR* = 1 to output	—	200
T3	WR* = 1 to OBF* = 0	—	150
T4	ACK* = 0 to OBF* = 1	—	150
T5	ACK* pulse width	100	—
T6	ACK* = 1 to INTR = 1	—	150

All timing values are in nanoseconds.

Mode 2 Bidirectional Timing

The following figure illustrates the timing specifications for bidirectional transfers in mode 2.



Name	Description	Minimum	Maximum
T1	WR* = 1 to OBF* = 0	—	150
T2	Data before STB* = 1	20	—
T3	STB* pulse width	100	—
T4	STB* = 0 to IBF = 1	—	150
T5	Data after STB* = 1	50	—
T6	ACK* = 0 to OBF = 1	—	150
T7	ACK* pulse width	100	—
T8	ACK* = 0 to output	—	150
T9	ACK* = 1 to output float	20	250
T10	RD* = 1 to IBF = 0	—	150

All timing values are in nanoseconds.

Chapter 4

Theory of Operation

This chapter contains a functional overview of the DAQPad-6507/6508 devices and explains the operation of each functional unit making up the DAQPad-6507 or DAQPad-6508.

The block diagram in Figure 4-1 illustrates the key functional components of the DAQPad-6507/6508 devices.

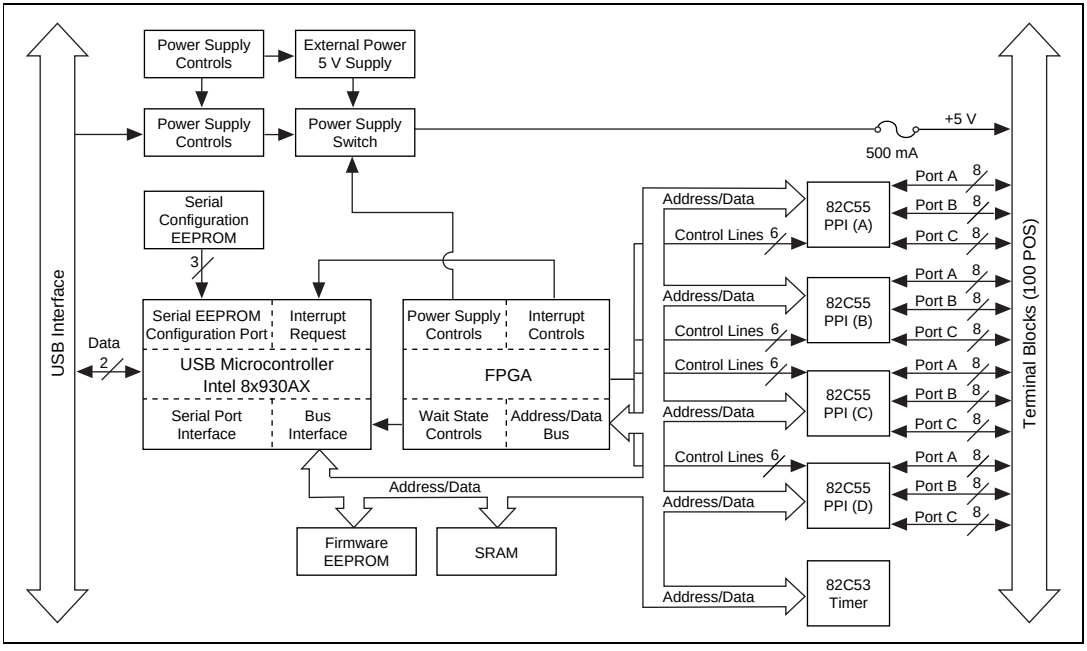


Figure 4-1. DAQPad-6507/6508 Devices Block Diagram

Interrupt Control Circuitry

Interrupt control circuitry enables and disables interrupts. Two software-controlled registers determine which devices, if any, generate interrupts in the interrupt circuitry of the DAQPad-6507/6508 devices. Each of the four 82C55A devices has two interrupt lines, PC3 and PC0, connected to the interrupt circuitry.

Each of the eight interrupt lines can interrupt the host computer if the interrupt circuitry is enabled and the corresponding enable bit is set. Normally, PC3 and/or PC0 of the 82C55A devices are controlled by the handshaking circuitry; however, you can configure and use either of these two lines for input and external interrupts. An interrupt occurs on the low-to-high transition of the signal line. Refer to Appendix B, *OKI 82C55A Data Sheet* for more information.

USB Microcontroller

The USB controller is a special microcontroller that has circuitry necessary to transmit and receive data over USB itself. It maintains information about the status of the bus and follows the USB protocol to acquire and send information over the bus. The microcontroller receives instruction codes over USB, parses the instructions, and executes them. NI-DAQ handles all interaction with the microcontroller.

82C55A Programmable Peripheral Interface

The four 82C55A PPI chips are the heart of the DAQPad-6507/6508 devices. Each of these chips has 24 programmable I/O pins that represent three 8-bit ports: PA, PB, and PC. Each port can be programmed as an input or an output port. The 82C55A has three modes of operation: simple I/O (mode 0), strobed I/O (mode 1), and bidirectional I/O (mode 2). In modes 1 and 2, the three ports are divided into two groups: group A and group B. Each group has eight data bits and four control and status bits from port C (PC). Modes 1 and 2 use handshaking signals from port C to synchronize data transfers. Refer to Appendix B, *OKI 82C55A Data Sheet*, for more detailed information.

Digital I/O Connector

All digital I/O is transmitted through a standard, 100-pin, female connector for the DAQPad-6508 or 100-pin screw terminal with a strain-relief clamp for the DAQPad-6507. Pins 49 and 99 are connected to +5 V through a self-restarting protection fuse (F1). See Figure 4-1 for its location. This +5 V supply is often required to operate I/O module mounting racks. Pins 50 and 100 are connected to ground. See the *Optional Equipment* section in Chapter 1, *Introduction*, as well as Chapter 2, *Installation and Configuration*, and the *Digital I/O Signal Connections* section in Chapter 3, *Signal Connections*, for additional information.

Specifications

Appendix
A

This appendix lists the specifications of the DAQPad-6507/6508 devices. These specifications are typical at 25° C, unless otherwise stated. The operating temperature range is 0° to 70° C.

Digital I/O

Number of channels ..... 96 I/O

Compatibility ..... TTL

Absolute max voltage rating ..... –0.5 to +5.5 V with respect to GND

Handshaking..... Requires 1 port

Power-on state..... Configured as inputs, high (selectable on the front panel switch)

Data transfers ..... Interrupts, programmed I/O

Digital logic levels

Level	Min	Max
Input low voltage	–0.3 V	0.8 V
Input high voltage	2.2 V	5.3 V
Input low current (V_{in}= 0.8 V)	—	–1.0 µA
Input high current (V_{in}= 2.4 V)	—	1.0 µA
Output low voltage (I_{out} = 2.5 mA)	0 V	0.4 V
Output high voltage (I_{out}= -2.5 mA)	3.7 V	5.0 V
Input current (0 < V_{in} < 5 V)	–1.0 µA	1.0 µA

Output signals

Pin 49 and pin 99 (at +5 V) .....0.5 A max

Note ***The total combined current output from pins 49 and 99 may be limited by the available current from the USB. If you do not have the external power supply connected, you have only 150 mA of current available to drive all outputs, including DIO lines.***

Transfer rates .....Up to 60 S/s

Power Requirement

External

9 to 30 VDC.....12 W max

USB

4.40 to 5.25 VDC.....220 mA typ, 500 mA max

Physical

Dimensions .....22.9 by 14.6 cm (9.0 by 5.7 in.)

I/O connector

DAQPad-6507 .....100-screw terminals

DAQPad-6508 .....100-pin female, 0.050 series D-type

Environment

Operating temperature .....0° to 70° C

Storage temperature.....–55° to 150° C

Relative humidity .....5% to 90% noncondensing

OKI 82C55A Data Sheet

Appendix
B

This appendix contains the manufacturer data sheet for the OKI 82C55A[1] (OKI Semiconductor) CMOS programmable peripheral interface. This interface is used on the DAQPad-6507/6508 devices.

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OKI semiconductor

MSM82C55A-2RS/GS/VJS

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

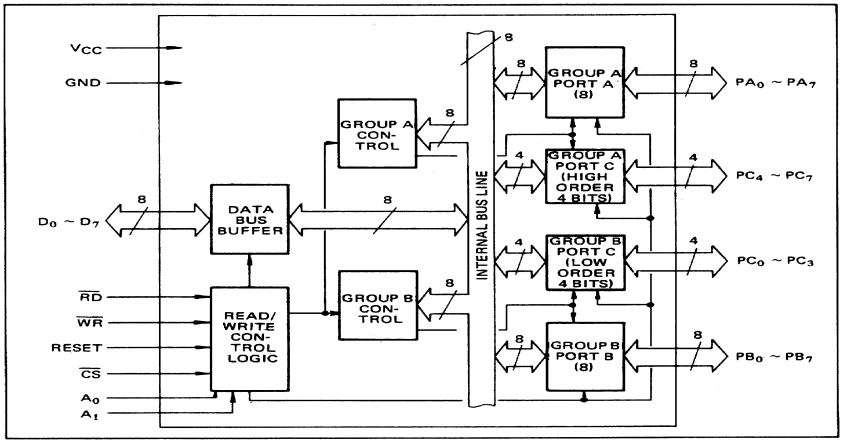
GENERAL DESCRIPTION

The MSM82C55A is a programmable universal I/O interface device which operates as high speed and on low power consumption due to 3 μ silicon gate CMOS technology. It is the best fit as an I/O port in a system which employs the 8-bit parallel processing MSM80C85A CPU. This device has 24-bit I/O pins equivalent to three 8-bit I/O ports and all inputs/outputs are TTL interface compatible.

FEATURES

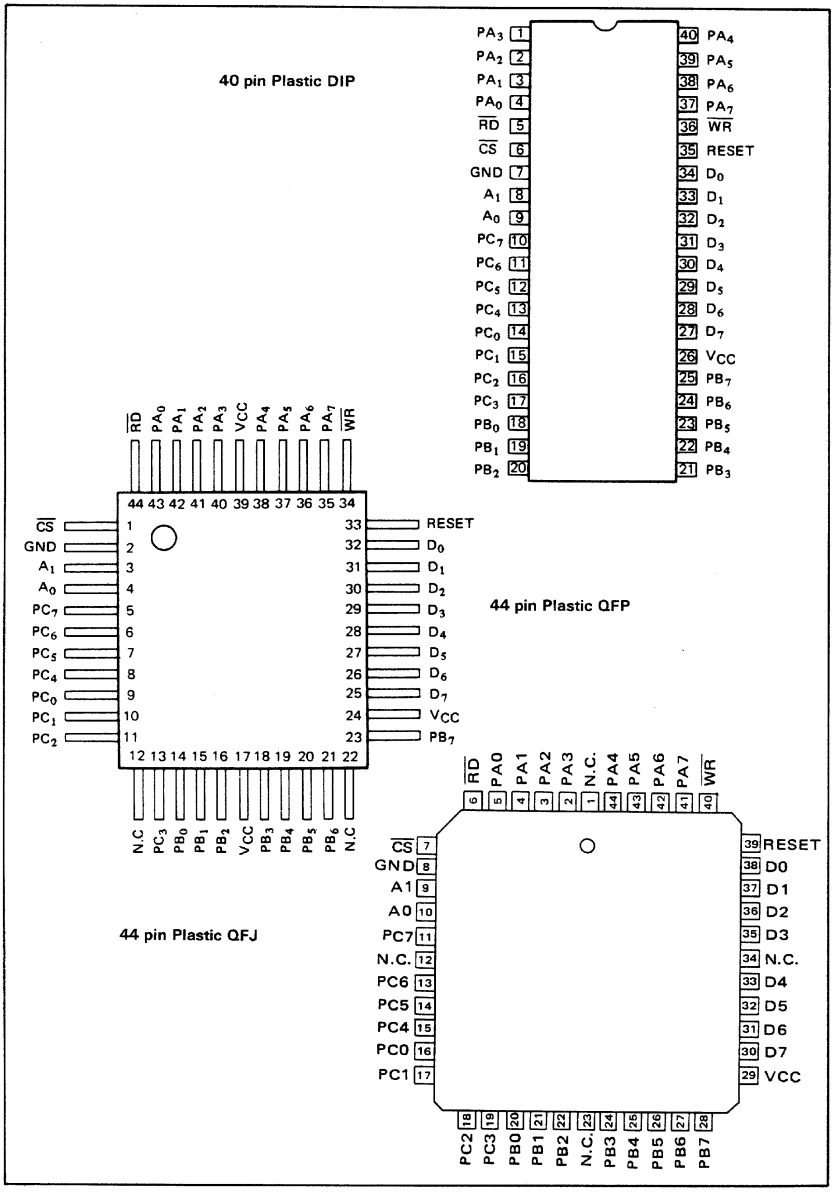
- High speed and low power consumption due to 3μ silicon gate CMOS technology
- 3V to 6V single power supply
- Full static operation
- Programmable 24-bit I/O ports
- Bidirectional bus operation (Port A)
- Bit set/reset function (Port C)
- TTL compatible
- Compatible with 8255A-5
- 40 pin Plastic DIP (DIP40-P-600): MSM82C55A-2RS
- 44 pin Plastic QFJ (QFJ44-P-S650): MSM82C55A-2JS
- 44 pin Plastic QFP (QFP44-P-910-2K): MSM82C55A-2GS-2K

CIRCUIT CONFIGURATION



■ I/O-MSM82C55A-2RS/GS/VJS ■

PIN CONFIGURATION (Top View)



■ I/O-MSM82C55A-2RS/GS/VJS ■

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C55A-2RS	MSM82C55A-2GS	MSM82C55A-2VJS	
Ssupply Voltage	V_{CC}	Ta = 25°C with respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V.
Storage Temperature	T_{stg}	—	−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	−40 to 85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	-0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		MSM82C55A-2			Unit
				Min.	Typ.	Max.	
"L" Output Voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC} = 4.5V to 5.5V Ta = −40°C to +85°C (C_L = 0pF)			0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = -40 μA		4.2			V
		I_{OH} = -2.5 mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		-1		1	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		-10		10	μA
Supply Current (standby)	I_{CCS}	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IH} \geq V_{CC}$ -0.2V $V_{IL} \leq 0.2V$			0.1	10	μA
Average Supply Current (active)	I_{CC}	I/O wire cycle 82C55A-2 ... 8MHzCPU timing				8	mA

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AC CHARACTERISTICS

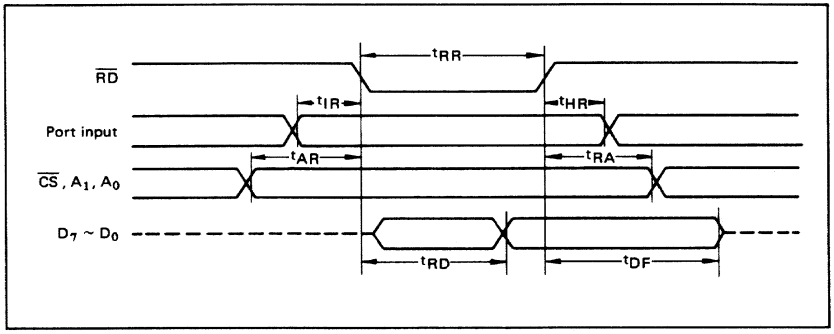
(V_{CC} = 4.5 to 5.5V, Ta = -40 to +80°C)

Parameter	Symbol	MSM82C55A-2		Unit	Remarks
		Min.	Max.		
Setup Time of address to the falling edge of $\overline{RD}$	t_{AR}	20		ns	
Hold Time of address to the rising edge of $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	100		ns	
Delay Time from the falling edge of $\overline{RD}$ to the output of defined data	t_{RD}		120	ns	
Delay Time from the rising edge of $\overline{RD}$ to the floating of data bus	t_{DF}	10	75	ns	
Time from the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next falling edge of $\overline{RD}$ or $\overline{WR}$	t_{RV}	200		ns	
Setup Time of address before the falling edge of $\overline{WR}$	t_{AW}	0		ns	
Hold Time of address after the rising edge or $\overline{WR}$	t_{WA}	20		ns	
$\overline{WR}$ Pulse Width	t_{WW}	150		ns	
Setup Time of bus data before the rising edge of $\overline{WR}$	t_{DW}	50		ns	
Holt Time of bus data after the rising edge of $\overline{WR}$	t_{WD}	30		ns	
Delay Time from the rising edge of $\overline{WR}$ to the output of defined data	t_{WB}		200	ns	
Setup Time of port data before the falling edge of $\overline{RD}$	t_{IR}	20		ns	
Hold Time of port data after the rising edge of $\overline{RD}$	t_{HR}	10		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	100		ns	
$\overline{STB}$ Pulse Width	t_{ST}	100		ns	Load 150 pF
Setup Time of port data before the rising edge of $\overline{STB}$	t_{PS}	20		ns	
Hold Time of port data after the rising edge of $\overline{STB}$	t_{PH}	50		ns	
Delay Time from the falling edge of $\overline{ACK}$ to the output of defined data	t_{AD}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the floating of port (Port A in mode 2)	t_{KD}	20	250	ns	
Delay Time from the rising edge of WR to the falling edge of $\overline{OBF}$	t_{WOB}		150	ns	
Delay Time from the falling edge of ACK to the rising edge of $\overline{OBF}$	t_{AOB}		150	ns	
Delay Time from the falling edge of STB to the rising edge of IBF	t_{SIB}		150	ns	
Delay Time from the rising edge of $\overline{RD}$ to the falling edge of IBF	t_{RIB}		150	ns	
Delay Time from the falling edge of $\overline{RD}$ to the falling edge of INTR	t_{RIT}		200	ns	
Delay Time from the rising edge of $\overline{STB}$ to the rising edge of INTR	t_{SIT}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the rising edge of INTR	t_{AIT}		150	ns	
Delay Time from the falling edge of $\overline{WR}$ to the falling edge of INTR	t_{WIT}		250	ns	

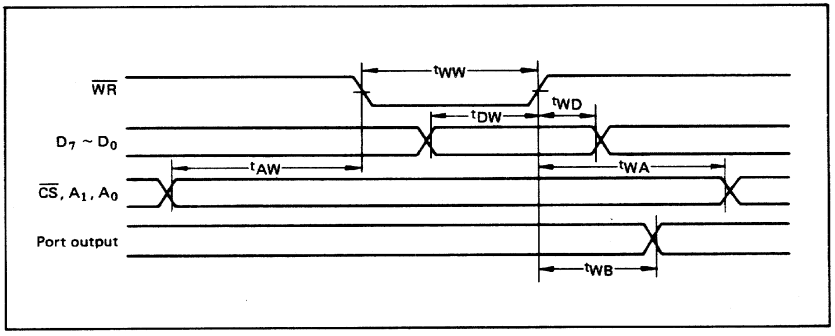
Note: Timing is measured at V_L = 0.8 V and V_H = 2.2 V for both input and outputs.

■ I/O-MSM82C55A-2RS/GS/VJS ■

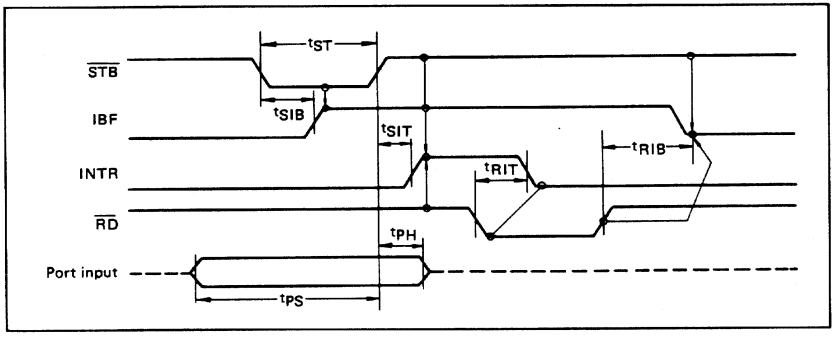
Basic Input Operation (Mode 0)



Basic Output Operation (Mode 0)

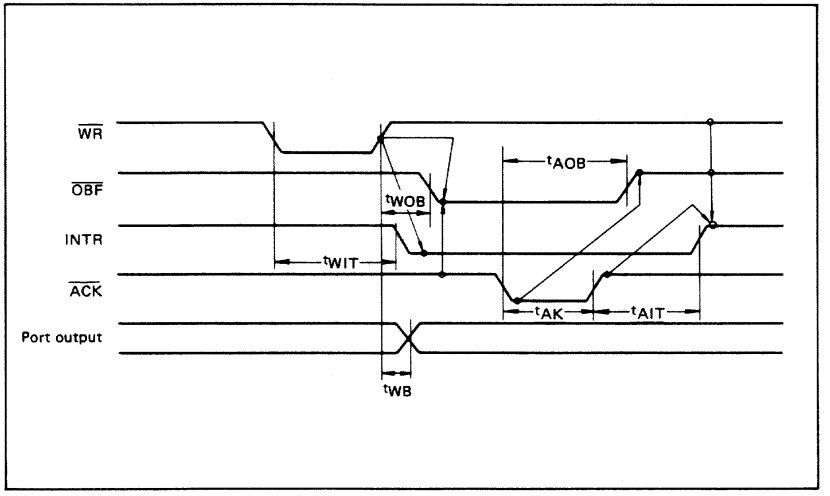


Strobe Input Operation (Mode 1)

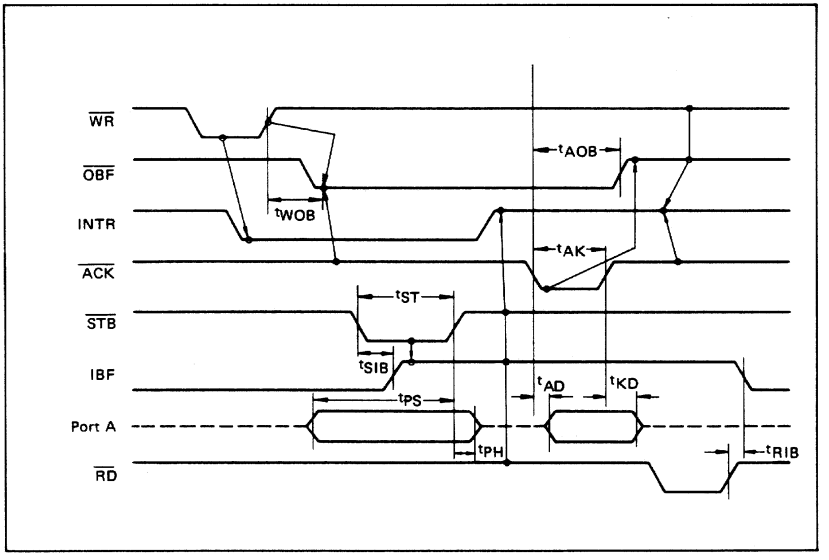


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Strobe Output Operation (Mode 1)



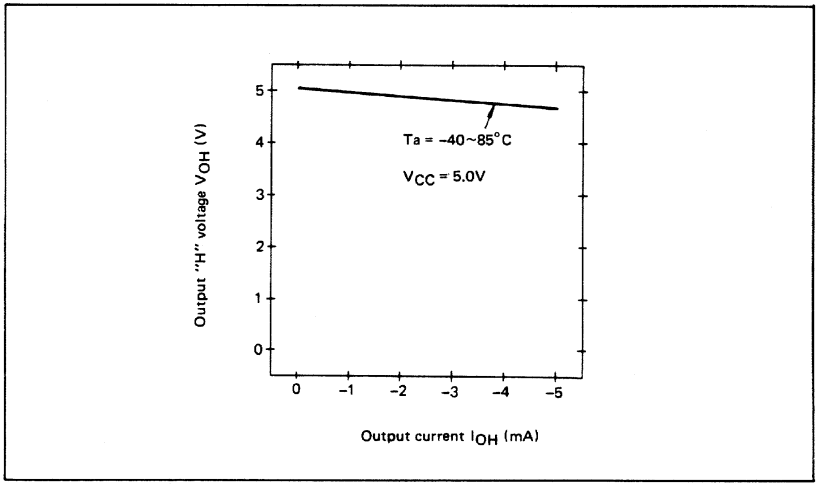
Bidirectional Bus Operation (Mode 2)



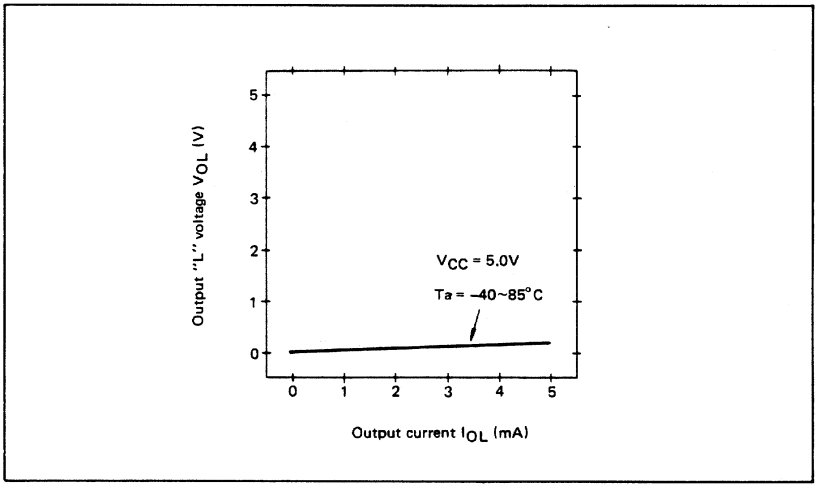
■ I/O-MSM82C55A-2RS/GS/VJS ■

OUTPUT CHARACTERISTICS (REFERENCE VALUE)

1 Output "H" Voltage (V_{OH}) vs. Output Current (I_{OH})



2 Output "L" Voltage (V_{OL}) vs. Output Current (I_{OL})



Note: The direction of flowing into the device is taken as positive for the output current.

■ I/O-MSM82C55A-2RS/GS/VJS ■

FUNCTIONAL DESCRIPTION OF PIN

Pin No.	Item	Input/Output	Function
D7 ~ D0	Bidirectional data bus	Input and output	These are three-state 8-bit bidirectional buses used to write and read data upon receipt of the $\overline{WR}$ and $\overline{RD}$ signals from CPU and also used when control words and bit set/reset data are transferred from CPU to MSM82C55A.
RESET	Reset input	Input	This signal is used to reset the control register and all internal registers when it is in high level. At this time, ports are all made into the input mode (high impedance status). all port latches are cleared to 0. and all ports groups are set to mode 0.
$\overline{CS}$	Chip select input	Input	When the $\overline{CS}$ is in low level, data transmission is enabled with CPU. When it is in high level, the data bus is made into the high impedance status where no write nor read operation is performed. Internal registers hold their previous status, however.
$\overline{RD}$	Read input	Input	When RD is in low level, data is transferred from MSM82C55A to CPU.
$\overline{WR}$	Write input	Input	When WR is in low level, data or control words are transferred from CPU to MSM82C55A.
A0, A1	Port select input (address)	Input	By combination of A0 and A1, either one is selected from among port A, port B, port C, and control register. These pins are usually connected to low order 2 bits of the address bus.
PA7 ~ PA0	Port A	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word. Especially, port A can be used as a bidirectional port when it is set to mode 2.
PB7 ~ PB0	Port B	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word.
PC7 ~ PC0	Port C	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word as 2 ports with 4 bits each. When port A or port B is used in mode 1 or mode 2 (port A only), they become control pins. Especially when port C is used as an output port, each bit can be set/reset independently.
V_{CC}			+5 V power supply.
GND			GND

BASIC FUNCTIONAL DESCRIPTION

Group A and Group B

When setting a mode to a port having 24 bits, set it by dividing it into two groups of 12 bits each.

Group A: Port A (8 bits) and high order 4 bits of port C (PC7 ~ PC4)

Group B: Port B (8 bits) and low order 4 bits of port C (PC3 ~ PC0)

Mode 0, 1, 2

There are 3 types of modes to be set by grouping as follows:

Mode 0: Basic input operation/output operation (Available for both groups A and B)

Mode 1: Strobe input operation/output operation (Available for both groups A and B)

Mode 2: Bidirectional bus operation (Available for group A only)

When used in mode 1 or mode 2, however, port C has bits to be defined as ports for control signal for operation ports (port A for group A and port B for group B) of their respective groups.

Port A, B, C

The internal structure of 3 ports is as follows:

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input)

Single bit set/reset function for port C

When port C is defined as an output port, it is possible to set (to turn to high level) or reset (to turn to low level) any one of 8 bits individually without affecting other bits.

■ I/O-MSM82C55A-2RS/GS/VJS ■

OPERATIONAL DESCRIPTION

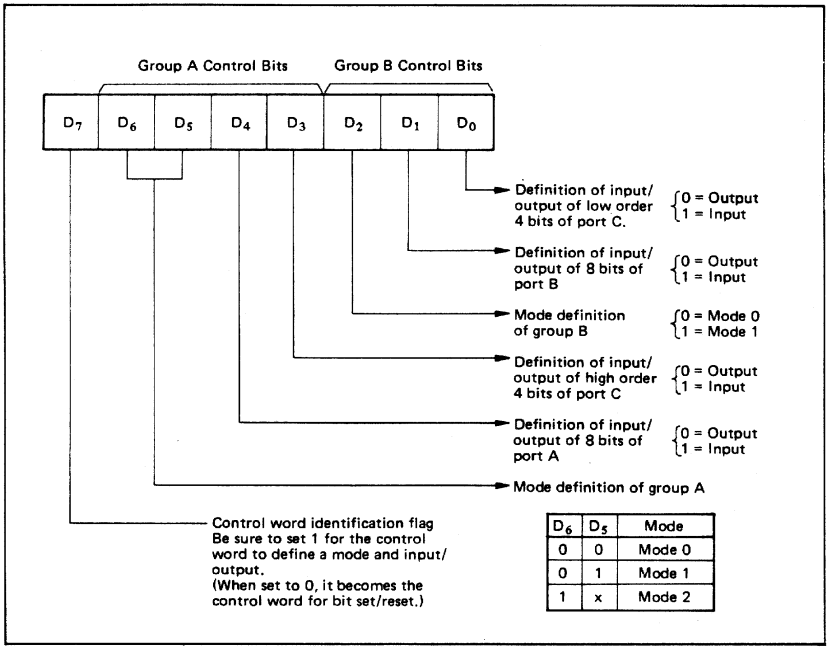
Control Logic

Operations by addresses and control signals, e.g., read and write, etc. are as shown in the table below:

Operation	A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Operation
Input	0	0	0	1	0	Port A → Data Bus
	0	1	0	1	0	Port B → Data Bus
	1	0	0	1	0	Port C → Data Bus
Output	0	0	0	0	1	Data Bus → Port A
	0	1	0	0	1	Data Bus → Port B
	1	0	0	0	1	Data Bus → Port C
Control	1	1	0	0	1	Data Bus → Control Register
Others	1	1	0	1	0	Illegal Condition
	x	x	1	x	x	Data bus is in the high impedance status.

Setting of Control Word

The control register is composed of 7-bit latch circuit and 1-bit flag as shown below.

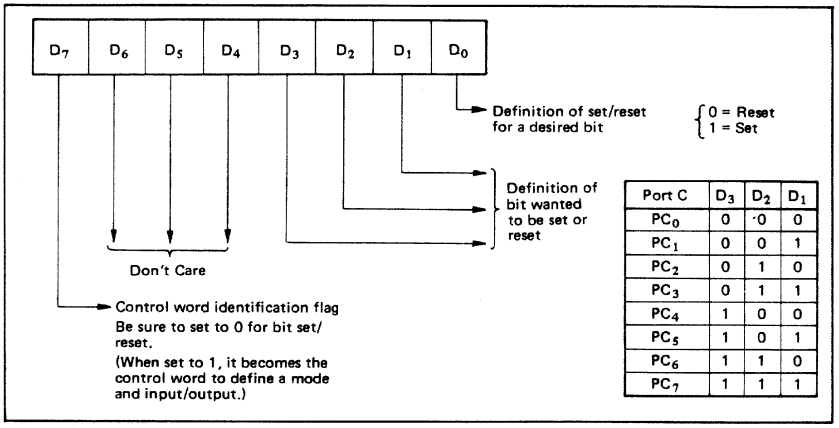


Precaution for mode selection

The output registers for ports A and C are cleared to ϕ each time data is written in the command register and the mode is changed, but the port B state is undefined.

Bit Set/Reset Function

When port C is defined as output port, it is possible to set (set output to 1) or reset (set output to 0) any one of 8 bits without affecting other bits as shown next page.



Port C	D_3	D_2	D_1
PC_0	0	0	0
PC_1	0	0	1
PC_2	0	1	0
PC_3	0	1	1
PC_4	1	0	0
PC_5	1	0	1
PC_6	1	1	0
PC_7	1	1	1

Interrupt Control Function

When the MSM82C55A is used in mode 1 or mode 2, the interrupt signal for the CPU is provided. The interrupt request signal is output from port C. When the internal flip-flop INTE is set beforehand at this time, the desired interrupt request signal is output. When it is reset beforehand, however, the interrupt request signal is not output. The set/reset of the internal flip-flop is made by the bit set/reset operation for port C virtually.

Bit set → INTE is set → Interrupt allowed
Bit reset → INTE is reset → Interrupt inhibited

Operational Description by Mode

1. Mode 0 (Basic input/output operation)

Mode 0 makes the MSM82C55A operate as a basic input port or output port. No control signals such as interrupt request, etc. are required in this mode. All 24 bits can be used as two-8-bit ports and two 4-bit ports. Sixteen combinations are then possible for inputs/outputs. The inputs are not latched, but the outputs are.

Type	Control Word								Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	High Order 4 Bits of Port C	Port B	Low Order 4 Bits of Port C
1	1	0	0	0	0	0	0	0	Output	Output	Output	Output
2	1	0	0	0	0	0	0	1	Output	Output	Output	Input
3	1	0	0	0	0	0	1	0	Output	Output	Input	Output
4	1	0	0	0	0	0	1	1	Output	Output	Input	Input
5	1	0	0	0	1	0	0	0	Output	Input	Output	Output
6	1	0	0	0	1	0	0	1	Output	Input	Output	Input
7	1	0	0	0	1	0	1	0	Output	Input	Input	Output
8	1	0	0	0	1	0	1	1	Output	Input	Input	Input
9	1	0	0	1	0	0	0	0	Input	Output	Output	Output
10	1	0	0	1	0	0	0	1	Input	Output	Output	Input
11	1	0	0	1	0	0	1	0	Input	Output	Input	Output
12	1	0	0	1	0	0	1	1	Input	Output	Input	Input
13	1	0	0	1	1	0	0	0	Input	Input	Output	Output
14	1	0	0	1	1	0	0	1	Input	Input	Output	Input
15	1	0	0	1	1	0	1	0	Input	Input	Input	Output
16	1	0	0	1	1	0	1	1	Input	Input	Input	Input

Note: When used in mode 0 for both groups A and B

2. Mode 1 (Strobe input/output operation)

In mode 1, the strobe, interrupt and other control signals are used when input/output operations are made from a specified port. This mode is available for both groups A and B. In group A at this time, port A is used as the data line and port C as the control signal.

Following is a descrption of the input operation in mode 1.

$\overline{STB}$ (Strobe input)

- When this signal is low level, the data output from terminal to port is fetched into the internal latch of the port. This can be made independent from the CPU, and the data is not output to the data bus until the RD signal arrives from the CPU.

IBF (Input buffer full flag output)

- This is the response signal for the $\overline{STB}$. This signal when turned to high level indicates that data is fetched into the input latch. This signal turns to high level at the falling edge of $\overline{STB}$ and to low level at the rising edge of $\overline{RD}$.

INTR (Interrupt request output)

- This is the interrupt request signal for the CPU of the data fetched into the input latch. It is indicated by high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{STB}$ (IBF = 1 at this time) and low level at the falling edge of the $\overline{RD}$ when the INTE is set.

  $INTE_A$ of group A is set when the bit for PC_4 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Following is a description of the output operation of mode 1.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data is written to the specified port upon receipt of the $\overline{WR}$ signal from the CPU. This signal turns to low level at the rising edge of the WR and high level at the falling edge of the ACK.

$\overline{ACK}$ (Acknowledge input)

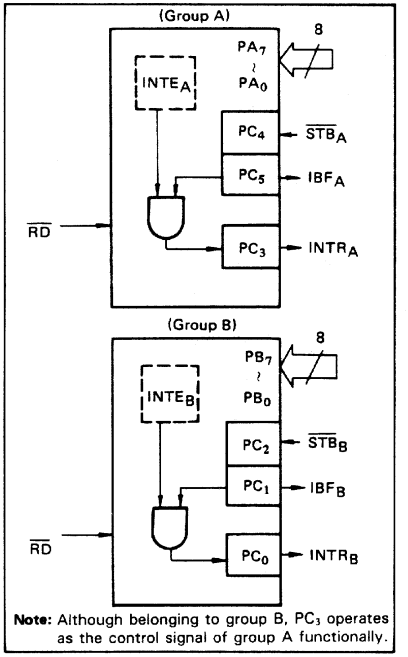
- This signal when turned to low level indicates that the terminal has received data.

INTR (Interrupt request output)

- This is the signal used to interrupt the CPU when a terminal receives data from the CPU via the MSM82C55A-5. It indicates the occurrence of the interrupt in high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{ACK}$ (OBF = 1 at this time) and low level at the falling edge of $\overline{WR}$ when the $INTE_B$ is set.

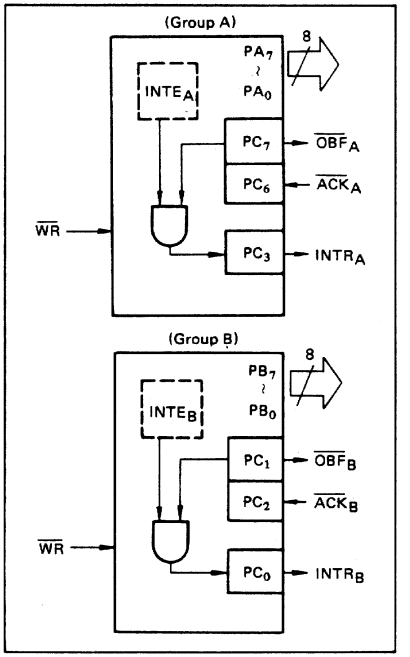
  $INTE_A$ of group A is set when the bit for PC_6 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Mode 1 Input



Note: Although belonging to group B, PC_3 operates as the control signal of group A functionally.

Mode 1 output

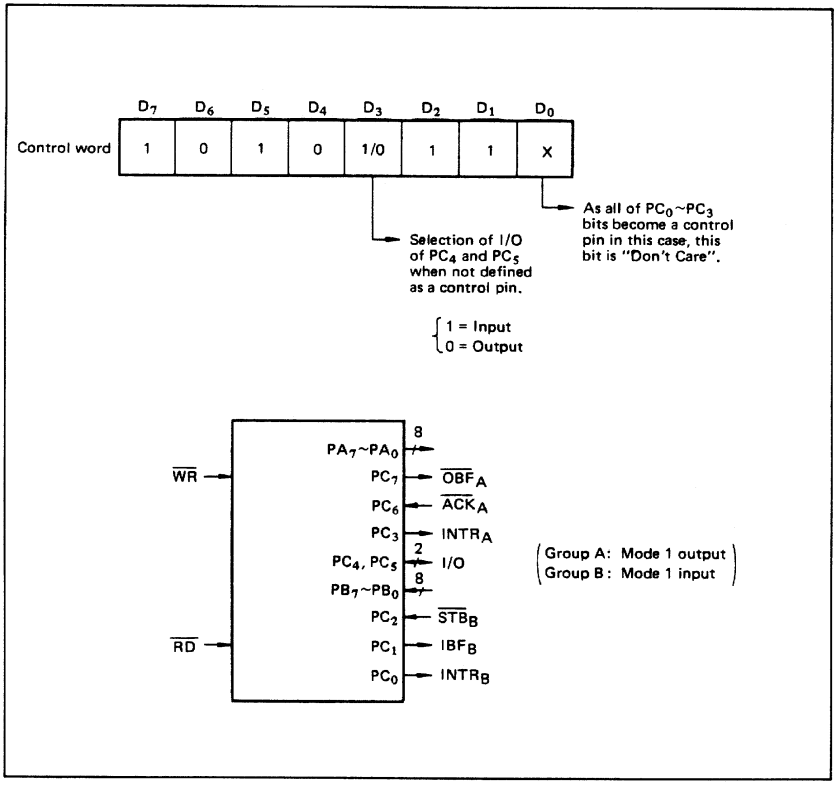


Port C Function Allocation in Mode 1

Combination of Input/Output / Port C	Group A: Input Group B: Input	Group A: Input Group B: Output	Group A: Output Group B: Input	Group A: Output Group B: Output
PC_0	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$
PC_1	IBF_B	$\overline{OBF}_B$	IBF_B	$\overline{OBF}_B$
PC_2	$\overline{STB}_B$	$\overline{ACK}_B$	$\overline{STB}_B$	$\overline{ACK}_B$
PC_3	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	$\overline{STB}_A$	$\overline{STB}_A$	I/O	I/O
PC_5	IBF_A	IBF_A	I/O	I/O
PC_6	I/O	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	I/O	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

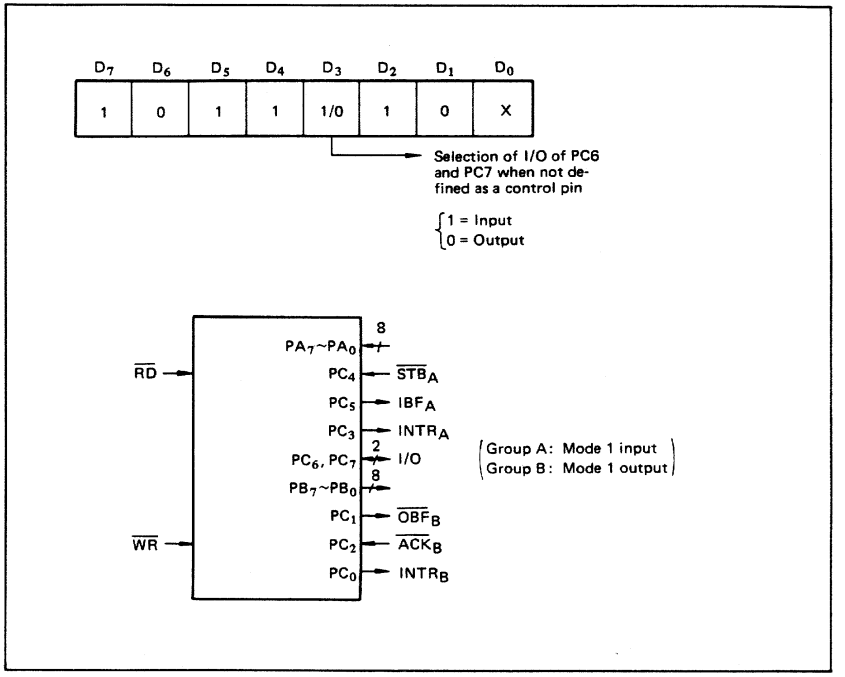
Note: I/O is a bit not used as the control signal, but it is available as a port of mode 0.

Examples of the relation between the control words and pins when used in mode 1 is shown below:
(a) When group A is mode 1 output and group B is mode 1 input.



■ I/O-MSM82C55A-2RS/GS/VJS ■

(b) When group A is mode 1 input and group B is mode 1 output.



3. Mode 2 (Strobe bidirectional bus I/O operation)

In mode 2, it is possible to transfer data in 2 directions through a single 8-bit port. This operation is akin to a combination between input and output operations. Port C waits for the control signal in this case, too. Mode 2 is available only for group A, however.

Next, a description is made on mode 2.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data has been written to the internal output latch upon receipt of the $\overline{WR}$ signal from the CPU. At this time, port A is still in the high impedance status and the data is not yet output to the outside. This signal turns to low level at the rising edge of the $\overline{WR}$ and high level at the falling edge of the $\overline{ACK}$.

$\overline{ACK}$ (Acknowledge input)

- When a low level signal is input to this pin, the high impedance status of port A is cleared, the buffer is enabled, and the data written to the internal output latch is output to port A. When the input returns to high level, port A is made into the high impedance status.

$\overline{STB}$ (Strobe input)

- When this signal turns to low level, the data output to the port from the pin is fetched into the internal input latch. The data is output to the data bus upon receipt of the RD signal from the CPU, but it remains in the high impedance status until then.

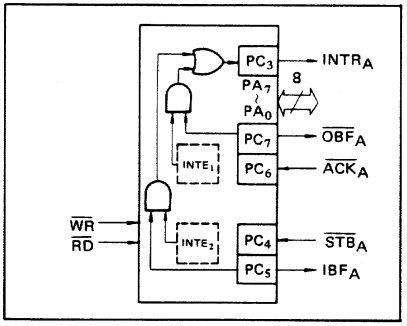
IBF (Input buffer full flag output)

- This signal when turned to high level indicates that data from the pin has been fetched into the input latch. This signal turns to high level at the falling edge of the $\overline{STB}$ and low level at the rising edge of the $\overline{RD}$.

INTR (Interrupt request output)

- This signal is used to interrupt the CPU and its operation in the same as in mode 1. There are two INTE flip-flops internally available for input and output to select either interrupt of input or output operation. The INTE1 is used to control the interrupt request for the output operation and it can be reset by the bit set for PC6. INTE2 is used to control the interrupt request for the input operation and it can be set by the bit set for PC4.

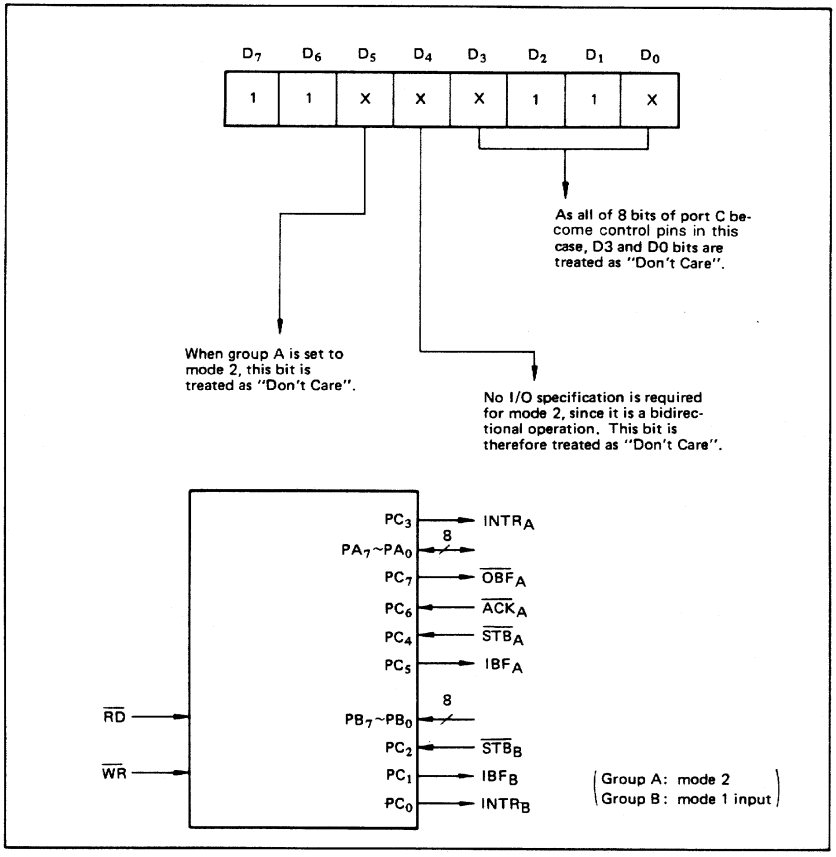
Mode 2 I/O Operation



Port C Function Allocation in Mode 2

Port C	Function
PC_0	Confirmed to the group B mode
PC_1	
PC_2	
PC_3	$INTR_A$
PC_4	$\overline{STB}_A$
PC_5	IBF_A
PC_6	$\overline{ACK}_A$
PC_7	$\overline{OBF}_A$

Following is an example of the relation between the control word and the pin when used in mode 2. When input in mode 2 for group A and in mode 1 for group B.



■ I/O-MSM82C55A-2RS/GS/VJS ■

4. When Group A is Different in Mode from Group B
Group A and group B can be used by setting them in different modes each other at the same time. When either group is set to mode1 or mode 2, it is possible to set the one not defined as a control pin in port C to both input and output as a port which operates in mode 0 at the 3rd and 0th bits of the control word.

(Mode combinations that define no control bit at port C)

	Group A	Group B	Port C							
			PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 0 output	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$\overline{STB}_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
			Controlled at the 3rd bit (D3) of the control word				Controlled at the 0th bit (D0) of the control word			

When the I/O bit is set to input in this case, it is possible to access data by the normal port C read operation.
When set to output, PC7 ~ PC4 bits can be accessed by the bit set/reset function only. Meanwhile, 3 bits from PC2 to PC0 can be accessed by normal write operation.

The bit set/reset function can be used for all of PC3 ~ PC0 bits. Note that the status of port C varies according to the combination of modes like this.

5. Port C Status Read

When port C is used for the control signal, that is, in either mode 1 or mode 2, each control signal and bus status signal can be read out by reading the content of port C.
The status read out is as follows:

	Group A	Group B	Status read on the data bus							
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 1 output	Mode 0	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$INTE_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	I/O	I/O	I/O
10	Mode 2	Mode 1 input	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
11	Mode 2	Mode 1 output	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$

6. Reset of MSM82C55A

Be sure to keep the RESET signal at power ON in the high level at least for 50 μs. Subsequently, it becomes the input mode at a high level pulse above 500 ns.

Note: Comparison of MSM82C55A-5 and MSM82C55A-2

MSM82C55A-5

After a write command is executed to the command register, the internal latch is cleared in PORTA PORTC. For instance, 00H is output at the beginning of a write command when the output port is assigned. However, if PORTB is not cleared at this time, PORTB is unstable. In other words, PORTB only outputs ineffective data (unstable value according to the device) during the period from after a write command is executed till the first data is written to PORTB.

MSM82C55A-2

After a write command is executed to the command register, the internal latch is cleared in All Ports(PORTA,PORTB,PORTC). 00H is ontput at the beginning of a write command when the output port is assigned.

Common Questions

Appendix
C

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of your DAQPad-6507/6508 devices.

General Information

What are DAQPad-6507/6508 devices?

The DAQPad-6507/6508 devices are USB platform, 96-line DIO devices.

What type of 5 V protection do the DAQPad-6507/6508 devices have?

The DAQPad-6507/6508 devices have 5 V lines equipped with a self-resetting 1 A fuse.

Installation and Configuration

How do I know if my version of Windows supports USB?

Look in the **System** properties in the control panel. The **Device Manager** tab should list a **Universal Serial Bus Controller** along with a USB Controller and a USB root hub. If your computer has this and also USB ports, your machine is supported. If your computer has USB ports but no controller is listed in the **Device Manager**, you might need to upgrade your software.

What is the best way to test my device without having to program the device?

If you are using Windows, the NI-DAQ Configuration Utility has a **Test** menu with some excellent tools for doing simple functional tests of the device, such as analog input and output, digital I/O, and counter/timer tests.

What does the blink pattern mean for the configuration LED on the front panel?

This LED blinks to indicate the status of the DAQPad-6507/6508 devices. It also can indicate an error through a blink code. Refer to Table 2-1 for more information.

Digital I/O

What are the power-on states of the PPI and DIO lines on the I/O connector?

At system power-on and reset, both the PPI and DIO lines are set to high impedance by the hardware. This means that the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in the *Digital I/O State Selection* section in Chapter 3, *Signal Connections*. These resistors weakly pull the output to either a logic high or logic low state.

Customer Communication

Appendix
D

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve your technical problems and a form you can use to comment on the product documentation. When you contact us, we need the information on the Technical Support Form and the configuration form, if your manual contains one, about your system configuration to answer your questions as quickly as possible.

National Instruments has technical assistance through electronic, fax, and telephone systems to quickly provide the information you need. Our electronic services include a bulletin board service, an FTP site, a fax-on-demand system, and e-mail support. If you have a hardware or software problem, first try the electronic support systems. If the information available on these systems does not answer your questions, we offer fax and telephone support through our technical support centers, which are staffed by applications engineers.

Electronic Services

Bulletin Board Support

National Instruments has BBS and FTP sites dedicated for 24-hour support with a collection of files and documents to answer most common customer questions. From these sites, you can also download the latest instrument drivers, updates, and example programs. For recorded instructions on how to use the bulletin board and FTP services and for BBS automated information, call 512 795 6990. You can access these services at:

United States: 512 794 5422
Up to 14,400 baud, 8 data bits, 1 stop bit, no parity

United Kingdom: 01635 551422
Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

France: 01 48 65 15 59
Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

FTP Support

To access our FTP site, log on to our Internet host, `ftp.natinst.com`, as `anonymous` and use your Internet address, such as `joesmith@anywhere.com`, as your password. The support files and documents are located in the `/support` directories.

Fax-on-Demand Support

Fax-on-Demand is a 24-hour information retrieval system containing a library of documents on a wide range of technical information. You can access Fax-on-Demand from a touch-tone telephone at 512 418 1111.

E-Mail Support (Currently USA Only)

You can submit technical support questions to the applications engineering team through e-mail at the Internet address listed below. Remember to include your name, address, and phone number so we can contact you with solutions and suggestions.

`support@natinst.com`

Telephone and Fax Support

National Instruments has branch offices all over the world. Use the list below to find the technical support number for your country. If there is no National Instruments office in your country, contact the source from which you purchased your software to obtain support.

Country	Telephone	Fax
Australia	03 9879 5166	03 9879 6277
Austria	0662 45 79 90 0	0662 45 79 90 19
Belgium	02 757 00 20	02 757 03 11
Brazil	011 288 3336	011 288 8528
Canada (Ontario)	905 785 0085	905 785 0086
Canada (Québec)	514 694 8521	514 694 4399
Denmark	45 76 26 00	45 76 26 02
Finland	09 725 725 11	09 725 725 55
France	01 48 14 24 24	01 48 14 24 14
Germany	089 741 31 30	089 714 60 35
Hong Kong	2645 3186	2686 8505
Israel	03 6120092	03 6120095
Italy	02 413091	02 41309215
Japan	03 5472 2970	03 5472 2977
Korea	02 596 7456	02 596 7455
Mexico	5 520 2635	5 520 3282
Netherlands	0348 433466	0348 430673
Norway	32 84 84 00	32 84 86 00
Singapore	2265886	2265887
Spain	91 640 0085	91 640 0533
Sweden	08 730 49 70	08 730 43 70
Switzerland	056 200 51 51	056 200 51 55
Taiwan	02 377 1200	02 737 4644
United Kingdom	01635 523545	01635 523154
United States	512 795 8248	512 794 5678

Technical Support Form

Photocopy this form and update it each time you make changes to your software or hardware, and use the completed copy of this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name _____

Company _____

Address _____

_____

Fax (___) _____Phone (___) _____

Computer brand_____ Model _____Processor_____

Operating system (include version number) _____

Clock speed _____MHz RAM _____MB Display adapter _____

Mouse ___yes ___no Other adapters installed_____

Hard disk capacity _____MB Brand_____

Instruments used _____

_____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is: _____

_____

_____

_____

_____

List any error messages: _____

_____

_____

The following steps reproduce the problem: _____

_____

_____

_____

_____

DAQPad-6507/6508 Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

National Instruments Products

DAQ hardware _____

Interrupt level of hardware _____

Base I/O address of hardware _____

Programming choice _____

NI-DAQ, LabVIEW, or LabWindows/CVI version _____

Other boards in system _____

Base I/O address of other boards _____

DMA channels of other boards _____

Interrupt level of other boards _____

Other Products

Computer make and model _____

Microprocessor _____

Clock frequency or speed _____

Type of video board installed _____

Operating system version _____

Operating system mode _____

Programming language _____

Programming language version _____

Other boards in system _____

Base I/O address of other boards _____

DMA channels of other boards _____

Interrupt level of other boards _____

Documentation Comment Form

National Instruments encourages you to comment on the documentation supplied with our products. This information helps us provide quality products to meet your needs.

Title: *DAQPad™-6507/6508 User Manual*

Edition Date: December 1998

Part Number: 321724B-01

Please comment on the completeness, clarity, and organization of the manual.

_____

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If you find errors in the manual, please record the page numbers and describe the errors.

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Thank you for your help.

Name _____

Title _____

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Prefix	Meanings	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Symbols/Numbers

%	percent
±	plus or minus
°	degrees
/	per
+	positive of, or plus
–	negative of, or minus
Ω	ohms
$\sqrt{\ }$	square root of
+5 V	+5 VDC source signal

A

A	amperes
AC	alternating current
AC coupled	allowing the transmission of AC signals while blocking DC signals
ACH	analog input channel signal
ACK*	acknowledge input signal
A/D	analog-to-digital
address	character code that identifies a specific location (or series of locations) in memory
AIRQ0	PPI A interrupt request bit for Port A
AIRQ1	PPI A interrupt request bit for POrt B
alias	a false lower frequency component that appears in sampled data acquired at too low a sampling rate
ALU	arithmetic logic unit—the element(s) in a processing system that perform(s) the mathematical functions such as addition, subtraction, multiplication, division, inversion, AND, OR, NAND, and NOR
AMD	Advanced Micro Devices
ANSI	American National Standards Institute
APA	bidirectional data lines for Port A of PPI A
APB	bidirectional data lines for Port B of PPI A
APC	bidirectional data lines for Port C of PPI A
ASIC	application-specific integrated circuit
asynchronous	(1) hardware—a property of an event that occurs at an arbitrary time, without synchronization to a reference clock (2) software—a property of a function that begins an operation and returns prior to the completion or termination of the operation

B

b	bit—one binary digit, either 0 or 1
B	byte—eight related bits of data, an eight-bit binary number. Also used to denote the amount of memory required to store one byte of data.
bandwidth	the range of frequencies present in a signal, or the range of frequencies to which a measuring device can respond
base address	a memory address that serves as the starting address for programmable registers. All other addresses are located by adding to the base address.
baud rate	serial communications data transmission rate expressed in bits per second (b/s)
BCD	binary-coded decimal
binary	a number system with a base of 2
BIOS	basic input/output system or built-in operating system
bipolar	a signal range that includes both positive and negative values (for example, –5 V to +5 V)
BIRQ0	PPI B interrupt request bit for Port A
BIRQ1	PPI B interrupt request bit for Port B
BNC	a type of coaxial signal connector
BPA	bidirectional data lines for Port A of PPI B
BPB	bidirectional data lines for Port B of PPI B
BPC	bidirectional data lines for Port C of PPI B
break-before-make	a type of switching contact that is completely disengaged from one terminal before it connects with another terminal
breakdown voltage	the voltage high enough to cause breakdown of optical isolation, semiconductors, or dielectric materials. *See also* working voltage.
buffer	temporary storage for acquired or generated data (software)

burst-mode	a high-speed data transfer in which the address of the data is sent followed by back-to-back data words while a physical signal is asserted
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the AT bus, NuBus, Micro Channel, and EISA bus.
bus master	a type of a plug-in board or controller with the ability to read and write devices on the computer bus

C

C	Celsius
channel	pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
channel clock	the clock controlling the time interval between individual channel sampling within a scan. Boards with simultaneous sampling do not have this clock.
chromatograph	an instrument used in chemical analysis of gases and liquids.
CI	computing index
circuit trigger	a condition for starting or stopping clocks
CIRQ0	PPI C interrupt request bit for Port A
CIRQ1	PPI C interrupt request bit for Port B
clock	hardware component that controls timing for reading from or writing to groups
CMOS	complementary metal-oxide semiconductor
coupling	the manner in which a signal is connected from one location to another
CPA	bidirectional lines for Port A of PPI C
CPB	bidirectional lines for Port A of PPI C

CPC	bidirectional lines for Port A of PPIC
CPU	central processing unit
crosstalk	an unwanted signal on one channel due to an input on a different channel
CTR1	counter 1 enable bit
CTRIRQ	counter interrupt enable bit
current drive capability	the amount of current a digital or analog output channel is capable of sourcing or sinking while still operating within voltage range specifications
current sinking	the ability of a DAQ board to dissipate current for analog or digital output signals
current sourcing	the ability of a DAQ board to supply current for analog or digital output signals

D

DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
daisy-chain	a method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO boards plugged into a computer, and possibly generating control signals with D/A and/or DIO boards in the same computer
DATA	data lines at the specified port signal
DC	direct current
DC coupled	allowing the transmission of both AC and DC signals

DCS	distributed control system—a large-scale process control system characterized by a distributed network of processors and I/O subsystems that encompass control, user interfacing, data collection, and system management. DCSs are commonly used in large industrial facilities, such as a petroleum refinery or paper mill.
default setting	a default parameter value recorded in the driver. In many cases, the default input of a control is a certain value (often 0) that means *use the current default setting*. For example, the default input for a parameter may be *do not change current setting*, and the default setting may be *no AMUX-64T boards*. If you do change the value of such a parameter, the new value becomes the new setting. You can set default settings for some parameters in the configuration utility or manually using switches located on the device.
device	a plug-in DAQ board, card, or pad that can contain multiple channels and conversion devices. Plug-in boards, PCMCIA cards, and devices such as the DAQPad-1200, which connects to your computer parallel port, are all examples of DAQ devices. SCXI modules are distinct from devices, with the exception of the SCXI-1200, which is a hybrid.
DGND	digital ground signal
digital port	*See* port.
digital trigger	a TTL level signal having two discrete levels—a high and a low level
DIN	Deutsche Industrie Norme
DIO	digital input/output
DIP	dual inline package
DIRQ0	PPI D interrupt request bit for Port A
DIRQ1	PPI D interrupt request bit for Port B
DMA	direct memory access
DNL	differential nonlinearity
DOS	disk operating system
downstream	the direction of data flow from the host computer or away from the host

DPA	bidirectional data lines for Port A of PPI D
DPB	bidirectional data lines for Port B of PPI D
DPC	bidirectional data lines for Port C of PPI D
DRAM	dynamic RAM
drivers	software that controls a specific hardware device such as a DAQ board or a GPIB interface board
DSP	digital signal processing
dual-access memory	memory that can be sequentially accessed by more than one controller or processor but not simultaneously accessed. Also known as shared memory.
dual-ported memory	memory that can be simultaneously accessed by more than one controller or processor
dynamic range	the ratio of the largest signal level a circuit can handle to the smallest signal level it can handle (usually taken to be the noise level), normally expressed in decibels

E

ECL	emitter-coupled logic
EEPROM	electrically erasable programmable read-only memory
EGA	enhanced graphics adapter
EISA	Extended Industry Standard Architecture
EMC	electromechanical compliance
EPROM	erasable programmable read-only memory—ROM that can be erased (usually by ultraviolet light exposure) and reprogrammed
event	the condition or state of an analog or digital signal
expansion ROM	an onboard EEPROM that may contain device-specific initialization and system boot functionality
external trigger	a voltage pulse from an external source that triggers an event such as A/D conversion

F

false triggering	triggering that occurs at an unintended time
fetch-and-deposit	a data transfer in which the data bytes are transferred from the source to the controller, and then from the controller to the target
FIFO	first-in-first-out
floating signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.
flyby	a type of high-performance data transfer in which the data bytes pass directly from the source to the target without being transferred to the controller
ft	feet

G

GND	ground
GPIB	General Purpose Interface bus, synonymous with HP-IB. The standard bus used for controlling electronic instruments with a computer. Also called IEEE 488 bus because it is defined by ANSI/IEEE Standards 488-1978, 488.1-1987, and 488.2-1987.
g_{rms}	level of random vibration
ground tie point	the location where two or more grounds (such as digital ground, analog output ground, analog input ground, and so on), are connected or tied together
grounded measurement system	*See* referenced single-ended measurement system.

H

h	hour
half-power bandwidth	the frequency range over which a circuit maintains a level of at least –3 dB with respect to the maximum level
handle	pointer to a pointer to a block of memory; handles reference arrays and strings. An array of strings is a handle to a block of memory containing handles to strings.
handler	a device driver that is installed as part of the operating system of the computer
handshaked digital I/O	a type of digital acquisition/generation where a device or module accepts or transfers data after a digital pulse has been received. Also called latched digital I/O.
hardware	the physical components of a computer system, such as the circuit boards, plug-in boards, chassis, enclosures, peripherals, cables, and so on
hardware triggering	a form of triggering where you set the start time of an acquisition and gather data at a known position in time relative to a trigger signal
hex	hexadecimal
host	the host computer system where the Universal Serial Bus host controller is installed
Hz	hertz

I

IBF	input buffer full signal
IBFA	input buffer bit for Port A
IBFB	input buffer bit for Port B
IBM	International Business Machines
IC	integrated circuit
ID	identification

IDE	integrated development environment
IEEE	Institute of Electrical and Electronics Engineers
IEEE 488	the shortened notation for ANSI/IEEE Standards 488-1978, 488.1-1987, and 488.2-1987. See also GPIB.
immediate digital I/O	a type of digital acquisition/generation where LabVIEW updates the digital lines or port states immediately or returns the digital value of an input line. Also called nonlatched digital I/O.
in.	inches
Industrial Device Networks	standardized digital communications networks used in industrial automation applications; they often replace vendor-proprietary networks so that devices from different vendors can communicate in control systems
INL	integral nonlinearity—a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry
input bias current	the current that flows into the inputs of a circuit
input impedance	the measured resistance and capacitance between the input terminals of a circuit
input offset current	the difference in the input bias currents of the two inputs of an instrumentation amplifier
instrument driver	a set of high-level software functions that controls a specific GPIB, VXI, or RS-232 programmable instrument or a specific plug-in DAQ board. Instrument drivers are available in several forms, ranging from a function callable language to a virtual instrument (VI) in LabVIEW.
instrumentation amplifier	a circuit whose output voltage with respect to ground is proportional to the difference between the voltages at its two inputs
INTE1	interrupt enable bit for Port A output interrupts
INTE2	interrupt enable bit for Port A input interrupts
INTEA	interrupt enable bit for Port A
INTEB	interrupt enable bit for Port B
integral control	a control action that eliminates the offset inherent in proportional control

INTEN	global interrupt enable bit
interrupt	a computer signal indicating that the CPU should suspend its current task to service a designated activity
interrupt level	the relative priority at which a device can interrupt
interval scanning	scanning method where there is a longer interval between scans than there is between individual channels comprising a scan
INTR	interrupt request signal
INTRA	interrupt request status bit for Port A
INTRB	interrupt request status bit for Port B
I/O	input/output
I_{OH}	current, output high
I_{OL}	current, output low
IRQ	interrupt request
ISA	Industry Standard Architecture
isolation	a type of signal conditioning in which you isolate the transducer signals from the computer for safety purposes. This protects you and your computer from large voltage spikes and makes sure the measurements from the DAQ device are not affected by differences in ground potentials.
isolation voltage	the voltage that an isolated circuit can normally withstand, usually specified from input to input and/or from any input to the amplifier output, or to the computer bus
isothermal	constructed to maintain constant temperature across area. Isothermal construction of terminal blocks increases thermocouple measurement accuracy.

K

k	kilo—the standard metric prefix for 1,000, or 10^3, used with units of measure such as volts, hertz, and meters
K	kilo—the prefix for 1,024, or 2^{10}, used with B in quantifying data or computer memory
kbytes/s	a unit for data transfer that means 1,000 or 10^3 bytes/s
kS	1,000 samples
Kword	1,024 words of memory

L

LabVIEW	laboratory virtual instrument engineering workbench
latched digital I/O	a type of digital acquisition/generation where a device or module accepts or transfers data after a digital pulse has been received. Also called handshaked digital I/O.
LED	light-emitting diode
library	a file containing compiled object modules, each comprised of one of more functions, that can be linked to other object modules that make use of these functions. NIDAQMSC.LIB is a library that contains NI-DAQ functions. The NI-DAQ function set is broken down into object modules so that only the object modules that are relevant to your application are linked in, while those object modules that are not relevant are not linked.
listener	a device on the GPIB that receives information from a Talker on the bus
LSB	least significant bit

M

m	meters
M	(1) Mega, the standard metric prefix for 1 million or 10^6, when used with units of measure such as volts and hertz; (2) mega, the prefix for 1,048,576, or 2^{20}, when used with B to quantify data or computer memory

MB	megabytes of memory
MBLT	eight-byte block transfers in which both the Address bus and the Data bus are used to transfer data
Mbytes/s	a unit for data transfer that means 1 million or 10^6 bytes/s
memory buffer	*See* buffer.
MFLOPS	million floating-point operations per second—the unit for expressing the computational power of a processor
MIO	multifunction I/O
MIPS	million instructions per second—the unit for expressing the speed of processor machine code instructions
MITE	MXI Interfaces to Everything is a custom ASIC designed by National Instruments that implements the PCI bus interface. The MITE supports bus mastering for high speed data transfers over the PCI bus.
MS	million samples
MSB	most significant bit
MTBF	mean time between failure
multiplexed mode	an SCXI operating mode in which analog input channels are multiplexed into one module output so that your cabled DAQ device has access to the module's multiplexed output as well as the outputs on all other multiplexed modules in the chassis through the SCXI bus. Also called serial mode.
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel

N

NB	NuBus—a slot-dependent, 32-bit bus type used in Macintosh computers that has 32 interrupts
NC	normally closed, or not connected
NI-DAQ	National Instruments driver software for DAQ hardware

NIST	National Institute of Standards and Technology
nodes	execution elements of a block diagram consisting of functions, structures, and subVIs
noise	an undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
nonlatched digital I/O	a type of digital acquisition/generation where LabVIEW and NI-DAQ updates the digital lines or port states immediately or returns the digital value of an input line. Also called immediate digital I/O or non-handshaking.
nonreferenced signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called floating signal sources. Some common examples of nonreferenced signal sources are batteries, transformers, or thermocouples.

O

OBF*	output buffer full signal
OBFA*	output buffer bit for Port A
OBFB*	output buffer bit for Port B
onboard channels	channels provided by the plug-in data acquisition board
onboard RAM	optional RAM usually installed into SIMM slots
OpenDoc	a compound document architecture created by the joining of several technologies supplied by Apple (the base OpenDoc architecture, the Bento file system and the Open Scripting Architecture) and IBM (the System Object Model)
operating system	base-level software that controls a computer, runs programs, interacts with users, and communicates with installed hardware or peripheral devices
optical coupler	a device designed to transfer electrical signals by utilizing light waves

optical isolation	the technique of using an optoelectric transmitter and receiver to transfer data without electrical continuity, to eliminate high-potential differences and transient signals
optocoupler	to provide coupling with electrical isolation between input and output. Sometimes called optoisolator or photocoupler.
OUT	output
output settling time	the amount of time required for the analog output voltage to reach its final value within specified limits
output slew rate	the maximum rate of change of analog output voltage from one level to another

P

packet	a bundle of data organized in a group for transmission
parallel mode	a type of SCXI operating mode in which the module sends each of its input channels directly to a separate analog input channel of the device to the module
passband	the range of frequencies which a device can properly propagate or measure
pattern generation	a type of handshaked (latched) digital I/O in which internal counters generate the handshaked signal, which in turn initiates a digital transfer. Because counters output digital pulses at a constant rate, this means you can generate and retrieve patterns at a constant rate because the handshaked signal is produced at a constant rate.
PC	personal computer
PC Card	a credit-card-sized expansion card that fits in a PCMCIA slot, often referred to as a PCMCIA card
PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and workstations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.

PCMCIA	an expansion bus architecture that has found widespread acceptance as a *de facto* standard in notebook-size computers. It originated as a specification for add-on memory cards written by the Personal Computer Memory Card International Association.
PFI	Programmable Function Input
photoelectric sensor	an electrical device that responds to a change in the intensity of the light falling upon it
pipeline	a high-performance processor structure in which the completion of an instruction is broken into its elements so that several elements can be processed simultaneously from different instructions
PLC	programmable logic controller—a highly reliable special-purpose computer used in industrial monitoring and control applications. PLCs typically have proprietary programming and networking protocols, and special-purpose digital and analog I/O ports.
Plug and Play devices	devices that do not require DIP switches or jumpers to configure resources on the devices—also called switchless devices
Plug and Play ISA	a specification prepared by Microsoft, Intel, and other PC-related companies that will result in PCs with plug-in boards that can be fully configured in software, without jumpers or switches on the boards
PnP	Plug and Play
port	(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of four or eight lines of digital input and/or output
posttriggering	the technique used on a DAQ board to acquire a programmed number of samples after trigger conditions are met
potentiometer	an electrical device the resistance of which can be manually adjusted; used for manual adjustment of electrical circuits and as a transducer for linear or rotary position
PPI	programmable peripheral interface
ppm	parts per million
pretriggering	the technique used on a DAQ board to keep a continuous buffer filled with data, so that when the trigger conditions are met, the sample includes the data leading up to the trigger condition

propagation	the transmission of a signal through a computer system
propagation delay	the amount of time required for a signal to pass through a circuit
protocol	the exact sequence of bits, characters, and control codes used to transfer data between computers and peripherals through a communications channel, such as the GPIB bus
pts	points
pulsed output	a form of counter signal generation by which a pulse is outputted when a counter reaches a certain value

Q

QuickTime	Apple system software tools that make video presentation a standard part of the Macintosh. Applications can use QuickTime to record and display audio and video in the same way applications use system tools to generate and display text and graphics.

R

RAM	random-access memory
RD*	read signal
real time	a property of an event or system in which data is processed as it is acquired instead of being accumulated and processed at a later time
referenced signal sources	signal sources with voltage signals that are referenced to a system ground, such as the earth or a building ground. Also called grounded signal sources.
resource locking	a technique whereby a device is signaled not to use its local memory while the memory is in use from the bus
retry	an acknowledge by a destination that signifies that the cycle did not complete and should be repeated
R_{EXT}	external resistance
ribbon cable	a flat cable in which the conductors are side by side

rise time	the difference in time between the 10% and 90% points of a system's step response
R_L	load resistance
rms	root mean square
RTD	resistive temperature device

S

s	seconds
S	samples
sample counter	the clock that counts the output of the channel clock, in other words, the number of samples taken. On boards with simultaneous sampling, this counter counts the output of the scan clock and hence the number of scans.
SCADA	supervisory control and data acquisition—a common PC function in process control applications, where programmable logic controllers (PLCs) perform control functions but are monitored and supervised by a PC
scan	one or more analog or digital input samples. Typically, the number of input samples in a scan is equal to the number of channels in the input group. For example, one pulse from the scan clock produces one scan which acquires one new sample from every analog input channel in the group.
SCANCLK	scan clock signal
scan clock	the clock controlling the time interval between scans. On boards with interval scanning support (for example, the AT-MIO-16F-5), this clock gates the channel clock on and off. On boards with simultaneous sampling (for example, the EISA-A2000), this clock clocks the track-and-hold circuitry.
scan rate	the number of scans per second. For example, a scan rate of 10 Hz means sampling each channel 10 times per second.
SCXI	Signal Conditioning eXtensions for Instrumentation
SE	single-ended inputs
shared memory	*See* dual-access memory

signal conditioning	the manipulation of signals to prepare them for digitizing
signal divider	performing frequency division on an external signal
SIMM	single in-line memory module
SISOURCE	SI counter clock signal
SMB	a type of miniature coaxial signal connector
software trigger	a programmed event that triggers an event such as data acquisition
software triggering	a method of triggering in which you simulate an analog trigger using software. Also called conditional retrieval.
source impedance	a parameter of signal sources that reflects current-driving ability of voltage sources (lower is better) and the voltage-driving ability of current sources (higher is better)
SOURCE input pin	an counter input pin where the counter counts the signal transitions
SPDT	single-pole double throw—a property of a switch in which one terminal can be connected to one of two other terminals
SS	simultaneous sampling—a property of a system in which each input or output channel is digitized or updated at the same instant
S/s	samples per second—used to express the rate at which a DAQ board samples an analog signal
STARTSCAN	start scan signal
STB	strobe input signal
STC	system timing controller
statically configured device	a device whose logical address cannot be set through software; that is, it is not dynamically configurable
switchless device	devices that do not require dip switches or jumpers to configure resources on the devices—also called Plug and Play devices
synchronous	(1) hardware—a property of an event that is synchronized to a reference clock (2) software—a property of a function that begins an operation and returns only when the operation is complete

system RAM	RAM installed on a personal computer and used by the operating system, as contrasted with onboard RAM
system noise	a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

TC	terminal count
T/H	track-and-hold—a circuit that tracks an analog voltage and holds the value on command
Theorem	signal contains no frequency components higher than half the frequency at which it is sampled, then the original signal can be recovered without distortion
throughput rate	the data, measured in bytes/s, for a given continuous operation, calculated to include software overhead. Throughput Rate = Transfer Rate Software Overhead Factor.
top-level VI	VI at the top of the VI hierarchy. This term is used to distinguish the VI from its subVIs.
transfer rate	the rate, measured in bytes/s, at which data is moved from source to destination after software initialization and set up operations; the maximum rate at which the hardware can operate
TRIG	trigger signal
trigger	any event that causes or starts some form of data capture
TTL	transistor-transistor logic

U

UART	universal asynchronous receiver/transmitter—an integrated circuit that converts parallel data to serial data (and vice versa), commonly used as a computer bus to serial device interface for serial communication
UI	update interval
UISOURCE	update interval counter clock signal

unipolar	a signal range that is always positive (for example, 0 to +10 V)
update	the output equivalent of a scan. One or more analog or digital output samples. Typically, the number of output samples in an update is equal to the number of channels in the output group. For example, one pulse from the update clock produces one update which sends one new sample to every analog output channel in the group.
UPDATE	update signal
update rate	the number of output updates per second
upstream	the direction data flow towards the host computer
USB	Universal Serial Bus

V

V	volts
V_{CC}	+5 V power supply
VDC	volts direct current
VDMAD	virtual DMA driver
V_{EXT}	external volt
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{IN}	volts in
VISA	a new driver software architecture developed by National Instruments to unify instrumentation software for GPIB, DAQ, and VXI. It has been accepted as a standard for VXI by the VXIplug&play Systems Alliance.

visual basic custom control (VBXs)	a specific form of binary packaged object that can be created by different companies and integrated into applications written using Visual Basic
V_{OH}	volts, output high
V_{OL}	volts, output low

W

wire	data path between nodes
word	the standard number of bits that a processor or memory manipulates at one time. Microprocessors typically use 8-, 16-, or 32-bit words.
working voltage	the highest voltage that should be applied to a product in normal use, normally well under the breakdown voltage for safety margin. *See also* breakdown voltage.
WR*	write signal

Z

zero-overhead looping	the ability of a high-performance processor to repeat instructions without requiring time to branch to the beginning of the instructions
zero-wait-state memory	memory fast enough that the processor does not have to wait during any reads and writes to the memory

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