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NI Dynamic Signal Acquisition

NI Dynamic Signal Acquisition User Manual

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This hardware was tested and complies with applicable regulatory requirements and limits for electromagnetic compatibility (EMC) as indicated in the Declaration of Conformity (DoC)* of this hardware. These requirements and limits are designed to provide reasonable protection against harmful interference when the hardware is operated in the electromagnetic environment indicated in the DoC*. In special cases, for example when either highly sensitive or noisy hardware is being used in close proximity to National Instruments hardware, you may have to employ additional mitigation measures to minimize the potential for electromagnetic interference.

While this hardware is compliant with the applicable regulatory EMC requirements, there is no guarantee that interference will not occur in a particular installation. To minimize the potential for the hardware to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this hardware in strict accordance with the instructions in the hardware documentation and the DoC*.

If this hardware causes interference with licensed radio communications services or other nearby electronic hardware, which you can determine by powering the hardware off and on, you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the antenna of the receiver (the device suffering interference).
- Relocate the transmitter (the device generating interference) with respect to the receiver.
- Plug the transmitter into a different outlet so that the transmitter and the receiver are on different branch circuits.

This hardware may generate emissions that exceed regulatory requirements or may become more sensitive to disturbances in the local electromagnetic environment when test leads are attached or when connected to a test object.

Operation of this hardware in a residential area is likely to cause harmful interference. Users are required to correct the interference at their expense or cease operation of the hardware.

Changes or modifications not expressly approved by National Instruments may void the authority of the user to operate the hardware under the local regulatory rules.

* The Declaration of Conformity (DoC) contains important supplementary EMC compliance information and instructions for the user or installer. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

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About This Manual

This manual contains information about using National Instruments Dynamic Signal Acquisition (DSA) devices. These devices have 24-bit resolution and support sample rates of up to 204.8 kS/s. With excellent dynamic range, noise and distortion performance, and simultaneous sampling and synchronization capabilities, the DSA devices discussed in this help file are well-suited for many applications including, but not limited to:

- Audio testing
- Acoustic measurements
- Environmental noise testing
- Vibration analysis
- Noise, vibration, and harshness measurements
- Machine condition monitoring
- Rotating machinery evaluation

If you have not already installed the device, refer to the *DAQ Getting Started Guide*.

This manual does *not* describe how to use the USB-923*x*, cRIO-923*x*, or cRIO-4408 devices. For information about these devices, go to `ni.com/manuals`.

To comment on National Instruments documentation, refer to the National Instruments Web site at `ni.com`.

Conventions

The following conventions are used in this manual:

<> Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <3..0>.

» The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

	This icon denotes a note, which alerts you to important information.
	This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on a product, refer to the *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, or *NI 449x Specifications* for information about precautions to take.
bold	Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
italic	Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.
NI USB-443x	NI USB-443x refers to the NI USB-4431 and NI USB-4432 unless otherwise noted.
NI 446*x*	NI 446*x* refers to the NI PCI-4461, NI PXI-4461, NI PCI-4462, and NI PXI-4462 unless otherwise noted.
NI 447*x*	NI 447*x* refers to the NI PCI-4472, NI PXI-4472, NI PCI-4474, NI PCI-4472B, and NI PXI-4472B unless otherwise noted.
NI 449*x*	NI 449*x* refers to the any applicable bus version of NI 4495, NI 4496 and NI 4498 product unless otherwise noted.
Platform	Text in this font denotes a specific platform and indicates that the text following it applies only to that platform.

Related Documentation

Each application software package and instrument driver includes information about writing applications for taking measurements and controlling measurement devices. The following references to documents assume you have NI-DAQmx 8.8 or later, and where applicable, version 8.*x* or later of the NI application software.

Refer to the National Instruments Product Manuals Library at `ni.com/manuals` for updated documentation resources.

The following documents contain information that you might find helpful as you use this manual.

NI-DAQ

The *DAQ Getting Started Guide* describes how to install your NI-DAQmx for Windows software, your NI-DAQmx-supported DAQ device, and how to confirm that your device is operating properly. Select **Start»All Programs»National Instruments»NI-DAQ»DAQ Getting Started Guide**.

The *NI-DAQ Readme* lists which devices are supported by this version of NI-DAQ. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQ Readme**.

The *NI-DAQmx Help* contains general information about measurement concepts, key NI-DAQmx concepts, and common applications that are applicable to all programming environments. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.

The *Traditional NI-DAQ (Legacy) User Manual* contains an API overview and general information about measurement concepts. Select **Start»All Programs»National Instruments»NI-DAQ»Traditional NI-DAQ (Legacy) User Manual**.

The *DAQ Assistant Help* describes how to use the DAQ Assistant to interactively configure common measurement tasks, global virtual channels, or scales. Select **Help»Help Topics»NI-DAQmx»DAQ Assistant** in the **Measurement & Automation Explorer** window.

NI-DAQmx for Linux

The *DAQ Getting Started Guide* describes how to install your NI-DAQmx-supported DAQ device and confirm that your device is operating properly.

The *NI-DAQ Readme* for Linux lists supported devices and includes software installation instructions, frequently asked questions, and known issues.

The *C Function Reference Help* describes functions and attributes.

The *NI-DAQmx for Linux Configuration Guide* provides configuration instructions, templates, and instructions for using test panels.

Note All NI-DAQmx documentation for Linux is installed at `/usr/local/natinst/nidaqmx/docs`.

LabVIEW

If you are a new user, use the *Getting Started with LabVIEW* manual to familiarize yourself with the LabVIEW graphical programming environment and the basic LabVIEW features you use to build data acquisition and instrument control applications. Open the *Getting Started with LabVIEW* manual by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals** or by navigating to the `labview\manuals` directory and opening `LV_Getting_Started.pdf`.

Use the *LabVIEW Help*, available by selecting **Help»Search the LabVIEW Help** in LabVIEW, to access information about LabVIEW programming concepts, step-by-step instructions for using LabVIEW, and reference information about LabVIEW VIs, functions, palettes, menus, and tools. Refer to the following locations on the **Contents** tab of the *LabVIEW Help* for information about NI-DAQmx:

- **Getting Started»Getting Started with DAQ**—Includes overview information and a tutorial to learn how to take an NI-DAQmx measurement in LabVIEW using the DAQ Assistant.
- **VI and Function Reference»Measurement I/O VIs and Functions**—Describes the LabVIEW NI-DAQmx VIs and properties.
- **Taking Measurements**—Contains the conceptual and how-to information you need to acquire and analyze measurement data in LabVIEW, including common measurements, measurement fundamentals, NI-DAQmx key concepts, and device considerations.

If you use the LabVIEW Sound and Vibration Toolkit, the LabVIEW Order Analysis Toolkit, or the Sound and Vibration Measurement Suite, you can use the *LabVIEW Help* to access information about Sound and Vibration or Order Analysis VIs, functions, and palettes. You also can use the user manuals for each toolkit to access information about sound and vibration or order analysis concepts.

LabWindows/CVI

The **Data Acquisition** book of the *LabWindows/CVI Help* contains measurement concepts for NI-DAQmx. This book also contains **Taking an NI-DAQmx Measurement in LabWindows/CVI**, which includes step-by-step instructions about creating a measurement task using the DAQ Assistant. In LabWindows™/CVI™, select **Help»Contents**, then select **Using LabWindows/CVI»Data Acquisition**.

The **NI-DAQmx Library** book of the *LabWindows/CVI Help* contains API overviews and function reference for NI-DAQmx. Select **Library Reference»NI-DAQmx Library** in the *LabWindows/CVI Help*.

Measurement Studio

If you program your NI-DAQmx-supported device in Measurement Studio using Visual C++, Visual C#, or Visual Basic .NET, you can interactively create channels and tasks by launching the DAQ Assistant from MAX or from within Visual Studio .NET. You can generate the configuration code based on your task or channel in Measurement Studio. Refer to the *DAQ Assistant Help* for additional information about generating code. You also can create channels and tasks, and write your own applications in your ADE using the NI-DAQmx API.

For help with NI-DAQmx methods and properties, refer to the NI-DAQmx .NET Class Library or the NI-DAQmx Visual C++ Class Library included in the *NI Measurement Studio Help*. For general help with programming in Measurement Studio, refer to the *NI Measurement Studio Help*, which is fully integrated with the Microsoft Visual Studio .NET help. To view this help file in Visual Studio. NET, select **Measurement Studio» NI Measurement Studio Help**.

To create an application in Visual C++, Visual C#, or Visual Basic .NET, follow these general steps:

1. In Visual Studio .NET, select **File»New»Project** to launch the New Project dialog box.
2. Find the Measurement Studio folder for the language you want to create a program in.
3. Choose a project type. You add DAQ tasks as a part of this step.

ANSI C without NI Application Software

The *NI-DAQmx Help* contains API overviews and general information about measurement concepts. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.

The *NI-DAQmx C Reference Help* describes the NI-DAQmx Library functions, which you can use with National Instruments data acquisition devices to develop instrumentation, acquisition, and control applications. Select **Start»All Programs»National Instruments»NI-DAQ» NI-DAQmx C Reference Help**.

.NET Languages without NI Application Software

With the Microsoft .NET Framework version 1.1 or later, you can use NI-DAQmx to create applications using Visual C# and Visual Basic .NET without Measurement Studio. You need Microsoft Visual Studio .NET 2003 or Microsoft Visual Studio 2005 for the API documentation to be installed.

The installed documentation contains the NI-DAQmx API overview, measurement tasks and concepts, and function reference. This help is fully integrated into the Visual Studio .NET documentation. To view the NI-DAQmx .NET documentation, go to **Start»Programs»National Instruments»NI-DAQ»NI-DAQmx .NET Reference Help**. Expand **NI Measurement Studio Help»NI Measurement Studio .NET Class Library»Reference** to view the function reference. Expand **NI Measurement Studio Help»NI Measurement Studio .NET Class Library»Using the Measurement Studio .NET Class Libraries** to view conceptual topics for using NI-DAQmx with Visual C# and Visual Basic .NET.

To get to the same help topics from within Visual Studio, go to **Help» Contents**. Select **Measurement Studio** from the **Filtered By** drop-down list and follow the previous instructions.

Device Documentation and Specifications

NI-DAQ 7.0 and later includes the **Device Document Browser**, which contains online documentation for supported DAQ, SCXI, and switch devices, such as help files describing device pinouts, features, and operation, and PDF files of the printed device documents. You can find, view, and/or print the documents for each device using the **Device Document Browser** at any time by inserting the CD. After installing the **Device Document Browser**, device documents are accessible from **Start»**

All Programs»National Instruments»NI-DAQ»Browse Device Documentation.

Training Courses

If you need more help getting started developing an application with NI products, NI offers training courses. To enroll in a course or obtain a detailed course outline, refer to `ni.com/training`.

Technical Support on the Web

For additional support, refer to `ni.com/support` or `zone.ni.com`.



Note You can download these documents at `ni.com/manuals`.

DAQ specifications and some DAQ manuals are available as PDFs. You must have Adobe Acrobat Reader with Search and Accessibility 5.0.5 or later installed to view the PDFs. Refer to the Adobe Systems Incorporated Web site at `www.adobe.com` to download Acrobat Reader. Refer to the National Instruments Product Manuals Library at `ni.com/manuals` for updated documentation resources.

1

Getting Started

Before installing the NI Dynamic Signal Acquisition (DSA) device, you must install the software you plan to use with the device.

Installing NI-DAQ

You must install the latest version of NI-DAQ before installing the DSA device. Refer to the *DAQ Getting Started Guide*, which you can download at `ni.com/manuals`. The *DAQ Getting Started Guide* provides installation instructions and information on NI software, tools, and application development environments (ADEs) that you can use to configure and control DSA devices.

Installing Other Software

If you are using other software, such as another application development environment (ADE), refer to the installation instructions that accompany your software.

Installing the Hardware

The *DAQ Getting Started Guide* contains general information on how to install PCI and PXI devices, accessories, and cables.

Device Pinouts

Refer to the *NI-DAQmx Help* for DSA device pinout information. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.

Measurement System Overview

A measurement system can consist of several components including a computer, signal conditioning components, and sensors. Refer to the *DAQ Getting Started Guide* for a measurement system overview showing the path of physical phenomena to your measurement application.

Sensors and Transducers

A sensor or transducer is a device that outputs an electrical signal in response to a measured physical phenomenon such as pressure or temperature. The most common sensors for use with DSA devices include microphones for measuring sound pressure and accelerometers for measuring linear acceleration or vibration.

Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about typical DSA device measurements. You also can refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information about microphones or accelerometers.

2

Dynamic Signal Acquisition Device Concepts

This chapter contains information about Dynamic Signal Acquisition (DSA) device concepts, including Nyquist frequency and bandwidth, noise, analog input and output, timing and triggering, and synchronization.

Nyquist Frequency and Nyquist Bandwidth

Any sampling system, such as an *ADC*, is limited in the bandwidth of the signals it can measure. Specifically, a sampling rate of f_s can represent only signals with frequencies lower than $f_s/2$. This maximum frequency is known as the *Nyquist frequency*. The bandwidth from 0 Hz to the Nyquist frequency is the *Nyquist bandwidth*.

Noise



Caution Electromagnetic interference can adversely affect the measurement accuracy of the DSA products described in this document. The inputs and outputs of these products are isolated from chassis ground for functional reasons. Therefore, the outer conductor of any connected coaxial cable is not connected to chassis ground and the outer conductor will not act as a shield for unwanted noise. The shield can act as an antenna to transmit noise into the environment or receive noise from the environment that could affect measurement accuracy. To ensure proper shielding effectiveness of connected coaxial cables, the outer conductor must be directly connected to chassis or earth ground at the load end of the cable. In addition, snap-on ferrite beads or other remedial measures may be required to prevent unwanted emissions or immunity. Refer to the specifications of your product for more information about EMC performance.

DSA devices typically have a dynamic range of more than 110 dB. Several factors can degrade the noise performance of input channels, such as noise picked up from nearby electronic devices. DSA devices work best when kept as far away as possible from other plug-in devices, power supplies, disk drives, and computer monitors. Cabling is also critical. Use well-shielded coaxial or floating cables for all connections. Route the

cables away from sources of interference such as computer monitors, switching power supplies, and fluorescent lights. Physical motion or deformation can induce noise on sensitive analog cables. Use a transducer with a low output impedance to minimize system susceptibility to external noise sources and crosstalk.

You can reduce the effects of noise on your measurements by carefully choosing the sample rate to maximize the effectiveness of the anti-alias filtering. Computer monitor noise, for example, typically occurs at frequencies between 15 kHz and 65 kHz. If the signal of interest is restricted to below 10 kHz, for example, the anti-alias filters reject the monitor noise outside the frequency band of interest, and a sampling rate of at least 21.6 kS/s guarantees that any signal components in the 10 kHz bandwidth of interest are acquired without aliasing and without being attenuated by the digital filter. Refer to the *Analog Input Filters* section of this chapter for more information about anti-alias filtering.

When possible, use the differential configuration to minimize the effect of any noise produced by ground currents in the chassis and common-mode noise. If you have particularly noisy AC power, consider external filtering, such as a line conditioner or an uninterruptible power supply.

Analog Input

This section contains information about DSA device analog input concepts.

Analog Input Channel Configurations

The NI 446*x* supports two terminal configurations for analog input: *differential* and *pseudodifferential*. The NI USB-443*x*, NI 447*x* and NI 449*x* support only the pseudodifferential channel configuration. The term pseudodifferential refers to the 50 Ω and 1 kΩ resistance between the outer connector shell and chassis ground.

Note Attach all DSA devices to the chassis with screws to provide a reliable ground connection. If you use a PXI device, tighten the screws at the top and bottom of the front face of the module. If you use a PCI device, keep the screw that held the PCI slot cover to the computer chassis. Reinsert this screw to securely attach the device.

Choosing Channel Configurations

If the signal source or DUT inputs are *floating*, use the pseudodifferential configuration. You must provide a ground reference for a floating signal. If you do not provide a ground-reference point—for example, selecting

differential mode with a floating microphone or shaker table input amplifier with differential inputs—the outputs or inputs can drift outside the device *common-mode range*.

For AI, if the signal source is grounded, use either the differential or pseudodifferential configurations. Provide only one ground-reference point for each channel by properly selecting differential or pseudodifferential configuration. If you provide two ground-reference points—for example, if you select pseudodifferential mode with a grounded accelerometer or amplifier—the difference in ground potential results in currents in the ground system that can cause measurement errors. The 50 Ω and 1 kΩ resistor on the signal ground is usually sufficient to reduce this current to negligible levels, but results can vary depending on the system setup.

Configure the channels based on the signal source reference or DUT configuration. Refer to Table 2-1 to determine how to configure the channel.

Table 2-1. Analog Input

Source Reference	Channel Configuration
Floating	Pseudodifferential
Grounded	Differential or pseudodifferential

The NI 446*x* is automatically configured for differential mode when powered on or powered off. This configuration protects the 50 Ω resistor on the negative pin.

Input Coupling

You can configure each NI USB-443*x*, NI 446*x* or NI 447*x* device AI channel for either AC or DC coupling. If you select DC coupling, any DC offset present in the source signal is passed to the ADC. The DC-coupling configuration is usually best if the signal source has only small amounts of offset voltage or if the DC content of the acquired signal is important. If the source has a significant amount of unwanted offset, select AC coupling to take full advantage of the input dynamic range.

Note The NI 449*x* allows AC coupling only.

Selecting AC coupling enables a highpass resistor-capacitor (RC) filter into the positive and negative signal paths. The filter time constant is 47 ms for the NI 446*x*, NI 4472, and NI PCI-4474. The highpass RC filter settles to

0.5% accuracy in 0.25 s in response to a step input. It takes 0.782 s to settle to 24-bit accuracy in response to a step input. The settling time is somewhat dependent on the DUT impedance as well.

The NI 4472B and NI 449*x* have a larger time constant (330 ms). It takes 5.5 s to settle to 24-bit accuracy in response to a step input.

The NI USB-4431 has a time constant of 0.2 seconds and takes 3.4 seconds to settle to 24-bits. The NI USB-4432 has a time constant of 1.75 seconds and takes 30.0 seconds to settle to 24-bits.

Note NI-DAQmx does not compensate for the settling time introduced by the RC filter when switching from DC to AC coupling. To compensate for the filter settling time, you can discard the samples taken during the settling time or force a delay before you restart the measurement. You must force the delay after the AI task is committed but before the task starts.

Using AC coupling results in an attenuation of the low-frequency response of the AI circuitry. Refer to the *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for information about cut-off frequency for each device.

TEDS (Transducer Electronic Data Sheet)

TEDS-capable sensors carry a built-in, self-identification EEPROM that stores a table of parameters and sensor information. TEDS sensors have two modes of operation: an analog mode, which allows the sensors to operate as transducers measuring physical phenomena, and a digital mode, which allows the user to write and read information to and from the TEDS. The NI USB-443*x*, NI PCI-4461, NI 4462, and NI 449*x* support modes for Class I TEDS sensors without any additional hardware. The NI 447*x* devices require an accessory such as the BNC-2096 to allow the user to digitally communicate with the EEPROM on Class I TEDS sensors.

TEDS contains information about the sensor such as calibration, sensitivity, and manufacturer information. This information is accessible in Measurement & Automation Explorer (MAX), VIs in LabVIEW, or by calling the equivalent function calls in a text-based ADE.

Refer to the following installed help files for more information about TEDS:

- *Measurement & Automation Explorer Help for NI-DAQmx*—Contains information on configuring and testing data acquisition (DAQ) devices, RT Series DAQ devices, SCXI devices, SCC devices, TEDS carriers, and RTSI cables using Measurement & Automation Explorer (MAX) for NI-DAQmx, and special considerations for operating systems. Select **Help»Help Topics»NI-DAQmx»MAX Help for NI-DAQmx** in MAX.
- *NI-DAQmx Help*—Contains general information about measurement concepts, key NI-DAQmx concepts, and common applications that are applicable to all programming environments. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.
- *LabVIEW Help*—Contains information about LabVIEW programming concepts, step-by-step instructions for using LabVIEW, and reference information about LabVIEW VIs, functions, palettes, menus, and tools.

You also can refer to the following pages on `ni.com` for more information. Go to `ni.com/info` and enter the info code.

- *Smart Sensors*—Info code `rdsenr`
- *What Are Plug & Play Sensors?*—Info code `rdpnpy`
- *IEEE 1451.4 Sensor Templates Overview*—Info code `rdted6`

IEPE

If you attach an *IEPE* accelerometer or microphone to an AI channel that requires excitation from the DSA device, you must enable the IEPE excitation circuitry for that channel to generate the required excitation current. You can independently configure IEPE signal conditioning on a per channel basis on all DSA devices.

A DC voltage offset is generated equal to the product of the excitation current and sensor impedance when IEPE signal conditioning is enabled. To remove the unwanted offset, enable AC coupling. Use DC coupling with IEPE excitation enabled only if the offset does not exceed the voltage range of the channel.

Common IEPE excitation values are 2.1, 4 and 10 mA. Refer to the *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for a list of supported IEPE current values for each device.

Note You must set the NI 446*x* inputs in pseudodifferential mode when IEPE is turned on.

Overload Detection

When the signal voltage exceeds the ADC range, distortion caused by a clipped or overranged waveform can occur. The NI USB-443x and NI 446*x* devices include overload detection in both the analog domain (predigitization) and digital domain (postdigitization). The NI 447*x* and 449*x* devices support digital domain overload detection. An analog overrange can occur independently from a digital overrange, and vice versa. For example, an IEPE accelerometer might have a resonant frequency that, when stimulated, can produce an overrange in the analog signal. However, because the ADC delta-sigma technology uses very sharp anti-aliasing filters, the overrange is not passed into the digitized signal.

Conversely, a sharp transient on the analog side might not overrange, but the step response of the delta-sigma anti-aliasing filters might produce clipping in the digital data. The NI USB-443x and NI 446*x* analog overload detection circuitry detects a clipped or overloaded condition. You can programmatically poll the overload detection circuitry on a per channel basis to monitor for an overload condition. If an overload is detected, consider any data acquired at that time corrupt.

DSA devices perform digital overload detection as a percentage of the range. The overload detection occurs before the device applies gain and offset corrections. Detecting the overload before the gain and offset corrections catches an overflow condition in the delta-sigma modulator or ADC filter.

For instance on some DSA devices, the analog overload point for DSA devices is approximately 10.7 V_{pk}, the voltage at which the front-end circuitry begins showing signs of saturation. Figure 2-1 shows harmonic aliases caused by clipping with a 1.0 kHz sine wave at 10.8 V_{pk} versus the same signal at 8.9 V_{pk}, which shows no clipping, on an NI 446*x* device. NI USB-443*x*, NI 447*x* and NI 449*x* devices display similar behavior.

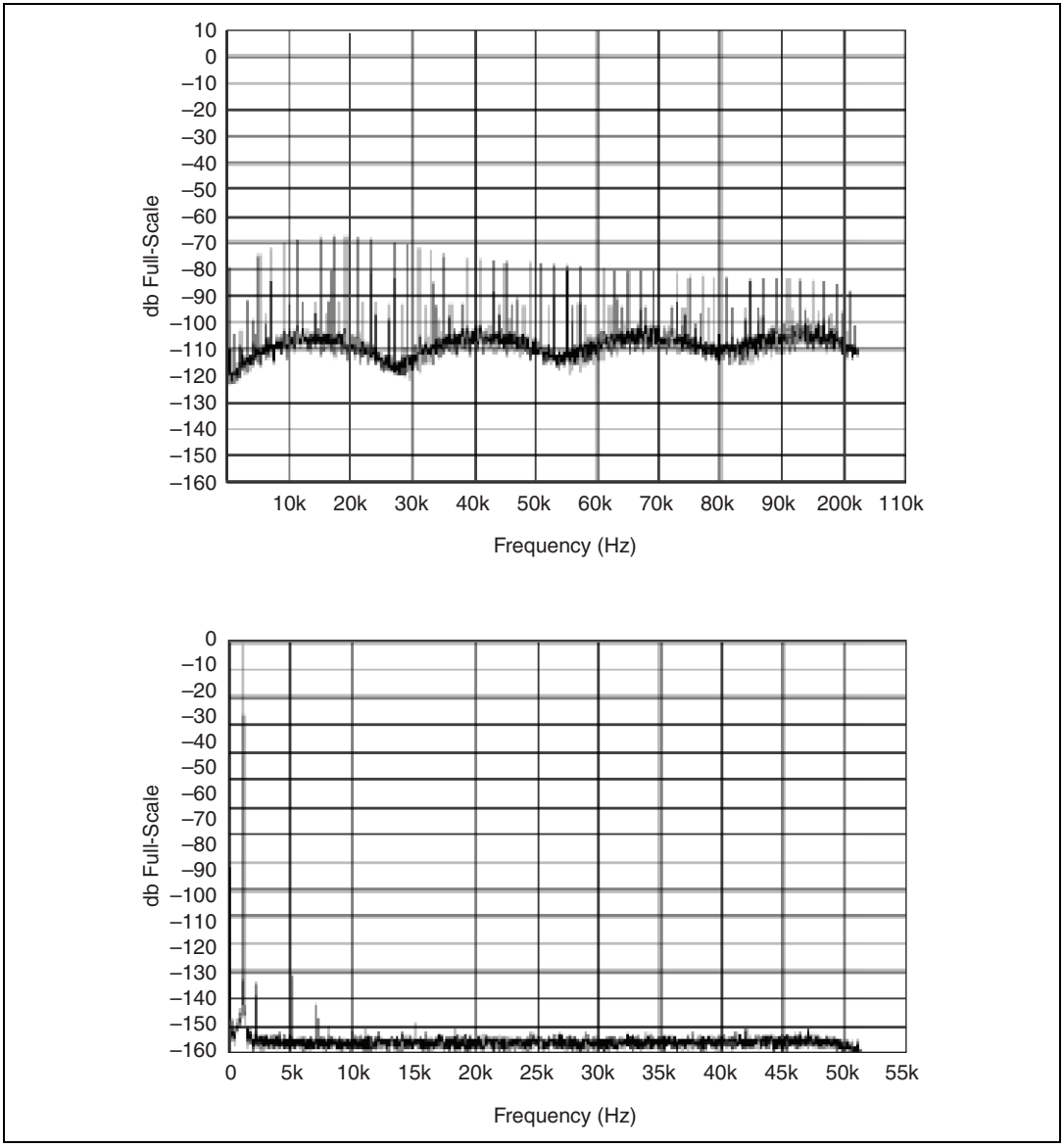


Figure 2-1. NI 446*x* Harmonic Aliases

Caution For NI 446*x* devices, overload detection is not supported for the ±42.4 V_{pk} input range setting. This setting attenuates the signal by a factor of 10. This attenuation factor implies that the ADC reaches the analog saturation point at 115 V_{pk}. This level is greater than what the ±42.4 V_{pk} range can safely support. You risk damaging the input circuitry

when measuring voltages capable of producing an overload condition when you use the ±42.4 V_{pk} range or –20 dB gain setting.

ADC

Each ADC in a DSA device uses a conversion method known as delta-sigma modulation. If the desired data rate is 51.2 kS/s, each ADC actually samples its input signal at 6.5536 MS/s, 128 times the data rate, producing 1-bit samples that are sent to a digital filter. This filter rejects signal components greater than the Nyquist frequency of 25.6 kHz. The 1-bit, 6.5536 MS/s data stream from the ADC contains all of the information necessary to produce 24-bit samples at 51.2 kS/s. The delta-sigma ADC achieves this conversion from high speed to high resolution with a technique called noise shaping. The ADC adds random noise to the signal so that the resulting quantization noise, although large, is restricted to frequencies above the Nyquist frequency, 25.6 kHz in this case. This noise is not correlated with the input signal and is almost completely rejected by the digital filter.

The resulting output of the filter is a band-limited signal with a large dynamic range. One of the advantages of a delta-sigma ADC is that it uses a 1-bit DAC as an internal reference. As a result, the delta-sigma ADC is free from the differential nonlinearity (DNL) and associated noise inherent in high-resolution ADCs using other conversion techniques.

Analog Input Filters

This section contains information about analog input filters.

Anti-Alias Filters

A digitizer or ADC might sample signals containing frequency components above the Nyquist limit. The undesirable effect of the digitizer modulating out-of-band components into the Nyquist bandwidth is aliasing. The greatest danger of aliasing is that you cannot determine whether aliasing occurred by looking at the ADC output. If an input signal contains several frequency components or harmonics, some of these components might be represented correctly while others contain aliased artifacts.

Lowpass filtering to eliminate components above the Nyquist frequency either before or during the digitization process can guarantee that the digitized data set is free of aliased components. DSA devices employ both digital and analog lowpass filters to achieve this protection.

The delta-sigma ADCs on DSA devices include an oversampled architecture and sharp digital filters with cut-off frequencies that track the sampling rate. Thus, the filter automatically adjusts to follow the Nyquist frequency. Although the digital filter eliminates almost all out-of-band components, it is still susceptible to aliases from certain narrow frequency bands, defined by the following rules:

- When you select a sample rate greater than 102.4 kS/s and less than or equal to 204.8 kS/s, the susceptible areas are centered around 32, 64, 96, and other multiples of 32 f_s (NI 446*x* and NI 449*x* only, because only the NI 446*x* and NI 449*x* devices support sample rates higher than 102.4 kS/s).
- When you select a sample rate greater than 51.2 kS/s and less than or equal to 102.4 kS/s, the susceptible areas are centered around 64, 128, 192, and other multiples of 64 f_s.
- When you select a sample rate greater than or equal to the minimum rate for the specific DSA device and less than or equal to 51.2 kS/s, the susceptible areas are centered around 128, 256, 384 and other multiples of 128 f_s.

Note On the NI USB-443*x* the susceptible areas are at multiples of 64 f_s regardless of the sample rate.

The susceptible frequency band is always one f_s wide. For example, if f_s = 10,000 S/s, the digital filter can admit aliases from analog components between 1.275 MHz and 1.285 MHz.

In addition to the ADC built-in digital filtering, DSA devices feature a fixed-frequency analog filter. The analog filter removes high-frequency components in the analog signal path before they reach the ADC. This filtering addresses the possibility of high-frequency aliasing from the narrow bands that are not covered by the digital filter. Each input channel on a DSA device is equipped with a two-pole lowpass Butterworth filter.

While the frequency response of the digital filter directly scales with the sample rate, the analog filter –3 dB point is fixed. The analog filter response produces good high-frequency alias rejection while maintaining a flat in-band frequency response. Because the analog filter is a two-pole system, the filter roll-off is not extremely sharp. The filter provides effective alias rejection at higher sampling rates, where only very high frequencies in the previously mentioned susceptible areas can pass through the digital filter. Some DSA devices support enhanced low-frequency alias rejection. The NI USB-443x, NI 446*x*, NI 447*x*, and NI 449*x* devices have different filter response curves.

Low-Frequency Alias Rejection

At very low sample rates, between the minimum rate for the specific DSA device and 25.6 kS/s, the anti-aliasing filters of DSA device AI channels might not completely reject all out-of-band signals. The internal digital filter of the delta-sigma ADC cannot suppress signals with frequencies near the multiples of the oversample rate (sample rate multiplied by oversample factor). DSA devices also employ fixed cutoff analog lowpass anti-aliasing filters. At low sample rates, some multiples of the oversample rate can fall below the analog anti-aliasing filter cut-off frequency.

For example, for a device using ADCs with an oversample factor of 128 f_s and sampling at a rate of 1 kS/s, the oversample rate is 128 kHz. Some multiples of that oversample rate fall below the cut-off frequency of the analog anti-aliasing filter. If the signal contains energy near these frequencies, aliasing can result.

You can prevent aliasing by raising the sample rate so that the first 128 f_s multiple falls above the cut-off frequency of the analog anti-aliasing filter. For example, a sample rate of 25.6 kS/s is not subject to aliasing because the first 128 f_s multiple, 3.2 MHz, is well above the analog anti-aliasing filter cut-off frequency. You can also enable low-frequency alias rejection with the AI.EnhancedAliasRejectionEnable property. This property causes the DSA device to automatically oversample for sample rates between 1 kS/s and 25.6 kS/s. The resulting oversampled rate always falls in the 25.6 kS/s to 51.2 kS/s range. The data stream is then decimated down by the same multiple to produce samples at the specified sample rate. Table 2-2 lists the decimation factors for given sample rates. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information about the AI.EnhancedAliasRejectionEnable property.

Table 2-2. Decimation Factors for Given Sample Rates

Sample Rate	Decimation Factor
100 S/s ≤ f_s ≤ 200 S/s	256
200 S/s < f_s ≤ 400 S/s	128
400 S/s < f_s ≤ 800 S/s	64
800 S/s < f_s ≤ 1.6 kS/s	32
1.6 kS/s < f_s ≤ 3.2 kS/s	16
3.2 kS/s < f_s ≤ 6.4 kS/s	8

Table 2-2. Decimation Factors for Given Sample Rates (Continued)

Sample Rate	Decimation Factor
6.4 kS/s < f_s ≤ 12.8 kS/s	4
12.8 kS/s < f_s ≤ 25.6 kS/s	2

Supported DSA Devices

Not all DSA devices support low-frequency alias rejection. The following list provides more information about which devices support low-frequency alias rejection:

- NI 446*x* devices
- NI PXI-447*x* devices revision H and later
- NI PCI-447*x* devices revision F and later
- NI PCI-4474 devices revision B and later
- NI 449*x* devices

Note The AI.EnhancedAliasRejectionEnable property is enabled by default for NI 446*x* and disabled for NI 447*x* and NI 449*x* (for rates above 1 kS/s) devices.

Filter Delay

The filter delay is the time required for data to propagate through a converter. All DSA device channels have filter delays due to the presence of filter circuitry on both input and output channels. To understand how a filter delay can affect your measurement, consider an ADC digital filter with a delay of 63 sample clock samples. At a 10 kS/s sample rate the signal experiences a delay equal to 6.3 ms.

The filter delay is an important factor for stimulus-response measurements, control applications, or any application where loop time is critical. You often might maximize the sample rate and minimize the time required for the filter delay.

The input filter delay also makes an external digital trigger appear to occur earlier than expected. The acquired buffer appears to begin earlier than expected because of some triggering and filter delay relationships.

Refer to the *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for information about filter delay for each device.

FIFO and PCI Data Transfer

DSA device input channels share a FIFO buffer, and the output channels share a separate FIFO buffer. The *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* contain information about the buffer sample depth.

The devices have a flexible data transfer request condition. You can program the device to request DMA transfers according to a user-programmable FIFO condition. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for information about conditions available for specific devices.

Note USB devices do *not* allow setting the transfer request condition.

Analog Output (NI USB-4431 and NI 4461 Only)

This section contains information about analog output concepts.

Output Distortion

You can minimize output distortion by connecting the outputs to external devices with a high input impedance. Each output channel of the NI 4461 is rated to drive a minimal load of 600 Ω. Each output channel of the NI 4431 is rated to drive a minimal load of 1 kΩ. However, you can achieve optimal performance with larger load resistances such as 10 kΩ or 100 kΩ. Refer to the *NI USB-443x Specifications and NI 446x Specifications* for more information.

Analog Output Channel Configurations

The NI 4461 supports two terminal configurations for analog output, differential and pseudodifferential. The term pseudodifferential refers to the fact that there is a 50 Ω or 1 kΩ resistor between the outer connector shell and chassis ground. The NI USB-4431 only supports pseudodifferential.

Note Attach all DSA devices to the chassis with screws to provide a reliable ground connection. If you are using a PXI device, be sure to tighten the screws at the top and bottom of the front face of the module. If you are using a PCI device, keep the screw that held the PCI slot cover to the computer chassis. Reinsert this screw to securely attach the device.

Choosing Channel Configurations

If the signal source or DUT inputs are floating, use the pseudodifferential configuration. You must provide a ground reference for a floating signal. If you do not provide a ground-reference point—for example, selecting differential mode with a floating microphone or shaker table input amplifier with differential inputs—the outputs or inputs can drift outside the device common-mode range.

For AO, if the DUT input is grounded, use the differential channel configuration. A grounded source or DUT is already connected to a ground-reference point with respect to the device, if the PXI or CompactPCI chassis and controller are plugged into the same power system.

Provide only one ground-reference point for each channel by properly selecting differential or pseudodifferential configuration. If you provide two ground-reference points—for example, if you select pseudodifferential mode with a grounded accelerometer or amplifier—the difference in ground potential results in currents in the ground system that can cause measurement errors. The 50 Ω or 1 kΩ resistor on the signal ground is usually sufficient to reduce this current to negligible levels, but results can vary depending on the system setup.

Configure the channels based on the signal source reference or DUT configuration. Refer to Table 2-3 to determine how to configure the channel.

Table 2-3. Analog Output

DUT Input Reference	Channel Configuration
Floating	Pseudodifferential
Grounded	Differential

The NI 446*x* is automatically configured for differential mode when powered on or powered off. This configuration protects the 50 Ω resistor on the negative pin.

Output Impedance

The differential output impedance between positive and negative signal legs is approximately 22 Ω when you generate a waveform. When you are not generating a waveform, configure the AO.IdleOutputBehavior property for one of the following three idle behavior options.

Table 2-4. Output Impedence

Idle Behavior Option	Output Impedance (Differential Mode Only)
`Maintain Existing Value`	22 Ω
`Zero Volts`	22 Ω
`High Impedance`	9 kΩ

DAC

The delta-sigma DACs on the NI 4461 function in a way analogous to delta-sigma ADCs. The digital data first passes through a digital interpolation filter, then to the DAC resampling filter, and finally to the delta-sigma modulator.

In the DAC, the delta-sigma modulator converts high-resolution digital data to high-rate, 1-bit digital data. As in the ADC, the modulator frequency shapes the quantization noise so that almost all of the quantization noise energy is above the Nyquist frequency.

The digital 1-bit data is then passed to an inherently linear 1-bit DAC. The output of the DAC includes quantization noise at higher frequencies, and some images still remain near multiples of eight times the effective sample rate.

Analog Output Filters

This section contains information about analog output filters.

Anti-Imaging and Interpolation Filters

A sampled signal repeats itself throughout the frequency spectrum, as shown in Figure 2-2. This figure shows how the signal repetitions begin above one-half the sample rate, f_s, and, theoretically, continue up through the spectrum to infinity. Images remain in the sampled data because the data actually represents only the frequency components below one-half f_s (the baseband). The device filters out the extra images in the signal in three stages.

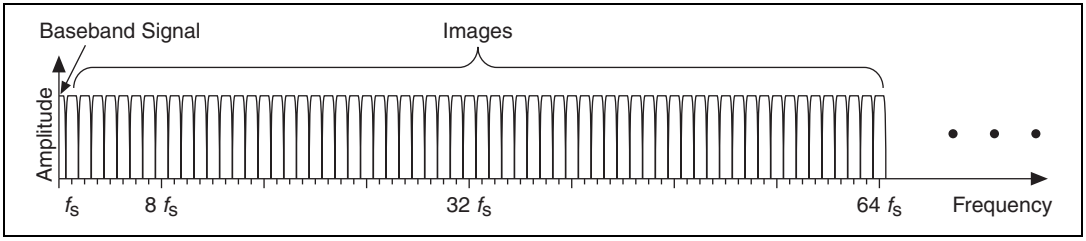


Figure 2-2. Sampled Signal

First, the data is digitally interpolated at 2^n times f_s, where n is a positive integer from 0 to 7. The interpolation factor must be sufficient to move the resulting effective sample rate (f_{es}) into the 102.4 kS/s or higher range. Figure 2-3 shows an example of four-times interpolation and the resulting images. A linear-phase digital filter then removes almost all energy above one-half f_s.

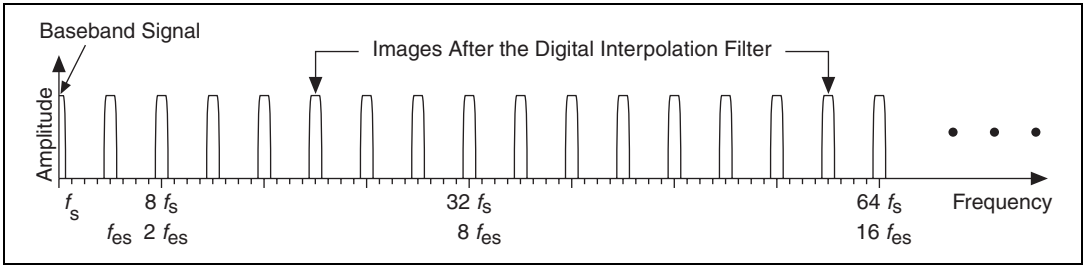


Figure 2-3. Signal After Digital Filter

Second, the DAC resamples the data to a new frequency (f_{DAC}). The frequency f_{DAC} is eight times higher than f_{es}. Figure 2-4 shows the resulting images.

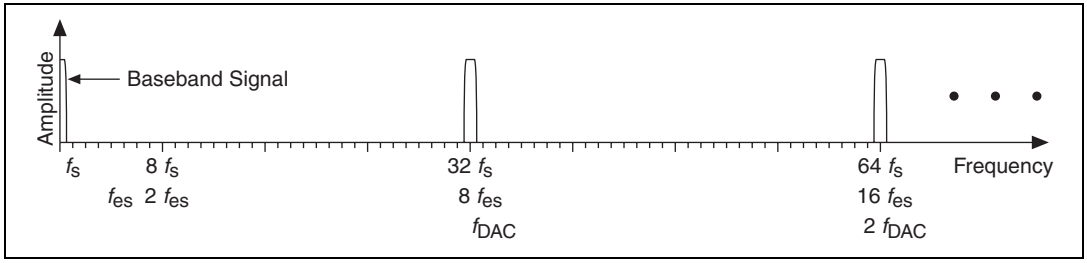


Figure 2-4. Images After DAC Filter

Some further (inherent) filtering occurs at the DAC because the data is digitally sampled and held at eight times f_{es}. This filtering has a sin*x*/*x* response, yielding nulls at multiples of eight times f_s, as shown in Figure 2-5.

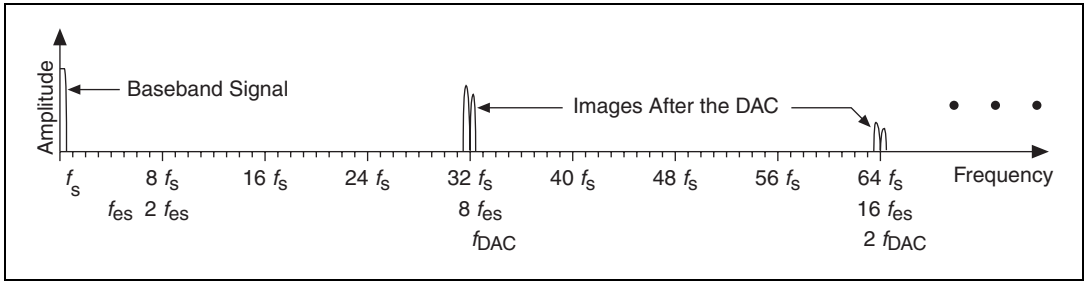


Figure 2-5. Signal After DAC

Third, a four-pole analog filter with a fixed cut-off at 243 kHz filters the remaining images, as shown in Figure 2-6.

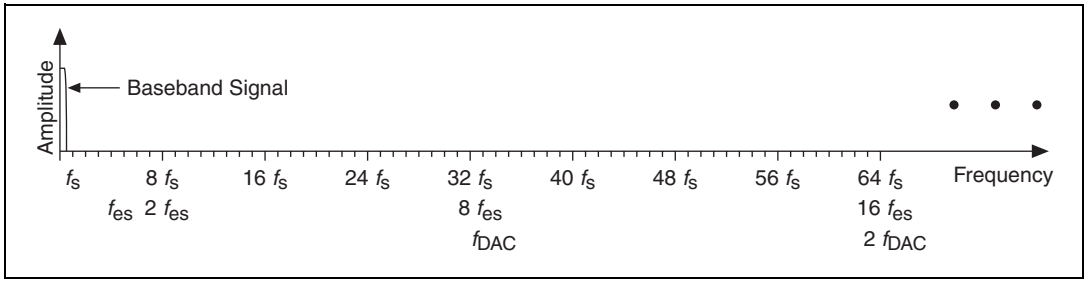


Figure 2-6. Signal After Analog Filters

Filter Delay

Output filter delay, the time required for digital data to propagate through the DAC and interpolation digital filters, varies depending on the update rate for DACs. For example, the filter delay at 10 kS/s for the NI 4461 is 38.5 update clock cycles. This signal experiences a delay equal to 3.85 ms. This delay is an important factor for stimulus-response measurements, control applications, or any application where loop time is critical. You often might want to maximize the sample rate and minimize the time required for 38.5 update clock cycles to elapse.

The interpolation filter adds additional output filter delay depending on the update rate. Table 2-5 provides more information on how the interpolation filter affects the output filter delay.

Table 2-5. Interpolation Factor and Output Filter Delay

Update Rate (kS/s)	Interpolation Factor	NI 4461 Output Filter Delay (Samples)	NI USB-4431 Output Filter Delay (Samples)
$1.0 \le f_s \le 1.6$	128	36.6	63.3
$1.6 < f_s \le 3.2$	64	36.8	62.6
$3.2 < f_s \le 6.4$	32	37.4	61.3
$6.4 < f_s \le 12.8$	16	38.5	58.5
$12.8 < f_s \le 25.6$	8	40.8	53
$25.6 < f_s \le 51.2$	4	43.2	42
$51.2 < f_s \le 102.4$	2	48.0	20
$102.4 < f_s \le 204.8$	1	32.0	Not Supported

FIFO and PCI Data Transfer

DSA device input channels share a FIFO buffer, and the output channels share a separate FIFO buffer. The *NI USB-4431* and *NI 446x Specifications* contain information about the buffer sample depth.

The NI 4461 has a flexible data transfer request condition. You can program the device to request DMA transfers according to a user-programmable FIFO condition. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for information about conditions available for specific devices.

Note USB devices do *not* support setting the transfer request condition.

Power Off and Power Loss

When the NI USB-4431 and NI 4461 are powered down or lose power, the output channels assume a high-impedance state. The NI 4461 for instance, drops to 0.0 V in approximately 8 µs. Figure 2-7 illustrates the typical behavior of an NI USB-4431 and NI 4461 generating 10 V when powered off or when the device loses power.

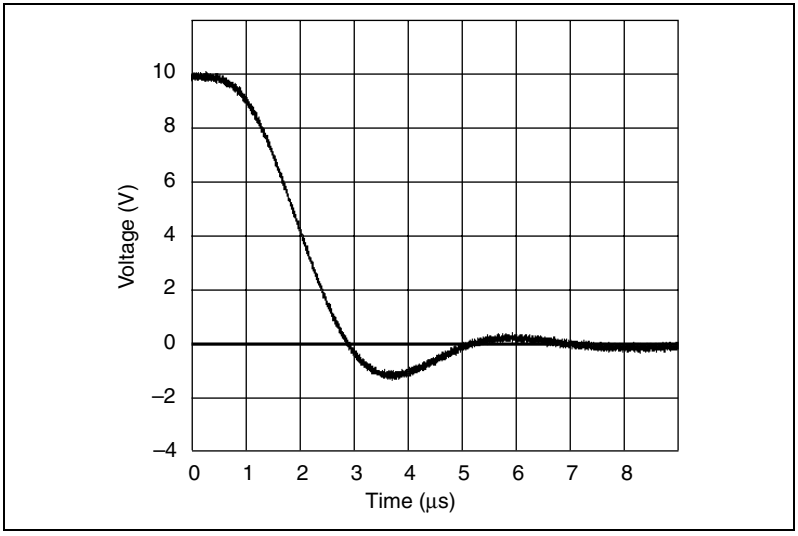


Figure 2-7. Power Off and Power Loss Behavior

Timing and Triggering

This section contains information about timing and triggering theory of operation.

Sample Clock Timebase

The ADCs and DACs require an oversample clock to drive the conversion. The oversample clock frequency is greater than the sample rate. The oversample clock is produced from the sample clock timebase, an even higher frequency signal. The timing information for all ADCs and DACs comes from the common sample clock timebase signal. You can share the sample clock timebase among synchronized devices. Refer to the *Master Sample Clock Timebase Synchronization* section of this chapter for more information.

Note USB devices do *not* support synchronization.

A DDS chip produces the sample clock timebase. DDS is a method of generating a programmable clock with excellent frequency resolution. The DDS chip is capable of 32-bit resolution and can produce 4,294,967,296 steps to create the sample clock timebase. Refer to the *NI USB-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for more information about device frequency resolution.

External Clock

The sample clock timebase, which drives the conversion on DSA devices, has stringent requirements for frequency and stability. DSA devices do not accept arbitrary clock signals from external sources such as encoders or tachometers. However, signal processing features in the Sound and Vibration Measurement Suite often provide an excellent alternative to external clocking in encoder and tachometer applications. Visit `ni.com/soundandvibration` for more information about the Sound and Vibration Measurement Suite.

Note **(NI USB-4431 and NI 4461)** You can run input and output operations simultaneously at different rates on the NI USB-4431 and NI 4461. However, because the timing information for all operations is derived from a common sample clock timebase, the ratios between input and output sample rates can differ only by a factor of 2^n, where n is an integer. For example, assume that the input sample rate is 8 kS/s. Valid output sample rates include, but are not limited to, 2 kS/s, 8 kS/s, 16 kS/s, and 64 kS/s. In this case, 20 kS/s is not a valid output sample rate, because the ratio between 8 kS/s and 20 kS/s is not a power of 2.

Sharing the Sample Clock Timebase

When you synchronize two or more DSA devices, they must share a common sample clock timebase. Each device uses the sample clock timebase to generate input and output sample clocks. This common signal passes along the PXI_Star/RTSI trigger bus. You can program the master device to export the internally generated sample clock timebase to slave devices.

You *must* configure the slave devices to import the sample clock timebase. Programming multiple DSA devices to share a common sample clock timebase provides tight synchronization and eliminates clock drift between devices.

The ratio between the sample rate (f_s) and sample clock timebase rate (f_{tb}) can have one of several values. Refer to the *NI 446x Specifications*, *NI 447x Specifications*, or *NI 449x Specifications* for more information.

Triggering

This section contains information about triggering theory of operation.

Digital Triggering

You can configure DSA devices to start an acquisition in response to a digital trigger signal on the PFI 0 connector, located on the device front panel. This pin is labeled EXT TRIG on NI 447*x* devices, and it is labeled PFI0 on NI 446*x* and NI 449*x* devices. The trigger circuit can respond either to a rising or a falling edge. The trigger signal must comply to TTL voltage levels. Refer to the *NI UBS-443x Specifications, NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for additional trigger requirements.

DSA devices also offer digital triggering in response to signals on the PXI or RTSI trigger bus. Use any line from PXI_Trig<0..6> or RTSI<0..6>. One exception applies—when synchronizing multiple NI PXI-447*x* devices, PXI_Trig 5 is reserved for internal use. As with external digital triggering, you can program the device to respond to either the rising or falling signal edge.

Note The NI USB-443*x* devices have eight PFI lines for triggering.

Analog Triggering

You can configure the DSA device analog trigger circuitry to monitor any input channel from which you acquire data. Choosing an input channel as the trigger channel does not influence the input channel acquisition capabilities.

The trigger circuit generates an internal digital trigger based on the input signal and the user-defined trigger levels. For example, you can configure the device to start acquiring samples after the input signal crosses a specific threshold. You also can route this internal trigger to the PXI or RTSI trigger bus to synchronize the start of the acquisition operation by one device with the operation of other devices in the system.

During repetitive triggering on a waveform, you might observe jitter because of the uncertainty of where a trigger level falls compared to the actual digitized data. Although this trigger jitter is never greater than one sample period, it might be significant when the sample rate is only twice the bandwidth of interest. This jitter usually has no effect on data processing, and you can decrease this jitter by sampling at a higher rate.

You can use several analog triggering modes with DSA devices, including analog edge, analog edge with hysteresis, and window triggering.

Analog Edge Triggering

For analog edge triggering, configure the device to detect a certain signal **Level** and slope, either rising or falling. Figure 2-8 shows an example of rising edge analog triggering. The trigger asserts when the signal starts below **Level** and then crosses above **Level**.

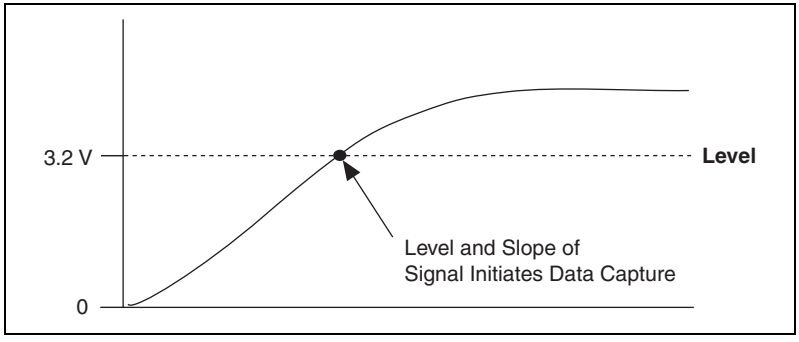


Figure 2-8. Analog Trigger Level

Analog Edge Triggering With Hysteresis

When you add hysteresis to analog edge triggering, you add a window above or below the trigger level. This trigger often is used to reduce false triggering due to noise or jitter in the signal. For example, if you add a hysteresis of 1 V to the example in Figure 2-8, which uses a level of 3.2 V, the signal must start at or drop below 2.2 V to arm the trigger. The trigger asserts when the signal rises above 3.2 V and deasserts when it falls below 2.2 V, as shown in Figure 2-9.

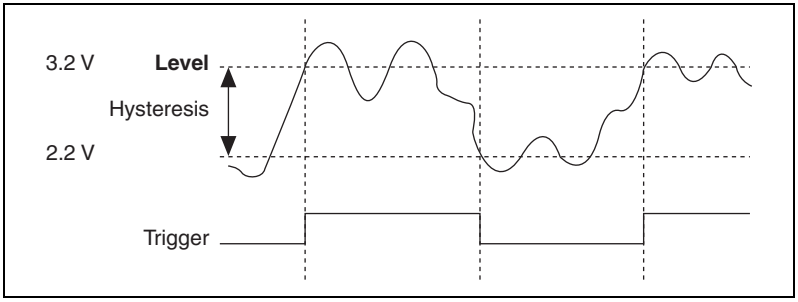


Figure 2-9. Analog Edge Triggering with Hysteresis on Rising Slope

When using hysteresis with a falling slope, the trigger is armed when the signal starts above **Level**, plus the hysteresis value, and asserts when the signal crosses below **Level**. For example, if you add a hysteresis of 1 V to a level of 3.2 V, the signal must start at or rise above 4.2 V to arm the trigger. The trigger asserts as the signal falls below 3.2 V and deasserts when it rises above 4.2 V, as shown in Figure 2-10.

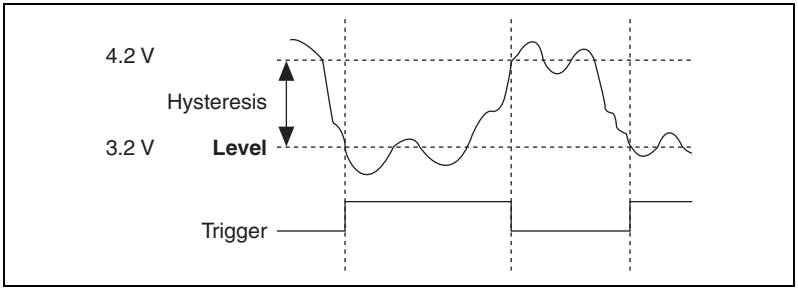


Figure 2-10. Analog Edge Triggering with Hysteresis on Falling Slope

Window Triggering

A window trigger occurs when an analog signal either passes into (enters) or passes out of (leaves) a window defined by two levels. Specify the levels by setting a value for the top and bottom window boundaries. Figure 2-11

demonstrates a trigger that acquires data when the signal enters the window. You can also program the trigger circuit to acquire data when the signal leaves the window.

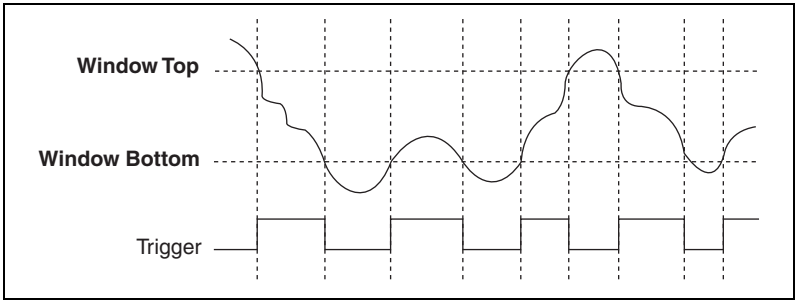


Figure 2-11. Window Triggering

Triggering and Filter Delay

Analog and digital triggering exhibit different behaviors with respect to the filter delay in the ADC.

When you use digital triggering, the ADCs begin generating digital data immediately after receiving the digital trigger signal. However, the analog signal entering the ADCs is still subject to the filter delay. This circumstance means that when the trigger is received, the analog levels at the front of the ADCs are not digitized until a certain number of sample intervals later. You can observe this behavior with an experiment. Connect the same TTL signal to the external digital trigger input and to an AI channel. Configure the acquisition to respond to a digital trigger. The rising edge of the trigger does not appear in the digitized waveform until a specific number of samples pass. Refer to the *NI USB-443x Specifications*, *NI 446x Specifications*, *NI 447x Specifications*, and *NI 449x Specifications* for more information about filter delay.

Analog triggering is performed on the digital output of the ADC. The analog trigger circuit on a DSA device is a digital comparator. Because the trigger is located after the ADC in the signal path, the filter delay is not evident in the acquired data. If the analog trigger is configured with a rising edge and a level of 1.0 V, the voltage of the first sample is just above 1.0 V.

Note (NI USB-4431 and NI 4461) You must also consider the AO filter delay in your application. The digital filter introduces a deterministic delay during AO operations.

Synchronization

Some applications require tight synchronization between input and output operations on multiple devices. Synchronization is important to minimize skew between channels or to eliminate clock drift between devices in long-duration operations. You can synchronize the analog input and output operations on two or more DSA devices to extend the channel count of DSA measurements. Table 2-6 lists possible DSA device synchronization configurations to help you decide which method of synchronization to use.

Note This section discusses synchronizing only DSA devices. You can synchronize other NI products with DSA devices, but the DSA device must be the master device. Refer to the NI Developer Zone at `ni.com/zone` for more information about synchronizing other devices with DSA devices.

Table 2-6. Supported DSA Device Synchronization Configuration

Configuration	Reference Clock (PXI Only)	Master Sample Clock Timebase
449*x* and 449*x*	Supported	—
446*x* and 446*x*	Supported	Supported
447*x* and 447*x*	—	Supported
449*x* and 446*x*	Supported	—
449*x* and 447*x*	—	—
446*x* and 447*x*[*, †]	—	Supported

[*] Multrate synchronization is not supported.

[†] The NI 446*x* must be the master DSA device.

Note: NI USB-443*x* devices do not support synchronization.

Reference Clock Synchronization (PXI, PXIe Only)

With reference clock synchronization, master and slave devices lock their ADC or DAC over the sample clock to the shared 10 MHz reference clock on the PXI and PXIe chassis backplane (PXI_CLK10). The chassis supplies the clock independently to each peripheral slot. An independent buffer drives the clock signal to each peripheral slot. DSA devices that can synchronize with this method have phase-locked loop (PLL) circuitry that allows them to lock to the reference clock. You can drive PXI_CLK10 from

an external source through the PXI_CLK_IN pin on the P2 connector of the star trigger slot on the chassis. Driving an external clock source on this pin automatically disables the 10 MHz source generated on the PXI backplane. You can place the master and slave devices in any slot. You also can synchronize all devices in the chassis.

After you install the DSA devices in the chassis, complete the following steps to synchronize the hardware.

1. Specify PXI_CLK10 as the reference clock source for all devices to force the DSA devices to lock to the reference clock on the PXI chassis.
2. Choose an arbitrary master board to issue a synch pulse on one of the PXI Trigger lines. The sync pulse resets the ADCs and DACs and also resets the divide counter to phase align all the clocks in the system to within nanoseconds.
3. Start acquiring data on all DSA devices simultaneously. Force one DSA device to export the start trigger on one of the PXI Trigger lines for a PXI system. The device does not have to be the master to send the start trigger. Any device in the test system now can begin the acquisition.

Consider the following caveats to using Reference Clock synchronization:

- Not all DSA devices support low-frequency alias rejection. When you synchronize multiple DSA devices, you must verify that all the devices share the same low-frequency alias rejection setting. You can enable low-frequency alias rejection if all of the DSA devices in the system support it. Disable low-frequency alias rejection on all devices when at least one DSA devices does not support it.
- Inherent delays exist between different families of DSA boards. You might need to compensate for group delay in the waveforms when you synchronize between device families.
- At very low sample rates, you might notice that it takes several seconds for an acquisition to begin. This is because during the sync pulse, the ADCs get reset and have to wait many samples before delta sigmas are operational. That time is dependant on the sample rate. To improve the time it takes an acquisition to begin, select a higher sample rate or enable low frequency alias rejection if possible on all boards. This causes the ADC to run at a higher sample rate, while the onboard firmware decimates the data back to your low sample rate.
- For configurations that specify multiple sample rates between different devices, the slave devices must be a power of two of the master device sharing the clock. For example, if the master device has a sample rate

of 100 kS/s, the slave devices can run at 50 kS/s, 25 kS/s, or 200 kS/s but not at 40 kS/s. The slowest sample rate device in the system must export the start trigger. Because the delta sigmas run at different rates, you have different group delays among all devices running at different rates.

Master Sample Clock Timebase Synchronization

Master Sample Clock Timebase synchronization occurs with one DSA device exporting its Sample Clock Timebase signal to all other devices in the system. For a PXI system, the master device must reside in the master timebase slot of the chassis, because the master timebase slot has specific point-to-point routing, called PXI Star, to slots 3 through 14 on which it exports the clock. A PXI system cannot synchronize boards with master sample timebase synchronization beyond slot 14. For PCI devices, the clock is physically exported through a RTSI cable that you must attach to the back of all the devices in the system.

After you install the DSA devices, complete the following steps to synchronize the hardware.

1. Program the master device to share its Sample Clock Timebase to all the slave devices. This shared clock guarantees that all ADC and DAC clocks share the same frequency. The signal is routed on PXI Star for PXI systems and any of the RTSI lines for PCI systems. The default RTSI line is 8.
2. Program the master device to route a sync pulse to all the slave boards. For PXI systems, you can use any of the PXI trigger lines to do this. For PCI devices, the default RTSI line is 9, but you can program another line. The sync pulse first resets the ADCs and DACs in the entire system at the same time, then phase aligns all the clocks on the board to within nanoseconds.
3. Start acquiring on all boards simultaneously. Force one device to export its start trigger on one of the PXI trigger lines for a PXI system, or one of the RTSI lines 0 to 6 for a PCI system. The device does not have to be the master to send the start trigger. Any device in the test system now can begin the acquisition.

Consider the following caveats to using Master Sample Timebase synchronization:

- Not all DSA devices support low-frequency alias rejection. When you synchronize multiple DSA devices, you must verify that all the devices share the same low-frequency alias rejection setting. You can enable low-frequency alias rejection if all of the DSA devices in the system support it. Disable low-frequency alias rejection on all devices when you synchronize DSA devices that do not support low-frequency alias rejection.
- Inherent delays exist between different between families of DSA boards. You might need to compensate for group delay in the waveforms when you synchronize between device families.
- At very low sample rates, you might notice that it takes several seconds for an acquisition to begin. This is because during the sync pulse, the ADCs get reset and have to wait many samples before delta sigmas are operational. That time is dependant on the sample rate. To improve the time it takes an acquisition to begin, select a higher sample rate or enable low frequency alias rejection if possible on all boards. This causes the ADC to run at a higher sample rate, while the onboard firmware decimates the data back to your low sample rate.
- For configurations that specify multiple sample rates between different devices, the slave devices must be a power of two and slower than the master device sharing the clock. For example, if the master device has a sample rate of 100 kS/s, the slave devices can run at 50 kS/s or 25 kS/s but not at 40 kS/s or 200 kS/s. The slowest sample rate device in the system must export the start trigger. Because the delta sigmas run at different rates, you have different group delays among all devices running at different rates.

3

Developing Your Dynamic Signal Acquisition Application

This chapter contains information about developing applications with Dynamic Signal Acquisition (DSA) devices.

Creating a Task Using the DAQ Assistant

Using the DAQ Assistant to create and configure a task allows you to save several programming steps in your application. In addition, you can save the task for use in future applications. You can use tasks you create with the DAQ Assistant with any NI application software you use to control a DSA device. You can launch the DAQ Assistant from any NI application software.

If you are programming in LabVIEW, you can take advantage of the DAQ Assistant Express VI to further simplify your application. The DAQ Assistant Express VI allows you to perform a complete analog input or analog output operation using a single VI on the LabVIEW block diagram. The DAQ Assistant Express VI uses the DAQ Assistant to create and configure a task and also handles task execution. Refer to the *LabVIEW Help* for more information about the DAQ Assistant Express VI.

Refer to your NI application software documentation for specific information about launching the DAQ Assistant. Refer to the *DAQ Assistant Help* for more information about using the DAQ Assistant.

Analog Input Applications

This section contains information about developing analog input applications with DSA devices.

Analog Input Application Overview

This section presents some general overview information about creating an analog input application using NI-DAQmx and LabVIEW or LabWindows/CVI.

Figure 3-1 shows a typical flowchart for programming an analog input task, taking a measurement, and clearing the task.

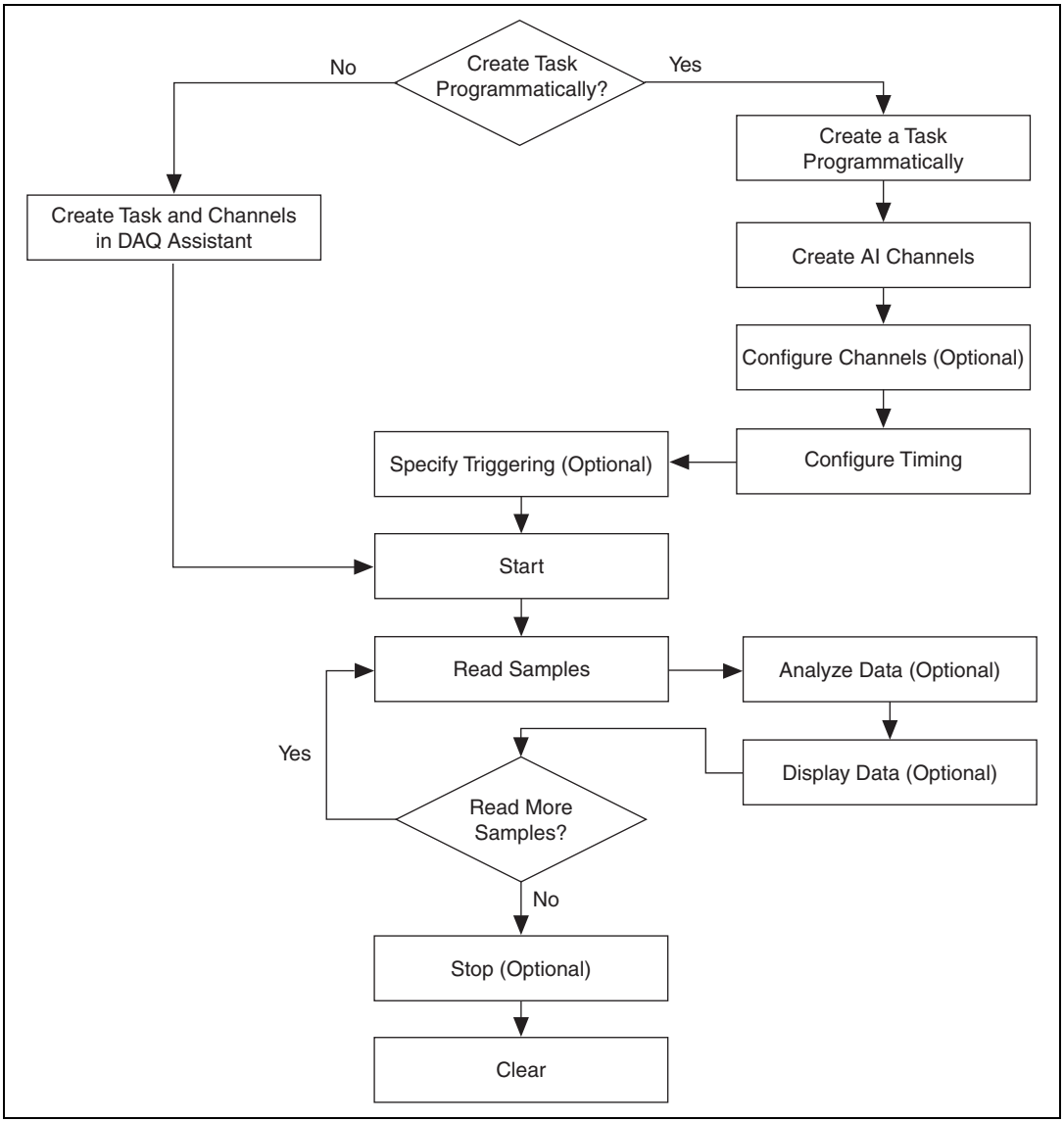


Figure 3-1. Analog Input Task Flowchart

Table 3-1 describes in more detail the steps outlined in the previous figure. Some steps might be optional, depending on your application. Refer to your NI application software for more information about each step.

Table 3-1. Analog Input Application Steps

Flowchart Step	LabVIEW Step	LabWindows/CVI Step
Create Task	Create a task using the DAQ Assistant *or* Create a task programmatically using the following VIs: • DAQmx Create Task VI* • DAQmx Create Virtual Channel VI • DAQmx Timing VI • DAQmx Triggering VI*	Create a task using the DAQ Assistant *or* Create a task programmatically using the following functions: • `DAQmxCreateTask` • `DAQmxCreateAIVoltageChan` • `DAQmxCfgSampClkTiming` • `DAQmxAnlgEdgeStartTrig`* *or* • `DAQmxCfgDigEdgeStartTrig`*
Configure Channels	One or more channel property node(s)†	One or more calls to `DAQmxSetChanAttribute`†
Start Measurement*	DAQmx Start Task VI	`DAQmxStartTask`
Read Measurement	DAQmx Read VI	`DAQmxReadAnalog64` or other data reading function
Analyze Data	Common analysis tools include VIs from the Sound and Vibration Measurement Suite or Waveform Measurement Functions‡	Common analysis tools include the functions in the LabWindows/CVI Advanced Analysis Library‡
Display Data	Front panel graph, chart, or indicator	Graphical User Interface (GUI) graph, chart, or indicator
Continue Sampling	Loop around DAQmx Read VI	Loop around `DAQmxReadAnalog64` or other data reading function
Stop Measurement*	DAQmx Stop Task VI	`DAQmxStopTask`

Table 3-1. Analog Input Application Steps (Continued)

Flowchart Step	LabVIEW Step	LabWindows/CVI Step
Clear Task	DAQmx Clear Task VI	`DAQmxClearTask`

* These steps might be optional depending on your application.

† Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information about NI-DAQmx properties.

‡ This library requires either the Full or Professional Development System of the NI application software.

Note Table 3-1 provides example functions for LabWindows/CVI. In most cases, LabWindows/CVI code ports directly to other ANSI C environments including Microsoft Visual C++. If you are using other text-based application software, including NI Measurement Studio in a .NET environment, you might need to make minor changes in the function syntax.

Refer to your application software or the *Analog Input Application Examples* section of this chapter to view some example analog input applications.

Analog Input Application Examples

NI-DAQmx and all NI ADEs ship with examples you can use to get started with your application.

LabVIEW Examples

The following LabVIEW examples illustrate common DSA analog input applications:

- Example Acceleration Application—Cont Acq Accel Samples-Int Clk-Analog Start VI located in `labview\examples\DAQmx\Analog In\Measure Acceleration.llb`
- Example Sound Pressure Application—Cont Acq Snd Pressure Samples-Int Clk VI located in `labview\examples\DAQmx\Analog In\Measure Sound Pressure.llb`

LabWindows/CVI Examples

The following LabWindows/CVI examples in the CVI folder illustrate common DSA analog input applications:

- Example Acceleration Application—`samples\DAQmx\Analog In\Measure Acceleration\Cont Accel Samps-Int Clk-Anlg Start`
- Example Sound Pressure Application—`samples\DAQmx\Analog In\Measure Sound Pressure\Cont Acq Snd Press Samps-Int Clk`

Analog Output Applications (NI USB-4431 and NI 4461 Only)

This section contains information about developing analog output applications with DSA devices.

Analog Output Application Overview

This section presents some general overview information about creating an analog output application using NI-DAQmx and LabVIEW or LabWindows/CVI.

Figure 3-2 shows a typical flowchart for programming an analog output task, generating a waveform, and clearing the task.

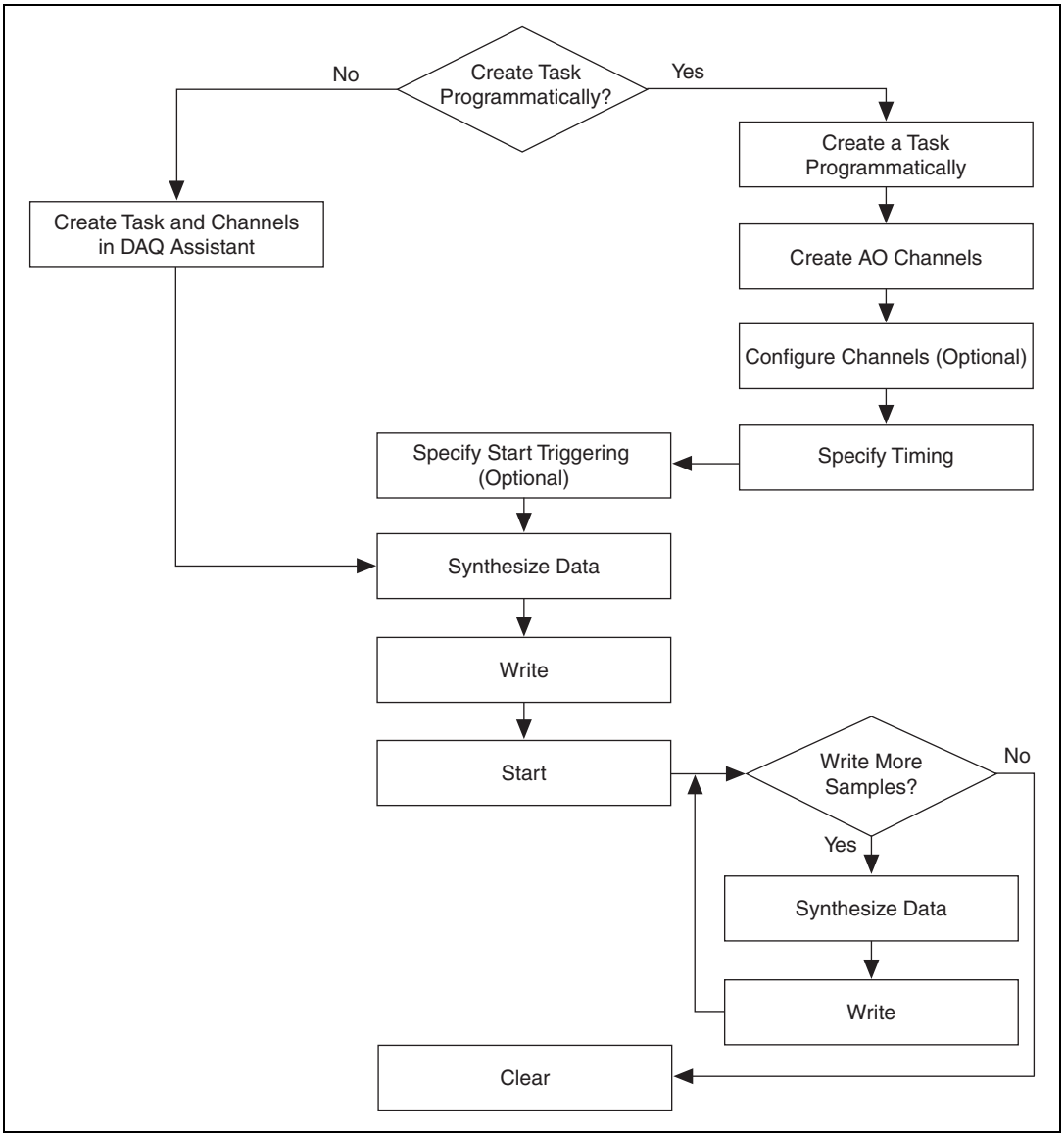


Figure 3-2. NI 4461 Analog Output Task Flowchart

Table 3-2 describes in more detail the steps outlined in Figure 3-2. Some steps might be optional, depending on your application. Refer to your NI application software documentation for more information about each step.

Table 3-2. Analog Output Application Steps

Flowchart Step	LabVIEW Step	LabWindows/CVI Step
Create Task	Create a task using the DAQ Assistant *or* Create a task programmatically using the following VIs: • DAQmx Create Task VI* • DAQmx Create Virtual Channel VI • DAQmx Timing VI • DAQmx Triggering VI*	Create a task using the DAQ Assistant *or* Create a task programmatically using the following functions: • `DAQmxCreateTask` • `DAQmxCreateAOVoltageChan` • `DAQmxCfgSampClkTiming` • `DAQmxAnlgEdgeStartTrig`* *or* • `DAQmxCfgDigEdgeStartTrig`*
Configure Channels	One or more channel property node(s)†	One or more calls to `DAQmxSetChanAttribute`
Synthesize Data*	Common tools include VIs from the Sound and Vibration Measurement Suite or Waveform Measurement VIs†	Common analysis tools include the functions in the LabWindows/CVI Advanced Analysis Library†
Write Data	DAQmx Write VI	`DAQmxWriteAnalog64` or other data writing function
Start Generation	DAQmx Start Task VI	`DAQmxStartTask`
Continue Generation*	Loop around data synthesis and DAQmx Write VI	Loop around data synthesis and `DAQmxWriteAnalog64` or other data writing function
Stop Generation*	DAQmx Stop Task VI	`DAQmxStopTask`
Clear Task	DAQmx Clear Task VI	`DAQmxClearTask`

* These steps might be optional depending on your application.

† This library requires either the Full or Professional Development System of the NI application software.

Note Table 3-2 provides example functions for LabWindows/CVI. In most cases, LabWindows/CVI code ports directly to other ANSI C environments including Microsoft Visual C++. If you are using other text-based application software, including NI Measurement Studio in a .NET environment, you might need to make minor changes in the function syntax.

Refer to your application software or the *Analog Output Application Examples* section of this chapter to view some example analog output applications.

Analog Output Application Examples

NI-DAQmx and all NI ADEs ship with examples you can use to get started with your application.

LabVIEW Example

The following LabVIEW example illustrates a common continuous generation application:

Example Generation Application—Cont Gen Voltage Wfm-Int Clk-Non Regeneration VI located in `labview\examples\DAQmx\Analog Out\Generate Voltage.llb`

LabWindows/CVI Example

The following LabWindows/CVI example in the CVI folder illustrates a common continuous generation application:

Example Generation Application—`samples\DAQmx\Analog Out\Generate Voltage\Cont Gen Volt Wfm-Int Clk`

Synchronization Applications

This section contains information about developing synchronization applications with DSA devices.

Note USB devices do *not* support synchronization.

Synchronization Application Overview

Due to the many synchronization configurations possible, there is no way to present a general overview of how to construct a synchronization application. It is important to know the theory behind the configurations,

signals involved, and any applicable rules when constructing a synchronization application. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about synchronization theory.

Use the synchronization examples to help you get started with your synchronization application. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information about software steps necessary for synchronizing DSA devices.

Synchronization Application Examples

NI-DAQmx and all NI ADEs ship with examples you can use to get started with your application.

LabVIEW Examples

The following LabVIEW examples illustrate synchronized analog input and output applications:

- Example Analog Input Synchronization Application—Multi Device Sync-AI-Shared Timebase & Trig-DSA VI located in `labview\examples\DAQmx\Synchronization\Multi-Device.llb`
- Example Analog Output Synchronization Application—Multi Device Sync-AI and AO-Shared Timebase & Trig-DSA VI located in `labview\examples\DAQmx\Synchronization\Multi-Device.llb`

LabWindows/CVI Example

The following LabWindows/CVI example in the CVI folder illustrates a synchronized DSA analog input application:

Example Analog Input Application—`samples\DAQmx\Synchronization\Multi-Device\AI-Shared Timebase & Trig-DSA`

A

Device-Specific Information

This appendix contains information about specific National Instruments Dynamic Signal Acquisition (DSA) devices.

Note Refer to `ni.com/manuals` for documentation for devices not listed here.

NI 446*x* Devices

This section contains information about the NI 446*x* devices.

NI 446*x* Features

The NI 446*x* devices are high-performance, high-accuracy analog devices for PCI and PXI. The NI 4461 devices feature two analog input and two analog output channels with gain and attenuation. The NI 4462 features four analog input channels. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about analog input, analog output, gain, attenuation, and other feature concepts.

NI 446*x* Analog Input Features

Figure A-1 shows the NI 446*x* analog input circuitry block diagram.

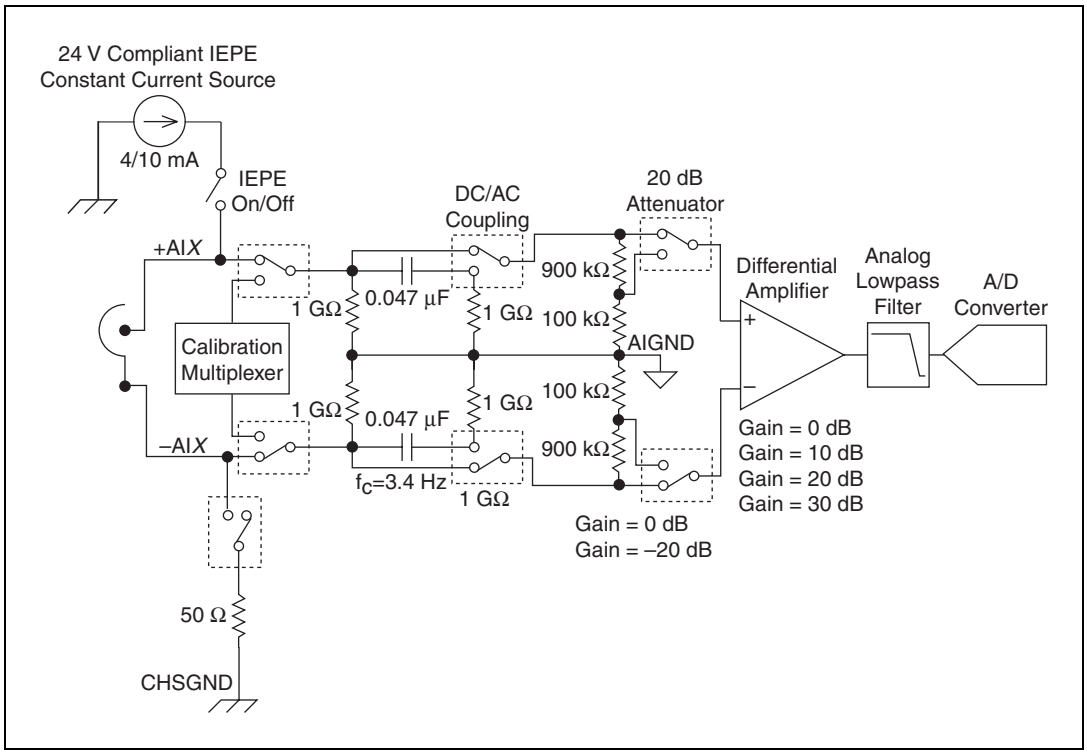


Figure A-1. NI 446*x* Analog Input Block Diagram

The NI 446*x* input channels feature the following:

- Sampling rates up to 204.8 kS/s
- Per channel selection of six input voltage ranges from ±0.316 V to ±42.4 V_{pk}
- Per channel differential and pseudodifferential channel configuration
- Per channel AC or DC coupling
- Per channel IEPE current excitation
- Pre-digitization and post-digitization overload detection
- Anti-alias filtering
- Multiple triggering modes, including external digital triggering

NI 4461 Analog Output Features

Figure A-2 shows the NI 4461 analog output circuitry block diagram.

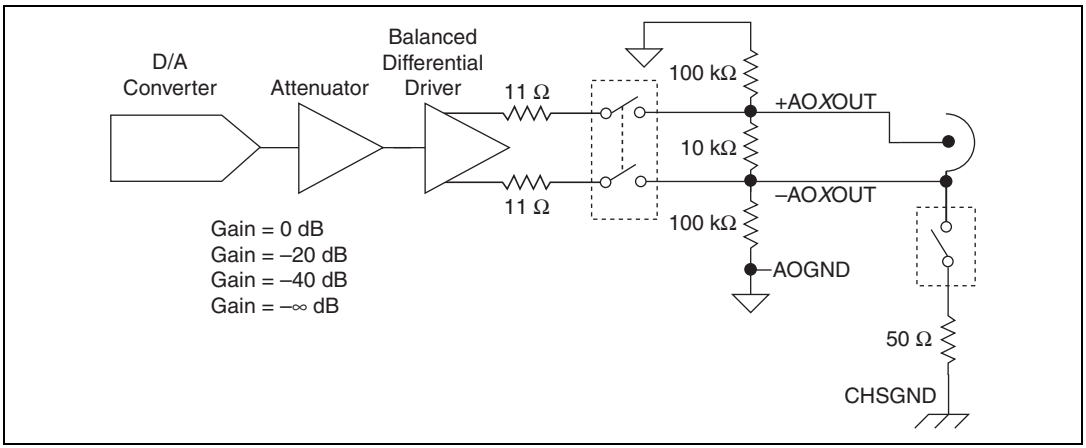


Figure A-2. NI 4461 AO Block Diagram

The NI 4461 output channels feature the following:

- Update rates to 204.8 kS/s
- Per channel selection of three output voltage ranges from ±10 V to ±0.1 V
- Per channel differential and pseudodifferential channel configuration
- Anti-image filtering
- External digital triggering

NI 446*x* Gain and Attenuation

Positive gain values amplify the signal before the A/D converter (ADC) digitizes it. This signal amplification reduces the measurement range. However, amplifying the signal before digitization allows better resolution by strengthening weak signal components before they reach the ADC. Conversely, negative gains attenuate the signal before they reach the ADC. This attenuation increases the effective measurement range, though it sacrifices some resolution for weaker signal components. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about ADCs.

Note In this manual, AI attenuation is referred to as gain with a negative value. You can set attenuation directly in software by assigning a negative value to the AI.Gain property. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

The NI 446*x* has six available gain settings for each AI channel. Each gain setting corresponds to a particular AI range, and each range is centered on 0 V. The gain settings are specified in decibels, where the 0 dB reference is the default input range of ±10 V. Refer to the *NI 446x Specifications* for detailed information about each gain setting and corresponding range.

Caution The range for the −20 dB setting corresponds to a maximum input range of ±42.4 V_{pk}. Setting the gain to −20 dB attenuates the signal by a factor of 10, implying a maximum ADC range of ±100 V. However, the analog front-end circuitry is not rated beyond ±42.4 V_{pk}. When you use this gain setting, the ADC does not saturate at ±42.4 V_{pk}; however, you risk damaging the measurement system or creating a possible safety hazard if you exceed the maximum rated input of ±42.4 Vpk.

Table A-1 shows the gain setting sources.

Table A-1. Gain Setting Sources

Gain Setting (dB)	Source
0, 10, 20, 30	Differential amplifier
−10	Combination of −20 and 10 gains
−20	Resistor divider network

In general, select the voltage range that provides the greatest dynamic range and the least distortion. For example, consider an accelerometer with a 100 mV/g sensitivity rating with an absolute maximum output voltage of 5 Vpk. In this case, the ±10 Vpk is appropriate, corresponding to 0 dB gain. However, the ±3.16 Vpk setting maximizes the dynamic range if you know the stimulus is limited to, for example, 20 g or 2 Vpk.

Minimize system distortion by providing sufficient headroom between the stimulus setting, 2 Vpk in this instance, and the range. Choose the next highest range setting above the peak level you expect to measure to provide sufficient headroom. In applications where distortion performance is critical, you can sacrifice overall dynamic range to improve distortion performance by selecting the ±10 Vpk setting. Refer to the *NI 446x Specifications* for distortion specifications for each gain setting.

The ADC is the most significant source of measurement noise until you use the 20 dB or 30 dB gain settings. At these higher gain settings, the analog front-end circuitry becomes the dominant noise source. To achieve the best absolute noise performance, select the highest gain setting appropriate for your application.

NI 446*x* Block Diagrams

This section contains the NI 446*x* block diagrams.

NI 4461 Block Diagram

Figure A-3 shows the NI 4461 block diagram.

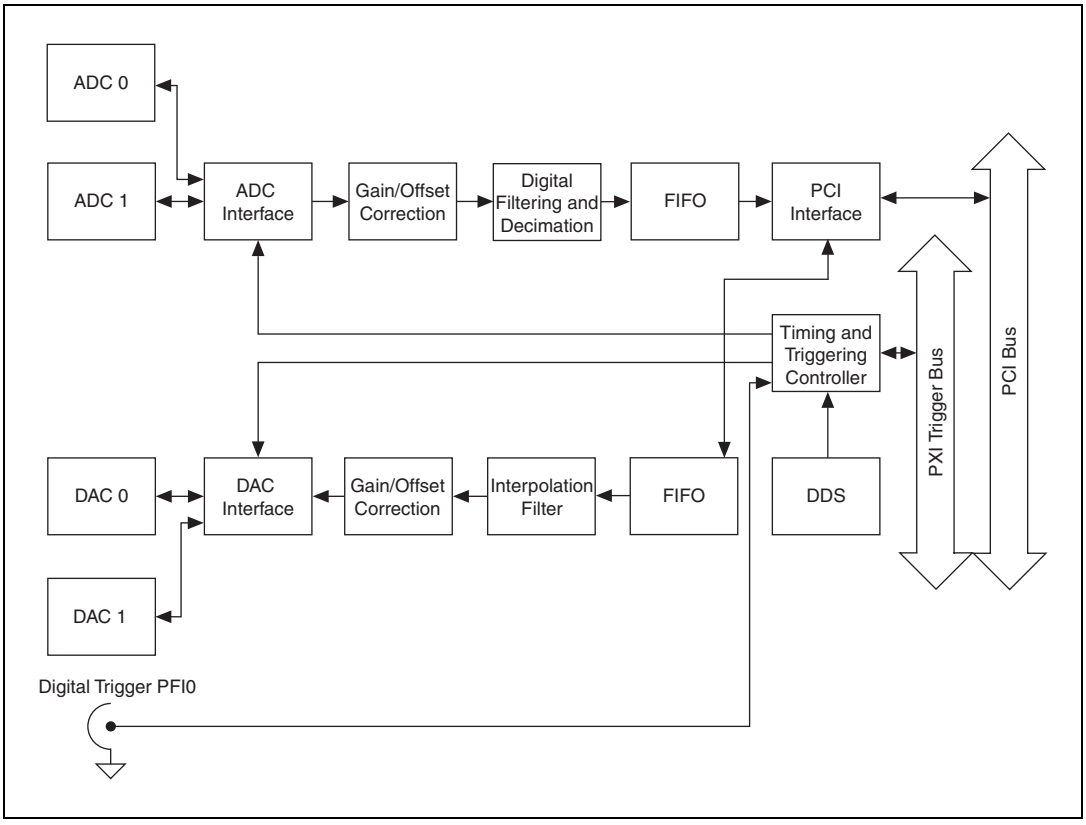


Figure A-3. NI 4461 Block Diagram

NI 4462 Block Diagram

Figure A-4 shows the NI 4462 block diagram.

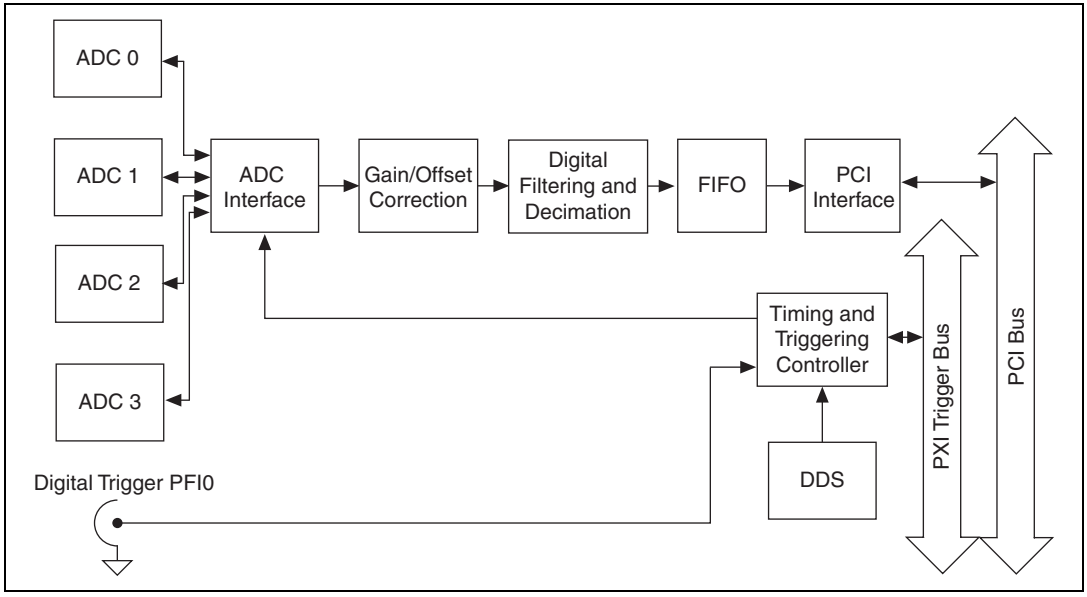


Figure A-4. NI 4462 Block Diagram

Connecting Signals to NI 446*x* Devices

This section contains information about connecting signals to NI 446*x* devices.

NI 446*x* Front Panels

Figure A-5 shows the NI PXI-4461, NI PCI-4461, NI PXI-4462, and NI PCI-4462 front panels.

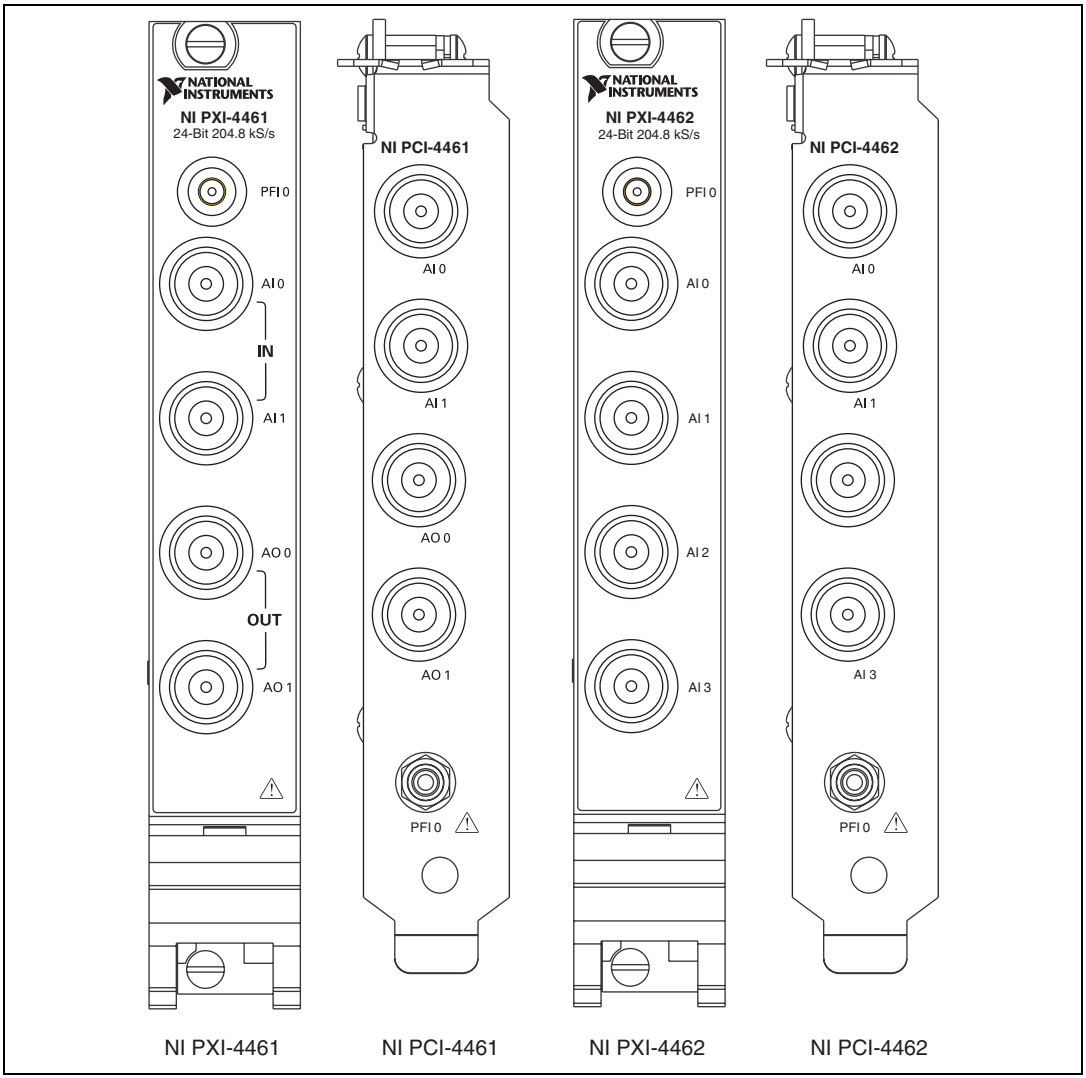


Figure A-5. NI 446*x* Front Panels

BNC Connector Polarity

Figure A-6 shows the BNC connector polarity for all NI 446*x* devices.

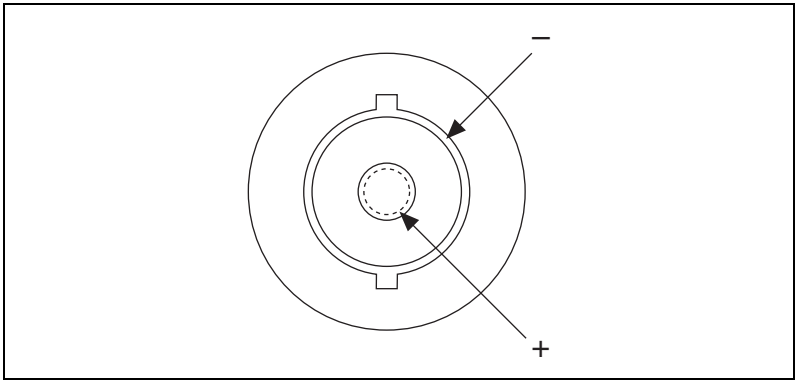


Figure A-6. BNC Connector Polarity for NI 446*x* Devices

NI 446*x* Input Connections

Figure A-7 shows an NI 446*x* input connection with the NI 446*x* terminal configuration in differential mode. Refer to the *Analog Input Channel Configurations* section of Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about terminal configuration.

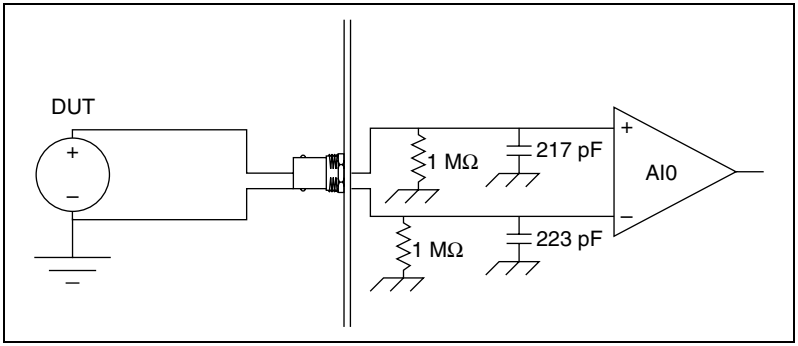


Figure A-7. NI 446*x* Input Connection in Differential Mode

Figure A-8 shows an NI 446*x* input connection with the NI 446*x* terminal configuration in pseudodifferential mode.

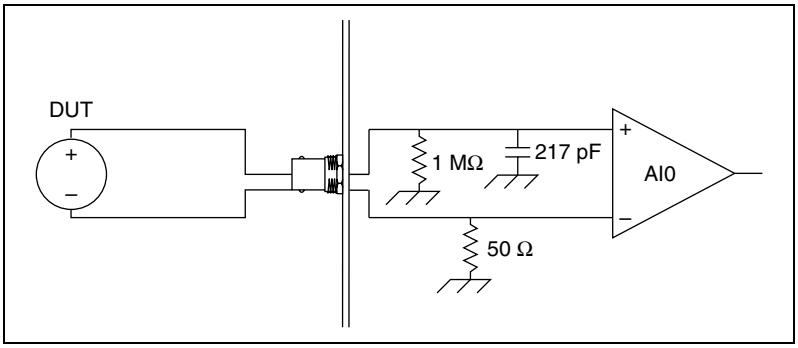


Figure A-8. NI 446*x* Terminal Configuration in Pseudodifferential Mode

NI 4461 Output Connections

Figure A-9 shows an NI 4461 output connection with the NI 4461 terminal configuration in differential mode. Refer to the *Analog Output Channel Configurations* section of Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about terminal configuration.

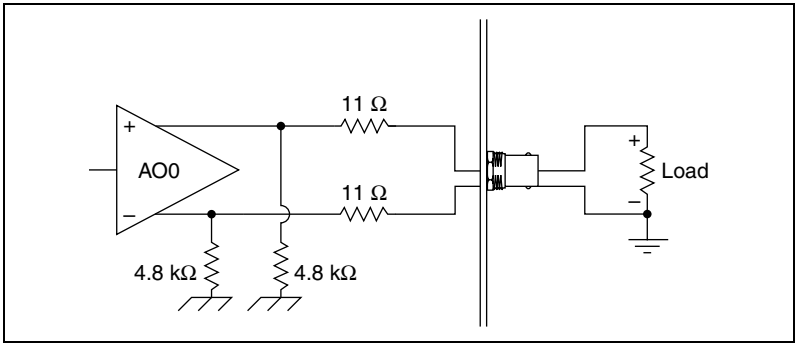


Figure A-9. NI 4461 Output Connection with Terminal Configuration in Differential Mode

Figure A-10 shows an NI 4461 output connection with the NI 4461 terminal configuration in pseudodifferential mode.

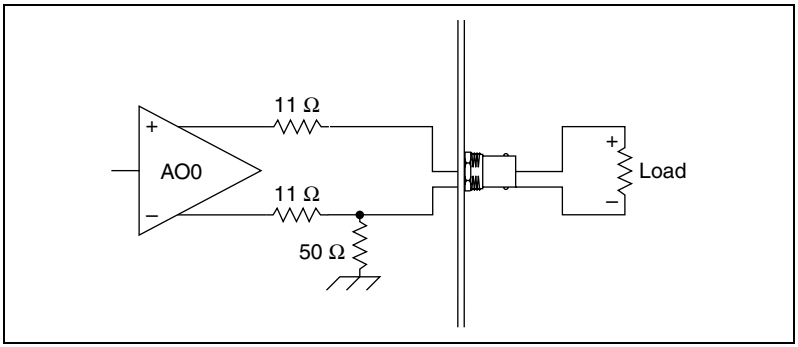


Figure A-10. NI 4461 Output Connection with Terminal Configuration in Pseudodifferential Mode

NI 446*x* Filter Response

Figure A-11 shows the digital filter input frequency response with low-frequency alias rejection enabled.

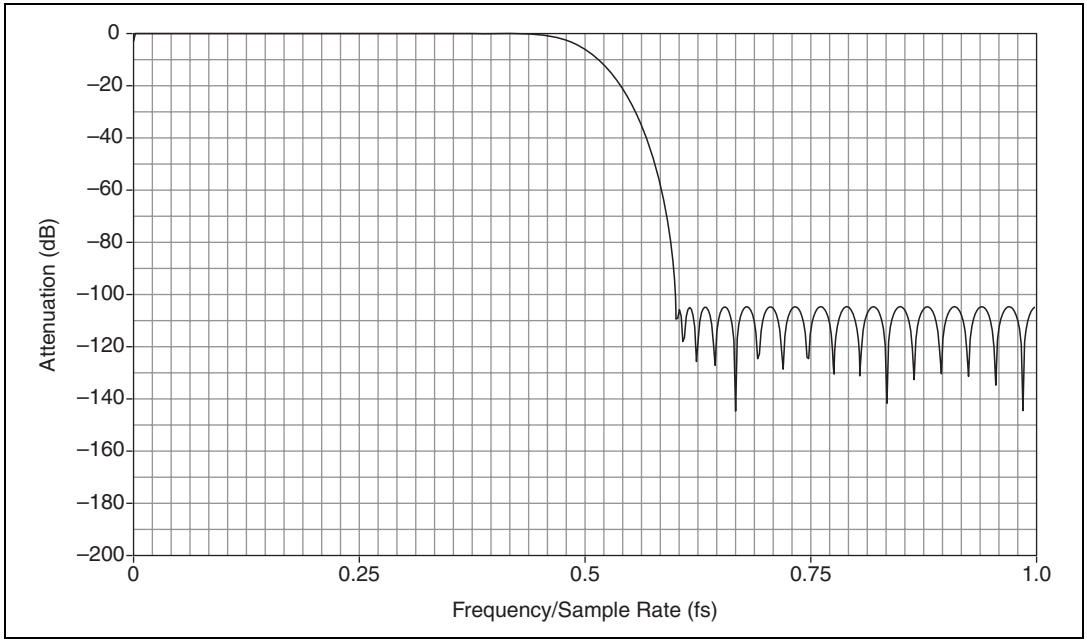


Figure A-11. NI 446*x* Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Enabled

Figure A-12 shows the digital filter input frequency response with low-frequency alias rejection disabled.

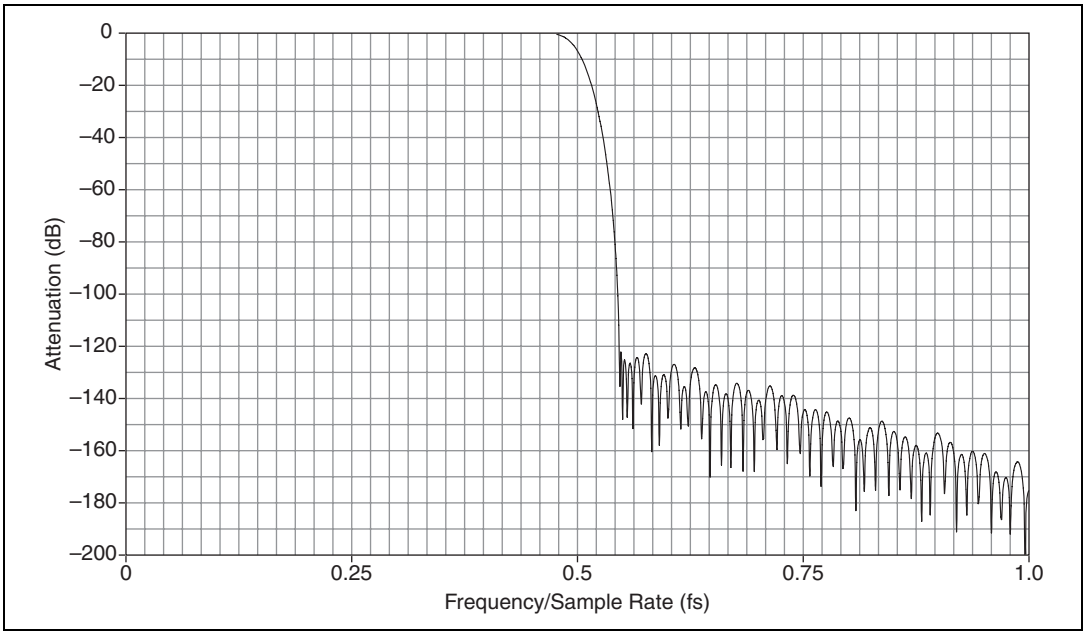


Figure A-12. NI 446*x* Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Disabled

Figure A-13 shows the response of the analog filter. Figure A-13 illustrates the alias rejection for a tone that passes the digital filter by falling into one of the narrow bands centered on one of three sets of sample rate multiples. One set of narrow bands centers on 32 f_s and succeeding multiples of 32. The other two sets center on 64 f_s and 128 f_s and succeeding multiples of 64 and 128, respectively. The first set of x-axis labels denotes the NI 446*x* sample rate in kS/s. The second set of x-axis labels shows the frequency of an input signal which could pass through the digital filter at the given sampling rate.

In the following example, the NI 446*x* is set to sample at 10 kS/s. A clean tone of 1 Vpk amplitude is sent to an input channel on the device. If the input frequency is less than approximately 4.9 kHz (0.49 f_s), it passes through the digital filter. At 4.91 kHz, the digital filter applies −3 dB attenuation. The digital filter provides at least −120 dB of attenuation for frequency components above the Nyquist frequency. However, the digital filter can potentially admit aliases in the much higher frequency range from 1.275 MHz to 1.285 MHz (128 f_s the example sample rate of 10 kS/s). If

noise in the input signal falls into this narrow window, the noise is not rejected by the digital filter. In this limited frequency range, you must consider the response of the analog filter. Figure A-13 illustrates that with a sampling rate of 10 kS/s, the analog filter attenuates an input signal frequency of 1.28 MHz by −10 dB.

The sawtooth line in Figure A-13 represents the filter response with low-frequency alias rejection enabled. The worst-case alias rejection is approximately −25 dB. This corresponds to the analog filter attenuation at 25.6 kS/s.

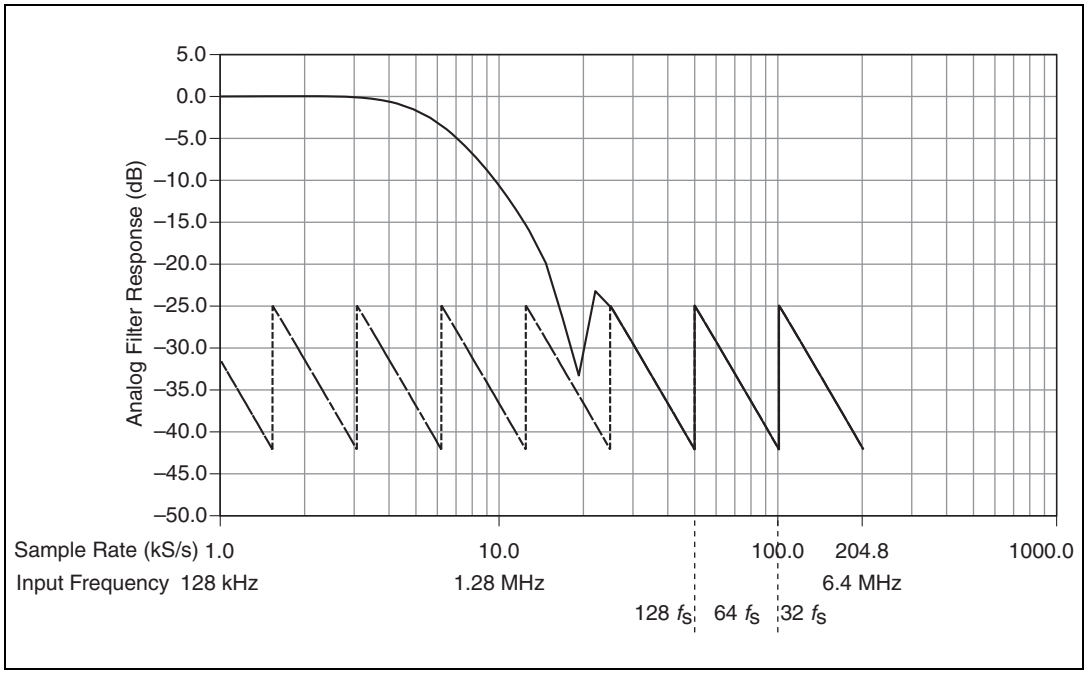


Figure A-13. NI 446*x* Analog Filter Response

This situation represents the set of worst-case alias rejections for each sample rate. You would only observe this worst-case scenario with a well-defined tone in a narrow frequency range. In real measurement situations, it is more likely that any energy passing the digital filter consists only of low-amplitude noise. If an unwanted component does appear in the digitized signal, increasing the sampling rate might provide an easy solution by both improving the rejection from the analog filter and by repositioning the digital filter so that it can eliminate the alias. Under most circumstances, use the first figure to calculate the NI 446*x* alias rejection.

NI PXI-446*x* Reference Clock Synchronization

NI PXI-446*x* devices employ onboard PLL circuitry. The PLL circuitry locks the onboard 100 MHz voltage-controlled crystal oscillator (VCXO) to the PXI 10 MHz reference clock signal, PXI_CLK10. The VCXO output provides the source for the DDS chip, which generates the sample clock timebase. In this way the NI PXI-446*x* devices lock the sample clock timebase to PXI_CLK10.

NI 446*x* Specifications

Refer to the *NI 446x Specifications* for more detailed information about the NI 446*x* devices.

NI 447*x* Devices

This section contains information about the NI 447*x* devices.

NI 447*x* Features

The NI 447*x* devices are high-performance, high-accuracy analog input devices for PXI and PCI. The NI 447*x* devices have the following features:

- The NI 4472 features eight input channels
- The NI 4472B features eight input channels with a lower cutoff frequency on AC-coupled channels
- The NI PCI-4474 features four input channels

NI 447*x* Analog Input Features

Figure A-14 shows the NI 447*x* analog input circuitry block diagram.

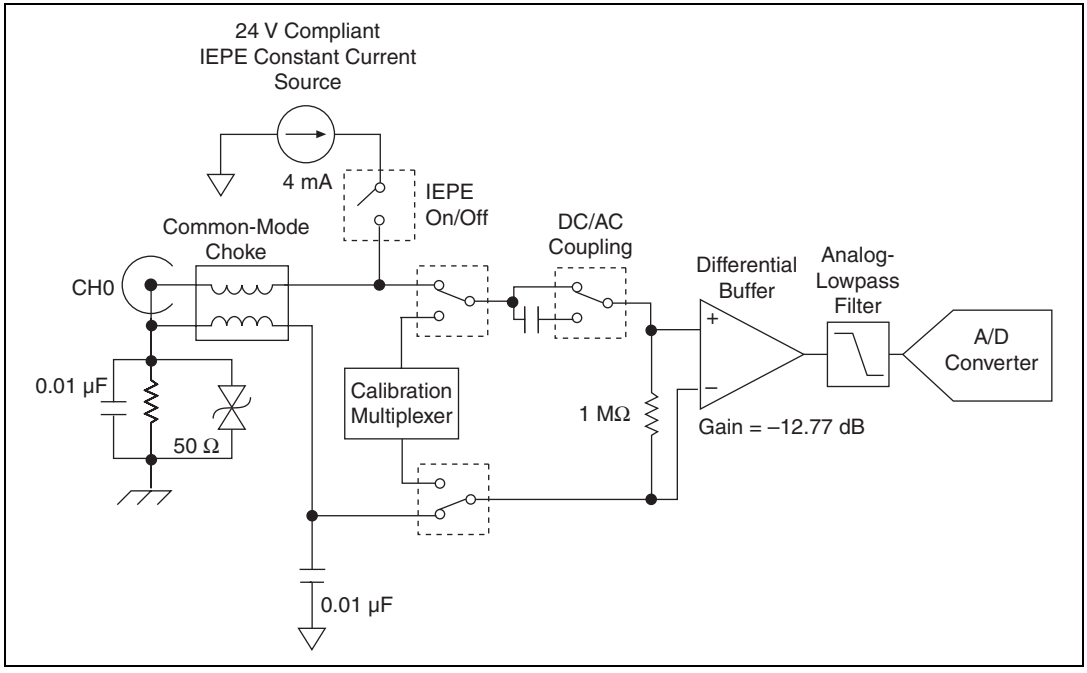


Figure A-14. NI 447*x* Analog Block Diagram

The NI 447*x* analog input channels feature the following:

- Simultaneous sampling at up to 102.4 kS/s
- Per channel AC or DC coupling
- Per channel IEPE current excitation
- Anti-alias filtering
- Postdigitization digital overload detection
- Multiple triggering modes, including external digital triggering

NI 447*x* Digital Function Block Diagram

Figure A-15 shows the NI 447*x* digital function block diagram.

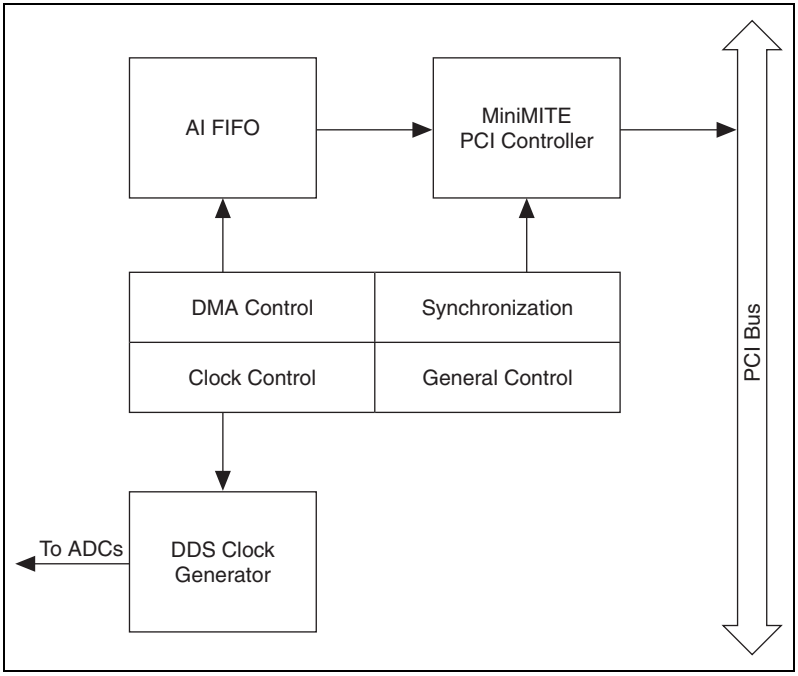


Figure A-15. NI 447*x* Digital Function Block Diagram

Connecting Signals to NI 447*x* Devices

This section contains information about connecting signals to NI 447*x* devices.

NI 447*x* Front Panels

Figure A-16 shows the NI PXI-4472, NI PXI-4472B, NI PCI-4472, NI PCI-4472B, and NI PCI-4474 front panels.

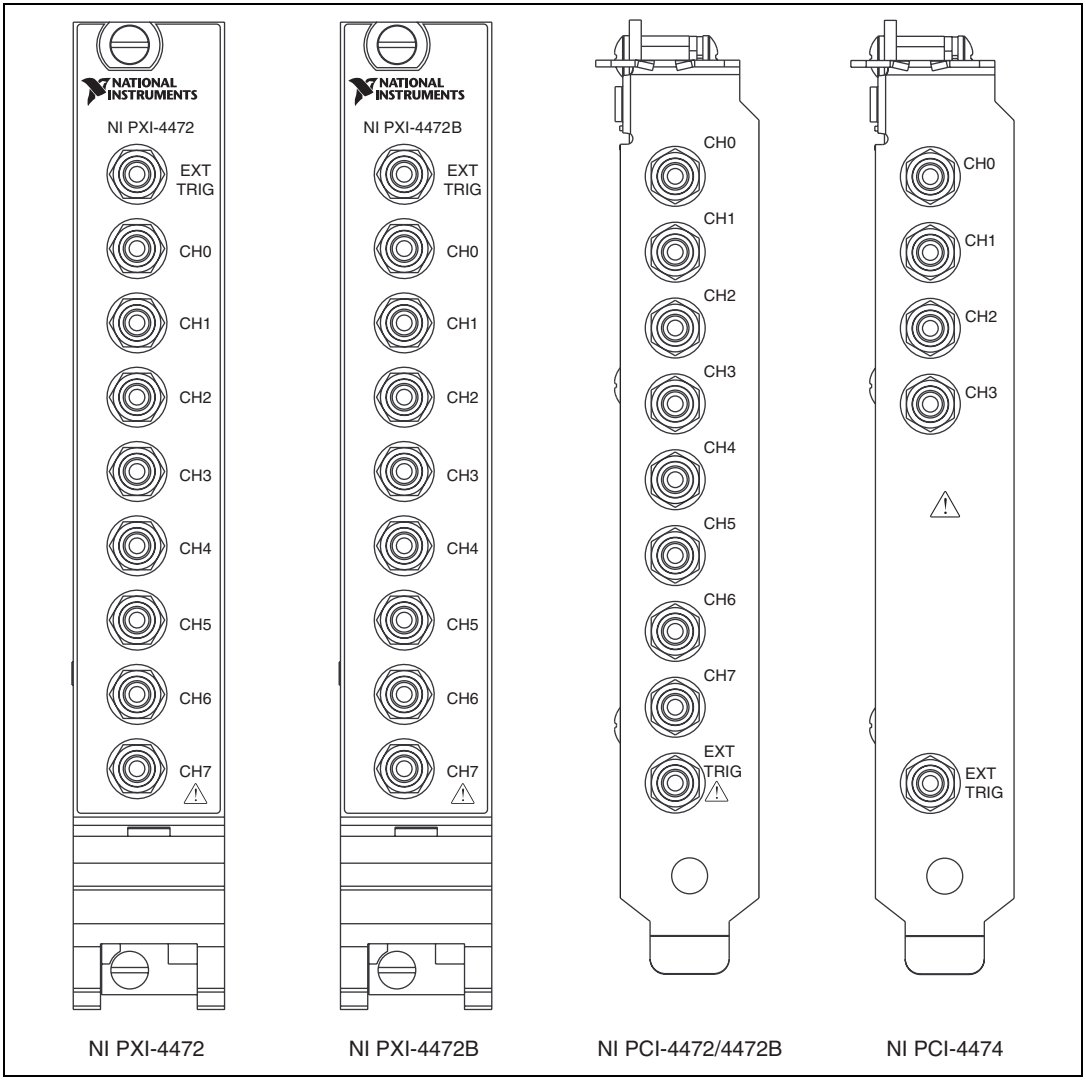


Figure A-16. NI 447*x* Front Panels

NI 447*x* Input Connections

The NI 447*x* channels have pseudodifferential inputs. Figure A-17 shows the *input configurations* for floating and grounded signal sources.

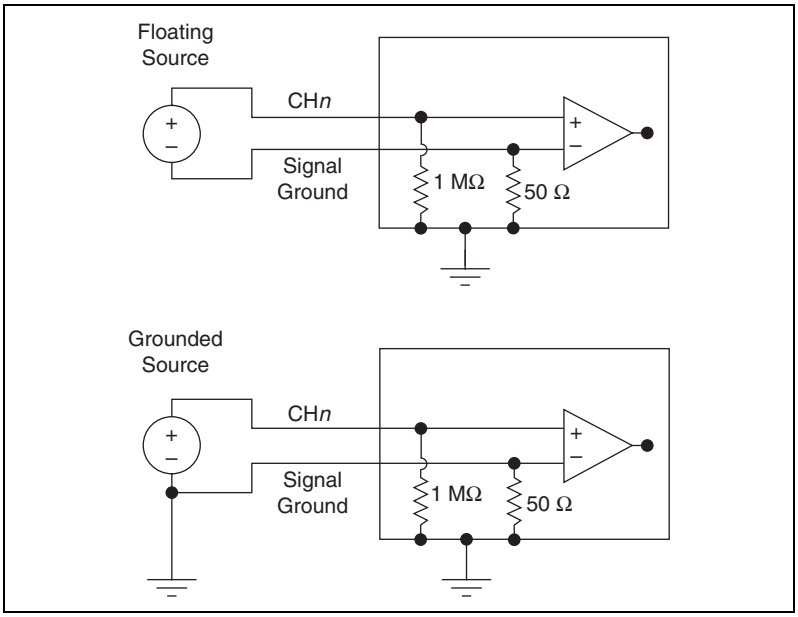


Figure A-17. NI 447*x* Input Connections

Caution Connecting a signal that varies more than ±2.5 V from the NI 447*x* ground reference to the ground (shield) of any input channel can result in inaccurate measurements or damage to the device. NI is *not* responsible for damage caused by such connections.

NI 447*x* Filter Response

Figure A-18 shows the digital filter input frequency response.

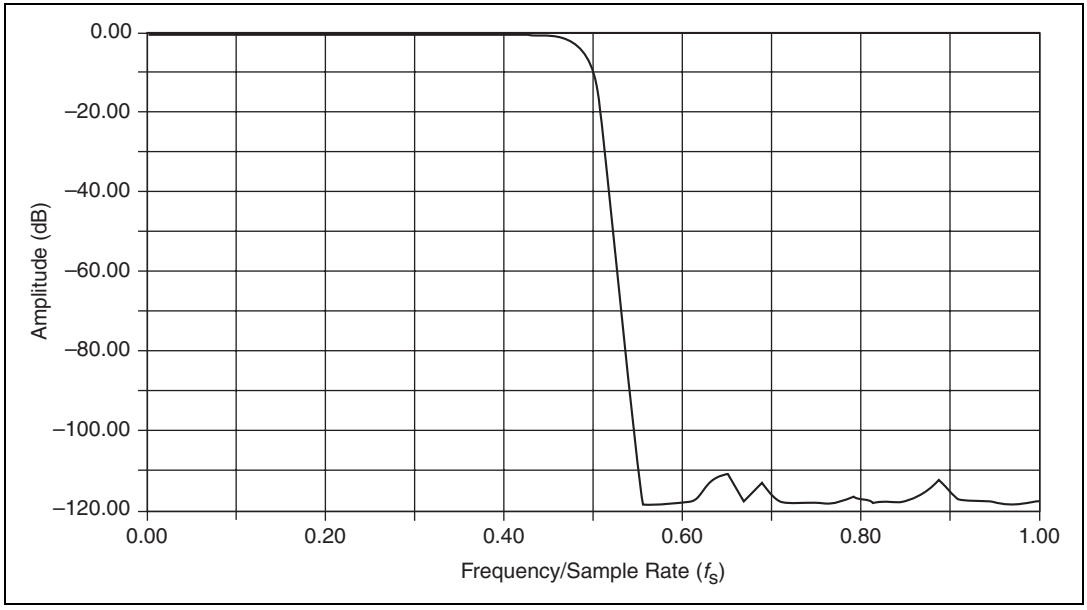


Figure A-18. NI 447*x* Digital Filter Input Frequency Response

Figure A-19 shows the digital filter frequency response near the cut-off point.

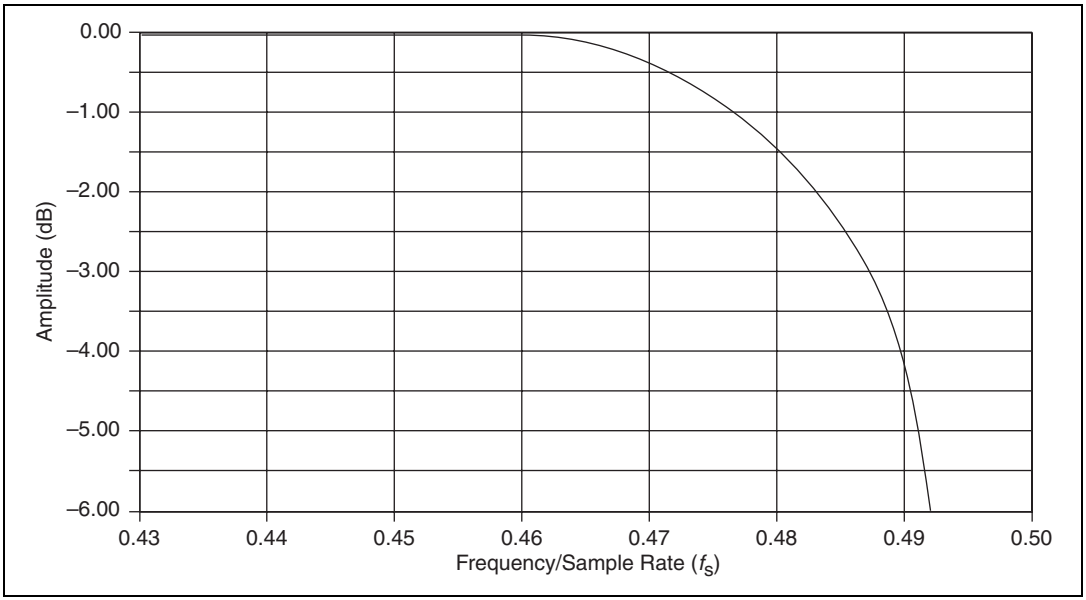


Figure A-19. NI 447*x* Digital Filter Frequency Response Near the Cut-off Point

Figure A-20 shows the response of the analog filter. Figure A-20 illustrates the alias rejection for a tone that passes the digital filter by falling into one of the narrow bands centered on 128 or 64 f_s. The first set of x-axis labels denotes the NI 447*x* sample rate in kS/s. The second set of x-axis labels shows the frequency of an input signal which could pass through the digital filter at the given sampling rate.

In the following example, the NI 447*x* is set to sample at 10 kS/s. A clean tone of 1 Vpk amplitude is sent to an input channel on the device. If the input frequency is less than approximately 4.6 kHz (0.46 f_s), it passes through the digital filter. At 4.86 kHz, the digital filter applies −3 dB attenuation. The digital filter provides at least −110 dB of attenuation for frequency components above the Nyquist frequency. However, the digital filter can potentially admit aliases in the much higher frequency range from 1.275 MHz to 1.285 MHz (128 f_s the example sample rate of 10 kS/s). If noise in the input signal falls into this narrow window, the noise is not rejected by the digital filter. In this limited frequency range, you must consider the response of the analog filter. Figure A-20 illustrates that with a sampling rate of 10 kS/s, the analog filter attenuates an input signal frequency of 1.28 MHz by −40 dB.

On NI 447*x* devices with low-frequency alias rejection enabled, the sawtooth line in Figure A-20 represents the filter response. The worst-case alias rejection is approximately –63 dB. This corresponds to the analog filter attenuation at 25.6 kS/s.

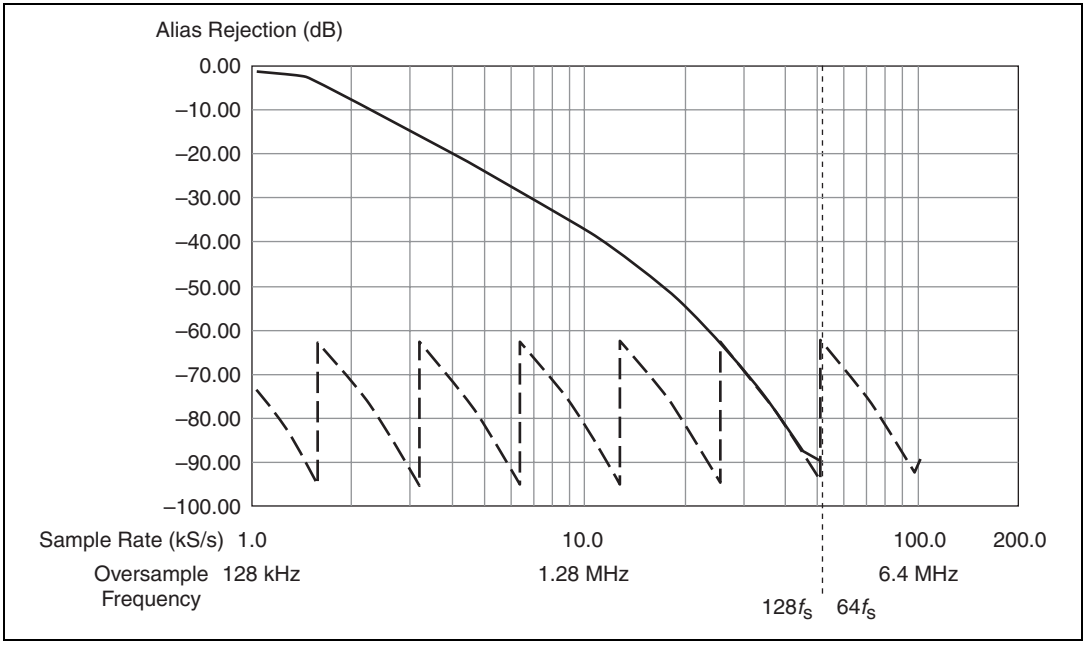


Figure A-20. NI 447*x* Analog Filter Response

This situation represents the set of worst-case alias rejections for each sample rate. You would only observe this worst-case scenario with a well-defined tone in a narrow frequency range. In real measurement situations, it is more likely that any energy passing the digital filter consists only of low-amplitude noise. If an unwanted component does appear in the digitized signal, increasing the sampling rate might provide an easy solution by both improving the rejection from the analog filter and by repositioning the digital filter so that it can eliminate the alias. Under most circumstances, use the first figure to calculate the NI 447*x* alias rejection.

NI 447*x* Specifications

Refer to the *NI 447x Specifications* for more detailed information about the NI 447*x* devices.

NI 449*x* Devices

This section contains information about the NI 449*x* devices.

NI 449*x* Features

The NI 449*x* devices are high-performance, high-accuracy analog input devices for PXI or PXIe. The NI 4498 and 4496 devices feature 16 AC-coupled inputs with IEPE and TEDS capability. The NI 4498 features four input ranges of ±0.316 V, ±1 V, ±3.16 V, and ±10 V. The NI 4496 has two input ranges of ±3.16 V and ±10 V. Refer to Chapter 2, *Dynamic Signal Acquisition Device Concepts*, for more information about analog input and other feature concepts.

NI 449*x* Analog Input Features

Figure A-21 shows the NI 449*x* analog input circuitry block diagram.

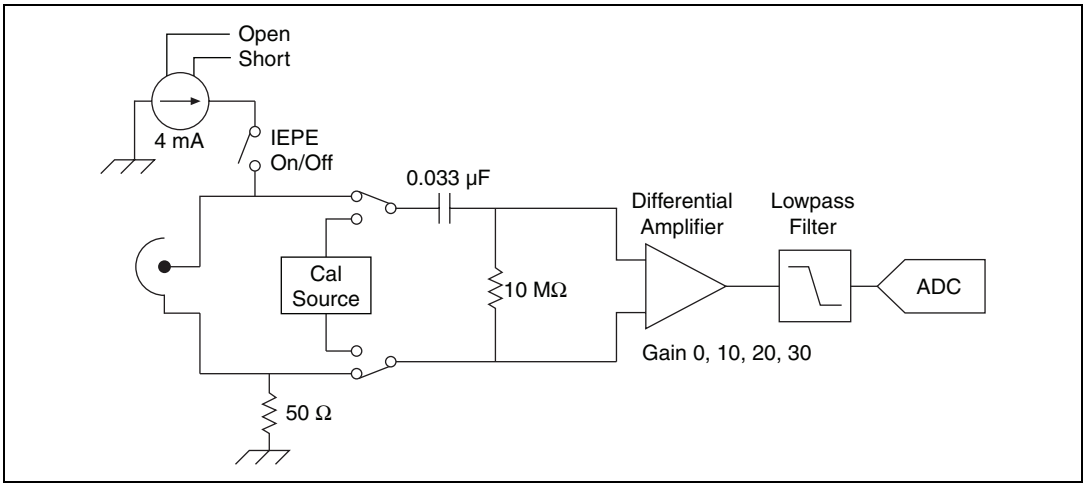


Figure A-21. NI 449*x* Analog Input Block Diagram

Note Certain NI 449*x* devices support different gain options. Refer to the *NI 449x Specifications* for more information about supported gain settings.

The NI 449*x* input channels feature the following:

- Simultaneous sampling rates up to 204.8 kS/s
- Per channel selection of gain
- Per channel IEPE current excitation

- Per channel IEPE sensor open and short detect
- Multiple triggering modes, including external digital triggering
- Per channel digital overload detection
- Hardware data packing
- TEDS

NI 449*x* Block Diagram

Figure A-22 shows the NI 449*x* block diagram.

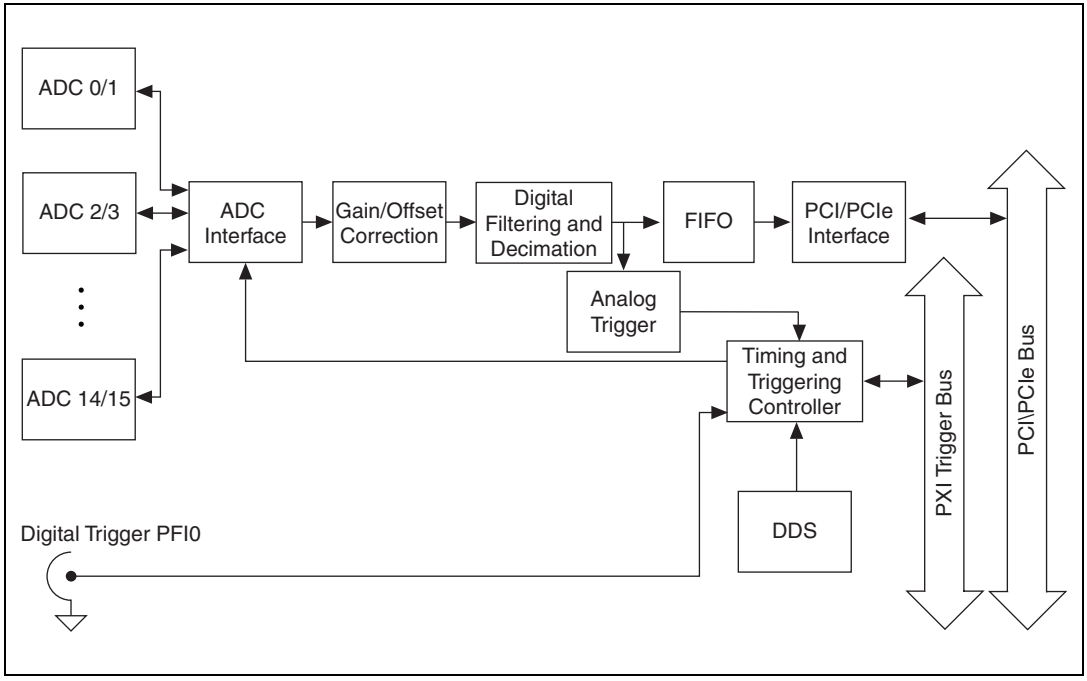


Figure A-22. NI 449*x* Block Diagram

Connecting Signals to NI 449*x* Devices

This section contains information about connecting signals to NI 449*x* devices.

NI 449*x* Front Panels

Figure A-23 shows the NI 4496 and NI 4498 front panels. The NI 449*x* devices have Infiniband 4x connectors. Refer to the *NI-DAQmx Help* for more information about the NI 449*x* connectors.

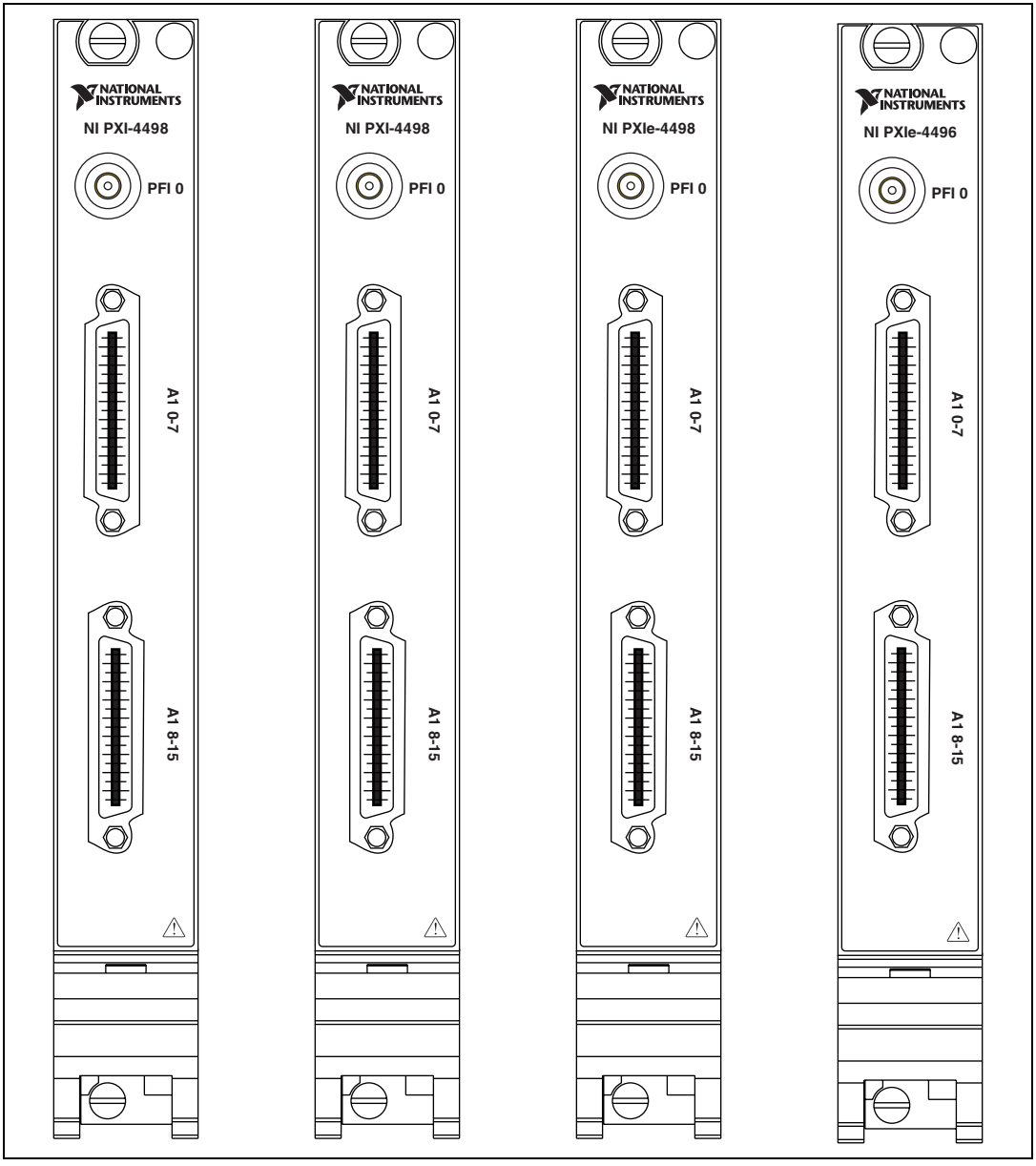


Figure A-23. NI 449*x* Front Panels

Caution Connecting a signal that varies more than ±5 V from the NI 449*x* ground reference to the ground (shield) of any input channel can result in damage to the device. NI is *not* responsible for damage caused by such connections.

BNC Connector Polarity

You can use an NI BNC-2144 or an Infiniband 4x to 8 BNC cable assembly to create BNC connectors from the NI 449*x*. Figure A-24 shows the BNC connector polarity for all NI 449*x* devices.

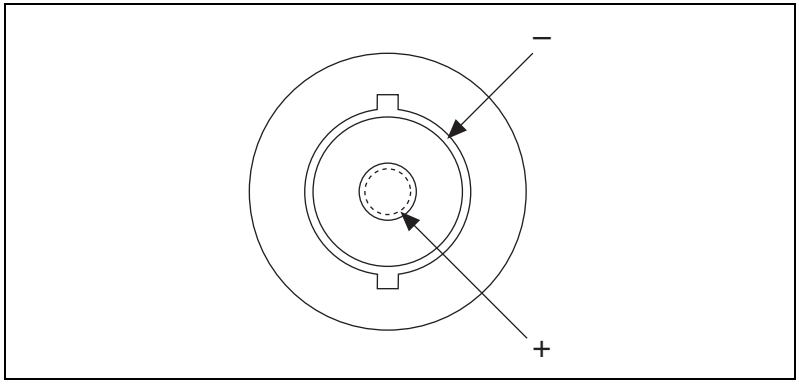


Figure A-24. BNC Connector Polarity for NI 449*x* Devices

NI 449*x* Filter Response

Figure A-25 shows the digital filter input frequency response with low-frequency alias rejection enabled.

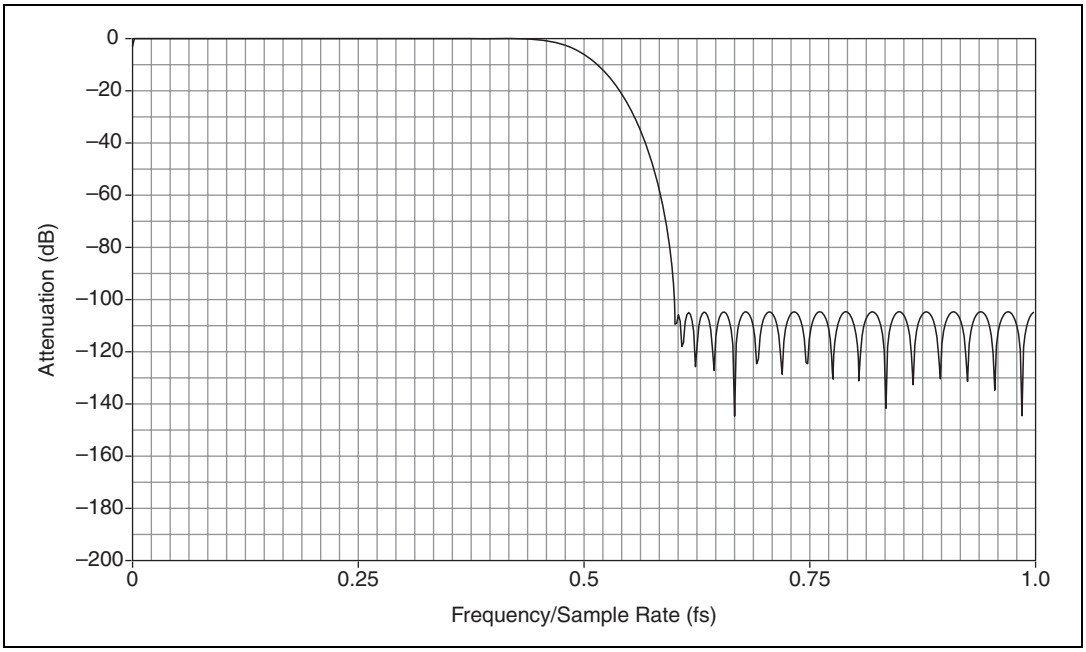


Figure A-25. NI 449*x* Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Enabled

Figure A-26 shows the digital filter input frequency response with low-frequency alias rejection disabled.

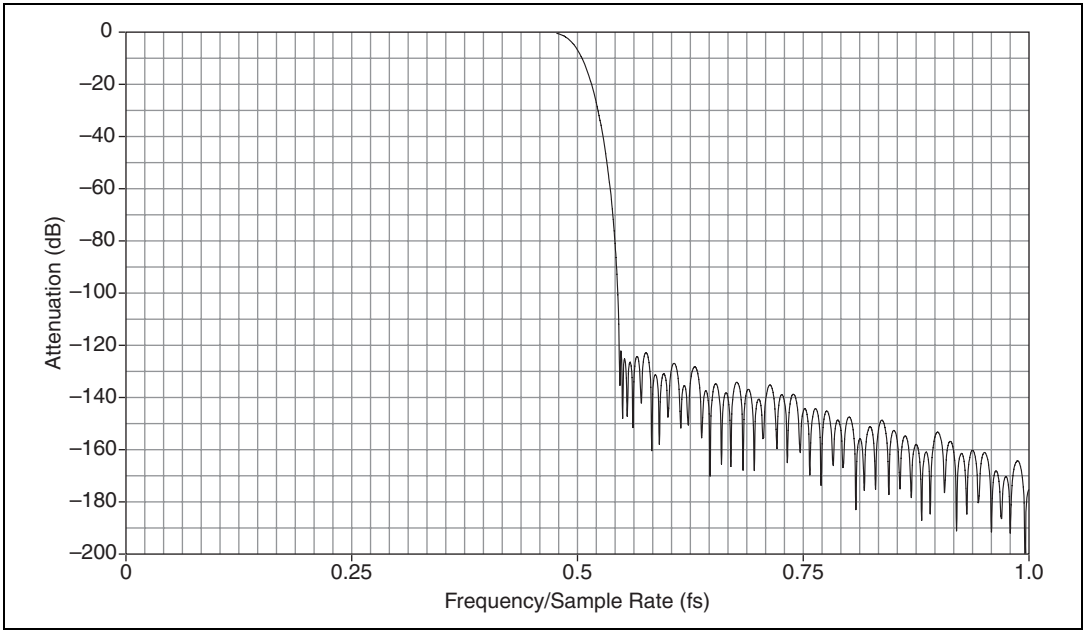


Figure A-26. NI 449*x* Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Disabled

NI 449*x* Reference Clock Synchronization

NI 449*x* devices employ onboard PLL circuitry. The PLL circuitry locks the onboard 100 MHz voltage-controlled crystal oscillator (VCXO) to the PXI/PXIe 10 MHz reference clock signal, PXI_CLK10. The VCXO output provides the source for the DDS chip, which generates the sample clock timebase. In this way the NI PXI-449*x* devices lock the sample clock timebase to PXI_CLK10.

NI 449*x* Specifications

Refer to the *NI 449x Specifications* for more detailed information about the NI 449*x* devices.

B

Technical Support and Professional Services

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- **Support**—Technical support at ni.com/support includes the following resources:
  - **Self-Help Technical Resources**—For answers and solutions, visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
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- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting `ni.com/certification`.
- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at `ni.com/calibration`.

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Glossary

Symbols

%	Percent.
+	Positive of, or plus.
–	Negative of, or minus.
±	Plus or minus.
<	Less than.
>	Greater than.
≤	Less than or equal to.
≥	Greater than or equal to.
/	Per.
º	Degree.
Ω	Ohm.

A

A	Amperes.
AC	Alternating current.
AC coupling	Allowing the transmission of AC signals while blocking DC signals.
ADC	A/D converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number.
ADC resolution	The size of the discrete steps in the ADCs input-to-output transfer function; therefore, the smallest voltage difference an ADC can discriminate with a single measurement.

ADE	Application development environment—an application designed to make it easier for you to develop software. Usually, ADEs have a graphical user interface and programming tools to help with development. Examples of ADEs are LabVIEW, LabWindows/CVI, Visual Basic, and Visual C++.
AI	Analog input.
alias	A false lower frequency component that appears in sampled data acquired at too low a sampling rate.
amplification	The process of increasing signal amplitude using electronic components. A signal with increased amplitude may allow improved measurement accuracy by using more ADC range and reducing analog signal noise prior to digitization.
amplifier	An electronic component that increases analog signal amplitude. *See also* amplification.
amplify	To increase signal amplitude using electronic components. *See also* amplification.
amplitude flatness	A measure of how close to constant the gain of a circuit remains over a range of frequencies.
AO	Analog output.
API	Application programming interface.
asynchronous	Hardware—a property of an event that occurs at an arbitrary time, without synchronization to a reference clock; Software—a property of a function that begins an operation and returns prior to the completion or termination of the operation.
attenuate	To decrease the amplitude of a signal.

B

bandwidth	The range of frequencies present in a signal, or the range of frequencies to which a measuring device can respond.
bipolar	A signal range that includes both positive and negative values (for example, –5 V to +5 V).

BNC	Bayonet-Neill-Concelman—a type of coaxial connector used in situations that require shielded cable for signal connections and/or controlled-impedance applications.
buffer	Software temporary storage for acquired or generated data.
burst DMA transfer	A DMA transfer in which one sample of data transfers to memory every bus clock period.
bus	The group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the ISA and PCI bus.
Butterworth filter	A filter with a smooth response over all frequencies and a monotonic decrease from the specified cut-off frequency.

C

C	Celsius.
CCIF	*See* IMD.
channel	Pin or wire lead used to acquire or generate an analog or digital signal. Analog channels can be single-ended or differential.
clipping	Clipping occurs when an input signal exceeds the input range of the amplifier and results in an overload condition.
clock	Digital signal that controls timing.
CMRR	common-mode rejection ratio—a measure of the ability of an instrument to reject interference from a common-mode signal, usually expressed in decibels (dB).
code width	The smallest detectable change in an input voltage of a device. *See also* ADC resolution.
common-mode range	The input range over which a circuit can handle a common-mode signal.
common-mode signal	The mathematical average voltage, relative to the computer's ground, of the signals from a differential input.
counter/timer	A circuit that counts external pulses or clock pulses (timing).

coupling	The manner in which a signal is connected from one location to another.
crosstalk	An unwanted signal on one channel due to an input on a different channel.
current sourcing	The ability of a device to supply current for analog or digital output signals.

D

DAC	D/A converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current.
DAQ	Data acquisition. 1. Acquiring and measuring analog or digital electrical signals from sensors, transducers, and test probes or fixtures. 2. Generating analog or digital electrical signals.
dB	Decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 (V1/V2), for signals in volts.
dBFS	Absolute signal level compared to full scale.
DC	Direct current.
DC coupling	Allowing the transmission of both AC and DC signals.
DDS clock	Direct digital synthesis clock—a type of clock source with an output frequency controlled by a digital tuning word.
delta-sigma modulating ADC	A high-accuracy circuit that samples at a higher rate than needed and pushes the quantization noise above the frequency range of interest. This out-of-band noise is typically removed by digital filters.
device	A plug-in board that can contain multiple channels and conversion devices. SCXI modules are distinct from devices.
differential input	An AI consisting of two terminals not connected to a fixed reference, such as the earth or a building ground.
differential measurement system	A two terminal measurement configuration in which you do not need to connect either input to a fixed reference, such as the earth or a building ground.
digital trigger	A TTL level signal having two discrete levels—a high and a low level.

digital tuning word	A 32-bit word that selects the DDS clock frequency.
DIO	Digital input/output.
DMA	Direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	Differential nonlinearity—a measure in LSBs of the worst-case deviation of code widths from their ideal value of 1 LSB.
DoC	Declaration of Conformity.
DOC	Canadian Department of Communications.
down counter	Performing frequency division on an internal signal.
drivers	Software that controls a specific hardware device such as a DAQ device or a GPIB interface device.
DSA	Dynamic signal acquisition.
DUT	Device under test.
dynamic range	The ratio of the largest signal level a circuit can handle to the smallest signal level it can handle (usually taken to be the noise level), normally expressed in decibels.

E

ESD	Electrostatic discharge.
event	The condition or state of an analog or digital signal.
external trigger	A voltage pulse from an external source that triggers an event, such as A/D conversion.

F

falling edge	A signal component with a negative slope that passes a threshold.
f_{DAC}	The frequency after the data passes through the DAC.

f_{es}	The effective sampling frequency.
FIFO	First-in first-out memory buffer—the first data stored is the first data sent to the acceptor. FIFOs are often used on devices to temporarily store incoming or outgoing data until that data can be retrieved or output. For example, an AI FIFO stores the results of A/D conversions until the data can be retrieved into system memory, a process that requires the servicing of interrupts and often the programming of the DMA controller. This process can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of AO, a FIFO permits faster update rates, because the waveform data can be stored on the FIFO ahead of time. Faster update rates again reduce the effect of latencies associated with getting the data from system memory to the device.
filter delay	The time required for data to propagate through a converter.
filtering	A type of signal conditioning that allows you to attenuate unwanted portions of the signal you are trying to measure resulting in a signal with less noise and unwanted components.
f_{in}	Input signal frequency.
FIR	Finite impulse response—a non recursive digital filter with linear phase.
floating signal sources	Signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common examples of floating signal sources are batteries, transformers, or thermocouples.
f_s	Sampling frequency or rate.

G

gain	The factor by which a signal is amplified, sometimes expressed in decibels.
grounded source	A signal source connected in some way to a ground reference, either chassis or earth ground.

H

h	Hours.
hardware	The physical components of a computer system, such as the circuit boards, plug-in devices, chassis, enclosures, peripherals, and cables.
hardware triggering	A form of triggering where you set the start time of an acquisition and gather data at a known position in time relative to a trigger signal.
harmonics	Frequency components that are integral multiples of a fundamental frequency.
high-impedance	In logic circuits designed to have three possible states—0, 1, and tristate (high-impedance)—the high-impedance state effectively removes the output from its circuit and can be used to simplify bus communication by wire-ANDing tristate inputs.
hysteresis triggering	Triggering with a trigger condition based on both current analog signal levels and the past signal history. For example, a hysteresis trigger can be set to fire when a signal rises above 0 V, but only if it fell below 0 V at some point in the past.
Hz	Hertz—cycles per second. Specifically refers to the repetition frequency of a waveform.

I

IEPE	Integrated electronic piezoelectric—a type of transducer that operates using a constant current source as the conditioning medium and returns a signal in the form of voltage modulation on the same line as the current source.
images	Unwanted frequency components beyond the Nyquist bandwidth produced during D/A conversion during analog output operations.
IMD	Intermodulation distortion—the ratio, in dB, of the total rms signal level of harmonic sum and difference distortion products, to the overall rms signal level. The test signal is two sine waves added together according to the CCIF standard of one 14 kHz sine wave and one 15 kHz sine wave added in a 1:1 amplitude ratio.
in.	Inches.

INL	Integral nonlinearity—a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry.
input impedance	The measured resistance and capacitance between the input terminals of a circuit and ground.
interrupt	A computer signal indicating that the CPU should suspend its current task to service a designated activity.

K

k	Kilo—the standard metric prefix for 1,000, or 103, used with units of measure such as volts, hertz, and meters.
kS	1,000 samples.

L

LabVIEW	A program development application based on the programming language G and used commonly for test and measurement purposes.
linearity	The adherence of device response to the equation R = K1S+K2, where R = response, S = stimulus, and K1, K2 = constants.
LSB	Least significant bit—the bit of a digital word that has the lowest numerical value.

M

memory buffer	*See* buffer.
MSB	Most significant bit—the bit of a digital word that has the highest numerical value.

N

noise	An undesirable electrical signal—noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
nonreferenced signal sources	Signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called floating signal sources. Some common example of nonreferenced signal sources are batteries, transformers, or thermocouples.
Nyquist bandwidth	The bandwidth from 0 Hz to the Nyquist frequency.
Nyquist frequency	A frequency that is one-half the sampling rate. *See also* Nyquist Sampling Theorem.
Nyquist Sampling Theorem	The theorem that states that if a continuous bandwidth-limited analog signal contains no frequency components equal to or higher than half the frequency at which it is sampled, then the original signal can be recovered without distortion.

O

overrange	A measurement level beyond the stated or selected range of a device.
oversampling	Sampling at a rate higher than the Nyquist frequency.

P

passband	The range of frequencies which a device can properly propagate or measure.
PCI	Peripheral component interconnect—a high-performance PC expansion bus architecture originally developed by Intel to replace ISA and EISA. It offers a theoretical maximum transfer rate of 132 Mbytes/s.
PFI	Programmable function input—a signal line often used for timing, triggering, and synchronization.

posttriggering	The technique used on a device to acquire a programmed number of samples after trigger conditions are met.
pretriggering	The technique used on a device to keep a continuous buffer filled with data, so that when the trigger conditions are met, the sample includes the data leading up to the trigger condition.
pseudodifferential	Pseudodifferential channels are all referred to a common ground, but this ground is not directly connected to the computer ground. Often this connection is made by a relatively low value resistor to give some isolation between the two grounds.

Q

quantization error	The inherent uncertainty in digitizing an analog value as a result of the finite resolution of the conversion process.
quantizer	A device that maps a variable from a continuous distribution to a discrete distribution.

R

RC	Resistor-capacitor—for example, an RC network is a circuit consisting of a resistor and capacitor.
relative accuracy	A measure in LSB of the linearity of an ADC. It includes all nonlinearity and quantization errors. It does not include offset and gain errors of the circuitry feeding the ADC.
resolution	The smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or as a percentage of full scale. For example, a system can have 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
rise time	Generally, the time for a signal to transition from 10% to 90% of the maximum signal amplitude.
rising edge	A signal component with a positive slope that passes a threshold.

rms	Root mean square—the square root of the average value of the square of the instantaneous signal amplitude; a measure of signal amplitude.
RTSI bus	Real-time system integration bus—the NI timing bus that connects devices directly for precise synchronization of functions.

S

s	Seconds.
S	Samples.
sample rate	Sample rate is the rate at which data is sampled.
self-calibrating	A property of a device that has an extremely stable onboard reference and calibrates its own A/D and D/A circuits without manual adjustments by the user.
sensor	A device that responds to a physical stimulus (heat, light, sound, pressure, motion, flow, and so on), and produces a corresponding electrical signal.
SFDR	Spurious free dynamic range—The dynamic range from full-scale deflection to the highest spurious signal in the frequency domain.
Shannon Sampling Theorem	*See* Nyquist Sampling Theorem.
signal conditioning	The manipulation of signals to prepare them for digitizing.
single-ended	A circuit that responds to the voltage on one input terminal and ground.
SMB	Sub-miniature type B—a type of coaxial connector.
SNR	Signal-to-noise ratio—the ratio of the overall rms signal level to the rms noise level, expressed in decibels.
software trigger	A programmed event that triggers an event such as data acquisition.
software triggering	A method of triggering in which you trigger an operation using software.

synchronous	Hardware—a property of an event that is synchronized to a reference clock;software—a property of a function that begins an operation and returns only when the operation is complete.
system noise	A measure of the amount of noise seen by an analog circuit or an ADC when the AI channels are grounded.

T

TEDS	Transducer electronic data sheet—a transducer with a built-in self-identification EEPROM as standardized by IEEE 1451.4.
THD	Total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal. Usually expressed in decibels or as a percentage of the signal.
THD+N	THD plus noise—the ratio in decibels of the rms signal of harmonic distortion plus noise introduced to the overall rms signal.
transducer	*See* sensor.
transfer rate	The rate, measured in bytes/s, at which data is moved from source to destination after software initialization and set up operations; the maximum rate at which the hardware can operate.
tp	The interval between pulses in a pulse train.
treset	The length of the reset period.
trigger	Any event that causes or starts some form of data capture.
TTL	Transistor-transistor logic.
TTL-compatible	Operating in a nominal range of 0 to 5 VDC, with a signal below 0.8 V at logic low, and a signal above 2.4 V at logic high.

U

undersampling	Sampling at a rate lower than twice the Nyquist frequency—can cause aliasing.

V

V	Volts.
VCXO	Voltage-controlled crystal oscillator.
VDC	Volts direct current.
VI	Virtual instrument—a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument; a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program.
Vin	Volts in.
Vpk	Voltage peak.
Vref	Reference voltage.

W

waveform	Multiple voltage readings taken at a specific sampling rate.

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