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UBX

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The UBX daughterboard is a full-duplex wideband transceiver that covers frequencies from 10 MHz to 6 GHz. Coherent and phase-aligned operation across multiple UBX daughterboards on USRP X Series motherboards enables users to explore MIMO and direction finding applications. The UBX daughterboard is supported by the USRP Hardware Driver? (UHD) software API for seamless integration into existing applications.

The UBX is capable of phase coherent operation, and therefore is suitable for MIMO and Phased Array applications, on the X Series. Additionally this capability is only available on the X Series devices.

- Frequency Range: 10 MHz - 6 GHz
- Versions: 40MHz / 160MHz
- RF shielding
- Full duplex operation with independent TX and RX frequencies
- Synthesizer synchronization for applications requiring coherent or phase-aligned operation, supported on USRP X Series motherboards only





- 2 quadrature frontends (1 transmit, 1 receive)
  - Defaults to direct conversion
  - Can be used in low IF mode through lo_offset with uhd::tune_request_t
- Independent receive and transmit LO's and synthesizers
  - Allows for full-duplex operation on different transmit and receive frequencies
  - Can be set to use Integer-N tuning for better spur performance with uhd::tune_request_t

Transmit: **TX/RX**

Receive: **TX/RX** or **RX2**

- **Frontend 0:** Complex baseband signal for selected antenna
- **Note:** The user may set the receive antenna to be TX/RX or RX2. However, when using a UBX board in full-duplex mode, the receive antenna will always be set to RX2, regardless of the settings.

- Transmit Gains: **PGA0**, Range: 0-31.5dB
- Receive Gains: **PGA0**, Range: 0-31.5dB

- UBX: 40 MHz, RX & TX
- UBX-160: 160 MHz, RX & TX

- **lo_locked:** boolean for LO lock state

- **LOCK**: Synthesizer Lock Detect
- **TX/RX TXD**: Transmitting on TX/RX antenna port
- **TX/RX RXD**: Receiving on TX/RX antenna port
- **RX2 RXD**: Receiving on RX2 antenna port

- 10MHz - 6GHz

- 10 MHz - 500 MHz: 3 - 4 dB
- 500 MHz - 1.5 GHz: 2 - 3 dB
- 1.5GHz - 6GHz: 4 - 10 dB

- 10 MHz - 6 GHz: 8 - 9 dBm

- 10 MHz - 6 GHz: < -30dBc

- 10 MHz - 3 GHz: 20 dBm
- 3 - 6 GHz: 8 - 20 dBm

- 10 - 500 MHz: 41 dBm
- 0.5 - 3 GHz: 36 dBm
- 3 - 6 GHz: 26 dBm - 36 dBm

- 10 MHz - 6 GHz: < -30 dBc

Note: The UBX 160 transmitter path has 160 MHz of bandwidth throughout the full frequency range of the device; the receiver path has 84 MHz of bandwidth for center frequencies from 10 MHz to 500 MHz.

- All RF Ports are matched to 50 Ohm with -10dB or better return loss generally. Detailed test is pending.

- The maximum input power for the UBX is -15 dBm.

- UBX without UHD Corrections

- Ettus Research recommends to always use the latest stable version of UHD

- Current Hardware Revision: 2
- Minimum version of UHD required for UBX rev-1: 3.8.2
- Minimum version of UHD required for UBX rev-2: 3.9.5

- Current Hardware Revision: 2
- Minimum version of UHD required for UBX rev-1: 3.8.2
- Minimum version of UHD required for UBX rev-2: 3.9.5

- 0-40 °C

- 10% to 90% non-condensing

- N or X Series

- X Series only

The UBX daughterboard is capable of phase-synchronous operation, and is recommended for phase-coherent applications. The SBX and TwinRX daughterboards are also recommended for phase-coherent applications.

If you are operating the UBX at frequencies below 1 GHz and need phase synchronization, then it is necessary to select a 20 MHz daughterboard clock rate, instead of using the default 50 MHz rate. Note that this is only required for phase synchronization below 1 GHz. The UBX can still operate below 1 GHz without setting this lower daughterboard clock rate, but it will operate without any phase synchronization capability.

If you're using a UHD program, then you can specify the lower daughterboard clock rate on the command line of the program, with `--args="dboard_clock_rate=20e6"`.

If you're using the UHD API from a C++ program, then you can include `"dboard_clock_rate=20e6"` in the device arguments parameter when first invoking `multi_usrp::make()`.

If you're using GNU Radio, then you can add `"dboard_clock_rate=20e6"` to the `"Device Arguments"` field of the properties for the UHD Sink and UHD Source blocks.

UBX Schematics

Part Number	Description	Schematic ID (Page)
MAX2871	Fractional/Integer-N Synthesizer/VCO	U3 (3); U9 (5); U19 (7); U23 (9)
ADL5375-05	Quadrature Modulator	U22 (8)
LFCN-2250+	Low Pass Filter	F1 (3); F24 (7); F34, F35 (10)
LTC5510	Active Mixer	U15 (6)
LFCN-490+	Low Pass Filter	F12 (5); F15 (6); F26 (7); F31 (9); F33, F36 (10)
HMC624LP4E	ATTENUATOR	U16 (6)
NBB-400	Amplifier	U13 (6); U30 (11)
PHA-1+	Amplifier	U31 (11)
ADA4927-2	Differential ADC Driver	U6 (4)
ADL5380	Quadrature Demodulator	U8 (4)
MGA-62563	Low Noise Amplifier	U36 (11)
LFCN-1700+	Low Pass Filter	F41 (11)
VMMK-3603	Low Noise Amplifier	U34 (11)
LFCN-2600+	Low Pass Filter	F14, F17 (6)
855916	SAW Filter	F16 (6)
LTC5510	Active Mixer	U15 (6); U28 (10)
LFCN-2600+	Low Pass Filter	F14, F17 (10)
TCM1-63AX+	RF Transformer	T1 (3); T2, T3 (4); T7 (8)
ADA4927-2	Differential ADC Driver	U6 (4)
AD8591	Operational Amplifiers	U7 (4)
ADL5380	Quadrature Demodulator	U8 (4)
ZXTC2062E6	TRANSISTORS	Q1 (6)
HMC624ALP4E	ATTENUATOR	U16 (6); U29 (10)
LFCN-800+	Low Pass Filter	F2 (3); F25 (7)
ADP7104-3.3	CMOS LDO	U4, U5 (3); U10, U11 (5); U20, U21 (7); U24, U25 (9); U48 (13)
ADL5375-05	Quadrature Modulator	U22 (8)
LTC5510	Active Mixer	U28 (10)
24LC024	EEPROM	U38, U39 (12)
ADP7104-5.0	CMOS LDO	U41, U42, U43, U44, U45, U46, U47 (13)
ZXTC2062E6	TRANSISTORS	Q2, Q3, Q4, Q5 (13)

- PDF Format
- STP Format

- The UBX daughterboard features female SMA connectors for both the TX/RX and RX2 connectors.

As of December 1st, 2010 all Ettus Research products are RoHS compliant unless otherwise noted. More information can be found at http://ettus.com/legal/rohs-information

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- Media:volatility UBX CBX WBX SBX r1 1.pdf

- A larger 24W (6V, 4A) power supply is required when using a UBX-40 daughterboard and integrated GPS Disciplined Oscillator accessory together in a USRP2, USRP N200, or USRP N210 device.
- The UBX-160 transmitter path has 160 MHz of bandwidth throughout the full frequency range of the device; the receiver path has 84 MHz of bandwidth for center frequencies from 10 MHz to 500 MHz.

FPGA Resources

UHD Stable Binaries

UHD Source Code on Github

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