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Lab-NB
User Manual

Low-Cost Multifunction I/O Board for Macintosh NuBus

September 1995 Edition

Part Number 320174B-01

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About This Manual

This manual describes the mechanical and electrical aspects of the Lab-NB and contains information concerning its installation and operation. The Lab-NB is a low-cost multifunction analog, digital, and timing I/O board for Macintosh NuBus computers. It contains a 12-bit successive-approximation A/D converter (ADC) with eight analog inputs, two 12-bit D/A converters (DACs) with voltage outputs, 24 lines of transistor-transistor logic (TTL) compatible digital I/O, and three 16-bit counter/timer channels for timing I/O.

Organization of This Manual

The *Lab-NB User Manual* is organized as follows.

- Chapter 1, *Introduction*, describes the Lab-NB, lists what you need to get started, software programming choices, optional equipment, and explains how to unpack the Lab-NB.
- Chapter 2, *Configuration and Installation*, describes how to configure and install the Lab-NB into your Macintosh computer, and also includes signal connections to the Lab-NB and cable wiring.
- Chapter 3, *Theory of Operation*, contains a functional overview of the Lab-NB and explains the operation of each functional unit making up the Lab-NB.
- Chapter 4, *Register-Level Programming*, describes in detail the address and function of each of the Lab-NB control and status registers. This chapter also includes important information about register-level programming the Lab-NB.
- Chapter 5, *Calibration*, discusses the calibration procedures for the Lab-NB analog input and analog output circuitry.
- Appendix A, *Specifications*, lists the specifications of the Lab-NB.
- Appendix B, *I/O Connector*, contains the pinout and signal names for the I/O connector on the Lab-NB.
- Appendix C, *AMD 8253 Data Sheet*, contains the manufacturer data sheet for the AMD 8253 System Timing Controller integrated circuit (Advanced Micro Devices, Inc.). This circuit is used on the Lab-NB.
- Appendix D, *OKI 82C55A Data Sheet*, contains the manufacturer data sheet for the OKI 82C55A (OKI Semiconductor) CMOS programmable peripheral interface. This interface is used on the Lab-NB.
- Appendix E, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products and manuals.

- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms.
- The *Index* alphabetically lists topics covered in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual.

bold	Bold text denotes menus, menu items, or dialog box buttons or options.
bold italic	Bold italic text denotes a note, caution, or warning.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
Macintosh	Macintosh refers to all Macintosh II, Macintosh Quadra, and Macintosh Centris computers, except the Centris 610, unless otherwise noted.
NI-DAQ	NI-DAQ is used throughout this manual to refer to the NI-DAQ software for Macintosh unless otherwise noted.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ boards.
< >	Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name (for example, ACH <0..7> stands for ACH0 through ACH7).

Abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms are listed in the *Glossary*.

National Instruments Documentation

The *Lab-NB User Manual* is one piece of the documentation set for your data acquisition (DAQ) system. You could have any of several types of manuals, depending on the hardware and software in your system. Use the different types of manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.

- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.

- Software manuals—Examples of software manuals you may have are the LabVIEW and LabWindows®/CVI manual sets and the NI-DAQ manuals (a 4.6.1 or earlier version of NI-DAQ supports LabWindows for DOS). After you set up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) manuals or the NI-DAQ manuals to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software manuals before you configure your hardware.

- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides or accessory board user manuals. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.

- SCXI chassis manuals—If you are using SCXI, read these manuals for maintenance information on the chassis and installation instructions.

Related Documentation

The following documents contain information that you may find helpful as you read this manual.

- Macintosh II or Quadra *Owner's Manual*, *Getting Started* manual, or *Setting Up* manual

- *Inside Macintosh–Volume 5*

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix E, *Customer Communication*, at the end of this manual.

Chapter 1
Introduction

This chapter describes the Lab-NB, lists what you need to get started, software programming choices, optional equipment, and explains how to unpack the Lab-NB.

About the Lab-NB

Thank you for buying the National Instruments Lab-NB. The Lab-NB is a low-cost multi-function analog, digital, and timing I/O board for Macintosh NuBus computers. It contains a 12-bit successive-approximation ADC with eight analog inputs, two 12-bit DACs with voltage outputs, 24 lines of TTL-compatible digital I/O, and six 16-bit counter/timer channels for timing I/O.

The low cost of a Lab-NB-based system makes it ideal for laboratory work in industrial and academic environments. The multichannel analog input is useful in signal analysis and data logging. The 12-bit ADC is useful in high-resolution applications such as chromatography, temperature measurement, and DC voltage measurement. The analog output channels can be used to generate experiment stimuli and are also useful for machine and process control and analog function generation. The 24 TTL-compatible digital I/O lines can be used for switching external devices such as transistors and solid-state relays, for reading the status of external digital logic, and for generating interrupts. The counter/timers can be used to synchronize events, generate pulses, and measure frequency and time. The Lab-NB, used in conjunction with the Macintosh, is a versatile, cost-effective platform for laboratory test, measurement, and control.

Note: ***The Lab-NB cannot sink sufficient current to drive the SSR-OAC-5 and SSR-OAC-5A output modules. However, it can drive the SSR-ODC-5 output module and all SSR input modules available from National Instruments.***

If you need to drive a SSR-OAC-5 or SSR-OAC-5A, you can use a non-inverting digital buffer chip between the Lab-NB and the SSR backplane.

Detailed Lab-NB specifications are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your Lab-NB board, you will need the following:

- ❑ Lab-NB board
- ❑ *Lab-NB User Manual*
- ❑ One of the following software packages and documentation:
  NI-DAQ software for Macintosh
  LabVIEW for Macintosh
- ❑ Your computer

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use LabVIEW, LabWindows/CVI, or NI-DAQ. A 4.6.1 or earlier version of NI-DAQ supports LabWindows for DOS.

LabVIEW and LabWindows/CVI Application Software

LabVIEW and LabWindows/CVI are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows/CVI enhances traditional programming languages. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Libraries are functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition libraries are functionally equivalent to the NI-DAQ software.

Using LabVIEW or LabWindows/CVI software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Figure 1-1 illustrates the relationship between NI-DAQ and LabVIEW and LabWindows/CVI.

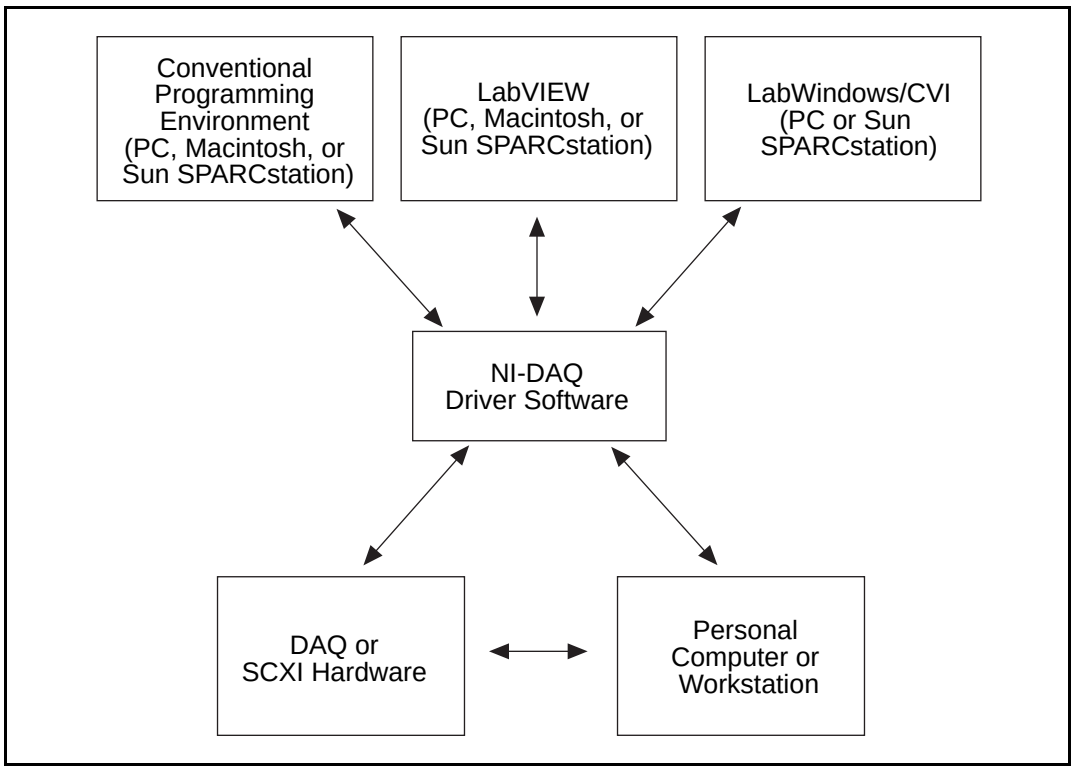


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient, and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using NI-DAQ, LabVIEW, or LabWindows/CVI to program your National Instruments DAQ hardware. Using the NI-DAQ, LabVIEW, or LabWindows/CVI software is easier than, and as flexible as, register-level programming, and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with your Lab-NB board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50-pin screw terminals
- Real Time System Integration (RTSI) bus cables
- Signal conditioning eXtensions for Instrumentation (SCXI) modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays.

For more specific information about these products, refer to your National Instruments catalog or call the office nearest you.

Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change board interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

National Instruments currently offers a cable termination accessory, the CB-50, for use with the Lab-NB board. This kit includes a terminated, 50-conductor, flat ribbon cable and a connector block. Signal input and output wires can be attached to screw terminals on the connector block and thereby connected to the Lab-NB I/O connector.

The CB-50 is useful for initially prototyping an application or in situations where Lab-NB interconnections are frequently changed. When you develop a final field wiring scheme, however, you may wish to develop your own cable.

The Lab-NB I/O connector is a 50-pin male ribbon cable header. The manufacturer part numbers used by National Instruments for this header are as follows:

- Electronic Products Division/3M (part number 3596-5002)
- T&B/Ansley Corporation (part number 609-500)

The mating connector for the Lab-NB is a 50-position, polarized, ribbon socket connector with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside-down connection to the Lab-NB. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

The following are the standard ribbon cables (50-conductor, 28 AWG, stranded) that can be used with these connectors:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

Unpacking

Your Lab-NB board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components of the board. To avoid such damage in handling the board, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.
- *Never* touch the exposed pins of connectors.

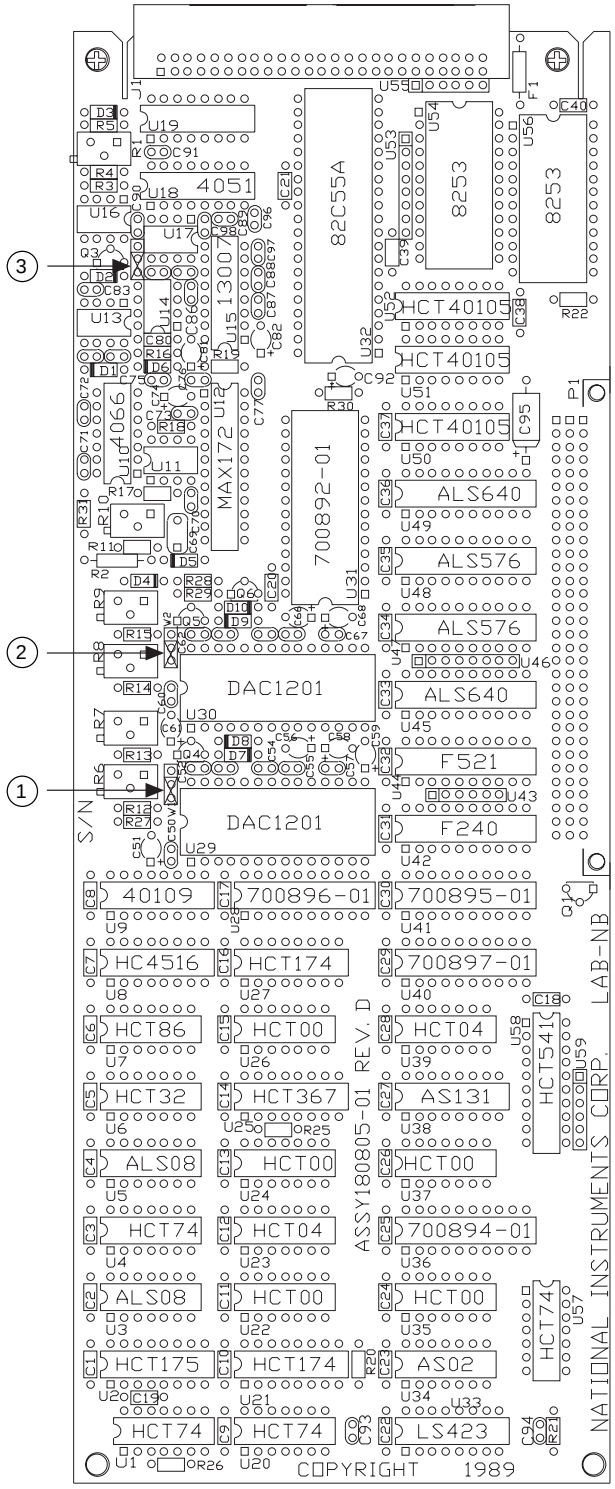
Chapter 2
Configuration and Installation

This chapter describes how to configure and install the Lab-NB into your Macintosh computer, and also includes signal connections to the Lab-NB and cable wiring.

Board Configuration

The Lab-NB contains three jumpers for changing the analog input and output configuration of the board. The jumpers are shown in the parts locator diagram in Figure 2-1. Jumpers W1 and W2 configure the two analog outputs. Jumper W3 (not labeled on the board) is used to select the analog input range. Because of space constraints on the board, the jumper post labels are missing. To distinguish between the A, B, and C posts of the jumpers, hold the board so that the component side is facing you, the NuBus connector is down, and the 50-pin I/O connector is on your right. The posts are then in the order A-B-C from left to right on all three of the horizontal jumpers, as shown in Figure 2-1.

Note: ***This same orientation of the board is also assumed in the figures illustrating the jumper connections*** *(Figures 2-2 and 2-3)****.***



1	W1
2	W2
3	W3

Figure 2-1. Parts Locator Diagram

Factory Default Jumper Settings

The Lab-NB is shipped from the factory with the following configuration:

- Jumpers W1 and W2–bipolar analog output
- Jumper W3–bipolar analog input

Table 2-1 lists all the available jumper configurations for the Lab-NB with the factory defaults noted.

Table 2-1. Lab-NB Jumper Settings

	Configuration	Jumper Setting
Output CH0 Polarity	Bipolar: ±5 V (factory setting) Unipolar: 0 to 10 V	**W1:** A-B **W1:** B-C
Output CH1 Polarity	Bipolar: ±5 V (factory setting) Unipolar: 0 to 10 V	**W2:** A-B **W2:** B-C
Input Range	Bipolar: ±5 V (factory setting) Unipolar: 0 to 10 V	**W3:** A-B **W3:** B-C

Analog Output Configuration

Two ranges are available for the analog outputs: bipolar (±5 V) and unipolar (0 to 10 V). Jumper W1 controls output channel 0, and W2 controls output channel 1.

Bipolar Output Selection

You can select the bipolar (±5 V) output configuration for either analog output channel by setting the following jumpers:

Analog Output Channel 0	W1	A-B
Analog Output Channel 1	W2	A-B

This configuration is shown in Figure 2-2.

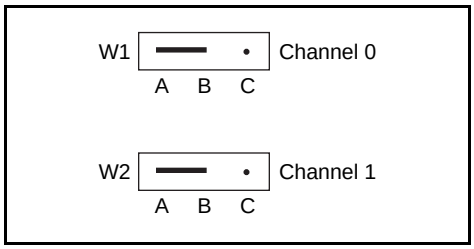


Figure 2-2. Bipolar Output Jumper Configuration

Unipolar Output Selection

You can select the unipolar (0 to 10 V) output configuration for either analog output channel by setting the following jumpers:

Analog Output Channel 0	W1	B-C
Analog Output Channel 1	W2	B-C

This configuration is shown in Figure 2-3.

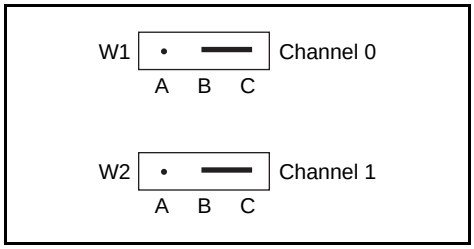


Figure 2-3. Unipolar Output Jumper Configuration

Analog Input Configuration

Two ranges are available for the analog inputs: bipolar (±5 V) and unipolar (0 to 10 V). Jumper W3 controls the input range for all eight analog input channels.

Bipolar Input Selection

You can select the bipolar (±5 V) input configuration by setting the following jumper:

Analog Input	W3	A-B

This configuration is shown in Figure 2-4.

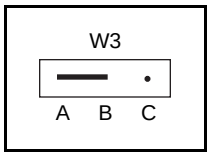


Figure 2-4. Bipolar Input Jumper Configuration

Unipolar Input Selection

You can select the unipolar (0 to 10 V) input configuration by setting the following jumper:

Analog Input W3 B-C

This configuration is shown in Figure 2-5.

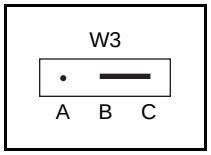


Figure 2-5. Unipolar Input Jumper Configuration

Note: ***If you are using a software package such as NI-DAQ or LabVIEW, you may need to reconfigure your software to reflect any changes in jumper or switch settings.***

Installation

Find the section in your Macintosh documentation that explains how to install an expansion board in your computer. You can use this procedure as a universal board installation guide.

First, read the entire procedure. Then, install your Lab-NB board in the Macintosh by following the outlined procedure.

Signal Connections

I/O Connector Pin Description

Figure 2-6 shows the pin assignments for the Lab-NB I/O connector. This connector is located on the back panel of the Lab-NB board and is accessible at the rear of the Macintosh computer after the board has been properly installed.

Warning: ***Connections that exceed any of the maximum ratings of input or output signals on the Lab-NB may result in damage to the Lab-NB board and to the Macintosh computer. This includes connecting any power signals to ground and vice versa. National Instruments is NOT liable for any damages resulting from any such signal connections.***

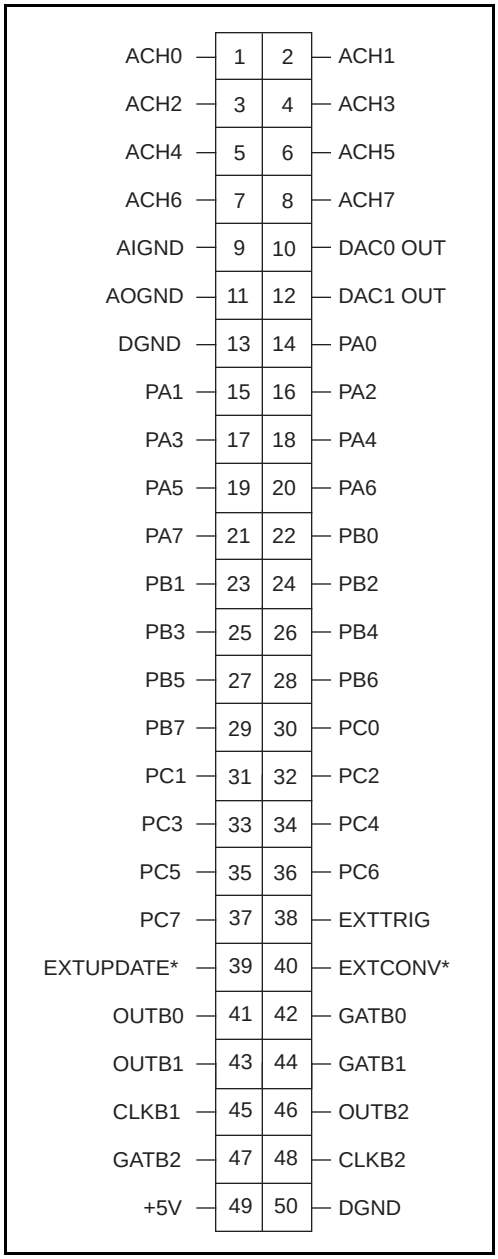


Figure 2-6. Lab-NB I/O Connector Pin Assignments

Signal Connection Descriptions

Pin	Signal Name	Description
1-8	ACH<0..7>	Analog input channels 0 through 7 (single-ended).
9	AIGND	Analog input ground.
10	DAC0 OUT	Voltage output signal for analog output channel 0.
11	AOGND	Analog output ground.
12	DAC1 OUT	Voltage output signal for analog output channel 1.
13	DGND	Digital ground.
14–21	PA<0..7>	Bidirectional data lines for port A. PA7 is the MSB, PA0 the LSB.
22–29	PB<0..7>	Bidirectional data lines for port B. PB7 is the MSB, PB0 the LSB.
30–37	PC<0..7>	Bidirectional data lines for port C. PC7 is the MSB, PC0 the LSB.
38	EXTTRIG	External control signal to start a timed conversion sequence.
39	EXTUPDATE*	External control signal to update DAC outputs.
40	EXTCONV*	External control signal to trigger A/D conversions.
41	OUTB0	Counter B0 output.
42	GATB0	Counter B0 gate.
43	OUTB1	Counter B1 output.
44	GATB1	Counter B1 gate.
45	CLKB1	Counter B1 clock.
46	OUTB2	Counter B2 output.
47	GATB2	Counter B2 gate.
48	CLKB2	Counter B2 clock.
49	+5 V	+5 V out, 1 A maximum.
50	DGND	Digital ground.
Note: ***Pin 49 is connected to the NuBus +5 V supply via a 1 A fuse. A replacement fuse is available from Allied Electronics, part number 845-2007, and Littelfuse, part number 251001.***		
* Indicates that the signal is active low.		

The connector pins can be grouped into analog input signal pins, analog output signal pins, digital I/O signal pins, and timing I/O signal pins. Signal connection guidelines for each of these groups are included later in this chapter.

Analog Input Signal Connections

Pins 1 through 8 are analog input signal pins for the 12-bit ADC. Pin 9, AIGND, is an analog common signal. This pin can be used for a general analog power ground tie to the Lab-NB. Pins 1 through 8 are tied to the eight single-ended analog input channels of the input multiplexer through 4.7-kΩ series resistances. Pin 40 is EXTCONV* and can be used to trigger conversions. A conversion occurs when this signal makes a high-to-low transition. It can only be used to

cause conversions to occur; it cannot be used as a monitor to detect conversions caused by the onboard sample-interval timer.

The following input ranges and maximum ratings apply to inputs ACH<0..7>:

Input impedance	0.1 GΩ in parallel with 45 pF
Input signal range	Bipolar input: ±(5 / gain) V Unipolar input: 0 to (10 / gain) V
Maximum input voltage rating	±45 V powered on or off

Exceeding the input signal range for gain settings greater than 1 will not damage the input circuitry as long as the maximum input voltage rating of ±45 V is not exceeded. For example, with a gain of 10, the input signal range is ±0.5 V for bipolar input and 0 to 1 V for unipolar input, but the Lab-NB is guaranteed to withstand inputs up to the maximum input voltage rating.

Warning: ***Exceeding the input signal range will result in distorted input signals. Exceeding the maximum input voltage rating may result in damage to the Lab-NB board and to the Macintosh computer. National Instruments is NOT liable for any damages resulting from any such signal connections.***

Connections for Signal Sources

Figure 2-7 shows how to connect a signal source to a Lab-NB board. When you connect grounded signal sources, observe the polarity carefully to avoid shorting the signal source output.

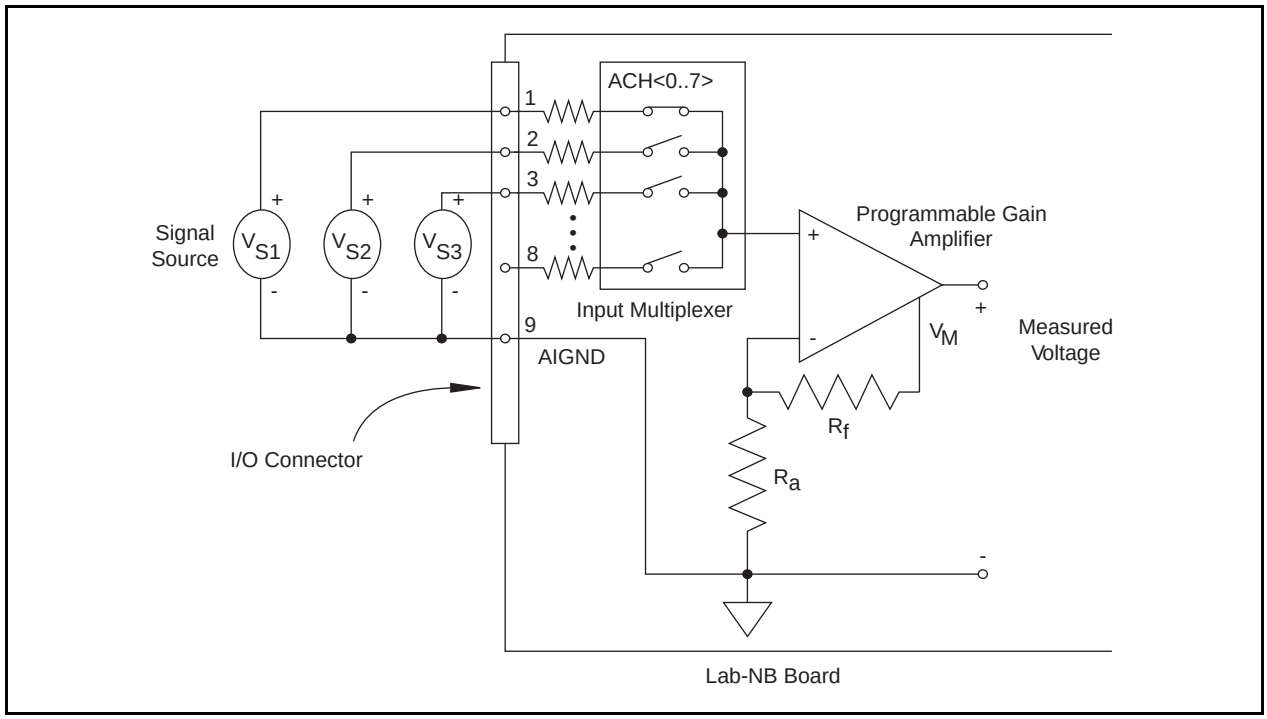


Figure 2-7. Analog Input Signal Connections

Analog Output Signal Connections

Pins 10 through 12 of the I/O connector are analog output signal pins.

Pins 10 and 12 are the DAC0 OUT and DAC1 OUT signal pins. DAC0 OUT is the voltage output signal for Analog Output Channel 0. DAC1 OUT is the voltage output signal for Analog Output Channel 1.

Pin 11, AOGND, is the ground reference point for both analog output channels as well as analog input.

The following output ranges are available:

Output signal range	Bipolar input: ±5 V* Unipolar input: 0 to 10 V*

* Maximum load current = ±1 mA for 12-bit linearity

Figure 2-8 shows how to make analog output connections.

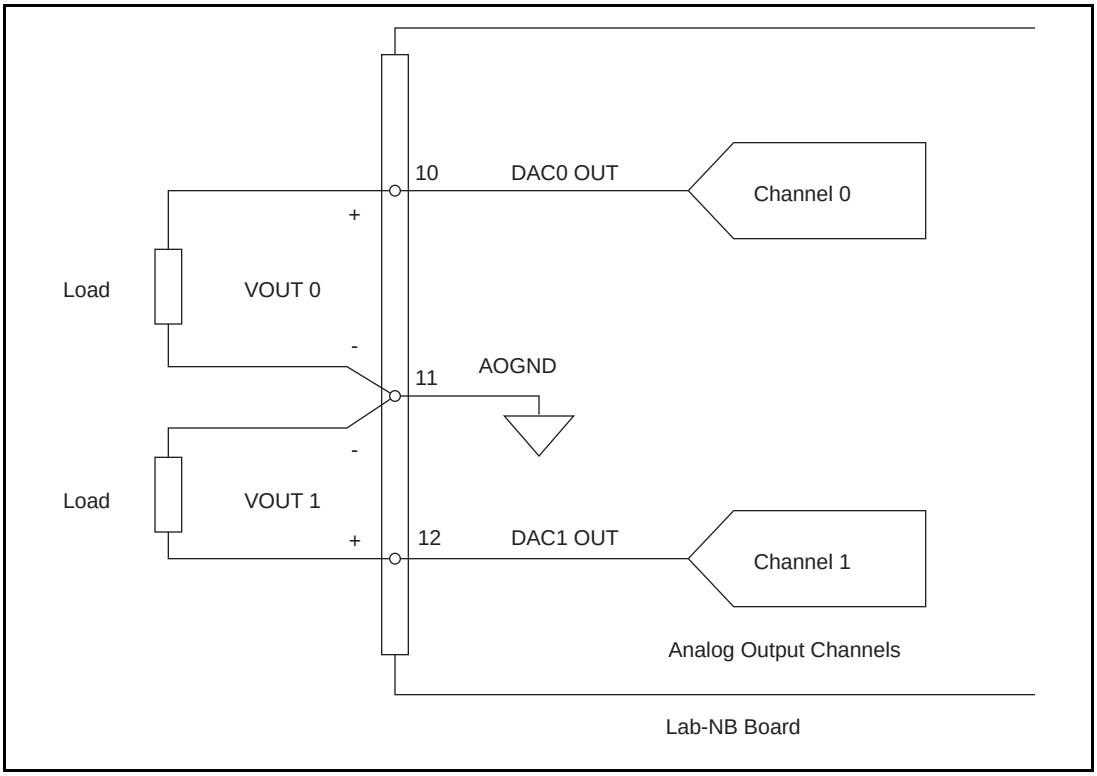


Figure 2-8. Analog Output Signal Connections

Digital I/O Signal Connections

Pins 13 through 37 of the I/O connector are digital I/O signal pins. Digital I/O on the Lab-NB is designed around the 82C55A integrated circuit. The 82C55A is a general-purpose PPI containing 24 programmable I/O pins. These pins represent the three 8-bit ports (PA, PB, and PC) of the 82C55A.

Pins 14 through 21 are connected to the digital lines PA<0..7> for digital I/O port A. Pins 22 through 29 are connected to the digital lines PB<0..7> for digital I/O port B. Pins 30 through 37 are connected to the digital lines PC<0..7> for digital I/O port C. Pin 13, DGND, is the digital ground pin for all three digital I/O ports.

The following specifications and ratings apply to the digital I/O lines.

Absolute maximum voltage input rating	+5.5 V with respect to DGND -0.5 V with respect to DGND

Digital input specifications (referenced to DGND):

V_{IH} input logic high voltage	2.2 V min
V_{IL} input logic low voltage	0.8 V max
I_{IH} input current load, logic high input voltage	1.0 µA max
I_{IL} input current load, logic low input voltage	-1.0 µA max

Digital output specifications (referenced to DGND):

V_{OH} output logic high voltage	3.7 V min
V_{OL} output logic low voltage	0.4 V max
I_{OH} output source current, logic high	-2.5 mA max
I_{OL} output sink current, logic low	2.5 mA max

Figure 2-9 illustrates signal connections for three typical digital I/O applications.

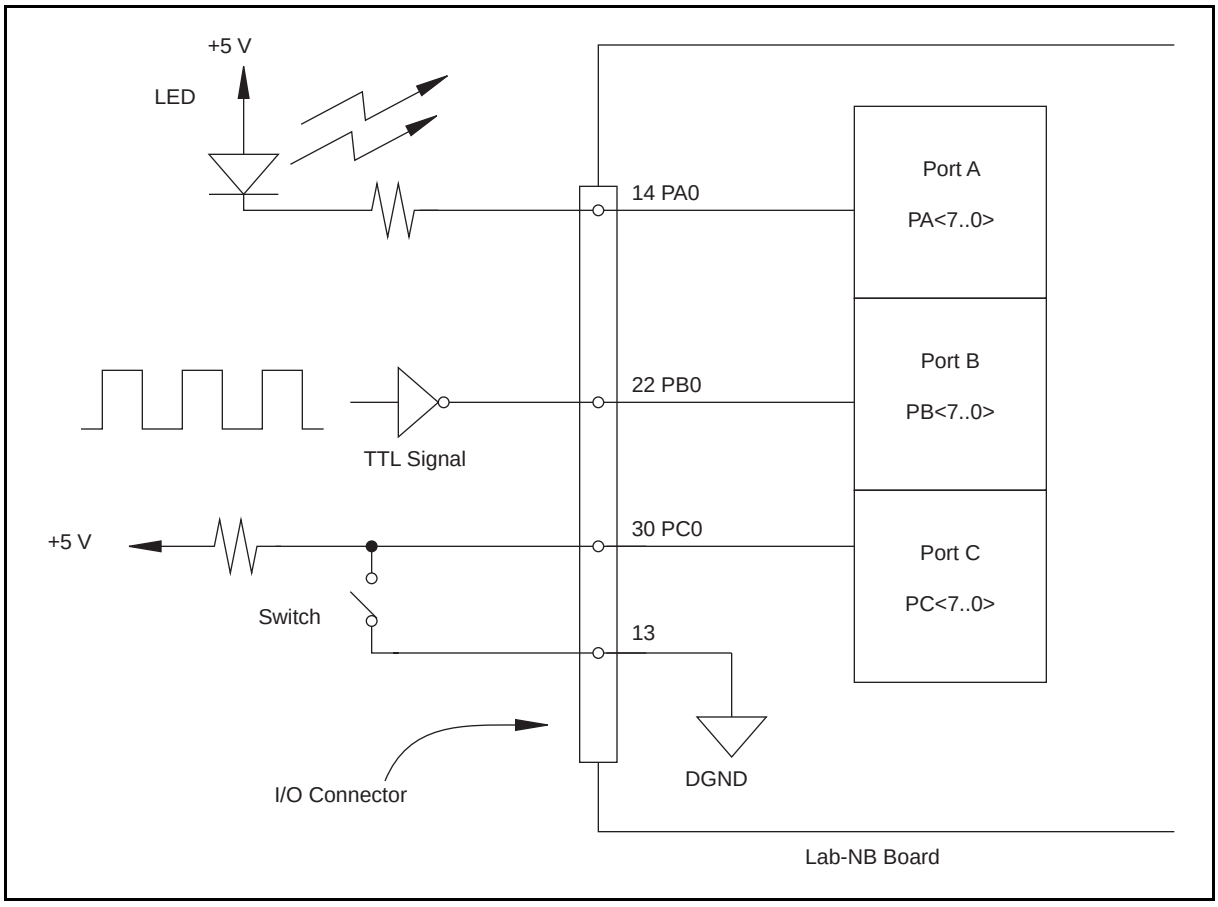


Figure 2-9. Digital I/O Connections

In Figure 2-9, port A is configured for digital output, and ports B and C are configured for digital input. Digital input applications include receiving TTL signals and sensing external device states such as the switch in Figure 2-9. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 2-9.

Port C Pin Connections

The signals assigned to port C depend on the mode in which the 82C55A is programmed. In mode 0, port C is considered as two 4-bit I/O ports. In modes 1 and 2, port C is used for status and handshaking signals with two or three I/O bits mixed in. The following table summarizes the signal assignments of port C for each programmable mode. See Chapter 4, *Register-Level Programming*, for programming information.

Warning: ***During programming, note that each time a port is configured, output ports A and C are reset to 0, and output port B is undefined.***

Table 2-2. Port C Signal Assignments

Programming Mode	Group A					Group B		
	PC7	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O
* Indicates that the signal is active low.								

Timing Specifications

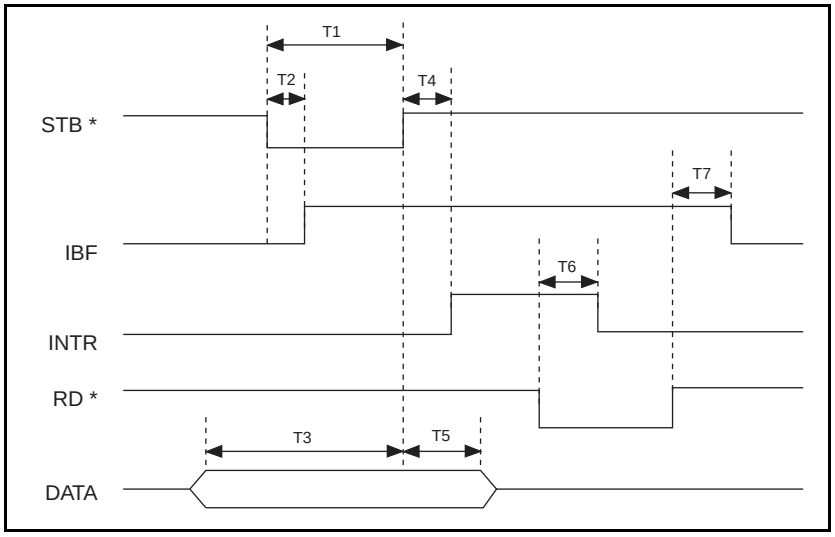
The handshaking lines STB* and IBF are used to synchronize input transfers. The handshaking lines OBF* and ACK* are used to synchronize output transfers.

The following signals are used in the timing diagrams shown later in this chapter:

Pin	Direction	Description
STB*	Input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. This is basically an input acknowledge signal.
ACK*	Input	Acknowledge Input—A low signal on this handshaking line indicates that the data written from the specified port has been accepted. This signal is basically a response from the external device that it has received the data from the Lab-NB.
OBF*	Output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written from the specified port.
INTR	Output	Interrupt Request—This signal becomes high when the 82C55A is requesting service during a data transfer. The appropriate interrupt enable signals must be set to generate this signal.
RD*	Internal	Read Signal—This signal is the read signal generated from the control lines of the NuBus.
WR*	Internal	Write Signal—This signal is the write signal generated from the control lines of the NuBus.
DATA	Bidirectional	Data Lines at the Specified Port—This signal indicates when the data on the data lines at a specified port is or should be available.

Mode 1 Input Timing

The following figure illustrates the timing specifications for an input transfer in mode 1.

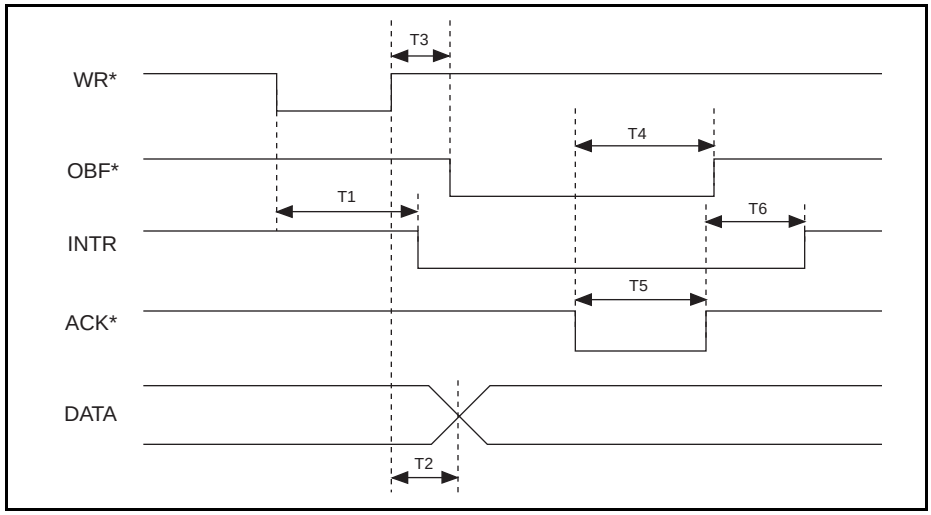


Name	Description	Minimum	Maximum
T1	STB* pulse width	100	–
T2	STB* = 0 to IBF = 1	–	150
T3	Data before STB* = 1	20	–
T4	STB* = 1 to INTR = 1	–	150
T5	Data after STB* = 1	50	–
T6	RD* = 0 to INTR = 0	–	200
T7	RD* = 1 to IBF = 0	–	150

All timing values are in nanoseconds.

Mode 1 Output Timing

The following figure illustrates the timing specifications for an output transfer in mode 1.

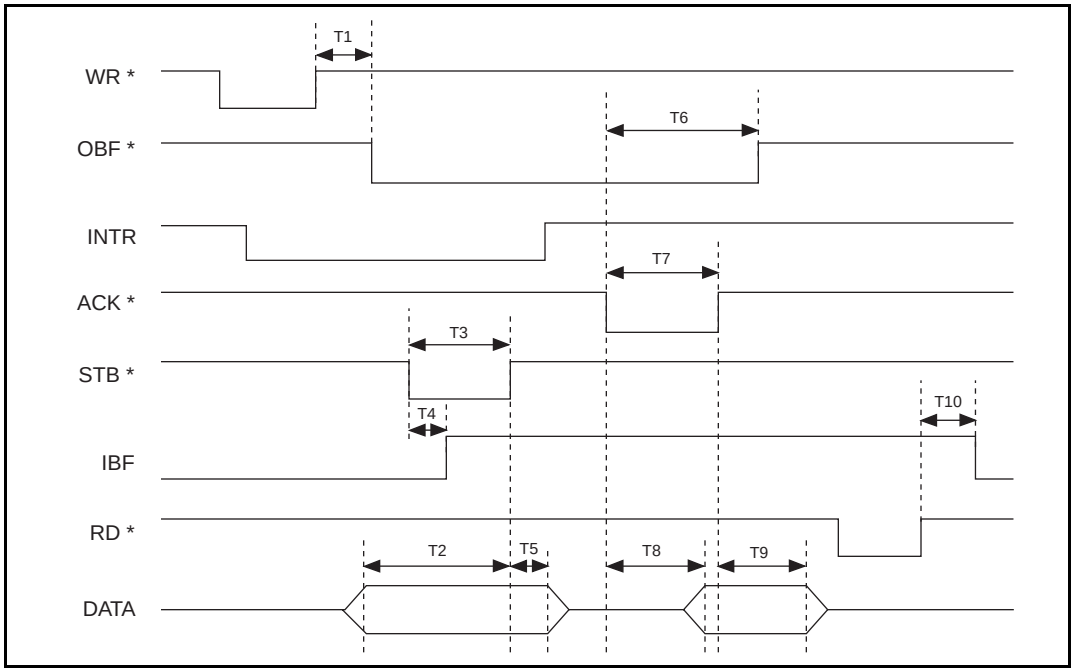


Name	Description	Minimum	Maximum
T1	WR* = 0 to INTR = 0	–	250
T2	WR* = 1 to output	–	200
T3	WR* = 1 to OBF* = 0	–	150
T4	ACK* = 0 to OBF* = 1	–	150
T5	ACK* pulse width	100	–
T6	ACK* = 1 to INTR = 1	–	150

All timing values are in nanoseconds.

Mode 2 Bidirectional Timing

The following figure illustrates the timing specifications for bidirectional transfers in mode 2.



Name	Description	Minimum	Maximum
T1	WR* = 1 to OBF* = 0	–	150
T2	Data before STB* = 1	20	–
T3	STB* pulse width	100	–
T4	STB* = 0 to IBF = 1	–	150
T5	Data after STB* = 1	50	–
T6	ACK* = 0 to OBF = 1	–	150
T7	ACK* pulse width	100	–
T8	ACK* = 0 to output	–	150
T9	ACK* = 1 to output float	20	250
T10	RD* = 1 to IBF = 0	–	150

All timing values are in nanoseconds.

Timing Connections

Pins 38 through 48 of the I/O connector are connections for timing I/O signals. The timing I/O of the Lab-NB is designed around the 8253 Counter/Timer integrated circuit. Two of these integrated circuits are employed in the Lab-NB. One, designated 8253(A), is used exclusively for DAQ timing, and the other, 8253(B), is available for general use. Pins 38 through 40 carry external signals that can be used for DAQ timing in place of the dedicated 8253(A). These signals are explained under *DAQ Timing Connections* later in this chapter. Pins 41 through 48 carry general-purpose timing signals from 8253(B). These signals are explained under *General-Purpose Timing Connections* later in this chapter.

DAQ Timing Connections

Counter 0 on the 8253(A) Counter/Timer (referred to as A0) is used as a sample-interval counter in timed A/D conversions. Counter 1 on the 8253(B) Counter/Timer (referred to as A1) is used as a sample counter in conjunction with counter 0 for data acquisition. These counters are not available for general use. In addition to counter A0, EXTCONV* can be used to externally time conversions. See Chapter 4, *Register-Level Programming*, for the programming sequence needed to enable this input. Figure 2-10 shows the timing requirements for the EXTCONV* input. An A/D conversion is initiated by a falling edge on the EXTCONV*. If EXTCONV* stays low more than 12 μsec, the data from this conversion is not latched into the FIFO memory until the following rising edge on EXTCONV*. If EXTCONV* stays low less than 12 μsec, the data from this conversion is latched into the FIFO memory after 12 μsec.

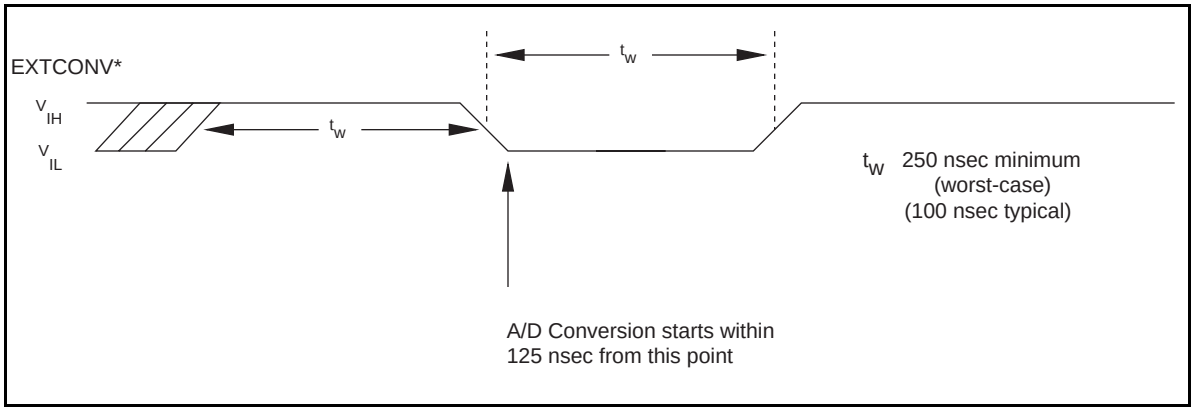


Figure 2-10. EXTCONV* Signal Timing

Another external control, EXTTRIG, is used for either starting a DAQ sequence or terminating an ongoing DAQ sequence, depending on the settings of the EXTTRIGEN and PRETRIG bits in the ADC Configuration Register.

If EXTTRIGEN is set, EXTTRIG serves as an external trigger to start a DAQ sequence. In this mode, posttrigger mode, the sample-interval counter is gated off until a rising edge is sensed on the EXTTRIG line. EXTCONV*, however, is enabled on the first rising edge of EXTCONV*, following the rising edge on the EXTTRIG line. Further transitions on the EXTTRIG line have no

effect until a new DAQ sequence is established. Figures 2-11 and 2-12 illustrate two possible posttrigger DAQ timing cases. In Figure 2-11, the rising edge on EXTTRIG is sensed when the EXTCONV* input is high. Thus, the first A/D conversion occurs on the second falling edge of EXTCONV*, after the rising edge on EXTTRIG. In Figure 2-12, the rising edge on EXTTRIG is sensed when the EXTCONV* input is low. In this case, the first A/D conversion occurs on the first falling edge of EXTCONV*, after the rising edge on EXTTRIG. Notice that Figures 2-11 and 2-12 show a controlled acquisition mode DAQ sequence; that is, Sample Counter A1 disables further A/D conversions after the programmed count (3 in the examples shown in Figures 2-11 and 2-12) expires. The counter is not loaded with the programmed count until the first falling edge following a rising edge on the clock input; therefore two extra conversion pulses are generated as shown in Figures 2-11 and 2-12. EXTTRIG can also be used as an external trigger in freerun acquisition mode.

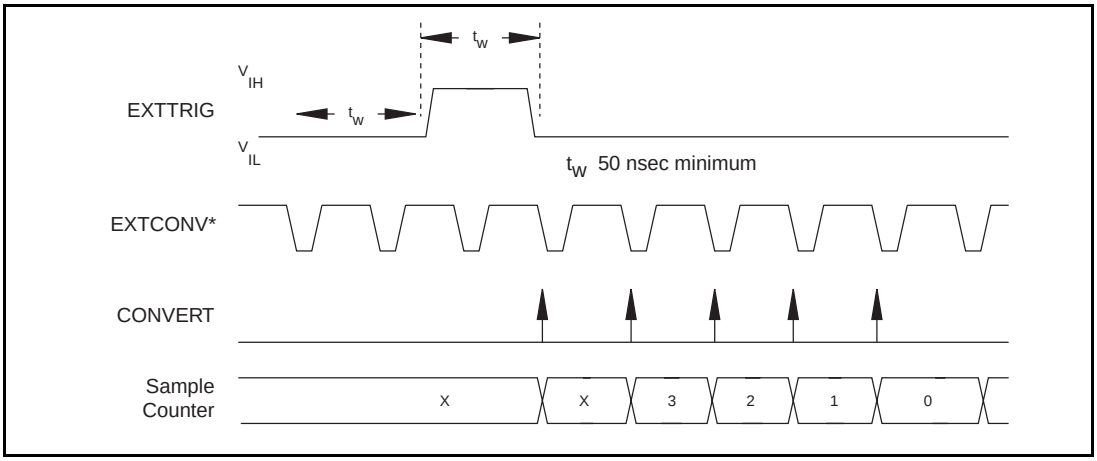


Figure 2-11. Posttrigger DAQ Timing
(EXTCONV* High When Trigger Sensed)

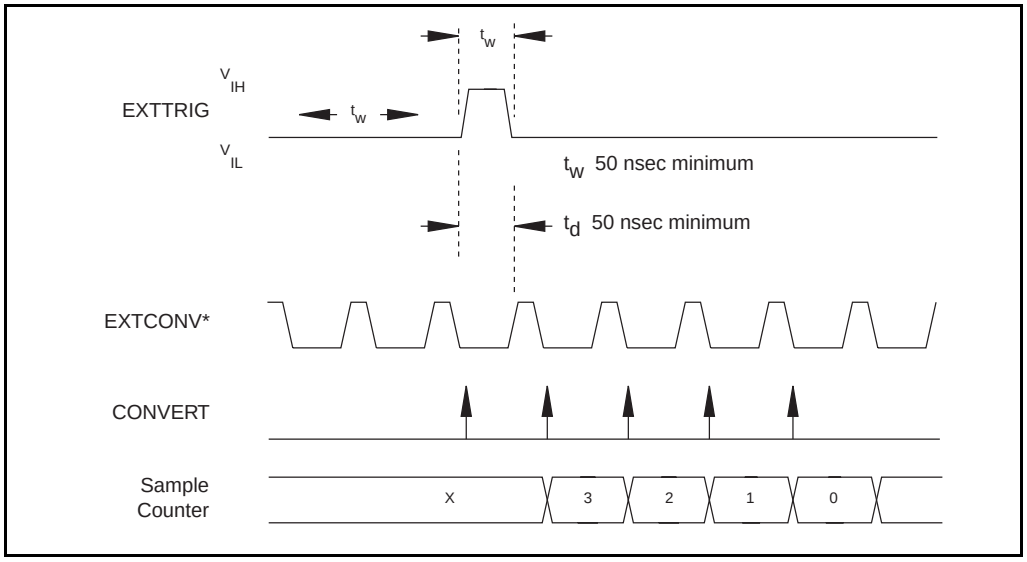


Figure 2-12. Posttrigger DAQ Timing
(EXTCONV* Low When Trigger Sensed)

If PRETRIG is set, EXTTRIG serves as a pretrigger signal. In pretrigger mode, A/D conversions are enabled via software before a rising edge is sensed on the EXTTRIG input. However, the sample counter, counter A1, is not gated on until a rising edge is sensed on the EXTTRIG input. Additional transitions on this line have no effect until a new DAQ sequence is set up. Conversions remain enabled for the programmed count after the trigger; therefore, data can be acquired before and after the trigger. Pretrigger mode works only in controlled acquisition mode, that is, counter A1 is required to disable A/D conversions after the programmed count expires. Thus, the maximum number of samples acquired after the trigger is limited to 65,535. The number of samples acquired before the trigger is limited only by the size of the memory buffer available for data acquisition. Figure 2-13 shows a pretrigger DAQ timing sequence.

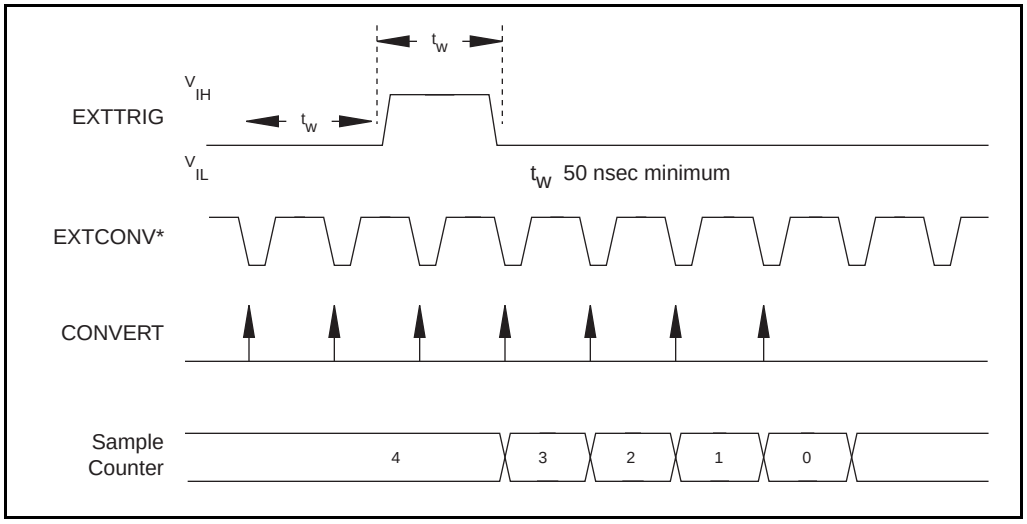


Figure 2-13. Pretrigger DAQ Timing

Because both pretrigger and posttrigger modes use EXTTRIG input, only one mode can be used at a time. If neither PRETRIG nor EXTTRIGEN is set high, this signal has no effect.

The final external control signal, EXTUPDATE*, is used to externally control the updating of the output voltage of the 12-bit DACs or to generate an externally timed interrupt on the NuBus. If the TMRWGEN bit in the DAC Configuration Register is set, the DAC voltage is updated by a low level on the EXTUPDATE* signal. If the TMRINTEN bit in the Interrupt Control Register is set, an interrupt is generated whenever a rising edge is detected on the EXTUPDATE* bit . Therefore, externally timed, interrupt-driven waveform generation is possible on the Lab-NB. Figure 2-14 illustrates a waveform generation timing sequence using the EXTUPDATE* signal. Notice that the DACs are updated by a *low level* on the EXTUPDATE* line. Any writes to the DAC Data Registers while EXTUPDATE* is low therefore result in immediate update of the DAC output voltages.

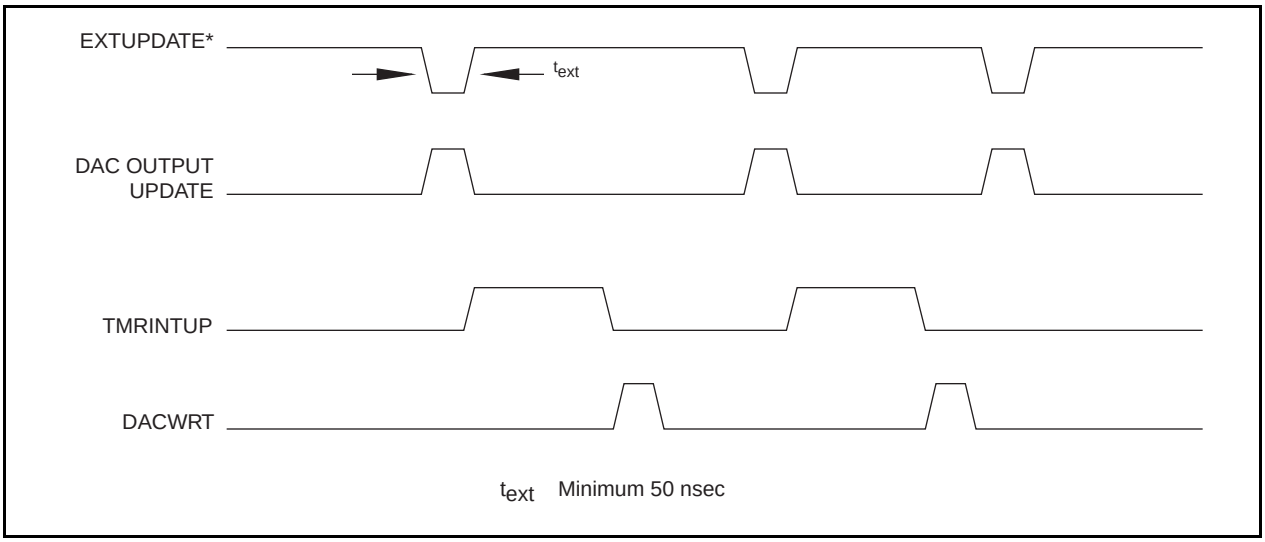


Figure 2-14. Waveform Generation Timing with the EXTUPDATE* Signal

Since a rising edge on the EXTUPDATE* signal always sets the TMRINTUP bit in the Interrupt Status Register, the EXTUPDATE* signal can also be used for periodic interrupt generation timed by an external source. The TMRINTUP bit is cleared by writing to either of the two DACs or to the TMRINTCL bit location. Figure 2-15 illustrates a timing sequence where EXTUPDATE* is being used to generate a NuBus interrupt.

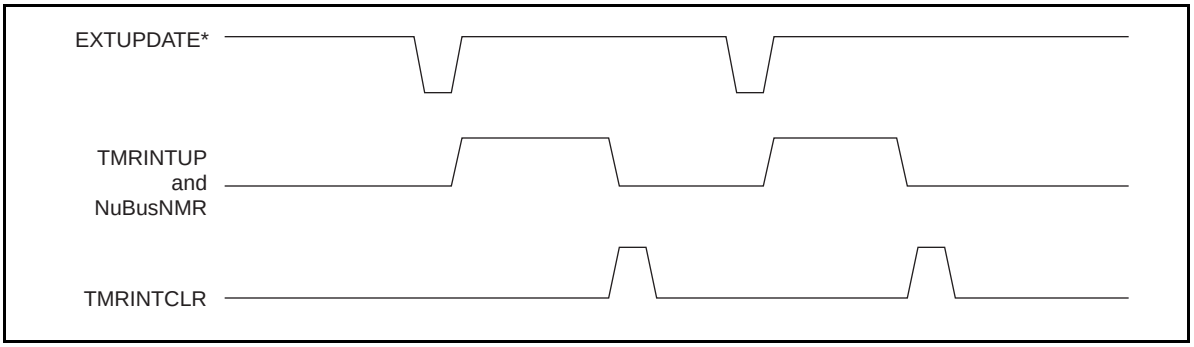


Figure 2-15. NuBus Interrupt Generation with the EXTUPDATE* Signal

The following specifications and ratings apply to the EXTCONV*, EXTTRIG and EXTUPDATE* signals.

Absolute maximum voltage input rating -0.5 to 7.0 V with respect to DGND

8253 digital input specifications (referenced to DGND):

V_{IH} input logic high voltage	2.2 V min
V_{IL} input logic low voltage	0.8 V max
Input load current	±10 µA max

8253 digital output specifications (referenced to DGND):

V_{OH} output logic high voltage	2.4 V min
V_{OL} output logic low voltage	0.45 V max
I_{OH} output source current, at V_{OH}	400 µA max
I_{OL} output sink current, at V_{OL}	2.2 mA max

General-Purpose Timing Signal Connections

The general-purpose timing signals include the GATE, CLK, and OUT signals for the three 8253(B) counters. The 8253 Counter/Timers can be used for general-purpose applications such as pulse and square wave generation; event counting; and pulse-width, time-lapse, and frequency measurement. For these applications, CLK and GATE signals are sent to the counters, and the counters are programmed for various operations. The single exception is counter B0, which has an internal 2-MHz clock.

The 8253 Counter/Timer is described briefly in Chapter 3, *Theory of Operation*. For detailed programming information, consult Appendix C, *AMD 8253 Data Sheet*.

Pulse and square wave generation are performed by programming a counter to generate a timing signal at its OUT output pin.

Event counting is performed by programming a counter to count rising or falling edges applied to any of the 8253 CLK inputs. The counter value can then be read to determine the number of edges that have occurred. Counter operation can be gated on and off during event counting. Figure 2-16 shows connections for a typical event-counting operation where a switch is used to gate the counter on and off.

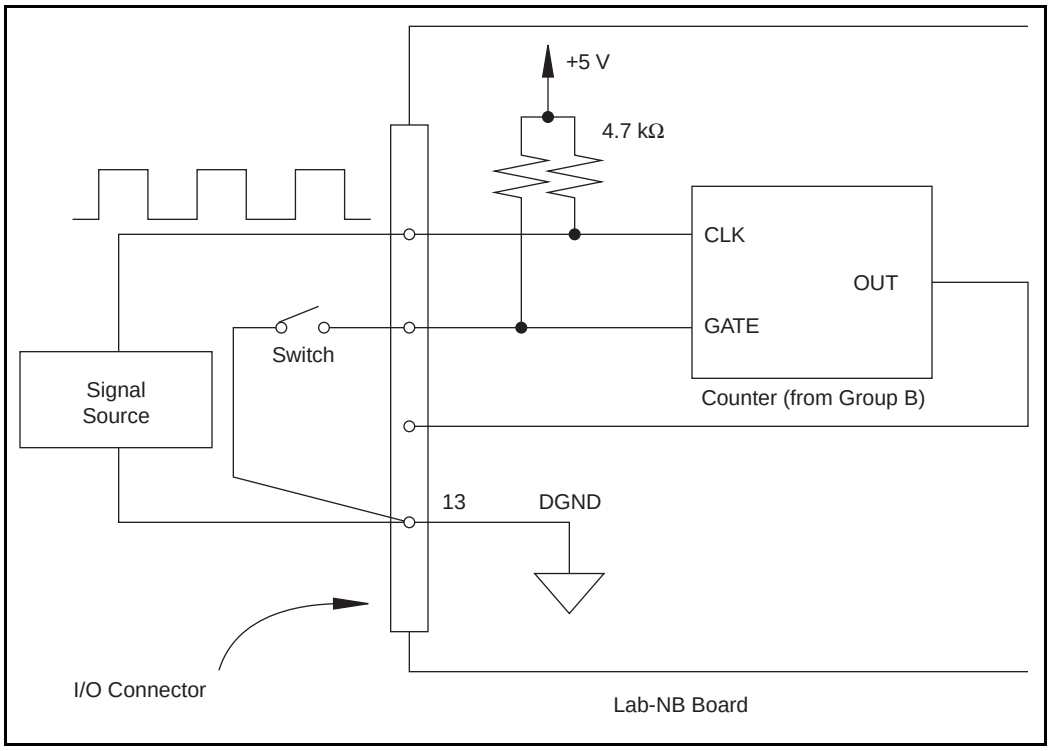


Figure 2-16. Event-Counting Application with External Switch Gating

Pulse-width measurement is performed by level gating. The pulse to be measured is applied to the counter GATE input. The counter is loaded with the known count and is programmed to count down while the signal at the GATE input is high. The pulse width equals the counter difference (loaded value minus read value) multiplied by the CLK period.

Time-lapse measurement is performed by programming a counter to be edge gated. An edge is applied to the counter GATE input to start the counter. The counter can be programmed to start counting after receiving a low-to-high edge. The time lapse since receiving the edge equals the counter value difference (loaded value minus read value) multiplied by the CLK period.

Frequency measurement is performed by programming a counter to be level gated and by counting the number of falling edges in a signal applied to a CLK input. The gate signal applied to the counter GATE input is of known duration. In this case, the counter is programmed to count falling edges at the CLK input while the gate is applied. The frequency of the input signal then equals the count value divided by the gate period. Figure 2-17 shows the connections for a frequency measurement application. A second counter could also be used to generate the gate signal in this application.

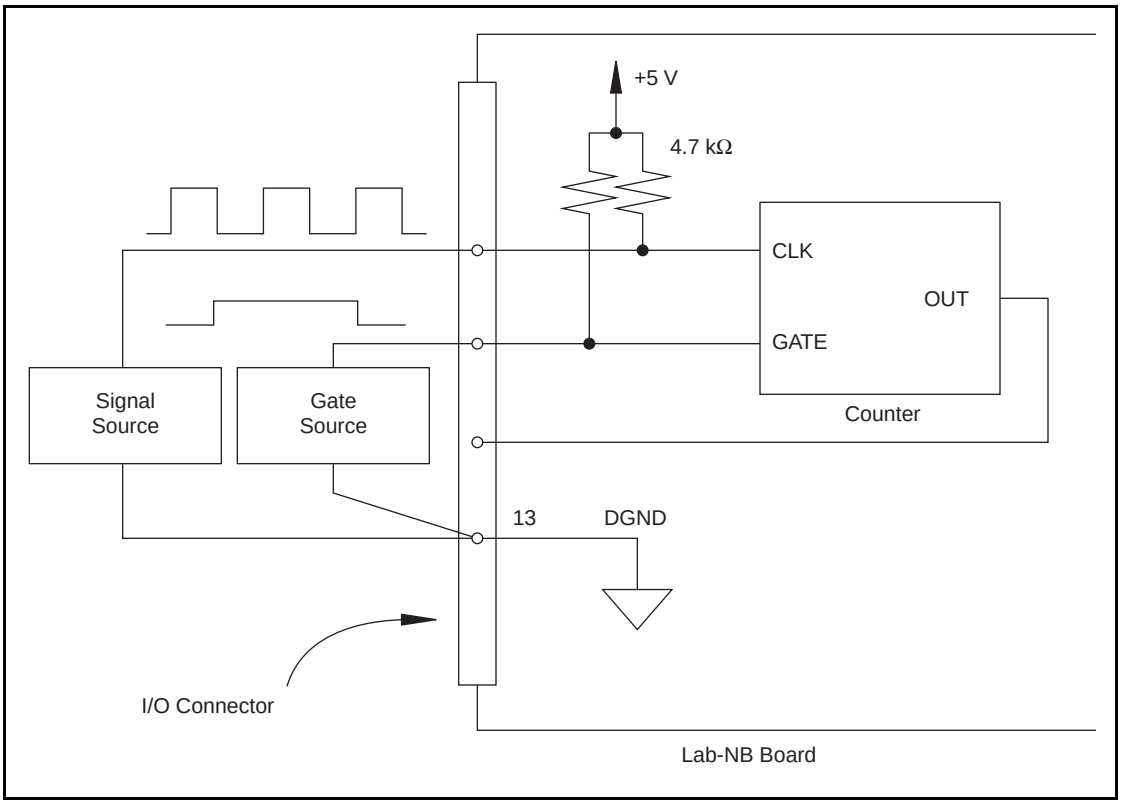


Figure 2-17. Frequency Measurement Application

The GATE, CLK, and OUT signals for counters B1 and B2 are available at the I/O connector. In addition, the GATE and CLK pins are pulled up to +5 V through a 4.7 kΩ resistor. The input and output ratings and timing specifications for the 8253 signals are given next.

The following specifications and ratings apply to the 8253 I/O signals:

Absolute maximum voltage input rating -0.5 to 7.0 V with respect to DGND

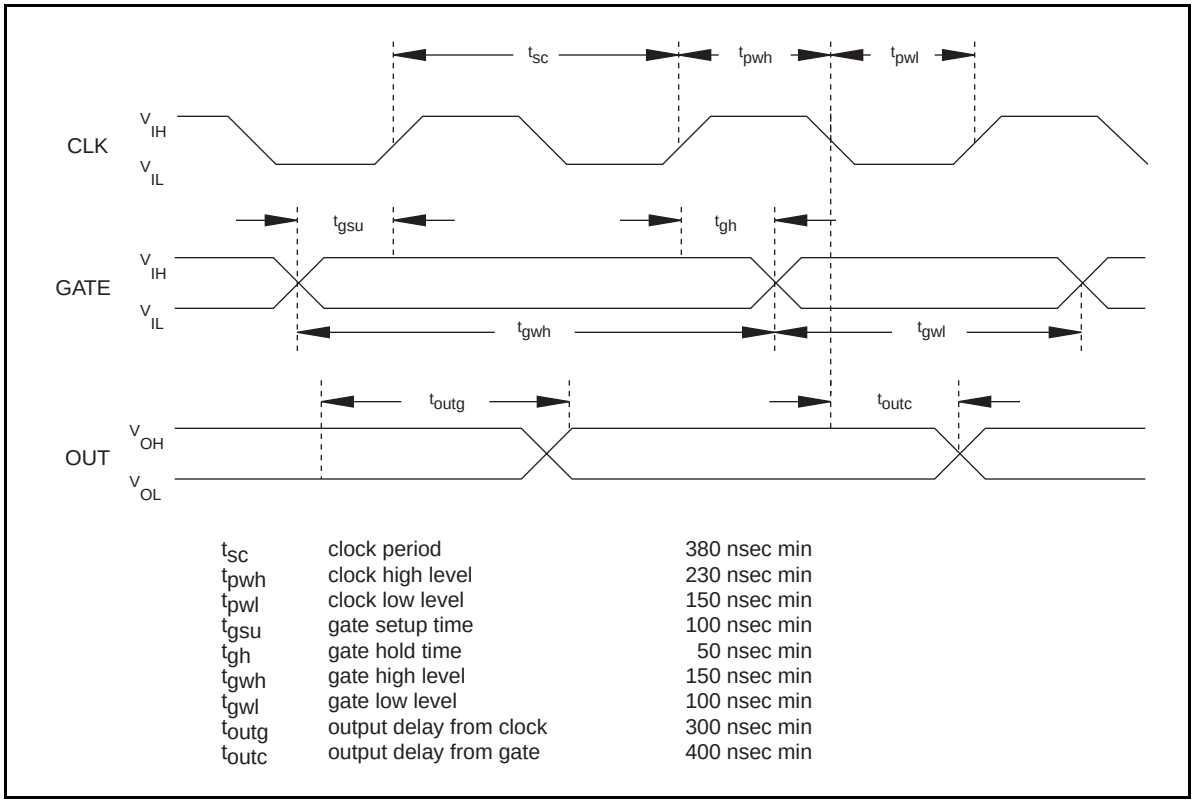
8253 digital input specifications (referenced to DGND):

V_{IH} input logic high voltage	2.2 V min
V_{IL} input logic low voltage	0.8 V max
Input load current	±10 µA max

8253 digital output specifications (referenced to DGND):

V_{OH} output logic high voltage	2.4 V min
V_{OL} output logic low voltage	0.45 V max
I_{OH} output source current, at V_{OH}	400 µA max
I_{OL} output sink current, at V_{OL}	2.2 mA max

Figure 2-18 shows the timing requirements for the GATE and CLK input signals and the timing specifications for the OUT output signals of the 8253.



t_{sc}	clock period	380 nsec min
t_{pwh}	clock high level	230 nsec min
t_{pwl}	clock low level	150 nsec min
t_{gsu}	gate setup time	100 nsec min
t_{gh}	gate hold time	50 nsec min
t_{gwh}	gate high level	150 nsec min
t_{gwl}	gate low level	100 nsec min
t_{outg}	output delay from clock	300 nsec min
t_{outc}	output delay from gate	400 nsec min

Figure 2-18. General-Purpose Timing Signals

The GATE and OUT signals in Figure 2-18 are referenced to the rising edge of the CLK signal.

Chapter 3
Theory of Operation

This chapter contains a functional overview of the Lab-NB and explains the operation of each functional unit making up the Lab-NB.

Functional Overview

The block diagram in Figure 3-1 shows a functional overview of the Lab-NB board.

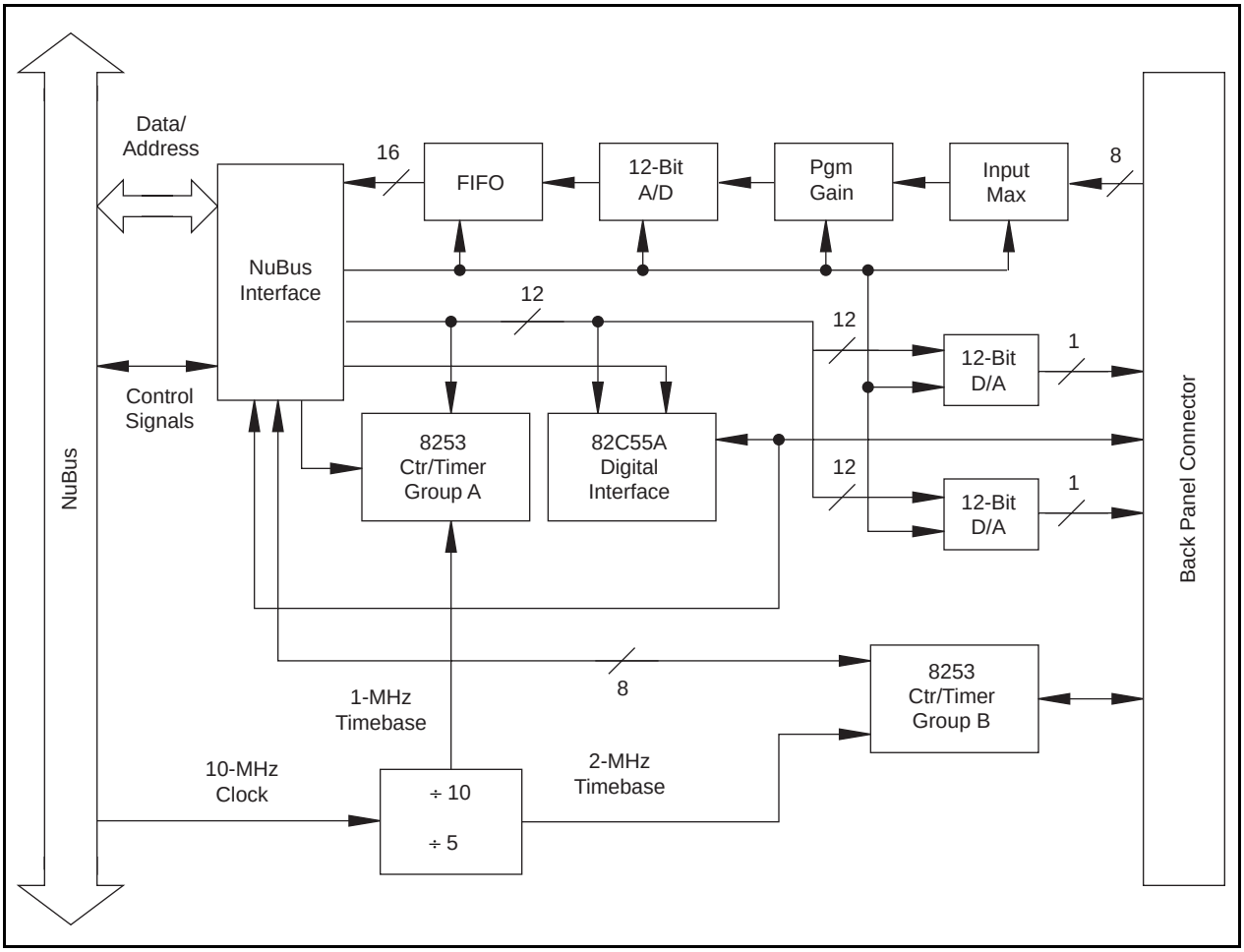


Figure 3-1. Lab-NB Block Diagram

The following are the major components making up the Lab-NB board:

- NuBus interface circuitry
- Analog input and DAQ circuitry
- Analog output circuitry
- Digital I/O circuitry
- Timing I/O circuitry

DAQ functions can be executed by using the analog input circuitry and some of the timing I/O circuitry. The internal data and control buses interconnect the components. The theory of operation for each of these components is explained in the remainder of this chapter. The theory of operation for the DAQ circuitry is included with the discussion of the analog input circuitry.

NuBus Interface Circuitry

The Macintosh NuBus is a 32-bit multiplexed address and data bus with a 10-MHz bus clock. In addition, the NuBus provides interface signals for interrupt and read/write operations. The NuBus interface circuitry consists of a starting address detector, interface timing signals, and address-decoder circuitry. This interface circuitry generates the signals necessary to control and monitor the operation of the Lab-NB multifunction circuitry.

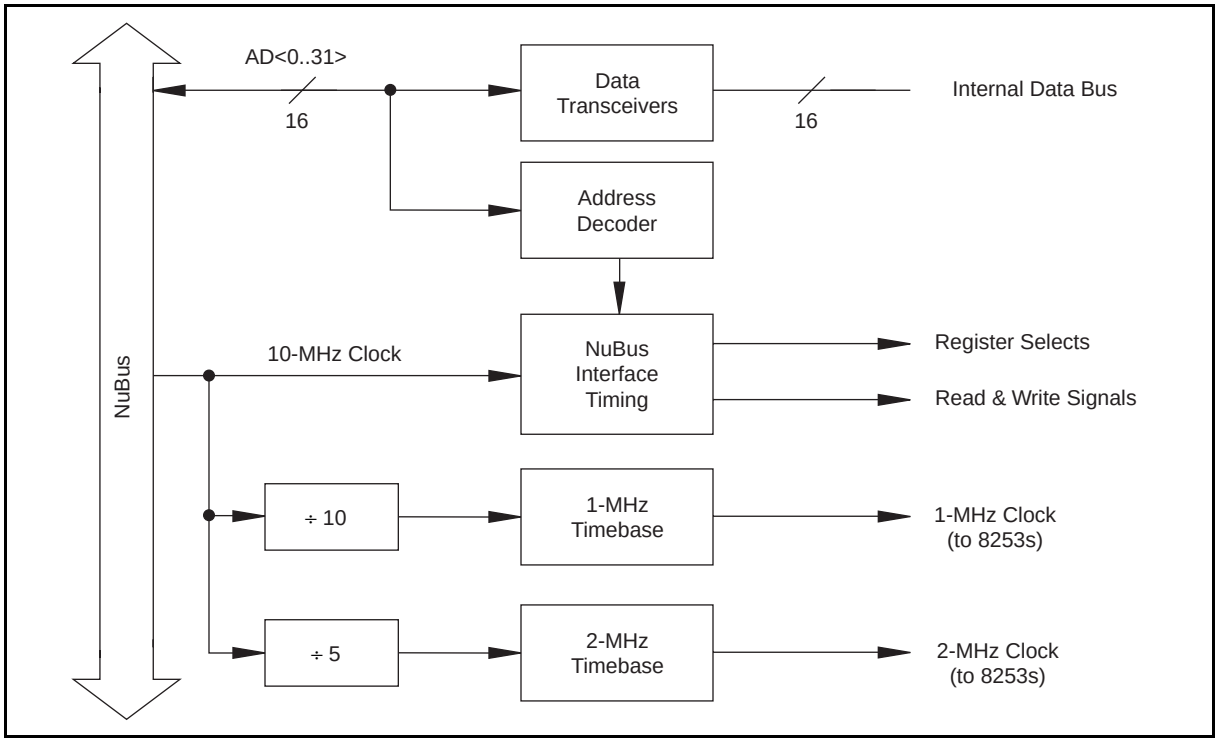


Figure 3-2. NuBus Interface Circuitry Block Diagram

The starting-address-detecting circuitry on the Lab-NB matches address lines 23 through 21 to the starting address specified by the slot in which the Lab-NB board is installed. The remaining address lines (19 through 0) are decoded by the Lab-NB address-decoding circuitry to generate select signals for the registers on the board. The NuBus interface timing signals are decoded by the Lab-NB interface timing circuitry, which generates the proper read and write signals for the remaining Lab-NB circuitry. The Lab-NB board can cause interrupts in the Macintosh by driving the NuBus NMRQ* interrupt line.

Analog Input and DAQ Circuitry

The Lab-NB provides eight channels of analog input with software-programmable gain and 12-bit A/D conversion. Using the timing circuitry, the Lab-NB can also automatically time multiple A/D conversions. Figure 3-3 shows a block diagram of the analog input and DAQ circuitry.

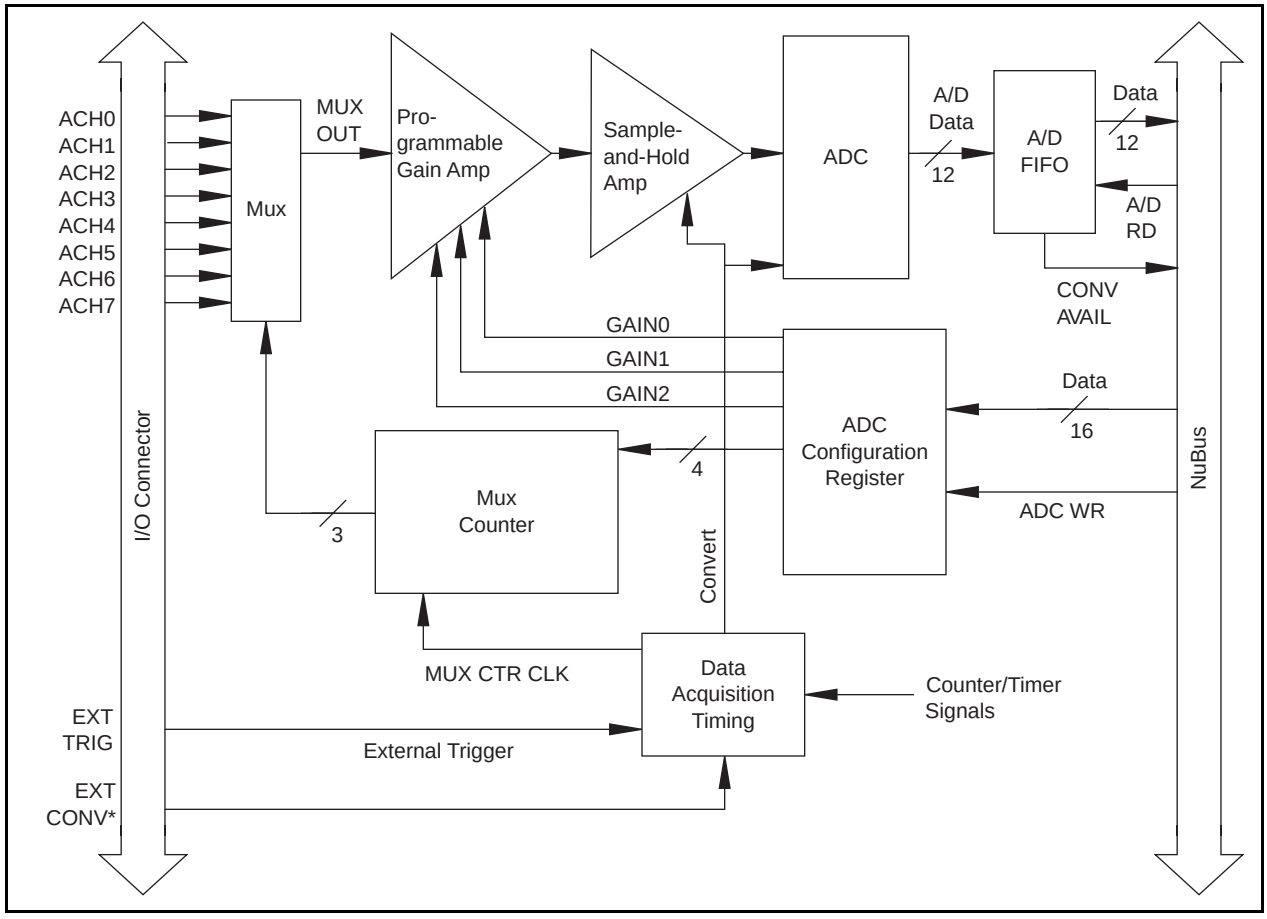


Figure 3-3. Analog Input and DAQ Circuitry Block Diagram

Analog Input Circuitry

The analog input circuitry consists of an input multiplexer, a software-programmable gain amplifier, a 12-bit ADC, and a 12-bit FIFO memory that is sign-extended to 16 bits.

The input multiplexer is made up of a CMOS analog input multiplexer and has eight analog input channels (channels 0 through 7). The input multiplexers provide input overvoltage protection of ±45 V, powered on or off.

The programmable gain amplifier applies gain to the input signal, allowing an input analog signal to be amplified before being sampled and converted, thus increasing measurement resolution and accuracy. The gain of the instrumentation amplifier is selected under software control. The Lab-NB board provides gains of 1, 2, 5, 10, 20, 50, and 100.

The Lab-NB uses a 12-bit successive-approximation ADC. The 12-bit resolution of the converter allows the converter to resolve its input range into 4,096 different steps. This resolution also provides a 12-bit digital word that represents the value of the input voltage level with respect to the converter input range. The ADC itself has a single input range of 0 to +5 V. Additional circuitry allows inputs of ±5 V or 0 to 10 V.

When an A/D conversion is complete, the ADC clocks the result into the A/D FIFO. The A/D FIFO is 16 bits wide and 16 words deep. This FIFO serves as a buffer to the ADC and provides two benefits. First, any time an A/D conversion is complete, the value is saved in the A/D FIFO for later reading, and the ADC is free to start a new conversion. Secondly, the A/D FIFO can collect up to 16 A/D conversion values before any information is lost, thus allowing software some extra time (16 times the sample interval) to catch up with the hardware. If more than 16 values are stored in the A/D FIFO without the A/D FIFO being read from, an error condition called A/D FIFO Overflow occurs and A/D conversion information is lost.

The A/D FIFO generates a signal that indicates when it contains A/D conversion data. The state of this signal can be read from the Lab-NB Status Register.

The output from the ADC can be interpreted as either straight binary or two's complement, depending on which input mode you select (unipolar or bipolar). In unipolar mode, the data from the ADC is interpreted as a 12-bit straight binary number with a range of 0 to +4,095. In bipolar mode, the data from the ADC is interpreted as a 12-bit two's complement number with a range of -2,048 to +2,047. In this mode, the MSB of the ADC result is inverted to make it two's complement. The output from the ADC is then sign-extended to 16 bits, causing either a leading 0 or a leading F (hex) to be added, depending on the coding and the sign. Thus, data values read from the FIFO are 16 bits wide.

DAQ Timing Circuitry

A DAQ operation refers to the process of taking a sequence of A/D conversions with the sample interval (the time between successive A/D conversions) carefully timed. The DAQ timing circuitry consists of various clocks and timing signals that perform this timing. Two types of data acquisition can be performed by the Lab-NB board: single-channel data acquisition and

multichannel (scanned) data acquisition. Scanned data acquisition uses a counter to automatically switch between analog input channels during data acquisition.

DAQ timing consists of signals that initiate a DAQ operation, initiate individual A/D conversions, gate the DAQ operation, and generate scanning clocks. Sources for these signals are supplied mainly by timers on the Lab-NB board. One of the two 8253 integrated circuits is reserved for this purpose.

An A/D conversion can be initiated by a high-to-low transition on the counter A0 output (OUT A0) of the 8253(A) Counter/Timer chip on the Lab-NB or by a high-to-low transition on EXTCONV* input. During data acquisition, the onboard sample-interval counter–counter 0 of 8253(A)–is used to generate pulses that initiate A/D conversions.

The sample-interval timer is a 16-bit down counter that uses the 1-MHz clock onboard to generate sample intervals from 2 µsec to 65,535 µsec (see *Timing I/O Circuitry* later in this chapter). Alternatively, it can use the output from counter B0 (OUTB0) of the 8253(B) Counter/Timer chip on the Lab-NB. Each time the sample-interval timer reaches 0, it generates a pulse and reloads with the programmed sample-interval count. This operation continues until the counter is reprogrammed.

As stated in Chapter 4, *Register-Level Programming*, only counter A0 is required for DAQ operations in freerun acquisition mode. The software must keep track of the number of conversions that has occurred and turn off counter A0 after the required number of conversions has been obtained. In controlled acquisition mode, two counters (counters A0 and A1) are required for a DAQ operation. Counter A0 generates the conversion pulses, and counter A1 gates off counter A0 after the programmed count has expired.

Single-Channel Data Acquisition

During single-channel data acquisition, the channel select and gain bits in the A/D Configuration Register select the gain and analog input channel before data acquisition is initiated. These gain and multiplexer settings remain constant during the entire DAQ process; therefore, all A/D conversion data is read from a single channel.

Multichannel (Scanned) Data Acquisition

Multichannel data acquisition is performed by enabling scanning during data acquisition. Multichannel scanning is controlled by a scan counter.

For scanning operations, the scan counter decrements from the highest numbered channel (specified by the user) through channel 0 and then repeats the sequence. Thus, any number of channels from 2 to 8 can be scanned. Notice that the same gain setting is used for all channels in the scan sequence.

DAQ Rates

Maximum DAQ rates (number of samples per second) are determined by the conversion period of the ADC plus the sample-and-hold acquisition time. During multichannel scanning, the DAQ rates are further limited by the settling time of the input multiplexers and programmable gain amplifier. After the input multiplexers are switched, the amplifier must be allowed to settle to the new input signal value to within 12-bit accuracy before an A/D conversion is performed, or else 12-bit accuracy will not be achieved. The settling time is a function of the gain selected.

The Lab-NB DAQ timing circuitry detects when DAQ rates are high enough to cause A/D conversions to be lost. If this is the case, this circuitry sets an Overrun error flag in the Lab-NB Status Register. If the recommended DAQ rates in Table 3-2 are exceeded (an error flag is *not* automatically set), the analog input circuitry may not perform at 12-bit accuracy. If these rates are exceeded by more than a few microseconds, A/D conversions may be lost. Table 3-1 shows the recommended multiplexer and gain settling times for different gain settings.

Table 3-2 shows the maximum recommended DAQ rates for both single-channel and multichannel data acquisition. Notice that for a single-channel data acquisition, the data can be acquired at the maximum rate at any gain setting. The analog input bandwidth, however, is lower for higher gains. For multichannel data acquisition, observing the DAQ rates given in Table 3-2 ensures 12-bit accuracy.

Table 3-1. Analog Input Settling Time Versus Gain

Gain Setting	Settling Time Recommended
1	16 µsec
2, 5	20 µsec
10, 20	30 µsec
50, 100	100 µsec

Table 3-2. Lab-NB Maximum Recommended DAQ Rates

Single-Channel Data Acquisition:	
Any Gain Setting	62.5 ksamples/sec
Multichannel Data Acquisition:	
Gain = 1	62.5 ksamples/sec
Gain = 2, 5	50.0 ksamples/sec
Gain = 10, 20	33.3 ksamples/sec
Gain = 50, 100	10.0 ksamples/sec

The recommended DAQ rates given in Table 3-2 assume that voltage levels on all the channels included in the scan sequence are within range for the given gain and are driven by low-impedance sources. The signal ranges for the possible gains are shown in Table 3-3 and Table 3-4. Signal levels outside the ranges shown in Table 3-3 on the channels included in the scan sequence adversely affect the input settling time. Similarly, greater settling time may be required for channels driven by high-impedance signal sources.

Table 3-3. Bipolar Analog Input Signal Range Versus Gain

Gain Setting	Input Signal Range
1	-5 V to 4.99756 V
2	-2.5 V to 2.49878 V
5	-1.0 V to 0.99951 V
10	-500 mV to 499.756 mV
20	-250 mV to 249.877 mV
50	-100 mV to 99.951 mV
100	-50 mV to 49.975 mV

Table 3-4. Unipolar Analog Input Signal Range Versus Gain

Gain Setting	Input Signal Range
1	0 V to 9.99756 V
2	0 V to 4.99878 V
5	0 V to 1.99951 V
10	0 mV to 999.756 mV
20	0 mV to 499.877 mV
50	0 mV to 199.951 mV
100	0 mV to 99.975 mV

Analog Output Circuitry

The Lab-NB provides two channels of 12-bit D/A output. Each analog output channel can provide unipolar or bipolar output. Figure 3-4 shows a block diagram of the analog output circuitry.

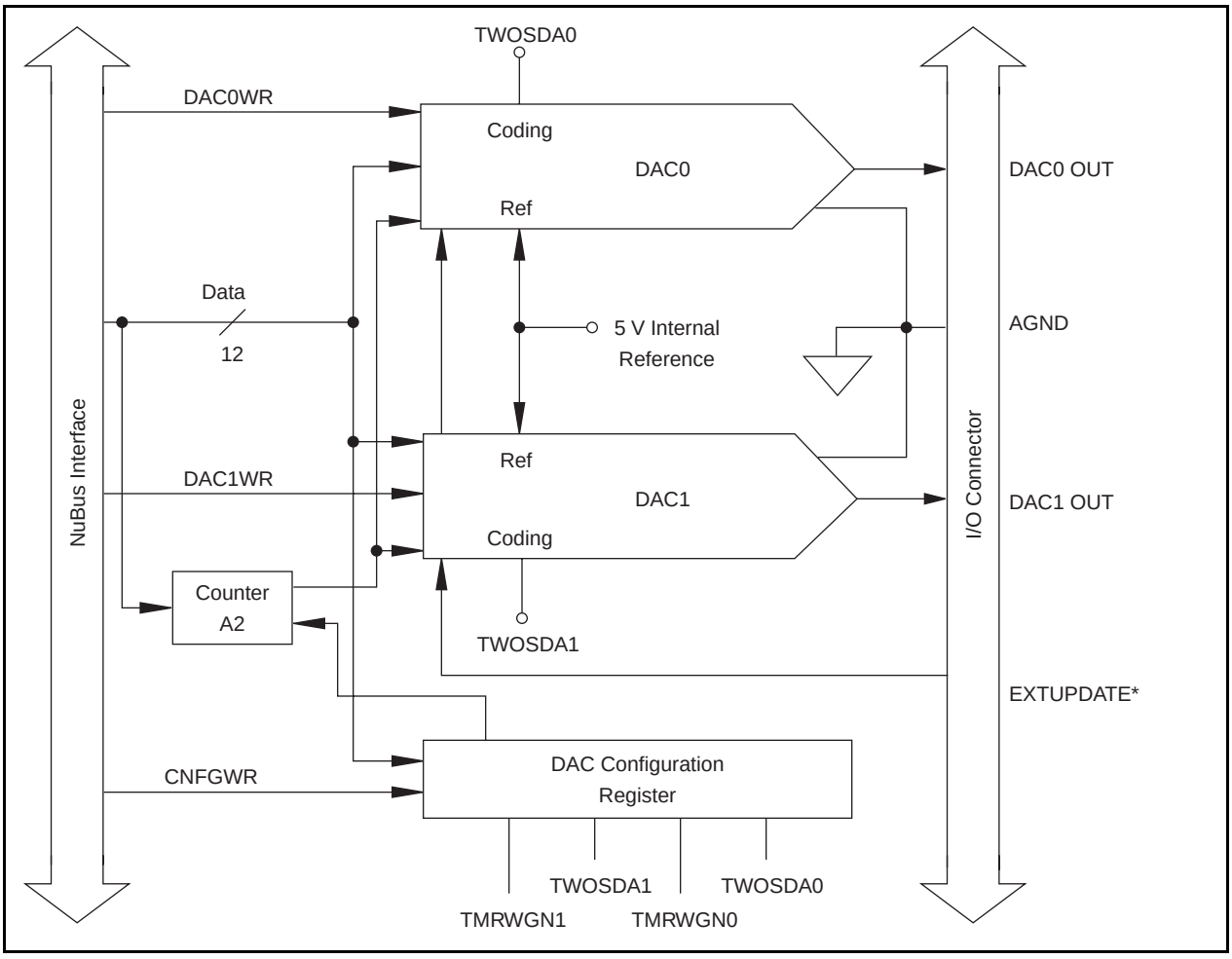


Figure 3-4. Analog Output Circuitry Block Diagram

Each analog output channel contains a 12-bit DAC. The DAC in each analog output channel generates a voltage proportional to the input voltage reference (V_{ref}) multiplied by the digital code loaded into the DAC. Each DAC can be loaded with a 12-bit digital code by writing to the DAC0 and DAC1 Registers on the Lab-NB board. The voltage output from the two DACs is available at the Lab-NB I/O connector DAC0 OUT and DAC1 OUT pins.

The DAC voltages can be updated in any of three ways, depending on the setting of the TMRWGN bit. If this bit is cleared, the DAC output voltage is updated as soon as the corresponding DAC Data Register is written to. If the TMRWGN bit is set, the DAC output voltage does not change until a falling edge is detected either from counter A2 or from EXTUPDATE*.

Each DAC channel can be jumper-programmed for either a unipolar voltage output or a bipolar voltage output range. A unipolar output gives an output voltage range of 0.0000 V to +9.9976 V. A bipolar output gives an output voltage range of -5.0000 V to +4.9976 V. For unipolar output, 0.0000 V output corresponds to a digital code word of 0. For bipolar output, -5.0000 V output corresponds to a digital code word of F800 (hex). One LSB is the voltage increment

corresponding to an LSB change in the digital code word. For both unipolar and bipolar output, one LSB corresponds to the following formula:

$$\frac{10\ V}{4,096}$$

Digital I/O Circuitry

The digital I/O circuitry is designed around an 82C55A integrated circuit. The 82C55A is a general-purpose PPI containing 24 programmable I/O pins. These pins represent the three 8-bit I/O ports (A, B, and C) of the 82C55A as well as PA<0..7>, PB<0..7>, and PC<0..7> on the Lab-NB I/O connector. The 82C55A also has a control register to configure each of the three I/O ports on the chip. These ports can be programmed as two groups of 12 signals or as three individual 8-bit ports. In addition, the board can be programmed in one of the three modes of operation: basic I/O, strobed I/O, or bidirectional bus. The programming of the digital I/O circuitry is covered in Chapter 4, *Register-Level Programming*.

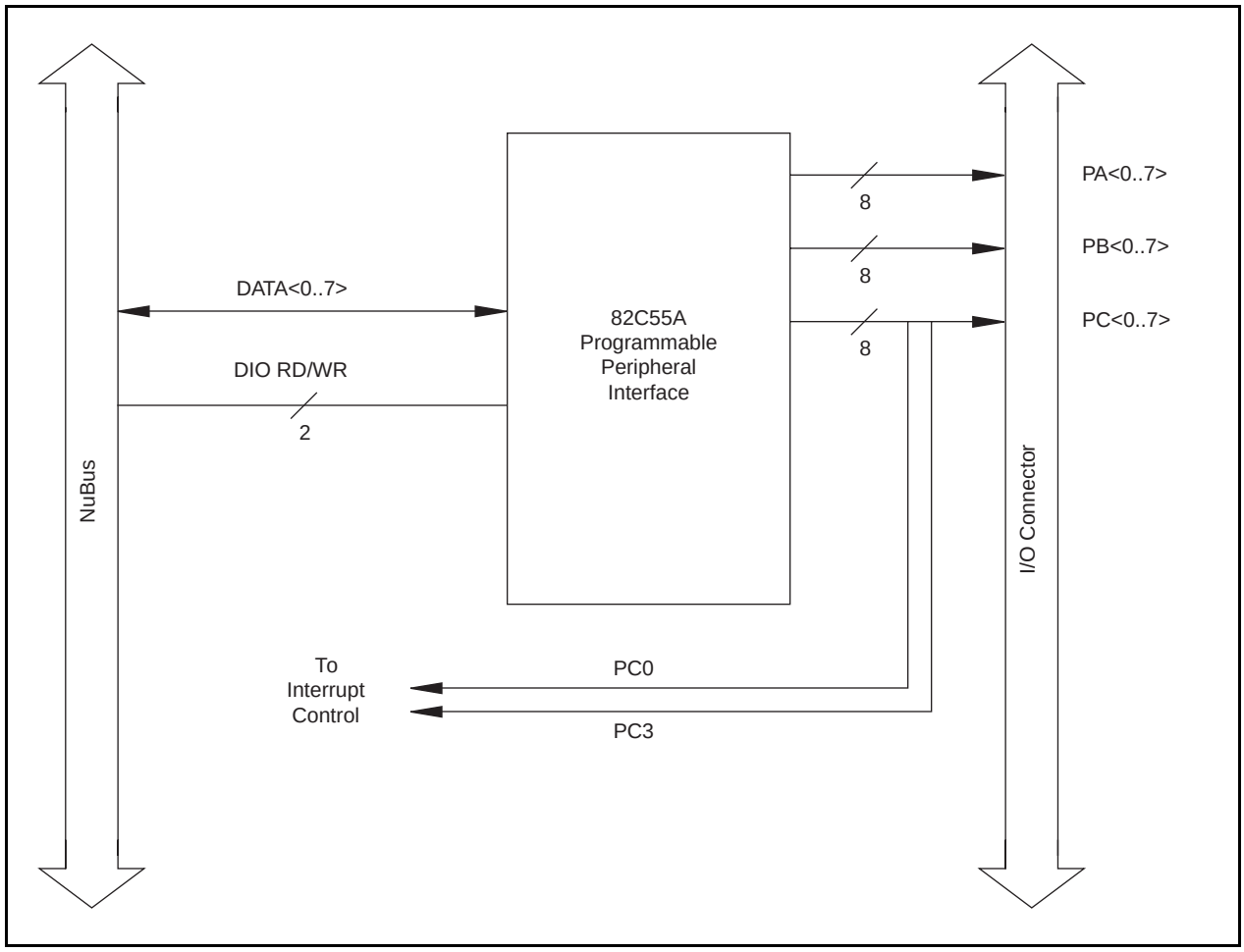


Figure 3-5. Digital I/O Circuitry Block Diagram

All three ports on the 82C55A are TTL-compatible. When enabled, the digital output ports are capable of sinking 2.5 mA of current and sourcing 2.5 mA of current on each digital I/O line. When the ports are not enabled, the digital I/O lines act as high-impedance inputs.

Timing I/O Circuitry

The Lab-NB uses two 8253 Counter/Timer integrated circuits for DAQ timing and for general-purpose timing I/O functions. One of these is used internally for DAQ timing, and the other is available for general use. Figure 3-6 shows a block diagram of both groups of timing I/O circuitry (counter groups A and B).

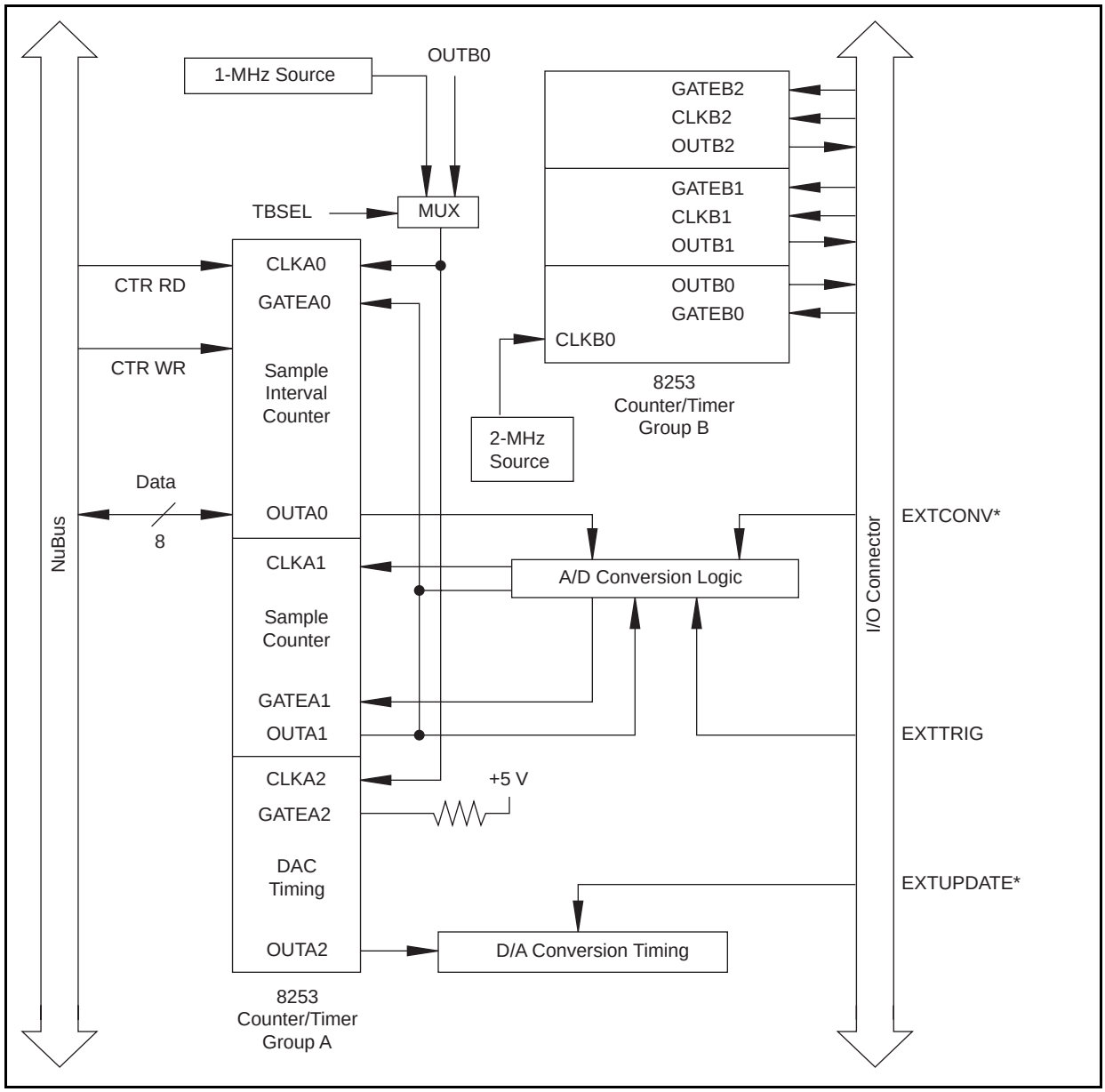


Figure 3-6. Timing I/O Circuitry Block Diagram

Each 8253 contains three independent 16-bit counter/timers and one 8-bit Mode Register. As shown in Figure 3-6, counter group A is reserved for DAQ timing, and counter group B is free for general use. The output of counter B0 can be used in place of the 1-MHz clock source on counter A0 to allow clock periods greater than 65,536 µsec. All six counter/timers can be programmed to operate in several useful timing modes. The programming and operation of the 8253 is presented in detail both in Chapter 4, *Register-Level Programming*, and in Appendix C, *AMD 8253 Data Sheet*.

The 8253 for counter group A uses either a 1-MHz clock generated from the NuBus clock or the output from counter B0, which has a 2-MHz clock source, for its timebase. The timebases for counters B1 and B2 must be supplied externally through the 50-pin I/O connector. The 16-bit counters in the 8253 can be diagrammed as shown in Figure 3-7.

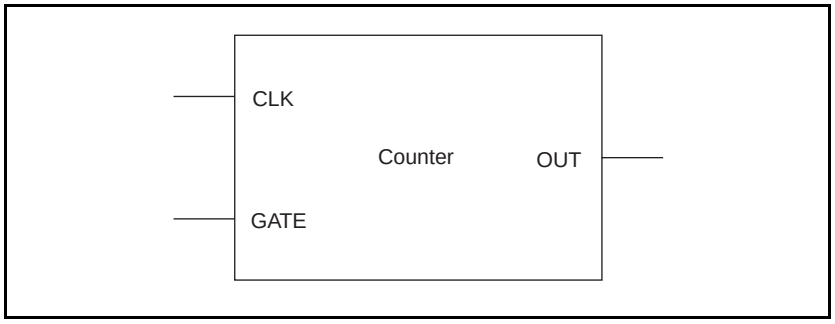


Figure 3-7. Counter Block Diagram

Each counter has a CLK input pin, a GATE input pin, and an output pin labeled OUT. The 8253 counters are numbered 0 through 2, and their GATE, CLK, and OUT pins are labeled GATE *N*, CLK *N*, and OUT *N*, where *N* is the counter number.

Chapter 4
Register-Level Programming

This chapter describes in detail the address and function of each of the Lab-NB control and status registers. This chapter also includes important information about register-level programming the Lab-NB.

Note: ***If you plan to use a programming software package such as NI-DAQ or LabVIEW with your Lab-NB board, you need not read this chapter.***

Register Access

The Macintosh uses memory mapping to access boards in the system. The following sections discuss how to access the various registers on the Lab-NB.

Slot Address Space

Each slot in the Macintosh computer is allocated a block of Macintosh memory addresses known as the *slot address space*. All I/O boards plugged into Macintosh slots are therefore memory mapped, and when a board is plugged into a given slot, its registers can be accessed within that slot address space. The block of memory addresses allocated to each slot depends on the slot number. The slots are labeled 1 through 6 next to the slot connectors inside the Macintosh II, IIx, and IIfx. Table 4-1 shows the slot address space for each slot.

Table 4-1. Macintosh Slot Addresses

Slot Number	Starting Address (Hex)	Ending Address (Hex)
24-Bit Mode		
9	0090 0000	009F FFFF
A	00A0 0000	00AF FFFF
B	00B0 0000	00BF FFFF
C	00C0 0000	00CF FFFF
D	00D0 0000	00DF FFFF
E	00E0 0000	00EF FFFF
32-Bit Mode		
0	F000 0000	F0FF FFFF
1	F100 0000	F1FF FFFF
2	F200 0000	F2FF FFFF
3	F300 0000	F3FF FFFF
4	F400 0000	F4FF FFFF
5	F500 0000	F5FF FFFF
6	F600 0000	F6FF FFFF
7	F700 0000	F7FF FFFF
8	F800 0000	F8FF FFFF
9	F900 0000	F9FF FFFF
A	FA00 0000	FAFF FFFF
B	FB00 0000	FBFF FFFF
C	FC00 0000	FCFF FFFF
D	FD00 0000	FDFF FFFF
E	FE00 0000	FEFF FFFF

Register Map

The register map for the Lab-NB is given in Table 4-2. This table gives the register name, the register address offset from the board's base address, the type of the register (read only, write only, or read and write), and the size of the register in bits.

The register addresses in Table 4-2 are the offset addresses from the slot starting address. To calculate the absolute address of the register, add the slot starting address given in Table 4-1 to the register offset given in Table 4-2. For example, if the Lab-NB is plugged into the third slot (corresponding to slot starting address B0 0000), the ADC FIFO memory is at address B0 0000 + 0 8010, that is, address B0 8010.

Table 4-2. Lab-NB Register Map

Register Name	Offset Address (Hex)	Type	Size
Analog Input Register Group			
A/D Configuration Register	0 8000	Write-only	16-bit
Status Register	0 8000	Read-only	8-bit
A/D FIFO Register	0 8010	Read-only	16-bit
A/D Clear Register	0 8010	Write-only	8-bit
Analog Output Register Group			
DAC Configuration Register	5 8000	Write-only	8-bit
DAC0 Data Register	5 8010	Write-only	16-bit
DAC1 Data Register	5 8020	Write-only	16-bit
DAC0 and DAC1 Data Registers	5 8030	Write-only	16-bit
8253 Counter/Timer Register Group A			
Counter A0 Data Register	4 0000	Read-and-write	8-bit
Counter A1 Data Register	4 0010	Read-and-write	8-bit
Counter A2 Data Register	4 0020	Read-and-write	8-bit
Counter A Mode Register	4 0030	Write-only	8-bit
8253 Counter/Timer Register Group B			
Counter B0 Data Register	4 8000	Read-and-write	8-bit
Counter B1 Data Register	4 8010	Read-and-write	8-bit
Counter B2 Data Register	4 8020	Read- and-write	8-bit
Counter B Mode Register	4 8030	Write-only	8-bit
82C55A Digital I/O Register Group			
Port A Register	5 0000	Read-and-write	8-bit
Port B Register	5 0010	Read-and-write	8-bit
Port C Register	5 0020	Read-and-write	8-bit
Digital Control Register	5 0030	Write-only	8-bit
Interrupt Control Register Group			
Interrupt Control Register	1 0000	Write-only	8-bit
Interrupt Status Register	1 0000	Read-only	8-bit
Timer Interrupt Clear Register	1 8000	Write-only	8-bit

Register Sizes

The Macintosh permits three different memory word sizes for memory read and write operations–byte (8-bit), half-word (16-bit), and word (32-bit). Table 4-2 shows the word sizes of the Lab-NB registers. For example, reading the A/D FIFO Register requires a 16-bit read operation at the specified address.

Register Descriptions

Table 4-2 divides the Lab-NB registers into six different register groups. A bit description of each of the registers making up these groups is included later in this chapter.

The Analog Input Register Group is used to read output from the 12-bit successive-approximation ADC. The Analog Output Group accesses the two 12-bit DACs. The two Counter/Timer Groups (A and B) are each made up of four registers—one group for each of the two onboard 8253 Counter/Timer integrated circuits. The Digital I/O Register Group consists of the four registers of the onboard 82C55A PPI integrated circuit used for digital I/O. The Interrupt Control Register Group can be used to enable the interrupt facility on the Lab-NB board.

Warning: ***During programming, note that each time a port is configured, output ports A and C are reset to 0, and output port B is undefined.***

Register Description Format

The remainder of this register description chapter discusses each of the Lab-NB registers in the order shown in Table 4-2. Each register group is introduced, followed by a detailed bit description of each register. The individual register description gives the address, type, word size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the MSB (bit 15 for a 16-bit register, bit 7 for an 8-bit register) shown on the left, and the LSB (bit 0) shown on the right. A square is used to represent each bit. Each bit is labeled with a name inside its square. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic).

In many of the registers, several bits are labeled with an X, indicating *don't care bits*. When a register is read, these bits may appear set or cleared but should be ignored because they have no significance. When a register is written to, setting or clearing these bit locations has no effect on the Lab-NB hardware.

The bit map field for some write-only registers states *not applicable, no bits used*. Writing to these registers causes some event to occur on the Lab-NB, such as clearing the analog input circuitry. The data is ignored when writing to these registers; therefore, any bit pattern will suffice.

Analog Input Register Group

The four registers making up the Analog Input Register Group control the analog input circuitry and are used for reading from the A/D FIFO. The A/D Configuration Register selects the input channel to be read, the gain for that channel, and some information about the input data. The Status Register reports the status of the current A/D conversion and returns any errors found. Reading the A/D FIFO Register returns stored A/D conversion results. Writing to this register resets the error bits in the Status Register and empties the A/D FIFO. One garbage data byte is stored in the FIFO as a result of the clear operation, so the FIFO must be read after an A/D clear to remove this data byte before starting a new conversion.

Bit descriptions for the registers in the Analog Input Register Group are given on the following pages.

A/D Configuration Register

The A/D Configuration Register indicates the input channel to be read and the gain for the analog input circuitry.

Address: Base address + 0 8000 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	TBSEL	EXTTRIGEN	PRETRIG

7	6	5	4	3	2	1	0
SCANEN	MA2	MA1	MA0	GAIN2	GAIN1	GAIN0	TWOSCMP

Bit	Name	Description
15–11	X	Don't care bits.
10	TBSEL	Clock Select Bit—This bit is used to select the clock source for A/D conversions. If this bit is cleared, an internal 1-MHz clock drives the counter (counter A0), and the interval between samples is the value loaded into counter A0 multiplied by 1 µsec. If this bit is set, then the output of user-programmable counter B0 is used as a clock source. The timebase for counter B0 is fixed at 2 MHz and cannot be changed. The interval between acquired samples is the value loaded into counter A0 multiplied by the period of the output signal from counter B0.
9	EXTTRIGEN	External Trigger Enable Bit—This bit is one of two bits that determines the effect of the EXTTRIG signal on the 50-pin I/O connector. The function of this bit depends on the setting of the PRETRIG bit. If PRETRIG is set, then this bit has no effect in either setting. If PRETRIG is cleared and EXTRIGEN is set, then a rising edge on the EXTTRIG signal starts a sequence of A/D conversions. Unlike the EXTCONV* line, which controls individual conversions, EXTTRIG in this case can only start a multiple A/D conversion DAQ operation with the sample period determined by the value in counter A0. If both EXTTRIGEN and PRETRIG are cleared, then the EXTTRIG line on the I/O connector has no effect.

Bit	Name	Description (continued)
8	PRETRIG	Pretrigger Bit—This bit is used to set the pretriggering feature on the Lab-NB. It also supersedes any setting in the EXTTRIGEN bit described earlier. If PRETRIG is cleared, then the function of the EXTTRIG line on the I/O connector is determined by EXTTRIGEN. If PRETRIG is set, then the EXTTRIG line becomes a pretrigger. In pretrigger operation, the sample counter (counter A1) does not begin decrementing until a rising edge is detected on EXTTRIG. When the conversion sequence terminates, some of the acquired data has been received before the trigger signal and some has arrived after the signal. The number of samples after the trigger is the value loaded into the sample counter (counter A1), but the number of samples before the trigger depends on the arrival time of the trigger signal.
7	SCANEN	Scan Enable Bit—This bit enables or disables multichannel scanning during data acquisition. If this bit is set, analog channels MA<2..0> through 0 are sampled alternately. If this bit is cleared, a single analog channel specified by MA<2..0> is sampled during the entire DAQ operation. See *Programming Multiple A/D Conversions with Channel Scanning* later in this chapter for the correct sequence involved in setting this bit. For example, if MA<2..0> is 011 and SCANEN is set, analog input channels 3 through 0 are sampled alternately during subsequent data conversions. If SCANEN is then cleared (with MA<2..0> still set to 011), only analog input channel 3 is sampled during the subsequent data conversions.
6–4	MA<2..0>	Multiplexer Address Bit—These three bits select which of the eight input channels are read. The analog input multiplexer depends on these three bits to select the input channel. The input channel is selected as follows:

MA<2..0>	Selected Channel
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

If SCANEN is set, analog channels MA<2..0> through 0 are sampled alternately. If SCANEN is cleared, a single analog channel specified by MA<2..0> is sampled during the entire DAQ operation. See *Programming Multiple A/D Conversions with*

Bit	Name	Description (continued)
		Channel Scanning later in this chapter for the correct sequence involved in setting the SCANEN bit.
3–1	GAIN<2..0>	Gain Bit—These three bits select the gain setting as follows:

GAIN<2..0>	Selected Gain
000	1
001	1.25
010	2
011	5
100	10
101	20
110	50
111	100

0	TWOSCMP	Two's Complement Bit—This bit selects the format of the coding of the output of the ADC. If this bit is set, the 12-bit data from the ADC is sign-extended to 16 bits. If this bit is cleared, bits <15..12> return 0.

Status Register

The Status Register indicates the status of the current A/D conversion. The bits in this register determine if a conversion is being performed or if data is available and any errors have been found.

Address: Base address + 0 8000 (hex)

Type: Read-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	GATA1	OVERRUN	OVERFLOW	GATA0	DAVAIL

Bit	Name	Description
7–5	X	Don't care bits.
4	GATA1	Gate 1 Input Status Bit—This bit indicates the status of the GATE 1 input on the counter/timer chip (counter group A).
3	OVERRUN	Overrun Error Status Bit—This bit indicates if an overrun error has occurred. If this bit is cleared, no error occurred. This bit is set if a convert command is issued to the ADC while the last conversion is still in progress.
2	OVERFLOW	Overflow Error Status Bit—This bit indicates if an overflow error has occurred. If this bit is cleared, no error was encountered. If this bit is set, the A/D FIFO has overflowed because the DAQ servicing operation could not keep up with the sampling rate.
1	GATA0	Gate 0 Input Status Bit—This bit indicates the status of the GATE 0 input on the counter/timer chip (counter group A). This bit can be used as a busy indicator for DAQ operations because conversions are enabled as long as GATE 0 is high and counter A0 is programmed appropriately.
0	DAVAIL	Data Available Bit—This bit indicates whether conversion output is available. If this bit is set, the ADC is finished with the last conversion and the result can be read from the FIFO. This bit is cleared if the FIFO is empty.

A/D FIFO Register

Reading the A/D FIFO Register returns the next A/D conversion value stored in the A/D FIFO. Whenever the A/D FIFO Register is read, the value read is removed from the A/D FIFO, thereby freeing space for another A/D conversion value to be stored. Values are stored into the A/D FIFO Register by the ADC whenever an A/D conversion is complete. Although A/D conversion values are in 12-bit format, they are automatically sign-extended to 16 bits in the FIFO.

The A/D FIFO is emptied when all values it contains are read. The Status Register should be read before the A/D FIFO Register is read. If the A/D FIFO contains one or more A/D conversion values, the DAVAIL bit is set in the Status Register, and the A/D FIFO Register can be read to retrieve a value. If the DAVAIL bit is cleared, the A/D FIFO is empty, in which case reading the A/D FIFO Register returns meaningless information.

The values returned by reading the A/D FIFO Register are available in two different binary formats: straight binary or two's complement binary. The binary format used is selected by the TWOSCMP bit in the A/D Configuration Register. The bit pattern returned for either format is given below.

Address: Base address + 0 8010 (hex)

Type: Read-only

Word Size: 16-bit

Bit Map: Straight binary mode

15	14	13	12	11	10	9	8
0	0	0	0	D11	D10	D9	D8

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
15–0	D<15..0>	Data Bit—These bits contain the straight binary result of a 12-bit A/D conversion. Bits D<15..12> are always 0 in straight binary mode. Values read, therefore, range from 0 to +4,095 decimal (0000 to 0FFF hex). Straight binary mode is useful for unipolar analog input readings because all values read reflect a positive polarity input signal.

A/D FIFO Register (continued)

Bit Map: Two’s complement binary mode

15	14	13	12	11	10	9	8
Sign Extension Bits				D11	D10	D9	D8

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
15– 0	D<15..0>	Data Bit—These bits contain the 16-bit, sign-extended two's complement result of a 12-bit A/D conversion. Values read, therefore, range from -2,048 to +2,047 decimal (F800 to 07FF hex). Two’s complement mode is useful for bipolar analog input readings because the values read reflect the polarity of the input signal.

A/D Clear Register

The ADC can be reset by writing to this register. This operation clears the FIFO and loads the last conversion value into the FIFO. All error bits in the Status Register are cleared as well. Notice that the FIFO contains one data word after reset, so a FIFO read is necessary after reset to empty the FIFO. The data that is read should be ignored.

Address: Base address + 0 8010 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map: Not applicable, no bits used

Analog Output Register Group

The four registers making up the Analog Output Register Group are used for loading the two 12-bit DACs in the two analog output channels. DAC0 controls analog output channel 0. DAC1 controls analog output channel 1. These DACs can be written to individually or simultaneously.

Bit descriptions of the registers making up the Analog Output Register Group are given on the following pages.

DAC Configuration Register

This register determines if data written to the DACs is in straight binary or two's complement form. It also configures the DACs to output data automatically at a rate controlled by counter A2 OR EXTUPDATE*. This feature is particularly useful for automatic waveform generation.

Address: Base address + 5 8000 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	X	TMRWGN1	TMRWGN0	TWOSDA1	TWOSDA0

Bit	Name	Description
7–4	X	Don't care bits.
3	TMRWGN1	Timer Waveform Generation Enable Bit for DAC1—This bit is used to enable timer waveform generation from DAC1. If this bit is set, DAC1 updates its output at regular intervals as determined by counter A2 or the EXTUPDATE* signal at the I/O connector. If this bit is cleared, then the voltage output of DAC1 is updated as soon as the data is loaded into its data register.
2	TMRWGN0	Timer Waveform Generation Enable Bit for DAC0—This bit is used to enable timer waveform generation from DAC0. If this bit is set, DAC0 updates its output at regular intervals as determined by counter A2 or the EXTUPDATE* signal at the I/O connector. If this bit is cleared, then the voltage output of DAC0 is updated as soon as the data is loaded into its data register.
1	TWOSDA1	Binary Coding Scheme Select Bit for DAC1—This bit selects the binary coding scheme used for the DAC1 data. If this bit is set, a two's complement binary coding scheme is used for interpreting the 12-bit data. Two's complement is useful if a bipolar output range is selected. If this bit is cleared, a straight binary coding scheme is used. Straight binary is useful if a unipolar output range is selected.
0	TWOSDA0	Binary Coding Scheme Select Bit for DAC0—This bit selects the binary coding scheme used for the DAC0 data. If this bit is set, a two's complement binary coding scheme is used for interpreting the 12-bit data. Two's complement is useful if a bipolar output range is selected. If this bit is cleared, a straight binary coding scheme is used. Straight binary is useful if a unipolar output range is selected.

DAC0 and DAC1 Data Registers

Writing to these registers loads the corresponding analog output channel DAC, thereby updating the voltages generated by the analog output channels. The voltage is updated immediately, unless the TMRWGN bit for that DAC is set. If this bit is set, then the voltages are not updated until the next pulse from counter A2 or the next low-to-high transition on the EXTUPDATE* line on the I/O connector. If the timer interrupt enable bit (TMRINTEN) in the Interrupt Status Register is set, then a write to any one of these registers will service that interrupt and clear TMRINTEN.

Address: Base address + 5 8010 (hex) Load DAC0.
Base address + 5 8020 (hex) Load DAC1.
Base address + 5 8030 (hex) Load DAC0 and DAC1 simultaneously.

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	D11	D10	D9	D8

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
15–12	X	Don’t care bits.
11–0	D<11..0>	Data Bit—These 12 bits are loaded into the specified DAC, thereby updating the voltage generated by the analog output channel (see *Programming the Analog Output Circuitry* later in this chapter for a table mapping digital values to output voltage).

8253 Counter/Timer Register Groups

The eight registers making up the two Counter/Timer Register Groups access the two onboard 8253 Counter/Timers. Each 8253 has three counters. For convenience, the two Counter/Timer Groups and their respective 8253 integrated circuits have been designated A and B. The three counters of group A control onboard DAQ timing and waveform generation. The three counters of group B are available for general-purpose timing functions.

Each 8253 has three independent 16-bit counters and one 8-bit Mode Register. The Mode Register is used to set the mode of operation for each of the three counters.

Bit descriptions for the registers in the Counter/Timer Register Groups are given in the following pages.

Counter A0 Data Register

The Counter A0 Data Register is used for loading and reading back contents of 8253(A) counter 0.

Address: Base address + 4 0000 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data Bit—8-bit counter A0 contents.

Counter A1 Data Register

The Counter A1 Data Register is used for loading and reading back contents of 8253(A) counter 1.

Address: Base address + 4 0010 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data Bit—8-bit counter A1 contents.

Counter A2 Data Register

The Counter A2 Data Register is used for loading and reading back contents of 8253(A) counter A2.

Address: Base address + 4 0020 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data Bit—8-bit counter A2 contents.

Counter A Mode Register

The Counter A Mode Register determines the operation mode for each of the three counters on the 8253(A) chip. The Counter A Mode Register selects the counter involved, its read/load mode, its operation mode (that is, any of the 8253's six operation modes), and the counting mode (binary or BCD counting).

The Counter A Mode Register is an 8-bit register. Bit descriptions for each of these bits are given in Appendix C, *AMD 8253 Data Sheet.*

Address: Base address + 4 0030 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Counter B0 Data Register

The Counter B0 Data Register is used for loading and reading back the contents of 8253(B) counter 0.

Address: Base address + 4 8000 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data Bit—8-bit counter B0 contents.

Counter B1 Data Register

The Counter B1 Data Register is used for loading and reading back the contents of 8253(B) counter 1.

Address: Base address + 4 8010 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data Bit—8-bit counter B1 contents.

Counter B2 Data Register

The Counter B2 Data Register is used for loading and reading back the contents of 8253(B) counter 2.

Address: Base address + 4 8020 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data Bit—8-bit counter B2 contents.

Counter B Mode Register

The Counter B Mode Register determines the operation mode for each of the three counters on the 8253(B) chip. The Counter B Mode Register selects the counter involved, its read/load mode, its operation mode (that is, any of the 8253's six operation modes), and the counting mode (binary or BCD counting).

The Counter Mode Register is an 8-bit register. Bit descriptions for each of these bits are given in Appendix C, *AMD 8253 Data Sheet*.

Address: Base address + 4 8030 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

82C55A Digital I/O Register Group

Digital I/O on the Lab-NB uses an 82C55A integrated circuit. The 82C55A is a general-purpose PPI containing 24 programmable I/O pins. These pins represent the three 8-bit I/O ports (A, B, and C) of the 82C55A. These ports can be programmed as two groups of 12 signals or as three individual 8-bit ports.

The Digital I/O Register Group contains the following four registers: Port A Register, Port B Register, Port C Register, and Digital Control Register. Bit descriptions for the registers in the Digital I/O Register Group are given on the following pages.

Port A Register

Reading the Port A Register returns the logic state of the eight digital I/O lines constituting port A, that is, PA<0..7>. If port A is configured for output, the Port A Register can be written to in order to control the eight digital I/O lines constituting port A. See *Programming the Digital I/O Circuitry* later in this chapter for information on how to configure port A for input or output.

Address: Slot starting address + 5 0000 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data Bit—8-bit port A data.

Port B Register

Reading the Port B Register returns the logic state of the eight digital I/O lines constituting port B, that is, PB<0..7>. If port B is configured for output, the Port B Register can be written to in order to control the eight digital I/O lines constituting port B. See *Programming the Digital I/O Circuitry* later in this chapter for information on how to configure port B for input or output.

Address: Slot starting address + 5 0010 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data Bit—8-bit port B data.

Port C Register

Port C is special in the sense that it can be used as an 8-bit I/O port like port A and port B if neither port A nor port B is used in handshaking (latched) mode. If either port A or port B is configured for latched I/O, some of the bits in port C are used for handshaking signals. See *Programming the Digital I/O Circuitry* later in this chapter for a description of the individual bits in the Port C Register.

Address: Slot starting address + 5 0020 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data Bit—8-bit port C data.

Digital Control Register

The Digital Control Register can be used to configure port A, port B, and port C as inputs or outputs as well as selecting simple mode (basic I/O) or handshaking mode (strobed I/O) for transfers. See *Programming the Digital I/O Circuitry* later in this chapter for a description of the individual bits in the Digital Control Register.

Address: Slot starting address + 5 0030 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
CW7	CW6	CW5	CW4	CW3	CW2	CW1	CW0

Bit	Name	Description
7–0	CW<7..0>	Control Word Bit—8-bit control word.

Interrupt Control Register Group

This group is made up of two registers. Writing to the Interrupt Control Register enables the interrupt facility on the Lab-NB. The Interrupt Status Register contains information about the Interrupt Control Register and the interrupt line.

Bit descriptions of the registers making up the Interrupt Control Group are given on the following pages.

Interrupt Control Register

Setting bits of this register causes an interrupt to occur when the current process is complete.

Address: Base address + 1 0000 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	X	PAINTEN	PBINTEN	TMRINTEN	ADCINTEN

Bit	Name	Description
7–4	X	Don't care bits.
3	PAINTEN	Port A Interrupt Enable Bit—This bit enables or disables generation of an interrupt via PC3. If port A on the Lab-NB is operated in latched mode, PC3 becomes INTRA, that is, Interrupt Request for port A. If this bit is set and port A is configured as an *input* port in latched mode, an interrupt is generated whenever new data has been strobed in and is ready to be read from port A. If this bit is set and port A is configured as an *output* port in latched mode, an interrupt is generated whenever new data can be written to port A; that is, the receiving device has acknowledged the previous data by driving ACKA* (acknowledge input for port A) low. If this bit is cleared, interrupts from PC3 are disabled. See Appendix D, *OKI 82C55A Data Sheet*, for timing details.
2	PBINTEN	Port B Interrupt Enable Bit—This bit enables or disables generation of an interrupt via PC0. If port B on the Lab-NB is operated in latched mode, PC0 becomes INTRB, that is, Interrupt Request for port B. If this bit is set and port B is configured as an *input* port in latched mode, an interrupt is generated whenever new data has been strobed in and is ready to be read from port B. If this bit is set and port B is configured as an *output* port in latched mode, an interrupt is generated whenever new data can be written to port B; that is, the receiving device has acknowledged the previous data by driving ACKB* (acknowledge input for port B) low. If this bit is cleared, interrupts from PC0 are disabled. See Appendix D, *OKI 82C55A Data Sheet*, for timing details.
1	TMRINTEN	Timer Interrupt Enable Bit—This bit enables interrupts to be caused by the counter A2 output and the EXTUPDATE* signal. If this bit is set, an interrupt occurs when either EXTUPDATE* or counter A2 output makes a low-to-high transition. The interrupt is cleared by writing either to any of the DAC output registers or to

Bit	Name	Description (continued)
		the Timer Interrupt Clear Register. This interrupt allows waveform generation on the analog output because the same signal that sets the interrupt also updates the DAC output if the corresponding TMRWG bit in the DAC Configuration Register is set. If this bit is cleared, interrupts from EXTUPDATE* and counter A2 output are ignored.
0	ADCINTEN	A/D Conversion Interrupt Enable Bit—This bit enables or disables generation of an interrupt at the end of an A/D conversion using the 12-bit ADC. A DAQ operation is a multiple A/D conversion sequence that is timed and controlled by the Lab-NB onboard counter/timers. Whether the operation is a single or multiple conversion, if this bit is set, an interrupt is generated whenever the A/D FIFO contains conversion data, that is, when the A/D FIFO is not empty. If this bit is cleared, interrupts from the A/D FIFO are disabled.

Interrupt Status Register

The Interrupt Status Register indicates the status of the Interrupt Control Register bits and the interrupt lines.

Address: Base address + 1 0000 (hex)

Type: Read-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	INT	TIMERUP	*PAINTEN	*PBINTEN	*TMRINTEN	*ADCINTEN

Bit	Name	Description
7, 6	X	Don’t care bits.
5	INT	Interrupt Bit—This bit shows the overall state of interrupts generated by the Lab-NB board. If this bit is set, the Lab-NB is asserting an interrupt that has not yet been serviced. If this bit is cleared, no interrupt is pending. This bit is normally cleared. As explained in the description of the Interrupt Control Register earlier in this chapter, there are four possible sources for an interrupt.
4	TIMERUP	TMRINTEN Interrupt Status Bit—This bit indicates the status of the TMRINTEN interrupt. If this bit is set and TMRINTEN has been set, the current interrupt is due to a rising edge on EXTUPDATE* or counter A2's output. TIMERUP is cleared by writing to the Timer Interrupt Clear Register or writing to either DAC0 or DAC1. TIMERUP is set whenever a rising edge on counter A2’s output or EXTUPDATE* is detected. TIMERUP generates an interrupt request if it is set and the TMRINTEN bit is set in the Interrupt Control Register.
3	*PAINTEN	Port A Interrupt Enable—This bit indicates the status of the PAINTEN bit in the Interrupt Control Register. Notice that the polarity is reversed in the Interrupt Status Register.
2	*PBINTEN	Port B Interrupt Enable—This bit indicates the status of the PBINTEN bit in the Interrupt Control Register. Notice that the polarity is reversed in the Interrupt Status Register.
1	*TMRINTEN	Active Low TMRINTEN Interrupt Status Bit—This bit indicates the status of the TMRINTEN bit in the Interrupt Control Register. Notice that the polarity is reversed in the Interrupt Status Register.
0	*ADCINTEN	ADCINTEN Status Bit—This bit indicates the status of the ADCINTEN bit in the Interrupt Control Register. Notice that the polarity is reversed in the Interrupt Status Register.

Timer Interrupt Clear Register

Writing to the Timer Interrupt Clear Register clears the TIMERUP bit in the Interrupt Status Register. The Timer Interrupt Clear Register can be used to service any timer-related or EXTUPDATE*-caused interrupts generated by the Lab-NB. This register provides an alternate means of clearing timer-generated interrupts besides writing to one or both of the DACs.

Address: Base address + 1 8000 (hex)

Type: Read-only

Word Size: 8-bit

Bit Map: Not applicable, no bits used

Configuration EPROM

The Configuration EPROM is an onboard read-only memory that contains information required by the Macintosh operating system. The Macintosh system Slot Manager reads the Configuration EPROM upon system startup.

The Configuration EPROM is mapped to address offset locations F 8000 through F FFFC. The EPROM is 8 bits (1 byte) wide and 8 kilobytes in length. Each byte of the EPROM is mapped to every fourth address location on the Lab-NB board as follows: the first byte is read from slot address + F 8000; the second byte is read from slot address + F 8004; the third byte is read from slot address + F 8008, and so on.

Programming Considerations

The following paragraphs contain programming instructions for operating the circuitry on the Lab-NB board. Programming the Lab-NB involves writing to and reading from the various registers on the board. The programming instructions included here list the sequence of steps to take. The instructions are language independent; that is, they tell you to write a value to a given register, to set or clear a bit in a given register, or to detect whether a given bit is set or cleared without presenting the actual code.

Register Programming Considerations

Registers in the Macintosh are memory mapped; that is, writing to a register involves storing a value in a memory location. A register is read by reading this memory location. Only memory location reads and writes can be performed on the Lab-NB registers. Mathematical or logical operations *cannot* be directly applied to the Lab-NB registers. Attempting to do so results in unpredictable program behavior.

Several write-only registers on the Lab-NB contain bits that control several independent pieces of the onboard circuitry. In the set or clear instructions provided, specific register bits should be set or cleared without changing the current state of the remaining bits in the register. However, writing to these registers affects all register bits simultaneously. You cannot read these registers to determine which bits have been set or cleared in the past; therefore, you should maintain a software copy of the write-only registers. This software copy can then be read to determine the status of the write-only registers. To change the state of a single bit without disturbing the remaining bits, set or clear the bit in the software copy and then write the software copy to the register.

Initializing the Lab-NB Board

The Lab-NB hardware must be initialized for the Lab-NB circuitry to operate properly. To initialize the Lab-NB hardware, complete these steps:

1. Write 38 (hex) to the Counter A Mode Register (8-bit write).
2. Write 78 (hex) to Counter A Mode Register (8-bit write).
3. Write 00 (hex) to the Interrupt Control Register (8-bit write).

4. Write 0000 (hex) to the A/D Configuration Register (16-bit write).
5. Write 00 (hex) to the A/D Clear Register (8-bit write).
6. Read the data from the A/D FIFO Register (16-bit read). Ignore the data.
7. Write 0000 (hex) to the DAC0 Data Register if DAC0 is configured for unipolar output.
   Write 0800 (hex) to the DAC0 Data Register if DAC0 is configured for bipolar output.
8. Write 0000 (hex) to the DAC1 Data Register if DAC1 is configured for unipolar output.
   Write 0800 (hex) to the DAC1 Data Register if DAC1 is configured for bipolar output.

This sequence leaves the Lab-NB circuitry in the following state:

- Counter A0 output is high. Low-going pulses on counter 0 initiate conversions.
- Counter A1 output is high. This disables EXTCONV*.
- All interrupts are disabled.
- EXTTRIG is disabled.
- The timebase for counter A0 is the onboard 1-MHz source.
- Analog input circuitry is initialized to a gain of 1 and channel 0 selected.
- The A/D FIFO is cleared.
- The D/A Configuration Register is initialized to 00 (hex) on power up. Thus, straight binary coding is selected for both DACs.
- The analog output circuitry is initialized to 0.0 V on both channels.

For additional details concerning the 8253 Counter/Timer, see Appendix C, *AMD 8253 Data Sheet*. For information about the 82C55A PPI, see Appendix D, *OKI 82C55A Data Sheet*.

Programming the Analog Input Circuitry

This section describes the analog input circuitry programming sequence, how to program the binary mode of the A/D conversion result, and how to clear the analog input circuitry.

Analog Input Circuitry Programming Sequence

Programming the analog input circuitry for a single A/D conversion involves the following sequence of steps:

1. Select analog input channel and gain.
2. Initiate an A/D conversion.
3. Read the A/D conversion result.

Each of these steps is discussed in detail as follows.

1. Select analog input channel and gain.

The analog input channel and gain are selected by writing to the A/D Configuration Register. See the A/D Configuration Register bit description earlier in this chapter for gain and analog input channel bit patterns. Set up the bits as given in the A/D Configuration Register bit description, and write to the A/D Configuration Register.

The A/D Configuration Register needs to be written to only when the analog input channel, gain setting, input mode (unipolar/bipolar), scanning mode, or interrupt enable bits need to be changed.

2. Initiate an A/D conversion.

An A/D conversion can be initiated by a high-to-low transition on the counter A0 output (OUTA0). Alternatively, a conversion can be performed by forcing a high-to-low transition on EXTCONV*. To perform a single conversion with the onboard counters, use the following programming sequence. All values are given in hexadecimal.

1. Write 38 to the Counter A Mode Register (8-bit write). This causes OUTA0 to be set high.

2. Write 30 to the Counter A Mode Register (8-bit write). This causes OUTA0 to be set low.

3. Write 38 to the Counter A0 Data Register (8-bit write). This causes OUTA0 to be set high.

Once an A/D conversion is initiated, the ADC stores the result in the A/D FIFO at the end of its conversion cycle or after a rising edge on OUTA0, whichever occurs later. In case of EXTCONV* initiating the conversion, OUTA0 and OUTA1 must both be set high.

3. Read the A/D conversion result.

A/D conversion results are obtained by reading the A/D FIFO Register. Before you read the A/D FIFO, however, you must read the Status Register to determine whether the A/D FIFO contains any results.

To read the A/D conversion results, complete these steps:

1. Read the A/D Status Register (8-bit read).

2. If the DAVAIL bit is set (bit 0), then read the A/D FIFO Register to obtain the result.

Reading the A/D FIFO Register removes the A/D conversion result from the A/D FIFO. The binary modes of the A/D FIFO output are explained later.

The DAVAIL bit indicates whether one or more A/D conversion results are stored in the A/D FIFO. If the DAVAIL bit is cleared, the A/D FIFO is empty and reading the A/D FIFO Register returns meaningless data. Once an A/D conversion is initiated, the DAVAIL bit should be set after 12 µsec or after a rising edge on OUTA0, whichever occurs later. If EXTCONV* is being

used for A/D timing, the DAVAIL bit should be set after 12 msec or after a rising edge in EXTCONV*, whichever occurs later.

An A/D FIFO overflow condition occurs if more than 16 conversions are initiated and stored in the A/D FIFO before the A/D FIFO Register is read. If this condition occurs, the OVERFLOW bit is set in the Status Register to indicate that one or more A/D conversion results have been lost because of FIFO overflow. Writing to the A/D Clear Register resets this error flag. A dummy read must be performed on the FIFO after an A/D Clear to reset the FIFO.

A/D FIFO Output Binary Modes

The A/D conversion result can be returned from the A/D FIFO as a 16-bit two's complement or straight binary value by setting or clearing the TWOSCMP bit in the A/D Configuration Register. If the analog input circuitry is configured for the input range 0 to +10 V, straight binary mode should be used (clear the TWOSCMP bit). Straight binary mode returns numbers between 0 and +4,095 (decimal) when the A/D FIFO Register is read. If the analog input circuitry is configured for the input range -5 to +5 V, two’s complement mode is more appropriate (set the TWOSCMP bit). Two's complement mode returns numbers between -2,048 and +2,047 (decimal) when the A/D FIFO Register is read.

Table 4-3 shows input voltage versus A/D conversion values for the 0 to +10 V input range. Table 4-4 shows input voltage versus A/D conversion values for two's complement mode and -5 to +5 V input range.

Table 4-3. Unipolar Input Mode A/D Conversion Values (Straight Binary Coding)

Input Voltage (Gain = 1)	**A/D Conversion Result Range: 0 to +10 V**	
	(Decimal)	**(Hex)**
0	0 0000	
2.5	1,024	0400
5.0	2,048	0800
7.5	3,072	0C00
9.9976	4,095	0FFF

Table 4-4. Bipolar Input Mode A/D Conversion Values (Two’s Complement Coding)

Input Voltage (Gain = 1)	**A/D Conversion Result Range: -5 to +5 V**	
	(Decimal)	**(Hex)**
-5.0	-2,048	F800
-2.5	-1,024	FC00
0	0 0000	
2.5	1,024	0400
4.9976	2,047	07FF

Clearing the Analog Input Circuitry

The analog input circuitry can be cleared by writing to the A/D Clear Register, which leaves the analog input circuitry in the following state:

- Analog input error flags OVERFLOW and OVERRUN are cleared.
- Pending interrupt requests are cleared.
- A/D FIFO has one garbage word of data.

Empty the A/D FIFO before starting any A/D conversions by performing a read on the A/D FIFO Register and ignoring the data read. This operation guarantees that the A/D conversion results read from the A/D FIFO are the results from the initiated conversions rather than leftover results from previous conversions.

To clear the analog input circuitry and the A/D FIFO, complete these steps:

- Write 0 to the A/D Clear Register (8-bit write).
- Read the A/D FIFO Register and ignore the data (16-bit read).

Programming Multiple A/D Conversions on a Single Input Channel

A sequence of timed A/D conversions is referred to in this manual as a *DAQ operation*. Two types of DAQ operations are available on the Lab-NB:

- Controlled acquisition mode
- Freerun acquisition mode

In controlled acquisition mode, two counters (counters A0 and A1) are required for a DAQ operation. Counter A0 is used as a sample-interval counter, while counter A1 is used as a sample counter. In this mode, a specified number of conversions is performed, after which the hardware shuts off the conversions. Counter A0 generates the conversion pulses, and counter A1 gates off counter A0 after the programmed count has expired. The number of conversions in a single DAQ operation in this case is limited to a 16-bit count (or 65,535).

In freerun acquisition mode, only one counter is required for a DAQ operation. Counter A0 continuously generates the conversion pulses as long as GATEA0 is held at a high logic level. The software keeps track of the number of conversions that has occurred and turns off counter A0 after the required number of conversions has been obtained. The number of conversions in a single DAQ operation in this case is unlimited. Counter A0 is clocked by a 1-MHz clock on start up.

Alternatively, a programmable timebase for counter A0 is available through the use of counter B0. If the TBSEL bit in the ADC Configuration Register is set, then the timebase for counter A0 is counter B0. Counter B0 has a fixed, unalterable 2-MHz clock as its own timebase, so its period is the value stored in it multiplied by 500 nsec. The minimum period that can be selected for counter B0 is 1 µsec. The period of counter A0, or the sample period, is then equal to the period of counter B0 multiplied by the value stored in counter A0. Regardless of the timebase chosen, the minimum sample period of 16 µsec must be observed for data integrity.

Programming in Controlled Acquisition Mode

The following programming steps are required for a DAQ operation in controlled acquisition mode:

1. Select analog input channel, gain, and timebase source for counter A0.
2. Program counter B0 (if necessary).
3. Program counters A0 and A1.
4. Clear the A/D circuitry.
5. Program the sample-interval counter (counter A0).
6. Service the DAQ operation.

Each of these programming steps is explained below.

1. Select analog input channel, gain, and timebase source for counter A0.

The analog input channel and gain are selected by writing to the A/D Configuration Register. The SCANEN bit must be cleared for DAQ operations on a single channel. See the A/D Configuration Register bit description earlier in this chapter for gain and analog input channel bit patterns. If counter B0 is being used as a timebase for counter A0, then the TBSEL bit in the ADC Configuration Register should be set at this time.

The A/D Configuration Register needs to be written to only when the analog input channel, gain setting, or other function needs to be changed.

2. Program counter B0 (if necessary).

The following sequence should be used to program counter B0 if it is being used. If counter B0 is not being used, skip to step 3. All writes are 8-bit write operations. All values given are hexadecimal.

a. Write 36 to the Counter B Mode Register (select mode 3).

b. Write the least significant byte of the timebase count to the Counter B Data Register.

c. Write the most significant byte of the timebase count to the Counter B Data Register. For example, programming a timebase of 10 µsec requires a timebase count of

$$\frac{10\ \mu\text{sec}}{0.5\ \mu\text{sec}} = 20\ \mu\text{sec}$$

3. Program counters A0 and A1.

This step involves programming counter A0 to generate periodic conversion pulses and programming counter A1 to interrupt on terminal count mode (mode 0).

Counter A0 of the 8253(A) Counter/Timer is used as the sample-interval counter. A high-to-low transition on the counter A0 output initiates a conversion. Counter A0 can be programmed to generate a pulse once every *N* µsec. *N* is referred to as the sample interval, that is, the time between successive A/D conversions. *N* can be between 2 and 65,535. The sample interval is equal to the period of the timebase clock used by counter A0 multiplied by *N*. Two timebases are available: a 1-MHz clock and the output of counter B0.

Counter A1 of the 8253(A) Counter/Timer is used as a sample counter. The sample counter tallies the number of A/D conversions initiated by counter A0 and stops counter A0 when the desired sample count is reached. The sample count must be less than or equal to 65,535. The minimum sample count is 2.

Write 34 (hex) to the Counter A Mode Register (select counter A0, mode 2) to force OUT0 to a high state prior to clearing the A/D FIFO. This is an 8-bit write operation.

Use the following sequence to program the sample counter:

a. Write 70 to the Counter A Mode Register (select counter A1, mode 0).

b. Write the least significant byte of *M*-1, where *M* is the sample count, to the counter A1 Data Register.

c. Write the most significant byte of *M*-1, where *M* is the sample count, to the counter A1 Data Register.

After you complete this programming sequence, counter A1 is configured to count A/D conversion pulses and counter A0 output is in a high state.

4. Clear the A/D circuitry.

Before the DAQ operation is started, the A/D FIFO must be emptied in order to clear out any old A/D conversion results. Empty the A/D FIFO *after* the counters are programmed because programming the counters can cause spurious edges. Write 0 to the A/D Clear Register to empty the FIFO (8-bit write), followed by a read from the A/D FIFO (16-bit read). Ignore the data obtained in the read.

5. Program the sample-interval counter (counter A0).

This step involves programming counter A0 (the sample-interval counter) in rate generator mode (mode 2).

Use the following programming sequence to program the sample-interval counter. All writes are 8-bit write operations. All values given are hexadecimal.

a. Write 34 to the Counter A Mode Register (select counter A0, mode 2).

b. Write the least significant byte of the sample interval to the Counter A0 Data Register.

c. Write the most significant byte of the sample interval to the Counter A0 Data Register.

6. Service the DAQ operation.

Once the DAQ operation is started by writing the most significant byte of the sample interval to the Counter A0 Data Register, the operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To do this, perform the following sequence until the desired number of conversion results has been read:

a. Read the Status Register (8-bit read).

b. If the DAVAIL bit is set (bit 0), then read the A/D FIFO Register to obtain the result.

Interrupts can also be used to service the DAQ operation. This topic is discussed later in this chapter.

Two error conditions may occur during a DAQ operation: an overflow error or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the DAVAIL bit.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is cleared.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is low. The minimum recommended sampling interval on the Lab-NB is 16 µsec.

Both the OVERFLOW and OVERRUN bits in the Status Register are reset by writing to the A/D Clear Register.

Programming in Freerun Acquisition Mode

Freerun acquisition mode uses only counter A0 as the sample-interval counter. The number of A/D conversions that have occurred (that is, the sample count) is maintained by software in this case. With this arrangement, DAQ operations can acquire more than 65,535 samples.

The following programming steps are required for a DAQ operation in freerun acquisition mode:

1. Select analog input channel, gain, and timebase for counter A0.
2. Program counter B0 (if necessary).
3. Program counter A0 to force OUT0 high.
4. Clear the A/D circuitry.
5. Program counter A1 to force OUT1 low.
6. Program the sample-interval counter (counter A0).
7. Service the DAQ operation.

Each of these programming steps is explained below.

1. Select analog input channel, gain, and timebase for counter A0.

The analog input channel and gain are selected by writing to the A/D Configuration Register. The SCANEN bit must be cleared for DAQ operations on a single channel. See the A/D Configuration Register bit description earlier in this chapter for gain and analog input channel bit patterns. If counter B0 is being used as a timebase for counter A0, then the TBSEL bit in the ADC Configuration Register should be set at this time.

The A/D Configuration Register needs to be written to only when the analog input channel, gain setting, or other function needs to be changed.

2. Program counter B0 (if necessary).

The following sequence should be used to program counter B0 if it is being used. If counter B0 is not being used, skip to step 3. All writes are 8-bit write operations. All values given are hexadecimal.

a. Write 36 to the Counter B Mode Register (select mode 3).

b. Write the least significant byte of the timebase count to the Counter B Data Register.

c. Write the most significant byte of the timebase count to the Counter B Data Register. For example, programming a timebase of 10 µsec requires a timebase count of

$$\frac{10\ \mu\text{sec}}{0.5\ \mu\text{sec}} = 20\ \mu\text{sec}$$

3. Program counter A0 to force OUT0 high.

Counter A0 of the 8253(A) Counter/Timer is used as the sample-interval counter. A high-to-low transition on OUT0 (counter A0 output) initiates a conversion. Counter A0 can be programmed to generate a pulse once every *N* µsec. *N* is referred to as the sample interval, that is, the time between successive A/D conversions. *N* can be between 2 and 65,535. The sample interval is equal to the period of the timebase clock used by counter A0 multiplied by *N*. A 1-MHz clock is internally connected to CLK0 (the clock used by counter A0).

Write 34 (hex) to the Counter A Mode Register (select counter A0, mode 2) to force OUT0 to a high state prior to clearing the A/D FIFO. This is an 8-bit write operation.

4. Clear the A/D circuitry.

Before you start the DAQ operation, the A/D FIFO must be emptied in order to clear out any old A/D conversion results. Empty the A/D FIFO *after* the counters are programmed because programming the counters can cause spurious edges. Write 0 to the A/D Clear Register to empty the FIFO (8-bit write), followed by a read from the A/D FIFO (8-bit read). Ignore the data obtained in the read.

5. Program counter A1 to force OUT1 low.

Counter A1 must be programmed so that OUT1 is at logic low state.

a. Write 70 (hex) to the Counter A Mode Register. This forces OUT1 low.

6. Program the sample-interval counter (counter A0).

Use the following programming sequence to program counter A0, the sample-interval counter. All writes are 8-bit write operations. All values given are hexadecimal.

a. Write 34 to the Counter A Mode Register (select counter A0, mode 2).

b. Write the least significant byte of the sample interval to the Counter A0 Data Register.

c. Write the most significant byte of the sample interval to the Counter A0 Data Register.

7. Service the DAQ operation.

Once the DAQ operation is started by writing the most significant byte of the sample interval to the Counter A0 Data Register, the operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To do this, perform the following sequence until the desired number of conversion results has been read:

a. Read the Status Register (8-bit read).

b. If the DAVAIL bit is set (bit 0), then read the A/D FIFO Register to obtain the result.

Interrupts can also be used to service the DAQ operation. This topic is discussed later in this chapter.

Two error conditions may occur during a DAQ operation: an overflow error or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the DAVAIL bit.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is set.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is set. The minimum recommended sampling interval on the Lab-NB is 16 µsec.

Both the OVERFLOW and OVERRUN bits in the Status Register are cleared by writing to the A/D Clear Register.

External Timing Considerations for Multiple A/D Conversions

Two external timing signals, EXTTRIG and EXTCONV*, can be used for multiple A/D conversions. EXTTRIG can be used to initiate a conversion sequence (posttrigger mode) or to terminate an ongoing conversion sequence (pretrigger mode), and the EXTCONV* signal can be used to time the individual A/D conversions from an external timing source. Chapter 2, *Configuration and Installation*, contains the EXTTRIG and EXTCONV* signal specifications. The posttrigger and pretrigger modes are described later in this chapter.

Using the EXTTRIG Signal to Initiate a Multiple A/D Conversion DAQ Operation (Posttrigger Mode)

If the PRETRIG bit is cleared and the EXTTRIGEN bit is set in the ADC Command Register, EXTTRIG functions as a start trigger for a multiple A/D conversion DAQ operation. In this mode, referred to as *posttriggering*, the sample-interval counter is gated off until a low-to-high edge is sensed on EXTTRIG. No samples are collected until EXTTRIG makes its low-to-high transition. Transitions on the EXTCONV* line are also ignored until a low-to-high edge is sensed on the EXTRIG followed by a low-to-high edge on EXTCONV* input.

Using the EXTTRIG Signal to Terminate a Multiple A/D Conversion DAQ Operation (Pretrigger Mode)

If the PRETRIG bit is set in the ADC Command Register, EXTTRIG functions as a stop trigger for a multiple A/D conversion DAQ operation. In this mode, referred to as *pretriggering*, the sample counter is gated off until a low-to-high edge is sensed on EXTTRIG. Pretriggering is performed in a manner similar to external triggering. With pretriggering, counter A0 (the sample-interval counter) starts as soon as the last byte is loaded. However, counter A1, the sample counter, does not start counting until the first rising edge on EXTTRIG. In this way, data is collected before the actual trigger rising edge. After the rising edge occurs, the number of points specified in counter A1 are collected and the acquisition stops. You must allocate sufficient array space for all of the data, and specify both the number of points and the indeterminate number of points that may be collected before the pretrigger signal arrives. Alternatively, a *circular buffer* can be set up by the acquisition software so that data is repeatedly loaded into the same section of memory. Although this method does not require an indeterminate amount of memory, you can examine only samples acquired during a limited time period before and after the trigger occurs. Pretriggering is set up by setting PRETRIG in the ADC Configuration Register. PRETRIG supersedes EXTTRIGEN; if both bits are set, then pretriggering is enabled.

Using the EXTCONV* Signal to Initiate A/D Conversions

As mentioned earlier, A/D conversions can be initiated by a falling edge on either OUTA0 or EXTCONV*. Setting the GATA0 bit low disables conversions from both OUTA0 and EXTCONV*. Setting the GATA0 bit high enables conversions from both OUTA0 and EXTCONV*. The GATA0 bit is set low whenever OUTA1 is high. If OUTA1 is low, GATA0 can be set high at any time by either setting the PRETRIG bit or initiating a rising edge on EXTRIG if the EXTRIGEN bit in the ADC Command Register is set.

Programming Multiple A/D Conversions Using External Timing

A DAQ operation using the external timing signals EXTCONV* or EXTTRIG can be in either controlled acquisition mode or freerun acquisition mode. In controlled acquisition mode, counter A1 shuts off A/D conversions after the programmed count expires. In freerun acquisition mode, A/D conversions are disabled under software control.

Programming in Controlled Acquisition Mode

Posttrigger Mode

The following programming steps are required for a DAQ operation in controlled acquisition mode using EXTCONV*. In the following programming sequence, EXTTRIG is used as a posttrigger signal; that is, data acquisition is not started until a rising edge is detected on the EXTTRIG input.

1. Disable EXTCONV* and EXTTRIG input.
2. Select analog input channel and gain and select posttrigger mode.
3. Program counter A0.

4. Clear the A/D circuitry.
5. Program counter A1 and enable EXTCONV* and EXTTRIG input.
6. Service the DAQ operation.

Each of these programming steps is explained as follows.

1. Disable EXTCONV* and EXTTRIG input.

The EXTCONV* bit can be disabled by setting the GATA0 bit low. The GATA0 bit is low whenever OUTA1 is high, regardless of the settings for the PRETRIG or EXTTRIGEN bits in the ADC Configuration Register or the EXTTRIG signal. Writing 78 (hex) to the Counter A Mode Register sets OUTA1 high. This write disables EXTCONV* and EXTTRIG input; that is, any transitions on these two inputs are ignored.

2. Select analog input channel and gain and select posttrigger mode.

The analog input channel and gain are selected by writing to the A/D Configuration Register. The SCANEN bit must be cleared for DAQ operations on a single channel. See the A/D Configuration Register bit description earlier in this chapter for gain and analog input channel bit descriptions. The PRETRIG bit must be cleared and the EXTRIGEN bit must be set high during this write to the A/D Configuration Register. These settings select posttrigger mode.

3. Program counter A0.

Since a high-to-low transition on the counter A0 output initiates an A/D conversion, counter A0 output must be programmed to a high state. This ensures that counter A0 does not cause any A/D conversions.

Write 34 (hex) to the Counter A Mode Register (select counter A0, mode 2) to force OUTA0 to a high state. This is an 8-bit operation.

4. Clear the A/D circuitry.

Before the DAQ operation is started, the A/D FIFO must be emptied in order to clear any old A/D conversion results. Empty the A/D FIFO *after* the counters are programmed because programming the counters can cause spurious edges. Write 0 to the A/D Clear Register to empty the FIFO (8-bit write) and read from the A/D FIFO (16-bit read). Ignore the data obtained while reading the A/D Clear Register.

5. Program counter A1 and enable EXTCONV* and EXTTRIG input.

Counter A1 of the 8253(A) Counter/Timer is used as a sample counter. The sample counter counts the number of A/D conversions and disables conversions when the programmed count is reached. The sample count must be less than or equal to 65,535. The minimum sample count is 2. EXTTRIG is enabled as soon as counter A1 is programmed.

To program the counters, use the following programming sequence:

a. Write 70 (hex) to the Counter A Mode Register (select counter A1, mode 0). This step sets the output of counter A1 (OUTA1) low, which in turn enables EXTTRIG; that is, the first rising edge on EXTTRIG after OUTA1 goes low starts the DAQ sequence.

b. Write the least significant byte of (*M*-1), where *M* is the sample count, to the Counter A1 Data Register.

c. Write the most significant byte of (*M*-1), where *M* is the sample count, to the Counter A1 Data Register.

After completing this programming sequence, counter A1 is configured to count A/D conversion pulses and EXTTRIG input is enabled.

6. Service the DAQ operation.

Once the DAQ operation is started by a rising edge on the EXTTRIG input, A/D conversions are initiated by falling edges on the EXTCONV* input. The operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To service the DAQ, perform the following sequence until the desired number of conversion results has been read:

a. Read the Status Register (8-bit read).

b. If the DAVAIL bit is set (bit 0), read the A/D FIFO Register to obtain the result.

Interrupts can also be used to service the DAQ operation. Interrupts are discussed later in this chapter.

Two error conditions may occur during a DAQ operation: an overflow error or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the DAVAIL bit.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is cleared.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is low. The minimum recommended sampling interval on the Lab-NB is 16 µsec.

Both the OVERFLOW and OVERRUN bits in the Status Register are reset by writing to the A/D Clear Register.

Pretrigger Mode

The following programming steps are required for a DAQ operation in controlled acquisition mode using EXTCONV*. In the following programming sequence, EXTTRIG is used as a pretrigger signal; that is, A/D conversions are enabled but the sample count is not started until a rising edge is detected on the EXTTRIG input. Data acquisition remains enabled for the programmed count after the rising edge on the EXTTRIG input. Thus, data can be acquired before and after the trigger (EXTTRIG).

1. Disable EXTCONV* and EXTTRIG input.
2. Select analog input channel and gain and select pretrigger mode.
3. Program counter A0.
4. Clear the A/D circuitry.
5. Program counter A1 and enable EXTCONV* and EXTTRIG input.
6. Service the DAQ operation.

Each of these programming steps is explained as follows.

1. Disable EXTCONV* and EXTTRIG input.

The EXTCONV* input can be disabled by setting the GATA0 bit low. The GATA0 bit is low whenever OUTA1 is high, regardless of the settings for the PRETRIG or EXTTRIGEN bits in the ADC Configuration Register or the EXTTRIG signal. Writing 78 (hex) to the counter A Mode Register sets OUTA1 high. This write disables EXTCONV* and EXTTRIG input; that is, any transitions on these two inputs are ignored.

2. Select analog input channel and gain and select pretrigger mode.

The analog input channel and gain are selected by writing to the A/D Configuration Register. The SCANEN bit must be cleared for DAQ operations on a single channel. See the A/D Configuration Register bit description earlier in this chapter for gain and analog input channel bit descriptions. The PRETRIG bit must be set high and the EXTRIGEN bit must be set low during this write to the A/D Configuration Register. These settings select pretrigger mode.

3. Program counter A0.

Since a high-to-low transition on the counter A0 output initiates an A/D conversion, counter A0 output must be programmed to a high state. This ensures that counter A0 does not cause any A/D conversions.

Write 34 (hex) to the Counter A Mode Register (select counter A0, mode 2) to force OUTA0 to a high state. This is an 8-bit operation.

4. Clear the A/D circuitry.

Before the DAQ operation is started, the A/D FIFO must be emptied in order to clear any old A/D conversion results. Empty the A/D FIFO *after* the counters are programmed because programming the counters can cause spurious edges. Write 0 to the A/D Clear Register to empty the FIFO (8-bit write) and to read from the A/D FIFO (16-bit read). Ignore the data obtained while reading the A/D Clear Register. In pretrigger mode, a write to the A/D Clear Register also sets the GATA1 bit low. A/D conversions are not counted until GATA1 is set high by a rising edge on the EXTTRIG input.

5. Program counter A1 and enable EXTCONV* input.

Counter A1 of the 8253(A) Counter/Timer is used as a sample counter. The sample counter counts the number of A/D conversions and disables conversions when the programmed count is reached. The sample count must be less than or equal to 65,535. The minimum sample count is 2. EXTCONV* is enabled as soon as counter A1 is programmed.

To program the counters, use the following programming sequence.

a. Write 70 (hex) to the Counter A Mode Register (select counter A1, mode 0). This step sets the output of counter A1 (OUTA1) low, which in turn, enables EXTCONV*; that is, falling edges on EXTCONV* initiate A/D conversions.

b. Write the least significant byte of (*M*-1), where *M* is the sample count after the trigger to the Counter A1 Data Register.

c. Write the most significant byte of (*M*-1), where *M* is the sample count after the trigger to the Counter A1 Data Register.

After you complete this programming sequence, counter A1 is configured to count A/D conversion pulses and EXTTRIG input is enabled. A/D conversions are initiated by falling edges on EXTCONV* input, but the sample counter (counter A1) is not gated on until a rising edge on the EXTTRIG input. After a rising edge on the EXTTRIG input is sensed, A/D conversions remain enabled for the programmed count after which GATA1 is set low and EXTCONV* input is disabled.

6. Service the DAQ operation.

Once the DAQ operation is enabled in step 5, A/D conversions are initiated by the falling edges on the EXTCONV* input. The operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To service the data acquisition, perform the following sequence until the GATA0 bit in the Status Register is set low:

a. Read the Status Register (8-bit read).

b. If the DAVAIL bit is set (bit 0), read the A/D FIFO Register to obtain the result.

Interrupts can also be used to service the DAQ operation. Interrupts are discussed later in this chapter.

Two error conditions may occur during a DAQ operation: an overflow error or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the DAVAIL bit.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is cleared.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is low. The minimum recommended sampling interval on the Lab-NB is 16 µsec.

Both the OVERFLOW and OVERRUN bits in the Status Register are reset by writing to the A/D Clear Register.

Programming in Freerun Acquisition Mode

Posttrigger Mode

A posttrigger data acquisition in freerun acquisition mode using EXTCONV* requires a programming sequence similar to controlled acquisition mode, except that steps 5c and 5d are not performed. The sample count is kept in software and conversions remain enabled until GATA0 is set high. GATA0 can be set low by writing 34 (hex) to the Counter A Mode Register after the required number of samples is obtained. This disables EXTCONV*, that is, further transitions on EXTCONV* are ignored.

Pretrigger Mode

Pretriggering mode requires that the A/D conversions be shut off at a programmed time by the hardware after the trigger on EXTTRIG. Therefore, pretriggered data acquisition is not possible in freerun acquisition mode.

Programming Multiple A/D Conversions with Channel Scanning

The data acquisition programming sequences given earlier in this chapter are for programming the Lab-NB for multiple A/D conversions on a single input channel. The Lab-NB can also be programmed for scanning analog input channels during the DAQ operation. Analog channels *N* through 0 can be scanned, where *N* can be 1 through 7. Programming scanned multiple A/D conversions involves the same sequence of steps as single-channel DAQ operations except that the SCANEN bit is set in the A/D Configuration Register. When the SCANEN bit is set in the A/D Configuration Register, the analog channel select bits MA<2..0> specify the highest numbered channel in the scan sequence. For example, if MA<2..0> is 011 (binary)–that is, channel 3 is selected and the SCANEN bit is set—the following scan sequence is used:

channel 3, channel 2, channel 1, channel 0, channel 3, channel 2, channel 1, channel 0, channel 3, and so on.

Note: ***Select the analog input channel and gain in the following order:***

1. ***Write the configuration value indicating the highest channel number in the scan sequence, the gain, and the input polarity to the A/D Configuration Register. The SCANEN bit must be cleared during this first write to the A/D Configuration Register.***
2. ***Write the same configuration value again to the A/D Configuration Register. The SCANEN bit, however, must be set during the second write to the A/D Configuration Register.***

Scanning can be enabled in either controlled or freerun acquisition mode. Use either counter A0 or EXTCONV* to control the scanning interval.

Interrupt Programming for the Analog Input Circuitry

Use interrupts to service the A/D FIFO during a DAQ operation. To use the conversion interrupt, set the ADCINTEN bit in the Interrupt Control Register. If this bit is set, an interrupt is generated whenever the DAVAIL bit in the Status Register is set. This interrupt condition is cleared when the A/D FIFO is emptied by reading its contents.

Programming the Analog Output Circuitry

The analog output circuitry on the Lab-NB uses double-buffered DACs. Thus, the voltage at the output pins (pins DAC0OUT and DAC1OUT on the Lab-NB I/O connector) does not update immediately with each write to the DAC Data Registers. The analog output can be updated in synchronization with counter A2 output or the external update control signal EXTUPDATE*. This ability is useful for waveform generation applications because the timed update pulses eliminate the timing jitter associated with software writes to the DAC Data Registers.

The voltage at the analog output circuitry pins (pins DAC0OUT and DAC1OUT on the Lab-NB I/O connector) is controlled by loading the DAC in the analog output channel with a 12-bit digital code. The DACs can be loaded by writing the digital code to the DAC0 and DAC1 Data Registers. Writing to the DAC0 Data Register loads DAC0, and writing to the DAC1 Data Register loads DAC1. Writing to the DAC0 and DAC1 Data Registers loads both DAC0 and DAC1 simultaneously with the same digital code. The analog output on pins DAC0OUT or DAC1OUT can be updated in one of three ways: immediately when the DAC0 Data Register or the DAC1 Data Register is written to, when a low level is detected on the EXTUPDATE* pin, or when a low level is detected on counter A's output (OUTA2). The TMRWGN bits in the DAC Configuration Register determine which update method is used. If TMRWGN0 is set high, the analog output from DAC0 is updated when a low level is detected on either EXTUPDATE* or OUTA2. If TMRWGN0 is set low, the analog output from DAC0 is updated as soon as the DAC0 Data Register is written to. TMRWGN1 controls the updating of DAC1 analog output in a similar manner.

The output voltage generated from the digital code depends on the configuration, unipolar or bipolar, of the associated analog output channel. Unipolar or bipolar configuration is determined

by jumper settings described in Chapter 2, *Configuration and Installation*. Table 4-5 shows the output voltage versus digital code for a unipolar analog output configuration. Table 4-6 shows the voltage versus digital code for a bipolar analog output configuration.

The following formula calculates the voltage output versus digital code for a unipolar analog output configuration and straight binary coding:

$$V_{out} = 10.0 * \left(\frac{\text{digital code}}{4,096} \right)$$

The digital code in the preceding formula is a decimal value ranging from 0 to +4,095. Notice that straight binary coding is selected by clearing the TWOSDA bit in the DAC Configuration Register.

Table 4-5. Analog Output Voltage Versus Digital Code
(Unipolar Mode, Straight Binary Coding)

Digital Code		**Voltage Output**
(Decimal)	**(Hex)**	
0	0000	0 V
1	0001	2.4414 mV
2,048	0800	5.0 V
4,095	0FFF	9.9976 V

The following formula calculates the voltage output versus digital code for a bipolar analog output configuration and two's complement coding:

$$V_{out} = 5.0 * \left(\frac{\text{digital code}}{2,048} \right)$$

The digital code in the above formula is a decimal value ranging from -2,048 to +2,047. Notice that two’s complement mode coding is selected by setting the TWOSDA bit high in the DAC Configuration Register.

Table 4-6. Analog Output Voltage Versus Digital Code
(Bipolar Mode, Two's Complement Coding)

Digital Code (Decimal)	Digital Code (Hex)	Voltage Output (V_{ref} = 10 V)
-2,048	F800	-5.0 V
-1,024	FC00	-2.5 V
0	0000	0.0 V
1,024	0400	2.5 V
2,047	07FF	4.9976 V

Interrupt Programming for the Analog Output Circuitry

Interrupts can be used for writing successive values in a sequence to the DAC Data Registers during a waveform generation operation. The TMRINTEN bit in the Interrupt Control Registers enables and disables counter A2 and EXTUPDATE* driven interrupts. See Chapter 2, *Configuration and Installation*, for timing requirements on the EXTUPDATE* signal.

The following programming steps are required for waveform generation using interrupts:

1. Set up the DAC Configuration Register.
2. Program counter A2.
3. Install an interrupt service routine.
4. Enable timer interrupts.

Each of these programming steps is explained below.

1. Set up the DAC Configuration Register.

The TMRWGN0 bit must be set high for enabling OUTA2 or EXTUPDATE* driven updates on DAC0. TMRWGN1 bit must be set high for enabling OUTA2 or EXTUPDATE* driven updates on DAC1.

2. Program counter A2.

If EXTUPDATE* is being used to update the DACs, counter A2 output (OUTA2) must be set high by writing B8(hex) to the Counter A Mode Register. If OUTA2 is being used to update the DACs, EXTUPDATE* must be left unconnected or driven to a TTL-high level. Counter A2 must be programmed in mode 2 with the appropriate update interval.

3. Install an interrupt service routine.

You must install an interrupt service routine for the slot containing the Lab-NB. Consult the *Inside Macintosh* manual for information regarding the installation of interrupt service routines. The interrupt service routine can use the TIMERUP bit in the Interrupt Status Register to determine whether the interrupt was a counter A2 (or EXTUPDATE*) generated interrupt, which is useful when interrupts from other sources such as data acquisition and digital I/O have been enabled on the Lab-NB. The interrupt service routine must write to either the DAC0, DAC1, or DAC0 and DAC1 Data Registers or to TMRINTCLR to reset the TIMERUP bit and acknowledge the current interrupt. Another interrupt is generated when a rising edge (low-to-high) is detected on OUTA2 or EXTUPDATE*.

4. Enable timer interrupts.

Timer interrupts refer to the interrupts generated by rising edges on OUTA2 or EXTUPDATE*. A rising edge on OUTA2 or EXTUPDATE* sets the TIMERUP bit high in the Interrupt Status Register. A timer interrupt is generated whenever the TIMERUP bit in the Interrupt Status Register and the TMRINTEN bit in the Interrupt Control Register are set high. Set the TMRINTEN bit in the Interrupt Control Register high to enable timer interrupts.

Programming the Digital I/O Circuitry

The digital I/O circuitry is designed around an 82C55A integrated circuit. The 82C55A is a general-purpose PPI containing 24 programmable I/O pins. These pins represent the three 8-bit I/O ports (A, B, and C) of the 82C55A. These ports can be programmed as two groups of 12 signals or as three individual 8-bit ports. The following paragraphs include programming information for the Lab-NB along with program examples written in C.

The three 8-bit ports are divided into two groups: group A and group B (two groups of 12 signals). One 8-bit configuration (or control) word specifies the mode of operation for each group. Group A's control bits configure port A (A0 through A7) and the upper 4 bits (nibble) of port C (C4 through C7). Group B's control bits configure port B (B0 through B7) and the lower nibble of port C (C0 through C3). These configuration bits are defined later in this chapter.

82C55A Modes of Operation

The three basic modes of operation for the 82C55A are as follows:

- Mode 0 – Basic I/O
- Mode 1 – Strobed I/O
- Mode 2 – Bidirectional bus

The 82C55A also has a single bit set/reset feature for port C. The 8-bit control word also programs this function. For additional information, refer to Appendix D, *OKI 82C55A Data Sheet*.

Mode 0–Basic I/O

This mode is for simple I/O operations for each of the ports. No handshaking is required; data is simply written to or read from a specified port.

Mode 0 has the following features:

- Two 8-bit ports (A and B) and two 4-bit ports (upper and lower nibble of port C).
- Any port can be input or output.
- Outputs are latched, but inputs are not latched.

Mode 1–Strobed I/O

This mode is used for transferring data with handshake signals. Ports A and B use the eight lines of port C to generate or receive the handshake signals. This mode divides the ports into two groups (group A and group B).

- Each group contains one 8-bit data port (port A or port B) and one 4-bit control/data port (upper or lower nibble of port C).
- The 8-bit data ports can be either input or output, both of which are latched.
- The 4-bit ports are used for control and status of the 8-bit data ports.
- Interrupt generation and enable/disable functions are available.

Mode 2–Bidirectional Bus

This mode is for communication over a bidirectional 8-bit bus. Handshake signals can be used in a manner similar to mode 1. Interrupt generation and enable/disable functions are also available. Other features of this mode include the following:

- Used in group A only (port A and upper nibble of port C).
- One 8-bit bidirectional port (port A) and a 5-bit control status port (port C).
- Both inputs and outputs are latched.

Single Bit Set/Reset Feature

Any of the 8 bits of port C can be set or reset with one control word. This feature is used to generate status and control for port A and port B when operating in mode 1 or mode 2.

Register Descriptions and Programming Examples

The following figures show the two control-word formats used to completely program the 82C55A. The control-word flag determines which control-word format is being programmed. When the control-word flag is 1, bits 0 through 6 specify the I/O characteristics of the 82C55A's ports and the mode in which they are operating (that is, mode 0, mode 1, or mode 2). When the control-word flag is 0, bits 3 through 0 specify the bit set/reset format of port C.

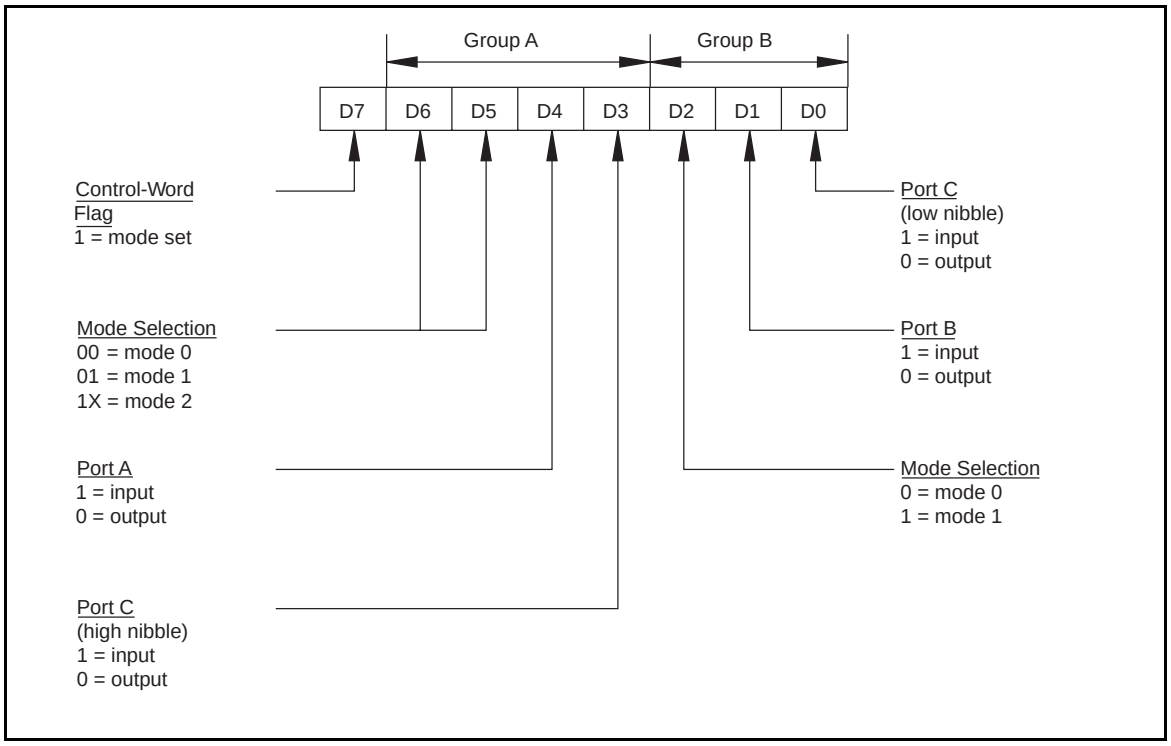


Figure 4-1. Control-Word Format with Control-Word Flag Set to 1

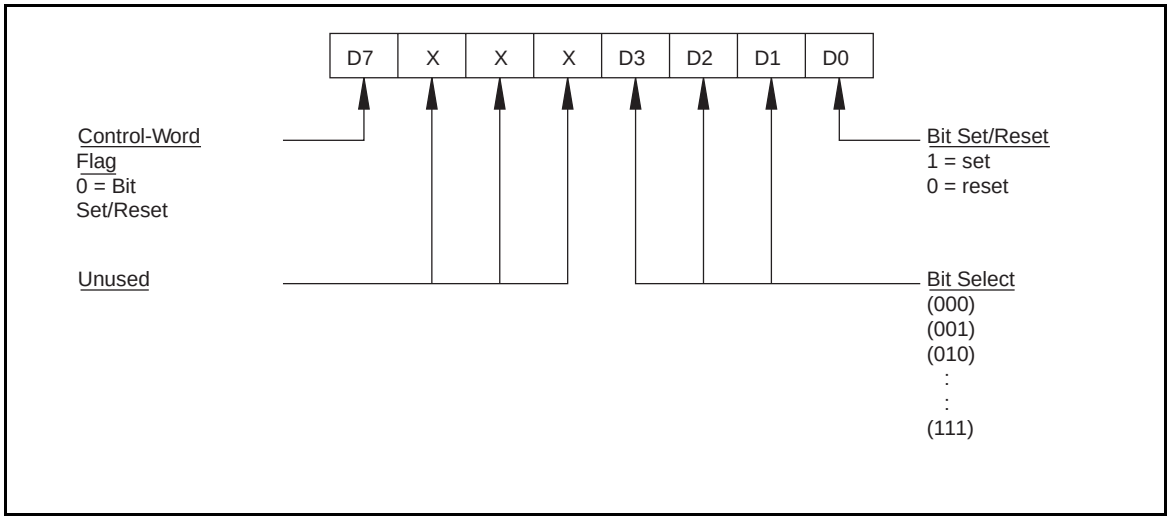


Figure 4-2. Control-Word Format with Control-Word Flag Set to 0

This section describes the Digital Control Register, which is used to program the 82C55A ports in any one of the three modes discussed earlier in this section. Specific control words for each mode are described later in this section along with programming examples for each mode.

Mode 0 Control Words

Mode 0 provides simple I/O functions for each of the three ports with no handshaking. Each port can be assigned as an input port or as an output port. The 16 possible I/O configurations are shown in Table 4-7. Notice that bit 7 of the control word is set when programming the mode of operation for each port.

Table 4-7. Mode 0 I/O Configurations

Control Word	**Group A**		**Group B**	
Bit 76543210	**Port A**	**Port C[1]**	**Port B**	**Port C[2]**
10000000	Output	Output	Output	Output
10000001	Output	Output	Output	Input
10000010	Output	Output	Input	Output
10000011	Output	Output	Input	Input
10001000	Output	Input	Output	Output
10001001	Output	Input	Output	Input
10001010	Output	Input	Input	Output
10001011	Output	Input	Input	Input
10010000	Input	Output	Output	Output
10010001	Input	Output	Output	Input
10010010	Input	Output	Input	Output
10010011	Input	Output	Input	Input
10011000	Input	Input	Output	Output
10011001	Input	Input	Output	Input
10011010	Input	Input	Input	Output
10011011	Input	Input	Input	Input

[1] Upper nibble of port C
[2] Lower nibble of port C

Mode 0 Programming Examples

Example 1. Configure all three ports (A, B, and C) as output ports in mode 0:

- Write 80 (hex) to the Digital Control Register.
- Write 8-bit data to the Port A, Port B, or Port C Register as appropriate.

Example 2. Configure port A for input, port B and port C for output:

- Write 90 (hex) to the Digital Control Register.
- Write 8-bit data to port B or port C. Read 8-bit data from port A as appropriate.

Example 3. Configure port A and port C for output, port B for input:

- Write 82 (hex) to the Digital Control Register.

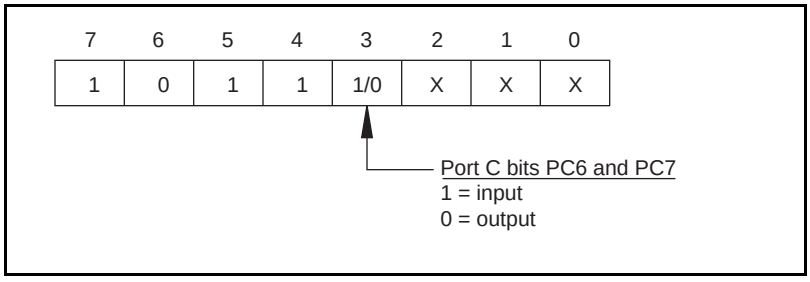
Example 4. Configure port A and port B for output, port C for input:

- Write 89 (hex) to the Digital Control Register.

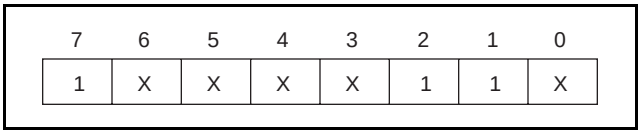
Mode 1 Strobed Input Control Words

In mode 1, the digital I/O bits are divided into two groups: group A and group B. Each of these groups contains one 8-bit port and one 4-bit control/data port. The 8-bit port can be either an input port or an output port, and the 4-bit port is used for control and status information for the 8-bit port. The transfer of data is synchronized by handshaking signals in the 4-bit port.

The control word written to the Digital Control Register to configure port A for input in mode 1 is shown here. Bits PC6 and PC7 of port C can be used as extra input or output lines.



The control word written to the Digital Control Register to configure port B for input in mode 1 is shown here. Notice that port B is not provided with extra input or output lines from port C.



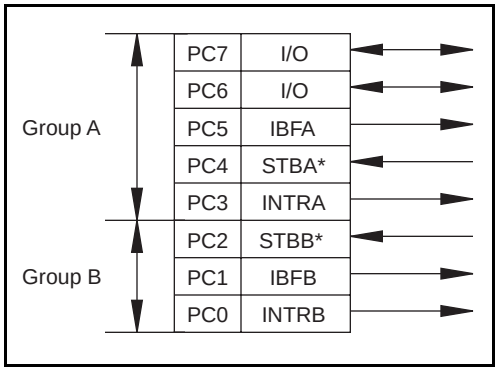
During a mode 1 data read transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The port C status-word bit definitions for an input transfer are shown next.

Port C status-word bit definitions for input (port A and port B):

7	6	5	4	3	2	1	0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB

Bit	Name	Description
7, 6	I/O	Extra I/O status lines when port A is in mode 1 input.
5	IBFA	Input Buffer Full for Port A—High indicates that data has been loaded into the input latch for port A.
4	INTEA	Interrupt Enable Bit for Port A—Enables interrupts from the 82C55A for port A. Controlled by setting or resetting of PC4.
3	INTRA	Interrupt Request Status for Port A—When INTEA is high and IBFA is high, this bit is high, indicating that an interrupt request is asserted.
2	INTEB	Interrupt Enable Bit for Port B—Enables interrupts from the 82C55A for port B. Controlled by setting or resetting PC2.
1	IBFB	Input Buffer Full for Port B—High indicates that data has been loaded into the input latch for port B.
0	INTRB	Interrupt Request Status for Port B—When INTEB is high and IBFB is high, this bit is high, indicating that an interrupt request is asserted.

At the digital I/O connector, port C has the following pin assignments when in mode 1 input. Notice that the status of STBA* and STBB* is not provided in the port C status word.



Mode 1 Input Programming Example

Example 1. Configure port A as an input port in mode 1:

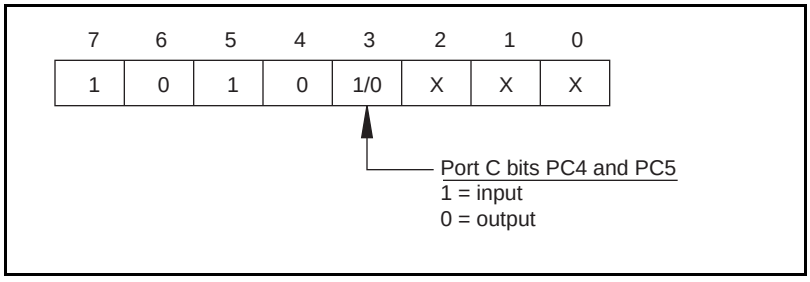
- Write B0 (hex) to the Digital Control Register.
- Wait for bit 5 of port C (IBFA) to be set, indicating that data has been latched into port A.
- Read data from port A.

Example 2. Configure port B as an input port in mode 1:

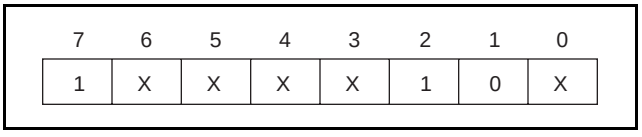
- Write 86 (hex) to the Digital Control Register.
- Wait for bit 1 of port C (IBFB) to be set, indicating that data has been latched into port A.
- Read data from port B.

Mode 1 Strobed Output Control Words

The control word written to the Digital Control Register to configure port A for output in mode 1 is shown here. Bits PC4 and PC5 of port C can be used as extra input or output lines when port A uses mode 1 output.



The control word written to the Digital Control Register to configure port B for output in mode 1 is shown here. Notice that port B is not provided with extra input or output lines from port C.



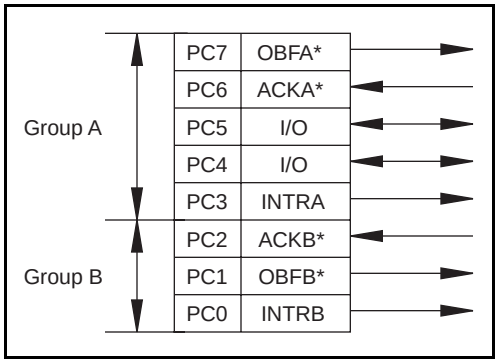
During a mode 1 data write transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. Notice that the bit definitions are different for a write and a read transfer.

Port C status-word bit definitions for output (port A and port B):

7	6	5	4	3	2	1	0
OBFA*	INTEA	I/O	I/O	INTRA	INTEB*	OBFB	INTRB

Bit	Name	Description
7	OBFA*	Output Buffer Full for Port A—Low indicates that the CPU has written data out to port A.
6	INTEA	Interrupt Enable Bit for Port A—If this bit is high, interrupts are enabled from the 82C55A for port A. Controlled by setting or resetting PC6.
5, 4	I/O	Input/Output—Extra I/O status line when port A is in mode 1 output.
3	INTRA	Interrupt Request Status for Port A—When INTEA is high and OBFA* is high, this bit is high, indicating that an interrupt request is asserted.
2	INTEB	Interrupt Enable Bit for Port B—If this bit is high, interrupts are enabled from the 82C55A for port B. Controlled by setting or resetting PC2.
1	OBFB*	Output Buffer Full for Port B—Low indicates that the CPU has written data out to port B.
0	INTRB	Interrupt Request Status for Port B—When INTEB is high and OBFB* is high, this bit is high, indicating that an interrupt request is asserted.

At the digital I/O connector, port C has the following pin assignments when in mode 1 output. Notice that the status of ACKA* and ACKB* is not provided when port C is read.



Mode 1 Output Programming Example

Example 1. Configure port A as an output port in mode 1:

- Write A0 (hex) to the Digital Control Register.
- Wait for bit 7 of port C (OBFA*) to be cleared, indicating that the data last written to port A has been read.
- Write new data to port A.

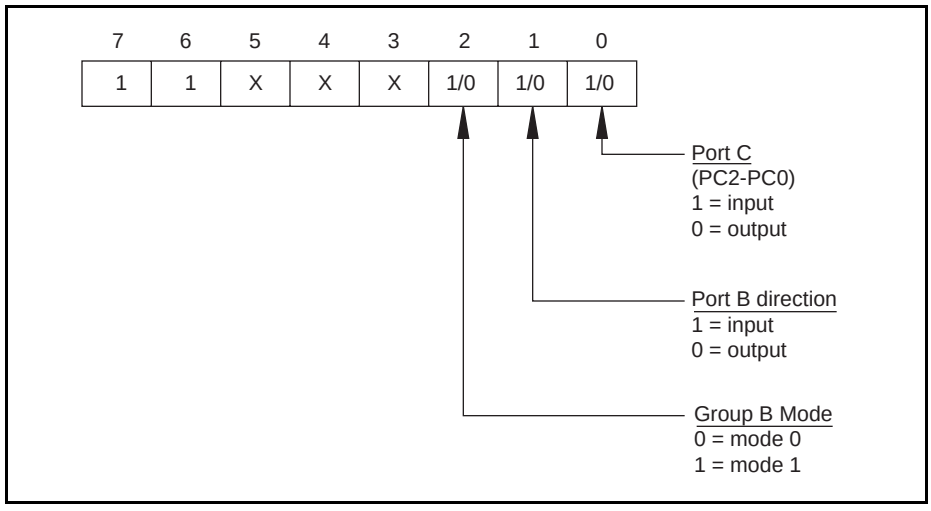
Example 2. Configure port B as an output port in mode 1:

- Write 84 (hex) to the Digital Control Register.
- Wait for bit 1 of port C (OBFB*) to be cleared, indicating that the data last written to port B has been read.
- Write new data to port A.

Mode 2 Control Words

In mode 2, an 8-bit bus can be used for both input and output transfers without changing the configuration. The data transfers are synchronized with handshaking lines in port C. This mode uses only port A; however, port B can be used in either mode 0 or mode 1 while port A is configured for mode 2.

The control word written to the Digital Control Register to configure port A as a bidirectional data bus in mode 2 is shown below. Because mode 2 is for port A only, port B can be programmed to operate in mode 0 or mode 1. If port B is configured for mode 0, then PC2, PC1, and PC0 of port C can be used as extra input or output lines.



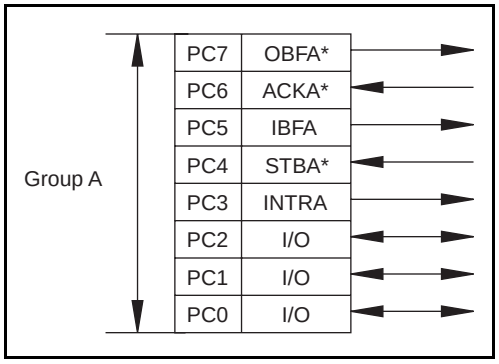
During a mode 2 data transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The port C status-word bit definitions for a mode 2 transfer are shown next.

Port C status-word bit definitions for bidirectional data path (port A only):

7	6	5	4	3	2	1	0
OBFA*	INTE1	IBFA	INTE2	INTRA	I/O	I/O	I/O

Bit	Name	Description
7	OBFA*	Output Buffer Full—Low indicates that the CPU has written data out to port A.
6	INTE1	Interrupt Enable Bit for Output—If this bit is set, interrupts are enabled from the 82C55A for OBF*. Controlled by setting or resetting PC6.
5	IBFA	Input Buffer Full—High indicates that data has been loaded into the input latch of port A.
4	INTE2	Interrupt Enable Bit for Input—If this bit is set, interrupts are enabled from the 82C55A for IBF. Controlled by setting or resetting PC4.
3	INTRA	Interrupt Request Status—If INTE1 is high and IBFA is high, this bit is high, indicating that an interrupt request is asserted for input transfers. If INTE2 is high and OBFA* is high, this bit is high, indicating that an interrupt request is asserted for output transfers.
2–0	I/O	Input/Output—Extra I/O status lines available if port B is not configured for mode 1.

At the digital I/O connector, port C has the following pin assignments when in mode 2.



Mode 2 Programming Example

Example 1. Configure port A in mode 2:

- Write C0 (hex) to the Digital Control Register.
- Wait for bit 7 of port C (OBFA*) to be cleared, indicating that the data last written to port A has been read.
- Write new data to port A.
- Wait for bit 5 of port C (IBFA) to be set, indicating that data is available in port A to be read.
- Read data from port A.

Single Bit Set/Reset Control Words

Table 4-8 shows the control words for setting or resetting each bit in port C. Notice that bit 7 of the control word is cleared for programming the set/reset option for the bits of port C.

Table 4-8. Port C Set/Reset Control Words

Bit Set Control Word	Bit Reset Control Word	The Bit Set or Reset in Port C
0xxx0001	0xxx0000	xxxxxxxn
0xxx0011	0xxx0010	xxxxxxnx
0xxx0101	0xxx0100	xxxxxnxx
0xxx0111	0xxx0110	xxxxnxxx
0xxx1001	0xxx1000	xxxnxxxx
0xxx1011	0xxx1010	xxnxxxxx
0xxx1101	0xxx1100	xnxxxxxx
0xxx1111	0xxx1110	nxxxxxxx

Interrupt Programming for the Digital I/O Circuitry

Interrupts can be enabled on PC0, PC3, or both PC0 and PC3 via the Interrupt Control Register. See the Interrupt Control Register description earlier in this chapter for corresponding bit positions.

An external signal can be used to generate an interrupt when port A or B is in mode 0. Program PC0 or PC3 for input and connect the external signal that should trigger an interrupt to PC0 or PC3. When the external signal becomes logic high, an interrupt request occurs. To negate the interrupt request, the external signal must become logic low.

Chapter 5
Calibration

This chapter discusses the calibration procedures for the Lab-NB analog input and analog output circuitry.

The Lab-NB is calibrated at the factory before shipment. To maintain the 12-bit accuracy of the Lab-NB analog input and analog output circuitry, recalibration at six-month intervals is recommended. Recalibration is also recommended whenever the input or output configuration is changed.

Factory calibration is performed with the Lab-NB in its default factory configuration:

- ±5 V analog input range (bipolar)
- ±5 V analog output range (bipolar)

Calibration Equipment Requirements

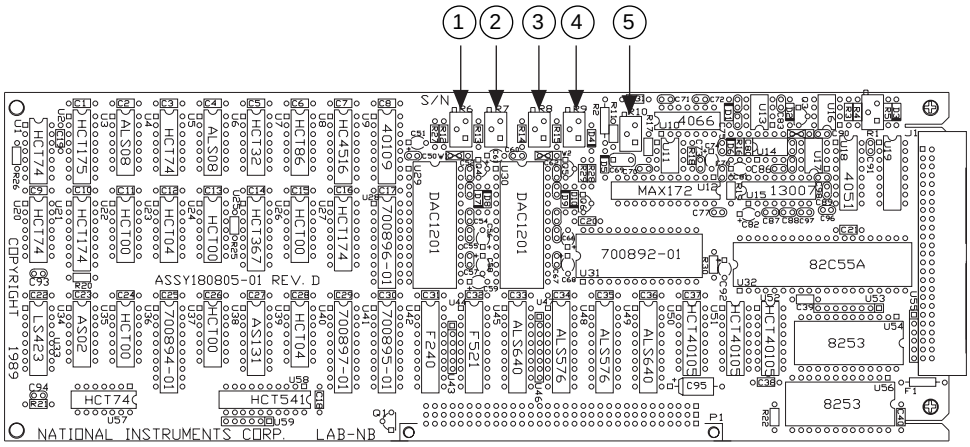
For best measurement results, the Lab-NB needs to be calibrated so that its measurement accuracy is within ±0.012% of its input range (±0.5 LSB). According to standard practice, the equipment used to calibrate the Lab-NB should be 10 times as accurate, that is, have ±0.001% rated accuracy. Practically speaking, calibration equipment with four times the accuracy of the item under calibration is generally considered acceptable. Four times the accuracy of the Lab-NB is 0.003%.

You need the following equipment to calibrate the Lab-NB board:

- For analog input calibration, you need a precision variable DC voltage source (usually a calibrator) with these features:
  - Accuracy — ±0.001% standard
±0.003% sufficient
  - Range — Greater than ±10 V
  - Resolution — 100 µV in ±10 V range ($5^1/_2$ digits)
- For analog output calibration, you need a voltmeter with these features:
  - Accuracy — ±0.001% standard
±0.003% sufficient
  - Range — Greater than ±10 V
  - Resolution — 100 µV in ±10 V range ($5^1/_2$ digits)

Calibration Trimpots

The Lab-NB has six trimpots for calibration. The location of these trimpots on the Lab-NB board is shown in the partial diagram of the board in Figure 5-1.



1	R6	2	R7
3	R8	4	R9
5	R10	6	R1

Figure 5-1. Calibration Trimpot Location Diagram

The following trimpots are used to calibrate the analog input circuitry:

- R1 – Offset trim, analog input
- R10 – Gain trim, analog input

The following trimpots are used to calibrate the analog output circuitry:

- R6 – Gain trim, analog output channel 0
- R7– Offset trim, analog output channel 0
- R8 – Gain trim, analog output channel 1
- R9 – Offset trim, analog output channel 1

Analog Input Calibration

To null out error sources that compromise the quality of measurements, you must calibrate the analog input circuitry by adjusting the following potential sources of error:

- Offset errors
- Gain error of the analog input circuitry

The calibration must be performed if the input configuration is changed from bipolar (the factory setting) to unipolar.

Offsets at the input to the instrumentation amplifier contribute gain-dependent offset error to the analog input circuitry. This offset is multiplied by the gain instrumentation amplifier. Other sources of offset error include the track-and-hold amplifier and the ADC. On the Lab-NB, one trimpot is used to null out all of these offset sources. Because one of these error sources is gain-dependent, the offset should be checked and recalibrated, if necessary, whenever the gain is changed significantly. Alternatively, the input offset calibration can be performed at gain = 1 with the offset errors noted for all other gains. A software correction can then be applied to the readings at gains higher than one by subtracting the offset errors. Using this method, the board can be used at all available gain levels without recalibrating the input.

The maximum offset at the gain amplifier is specified at 0.5 mV. The gain amplifier's maximum possible contribution to the total offset is therefore 0.5 mV multiplied by the gain. To find the error in LSBs, divide this voltage by the voltage of 1 LSB. Hence, with a large gain change, such as from 1 to 100, the number of LSBs of offset from this source changes from about 0.2 to almost 20. Clearly, an adjustment that is acceptable for a 0.2 LSB error is probably not suitable when the error is multiplied by 100. For small changes in the gain, the error that accompanies changes in gain is much less. If the gain is changed from 1 to 2 or 5, the offset probably does not need to be recalibrated. Likewise, changes between gains of 20, 50, or 100 probably do not require recalibration.

All the stages up to and including the input to the ADC contribute to the gain error of the analog input circuitry. With the amplifier set to a gain of 1, the gain of the analog input circuitry is ideally 1. The gain error is the deviation of the gain from 1 and appears as a multiplication of the input voltage being measured. To calibrate this offset, you must apply V_{+fs} -1.5 LSB to the analog input circuitry and adjust a potentiometer until the ADC returns readings that flicker between its most positive count and the most positive count minus 1. The voltages corresponding to V_{+fs} and 1 LSB are given in the following table.

The voltages corresponding to V_{-fs}, which is the most negative voltage that the ADC can read, V_{+fs} - 1, which is the most positive voltage the ADC can read, and 1 LSB, which is the voltage corresponding to one count of the ADC, depend on the input range selected. The value of these voltages for each input range is given in the following table.

Input Range	V_{-fs}	V_{+fs} - 1	1 LSB	0.5 LSB
-5 to +5 V	-5 V	+4.99756 V	2.44 mV	1.22 mV
0 to 10 V	0 V	+9.99756 V	2.44 mV	1.22 mV

Board Configuration

The calibration procedure differs if you select either bipolar or unipolar input configuration. A procedure for each configuration is given next.

Bipolar Input Calibration Procedure

If your board is configured for bipolar input, which provides the range -5 to +5 V, then complete the following procedure in the order given. This procedure assumes that ADC readings are in the range -2,048 to +2,047, that is, the TWOSCMP bit in the ADC Configuration Register is set high.

1. Offset Calibration

To adjust the amplifier input offset:

a. Connect ACH0 (pin 1 on the I/O connector) to AGND (pin 9).

b. Take analog input readings from channel 0 at the gain at which the system will be used.

c. Adjust trimpot R1 until the average reading is ±0.5 LSB.

Alternatively, the above offset calibration procedure can be carried out with the input gain set at 1, followed by recording the average reading at all other gains. These readings can be used later for software offset correction of the data at gains other than 1, thus eliminating the need to perform the input offset recalibration when a different gain is used. The software correction consists of subtracting the recorded reading at gain G from every A/D conversion value obtained at gain G.

2. Gain Calibration

Adjust the analog input gain by applying an input voltage across ACH0 and AGND. This input voltage is +4.99634 V or V_{+fs} - 1.5 LSB.

a. Connect the calibration voltage (+4.99634 V) across ACH0 (pin 1 on the I/O connector) and AGND (pin 9).

b. Take analog input readings from channel 0 at a gain of 1, and adjust trimpot R10 until the ADC readings flicker evenly between 2,046 and 2,047. Alternatively, you can average a number of readings (approximately 100) and adjust trimpot R10 until the average reading is 2,046.5.

Unipolar Input Calibration Procedure

If your board is configured for unipolar input, which has an input range of 0 to +10 V, then complete the following steps in sequence. This procedure assumes that ADC readings are in the range 0 to 4,095, that is, the TWOSCMP bit in the ADC Configuration Register is cleared.

1. Offset Calibration

To adjust the amplifier input offset:

a. Connect ACH0 (pin 1 on the I/O connector) to AGND (pin 9).

b. Take analog input readings from channel 0 at the gain at which the system will be used.

c. Adjust trimpot R1 until the readings flicker between 0 and 1. Care must be taken to avoid setting the potentiometer too low in the unipolar mode. If the potentiometer is set too low, the ADC then simply outputs 0 because its input is below the lower limit.

2. Gain Calibration

Adjust the analog input gain by applying an input voltage across ACH0 and AGND. This input voltage is +9.99634 V or V_{+fs} - 1.5 LSB.

a. Connect the calibration voltage (+9.99634 V) across ACH0 (pin 1 on the I/O connector) and AGND (pin 0).

b. Take analog input readings from channel 0 at a gain of 1, and adjust trimpot R10 until the ADC readings flicker evenly between 4,094 and 4,095. Alternately, you can average a number of readings (approximately 100) and adjust trimpot R10 until the average reading is 4,094.5.

Analog Output Calibration

To null out error sources that affect the accuracy of the output voltages generated, you must calibrate the analog output circuitry by adjusting the following potential sources of error:

- Analog output offset error
- Analog output gain error

Offset error in the analog output circuitry is the total of the voltage offsets contributed by each component in the circuitry. This error appears as a voltage difference between the desired voltage and the actual output voltage generated and is independent of the D/A setting. To correct this offset gain error, set the D/A to negative full-scale and adjust a trimpot until the output voltage is the negative full-scale value ±0.5 LSB.

Gain error in the analog output circuitry is the product of the gains contributed by each component in the circuitry. This error appears as a voltage difference between the desired voltage and the actual output voltage generated, which depends on the D/A setting. This gain error is corrected by setting the D/A to positive full-scale and adjusting a trimpot until the output voltage corresponds to the positive full-scale value ±0.5 LSB.

Board Configuration

The calibration procedure differs if you select either bipolar or unipolar output configuration. A procedure for each configuration is given next.

Bipolar Output Calibration Procedure

If your board is configured for bipolar output, which provides an output range of -5 to +5 V, then complete the following procedures in the order given.

1. Adjust the Analog Output Offset

Adjust the analog output offset by measuring the output voltage generated with the DAC set at negative full-scale (-2048). This output voltage should be V_{-fs} ±0.5 LSB. For bipolar output,

V_{-fs} = -5 V, and 0.5 LSB = 1.22 mV.

For analog output channel 0:

a. Connect the voltmeter between DAC0 OUT (pin 10 on the I/O connector) and AOGND (pin 11).

b. Set the analog output channel to -5 V by writing -2048 to the DAC.

c. Adjust trimpot R7 until the output voltage read is -5 V.

For analog output channel 1:

a. Connect the voltmeter between DAC1 OUT (pin 12 on the I/O connector) and AOGND (pin 11).

b. Set the analog output channel to -5 V by writing -2,048 to the DAC.

c. Adjust trimpot R9 until the output voltage read is -5 V.

2. Adjust the Analog Output Gain

Adjust the analog output gain by measuring the output voltage generated with the DAC set at positive full-scale (4,095). This output voltage should be V_{+fs} ±0.5 LSB. For bipolar output,

V_{+fs} = +4.99756 V, and 0.5 LSB = 1.22 mV.

For analog output channel 0:

a. Connect the voltmeter between DAC0 OUT (pin 10 on the I/O connector) and AOGND (pin 11).

b. Set the analog output channel to +4.99756 V by writing 2,047 to the DAC.

c. Adjust trimpot R6 until the output voltage read is +4.99756 V.

For analog output channel 1:

a. Connect the voltmeter between DAC1 OUT (pin 12 on the I/O connector) and AOGND (pin 11).

b. Set the analog output channel to +4.99756 V by writing 2,047 to the DAC.

c. Adjust trimpot R8 until the output voltage read is +4.99756 V.

Unipolar Output Calibration Procedure

If your analog output channel is configured for unipolar output, which has an output range of 0 to +10 V, then calibrate your board by completing the following procedure.

1. Adjust the Analog Output Offset

Adjust the analog output offset by measuring the output voltage generated with the DAC set at 0. This output voltage should be V_{-fs} ±0.5 LSB. For unipolar output,

V_{-fs} = 0 V, and 0.5 LSB = 1.22 mV

For analog output channel 0:

a. Connect the voltmeter between DAC0 OUT (pin 10 on the I/O connector) and AOGND (pin 11).

b. Set the analog output channel to 0 V by writing 0 to the DAC.

c. Adjust trimpot R7 until the output voltage read is 0 V.

For analog output channel 1:

a. Connect the voltmeter between DAC1 OUT (pin 12 on the I/O connector) and AOGND (pin 11).

b. Set the analog output channel to 0 V by writing 0 to the DAC.

c. Adjust trimpot R9 until the output voltage read is 0 V.

2. Adjust the Analog Output Gain

Adjust the analog output gain by measuring the output voltage generated with the DAC set at positive full-scale (4,095). This output voltage should be V_{+fs} ±0.5 LSB. For unipolar output,

V_{+fs} = +9.99756 V, and 0.5 LSB = 1.22 mV.

For analog output channel 0:

a. Connect the voltmeter between DAC0 OUT (pin 10 on the I/O connector) and AOGND (pin 11).

b. Set the analog output channel to +9.99756 V by writing 4,095 to the DAC.

c. Adjust trimpot R6 until the output voltage read is +9.99756 V.

For analog output channel 1:

a. Connect the voltmeter between DAC1 OUT (pin 12 on the I/O connector) and AOGND (pin 11).

b. Set the analog output channel to +9.99756 V by writing 4,095 to the DAC.

c. Adjust trimpot R8 until the output voltage read is +9.99756 V.

Appendix A
Specifications

This appendix lists the specifications of the Lab-NB. These specifications are typical at 25° C unless otherwise stated. The operating temperature range is 0° to 70° C.

Analog Input

Number of input channels	8 single-ended
Analog resolution	12 bits, one part in 4,096
Relative accuracy (nonlinearity)	±1.5 LSB max,
(nonlinearity + quantization error; see explanation of specifications)	±1.0 LSB typ
Differential nonlinearity	±1.0 LSB max (no missing codes), ±0.5 LSB typ
Analog input range	±5 V or 0 to +10 V; jumper-selectable
Input signal gain	1, 2, 5, 10, 20, 50, 100; software-selectable
Measurement (gain) accuracy	
gain = 1	±0.04% max, ±0.025% typ
Offset error	
(calibration performed at gain = 1)	
gain ≤ 20	±4 LSB max, ±2 LSB typ
gain > 20	±20 LSB max, ±10 LSB typ
Offset adjustment range, min	
(unipolar or bipolar ranges)	±47 LSB
Gain adjustment range, min	
(unipolar or bipolar ranges)	±31 LSB
System noise	0.3 LSB rms for gain = 1 0.6 LSB rms for gain = 100
Temperature coefficients	
Gain error	±10 ppm/°C
Offset error	450 µV/°C + 10 µV/°C∗ gain
Input bias current	150 pA
Input impedance	0.1 GΩ in parallel with 45 pF
Input protection	±45 V on all inputs (not ground)

Explanation of Analog Input Specifications

Relative accuracy is a measure of the linearity of an ADC. However, relative accuracy is a tighter specification than a *nonlinearity* specification. Relative accuracy indicates the maximum deviation from a straight line for the analog-input-to-digital-output transfer curve. If an ADC has been calibrated perfectly, then this straight line is the ideal transfer function, and the relative accuracy specification indicates the worst deviation from the ideal that the ADC permits.

A relative accuracy specification of ±1 LSB is roughly equivalent to (but not the same as) a $\pm 1/2$ LSB nonlinearity or integral nonlinearity specification because relative accuracy encompasses both nonlinearity and variable quantization uncertainty, a quantity often mistakenly assumed to be exactly $\pm 1/2$ LSB. Although quantization uncertainty is ideally $\pm 1/2$ LSB, it can be different for each possible digital code and is actually the analog width of each code. Thus, it is more specific to use relative accuracy as a measure of linearity than it is to use what is

normally called nonlinearity, because relative accuracy ensures that the *sum* of quantization uncertainty and A/D conversion error does not exceed a given amount.

Integral nonlinearity in an ADC is an often ill-defined specification that is supposed to indicate a converter's overall A/D transfer linearity. The manufacturers of the ADC chips used by National Instruments specify their integral nonlinearity by stating that the analog center of any code will not deviate from a straight line by more than $\pm 1/2$ LSB. This specification is misleading because although a particularly wide code's center may be found within $\pm 1/2$ LSB of the ideal, one of its edges may be well beyond ±1 LSB. Thus, the ADC has a relative accuracy of that amount. National Instruments tests its boards to ensure that they meet all three linearity specifications defined in this appendix; specifications for integral nonlinearity are included primarily to maintain compatibility with a convention of specifications used by other board manufacturers. Relative accuracy, however, is much more useful.

Differential nonlinearity is a measure of deviation of code widths from their theoretical value of 1 LSB. The width of a given code is the size of the range of analog values that can be input to produce that code, ideally 1 LSB. A specification of ±1 LSB differential nonlinearity ensures that no code has a width of 0 LSBs (that is, no missing codes) and that no code width exceeds 2 LSBs.

System noise is the amount of noise seen by the ADC when there is no signal present at the input of the board. The amount of noise that is reported directly (without any analysis) by the ADC is not necessarily the amount of real noise present in the system, unless the noise is ≥ 0.5 LSB RMS. Noise that is less than this magnitude produces varying amounts of flicker, and the amount of flicker seen is a function of how near the real mean of the noise is to a code transition. If the mean is near or at a transition between codes, the ADC flickers evenly between the two codes, and the noise is seen as very nearly 0.5 LSB. If the mean is near the center of a code and the noise is relatively small, very little or no flicker is seen, and the noise is reported by the ADC as nearly 0 LSB. From the relationship between the mean of the noise and the measured RMS magnitude of the noise, the character of the noise can be determined. National Instruments has determined that the character of the noise in the Lab-NB is fairly Gaussian, and so the noise specifications given are the amounts of pure Gaussian noise required to produce our readings.

Analog Data Acquisition

Data transfers	Programmed I/O or interrupts
Max sample rate	62.5 kHz
Analog bandwidth (-3 dB)	400 kHz (gain = 1)
	40 kHz (gain = 100)
Max multichannel scan rate	62.5 kHz (gain = ≤ 50)
	20 kHz (gain = 100)

Analog Output

Number of output channels	2 single-ended
Analog resolution	12 bits, one part in 4,096
Relative accuracy (nonlinearity)	±0.75 LSB max
Differential nonlinearity	±1 LSB max (monotonic over temperature),
	±0.25 LSB typ
Offset adjustment range, min	±37 mV
Gain adjustment range, min	±39 mV
Output voltage ranges	0 to +10 V, unipolar mode
	±5 V, bipolar mode; software selectable
Current drive capability	±1 mA
Output settling time	7 µsec for 10 V step to 0.012%
Output slew rate	9 V/µsec
Output Impedance	0.1 Ω max
Temperature coefficients	
Gain error	±10 ppm/° C

Voltage offset.....±60 µV/° C

Explanation of Analog Output Specifications

Relative accuracy in a D/A system is the same as nonlinearity, because no uncertainty is added due to code width. Unlike an ADC, every digital code in a D/A system represents a specific analog value rather than a range of values. The relative accuracy of the system is therefore limited to the worst-case deviation from the ideal correspondence (a straight line), excepting noise. If a D/A system has been calibrated perfectly, then the relative accuracy specification reflects its worst-case absolute error.

Differential nonlinearity in a D/A system is a measure of deviation of code width from 1 LSB. In this case, code width is the difference between the analog values produced by consecutive digital codes. A specification of ±1 LSB differential nonlinearity ensures that the code width is always greater than 0 LSBs (guaranteeing monotonicity) and is always less than 2 LSBs.

Digital I/O

Compatibility.....TTL-compatible
Configuration.....Three 8-bit ports (uses 82C55A PPI)
Input logic low voltage.....0.8 V max
Input logic high voltage.....2.2 V min
Output logic low voltage
  at output current = 2.5 mA.....0.4 V max
Output logic high voltage
  at output current = –2.5 µA.....3.7 V min
Input load current
  $0 \le V_{IN} \le 5$ V.....±1 µA max
Output current
  at V_{OL} = 0.5 V.....4.0 mA min
Output current
  at V_{OH} = 2.7 V.....4.0 mA min

Timing I/O

Compatibility.....TTL-compatible inputs and outputs. Counter gate and clock inputs are pulled up with 4.7 kΩ resistors onboard.
Configuration.....Six 16-bit counter/timers (uses two 8253s)
Input logic low voltage.....0.8 V max
Input logic high voltage.....2.2 V min
Output logic low voltage
  at output current = 1.6 mA.....0.45 V max
Output logic high voltage
  at output current = -150 µA.....2.4 V min
Input load current
  $0 \le V_{IN} \le 5$ V.....$(5.0 \text{ V} - V_{IN}) / 10\ \text{k}\Omega$
Input capacitance at 1 MHz.....10 pF max
Base clock frequency.....2 MHz ±0.01%

Power Requirements (from Macintosh NuBus)

Power consumption
  +5 VDC.....810 mA*
  +12 VDC.....70 mA
  -12 VDC.....100 mA
* Additional current up to 1 A can be drawn by the user through the 50-pin I/O connector.

Physical

Board dimensions.....27.62 by 10.16 cm (10.875 by 4.0 in.)
I/O connector.....50-pin D male ribbon-cable connector

Environment

Operating temperature.....0° to 70° C
Storage temperature.....-55° to 150° C
Relative humidity.....5% to 90% noncondensing

Appendix B
I/O Connector

This appendix contains the pinout and signal names for the I/O connector on the Lab-NB.

Figure B-1 shows the Lab-NB 50-pin I/O connector.

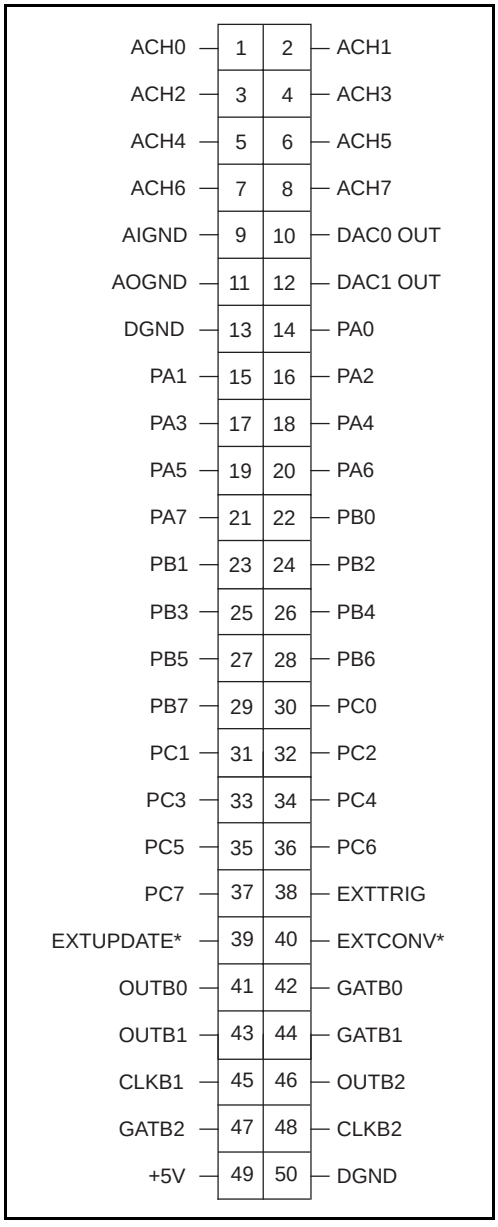


Figure B-1. Lab-NB I/O Connector

Detailed signal specifications are included in Chapter 2, *Configuration and Installation*, and in Appendix A, *Specifications*.

Appendix C
AMD 8253 Data Sheet*

This appendix contains the manufacturer data sheet for the AMD 8253 System Timing Controller integrated circuit (Advanced Micro Devices, Inc.). This circuit is used on the Lab-NB.

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Advanced Micro Devices, Inc. 1987 Data Book *MOS Microprocessors and Peripherals.*

8253

Programmable Interval Timer
iAPX86 Family

DISTINCTIVE CHARACTERISTICS

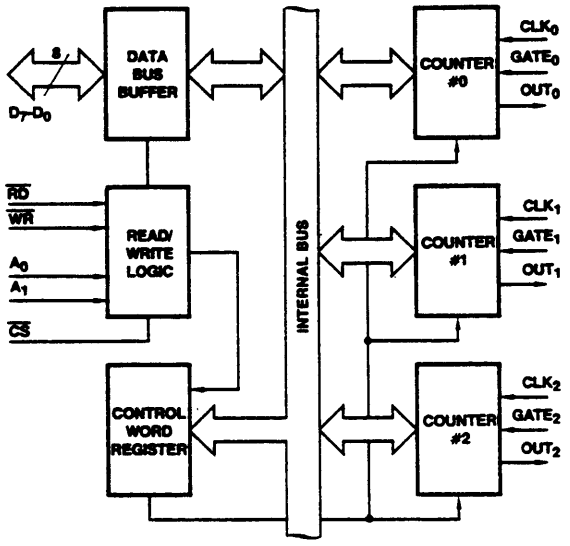
- Both Binary and BCD counting
- Single +5V supply
- Three independent 16-bit counters
- DC to 5MHz
- Programmable counter modes
- Bus oriented I/O

GENERAL DESCRIPTION

The 8253 is a programmable counter/timer chip designed for use with 8080A/8085A microprocessors. It uses NMOS technology with a single +5V supply and is a direct replacement for Intel's 8253/8253-5.

Each device is organized as three independent 16-bit counters, each counter having a rate of up to 5MHz. All modes of operation are software programmable. For improved performance devices see the Am9513A System Timing Controller.

BLOCK DIAGRAM



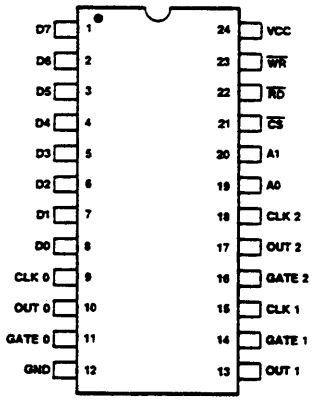
BD003760

Publication # 04126 | Rev. B | Amendment /0
Issue Date: May 1987

8253

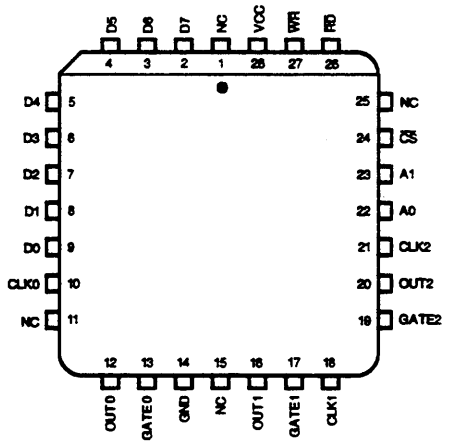
CONNECTION DIAGRAMS
Top View

DIPs



CD005672

PLCC



CD010071

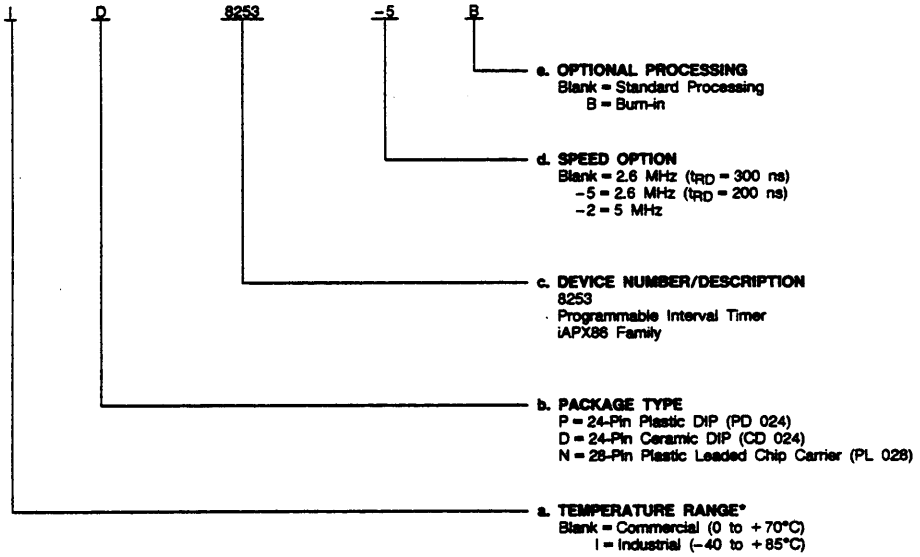
Note: Pin 1 is marked for orientation.

3-320

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Temperature Range**
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations	
P, D, N	8253
	8253-5
	8253-2
D, ID	8253B
	8253-5B
D	8253-2B

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

*This device is also available in Military temperature range. See MOS Microprocessors and Peripherals Handbook (Order #09275A/0) for electrical performance characteristics.

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8253

PIN DESCRIPTION

Pin No.*	Name	I/O	Description
1-8	D7-D0	I/O	Data bus (8-bit).
9, 15, 18	CLK N	I	Counter clock inputs.
11, 14, 16	GATE N	I	Counter gate inputs.
10, 13, 17	OUT N	O	Counter outputs.
22	$\overline{RD}$	I	Read counter.
23	$\overline{WR}$	I	Write command or data.
21	$\overline{CS}$	I	Chip select.
19, 20	A0-A1	I	Counter select.
24	VCC		+5 Volts.
12	GND		Ground.

* Pin numbers correspond to DIPs only.

DETAILED DESCRIPTION

General

The 8253 is a programmable interval timer/counter specifically designed for use with 8080A Microcomputer systems. Its function is that of a general-purpose, multitiming element that can be treated as an array of I/O ports in the system's software.

The 8253 solves one of the most common problems in any microcomputer system: the generation of accurate time delays under software control. Instead of setting up timing loops in the system's software, the programmer configures the 8253 to match his requirements and initializes one of the counters of the 8253 with a desired quantity. Then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its task. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real-Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions:

1. Programming the MODES of the 8253,
2. Loading the count registers, and
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no Read or Write operation can occur unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "LOW" on this input informs the 8253 that the CPU is inputting data in the form of a counter's value.

$\overline{WR}$ (Write)

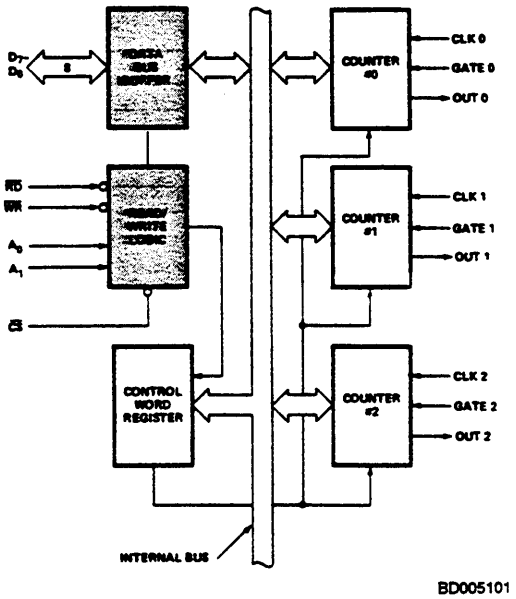
A "LOW" on this input informs the 8253 that the CPU is outputting data in the form of MODE information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for MODE selection.

$\overline{CS}$ (Chip Select)

A "LOW" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.



BD005101

Figure 1. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, the selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, presettable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have a different MODE configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications, and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write MODE Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

8253 SYSTEM INTERFACE

The 8253 is a component of the iAPX Family and interfaces in the same manner as all other peripherals of the family. It is treated by the system's software as an array of peripheral I/O ports; three are counters, and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method, or it can be connected to the output of a decoder, such as an AMD Am25LS2548 or Am25LS2538 for larger systems.

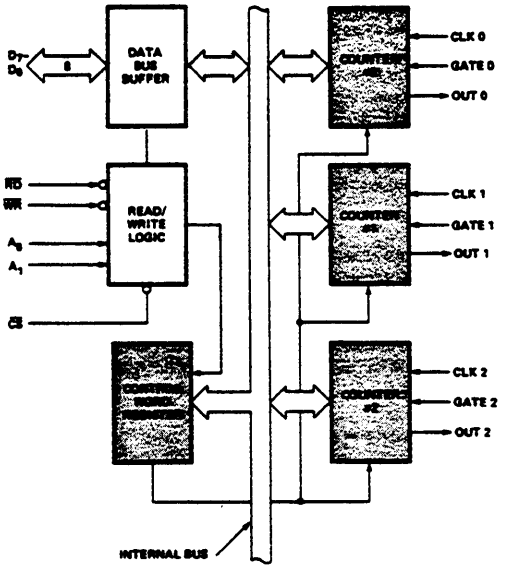


Figure 2. Block Diagram Showing Control Word Register and Counter Functions

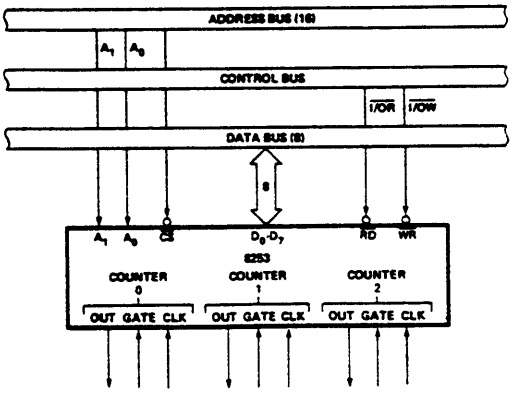


Figure 3. 8253 System Interface

8253 READ/WRITE PROCEDURE

Write Operations

The system's software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection; e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent (SC0, SC1).

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8253

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded, it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 a new count will not start until the load has been completed. The count register will accept one or two bytes depending on how the MODE control words (RL0, RL1) are programmed.

Programming Format

MODE Control Word
Counter n

LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Alternate Programming Formats

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253, the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253, it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read, then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

For the programmer to read the contents of any counter without effecting or disturbing the counting operation, the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly," he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter, and the contents of the latched register are available.

MODE Register for Latching Count

A0, A1 = 11

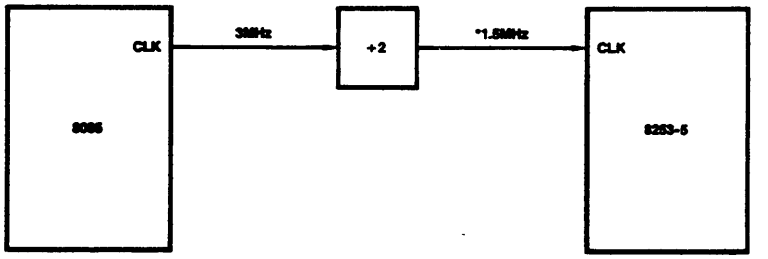
D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SCI,SCO – specify counter to be latched.
D5,D4 – 00 designates counter latching operation.
X – don't care

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.

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Clock Interface*



AF002870

*If an 8085 clock output is to drive an 8253-5 clock input, it must be reduced to 2MHz or less.

PROGRAMMING INFORMATION

General

The complete functional definition of the 8253 is programmed by the system's software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. These control words program the MODE, loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned.

The actual counting operation of each counter is completely independent, and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the system's software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register (A0, A1 = 11).

Control Word Format

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC – Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL – Read/Load:

RL1	RL0	
0	0	Counter Latching operation.
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M – MODE:

M2	M1	M0	
0	0	0	MODE 0
0	0	1	MODE 1
X	1	0	MODE 2
X	1	1	MODE 3
1	0	0	MODE 4
1	0	1	MODE 5

BCD:

0	Binary Counter 16-bits
1	Binary Code Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

3

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8253

MODE DEFINITION

MODE 0: Interrupt on Terminal Count

The output will be initially LOW after the mode set operation. After the count is loaded into the selected count register, the output will remain LOW and the counter will count. When terminal count is reached, the output will go HIGH and remain HIGH until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

1. Write 1st byte stops the current counting.
2. Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot

The output will go LOW on the count following the rising edge of the gate input.

The output will go HIGH on the terminal count. If a new count value is loaded while the output is LOW, it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain LOW for the full count after any rising edge of the gate input.

MODE 2: Rate Generator

Divide by N counter. The output will be LOW for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses, the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when LOW, will force the output HIGH. When the gate input goes HIGH, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain HIGH until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator

Similar to MODE 2 except that the output will remain HIGH until one half the count has been completed (for even numbers) and go LOW for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is HIGH, the first clock pulse (after the count is loaded) decrements the count by one. Subsequent clock pulses decrement the clock by two. After timeout, the output goes LOW and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by three. Subsequent clock pulses decrement the count by two until time-out. Then the whole process is repeated. In this way, if the count is odd, the output will be HIGH for $(N + 1)/2$ counts and LOW for $(N - 1)/2$ counts.

MODE 4: Software-Triggered Strobe

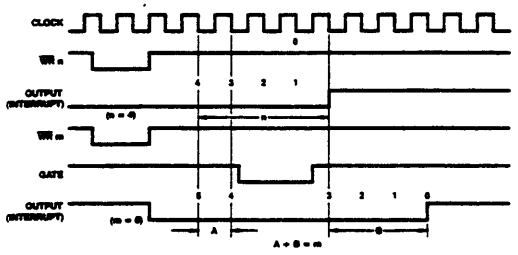
After the mode is set, the output will be HIGH. When the count is loaded, the counter will begin counting. On terminal count, the output will go LOW for one input clock period, then will go HIGH again.

If the count register is reloaded between output pulses, the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is LOW. Reloading the counter register will restart counting beginning with the new number.

MODE 5: Hardware-Triggered Strobe

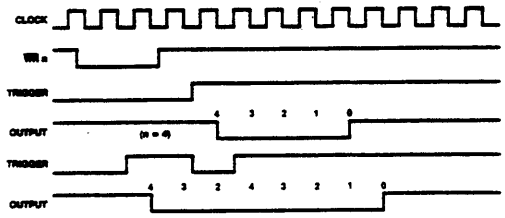
The counter will start counting after the rising edge of the trigger input and will go LOW for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go LOW until the full count after the rising edge of any trigger.

MODE 0. Interrupt on Terminal Count.



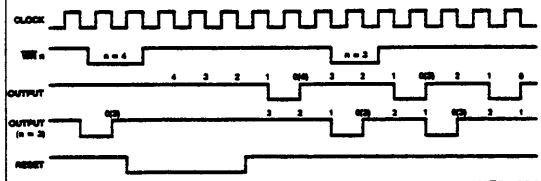
WF006860

MODE 1. Programmable One-Shot.



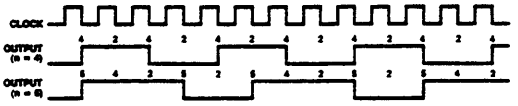
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MODE 2. Rate Generator.



WF006880

MODE 3. Square Wave Generator.

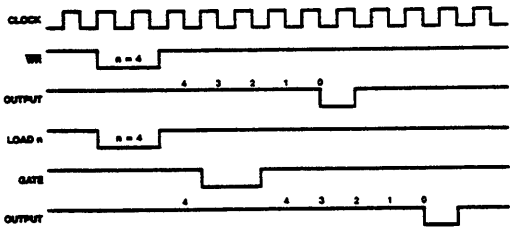


WF006890

Gate Pin Operations Summary

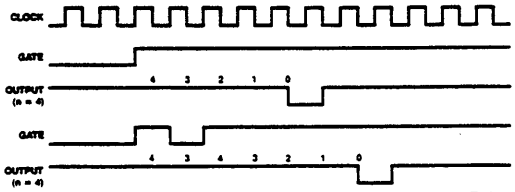
Modes	Signal Status		
	Low Or Going Low	Rising	High
0	Disables counting	–	Enables counting
1	–	1) Initiates counting 2) Resets output after next clock	–
2	1) Disables counting 2) Sets output immediately high	1) Reloads counter 2) Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	–	Enables counting
5	–	Initiates counting	–

MODE 4. Software-Triggered Strobe.



WF006900

MODE 5. Hardware-Triggered Strobe.



WF006910

8253 Timing Diagrams

8253

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage On Any Pin
with Respect to Ground ..... −0.5 to +7.0V
Power Dissipation 1W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... 5V ± 10%

Industrial (I) Devices
Temperature (T_A) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... 5V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

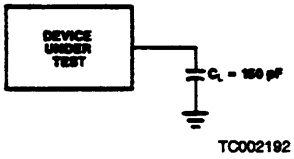
DC CHARACTERISTICS over operating ranges unless otherwise specified.

Parameters	Description	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage		-.5	.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + .5V	V
V_{OL}	Output Low Voltage	I_{OL} = 2.2 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0V		±10	µA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0V		±10	µA
I_{CC}	V_{CC} Supply Current			140	mA

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Parameters	Description	Test Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	f_c = 1MHz			10	pF
$C_{I/O}$	I/O Capacitance	Unmeasured pins returned to V_{SS}			20	pF

SWITCHING TEST CIRCUIT



TC002192

SWITCHING TEST INPUT WAVEFORM



WF006951

AC Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.2V for a logic "1" and 0.8V for a logic "0".

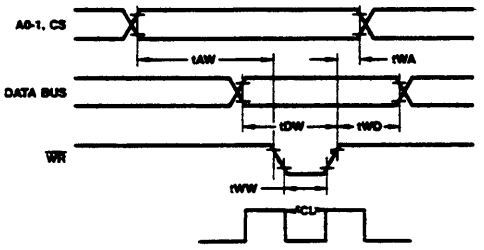
See Section 6 for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified.

Parameters	Description	8253		8253-5		8253-2		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{AR}	Address Stable Before $\overline{READ}$	50		30		25		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		150		ns
t_{RD}	Data Delay from $\overline{READ}$ (Note 2)		300		200		120	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	25	100	ns
t_{RV}	Recovery Time Between $\overline{READ}$ and Any Other Control Signal	1		1		0.5		μs
Write Cycle								
t_{AW}	Address Stable Before $\overline{WRITE}$	50		30		0		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		0		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		150		ns
t_{DW}	Data Set-up Time for $\overline{WRITE}$	300		250		100		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		0		ns
t_{RV}	Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal (Note 3)	1		1		0.5		μs

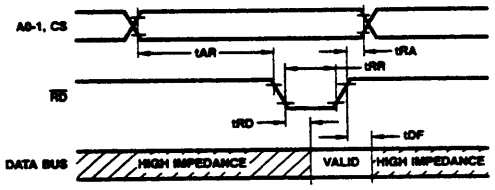
Notes: 1. AC timings measured at V_{OH} = 2.2, V_{OL} = 0.8.

Write Timing



WF006931

Read Timing



WF006940

3

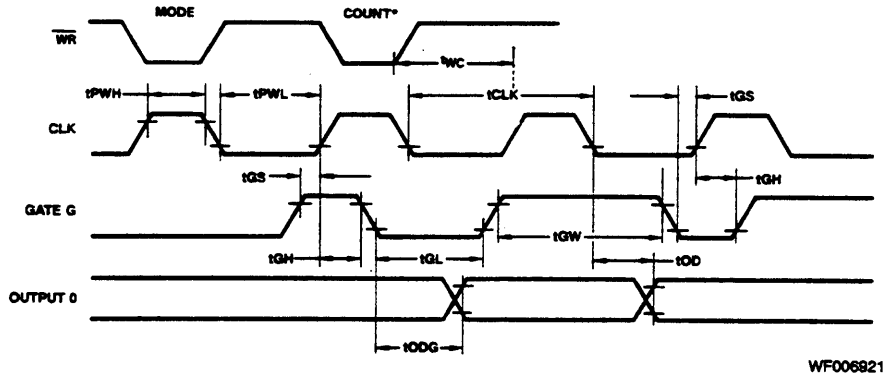
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8253

CLOCK AND GATE TIMING

Parameters	Description	8253		8253-5		8253-2		Units
		Min	Max	Min	Max	Min	Max	
t_{CLK}	Clock Period	380	DC	380	DC	200	DC	ns
t_{PWH}	High Pulse Width	230		230		90		ns
t_{PWL}	Low Pulse Width	150		150		90		ns
t_{GW}	Gate Width High	150		150		120		ns
t_{GL}	Gate Width Low	100		100		80		ns
t_{GS}	Gate Set-up Time to CLK↑	100		100		60		ns
t_{GH}	Gate Hold Time After CLK↑	50		50		50		ns
t_{OD}	Output Delay from CLK↓ (Note 1)		400		400		250	ns
t_{ODG}	Output Delay from Gate↓ (Note 1)		300		300		150	ns

CLOCK AND GATE TIMING



*last byte of count being written

Appendix D
OKI 82C55A Data Sheet*

This appendix contains the manufacturer data sheet for the OKI 82C55A (OKI Semiconductor) CMOS programmable peripheral interface . This interface is used on the Lab-NB.

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OKI Semiconductor Data Book *Microprocessor*, Seventh Edition, March 1993.

OKI semiconductor

MSM82C55A-2RS/GS/VJS

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

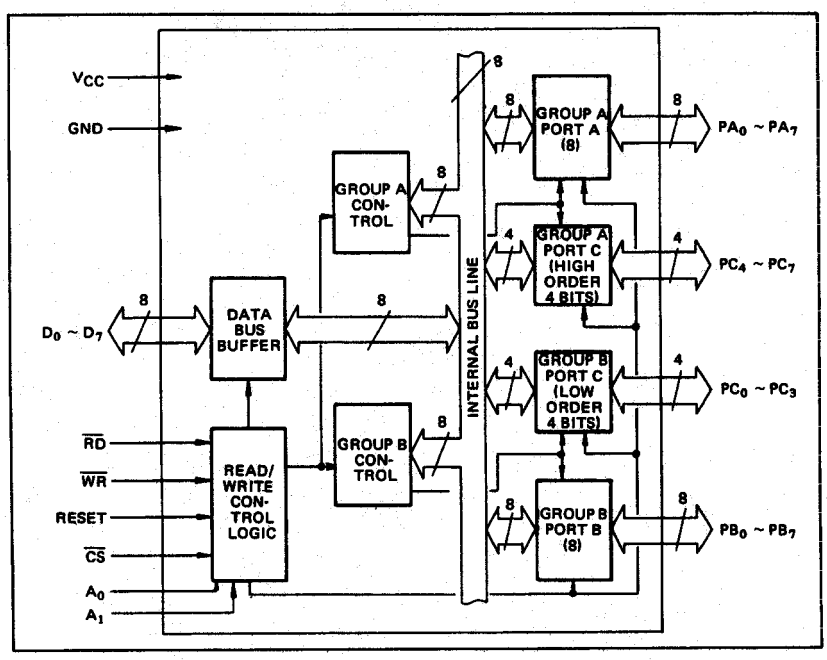
GENERAL DESCRIPTION

The MSM82C55A is a programmable universal I/O interface device which operates as high speed and on low power consumption due to 3 μ silicon gate CMOS technology. It is the best fit as an I/O port in a system which employs the 8-bit parallel processing MSM80C85A CPU. This device has 24-bit I/O pins equivalent to three 8-bit I/O ports and all inputs/outputs are TTL interface compatible.

FEATURES

- High speed and low power consumption due to 3 μ silicon gate CMOS technology
- 3 V to 6 V single power supply
- Full static operation
- Programmable 24-bit I/O ports
- Bidirectional bus operation (Port A)
- Bit set/reset function (Port C)
- TTL compatible
- Compatible with 8255A-5
- 40 pin Plastic DIP (DIP40-P-600)
- 44 pin PLCC (QFJ44-P-S650)
- 44 pin-V Plastic QFP (QFP44-P-910-VK)
- 44 pin-VI Plastic QFP (QFP44-P-910-VIK)

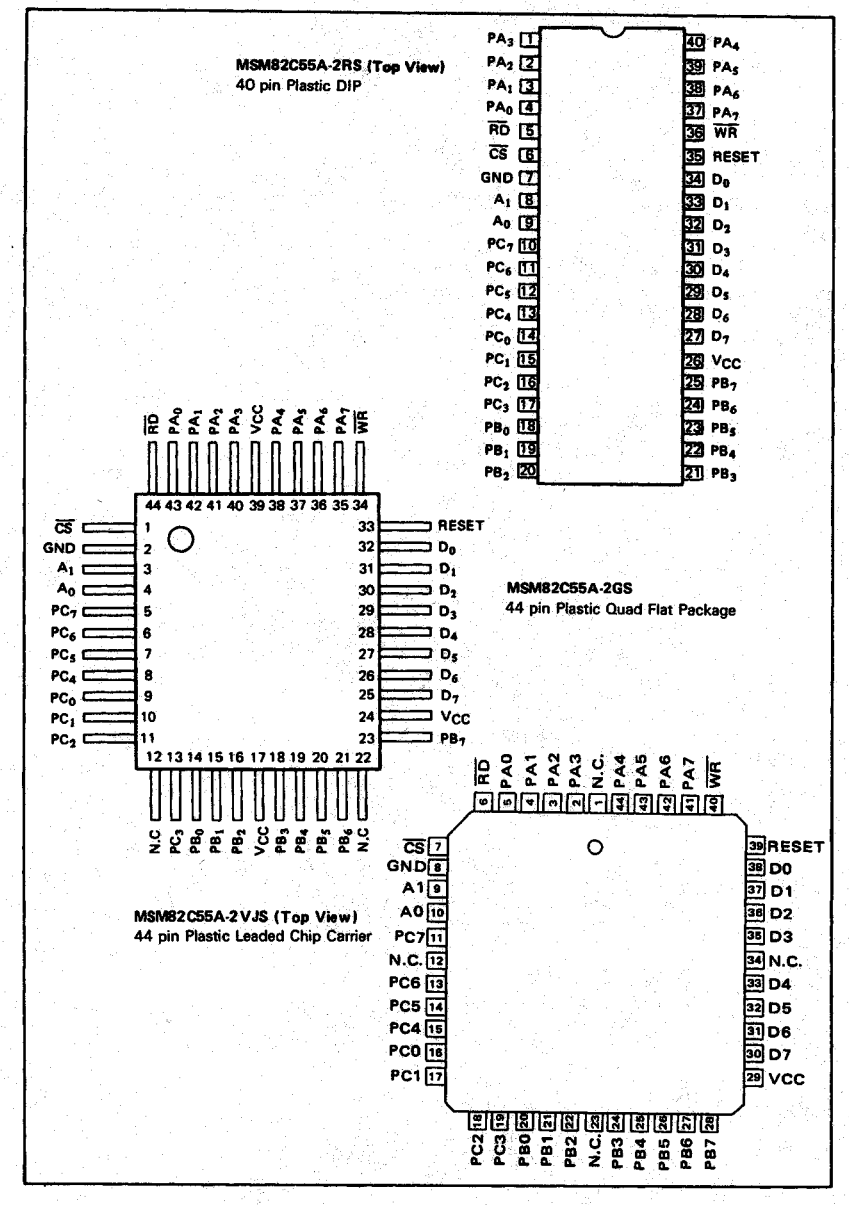
CIRCUIT CONFIGURATION



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I/O·MSM82C55A-2RS/GS/VJS

PIN CONFIGURATION



■ I/O·MSM82C55A-2RS/GS/VJS ■

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C55A-2RS	MSM82C55A-2GS	MSM82C55A-2VJS	
Ssupply Voltage	V_{CC}	Ta = 25°C with respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}	–	−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	–40 to 85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	–40	+25	+85	°C
"L" Input Voltage	V_{IL}	–0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		MSM82C55A-2			Unit
				Min.	Typ.	Max.	
"L" Output Voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC} = 4.5V to 5.5V Ta = −40°C to +85°C (C_L = 0pF)			0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = −40 μA		4.2			V
		I_{OH} = −2.5 mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−1		1	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Supply Current (standby)	I_{CCS}	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IH} \geq V_{CC}$ −0.2V $V_{IL} \leq$ 0.2V			0.1	10	μA
Average Supply Current (active)	I_{CC}	I/O wire cycle 82C55A-2 ... 8MHzCPU timing				8	mA

AC CHARACTERISTICS

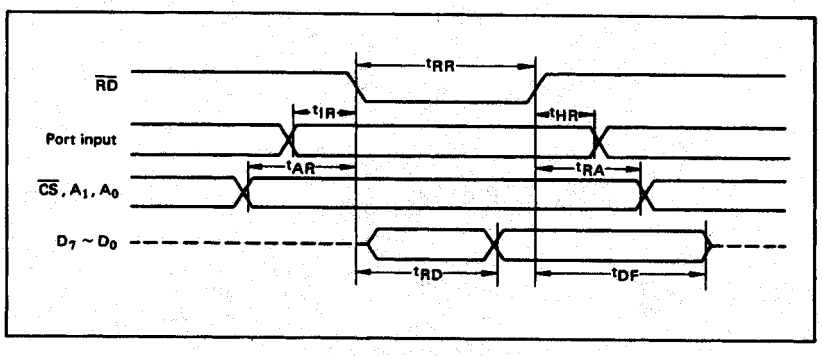
(V_{CC} = 4.5 to 5.5V, Ta = -40 to +80°C)

Parameter	Symbol	MSM82C55A-2		Unit	Remarks
		Min.	Max.		
Setup Time of address to the falling edge of $\overline{RD}$	t_{AR}	20		ns	Load 150 pF
Hold Time of address to the rising edge of $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	100		ns	
Delay Time from the falling edge of $\overline{RD}$ to the output of defined data	t_{RD}		120	ns	
Delay Time from the rising edge of $\overline{RD}$ to the floating of data bus	t_{DF}	10	75	ns	
Time from the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next falling edge of $\overline{RD}$ or $\overline{WR}$	t_{RV}	200		ns	
Setup Time of address before the falling edge of $\overline{WR}$	t_{AW}	0		ns	
Hold Time of address after the rising edge or $\overline{WR}$	t_{WA}	20		ns	
$\overline{WR}$ Pulse Width	t_{WW}	150		ns	
Setup Time of bus data before the rising edge of $\overline{WR}$	t_{DW}	50		ns	
Holt Time of bus data after the rising edge of $\overline{WR}$	t_{WD}	30		ns	
Delay Time from the rising edge of $\overline{WR}$ to the output of defined data	t_{WB}		200	ns	
Setup Time of port data before the falling edge of $\overline{RD}$	t_{IR}	20		ns	
Hold Time of port data after the rising edge of $\overline{RD}$	t_{HR}	10		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	100		ns	
$\overline{STB}$ Pulse Width	t_{ST}	100		ns	
Setup Time of port data before the rising edge of $\overline{STB}$	t_{PS}	20		ns	
Hold Time of port data after the rising edge of $\overline{STB}$	t_{PH}	50		ns	
Delay Time from the falling edge of $\overline{ACK}$ to the output of defined data	t_{AD}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the floating of port (Port A in mode 2)	t_{KD}	20	250	ns	
Delay Time from the rising edge of WR to the falling edge of $\overline{OBF}$	t_{WOB}		150	ns	
Delay Time from the falling edge of ACK to the rising edge of $\overline{OBF}$	t_{AOB}		150	ns	
Delay Time from the falling edge of STB to the rising edge of IBF	t_{SIB}		150	ns	
Delay Time from the rising edge of $\overline{RD}$ to the falling edge of IBF	t_{RIB}		150	ns	
Delay Time from the falling edge of $\overline{RD}$ to the falling edge of INTR	t_{RIT}		200	ns	
Delay Time from the rising edge of $\overline{STB}$ to the rising edge of INTR	t_{SIT}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the rising edge of INTR	t_{AIT}		150	ns	
Delay Time from the falling edge of $\overline{WR}$ to the falling edge of INTR	t_{WIT}		250	ns	

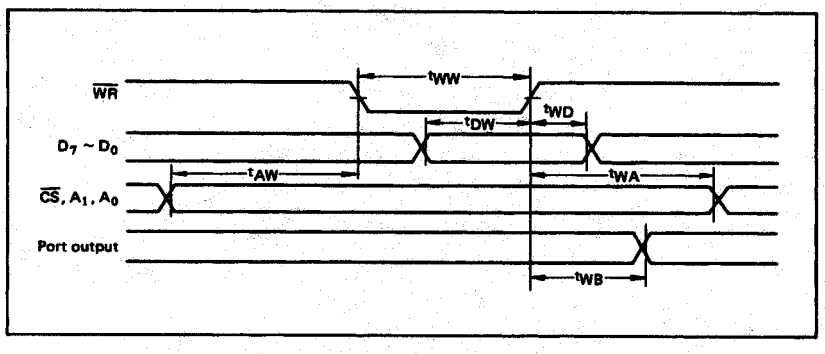
Note: Timing is measured at V_L = 0.8 V and V_H = 2.2 V for both input and outputs.

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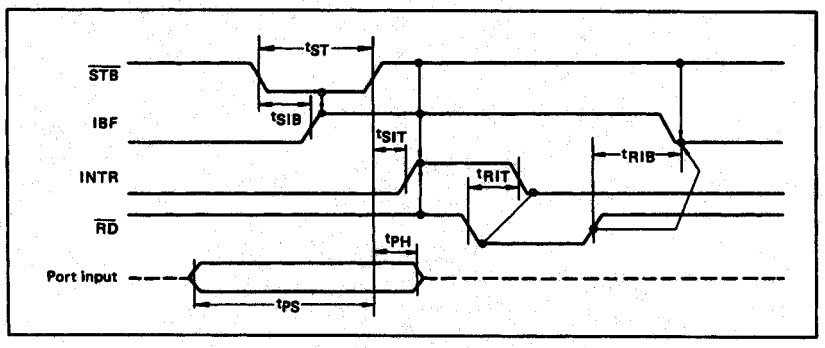
Basic Input Operation (Mode 0)



Basic Output Operation (Mode 0)

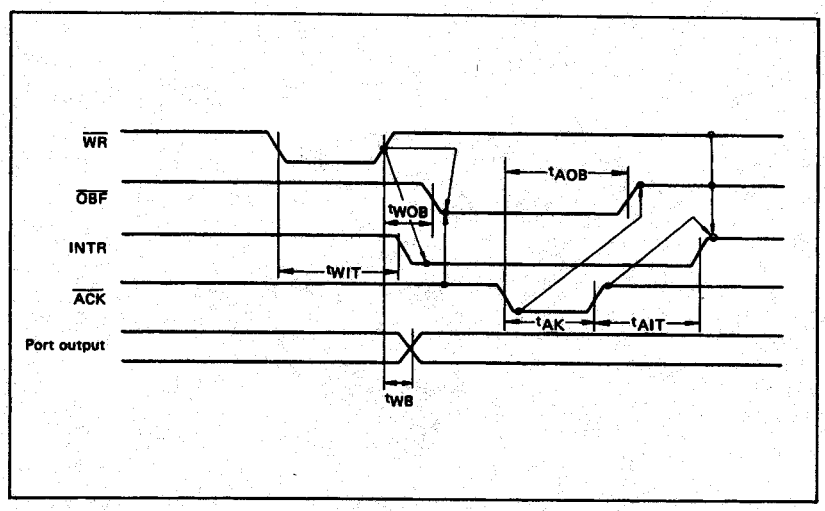


Strobe Input Operation (Mode 1)

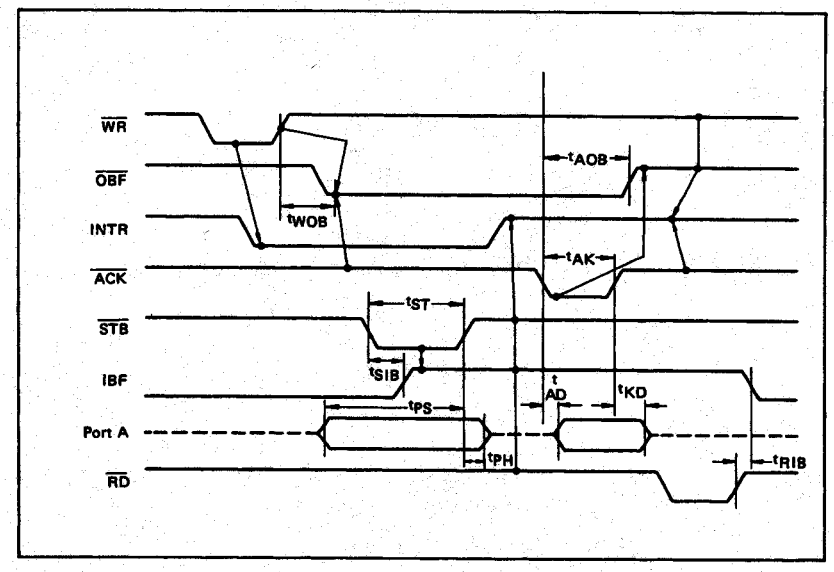


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Strobe Output Operation (Mode 1)



Bidirectional Bus Operation (Mode 2)

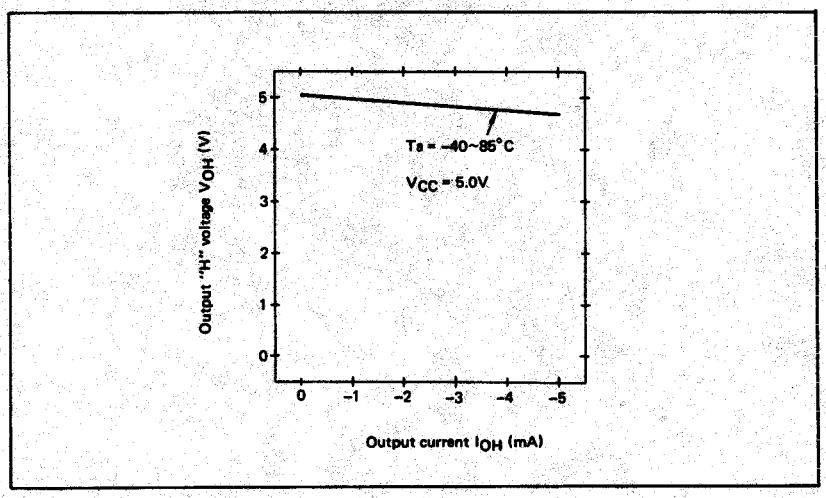


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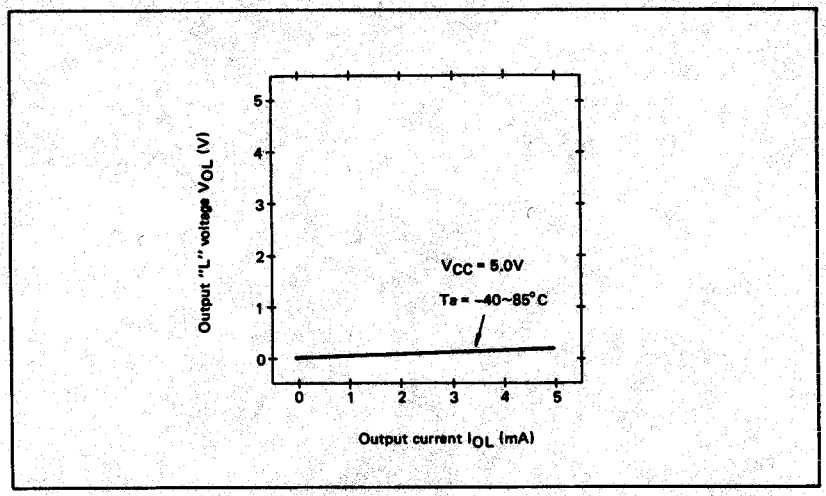
■ I/O·MSM82C55A-2RS/GS/VJS ■

OUTPUT CHARACTERISTICS (REFERENCE VALUE)

1 Output "H" Voltage (V_{OH}) vs. Output Current (I_{OH})



2 Output "L" Voltage (V_{OL}) vs. Output Current (I_{OL})



Note: The direction of flowing into the device is taken as positive for the output current.

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FUNCTIONAL DESCRIPTION OF PIN

Pin No.	Item	Input/Output	Function
D7 ~ D0	Bidirectional data bus	Input and output	These are three-state 8-bit bidirectional buses used to write and read data upon receipt of the $\overline{WR}$ and $\overline{RD}$ signals from CPU and also used when control words and bit set/reset data are transferred from CPU to MSM82C55A.
RESET	Reset input	Input	This signal is used to reset the control register and all internal registers when it is in high level. At this time, ports are all made into the input mode (high impedance status). all port latches are cleared to O. and all ports groups are set to mode O.
$\overline{CS}$	Chip select input	Input	When the $\overline{CS}$ is in low level, data transmission is enabled with CPU. When it is in high level, the data bus is made into the high impedance status where no write nor read operation is performed. Internal registers hold their previous status, however.
$\overline{RD}$	Read input	Input	When RD is in low level, data is transferred from MSM82C55A to CPU.
$\overline{WR}$	Write input	Input	When WR is in low level, data or control words are transferred from CPU to MSM82C55A.
A0, A1	Port select input (address)	Input	By combination of A0 and A1, either one is selected from among port A, port B, port C, and control register. These pins are usually connected to low order 2 bits of the address bus.
PA7 ~ PA0	Port A	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word. Especially, port A can be used as a bidirectional port when it is set to mode 2.
PB7 ~ PB0	Port B	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word.
PC7 ~ PC0	Port C	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word as 2 ports with 4 bits each. When port A or port B is used in mode 1 or mode 2 (port A only), they become control pins. Especially when port C is used as an output port, each bit can be set/reset independently.
V_{CC}			+5 V power supply.
GND			GND

BASIC FUNCTIONAL DESCRIPTION

Group A and Group B

When setting a mode to a port having 24 bits, set it by dividing it into two groups of 12 bits each.

- Group A: Port A (8 bits) and high order 4 bits of port C (PC7 ~ PC4)
- Group B: Port B (8 bits) and low order 4 bits of port C (PC3 ~ PC0)

Mode 0, 1, 2

There are 3 types of modes to be set by grouping as follows:

- Mode 0: Basic input operation/output operation (Available for both groups A and B)
- Mode 1: Strobe input operation/output operation (Available for both groups A and B)
- Mode 2: Bidirectional bus operation (Available for group A only)

When used in mode 1 or mode 2, however, port C has bits to be defined as ports for control signal for operation ports (port A for group A and port B for group B) of their respective groups.

Port A, B, C

The internal structure of 3 ports is as follows:

- Port A: One 8-bit data output latch/buffer and one 8-bit data input latch
- Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer
- Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input)

Single bit set/reset function for port C

When port C is defined as an output port, it is possible to set (to turn to high level) or reset (to turn to low level) any one of 8 bits individually without affecting other bits.

■ I/O-MSM82C55A-2RS/GS/VJS ■

OPERATIONAL DESCRIPTION

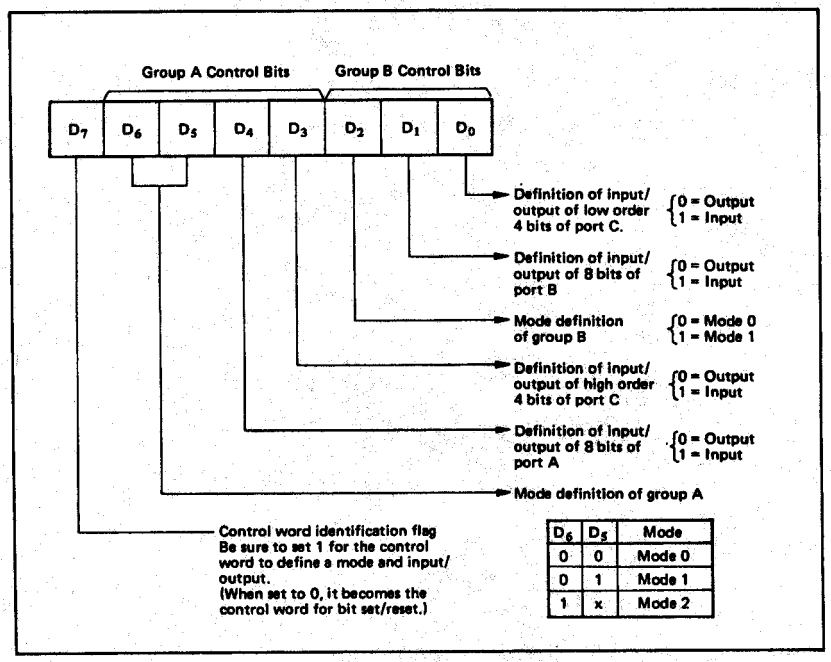
Control Logic

Operations by addresses and control signals, e.g., read and write, etc. are as shown in the table below:

Operation	A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Operation
Input	0	0	0	1	0	Port A → Data Bus
	0	1	0	1	0	Port B → Data Bus
	1	0	0	1	0	Port C → Data Bus
Output	0	0	0	0	1	Data Bus → Port A
	0	1	0	0	1	Data Bus → Port B
	1	0	0	0	1	Data Bus → Port C
Control	1	1	0	0	1	Data Bus → Control Register
Others	1	1	0	1	0	Illegal Condition
	x	x	1	x	x	Data bus is in the high impedance status.

Setting of Control Word

The control register is composed of 7-bit latch circuit and 1-bit flag as shown below.



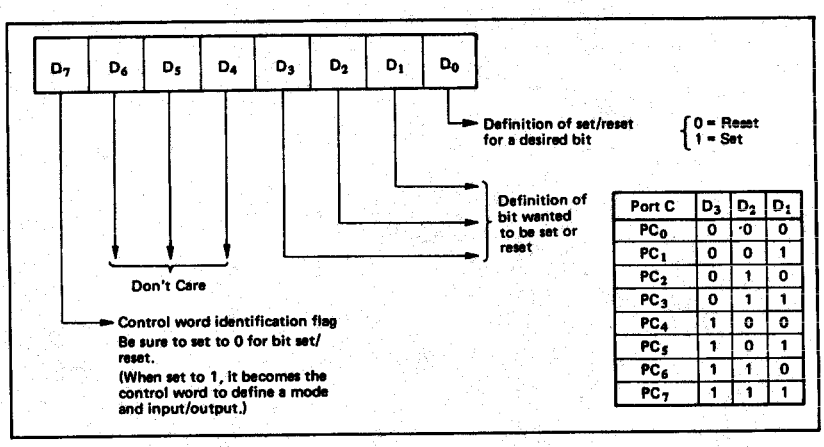
D_6	D_5	Mode
0	0	Mode 0
0	1	Mode 1
1	x	Mode 2

Precaution for mode selection

The output registers for ports A and C are cleared to ϕ each time data is written in the command register and the mode is changed, but the port B state is undefined.

Bit Set/Reset Function

When port C is defined as output port, it is possible to set (set output to 1) or reset (set output to 0) any one of 8 bits without affecting other bits as shown next page.



Port C	D_3	D_2	D_1
PC_0	0	0	0
PC_1	0	0	1
PC_2	0	1	0
PC_3	0	1	1
PC_4	1	0	0
PC_5	1	0	1
PC_6	1	1	0
PC_7	1	1	1

Interrupt Control Function

When the MSM82C55A is used in mode 1 or mode 2, the interrupt signal for the CPU is provided. The interrupt request signal is output from port C. When the internal flip-flop INTE is set beforehand at this time, the desired interrupt request signal is output. When it is reset beforehand, however, the interrupt request signal is not output. The set/reset of the internal flip-flop is made by the bit set/reset operation for port C virtually.

Bit set → INTE is set → Interrupt allowed
Bit reset → INTE is reset → Interrupt inhibited

Operational Description by Mode

1. Mode 0 (Basic input/output operation)

Mode 0 makes the MSM82C55A operate as a basic input port or output port. No control signals such as interrupt request, etc. are required in this mode. All 24 bits can be used as two-8-bit ports and two 4-bit ports. Sixteen combinations are then possible for inputs/outputs. The inputs are not latched, but the outputs are.

Type	Control Word								Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	High Order 4 Bits of Port C	Port B	Low Order 4 Bits of Port C
1	1	0	0	0	0	0	0	0	Output	Output	Output	Output
2	1	0	0	0	0	0	0	1	Output	Output	Output	Input
3	1	0	0	0	0	0	1	0	Output	Output	Input	Output
4	1	0	0	0	0	0	1	1	Output	Output	Input	Input
5	1	0	0	0	1	0	0	0	Output	Input	Output	Output
6	1	0	0	0	1	0	0	1	Output	Input	Output	Input
7	1	0	0	0	1	0	1	0	Output	Input	Input	Output
8	1	0	0	0	1	0	1	1	Output	Input	Input	Input
9	1	0	0	1	0	0	0	0	Input	Output	Output	Output
10	1	0	0	1	0	0	0	1	Input	Output	Output	Input
11	1	0	0	1	0	0	1	0	Input	Output	Input	Output
12	1	0	0	1	0	0	1	1	Input	Output	Input	Input
13	1	0	0	1	1	0	0	0	Input	Input	Output	Output
14	1	0	0	1	1	0	0	1	Input	Input	Output	Input
15	1	0	0	1	1	0	1	0	Input	Input	Input	Output
16	1	0	0	1	1	0	1	1	Input	Input	Input	Input

Note: When used in mode 0 for both groups A and B

■ I/O·MSM82C55A-2RS/GS/VJS ■

2. Mode 1 (Strobe input/output operation)

In mode 1, the strobe, interrupt and other control signals are used when input/output operations are made from a specified port. This mode is available for both groups A and B. In group A at this time, port A is used as the data line and port C as the control signal.

Following is a descrption of the input operation in mode 1.

$\overline{STB}$ (Strobe input)

- When this signal is low level, the data output from terminal to port is fetched into the internal latch of the port. This can be made independent from the CPU, and the data is not output to the data bus until the RD signal arrives from the CPU.

IBF (Input buffer full flag output)

- This is the response signal for the $\overline{STB}$. This signal when turned to high level indicates that data is fetched into the input latch. This signal turns to high level at the falling edge of $\overline{STB}$ and to low level at the rising edge of $\overline{RD}$.

INTR (Interrupt request output)

- This is the interrupt request signal for the CPU of the data fetched into the input latch. It is indicated by high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{STB}$ (IBF = 1 at this time) and low level at the falling edge of the $\overline{RD}$ when the INTE is set.

$INTE_A$ of group A is set when the bit for PC_4 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Following is a description of the output operation of mode 1.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data is written to the specified port upon receipt of the $\overline{WR}$ signal from the CPU. This signal turns to low level at the rising edge of the WR and high level at the falling edge of the ACK.

$\overline{ACK}$ (Acknowledge input)

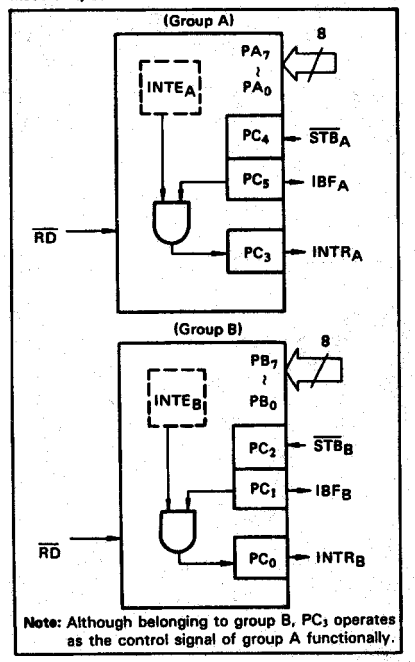
- This signal when turned to low level indicates that the terminal has received data.

INTR (Interrupt request output)

- This is the signal used to interrupt the CPU when a terminal receives data from the CPU via the MSM82C55A-5. It indicates the occurrence of the interrupt in high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{ACK}$ (OBF = 1 at this time) and low level at the falling edge of $\overline{WR}$ when the $INTE_B$ is set.

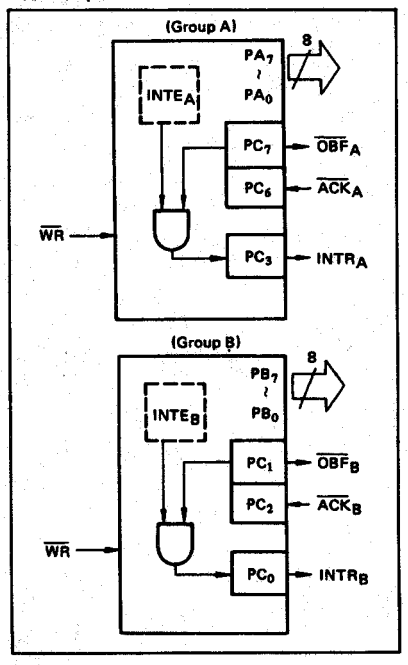
$INTE_A$ of group A is set when the bit for PC_6 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Mode 1 Input



Note: Although belonging to group B, PC_3 operates as the control signal of group A functionally.

Mode 1 output

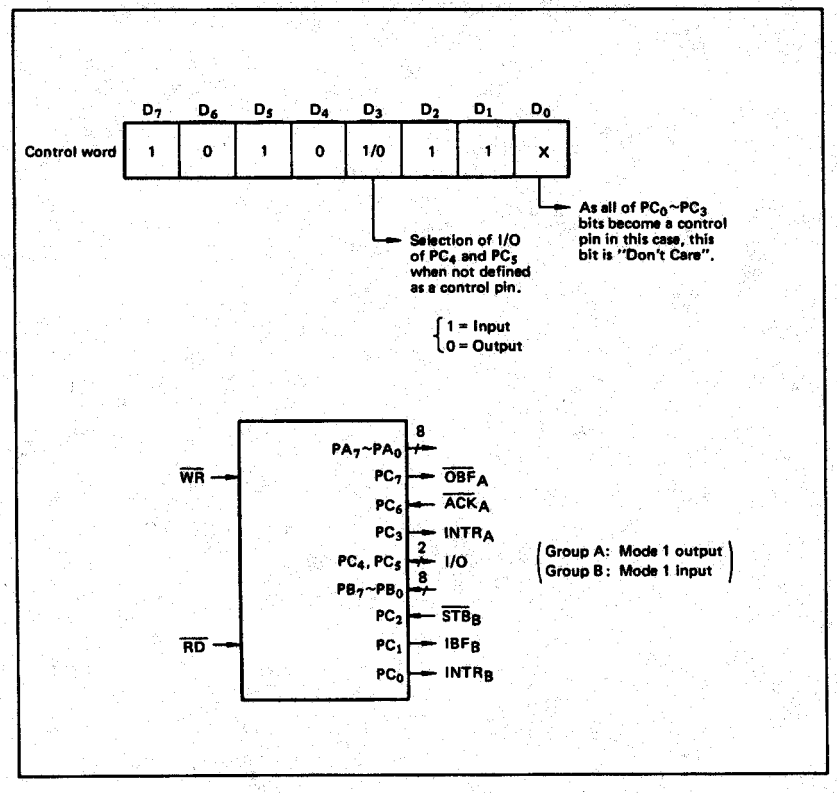


Port C Function Allocation in Mode 1

Port C \ Combination of Input/Output	Group A: Input Group B: Input	Group A: Input Group B: Output	Group A: Output Group B: Input	Group A: Output Group B: Output
PC_0	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$
PC_1	IBF_B	$\overline{OBF}_B$	IBF_B	$\overline{OBF}_B$
PC_2	$\overline{STB}_B$	$\overline{ACK}_B$	$\overline{STB}_B$	$\overline{ACK}_B$
PC_3	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	$\overline{STB}_A$	$\overline{STB}_A$	I/O	I/O
PC_5	IBF_A	IBF_A	I/O	I/O
PC_6	I/O	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	I/O	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

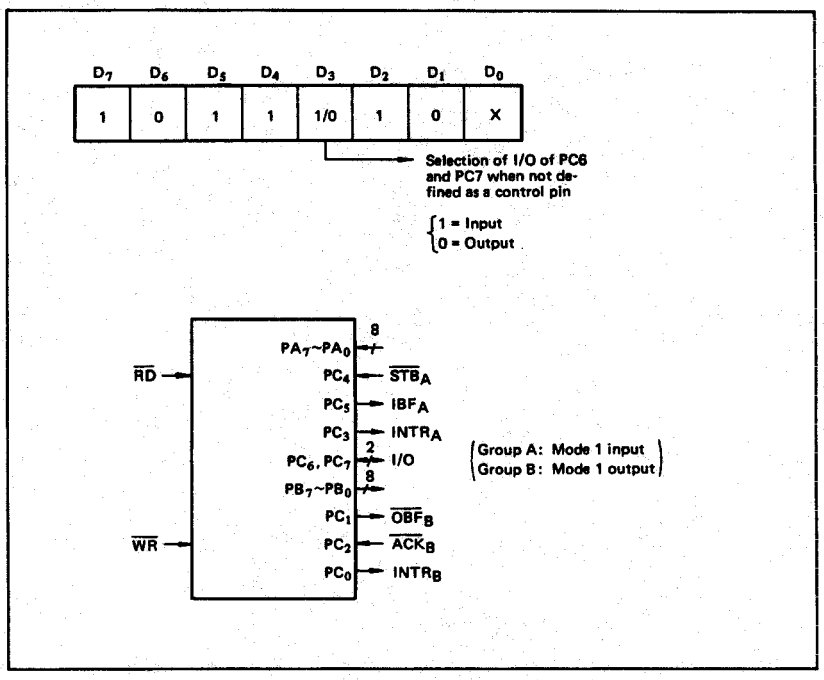
Note: I/O is a bit not used as the control signal, but it is available as a port of mode 0.

Examples of the relation between the control words and pins when used in mode 1 is shown below:
(a) When group A is mode 1 output and group B is mode 1 input.



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(b) When group A is mode 1 input and group B is mode 1 output.



3. Mode 2 (Strobe bidirectional bus I/O operation)

In mode 2, it is possible to transfer data in 2 directions through a single 8-bit port. This operation is akin to a combination between input and output operations. Port C waits for the control signal in this case, too. Mode 2 is available only for group A, however.

Next, a description is made on mode 2.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data has been written to the internal output latch upon receipt of the $\overline{WR}$ signal from the CPU. At this time, port A is still in the high impedance status and the data is not yet output to the outside. This signal turns to low level at the rising edge of the $\overline{WR}$ and high level at the falling edge of the $\overline{ACK}$.

$\overline{ACK}$ (Acknowledge input)

- When a low level signal is input to this pin, the high impedance status of port A is cleared, the buffer is enabled, and the data written to the internal output latch is output to port A. When the input returns to high level, port A is made into the high impedance status.

$\overline{STB}$ (Strobe input)

- When this signal turns to low level, the data output to the port from the pin is fetched into the internal input latch. The data is output to the data bus upon receipt of the RD signal from the CPU, but it remains in the high impedance status until then.

IBF (Input buffer full flag output)

- This signal when turned to high level indicates that data from the pin has been fetched into the input latch. This signal turns to high level at the falling edge of the $\overline{STB}$ and low level at the rising edge of the $\overline{RD}$.

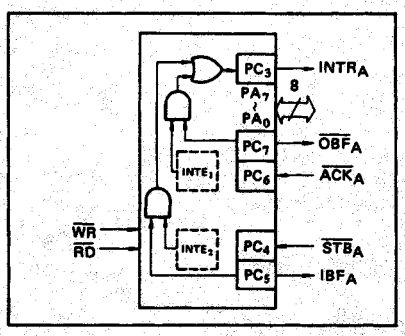
INTR (Interrupt request output)

- This signal is used to interrupt the CPU and its operation in the same as in mode 1. There are two INTE flip-flops internally available for input and output to select either interrupt of input or output operation. The INTE1 is used to control the interrupt request for output operation and it can be reset by the bit set for PC6. INTE2 is used to control the interrupt request for the input operation and it can be set by the bit set for PC4.

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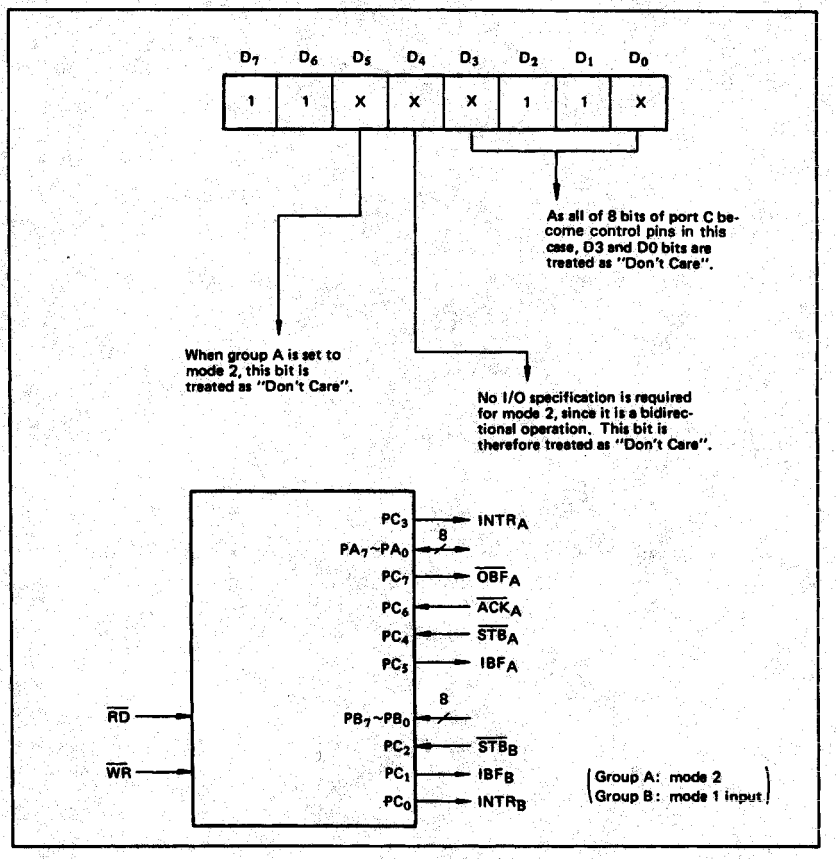
Mode 2 I/O Operation



Port C Function Allocation in Mode 2

Port C	Function
PC_0	Confirmed to the group B mode
PC_1	
PC_2	
PC_3	$INTR_A$
PC_4	$\overline{STB}_A$
PC_5	IBF_A
PC_6	$\overline{ACK}_A$
PC_7	$\overline{OBF}_A$

Following is an example of the relation between the control word and the pin when used in mode 2. When input in mode 2 for group A and in mode 1 for group B.



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4. When Group A is Different in Mode from Group B

Group A and group B can be used by setting them in different modes each other at the same time. When either group is set to mode1 or mode 2, it is possible to set the one not defined as a control pin in port C to both input and output as a port which operates in mode 0 at the 3rd and 0th bits of the control word.

(Mode combinations that define no control bit at port C)

	Group A	Group B	Port C							
			PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 0 output	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$\overline{STB}_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
			Controlled at the 3rd bit (D3) of the control word				Controlled at the 0th bit (D0) of the control word			

When the I/O bit is set to input in this case, it is possible to access data by the normal port C read operation.
When set to output, PC7 ~ PC4 bits can be accessed by the bit set/reset function only. Meanwhile, 3 bits from PC2 to PC0 can be accessed by normal write operation.

The bit set/reset function can be used for all of PC3 ~ PC0 bits. Note that the status of port C varies according to the combination of modes like this.

5. Port C Status Read

When port C is used for the control signal, that is, in either mode 1 or mode 2, each control signal and bus status signal can be read out by reading the content of port C.
The status read out is as follows:

	Group A	Group B	Status read on the data bus							
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 1 output	Mode 0	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$INTE_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	I/O	I/O	I/O
10	Mode 2	Mode 1 input	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
11	Mode 2	Mode 1 output	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$

6. Reset of MSM82C55A

Be sure to keep the RESET signal at power ON in the high level at least for 50 μs. Subsequently, it becomes the input mode at a high level pulse above 500 ns.

Note: Comparison of MSM82C55A-5 and MSM82C55A-2

MSM82C55A-5

After a write command is executed to the command register, the internal latch is cleared in PORTA PORTC. For instance, 00H is output at the beginning of a write command when the output port is assigned. However, if PORTB is not cleared at this time, PORTB is unstable. In other words, PORTB only outputs ineffective data (unstable value according to the device) during the period from after a write command is executed till the first data is written to PORTB.

MSM82C55A-2

After a write command is executed to the command register, the internal latch is cleared in All Ports(PORTA,PORTB,PORTC). 00H is ontput at the beginning of a write command when the output port is assigned.

Appendix E
Customer Communication

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve technical problems you might have as well as a form you can use to comment on the product documentation. Filling out a copy of the *Technical Support Form* before contacting National Instruments helps us help you better and faster.

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Hard disk capacity _____MB Brand _____

Instruments used _____

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Configuration _____

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Configuration _____

The problem is _____

_____

_____

_____

_____

List any error messages _____

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_____

_____

_____

The following steps will reproduce the problem _____

_____

_____

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Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

°	degrees
Ω	ohms
%	percent
A	amperes
A/D	analog-to-digital
ADC	A/D converter
AMD	Advanced Micro Devices
ANSI	American National Standards Institute
AWG	American Wire Gauge
BCD	binary-coded decimal
C	Celsius
CMOS	complementary metal-oxide semiconductor
D/A	digital-to-analog
DAC	D/A converter
DAQ	data acquisition
dB	decibels
DC	direct current
DMA	direct memory access
DOS	Disk Operating System
EPROM	erasable programmable read-only memory
F	farads
FIFO	first-in-first-out
ft	feet
hex	hexadecimal
Hz	hertz
I_{IH}	input current load, logic high input voltage
I_{IL}	input current load, logic low input voltage
in.	inches
I_{OH}	output source current, logic high
I_{OL}	output sink current, logic low
I/O	input/output

ksamples	1,000 samples
LED	light-emitting diode
LS	Low-power Schottky
LSB	least significant bit
MB	megabytes of memory
m	meters
MSB	most significant bit
PA	port A
PB	port B
PC	port C
PC	personal computer
PPI	programmable peripheral interface
ppm	parts per million
R_{EXT}	external resistance
rms	root mean square
RTSI	Real-Time System Integration
SCXI	System Conditioning eXtensions for Instrumentation
s	seconds
TTL	transistor-transistor logic
V	volts
V_{EXT}	external volts
V_{IH}	input logic high voltage
V_{IL}	input logic low voltage
V_{IN}	volts in
VI	virtual instrument

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