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Lab-PC+
User Manual

Low-Cost Multifunction I/O Board for ISA

June 1996 Edition

Part Number 320502B-01

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About This Manual

This manual describes the electrical and mechanical aspects of the Lab-PC+ and contains information concerning its operation and programming.

The Lab-PC+ is a low-cost multifunction analog, digital, and timing I/O board for PC compatible computers.

Organization of the *Lab-PC+ User Manual*

The *Lab-PC+ User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the Lab-PC+; lists what you need to get started; describes the optional software and optional equipment; and explains how to unpack the Lab-PC+.
- Chapter 2, *Configuration and Installation*, describes the Lab-PC+ jumper configuration and installation of the Lab-PC+ board in your computer.
- Chapter 3, *Signal Connections*, describes how to make input and output signal connections to your Lab-PC+ board via the board I/O connector.
- Chapter 4, *Theory of Operation*, contains a functional overview of the Lab-PC+ and explains the operation of each functional unit making up the Lab-PC+. This chapter also explains the basic operation of the Lab-PC+ circuitry.
- Chapter 5, *Calibration*, discusses the calibration procedures for the Lab-PC+ analog input and analog output circuitry.
- Appendix A, *Specifications*, lists the specifications of the Lab-PC+.
- Appendix B, *OKI 82C53 Data Sheet*, contains the manufacturer data sheet for the OKI 82C53 System Timing Controller integrated circuit (OKI Semiconductor). This circuit is used on the Lab-PC+.
- Appendix C, *OKI 82C55A Data Sheet*, contains the manufacturer data sheet for the OKI 82C55A Programmable Peripheral Interface integrated circuit (OKI Semiconductor). This circuit is used on the Lab-PC+.
- Appendix D, *Register Map and Descriptions*, describes in detail the address and function of each of the Lab-PC+ registers.
- Appendix E, *Register-Level Programming*, contains important information about programming the Lab-PC+.
- Appendix F, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products and manuals.

- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* contains an alphabetical list of key terms and topics used in this manual, including the page where each one can be found.

Conventions Used in This Manual

The following conventions appear in this manual.

8253	8253 refers to the OKI Semiconductor 82C53 System Timing Controller integrated circuit.
< >	Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name (for example, BDIO<3...0>).
bold	Bold text denotes the names of menus, menu items, parameters, dialog boxes, dialog box buttons or options, icons, windows [Windows OS], Windows 95 tabs or pages, or LEDs.
bold italic	Bold italic text denotes a note, caution, or warning.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept. This text denotes text for which you supply the appropriate word or value, such as in Windows 3.*x*.
`italic monospace`	Italic text in this font denotes that you must supply the appropriate words or values in the place of these items.
`monospace`	Bold text in this font denotes the messages and responses that the computer automatically prints to the screen. This font also emphasizes lines of code that are unique from the other examples.
`monospace`	Text in this font denotes text or characters that you should literally enter from the keyboard, sections of code, programming examples, and syntax examples. This font also is used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions, and for statements and comments taken from program code.
NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles unless otherwise noted.
paths	Paths are denoted using backslashes (\) to separate drive names, directories, folders, and files.
[ ]	Square brackets enclose optional items (for example, [`response`]).

The *Glossary* lists abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms.

National Instruments Documentation

The Lab-PC+ User Manual is one piece of the documentation set for your DAQ system. You could have any of several types of manuals depending on the hardware and software in your system. Use the manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.
- Software documentation—Examples of software documentation you may have are the LabVIEW and LabWindows®/CVI documentation sets and the NI-DAQ documentation. After you set up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure your hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.
- SCXI chassis manuals—If you are using SCXI, read these manuals for maintenance information on the chassis and installation instructions.

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix F, *Customer Communication*, at the end of this manual.

Chapter 1
Introduction

This chapter describes the Lab-PC+; lists what you need to get started; describes the optional software and optional equipment; and explains how to unpack the Lab-PC+.

About the Lab-PC+

The Lab-PC+ is a low-cost multifunction analog, digital, and timing I/O board for the PC. The Lab-PC+ contains a 12-bit successive-approximation ADC with eight analog inputs, which can be configured as eight single-ended or four differential channels. The Lab-PC+ also has two12-bit DACs with voltage outputs, 24 lines of TTL-compatible digital I/O, and six 16-bit counter/timer channels for timing I/O.

The low cost of a system based on the Lab-PC+ makes it ideal for laboratory work in industrial and academic environments. The multichannel analog input is useful in signal analysis and data logging. The 12-bit ADC is useful in high-resolution applications such as chromatography, temperature measurement, and DC voltage measurement. The analog output channels can be used to generate experiment stimuli and are also useful for machine and process control and analog function generation. The 24 TTL-compatible digital I/O lines can be used for switching external devices such as transistors and solid-state relays, for reading the status of external digital logic, and for generating interrupts. The counter/timers can be used to synchronize events, generate pulses, and measure frequency and time. The Lab-PC+, used in conjunction with the PC, is a versatile, cost-effective platform for laboratory test, measurement, and control.

Detailed specifications of the Lab-PC+ are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your Lab-PC+ board, you will need the following:

- ❑ Lab-PC+ board
- ❑ *Lab-PC+ User Manual*
- ❑ One of the following software packages and documentation:
  - NI-DAQ for PC compatibles
  - LabVIEW
  - LabWindows/CVI
- ❑ Your computer

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use LabVIEW, LabWindows/CVI, NI-DAQ, or register-level programming.

LabVIEW and LabWindows/CVI Application Software

LabVIEW and LabWindows/CVI are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows/CVI enhances traditional programming languages. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Libraries are functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition libraries are functionally equivalent to the NI-DAQ software.

Using LabVIEW or LabWindows/CVI software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with signal conditioning or accessory products. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation (timed D/A conversion), digital I/O, counter/timer operations, SCXI, RTSI, calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages, LabVIEW, or LabWindows/CVI, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

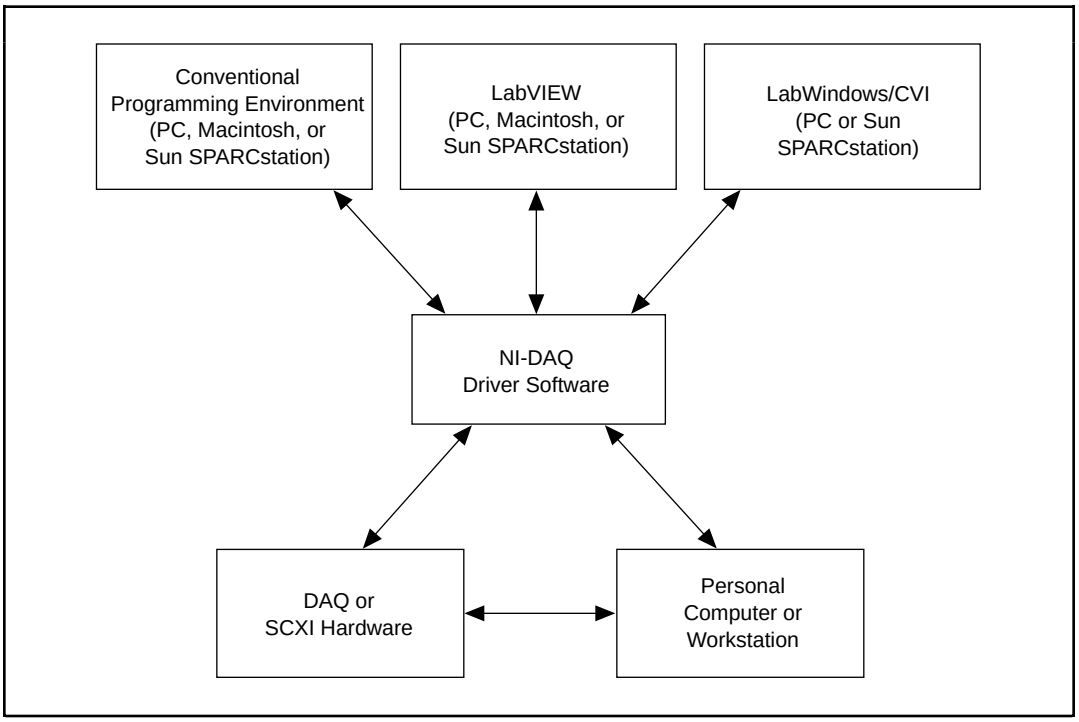


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

You can use your Lab-PC+ board, together with other PC, AT, EISA, DAQCard, and DAQPad Series DAQ and SCXI hardware, with NI-DAQ software for PC compatibles.

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using NI-DAQ, LabVIEW, or LabWindows/CVI to program your National Instruments DAQ hardware. Using the NI-DAQ, LabVIEW, or LabWindows/CVI software is as easy and as flexible as register-level programming and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with your Lab-PC+ board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50, 68, and 100-pin screw terminals
- Real Time System Integration (RTSI) bus cables
- Signal Condition eXtension for Instrumentation (SCXI) modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3072 channels.
- Low channel count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For more specific information about these products, refer to your National Instruments catalogue or call the office nearest you.

Unpacking

Your Lab-PC+ board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components on the board. To avoid such damage in handling the board, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.

Chapter 2
Configuration and Installation

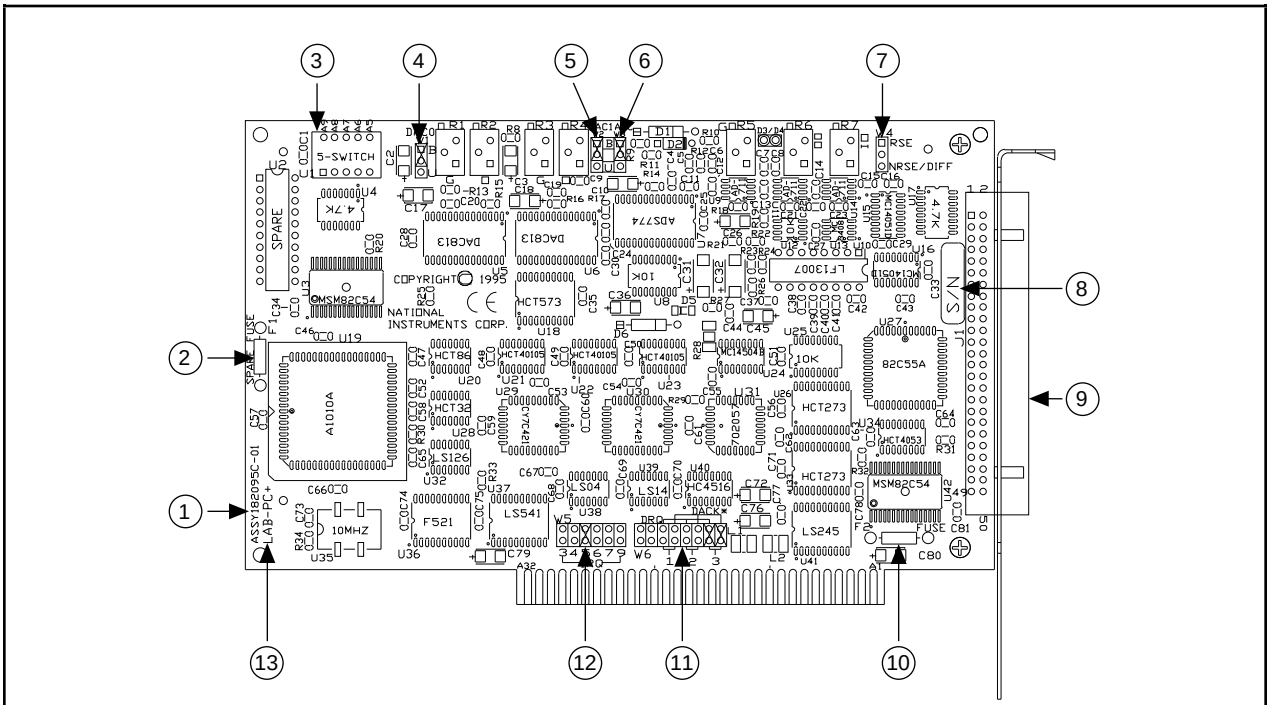
This chapter describes the Lab-PC+ jumper configuration and installation of the Lab-PC+ board in your computer.

Board Configuration

The Lab-PC+ contains six jumpers and one DIP switch to configure the PC bus interface and analog I/O settings. The DIP switch is used to set the base I/O address. Two jumpers are used as interrupt channel and DMA selectors. The remaining four jumpers are used to change the analog input and analog output circuitry. The parts locator diagram in Figure 2-1 shows the Lab-PC+ jumper settings. Jumpers W3 and W4 configure the analog input circuitry. Jumpers W1 and W2 configure the analog output circuitry. Jumpers W6 and W5 select the DMA channel and the interrupt level, respectively.

PC Bus Interface

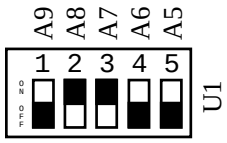
The Lab-PC+ is configured at the factory to a base I/O address of hex 260, to use DMA Channel 3, and to use interrupt level 5. These settings (shown in Table 2-1) are suitable for most systems. If your system, however, has other hardware at this base I/O address, DMA channel, or interrupt level, you will need to change these settings on the other hardware or on the Lab-PC+ as described in the following pages. Record your settings in the *Lab-PC+ Hardware and Software Configuration Form* in Appendix F.



1	Assembly Number	5	W2	8	Serial Number	11	W6
2	Spare Fuse	6	W3	9	J1	12	W5
3	U1	7	W4	10	Fuse	13	Product Name
4	W1						

Figure 2-1. Parts Locator Diagram

Table 2-1. PC Bus Interface Factory Settings

Lab-PC+ Board	Default Settings	Hardware Implementation
Base I/O Address	Hex 260	
DMA Channel	DMA Channel 3 (factory setting)	W6: DRQ3, DACK*3
Interrupt Level	Interrupt level 5 selected (factory setting)	W5: Row 5

Note: ***The shaded portion indicates the side of the switch that is pressed down.***

Base I/O Address Selection

The base I/O address for the Lab-PC+ is determined by the switches at position U1 (see Figure 2-1). The switches are set at the factory for the base I/O address hex 260. This factory setting is used as the default base I/O address value by National Instruments software packages for use with the Lab-PC+. The Lab-PC+ uses the base I/O address space hex 260 through 27F with the factory setting.

Note: ***Verify that this space is not already used by other equipment installed in your computer. If any equipment in your computer uses this base I/O address space, you must change the base I/O address of the Lab-PC+ or of the other device. If you change the Lab-PC+ base I/O address, you must make a corresponding change to any software packages you use with the Lab-PC+. For more information about your computer's I/O, refer to your computer's technical reference manual.***

Each switch in U1 corresponds to one of the address lines A9 through A5. Press the side marked OFF to select a binary value of 1 for the corresponding address bit. Press the other side of the switch to select a binary value of 0 for the corresponding address bit. Figure 2-2 shows two possible switch settings.

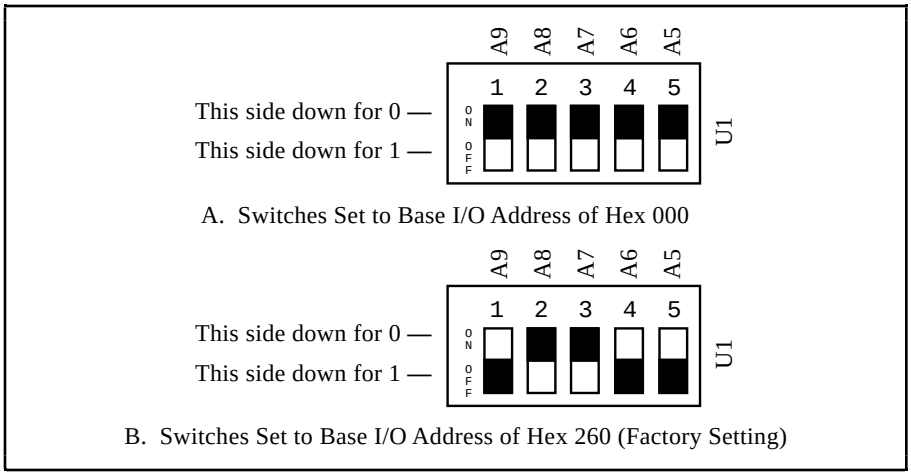


Figure 2-2. Example Base I/O Address Switch Settings

The five least significant bits of the address (A4 through A0) are decoded by the Lab-PC+ to select the appropriate Lab-PC+ register. To change the base I/O address, remove the plastic cover on U1; press each switch to the desired position; check each switch to make sure the switch is pressed down all the way; and replace the plastic cover. Record the new Lab-PC+ base I/O address in Appendix F, *Customer Communication,* for use when configuring the Lab-PC+ software.

Table 2-2 lists the possible switch settings, the corresponding base I/O address, and the base I/O address space used for that setting.

Table 2-2. Switch Settings with Corresponding Base I/O Address and Base I/O Address Space

Switch Setting A9	A8	A7	A6	A5	Base I/O Address (hex)	Base I/O Address Space Used (hex)
0	0	0	0	0	000	000 - 01F
0	0	0	0	1	020	020 - 03F
0	0	0	1	0	040	040 - 05F
0	0	0	1	1	060	060 - 07F
0	0	1	0	0	080	080 - 09F
0	0	1	0	1	0A0	0A0 - 0BF
0	0	1	1	0	0C0	0C0 - 0DF
0	0	1	1	1	0E0	0E0 - 0FF
0	1	0	0	0	100	100 - 11F
0	1	0	0	1	120	120 - 13F
0	1	0	1	0	140	140 - 15F
0	1	0	1	1	160	160 - 17F
0	1	1	0	0	180	180 - 19F
0	1	1	0	1	1A0	1A0 - 1BF
0	1	1	1	0	1C0	1C0 - 1DF
0	1	1	1	1	1E0	1E0 - 1FF
1	0	0	0	0	200	200 - 21F
1	0	0	0	1	220	220 - 23F
1	0	0	1	0	240	240 - 25F
1	0	0	1	1	260	260 - 27F
1	0	1	0	0	280	280 - 29F
1	0	1	0	1	2A0	2A0 - 2BF
1	0	1	1	0	2C0	2C0 - 2DF
1	0	1	1	1	2E0	2E0 - 2FF
1	1	0	0	0	300	300 - 31F
1	1	0	0	1	320	320 - 33F
1	1	0	1	0	340	340 - 35F
1	1	0	1	1	360	360 - 37F
1	1	1	0	0	380	380 - 39F
1	1	1	0	1	3A0	3A0 - 3BF
1	1	1	1	0	3C0	3C0 - 3DF
1	1	1	1	1	3E0	3E0 - 3FF

Note:*Base I/O address values hex 000 through 0FF are reserved for system use. Base I/O address values hex 100 through 3FF are available on the I/O channel.*

DMA Channel Selection

The Lab-PC+ uses the DMA channel selected by jumpers on W6 (see Figure 2-1). The Lab-PC+ is set at the factory to use DMA Channel 3. This is the default DMA channel used by the Lab-PC+ software handler. Verify that other equipment already installed in your computer does not use this DMA channel. If any device uses DMA Channel 3, change the DMA channel used by either the Lab-PC+ or the other device. The Lab-PC+ hardware can use DMA Channels 1, 2, and 3. Notice that these are the three 8-bit channels on the PC I/O channel. The Lab-PC+ *does not* use and *cannot* be configured to use the 16-bit DMA channels on the PC AT I/O channel.

Each DMA channel consists of two signal lines as shown in Table 2-3.

Table 2-3. DMA Channels for the Lab-PC+

DMA Channel	DMA Acknowledge	DMA Request
1	DACK1	DRQ1
2	DACK2	DRQ2
3	DACK3	DRQ3
Note: ***In most personal computers DMA Channel 2 is reserved for the disk drives. Therefore, you should avoid using this channel.***		

Two jumpers must be installed to select a DMA channel. The DMA Acknowledge and DMA Request lines selected must have the same number suffix for proper operation. Figure 2-3 displays the jumper positions for selecting DMA Channel 3.

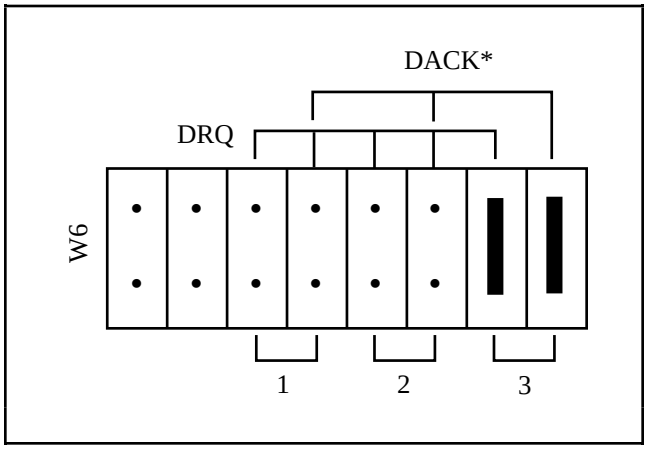


Figure 2-3. DMA Jumper Settings for DMA Channel 3 (Factory Setting)

If you do not want to use DMA for Lab-PC+ transfers, then place the configuration jumpers on W6 in the position shown in Figure 2-4.

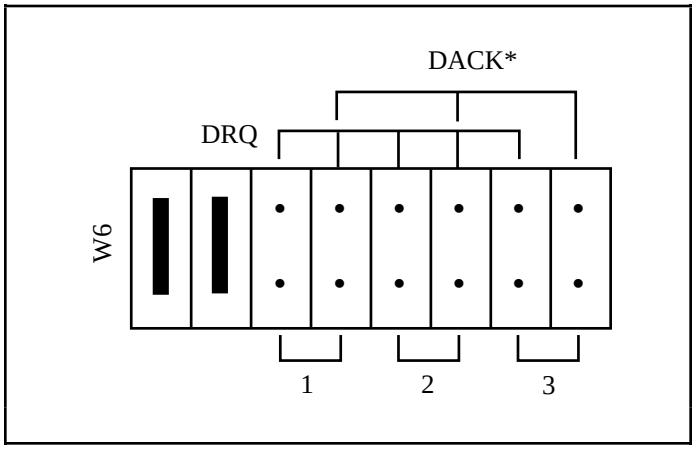


Figure 2-4. DMA Jumper Settings for Disabling DMA Transfers

Interrupt Selection

The Lab-PC+ board can connect to any one of the six interrupt lines of the PC I/O channel. The interrupt line is selected by a jumper on one of the double rows of pins located above the I/O slot edge connector on the Lab-PC+ (refer to Figure 2-1). To use the interrupt capability of the Lab-PC+, you must select an interrupt line and place the jumper in the appropriate position to enable that particular interrupt line.

The Lab-PC+ can share interrupt lines with other devices by using a tristate driver to drive its selected interrupt line. The Lab-PC+ hardware supports interrupt lines IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, and IRQ9.

Note: ***Do not use interrupt line 6. Interrupt line 6 is used by the diskette drive controller on most IBM PC and compatible computers.***

Once you have selected an interrupt level, place the interrupt jumper on the appropriate pins to enable the interrupt line.

The interrupt jumper set is W5. The default interrupt line is IRQ5, which you select by placing the jumper on the pins in row 5. Figure 2-5 shows the default interrupt jumper setting IRQ5. To change to another line, remove the jumper from IRQ5 and place it on the new pins.

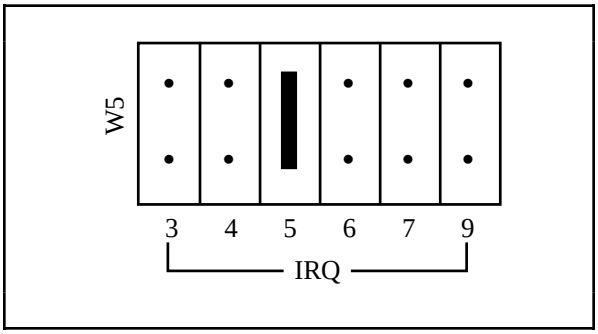


Figure 2-5. Interrupt Jumper Setting IRQ5 (Factory Setting)

If you do not want to use interrupts, place the jumper on W5 in the position shown in Figure 2-6. This setting disables the Lab-PC+ from asserting an interrupt line on the PC I/O channel.

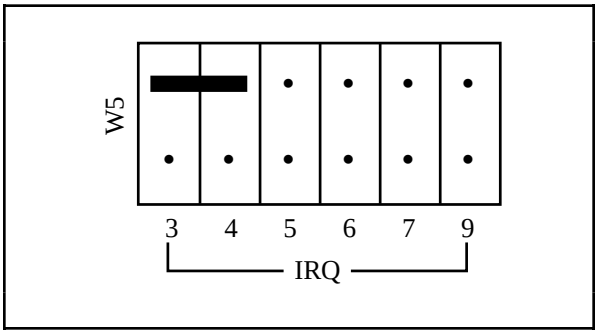


Figure 2-6. Interrupt Jumper Setting for Disabling Interrupts

Analog I/O Configuration

The Lab-PC+ is shipped from the factory with the following configuration:

- Referenced single-ended input mode
- ±5 V input range
- Bipolar analog output
- ±5 V output range

Table 2-4 lists all the available analog I/O jumper configurations for the Lab-PC+ with the factory settings noted.

Table 2-4. Analog I/O Jumper Settings

Parameter	Configuration	Jumper Settings
Output CH0 Polarity	Bipolar: ±5 V (factory setting) Unipolar: 0 to 10 V	W1: A-B W1: B-C
Output CH1 Polarity	Bipolar: ±5 V (factory setting) Unipolar: 0 to 10 V	W2: A-B W2: B-C
Input Range	Bipolar: ±5 V (factory setting) Unipolar: 0 to 10 V	W3: A-B W3: B-C
Input Mode	Referenced single-ended (RSE) (factory setting) Nonreferenced single-ended (NRSE) Differential (DIFF)	W4: A-B W4: B-C W4: B-C

Analog Output Configuration

Two ranges are available for the analog outputs–bipolar: ±5 V and unipolar: 0 to 10 V. Jumper W1 controls output Channel 0, and W2 controls output Channel 1.

Bipolar Output Selection

You can select the bipolar (±5 V) output configuration for either analog output channel by setting the following jumpers:

Analog Output Channel 0	W1	A-B
Analog Output Channel 1	W2	A-B

This configuration is shown in Figure 2-7.

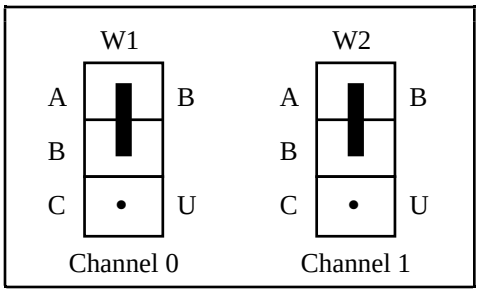


Figure 2-7. Bipolar Output Jumper Configuration (Factory Setting)

Unipolar Output Selection

You can select the unipolar (0 V to 10 V) output configuration for either analog output channel by setting the following jumpers:

Analog Output Channel 0	W1	B-C
Analog Output Channel 1	W2	B-C

This configuration is shown in Figure 2-8.

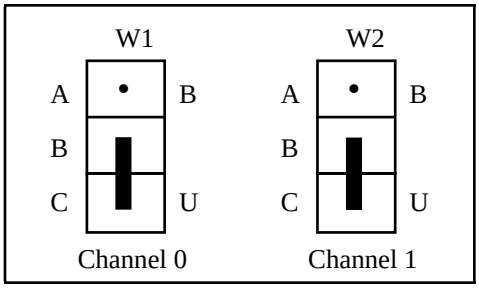


Figure 2-8. Unipolar Output Jumper Configuration

Analog Input Configuration

You can select different analog input configurations by using the jumper and register bit (software) settings as shown in Table 2-4. The following sections describe each of the analog input categories in detail.

Input Mode

The Lab-PC+ features three different input modes–referenced single-ended (RSE) input, non-referenced single-ended (NRSE) input, and differential (DIFF) input. The single-ended input configurations use eight channels. The DIFF input configuration uses four channels. These configurations are described in Table 2-5.

Table 2-5. Input Configurations Available for the Lab-PC+

Configuration	Description
DIFF	Differential configuration provides four differential inputs with the positive (+) input of the instrumentation amplifier tied to Channels 0, 2, 4, or 6 and the negative (-) input tied to Channels 1, 3, 5, or 7 respectively, thus choosing channel pairs (0,1), (2,3), (4,5), or (6,7).
NRSE	Non-referenced single-ended configuration provides eight single-ended inputs with the negative input of the instrumentation amplifier tied to AISENSE/AIGND and not connected to ground.
RSE	Referenced single-ended configuration provides eight single-ended inputs with the negative input of the instrumentation amplifier referenced to analog ground.

While reading the following paragraphs, you may find it helpful to refer to *Analog Input Signal Connections* in Chapter 3, *Signal Connections*, which contains diagrams showing the signal paths for the three configurations.

DIFF Input (Four Channels)

DIFF input means that each input signal has its own reference, and the difference between each signal and its reference is measured. The signal and its reference are each assigned an input channel. With this input configuration, the Lab-PC+ can monitor four differential analog input signals. To select the DIFF mode, you must set the $\overline{SE}$/D bit as described in the Command Register 4 bit description in Appendix D, *Register Map and Descriptions*. You must also set the following jumper.

W4: B-C Jumper is in stand-by position, and negative input of instrumentation amplifier is tied to multiplexer output.

This configuration is shown in Figure 2-9.

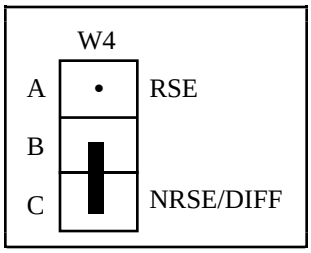


Figure 2-9. DIFF Input Configuration

Considerations in using the DIFF configuration are discussed in Chapter 3, *Signal Connections*. Note that the signal return path is through the negative terminal of the amplifier and through Channels 1, 3, 5, or 7, depending on which channel pair was selected.

RSE Input (Eight Channels, Factory Setting)

RSE input means that all input signals are referenced to a common ground point that is also tied to the analog input ground of the Lab-PC+. The negative input of the differential amplifier is tied to analog ground. This configuration is useful when measuring floating signal sources. See *Types of Signal Sources* in Chapter 3, *Signal Connections*. With this input configuration, the Lab-PC+ can monitor eight different analog input channels. To select the RSE input configuration, clear the SE/D bit as described in the Command Register 4 bit description in Appendix D, *Register Map and Descriptions*. You must also set the following jumper.

W4: A-B Jumper connects the negative input of the instrumentation amplifier to analog ground.

This configuration is shown in Figure 2-10.

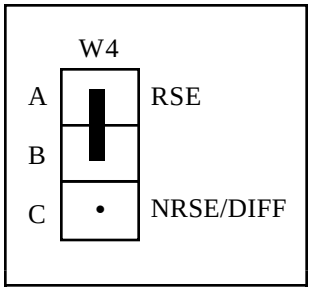


Figure 2-10. RSE Input Configuration

Considerations in using the RSE configuration are discussed in Chapter 3, *Signal Connections*. Note that in this mode, the return path of the signal is analog ground, available at the connector through pin AISENSE/AIGND.

NRSE Input (Eight Channels)

NRSE input means that all input signals are referenced to the same common mode voltage, which is allowed to float with respect to the analog ground of the Lab-PC+ board. This common mode voltage is subsequently subtracted out by the input instrumentation amplifier. This configuration is useful when measuring ground-referenced signal sources. To select the NRSE input configuration, clear the SE/D bit as described in the Command Register 4 bit description in Appendix D, *Register Map and Descriptions*. You must also set the following jumper.

W4: B-C Jumper is in standby position, and negative input of instrumentation amplifier is tied to multiplexed output.

This configuration is shown in Figure 2-11.

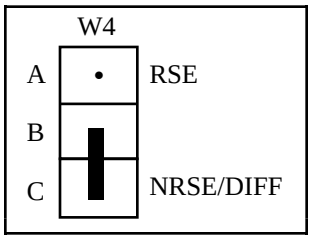


Figure 2-11. NRSE Input Configuration

Considerations in using the NRSE configuration are discussed in Chapter 3, *Signal Connections*. Note that in this mode, the return path of the signal is through the negative terminal of the amplifier, available at the connector through the pin AISENSE/AIGND.

Analog Input Polarity Configuration

Two ranges are available for the analog inputs–bipolar ±5 V and unipolar 0 to 10 V. Jumper W3 controls the input range for all eight analog input channels.

Bipolar Input Selection

You can select the bipolar (±5 V) input configuration by setting the following jumper:

Analog Input W3 A-B

This configuration is shown in Figure 2-12.

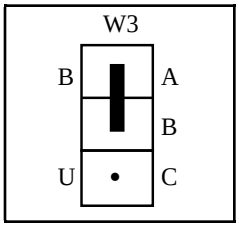


Figure 2-12. Bipolar Input Jumper Configuration (Factory Setting)

Unipolar Input Selection

You can select the unipolar (0 to 10 V) input configuration by setting the following jumper:

Analog Input W3 B-C

This configuration is shown in Figure 2-13.

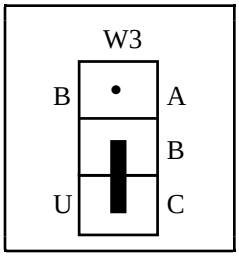


Figure 2-13. Unipolar Input Jumper Configuration

Note: ***If you are using a software package such as NI-DAQ or LabWindows/CVI, you may need to reconfigure your software to reflect any changes in jumper or switch settings.***

Hardware Installation

The Lab-PC+ can be installed in any available 8-bit or 16-bit expansion slot in your computer. After you have changed (if necessary), verified, and recorded the switches and jumper settings, you are ready to install the Lab-PC+. The following are general installation instructions, but consult your PC user manual or technical reference manual for specific instructions and warnings.

1. Turn off your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Insert the Lab-PC+ into an 8-bit or a 16-bit slot.
5. Screw the mounting bracket of the Lab-PC+ to the back panel rail of the computer.
6. Check the installation.
7. Replace the cover.

The Lab-PC+ board is installed. You are now ready to install and configure your software.

If you are using NI-DAQ, refer to your NI-DAQ release notes. Find the installation and system configuration section for your operating system and follow the instructions given there.

If you are using LabVIEW, the software installation instructions are in your LabVIEW release notes.

If you are using LabWindows/CVI, the software installation instructions are in your LabWindows/CVI release notes.

If you are a register-level programmer, refer to Appendix E, *Register-Level Programming.*

Chapter 3
Signal Connections

This chapter describes how to make input and output signal connections to your Lab-PC+ board via the board I/O connector.

I/O Connector Pin Description

Figure 3-1 shows the pin assignments for the Lab-PC+ I/O connector. This connector is located on the back panel of the Lab-PC+ board and is accessible at the rear of the PC after the board has been properly installed.

Warning: ***Connections that exceed any of the maximum ratings of input or output signals on the Lab-PC+ may result in damage to the Lab-PC+ board and to the computer. This includes connecting any power signals to ground and vice versa. National Instruments is NOT liable for any damages resulting from any such signal connections.***

ACH0	1	2	ACH1
ACH2	3	4	ACH3
ACH4	5	6	ACH5
ACH6	7	8	ACH7
AISENSE/AIGND	9	10	DAC0 OUT
AGND	11	12	DAC1 OUT
DGND	13	14	PA0
PA1	15	16	PA2
PA3	17	18	PA4
PA5	19	20	PA6
PA7	21	22	PB0
PB1	23	24	PB2
PB3	25	26	PB4
PB5	27	28	PB6
PB7	29	30	PC0
PC1	31	32	PC2
PC3	33	34	PC4
PC5	35	36	PC6
PC7	37	38	EXTTRIG
EXTUPDATE*	39	40	EXTCONV*
OUTB0	41	42	GATB0
COUTB1	43	44	GATB1
CCLKB1	45	46	OUTB2
GATB2	47	48	CLKB2
+5 V	49	50	DGND

Figure 3-1. Lab-PC+ I/O Connector Pin Assignments

Signal Connection Descriptions

The following list describes the connector pins on the Lab-PC+ I/O connector by pin number and gives the signal name and the significance of each signal connector pin.

Pin	Signal Name	Description
1-8	ACH0 through ACH7	Analog input Channels 0 through 7 (single-ended).
9	AISENSE/AIGND	Analog input ground in RSE mode, AISENSE in NRSE mode. Bi-directional.
10	DAC0 OUT	Voltage output signal for analog output Channel 0.
11	AGND	Analog ground. Analog output ground for analog output mode. Analog input ground for DIFF or NRSE mode. Bi-directional.
12	DAC1 OUT	Voltage output signal for analog output Channel 1.
13	DGND	Digital ground. Output.
14-21	PA0 through PA7	Bidirectional data lines for Port A. PA7 is the MSB, PA0 the LSB.
22-29	PB0 through PB7	Bidirectional data lines for Port B. PB7 is the MSB, PB0 the LSB.
30-37	PC0 through PC7	Bidirectional data lines for Port C. PC7 is the MSB, PC0 the LSB.
38	EXTTRIG	External control signal to start a timed conversion sequence. Input.
39	EXTUPDATE*	External control signal to update DAC outputs. Input.
40	EXTCONV*	External control signal to trigger A/D conversions. Bi-directional.
41	OUTB0	Counter B0 output.
42	GATB0	Counter B0 gate. Input.
43	COUTB1	Counter B1 output or pulled high (selectable).
44	GATB1	Counter B1 gate. Input.
45	CCLKB1	Counter B1 clock (selectable). Input.
46	OUTB2	Counter B2 output.
47	GATB2	Counter B2 gate. Input.
48	CLKB2	Counter B2 clock. Input.
49	+5V	+5 V out, 1 A maximum. Output.
50	DGND	Digital ground. Output.
*Indicates that the signal is active low.		

The connector pins can be grouped into analog input signal pins, analog output signal pins, digital I/O signal pins, and timing I/O signal pins. Signal connection guidelines for each of these groups are included later in this chapter.

Analog Input Signal Connections

Pins 1 through 8 are analog input signal pins for the 12-bit ADC. Pin 9, AISENSE/AIGND, is an analog common signal. This pin can be used for a general analog power ground tie to the Lab-PC+ in RSE mode, or as a return path in DIFF or NRSE mode. Pins 1 through 8 are tied to the eight single-ended analog input channels of the input multiplexer through 4.7 kΩ series resistances. Pins 2, 4, 6, and 8 are also tied to an input multiplexer for DIFF mode. Pin 40 is EXTCONV* and can be used to trigger conversions. A conversion occurs when this signal makes a high-to-low transition.

The following input ranges and maximum ratings apply to inputs ACH<0..7>:

Input signal range	Bipolar input: ±(5/gain) V Unipolar input: 0 to (10/gain) V
Maximum input voltage rating	±45 V powered on or off

Exceeding the input signal range for gain settings greater than 1 will not damage the input circuitry as long as the maximum input voltage rating of ±45 V is not exceeded. For example with a gain of 10, the input signal range is ±0.5 V for bipolar input and 0 to 1V for unipolar input, but the Lab-PC+ is guaranteed to withstand inputs up to the maximum input voltage rating.

Warning: ***Exceeding the input signal range results in distorted input signals. Exceeding the maximum input voltage rating may cause damage to the Lab-PC+ board and to the computer. National Instruments is NOT liable for any damages resulting from such signal connections.***

Connection of analog input signals to the Lab-PC+ depends on the configuration of the Lab-PC+ analog input circuitry and the type of input signal source. With the different Lab-PC+ configurations, the Lab-PC+ instrumentation amplifier can be used in different ways. Figure 3-2 shows a diagram of the Lab-PC+ instrumentation amplifier.

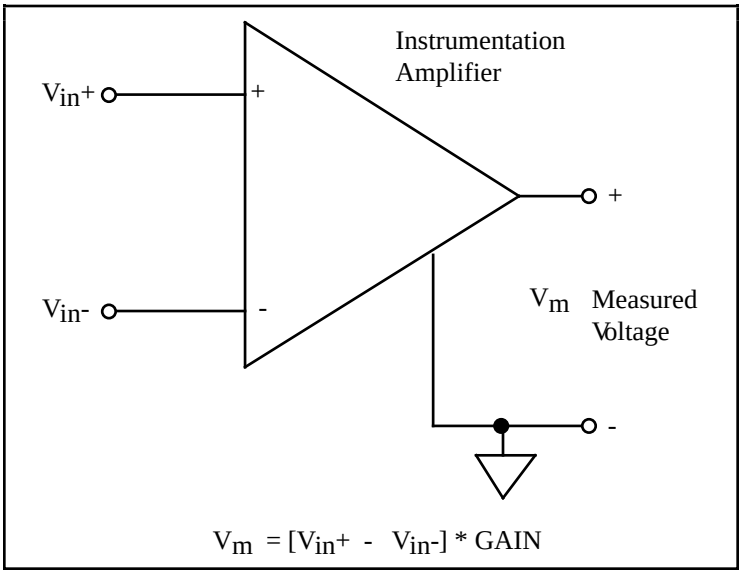


Figure 3-2. Lab-PC+ Instrumentation Amplifier

The Lab-PC+ instrumentation amplifier applies gain, common-mode voltage rejection, and high-input impedance to the analog input signals connected to the Lab-PC+ board. Signals are routed to the positive and negative inputs of the instrumentation amplifier through input multiplexers on the Lab-PC+. The instrumentation amplifier converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the Lab-PC+ ground. The Lab-PC+ ADC measures this output voltage when it performs A/D conversions.

All signals must be referenced to ground, either at the source device or at the Lab-PC+. If you have a floating source, you must use a ground-referenced input connection at the Lab-PC+. If you have a grounded source, you must use a non-referenced input connection at the Lab-PC+.

Types of Signal Sources

When configuring the input mode of the Lab-PC+ and making signal connections, you should first determine whether the signal source is floating or ground-referenced. These two types of signals are described as follows.

Floating Signal Sources

A floating signal source is one that is not connected in any way to the building ground system but rather has an isolated ground reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. The ground reference of a floating signal must be tied to the Lab-PC+ analog input ground in order to establish a local or onboard reference for the signal. Otherwise,

the measured input signal varies or appears to float. An instrument or device that provides an isolated output falls into the floating signal source category.

Ground-Referenced Signal Sources

A ground-referenced signal source is one that is connected in some way to the building system ground and is therefore already connected to a common ground point with respect to the Lab-PC+, assuming that the PC is plugged into the same power system. Non-isolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 mV and 100 mV but can be much higher if power distribution circuits are not properly connected. The connection instructions that follow for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Input Configurations

The Lab-PC+ can be configured for one of three input modes–NRSE, RSE, or DIFF. The following sections discuss the use of single-ended and differential measurements, and considerations for measuring both floating and ground-referenced signal sources. Table 3-1 summarizes the recommended input configurations for both types of signal sources.

Table 3-1. Recommended Input Configurations for Ground-Referenced and Floating Signal Sources

Type of Signal	Recommended Input Configuration
Ground-Referenced (non-isolated outputs, plug-in instruments)	DIFF NRSE
Floating (batteries, thermocouples, isolated outputs)	DIFF with bias resistors RSE

Differential Connection Considerations (DIFF Configuration)

Differential connections are those in which each Lab-PC+ analog input signal has its own reference signal or signal return path. These connections are available when the Lab-PC+ is configured in the DIFF mode. Each input signal is tied to the positive input of the instrumentation amplifier, and its reference signal, or return, is tied to the negative input of the instrumentation amplifier.

When the Lab-PC+ is configured for DIFF input, each signal uses two of the multiplexer inputs–one for the signal and one for its reference signal. Therefore, only four analog input channels are available when using the DIFF configuration. The DIFF input configuration should be used when any of the following conditions are present:

- Input signals are low-level (less than 1 V).
- Leads connecting the signals to the Lab-PC+ are greater than 15 ft.
- Any of the input signals requires a separate ground reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked-up noise and increase common mode signal and noise rejection. With these connections, input signals can float within the common mode limits of the input instrumentation amplifier.

Differential Connections for Grounded Signal Sources

Figure 3-3 shows how to connect a ground-referenced signal source to a Lab-PC+ board configured for DIFF input. Configuration instructions are included under *Analog Input Configuration* in Chapter 2, *Configuration and Installation*.

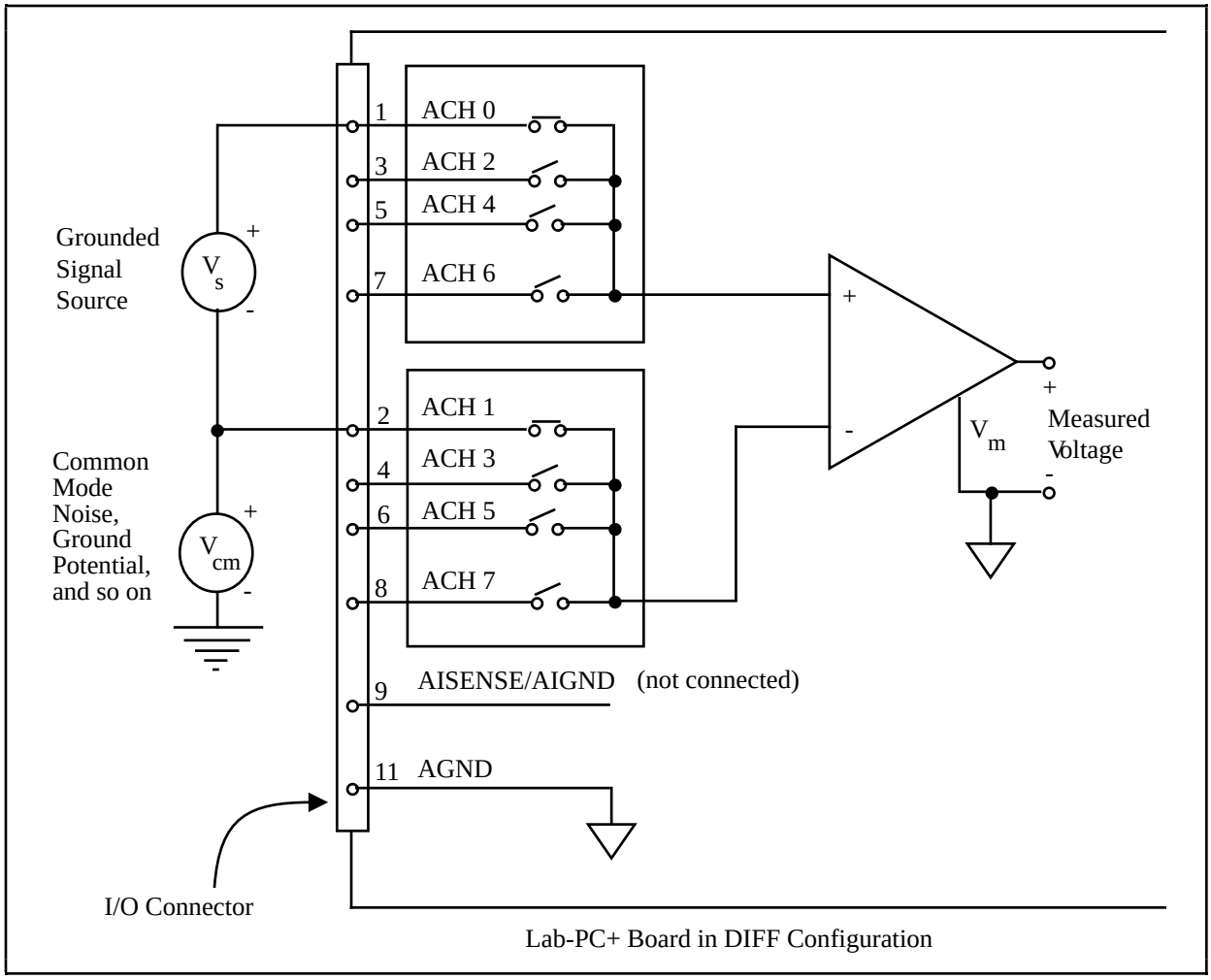


Figure 3-3. Differential Input Connections for Grounded Signal Sources

With this type of connection, the instrumentation amplifier rejects both the common mode noise in the signal and the ground potential difference between the signal source and the Lab-PC+ ground (shown as V_{cm} in Figure 3-3).

Differential Connections for Floating Signal Sources

Figure 3-4 shows how to connect a floating signal source to a Lab-PC+ board configured for DIFF input. Configuration instructions are included under *Analog Input Configuration* in Chapter 2, *Configuration and Installation*.

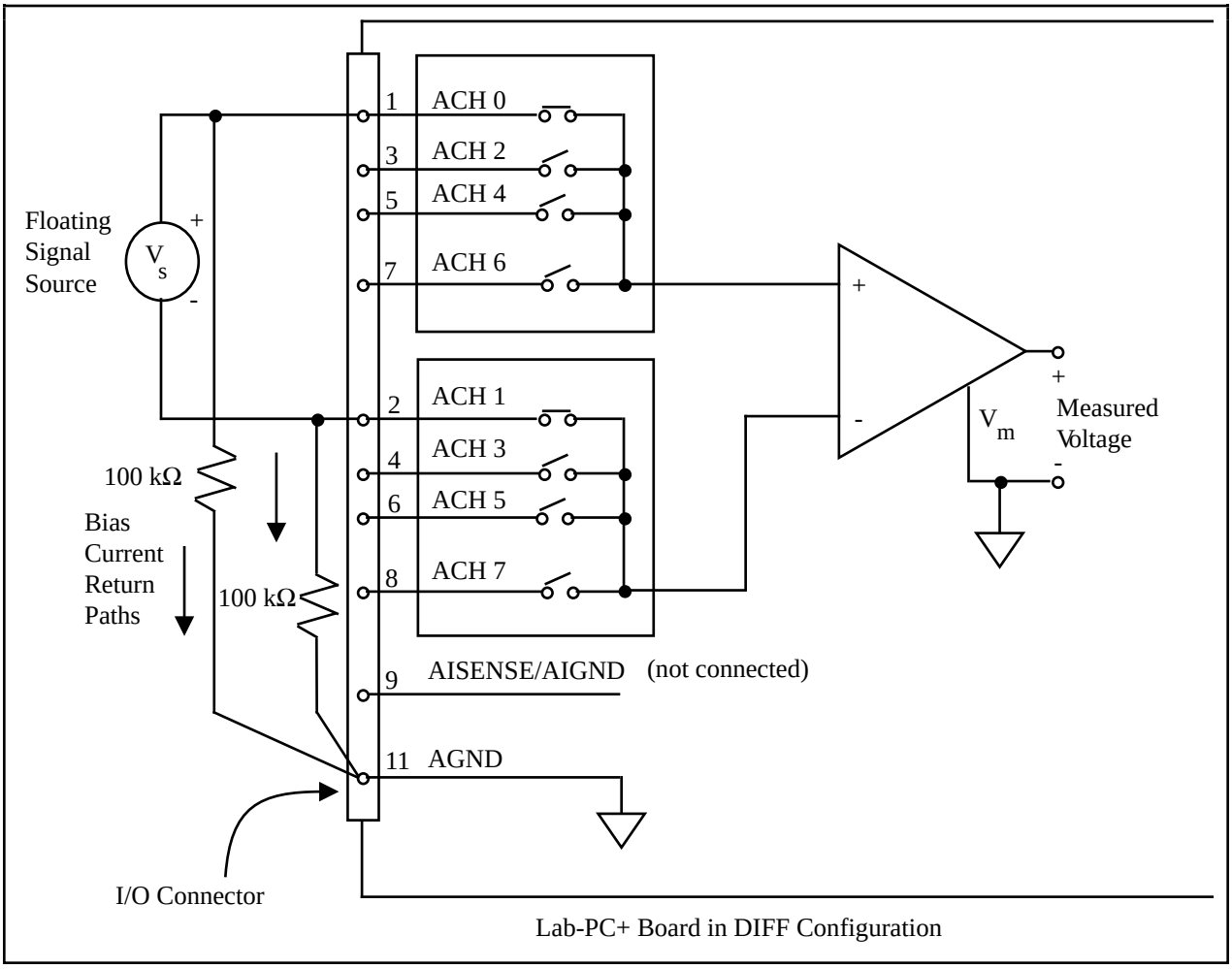


Figure 3-4. Differential Input Connections for Floating Sources

The 100 kΩ resistors shown in Figure 3-4 create a return path to ground for the bias currents of the instrumentation amplifier. If a return path is not provided, the instrumentation amplifier bias currents charge up stray capacitances, resulting in uncontrollable drift and possible saturation in the amplifier. Typically, values from 10 kΩ to 100 kΩ are used.

A resistor from each input to ground, as shown in Figure 3-4, provides bias current return paths for an AC-coupled input signal.

If the input signal is DC-coupled, then only the resistor connecting the negative signal input to ground is needed. This connection does not lower the input impedance of the analog input channel.

Single-Ended Connection Considerations

Single-ended connections are those in which all Lab-PC+ analog input signals are referenced to one common ground. The input signals are tied to the positive input of the instrumentation amplifier, and their common ground point is tied to the negative input of the instrumentation amplifier.

When the Lab-PC+ is configured for single-ended input (NRSE or RSE), eight analog input channels are available. Single-ended input connections can be used when the following criteria are met by all input signals:

1. Input signals are high-level (greater than 1 V).

2. Leads connecting the signals to the Lab-PC+ are less than 15 ft.

3. All input signals share a common reference signal (at the source).

If any of the preceding criteria are not met, using DIFF input configuration is recommended.

You can jumper-configure the Lab-PC+ for two different types of single-ended connections: RSE configuration and NRSE configuration. The RSE configuration is used for floating signal sources; in this case, the Lab-PC+ provides the reference ground point for the external signal. The NRSE configuration is used for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the Lab-PC+ should not supply one.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 3-5 shows how to connect a floating signal source to a Lab-PC+ board configured for single-ended input. The Lab-PC+ analog input circuitry must be configured for RSE input to make these types of connections. Configuration instructions are included under *Analog Input Configuration* in Chapter 2, *Configuration and Installation*.

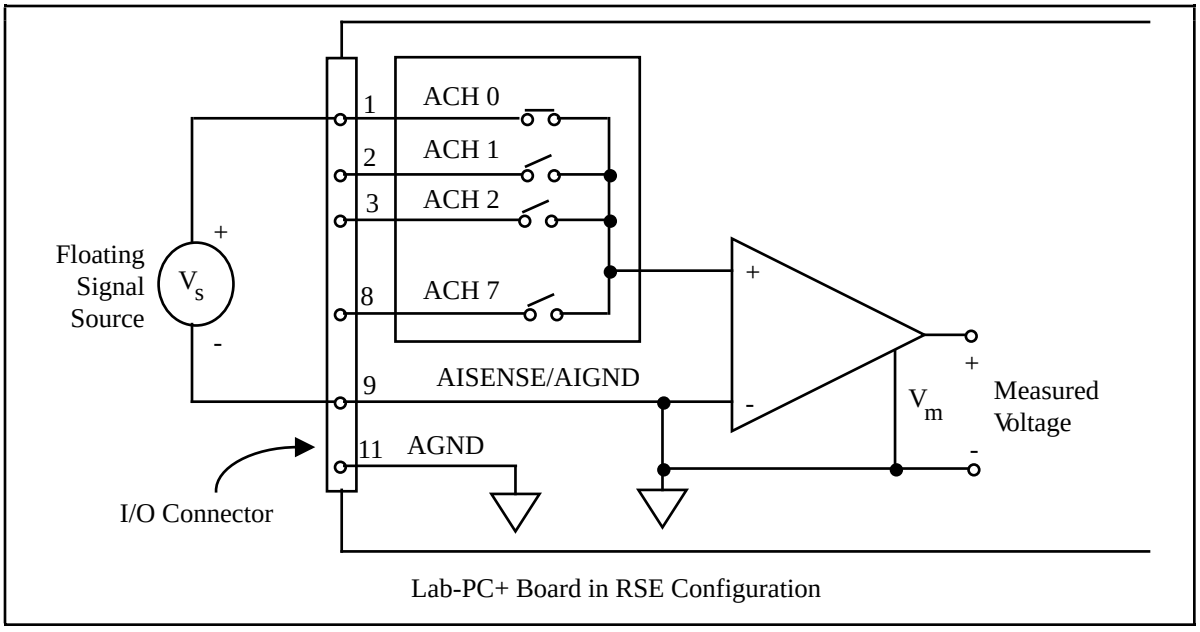


Figure 3-5. Single-Ended Input Connections for Floating Signal Sources

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

If a grounded signal source is to be measured with a single-ended configuration, then the Lab-PC+ must be configured in the NRSE input configuration. The signal is connected to the positive input of the Lab-PC+ instrumentation amplifier and the signal local ground reference is connected to the negative input of the Lab-PC+ instrumentation amplifier. The ground point of the signal should therefore be connected to the AISENSE pin. Any potential difference between the Lab-PC+ ground and the signal ground appears as a common mode signal at both the positive and negative inputs of the instrumentation amplifier and is therefore rejected by the amplifier. On the other hand, if the input circuitry of the Lab-PC+ is referenced to ground, such as in the RSE configuration, this difference in ground potentials appears as an error in the measured voltage.

Figure 3-6 shows how to connect a grounded signal source to a Lab-PC+ board configured in the NRSE configuration. Configuration instructions are included under *Analog Input Configuration* in Chapter 2, *Configuration and Installation*.

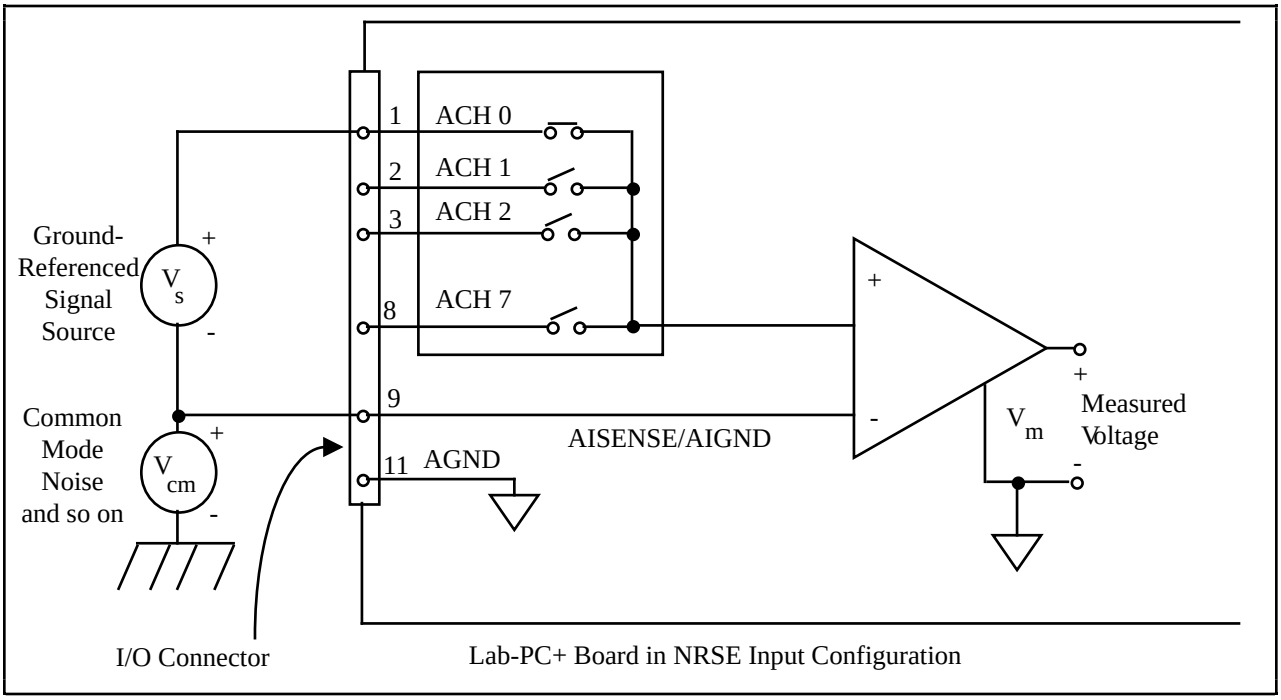


Figure 3-6. Single-Ended Input Connections for Grounded Signal Sources

Common-Mode Signal Rejection Considerations

Figures 3-3 and 3-6 show connections for signal sources that are already referenced to some ground point with respect to the Lab-PC+. In these cases, the instrumentation amplifier can reject any voltage due to ground potential differences between the signal source and the Lab-PC+. In addition, with differential input connections, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the Lab-PC+.

The common-mode input range of the Lab-PC+ instrumentation amplifier is defined as the magnitude of the greatest common-mode signal that can be rejected.

The common-mode input range for the Lab-PC+ depends on the size of the differential input signal ($V_{diff} = V^{+}_{in} - V^{-}_{in}$) and the gain setting of the instrumentation amplifier. In unipolar mode, the differential input range is 0 to 10 V. In bipolar mode, the differential input range is -5 to +5 V. Inputs should remain within a range of -5 to 10 V in both bipolar and unipolar modes.

Analog Output Signal Connections

Pins 10 through 12 of the I/O connector are analog output signal pins.

Pins 10 and 12 are the DAC0 OUT and DAC1 OUT signal pins. DAC0 OUT is the voltage output signal for Analog Output Channel 0. DAC1 OUT is the voltage output signal for Analog Output Channel 1.

Pin 11, AGND, is the ground reference point for both analog output channels as well as analog input.

The following output ranges are available:

Output signal range	Bipolar input: ±5 V*
	Unipolar input: 0 to 10 V*

* Maximum load current = ±2 mA for 12-bit linearity

Figure 3-7 shows how to make analog output signal connections.

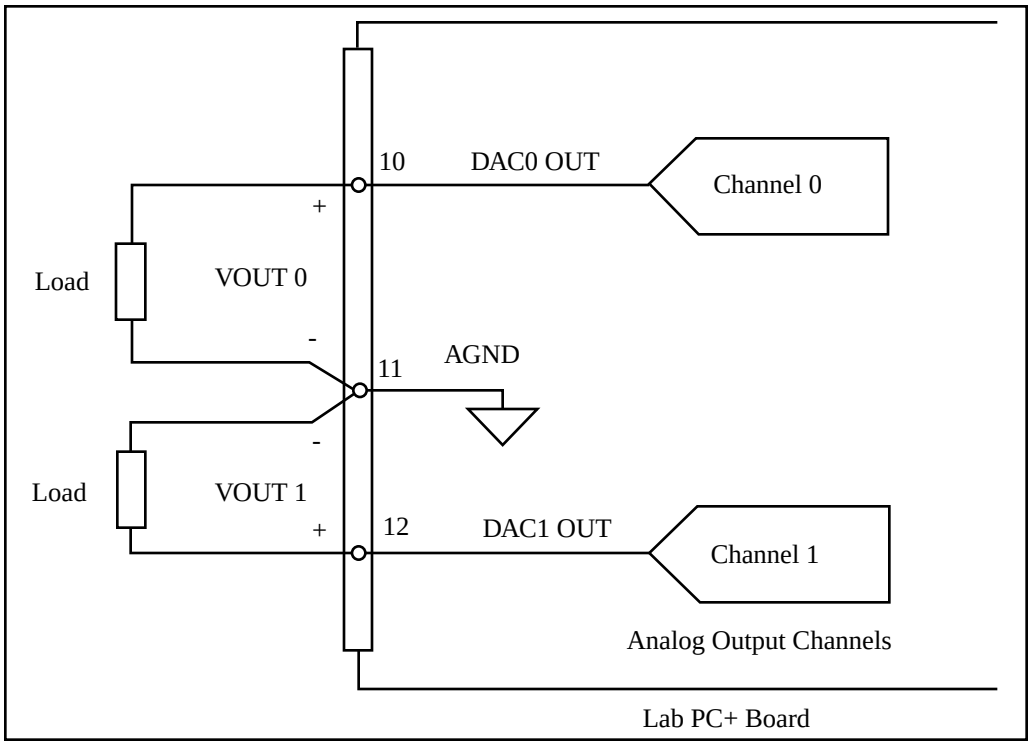


Figure 3-7. Analog Output Signal Connections

Digital I/O Signal Connections

Pins 13 through 37 of the I/O connector are digital I/O signal pins. Digital I/O on the Lab-PC+ is designed around the 8255A integrated circuit. The 8255A is a general-purpose peripheral interface containing 24 programmable I/O pins. These pins represent the three 8-bit ports (PA, PB, and PC) of the 8255A.

Pins 14 through 21 are connected to the digital lines PA<0..7> for digital I/O Port A. Pins 22 through 29 are connected to the digital lines PB<0..7> for digital I/O Port B. Pins 30 through 37

are connected to the digital lines PC<0..7> for digital I/O Port C. Pin 13, DGND, is the digital ground pin for all three digital I/O ports.

The following specifications and ratings apply to the digital I/O lines.

Absolute maximum voltage input rating: +5.5 V with respect to DGND
-0.5 V with respect to DGND

Logical Inputs and Outputs

Digital I/O lines:	**Minimum**	**Maximum**
Input logic low voltage	-0.3 V	0.8 V
Input logic high voltage	2.2 V	5.3 V
Output logic low voltage (at output current = 2.5 mA)	-	0.4 V
Output logic high voltage (at output current = -2.5 mA)	3.7 V	-
Darlington drive current (R_{EXT} = 700 Ω, V_{EXT} = 1.7 V)	±2.5 mA	±4.0 mA

Figure 3-8 illustrates signal connections for three typical digital I/O applications.

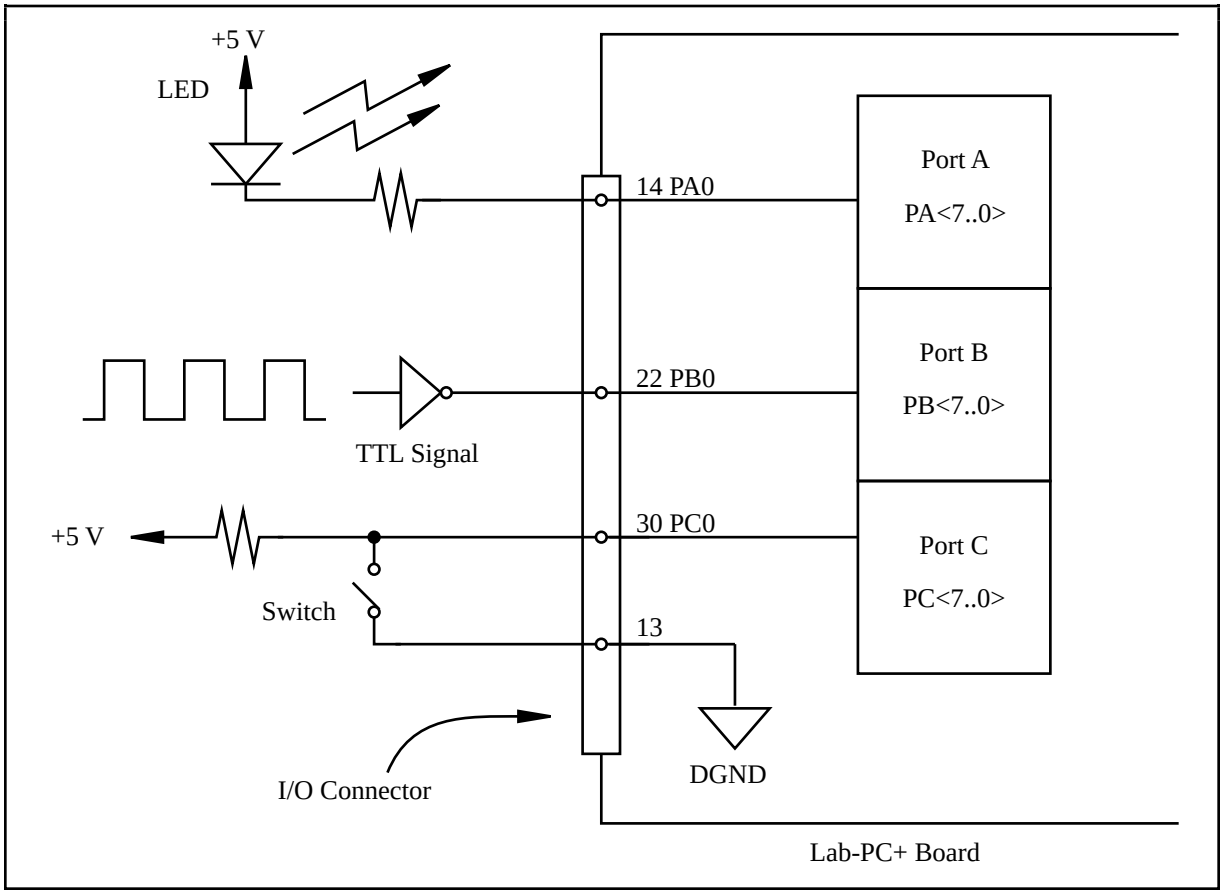


Figure 3-8. Digital I/O Connections

In Figure 3-8, Port A is configured for digital output, and Ports B and C are configured for digital input. Digital input applications include receiving TTL signals and sensing external device states such as the switch in Figure 3-8. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 3-8.

Port C Pin Connections

The signals assigned to Port C depend on the mode in which the 8255A is programmed. In Mode 0, Port C is considered as two 4-bit I/O ports. In Modes 1 and 2, Port C is used for status and handshaking signals with two or three I/O bits mixed in. The following table summarizes the signal assignments of Port C for each programmable mode. See Appendix E, *Register-Level Programming*, for programming information.

Table 3-2. Port C Signal Assignments

Programmable Mode	Group A					Group B		
	PC7	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O
*Indicates that the signal is active low.								

Timing Specifications

The handshaking lines STB* and IBF are used to synchronize input transfers. The handshaking lines OBF* and ACK* are used to synchronize output transfers.

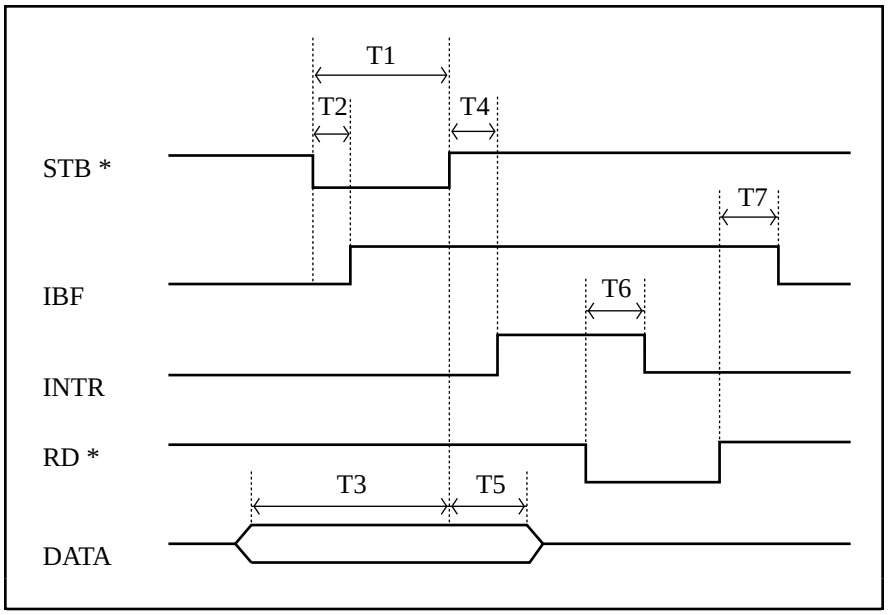
The following signals are used in the timing diagrams shown later in this chapter:

Name	**Type**	**Description**
STB*	Input	Strobe input–A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input buffer full–A high signal on this handshaking line indicates that data has been loaded into the input latch. This is primarily an input acknowledge signal.
ACK*	Input	Acknowledge input–A low signal on this handshaking line indicates that the data written from the specified port has been accepted. This signal is primarily a response from the external device that it has received the data from the Lab-PC+.

Name	Type	Description (continued)
OBF*	Output	Output buffer full–A low signal on this handshaking line indicates that data has been written from the specified port.
INTR	Output	Interrupt request–This signal becomes high when the 8255A is requesting service during a data transfer. The appropriate interrupt enable signals must be set to generate this signal.
RD*	Internal	Read signal–This signal is the read signal generated from the control lines of the PC I/O channel.
WR*	Internal	Write signal–This signal is the write signal generated from the control lines of the PC I/O channel.
DATA	Bidirectional	Data lines at the specified port–This signal indicates when the data on the data lines at a specified port is or should be available.

Mode 1 Input Timing

The timing specifications for an input transfer in Mode 1 are as follows:

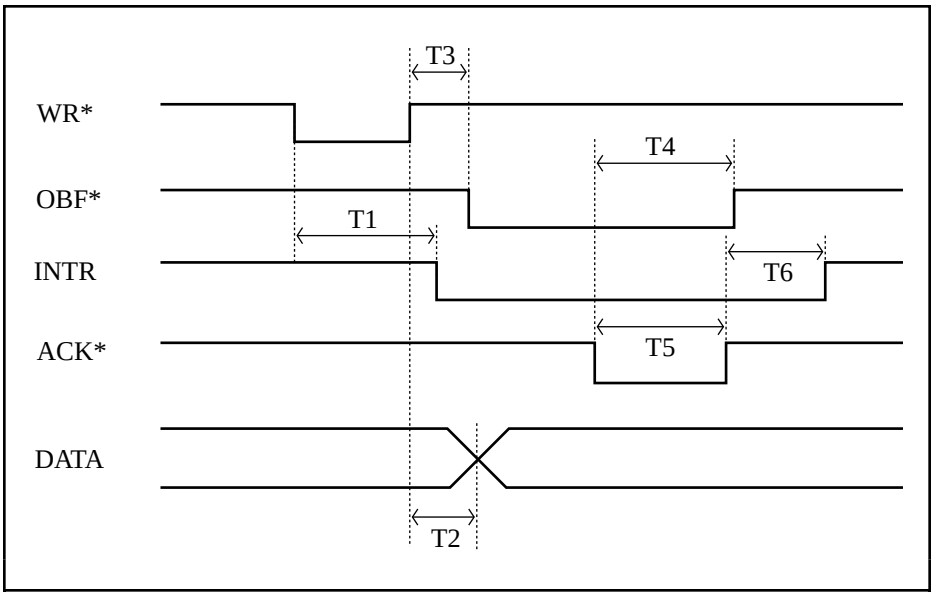


Name	Description	Minimum	Maximum
T1	STB* pulse width	500	–
T2	STB* = 0 to IBF = 1	–	300
T3	Data before STB* = 1	0	–
T4	STB* = 1 to INTR = 1	–	300
T5	Data after STB* = 1	180	–
T6	RD* = 0 to INTR = 0	–	400
T7	RD* = 1 to IBF = 0	–	300

All timing values are in nanoseconds.

Mode 1 Output Timing

The timing specifications for an output transfer in Mode 1 are as follows:

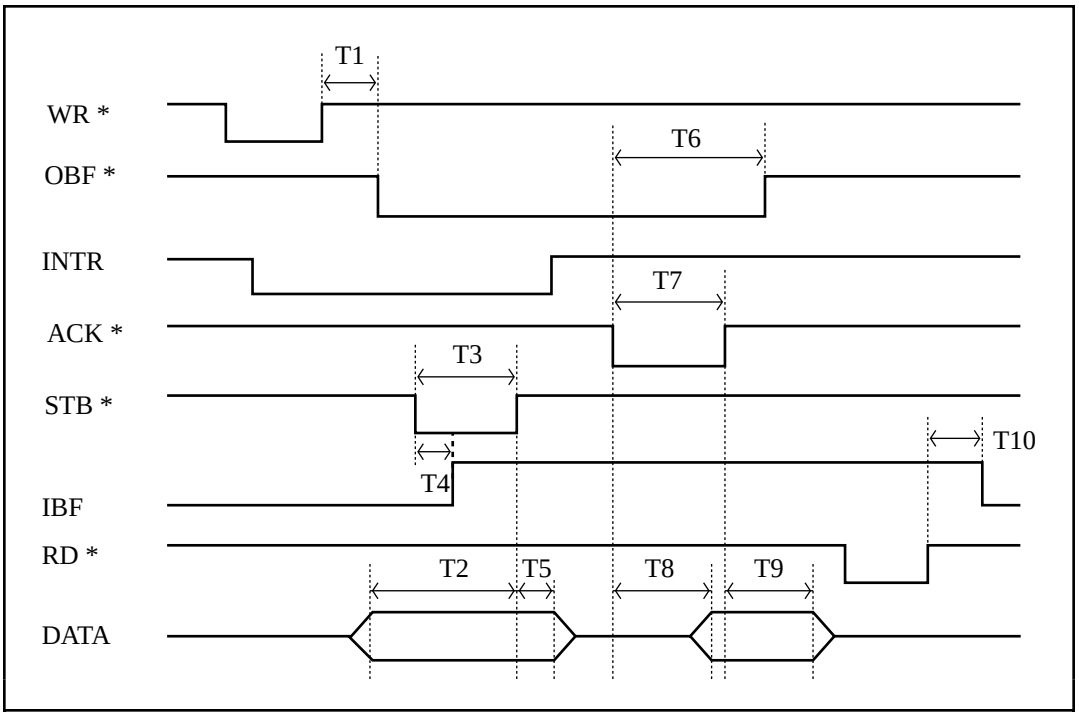


Name	Description	Minimum	Maximum
T1	WR* = 0 to INTR = 0	–	450
T2	WR* = 1 to output	–	350
T3	WR* = 1 to OBF* = 0	–	650
T4	ACK* = 0 to OBF* = 1	–	350
T5	ACK* pulse width	300	–
T6	ACK* = 1 to INTR = 1	–	350

All timing values are in nanoseconds.

Mode 2 Bidirectional Timing

The timing specifications for bidirectional transfers in Mode 2 are as follows:



Name	Description	Minimum	Maximum
T1	WR* = 1 to OBF* = 0	–	650
T2	Data before STB* = 1	0	–
T3	STB* pulse width	500	–
T4	STB* = 0 to IBF = 1	–	300
T5	Data after STB* = 1	180	–
T6	ACK* = 0 to OBF = 1	–	350
T7	ACK* pulse width	300	–
T8	ACK* = 0 to output	–	300
T9	ACK* = 1 to output float	20	250
T10	RD* = 1 to IBF = 0	–	300

All timing values are in nanoseconds.

Timing Connections

Pins 38 through 48 of the I/O connector are connections for timing I/O signals. The timing I/O of the Lab-PC+ is designed around the 8253 Counter/Timer integrated circuit. Two of these integrated circuits are employed in the Lab-PC+. One, designated 8253(A), is used exclusively for data acquisition timing, and the other, 8253(B), is available for general use. Pins 38 through 40 carry external signals that can be used for data acquisition timing in place of the dedicated 8253(A). These signals are explained in the next section, *Data Acquisition Timing Connections*. Pins 41 through 48 carry general-purpose timing signals from 8253(B). These signals are explained under *General-Purpose Timing Signal Connections and General-Purpose Counter/Timing Signals* later in this chapter.

Data Acquisition Timing Connections

Counter 0 on the 8253(A) Counter/Timer (referred to as A0) is used as a sample interval counter in timed A/D conversions. Counter 1 on the 8253(A) Counter/Timer (referred to as A1) is used as a sample counter in conjunction with Counter 0 for data acquisition. These counters are not available for general use. In addition to counter A0, EXTCONV* can be used to externally time conversions. See Appendix E, *Register-Level Programming*, for the programming sequence needed to enable this input. Figure 3-9 shows the timing requirements for the EXTCONV* input. An A/D conversion is initiated by a falling edge on the EXTCONV*.

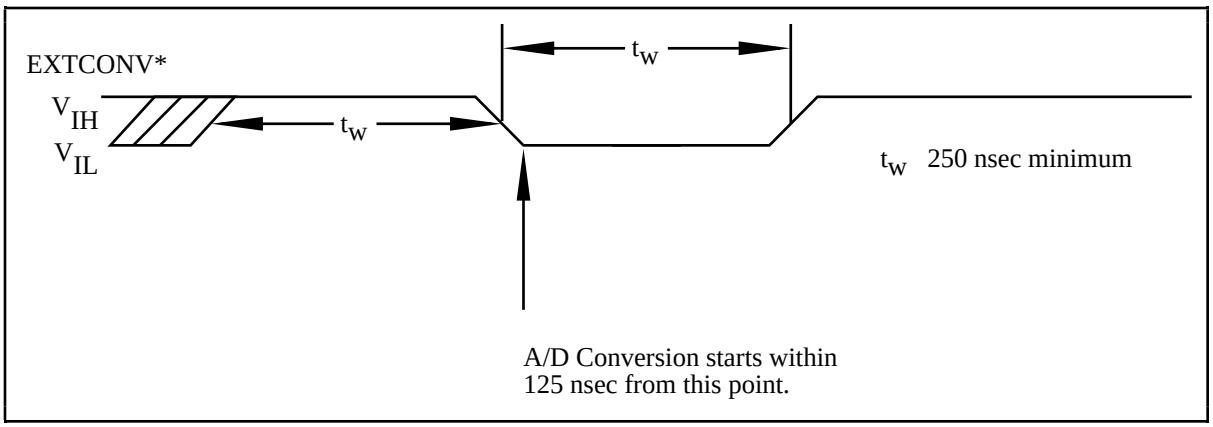


Figure 3-9. EXTCONV* Signal Timing

Another external control, EXTTRIG, is used for either starting a data acquisition sequence or terminating an ongoing data acquisition sequence, depending on the settings of the HWTRIG and PRETRIG bits in the Command Registers.

If HWTRIG is set, EXTTRIG serves as an external trigger to start a data acquisition sequence. In this mode, posttrigger mode, the sample interval counter is gated off until a rising edge is sensed on the EXTTRIG line. EXTCONV*, however, is enabled on the first rising edge of EXTCONV*, following the rising edge on the EXTTRIG line. Further transitions on the EXTTRIG line have no effect until a new data acquisition sequence is established. Figures 3-10

and 3-11 illustrate two possible posttrigger data acquisition timing cases. In Figure 3-10, the rising edge on EXTTRIG is sensed when the EXTCONV* input is high. Thus, the first A/D conversion occurs on the second falling edge of EXTCONV*, after the rising edge on EXTTRIG. In Figure 3-11, the rising edge on EXTTRIG is sensed when the EXTCONV* input is low. In this case, the first A/D conversion occurs on the first falling edge of EXTCONV*, after the rising edge on EXTTRIG. Notice that Figures 3-10 and 3-11 show a controlled acquisition mode data acquisition sequence; that is, Sample Counter A1 disables further A/D conversions after the programmed count (3 in the examples shown in Figures 3-10 and 3-11) expires. The counter is not loaded with the programmed count until the first falling edge following a rising edge on the clock input; therefore two extra conversion pulses are generated as shown in Figures 3-10 and 3-11. EXTTRIG can also be used as an external trigger in freerun acquisition mode.

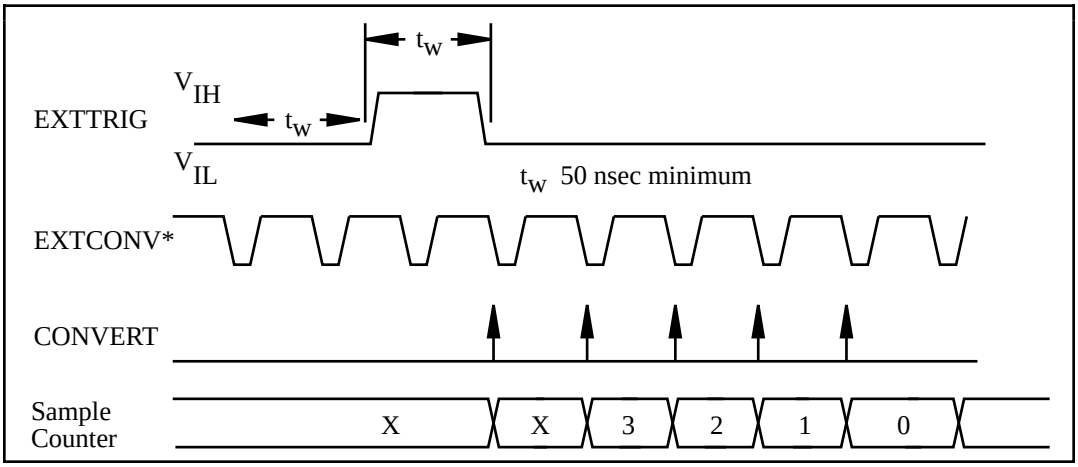


Figure 3-10. Posttrigger Data Acquisition Timing Case 1

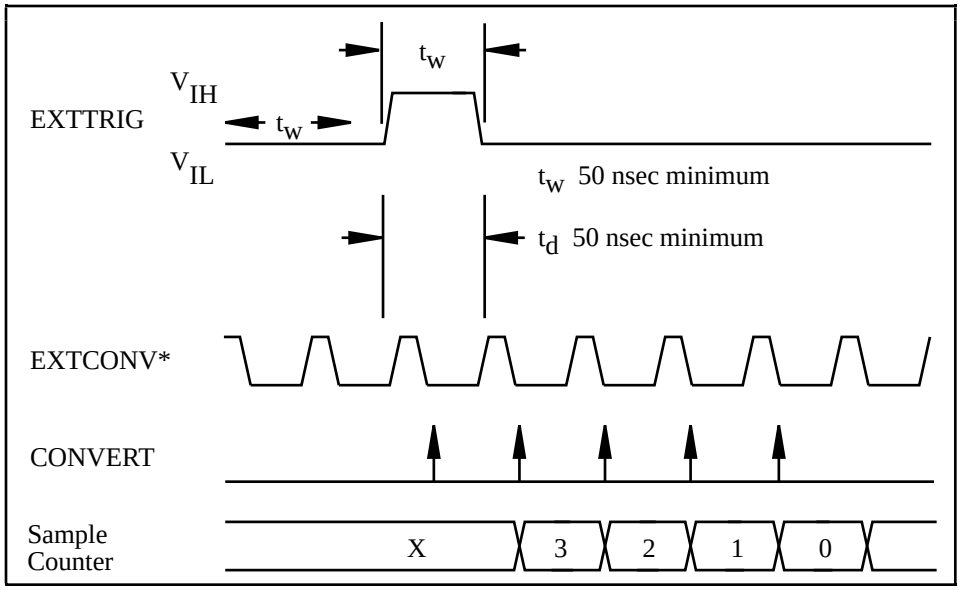


Figure 3-11. Posttrigger Data Acquisition Timing Case 2

If PRETRIG is set, EXTTRIG serves as a pretrigger signal. In pretrigger mode, A/D conversions are enabled via software before a rising edge is sensed on the EXTTRIG input. However, the sample counter, Counter A1, is not gated on until a rising edge is sensed on the EXTTRIG input. Additional transitions on this line have no effect until a new data acquisition sequence is set up. Conversions remain enabled for the programmed count after the trigger; therefore, data can be acquired before and after the trigger. Pretrigger mode works only in controlled acquisition mode, that is, Counter A1 is required to disable A/D conversions after the programmed count expires. Thus, the maximum number of samples acquired after the trigger is limited to 65,535. The number of samples acquired before the trigger is limited only by the size of the memory buffer available for data acquisition. Figure 3-12 shows a pretrigger data acquisition timing sequence.

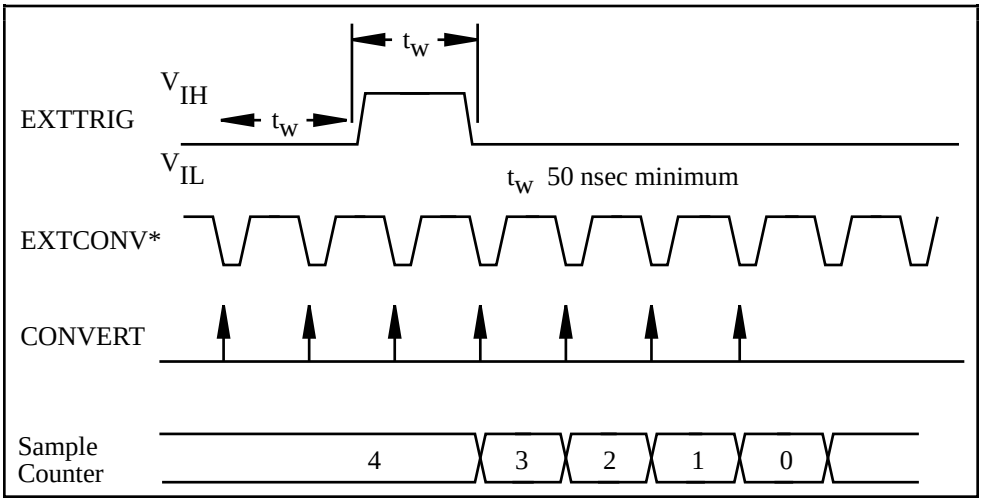


Figure 3-12. Pretrigger Data Acquisition Timing

Because both pretrigger and posttrigger modes use EXTTRIG input, only one mode can be used at a time. If neither PRETRIG nor HWTRIG is set high, this signal has no effect.

The final external control signal, EXTUPDATE*, is used to externally control the updating of the output voltage of the 12-bit DACs or to generate an externally timed interrupt. If the LDAC0 or LDAC1 bit in the Command Register 2 is set, the corresponding DAC voltage is updated by a low level on the EXTUPDATE* signal. If the CNTINTEN bit in the Command Register 3 is set, an interrupt is generated whenever a rising edge is detected on the EXTUPDATE* bit. Therefore, externally timed, interrupt-driven waveform generation is possible on the Lab-PC+. Figure 3-13 illustrates a waveform generation timing sequence using the EXTUPDATE* signal. Notice that the DACs are updated by a *low level* on the EXTUPDATE* line. Any writes to the DAC Data Registers while EXTUPDATE* is low therefore result in immediate update of the DAC output voltages.

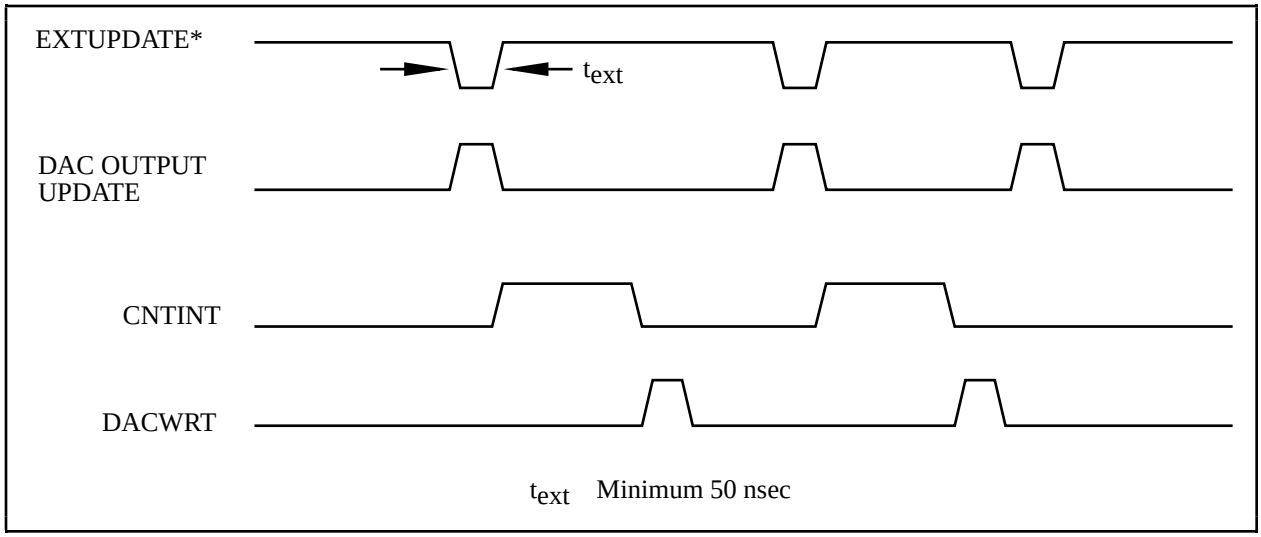


Figure 3-13. EXTUPDATE* Signal Timing for Updating DAC Output

Since a rising edge on the EXTUPDATE* signal always sets the CNTINT bit in the Status Register, the EXTUPDATE* signal can also be used for periodic interrupt generation timed by an external source. The CNTINT bit is cleared by writing to the Timer Interrupt Clear Register. Figure 3-14 illustrates a timing sequence where EXTUPDATE* is being used to generate an interrupt.

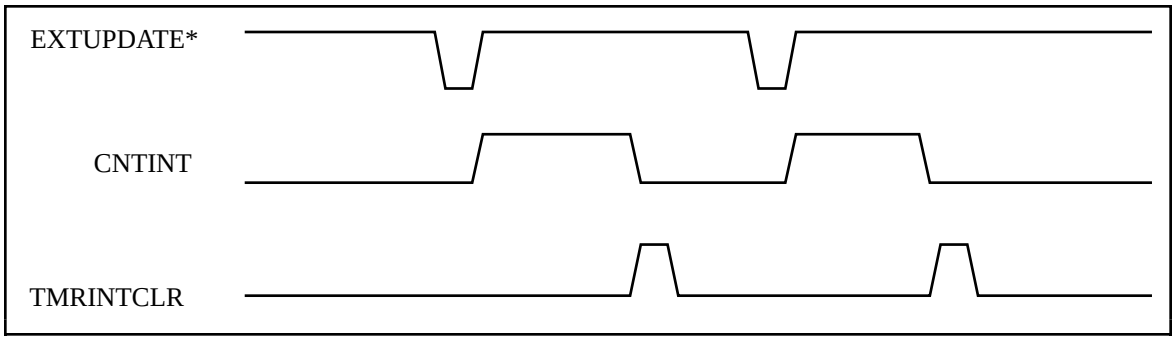


Figure 3-14. EXTUPDATE* Signal Timing for Generating Interrupts

The following rating applies to the EXTCONV*, EXTTRIG and EXTUPDATE* signals.

Absolute maximum voltage input rating: -0.5 to 7.0 V with respect to DGND

General-Purpose Timing Signal Connections and General-Purpose Counter/Timing Signals

The general-purpose timing signals include the GATE, CLK, and OUT signals for the three 8253(B) counters. The 8253 Counter/Timers can be used for general-purpose applications such as pulse and square wave generation; event counting; and pulse-width, time-lapse, and frequency

measurement. For these applications, CLK and GATE signals are sent to the counters, and the counters are programmed for various operations. The single exception is counter B0, which has an internal 2 MHz clock.

The 8253 Counter/Timer is described briefly in Chapter 4, *Theory of Operation.* For detailed programming information, consult Appendix B, *OKI 82C53 Data Sheet*.

Pulse and square wave generation are performed by programming a counter to generate a timing signal at its OUT output pin.

Event counting is performed by programming a counter to count rising or falling edges applied to any of the 8253 CLK inputs. The counter value can then be read to determine the number of edges that have occurred. Counter operation can be gated on and off during event counting. Figure 3-15 shows connections for a typical event-counting operation where a switch is used to gate the counter on and off.

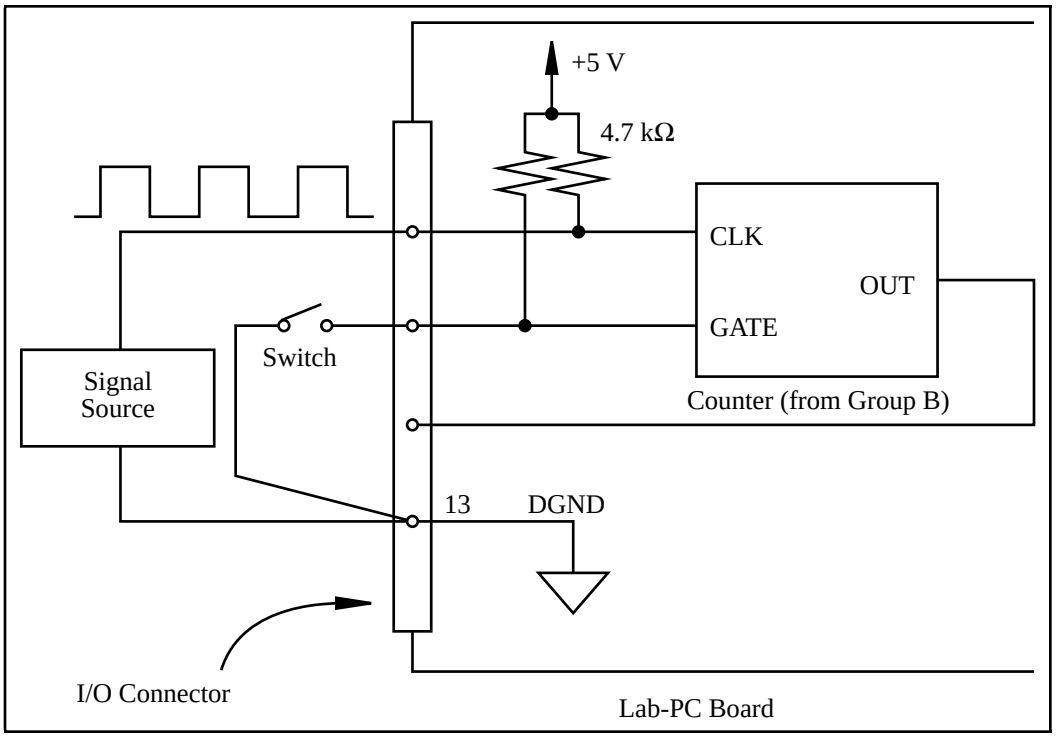


Figure 3-15. Event-Counting Application with External Switch Gating

Pulse-width measurement is performed by level gating. The pulse to be measured is applied to the counter GATE input. The counter is loaded with the known count and is programmed to count down while the signal at the GATE input is high. The pulse width equals the counter difference (loaded value minus read value) multiplied by the CLK period.

Time-lapse measurement is performed by programming a counter to be edge gated. An edge is applied to the counter GATE input to start the counter. The counter can be programmed to start

counting after receiving a low-to-high edge. The time lapse since receiving the edge equals the counter value difference (loaded value minus read value) multiplied by the CLK period.

To perform frequency measurement, program a counter to be level gated and count the number of falling edges in a signal applied to a CLK input. The gate signal applied to the counter GATE input is of known duration. In this case, you program the counter to count falling edges at the CLK input while the gate is applied. The frequency of the input signal then equals the count value divided by the gate period. Figure 3-16 shows the connections for a frequency measurement application. You can also use a second counter to generate the gate signal in this application. In this case, program the second counter for a one-shot mode. This scheme needs an external inverter to make the output pulse of the second counter active high.

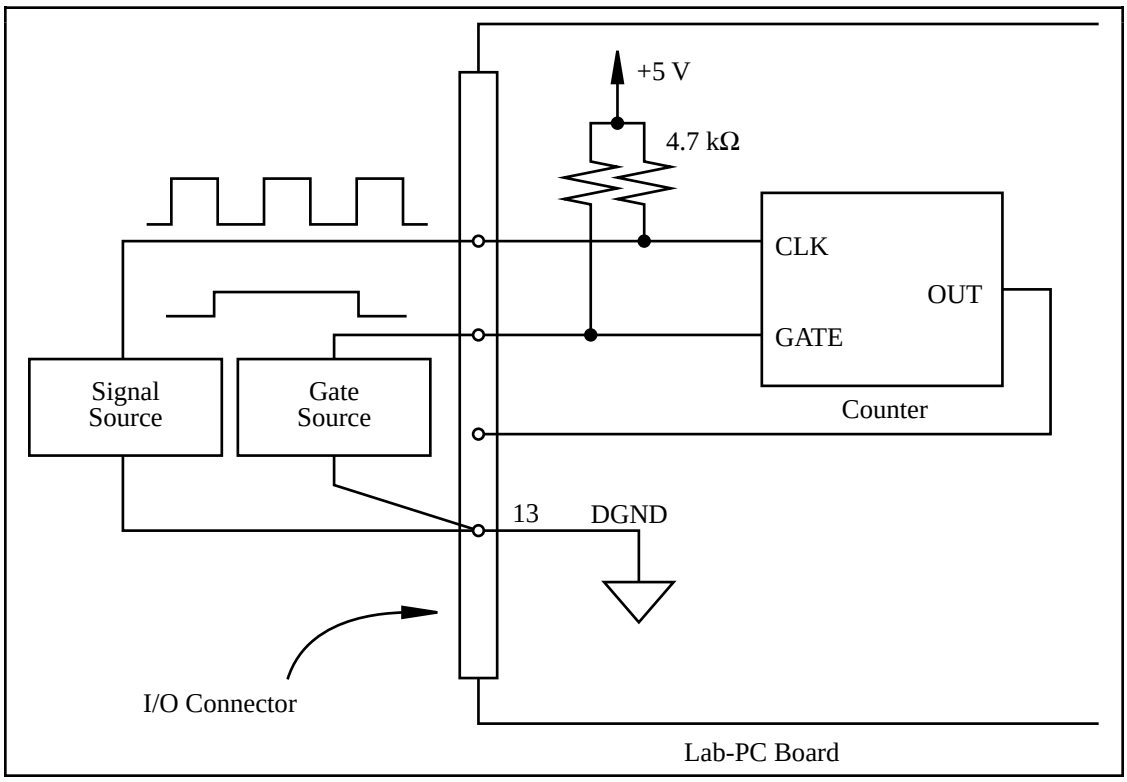


Figure 3-16. Frequency Measurement Application

The GATE, CLK, and OUT signals for Counters B1 and B2 are available at the I/O connector. In addition, the GATE and CLK pins are pulled up to +5 V through a 4.7 kΩ resistor.

Figure 3-17 shows the timing requirements for the GATE and CLK input signals and the timing specifications for the OUT output signals of the 8253.

The following specifications and ratings apply to the 8253 I/O signals:

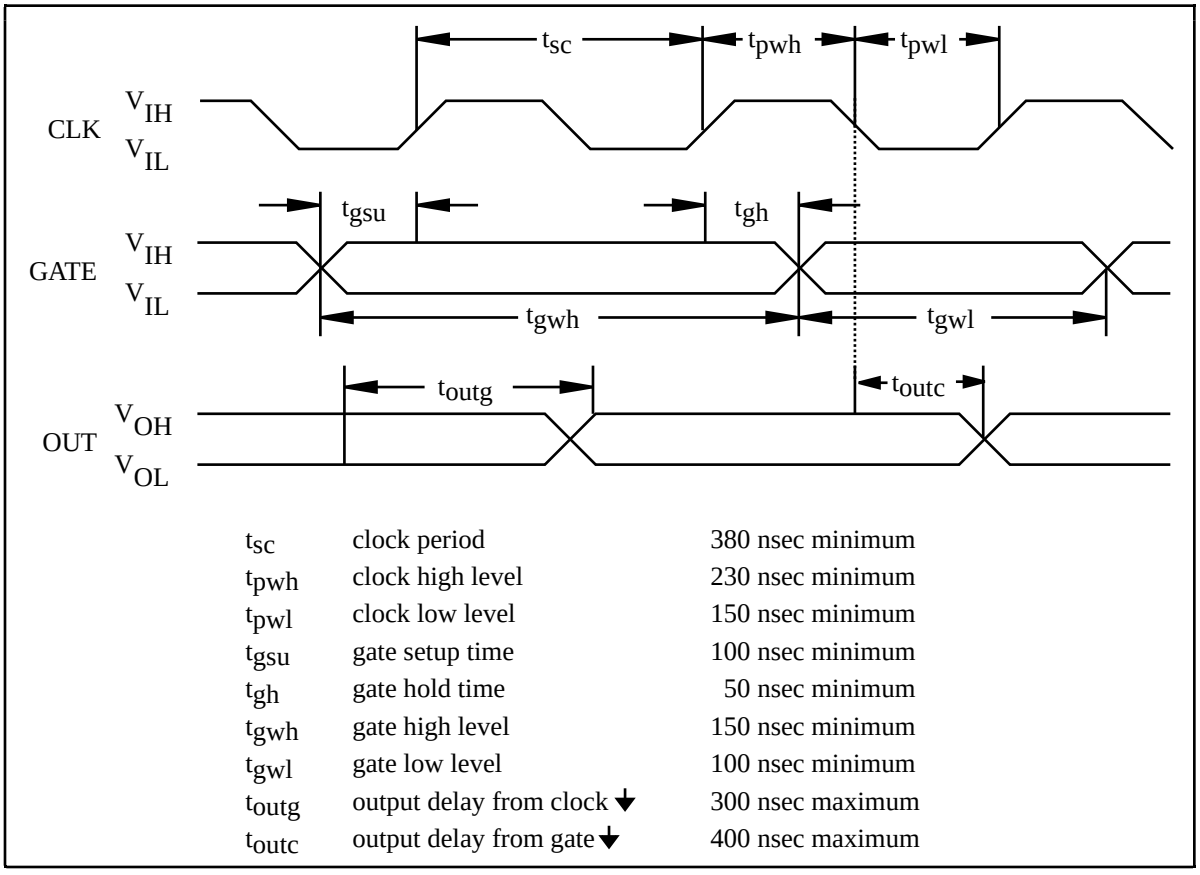
Absolute maximum voltage input rating: -0.5 to 7.0 V with respect to DGND

8253 digital input specifications (referenced to DGND):

V_{IH} input logic high voltage	2.2 V minimum
V_{IL} input logic low voltage	0.8 V maximum
Input load current	±10 µA maximum

8253 digital output specifications (referenced to DGND):

V_{OH} output logic high voltage	3.7 V minimum
V_{OL} output logic low voltage	0.45 V maximum
I_{OH} output source current, at V_{OH}	-1 mA maximum
I_{OL} output sink current, at V_{OL}	4 mA maximum



t_{sc}	clock period	380 nsec minimum
t_{pwh}	clock high level	230 nsec minimum
t_{pwl}	clock low level	150 nsec minimum
t_{gsu}	gate setup time	100 nsec minimum
t_{gh}	gate hold time	50 nsec minimum
t_{gwh}	gate high level	150 nsec minimum
t_{gwl}	gate low level	100 nsec minimum
t_{outg}	output delay from clock ↓	300 nsec maximum
t_{outc}	output delay from gate ↓	400 nsec maximum

Figure 3-17. General-Purpose Timing Signals

The GATE and OUT signals in Figure 3-17 are referenced to the rising edge of the CLK signal.

Cabling

National Instruments currently offers a cable termination accessory, the CB-50, for use with the Lab-PC+ board. This kit includes a terminated, 50-conductor, flat ribbon cable and a connector block. Signal input and output wires can be attached to screw terminals on the connector block and thereby connected to the Lab-PC+ I/O connector.

The CB-50 is useful for initially prototyping an application or in situations where Lab-PC+ interconnections are frequently changed. When you develop a final field wiring scheme, however, you may want to develop your own cable. This section contains information and guidelines for designing custom cables.

The Lab-PC+ I/O connector is a 50-pin male ribbon cable header. The manufacturer part numbers used by National Instruments for this header are as follows:

- Electronic Products Division/3M (part number 3596-5002)
- T&B/Ansley Corporation (part number 609-500)

The mating connector for the Lab-PC+ is a 50-position, polarized, ribbon socket connector with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside-down connection to the Lab-PC+. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

The following are the standard ribbon cables (50-conductor, 28 AWG, stranded) that can be used with these connectors:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

Chapter 4
Theory of Operation

This chapter contains a functional overview of the Lab-PC+ and explains the operation of each functional unit making up the Lab-PC+. This chapter also explains the basic operation of the Lab-PC+ circuitry.

Functional Overview

The block diagram in Figure 4-1 shows a functional overview of the Lab-PC+ board.

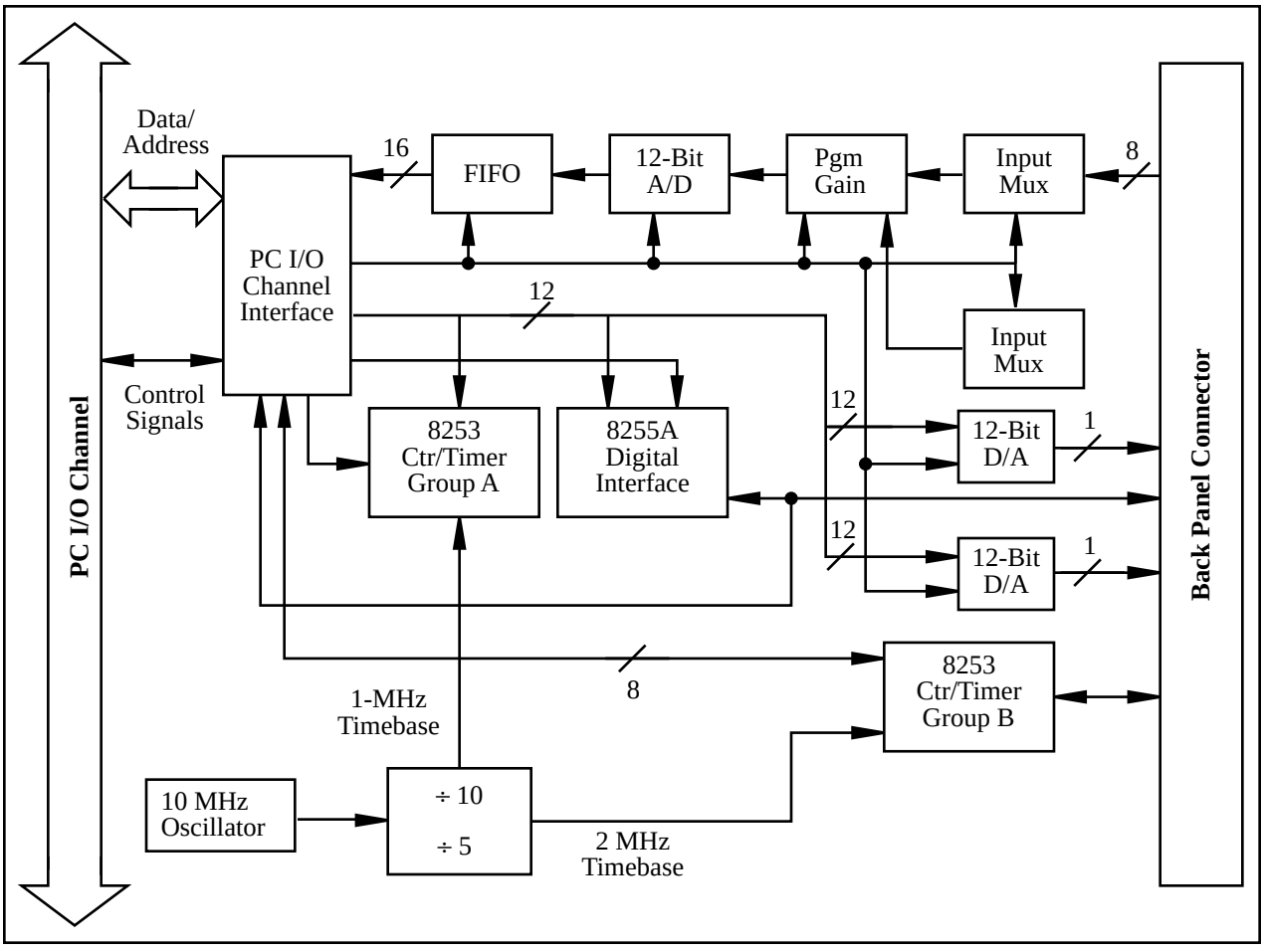


Figure 4-1. Lab-PC+ Block Diagram

The following are the major components making up the Lab-PC+ board:

- PC I/O channel interface circuitry
- Analog input and data acquisition circuitry
- Analog output circuitry
- Digital I/O circuitry
- Timing I/O circuitry

Data acquisition functions can be executed by using the analog input circuitry and some of the timing I/O circuitry. The internal data and control buses interconnect the components. The theory of operation for each of these components is explained in the remainder of this chapter. The theory of operation for the data acquisition circuitry is included with the discussion of the analog input circuitry.

PC I/O Channel Interface Circuitry

The PC I/O channel consists of an address bus, a data bus, a DMA arbitration bus, interrupt lines, and several control and support signals. The components making up the Lab-PC+ PC I/O channel interface circuitry are shown in Figure 4-2.

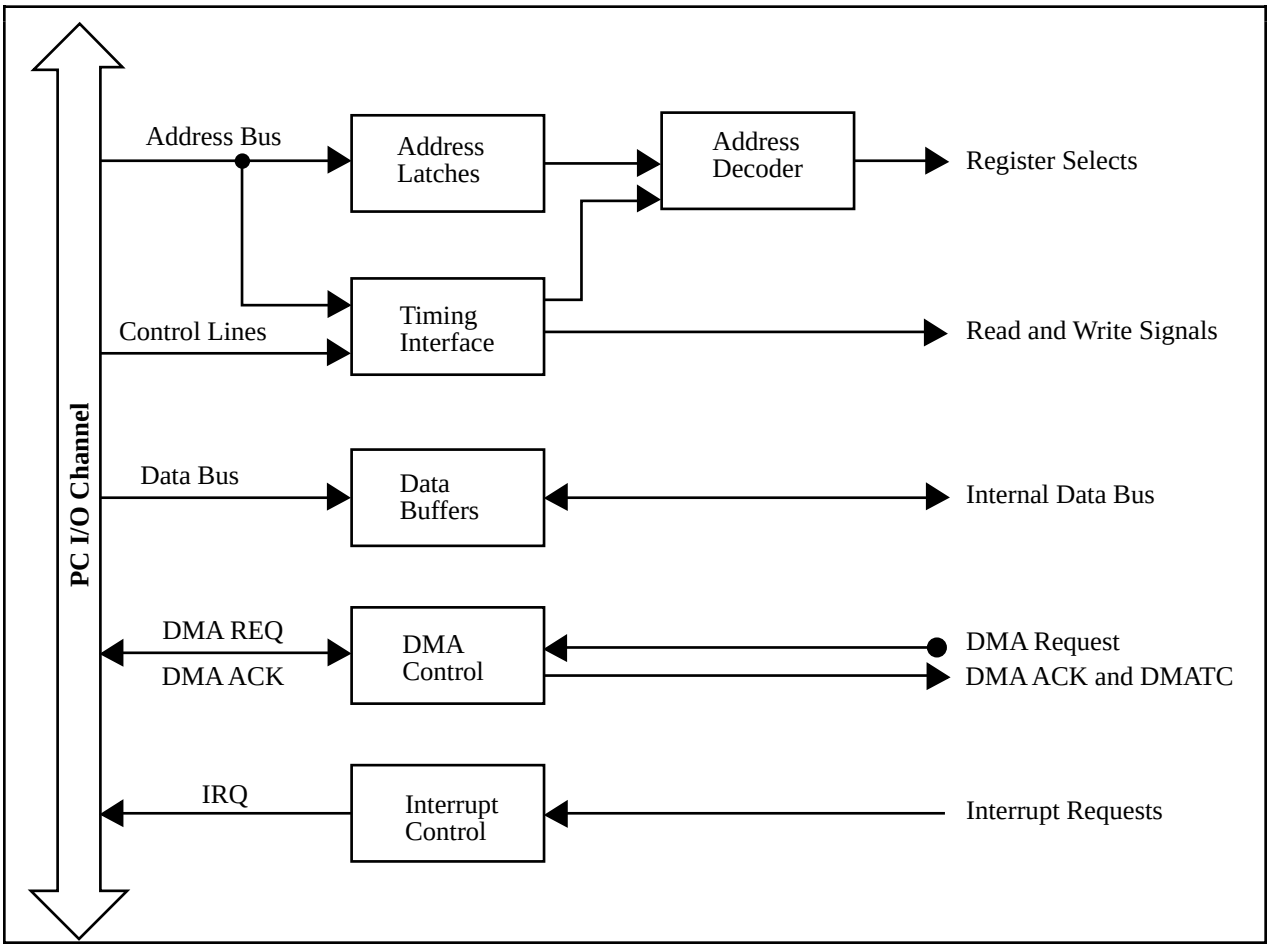


Figure 4-2. PC I/O Interface Circuitry Block Diagram

The circuitry consists of address latches, address decoders, data buffers, I/O channel interface timing control circuitry, interrupt control circuitry and DMA control circuitry. The circuitry monitors the address lines SA5 through SA9 to generate the board enable signal, and uses lines SA0 through SA4 plus timing signals to generate the onboard register select signals and read/write signals. The data buffers control the direction of data transfer on the bidirectional data lines based on whether the transfer is a read or write.

The interrupt control circuitry routes any enabled interrupts to the selected interrupt request line. The interrupt requests are tristate output signals allowing the Lab-PC+ board to share the interrupt lines with other devices. Six interrupt request lines are available for use by the Lab-PC+–IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, and IRQ9. Five different interrupts can be generated by the Lab-PC+:

- When an A/D conversion is available to be read from FIFO
- When either an OVERFLOW or an OVERRUN error occurs
- When DMA terminal count pulse is received

- When a digital I/O port is ready to transfer data
- When a rising edge signal is detected on Counter A2 output or on the EXTUPDATE line

Each one of these interrupts is individually enabled and cleared.

The DMA control circuitry generates DMA requests whenever an A/D conversion result is available from FIFO, if the DMA transfer is enabled. The Lab-PC+ supports 8-bit DMA transfers. DMA Channels 1, 2, and 3 of the PC I/O channel are available for such transfers.

Analog Input and Data Acquisition Circuitry

The Lab-PC+ provides eight channels of analog input with software-programmable gain and 12-bit A/D conversion. Using the timing circuitry, the Lab-PC+ can also automatically time multiple A/D conversions. Figure 4-3 shows a block diagram of the analog input and data acquisition circuitry.

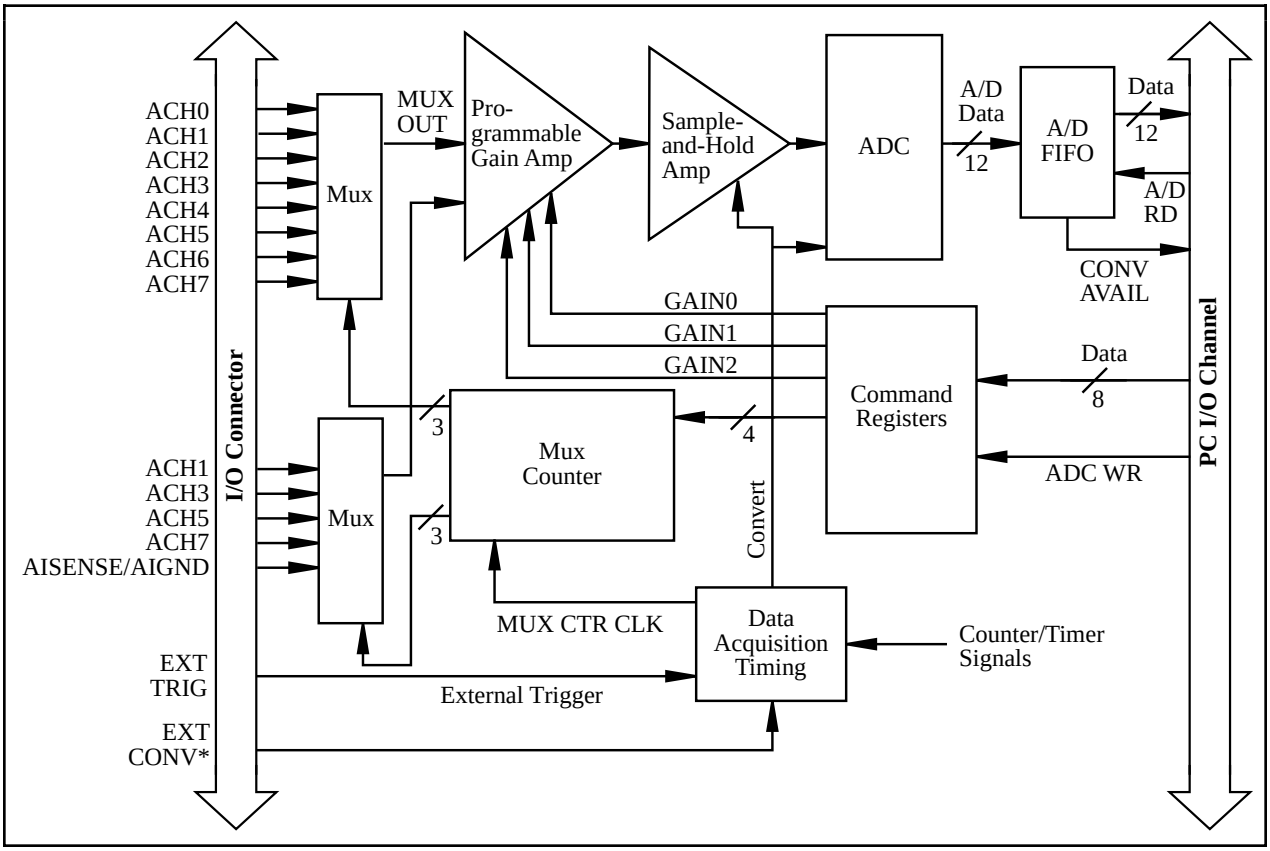


Figure 4-3. Analog Input and Data Acquisition Circuitry Block Diagram

Analog Input Circuitry

The analog input circuitry consists of two CMOS analog input multiplexers, a software-programmable gain amplifier, a 12-bit ADC, and a 12-bit FIFO memory that is sign-extended to 16 bits.

One of the input multiplexers has eight analog input channels (Channels 0 through 7). The other multiplexer is connected to Channels 1, 3, 5, and 7 for differential mode. The input multiplexers provide input overvoltage protection of ±45 V, powered on or off.

The programmable gain amplifier applies gain to the input signal, allowing an input analog signal to be amplified before being sampled and converted, thus increasing measurement resolution and accuracy. The gain of the instrumentation amplifier is selected under software control. The Lab-PC+ board provides gains of 1, 2, 5, 10, 20, 50, and 100.

The Lab-PC+ uses a 12-bit successive-approximation ADC. The 12-bit resolution of the converter allows the converter to resolve its input range into 4,096 different steps. This resolution also provides a 12-bit digital word that represents the value of the input voltage level with respect to the converter input range. The ADC itself has a single input range of 0 to +5 V. Additional circuitry allows inputs of ±5 V or 0 to 10 V.

When an A/D conversion is complete, the ADC clocks the result into the A/D FIFO. The A/D FIFO is 16 bits wide and 512 words deep. This FIFO serves as a buffer to the ADC and provides two benefits. First, any time an A/D conversion is complete, the value is saved in the A/D FIFO for later reading, and the ADC is free to start a new conversion. Secondly, the A/D FIFO can collect up to 512 A/D conversion values before any information is lost, thus allowing software some extra time (512 times the sample interval) to catch up with the hardware. If more than 512 values are stored in the A/D FIFO without the A/D FIFO being read from, an error condition called A/D FIFO overflow occurs and A/D conversion information is lost.

The A/D FIFO generates a signal that indicates when it contains A/D conversion data. The state of this signal can be read from the Lab-PC+ Status Register.

The output from the ADC can be interpreted as either straight binary or two's complement, depending on which input mode you select (unipolar or bipolar). In unipolar mode, the data from the ADC is interpreted as a 12-bit straight binary number with a range of 0 to +4,095. In bipolar mode, the data from the ADC is interpreted as a 12-bit two's complement number with a range of -2,048 to +2,047. In this mode, the MSB of the ADC result is inverted to make it two's complement. The output from the ADC is then sign-extended to 16 bits, causing either a leading 0 or a leading F (hex) to be added, depending on the coding and the sign. Thus, data values read from the FIFO are 16 bits wide.

Data Acquisition Timing Circuitry

A data acquisition operation refers to the process of taking a sequence of A/D conversions with the sample interval (the time between successive A/D conversions) carefully timed. The data acquisition timing circuitry consists of various clocks and timing signals that perform this timing. The Lab-PC+ board can perform both single-channel data acquisition and multiple-channel

(scanned) data acquisition in two modes–continuous and interval. The Lab-PC+ uses a counter to switch between analog input channels automatically during scanned data acquisition.

Data acquisition timing consists of signals that initiate a data acquisition operation, initiate individual A/D conversions, gate the data acquisition operation, and generate scanning clocks. Sources for these signals are supplied mainly by timers on the Lab-PC+ board. One of the two 8253 integrated circuits is reserved for this purpose.

An A/D conversion can be initiated by a high-to-low transition on the Counter A0 output (OUT A0) of the 8253(A) Counter/Timer chip on the Lab-PC+ or by a high-to-low transition on EXTCONV* input. During data acquisition, the onboard sample interval counter–Counter 0 of 8253(A)–is used to generate pulses that initiate A/D conversions.

The sample interval timer is a 16-bit down counter that uses the 1 MHz clock onboard to generate sample intervals from 2 µs to 65,535 µs (see *Timing I/O Circuitry* later in this chapter). Alternatively, the sample interval timer can use the output from Counter B0 (OUTB0) of the 8253(B) Counter/Timer chip on the Lab-PC+. Each time the sample interval timer reaches 0, it generates a pulse and reloads with the programmed sample interval count. This operation continues until the counter is reprogrammed.

As stated in Appendix E, *Register-Level Programming*, only Counter A0 is required for data acquisition operations in freerun acquisition mode. The software must keep track of the number of conversions that have occurred and turn off Counter A0 after the required number of conversions have been obtained. In controlled acquisition mode, two counters (Counters A0 and A1) are required for a data acquisition operation. Counter A0 generates the conversion pulses, and Counter A1 gates off Counter A0 after the programmed count has expired.

Single-Channel Data Acquisition

During single-channel data acquisition, the channel select and gain bits in Command Register 1 select the gain and analog input channel before data acquisition is initiated. These gain and multiplexer settings remain constant during the entire data acquisition process; therefore, all A/D conversion data is read from a single channel.

Multiple-Channel (Scanned) Data Acquisition

Multiple-channel data acquisition is performed by enabling scanning during data acquisition. Multiple-channel scanning is controlled by a scan counter.

For scanning operations, the scan counter decrements from the highest numbered channel (specified by the user) through Channel 0 and then repeats the sequence. Thus, any number of channels from two to eight can be scanned. Notice that the same gain setting is used for all channels in the scan sequence.

In single-channel continuous acquisition mode, the Lab-PC+ samples a single channel continuously without delays. In scanned continuous acquisition mode, the Lab-PC+ scans the selected channels repeatedly without delays and samples them.

You must initialize two additional counters to operate in interval acquisition mode. In single-channel interval acquisition mode, the Lab-PC+ samples a single channel a programmable number of times, waits for the duration of the scan interval, and repeats this cycle. In the scanned interval acquisition mode, the Lab-PC+ scans the selected samples, waits for the duration of the scan interval, and repeats the cycle.

Data Acquisition Rates

Maximum data acquisition rates (number of samples per second) are determined by the conversion period of the ADC plus the sample-and-hold acquisition time. During multiple-channel scanning, the data acquisition rates are further limited by the settling time of the input multiplexers and programmable gain amplifier. After the input multiplexers are switched, the amplifier must be allowed to settle to the new input signal value to within 12-bit accuracy before an A/D conversion is performed, or else 12-bit accuracy will not be achieved. The settling time is a function of the gain selected.

The Lab-PC+ data acquisition timing circuitry detects when data acquisition rates are high enough to cause A/D conversions to be lost. If this is the case, this circuitry sets an overrun error flag in the Lab-PC+ Status Register. If the recommended data acquisition rates in Table 4-2 are exceeded (an error flag is *not* automatically set), the analog input circuitry may not perform at 12-bit accuracy. If these rates are exceeded by more than a few microseconds, A/D conversions may be lost. Table 4-1 shows the recommended multiplexer and gain settling times for different gain settings. Table 4-2 shows the maximum recommended data acquisition rates for both single-channel and multiple-channel data acquisition. Notice that for a single-channel data acquisition, the data can be acquired at the maximum rate at any gain setting. The analog input bandwidth, however, is lower for higher gains. For multiple-channel data acquisition, observing the data acquisition rates given in Table 4-2 ensures 12-bit accuracy.

Table 4-1. Analog Input Settling Time Versus Gain

Gain Setting	Settling Time Recommended
1	12 µs
2, 5, 10, 20, 50	16 µs typical, 18 µs maximum
100	50 µs

Table 4-2. Lab-PC+ Maximum Recommended Data Acquisition Rates

Acquisition Mode	Gain Setting	Rate
Single Channel	1 2, 5, 10, 20, 50, 100	83.3 ksamples/s 71.4 ksamples/s*
Multiple Channel	1 2, 5, 10, 20, 50 100	83.3 ksamples/s 62.5 ksamples/s typical, 55.5 ksamples/s worst case 20.0 ksamples/s

* The single-channel acquisition rate decreases at higher gains because an offset error, dependent on the sampling rate, occurs at rates faster than 71.4 ksamples/s. This offset error is of the order of 1 LSB. If you can tolerate the offset error, the maximum sampling rate of 83.3 ksamples/s applies at all gains.

The recommended data acquisition rates given in Table 4-2 assume that voltage levels on all the channels included in the scan sequence are within range for the given gain and are driven by low-impedance sources. The signal ranges for the possible gains are shown in Table 4-3 and Table 4-4. Signal levels outside the ranges shown in Table 4-3 on the channels included in the scan sequence adversely affect the input settling time. Similarly, greater settling time may be required for channels driven by high-impedance signal sources.

Table 4-3. Bipolar Analog Input Signal Range Versus Gain

Gain Setting	Input Signal Range
1	-5 V to 4.99756 V
2	-2.5 V to 2.49878 V
5	-1.0 V to 0.99951 V
10	-500 mV to 499.756 mV
20	-250 mV to 249.877 mV
50	-100 mV to 99.951 mV
100	-50 mV to 49.975 mV

Table 4-4. Unipolar Analog Input Signal Range Versus Gain

Gain Setting	Input Signal Range
1	0 V to 9.99756 V
2	0 V to 4.99878 V
5	0 V to 1.99951 V
10	0 mV to 999.756 mV
20	0 mV to 499.877 mV
50	0 mV to 199.951 mV
100	0 mV to 99.975 mV

Analog Output Circuitry

The Lab-PC+ provides two channels of 12-bit D/A output. Each analog output channel can provide unipolar or bipolar output. Figure 4-4 shows a block diagram of the analog output circuitry.

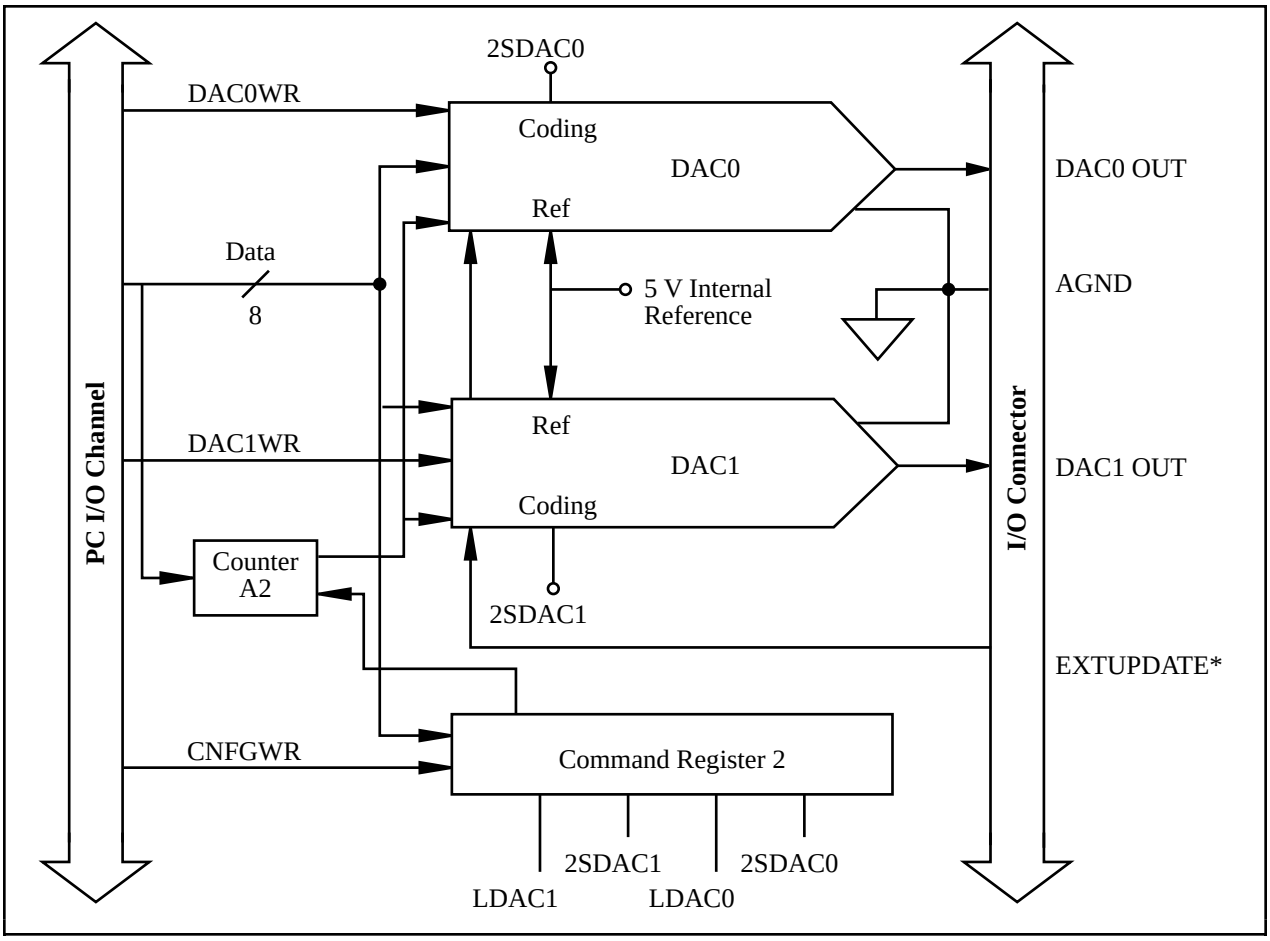


Figure 4-4. Analog Output Circuitry Block Diagram

Each analog output channel contains a 12-bit DAC. The DAC in each analog output channel generates a voltage proportional to the input V_{ref} multiplied by the digital code loaded into the DAC. Each DAC can be loaded with a 12-bit digital code by writing to the DAC0 (L and H) and DAC1 (L and H) Registers on the Lab-PC+ board. The voltage output from the two DACs is available at the Lab-PC+ I/O connector DAC0 OUT and DAC1 OUT pins.

The DAC voltages can be updated in any of three ways, depending on the setting of the LDAC bit. If this bit is cleared, the DAC output voltage is updated as soon as the corresponding DAC Data Register is written to. If the LDAC bit is set, the DAC output voltage does not change until a falling edge is detected either from Counter A2 or from EXTUPDATE*.

Each DAC channel can be jumper-programmed for either a unipolar voltage output or a bipolar voltage output range. A unipolar output gives an output voltage range of 0.0000 V to +9.9976 V. A bipolar output gives an output voltage range of -5.0000 V to +4.9976 V. For unipolar output, 0.0000 V output corresponds to a digital code word of 0. For bipolar output, -5.0000 V output corresponds to a digital code word of F800 (hex). One LSB is the voltage increment corresponding to a LSB change in the digital code word. For both unipolar and bipolar output, one LSB corresponds to:

$$\frac{10\ V}{4{,}096}$$

Digital I/O Circuitry

The digital I/O circuitry is designed around an 8255A integrated circuit. Figure 4-5 shows a block diagram of the digital I/O circuitry. The 8255A is a general-purpose PPI containing 24 programmable I/O pins. These pins represent the three 8-bit I/O ports (A, B, and C) of the 8255A as well as PA<0..7>, PB<0..7>, and PC<0..7> on the Lab-PC+ I/O connector. The 8255A also has a control register to configure each of the three I/O ports on the chip. These ports can be programmed as two groups of 12 signals or as three individual 8-bit ports. In addition, the board can be programmed in one of the three modes of operation–basic I/O, strobed I/O, or bidirectional bus. The programming of the digital I/O circuitry is covered in Appendix E, *Register-Level Programming*.

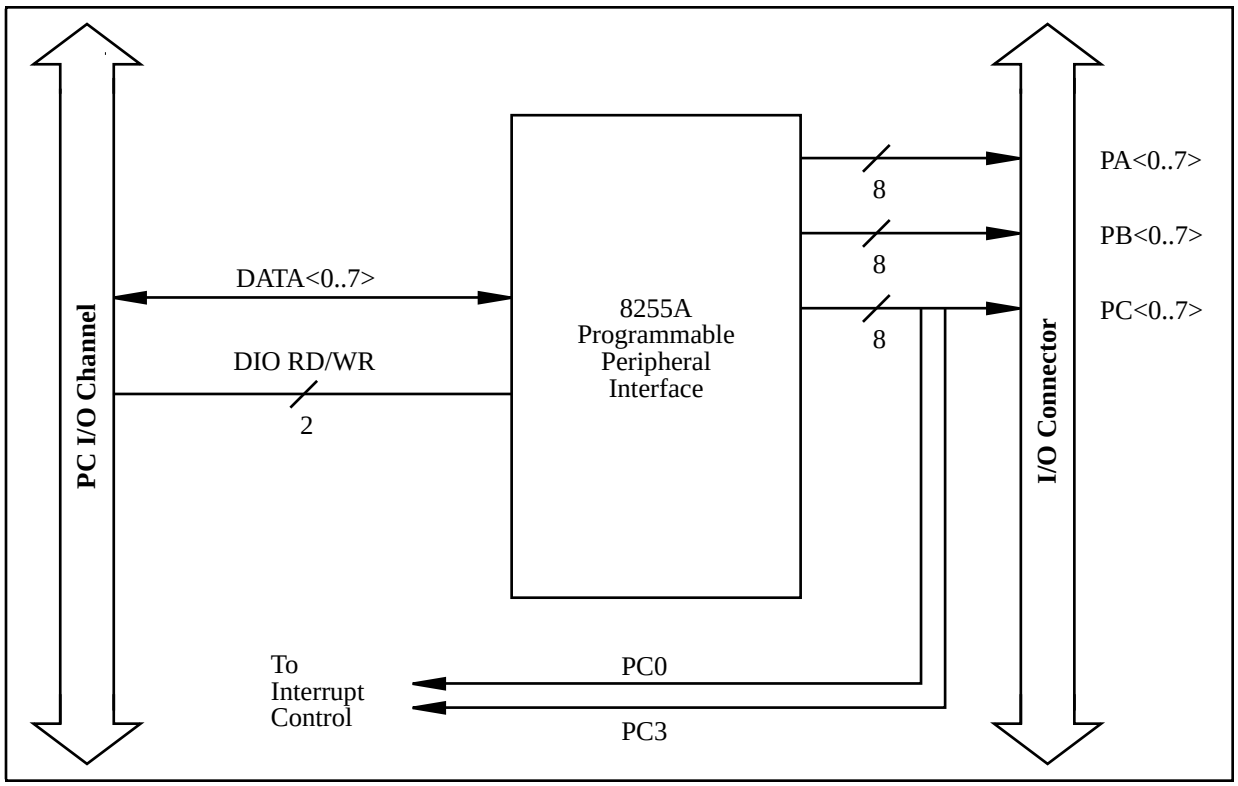


Figure 4-5. Digital I/O Circuitry Block Diagram

All three ports on the 8255A are TTL-compatible. When enabled, the digital output ports are capable of sinking 2.4 mA of current and sourcing 2.6 mA of current on each digital I/O line. When the ports are not enabled, the digital I/O lines act as high-impedance inputs.

Timing I/O Circuitry

The Lab-PC+ uses two 8253 Counter/Timer integrated circuits for data acquisition timing and for general-purpose timing I/O functions. One of these is used internally for data acquisition timing, and the other is available for general use. Figure 4-6 shows a block diagram of both groups of timing I/O circuitry (counter groups A and B).

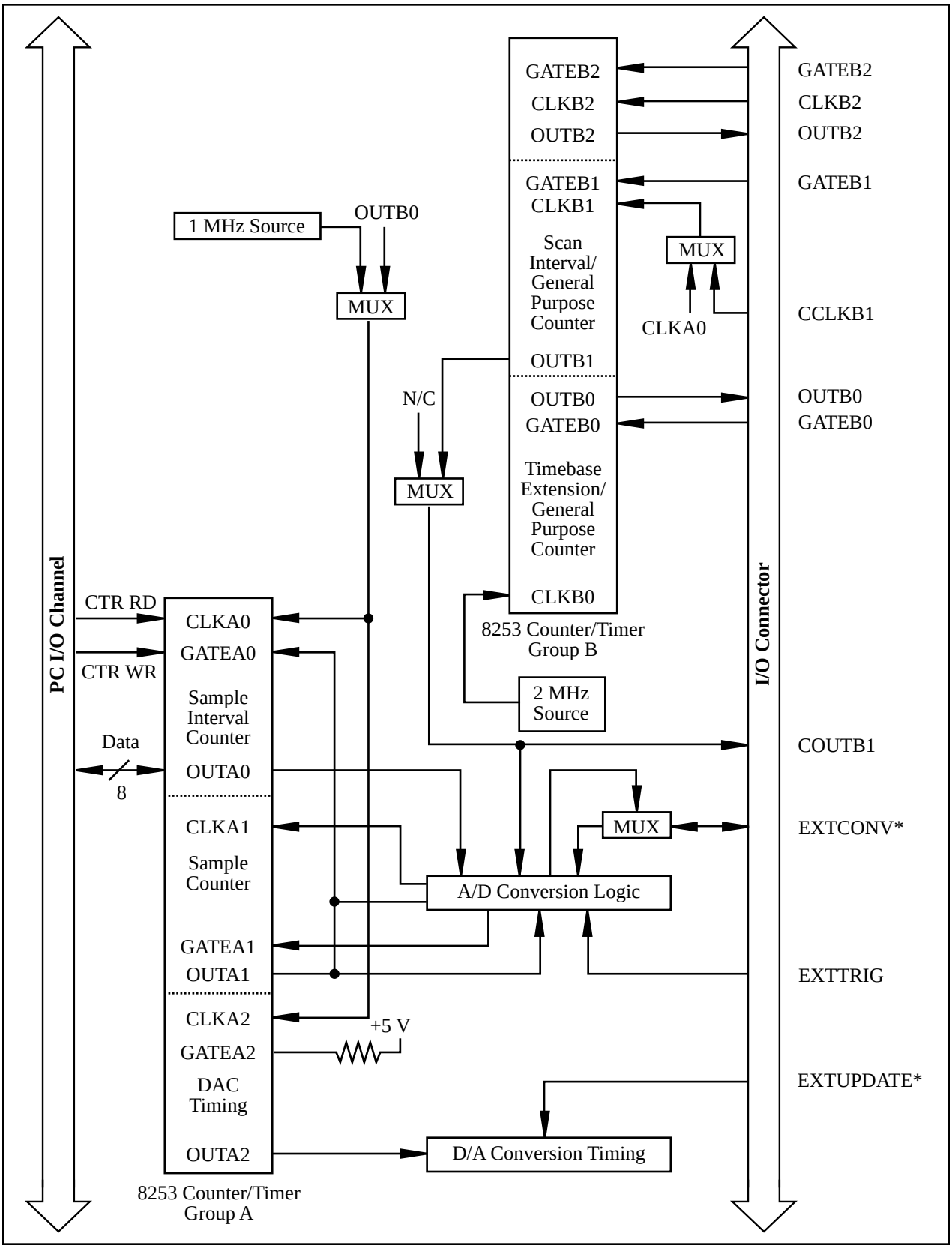


Figure 4-6. Timing I/O Circuitry Block Diagram

Each 8253 contains three independent 16-bit counter/timers and one 8-bit Mode Register. As shown in Figure 4-6, Counter Group A is reserved for data acquisition timing, and Counter Group B is free for general use. The output of Counter B0 can be used in place of the 1 MHz clock source on Counter A0 to allow clock periods greater than 65,536 µs. All six counter/timers can be programmed to operate in several useful timing modes. The programming and operation of the 8253 is presented in detail both in Appendix E, *Register-Level Programming*, and Appendix B, *OKI 82C53 Data Sheet*.

The 8253 for Counter Group A uses either a 1 MHz clock generated from the onboard 10 MHz oscillator or the output from Counter B0, which has a 2 MHz clock source, for its timebase. Optionally, Counter B1 can be used to provide interval-scanning timing. In the interval-scanning mode, the CLK pin of Counter B1 is driven by the same signal that is driving CLKA0. The OUTB1 pin on the I/O connector initiates scan sequences that are separated by a programmable scan interval time. The timebases for Counters B1 and B2 must be supplied externally through the 50-pin I/O connector.

Figure 4-7 shows an example of interval-scanning timing.

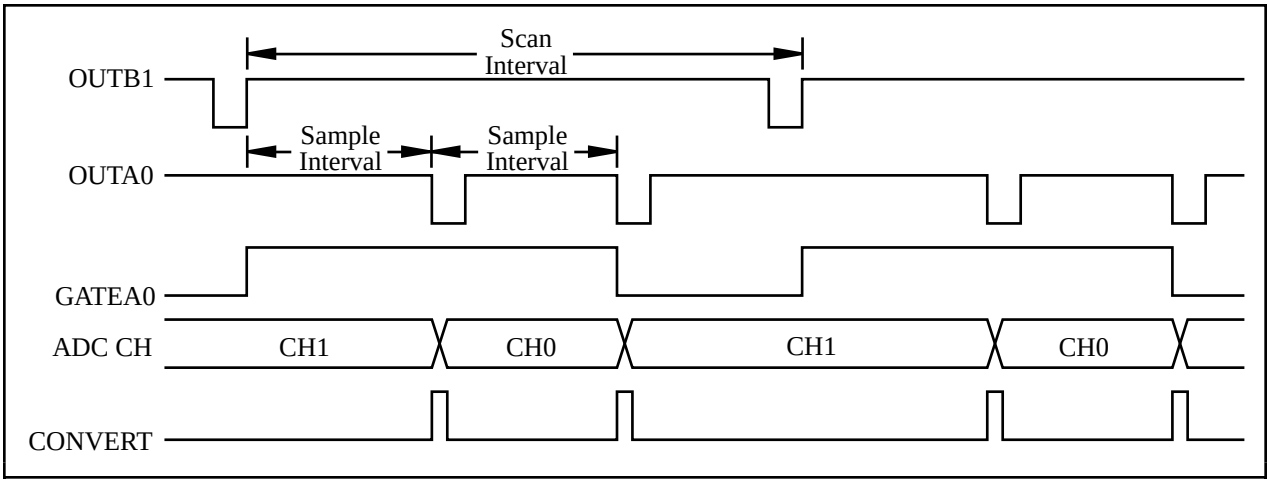


Figure 4-7. Two-Channel Interval-Scanning Timing

The single-channel interval acquisition mode makes use of an additional 8-bit counter–the Interval Counter. In this mode, Counter B1 initiates scan sequences that are separated by a programmable interval time. The Interval Counter is programmed for the number of samples of the selected channel in each interval. Figure 4-8 shows an example of single-channel interval timing. In this example, Counter B1 is programmed for the sample interval and the Interval Counter is programmed to count three samples, wait for the duration of the scan interval, count three samples, and so on. The acquisition operation ends when the sample counter (Counter A1) decrements to 0.

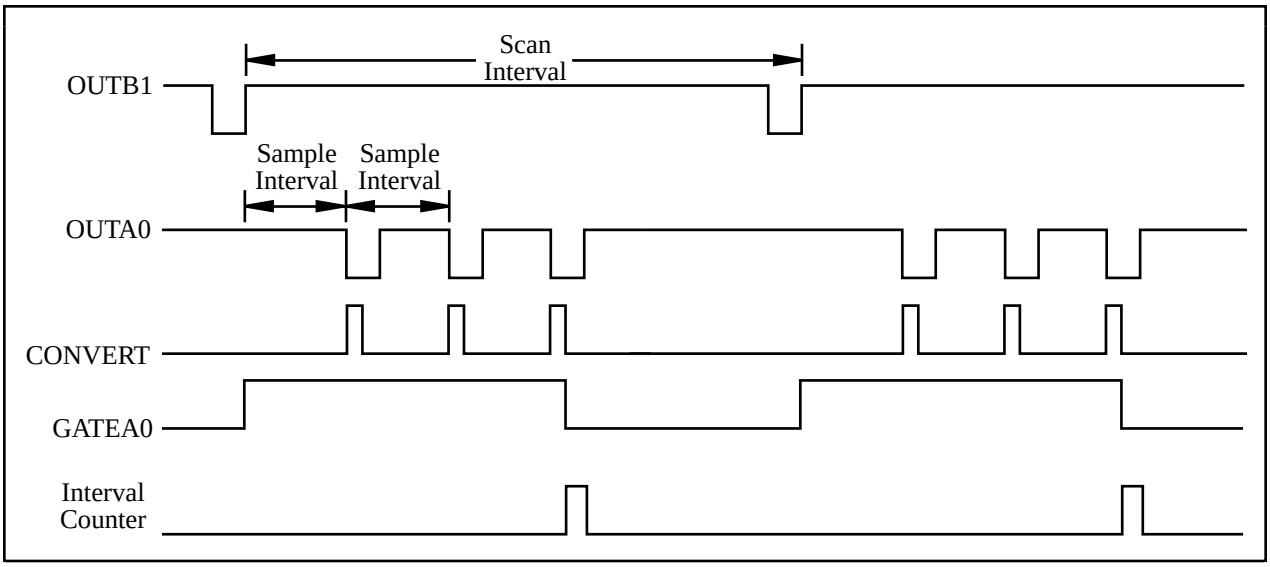


Figure 4-8. Single-Channel Interval Timing

The 16-bit counters in the 8253 can be diagrammed as shown in Figure 4-9.

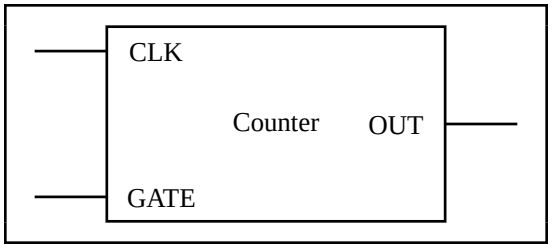


Figure 4-9. Counter Block Diagram

Each counter has a CLK input pin, a GATE input pin, and an output pin labeled OUT. The 8253 counters are numbered 0 through 2, and their GATE, CLK, and OUT pins are labeled GATE *N*, CLK *N*, and OUT *N*, where *N* is the counter number.

Chapter 5
Calibration

This chapter discusses the calibration procedures for the Lab-PC+ analog input and analog output circuitry.

The Lab-PC+ is calibrated at the factory before shipment. In order to maintain the 12-bit accuracy of the Lab-PC+ analog input and analog output circuitry, recalibration at six-month intervals is recommended. Recalibration is also recommended whenever the input or output configuration is changed.

Factory calibration is performed with the Lab-PC+ in its default factory configuration:

- -5 to +5 V analog input range (bipolar)
- -5 to +5 V analog output range (bipolar)

Calibration Equipment Requirements

For best measurement results, you should calibrate the Lab-PC+ so that its measurement accuracy is within ±0.012% of its input range (±0.5 LSB). According to standard practice, the equipment used to calibrate the Lab-PC+ should be 10 times as accurate, that is, have ±0.001% rated accuracy. Practically speaking, calibration equipment with four times the accuracy of the item under calibration is generally considered acceptable. Four times the accuracy of the Lab-PC+ is 0.003%. You need the following equipment to calibrate the Lab-PC+ board.

For analog input calibration, you need a precision variable DC voltage source (usually a calibrator) with these features:

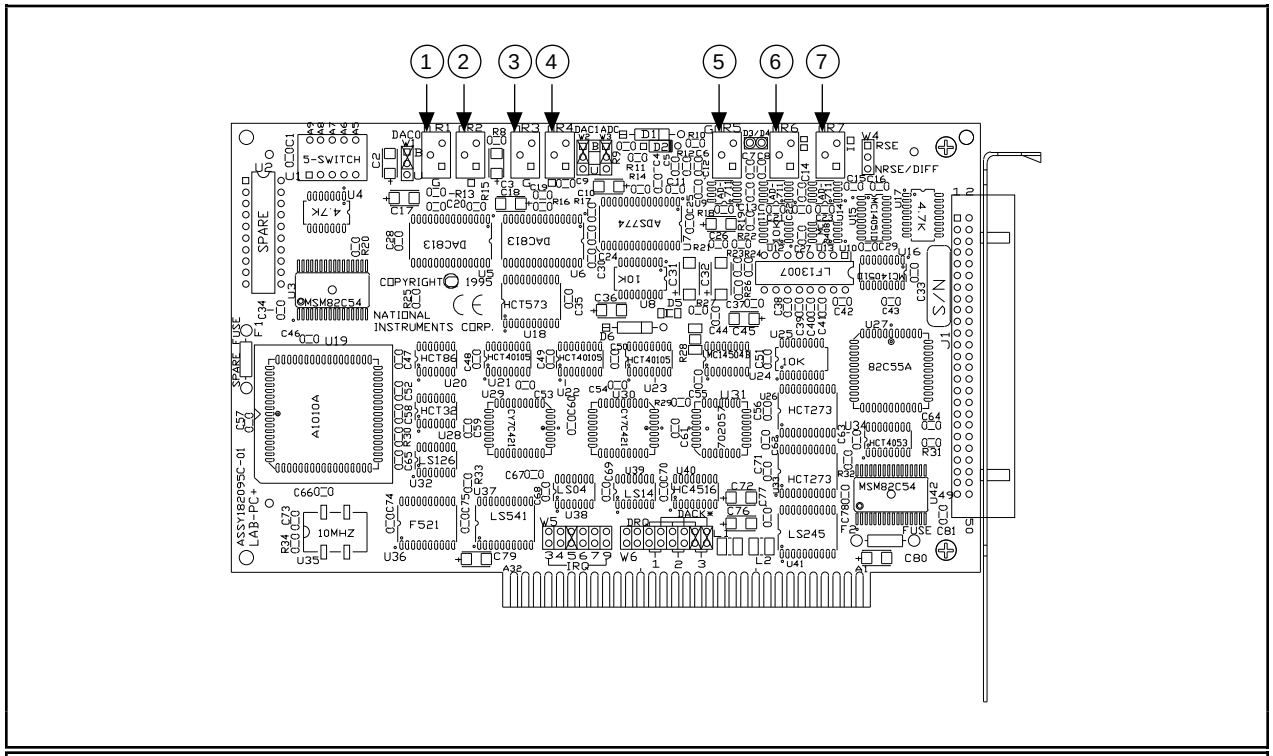
Accuracy	±0.001% standard ±0.003% sufficient
Range	Greater than ±10 V
Resolution	100 µV in ±10 V range (5½ digits)

For analog output calibration, you need a voltmeter with these features:

Accuracy	±0.001% standard ±0.003% sufficient
Range	Greater than ±10 V
Resolution	100 µV in ±10 V range (5½ digits)

Calibration Trimpots

The Lab-PC+ has six trimpots for calibration. The location of these trimpots on the Lab-PC+ board is shown in the partial diagram of the board in Figure 5-1.



1	R1	3	R3	5	R5	7	R7
2	R2	4	R4	6	R6		

Figure 5-1. Calibration Trimpot Location Diagram

The following trimpots are used to calibrate the analog input circuitry:

- R7 – Input offset trim, analog input
- R6 – Output offset trim, analog input
- R5 – Gain trim, analog input

The following trimpots are used to calibrate the analog output circuitry:

- R3 – Gain trim, analog output Channel 1
- R4 – Offset trim, analog output Channel 1
- R1 – Gain trim, analog output Channel 0
- R2 – Offset trim, analog output Channel 0

Analog Input Calibration

To null out error sources that compromise the quality of measurements, you must calibrate the analog input circuitry by adjusting the following potential sources of error:

- Offset errors
- Gain error of the analog input circuitry

You must perform the calibration if you change the input configuration from bipolar (the factory setting) to unipolar.

Offsets at the input to the instrumentation amplifier contribute gain-dependent offset error to the analog input circuitry. This offset is multiplied by the gain instrumentation amplifier. Other sources of offset error include the track-and-hold amplifier and the ADC. On the Lab-PC+, two trimpots are used to null out all of these offset sources. The first trimpot is used to null out the input offset (up to and including the instrumentation amplifier). To null out this offset, ground the input channel and adjust R7 until the readings at gains of 1 and 50 are the same. Then, to null out the output offset, adjust R6 until the readings are ±0.5 LSB. Because one of these error sources is gain-dependent, you should check and recalibrate the offset, if necessary, whenever the gain is changed significantly. Alternatively, you can calibrate the input offset at gain = 1 and note the offset errors for all other gains. You can then apply a software correction to the readings at gains higher than one by subtracting the offset errors. With this method, you can use the board at all available gain levels without recalibrating the input.

The maximum offset at the gain amplifier is specified at 0.5 mV. The maximum possible contribution of the gain amplifier to the total offset is therefore 0.5 mV multiplied by the gain. To find the error in LSBs, divide this voltage by the voltage of 1 LSB. Hence, with a large gain change, such as from 1 to 100, the number of LSBs offset from this source changes from about 0.2 to almost 20. Clearly, an adjustment that is acceptable for a 0.2 LSB error is probably not suitable when the error is multiplied by 100. For small changes in the gain, the error that accompanies changes in gain is much less. If the gain is changed from 1 to 2 or 5, the offset probably does not need to be recalibrated. Likewise, changes between gains of 20, 50, or 100 probably do not require recalibration.

All the stages up to and including the input to the ADC contribute to the gain error of the analog input circuitry. With the amplifier set to a gain of 1, the gain of the analog input circuitry is ideally 1. The gain error is the deviation of the gain from 1 and appears as a multiplication of the input voltage being measured. To calibrate this offset, you must apply V_{+fs} -1.5 LSB to the analog input circuitry and adjust a potentiometer until the ADC returns readings that flicker between its most positive count and the most positive count minus 1. The voltages corresponding to V_{+fs} and 1 LSB are given in Table 5-1.

The voltages corresponding to V_{-fs}, which is the most negative voltage that the ADC can read, V_{+fs} - 1, which is the most positive voltage the ADC can read, and 1 LSB, which is the voltage corresponding to one count of the ADC, depend on the input range selected. The value of these voltages for each input range is given in Table 5-1.

Table 5-1. Voltage Values of ADC Input

Input Range	V_{-fs}	V_{+fs} - 1	1 LSB	0.5 LSB
-5 to +5 V	-5 V	+4.99756 V	2.44 mV	1.22 mV
0 to 10 V	0 V	+9.99756 V	2.44 mV	1.22 mV

Board Configuration

The calibration procedure differs if you select either bipolar or unipolar input configuration. A procedure for each configuration is given next.

Bipolar Input Calibration Procedure

If your board is configured for bipolar input, which provides the range -5 to +5 V, then complete the following procedure in the order given. This procedure assumes that ADC readings are in the range -2,048 to +2,047, that is, the TWOSADC bit in Command Register 1 is set high. The following should be performed with the input configuration set to RSE.

1. Input Offset Calibration

   To adjust the amplifier input offset:

   a. Connect ACH0 (pin 1 on the I/O connector) to AISENSE/AIGND (pin 9).

   b. Take analog input readings from Channel 0 at gains of 1 and 50.

   c. Adjust trimpot R7 until the readings match to within one count at both gain settings.

2. Output Offset Calibration

   To adjust the amplifier output offset:

   a. Connect ACH0 (pin 1 on the I/O connector) to AISENSE/AIGND (pin 9).

   b. Take analog input readings from Channel 0 at the gain at which the system will be used.

   c. Adjust trimpot R6 until the readings are 0 ±0.5 LSB.

   Alternatively, the above offset calibration procedure can be carried out with the input gain set at 1, followed by recording the average reading at all other gains. These readings can be used

later for software offset correction of the data at gains other than 1, thus eliminating the need to perform the input offset recalibration when a different gain is used. The software correction consists of subtracting the recorded reading at gain *G* from every A/D conversion value obtained at gain *G*.

3. Gain Calibration

   Adjust the analog input gain by applying an input voltage across ACH0 and AISENSE/AIGND. This input voltage is +4.99634 V or V_{+fs} - 1.5 LSB.

   a. Connect the calibration voltage (+4.99634 V) across ACH0 (pin 1 on the I/O connector) and AISENSE/AIGND (pin 9).

   b. Take analog input readings from Channel 0 at a gain of 1, and adjust trimpot R5 until the ADC readings flicker evenly between 2,046 and 2,047. Alternatively, you can average a number of readings (approximately 100) and adjust trimpot R10 until the average reading is 2,046.5.

Unipolar Input Calibration Procedure

If your board is configured for unipolar input, which has an input range of 0 to +10 V, then complete the following steps in sequence. This procedure assumes that ADC readings are in the range 0 to 4,095, that is, the TWOSADC bit in Command Register 1 is cleared. The following should be performed with the input configuration set to RSE.

1. Input Offset Calibration

   To adjust the amplifier input offset:

   a. Connect ACH0 (pin 1 on the I/O connector) to AISENSE/AIGND (pin 9).

   b. Take analog input readings from Channel 0 at gains of 1 and 50.

   c. Adjust trimpot R7 until the readings match to within one count at both gain settings.

2. Output Offset Calibration

   To adjust the amplifier output offset:

   a. Connect ACH0 (pin 1 on the I/O connector) to AISENSE/AIGND (pin 9).

   b. Take analog input readings from Channel 0 at the gain at which the system will be used.

   c. Adjust trimpot R6 until the readings flicker between 0 and 1. Care must be taken to avoid setting the potentiometer too low in the unipolar mode. If the potentiometer is set too low, the ADC then simply outputs 0 because its input is below the lower limit.

3. Gain Calibration

   Adjust the analog input gain by applying an input voltage across ACH0 and AISENSE/AIGND. This input voltage is +9.99634 V or V_{+fs} - 1.5 LSB.

   a. Connect the calibration voltage (+9.99634 V) across ACH0 (pin 1 on the I/O connector) and AISENSE/AIGND (pin 9).

   b. Take analog input readings from Channel 0 at a gain of 1, and adjust trimpot R5 until the ADC readings flicker evenly between 4,094 and 4,095. Alternately, you can average a number of readings (approximately 100) and adjust trimpot R10 until the average reading is 4,094.5.

Analog Output Calibration

To null out error sources that affect the accuracy of the output voltages generated, you must calibrate the analog output circuitry by adjusting the following potential sources of error:

- Analog output offset error
- Analog output gain error

Offset error in the analog output circuitry is the total of the voltage offsets contributed by each component in the circuitry. This error appears as a voltage difference between the desired voltage and the actual output voltage generated and is independent of the D/A setting. To correct this offset gain error, set the D/A to negative full-scale and adjust a trimpot until the output voltage is the negative full-scale value ±0.5 LSB.

Gain error in the analog output circuitry is the product of the gains contributed by each component in the circuitry. This error appears as a voltage difference between the desired voltage and the actual output voltage generated, which depends on the D/A setting. This gain error is corrected by setting the D/A to positive full-scale and adjusting a trimpot until the output voltage corresponds to the positive full-scale value ±0.5 LSB.

Board Configuration

The calibration procedure differs if you select either bipolar or unipolar output configuration. A procedure for each configuration is given next.

Bipolar Output Calibration Procedure

If your board is configured for bipolar output, which provides an output range of -5 to +5 V, then complete the following procedures in the order given.

1. Adjust the Analog Output Offset

   Adjust the analog output offset by measuring the output voltage generated with the DAC set at negative full-scale (0). This output voltage should be V_{-fs} ±0.5 LSB. For bipolar output,

   V_{-fs} = -5 V, and 0.5 LSB = 1.22 mV.

   For analog output Channel 0:

   a. Connect the voltmeter between DAC0 OUT (pin 10 on the I/O connector) and AGND (pin 11).

   b. Set the analog output channel to -5 V by writing -2,048 to the DAC.

   c. Adjust trimpot R2 until the output voltage read is -5 V.

   For analog output Channel 1:

   a. Connect the voltmeter between DAC1 OUT (pin 12 on the I/O connector) and AGND (pin 11).

   b. Set the analog output channel to -5 V by writing -2,048 to the DAC.

   c. Adjust trimpot R4 until the output voltage read is -5 V.

2. Adjust the Analog Output Gain

   Adjust the analog output gain by measuring the output voltage generated with the DAC set at positive full-scale (4,095). This output voltage should be V_{+fs} ±0.5 LSB. For bipolar output,

   V_{+fs} = +4.99756 V, and 0.5 LSB = 1.22 mV.

   For analog output Channel 0:

   a. Connect the voltmeter between DAC0 OUT (pin 10 on the I/O connector) and AGND (pin 11).

   b. Set the analog output channel to +4.99756 V by writing 2,047 to the DAC.

   c. Adjust trimpot R1 until the output voltage read is +4.99756 V.

   For analog output Channel 1:

   a. Connect the voltmeter between DAC1 OUT (pin 12 on the I/O connector) and AGND (pin 11).

   b. Set the analog output channel to +4.99756 V by writing 2,047 to the DAC.

   c. Adjust trimpot R3 until the output voltage read is +4.99756 V.

Unipolar Output Calibration Procedure

If your analog output channel is configured for unipolar output, which has an output range of 0 to +10 V, then offset calibration is not needed. Calibrate your board by completing the following procedures for gain calibration.

Adjust the Analog Output Gain

Adjust the analog output gain by measuring the output voltage generated with the DAC set at positive full-scale (4,095). This output voltage should be V_{+fs} ±0.5 LSB. For unipolar output,

V_{+fs} = +9.99756 V, and 0.5 LSB = 1.22 mV.

For analog output Channel 0:

a. Connect the voltmeter between DAC0 OUT (pin 10 on the I/O connector) and AGND (pin 11).

b. Set the analog output channel to +9.99756 V by writing 4,095 to the DAC.

c. Adjust trimpot R1 until the output voltage read is +9.99756 V.

For analog output Channel 1:

a. Connect the voltmeter between DAC1 OUT (pin 12 on the I/O connector) and AGND (pin 11).

b. Set the analog output channel to +9.99756 V by writing 4,095 to the DAC.

c. Adjust trimpot R3 until the output voltage read is +9.99756 V.

Appendix A
Specifications

This appendix lists the specifications of the Lab-PC+. These specifications are typical at 25°C unless otherwise stated. The operating temperature range is 0° to 70°C.

Analog Input

Input Characteristics

Number of channels ..... 8 single-ended, 4 differential
Type of ADC..... Successive approximation
Resolution ..... 12 bits, 1 in 4,096
Maximum sampling rate ..... 83 ksamples/s
Input signal ranges .....

Board Gain (Software Selectable)	Board Range (Jumper Selectable)	
	bipolar	unipolar
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1 V	0 to 2 V
10	±0.5 V	0 to 1 V
20	±0.25 V	0 to 0.5 V
50	±0.1 V	0 to 0.2 V
100	±0.05 V	0 to 0.1 V

Input coupling ..... DC
Overvoltage protection..... ±45 V powered on, ±45 V powered off
  Inputs protected..... ACH<0..7>
FIFO buffer size ..... 512 samples
Data transfers ..... DMA, interrupts, programmed I/O
DMA modes..... Single transfer

Transfer Characteristics

Relative accuracy ..... ±1.0 LSB typ, ±1.5 LSB max
DNL ..... ±0.5 LSB typ, ±1 LSB max
No missing codes ..... 12 bits, guaranteed
Offset error
  Pregain error after calibration ..... Adjustable to 0 V
  Postgain error after calibration..... Adjustable to 0 V
Gain error (relative to calibration reference)
  After calibration ..... Adjustable to 0%
  Before calibration..... ±0.76% of reading (7,600 ppm) max
  Gain ≠ 1 with gain error
    adjusted to 0 at gain = 1 ..... ±0.5% of reading (500 ppm) max

Amplifier Characteristics

Input impedance ..... 0.1 GΩ in parallel with 45 pF
Input bias current ..... 150 pA
CMRR .....

Gain	CMRR at 60 Hz
1	75 dB
100	105 dB

Dynamic Characteristics

Bandwidth (-3 dB) ..... 400 kHz for gain = 1, 40 kHz for gain = 100
Settling time to full-scale step.....

Gain	Accuracy ±0.2% (± LSB)
≤10	14 µs
20, 50	20 µs
100	33 µs

System noise .....

Gain	±5 V Range
1	0.3 LSB rms
100	0.6 LSB rms

Stability

Recommended warm-up time ..... 15 minutes
Offset temperature coefficient
    Pregain ..... 450 µV/ºC
    Postgain ..... 10 µV/ºC
Gain temperature coefficient..... ±50 ppm/ºC

Explanation of Analog Input Specifications

Relative accuracy is a measure of the linearity of an ADC. However, relative accuracy is a tighter specification than a *nonlinearity* specification. Relative accuracy indicates the maximum deviation from a straight line for the analog input-to-digital output transfer curve. If an ADC has been calibrated perfectly, then this straight line is the ideal transfer function, and the relative accuracy specification indicates the worst deviation from the ideal that the ADC permits.

A relative accuracy specification of ±1 LSB is roughly equivalent to (but not the same as) a ±1/2 LSB nonlinearity or integral nonlinearity specification because relative accuracy encompasses both nonlinearity and variable quantization uncertainty, a quantity often mistakenly assumed to be exactly ±1/2 LSB. Although quantization uncertainty is ideally ±1/2 LSB, it can be different for each possible digital code and is actually the analog width of each code. Thus, it is more specific to use relative accuracy as a measure of linearity than it is to use what is normally called nonlinearity, because relative accuracy ensures that the *sum* of quantization uncertainty and A/D conversion error does not exceed a given amount.

Integral nonlinearity in an ADC is an often ill-defined specification that is supposed to indicate a converter's overall A/D transfer linearity. The manufacturers of the ADC chips used by National Instruments specify their integral nonlinearity by stating that the analog center of any code will not deviate from a straight line by more than ±1/2 LSB. This specification is misleading because, although the center of a particularly wide code may be found within ±1/2 LSB of the ideal, one of its edges may be well beyond ±1 LSB; thus, the ADC would have a relative accuracy of that amount. National Instruments tests its boards to ensure that they meet all three linearity specifications defined in this appendix; specifications for integral nonlinearity are included primarily to maintain compatibility with a convention of specifications used by other board manufacturers. Relative accuracy, however, is much more useful.

Differential nonlinearity is a measure of deviation of code widths from their theoretical value of 1 LSB. The width of a given code is the size of the range of analog values that can be input to produce that code, ideally 1 LSB. A specification of ±1 LSB differential nonlinearity ensures that no code has a width of 0 LSBs (that is, no missing codes) and that no code width exceeds 2 LSBs.

System noise is the amount of noise seen by the ADC when there is no signal present at the input of the board. The amount of noise that is reported directly (without any analysis) by the ADC is not necessarily the amount of real noise present in the system, unless the noise is ≥ 0.5 LSB rms. Noise that is less than this magnitude produces varying amounts of flicker, and the amount of flicker seen is a function of how near the real mean of the noise is to a code transition. If the mean is near or at a transition between codes, the ADC flickers evenly between the two codes, and the noise is seen as very nearly 0.5 LSB. If the mean is near the center of a code and the noise is relatively small, very little or no flicker is seen, and the noise is reported by the ADC as nearly 0 LSB. From the relationship between the mean of the noise and the measured rms magnitude of the noise, the character of the noise can be determined. National Instruments has determined that the character of the noise in the Lab-PC+ is fairly Gaussian, and so the noise specifications given are the amounts of pure Gaussian noise required to produce our readings.

Analog Output

Output Characteristics

Number of channels 2
Resolution ..... 12 bits, 1 in 4,096
Type of DAC..... Double-buffered multiplying
Data transfers ..... Interrupts, programmed I/O

Transfer Characteristics

Relative accuracy (INL).....
  bipolar range ..... ±0.25 LSB typ, ±0.5 LSB max
DNL ..... ±0.25 LSB typ, ±0.75 LSB max
Monotonicity ..... 12 bits, guaranteed
Offset error .....
  After calibration ..... Adjustable to 0 V
  Before calibration..... ±37 mV max
Gain error (relative to internal reference)
  After calibration ..... Adjustable to 0%
  Before calibration..... ±0.5% of reading (3,900 ppm) max

Voltage Output

Ranges ..... ±5 V, or 0 to 10 V, jumper selectable
Output coupling..... DC
Output impedance ..... 0.2 Ω max
Current drive ..... ±2 mA max
Protection ..... Short to AGND
Power on state ..... 0 V for ±5 V range, 5 V for 0 to 10 V range

Dynamic Characteristics

Settling time to FSR for 10 V step ..... 5 µs
Slew rate..... 10 V/µs

Stability

Offset temperature coefficient ..... ±30 µV/°C
Gain temperature coefficient
  internal reference..... ±10 ppm/°C

Explanation of Analog Output Specifications

Relative accuracy in a D/A system is the same as nonlinearity, because no uncertainty is added due to code width. Unlike an ADC, every digital code in a D/A system represents a specific analog value rather than a range of values. The relative accuracy of the system is therefore limited to the worst-case deviation from the ideal correspondence (a straight line), excepting noise. If a D/A system has been calibrated perfectly, then the relative accuracy specification reflects its worst-case absolute error.

Differential nonlinearity (DNL) in a D/A system is a measure of deviation of code width from 1 LSB. In this case, code width is the difference between the analog values produced by consecutive digital codes. A specification of ±1 LSB differential nonlinearity ensures that the code width is always greater than 0 LSBs (guaranteeing monotonicity) and is always less than 2 LSBs.

Digital I/O

Number of channels 24
Compatibility ..... TTL
Digital logic levels .....

Level	Min	Max
Input low voltage	-0.3 V	0.8 V
Input high voltage	2.2 V	5.3 V
Input low current (V_{in} = 0.8 V)	-	-1.0 µA
Input high current (V_{in} = 2.2 V)	-	1.0 µA
Output low voltage (I_{out} = 2.5 mA)	-	0.4 V
Output high voltage (I_{out} = -2.5 mA)	3.7 V	-

Darlington drive output current (Ports B and C only)
(R_{EXT} = 700 Ω, V_{EXT} = 1.7 V)..... ±2.5 mA min, ±4 mA max
Handshaking..... 3-wire (requires 1 port)
Power-on state..... Configured as input
Data transfers ..... Interrupt, programmed I/O

Timing I/O

Number of channels ..... 3 counter/timers
Resolution ..... 16 bits
Compatibility ..... TTL, gate and source pulled high with 4.7 kΩ resistors
Base clocks available ..... 2 MHz
Base clock accuracy 0.01%
Max source frequency ..... 8 MHz
Min source pulse duration..... 60 ns
Min gate pulse duration..... 50 ns
Data transfers ..... Programmed I/O

Digital logic levels .....

Level	Min	Max
Input low voltage	-0.3 V	0.8 V
Input high voltage	2.2 V	5.3 V
Output low voltage (I_{out} = 4 mA)	-	0.45 V
Output high voltage (I_{out} = -1 mA)	3.7 V	-

Triggers

Digital Trigger

Compatibility ..... TTL
Response ..... Rising edge
Pulse width ..... 250 ns

Bus Interface ..... Slave

Power Requirements (from PC)

+5 VDC (±10%) ..... 180 mA
+12 VDC ..... 80 mA
-12 VDC ..... 450 mA
Power available on rear connector ..... +5 V at 1 A max

Physical

Dimensions ..... 16.5 by 9.9 cm. (6.5 by 3.9 in)
I/O connector ..... 50-pin male

Environment

Operating temperature ..... 0° to 70° C
Storage temperature ..... -55° to 150° C
Relative humidity ..... 5% to 90% noncondensing

Appendix B
OKI 82C53 Data Sheet*

This appendix contains the manufacturer data sheet for the OKI 82C53 System Timing Controller integrated circuit (OKI Semiconductor). This circuit is used on the Lab-PC+.

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OKI Semiconductor. *Microprocessor Data Book 1990/1991*.

OKI semiconductor

MSM82C53-2RS/GS/JS

CMOS PROGRAMMABLE INTERVAL TIMER

GENERAL DESCRIPTION

The MSM82C53-2RS/GS/JS are programmable universal timers designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 100μA (max.) when the chip is in the nonselected state. During timer operation, power consumption is still very low with only 8 mA (max.) at 8 MHz of current required.

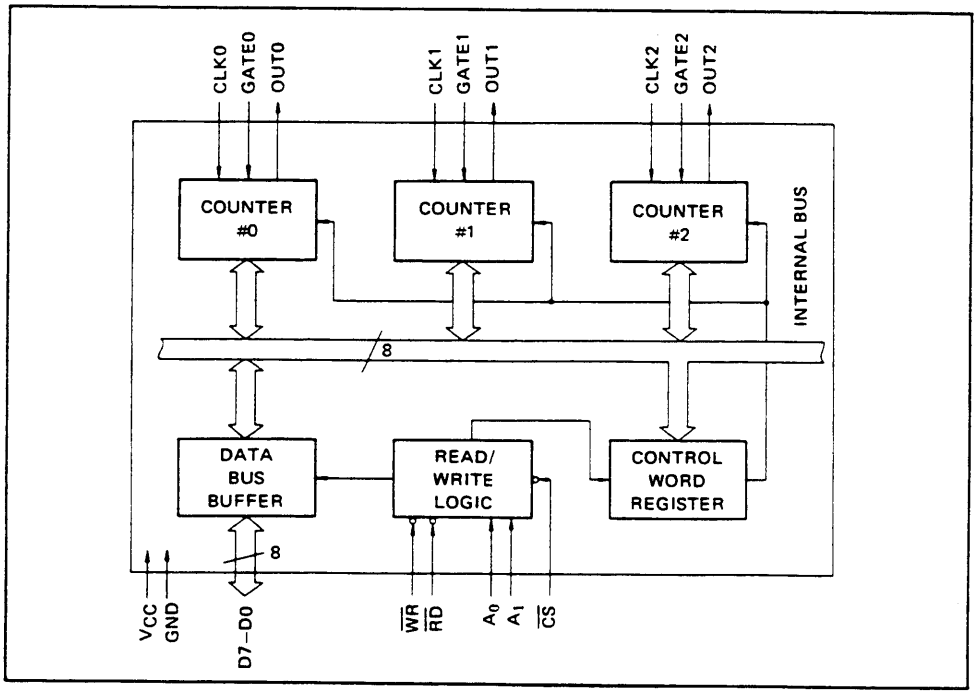
The devices consist of three independent counters, and can count up to a maximum of 8 MHz (MSM82C53-2) The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are freely programmable.

FEATURES

- Maximum operating frequency of 8 MHz (MSM82C53-2)
- High speed and low power consumption achieved through silicon gate CMOS technology.
- Completely static operation
- Three independent 16-bit down-counters
- 3V to 6V single power supply
- Six counter modes available for each counter
- Binary and decimal counting possible
- 24 pin Plastic DIP (DIP24-P-600)
- 28 pin PLCC (QFJ28-P-S450)
- 32 pin-V Plastic SOP (SSOP32-P-430-VK)

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FUNCTIONAL BLOCK DIAGRAM

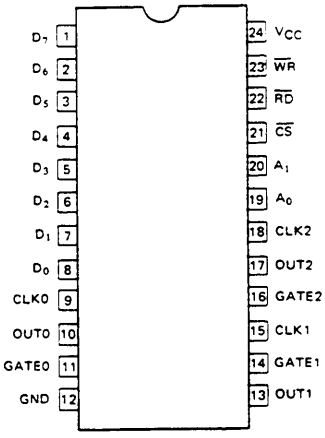


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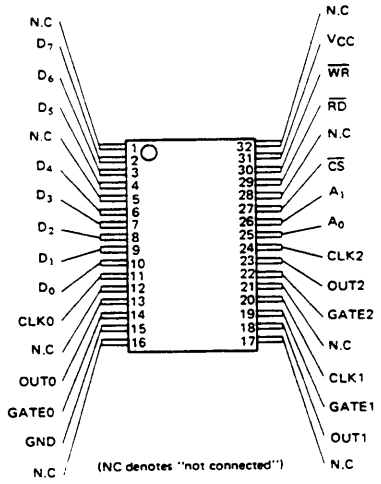
■ MSM82C53-2RS/GS/JS ■

PIN CONFIGURATION

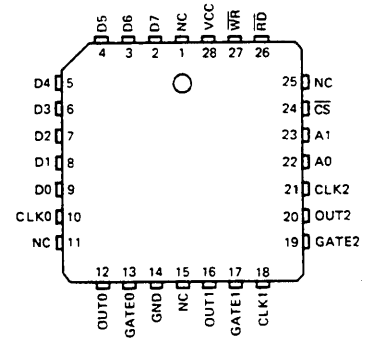
MSM82C53-2RS (Top View)
24 pin Plastic DIP



MSM82C53-2GS (Top View)
32 pin Plastic Small Outine Package



MSM82C53-2JS (Top View)
28 pin Plastic Leaded Chip Carrier



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■ I/O·MSM82C53-2RS/GS/JS ■

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C53-2RS	MSM82C53-2GS	MSM82C53-2JS	
Ssupply Voltage	V_{CC}	Respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}		−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

OPERATING RANGES

Parameter	Symbol	Limits	Conditions	Unit
Supply Voltage	V_{CC}	3 to 6	V_{IL} = 0.2V, V_{IH} = V_{CC} − 0.2V, operating frequency 2.6 MHz	V
Operating Temperature	T_{OP}	−40 to +85		°C

RECOMMENDED OPERATING CONDITIONS

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Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 4mA				0.45	V
"H" Output Voltage	V_{OH}	I_{OH} = −1mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$	V_{CC}=4.5V to 5.5V	−10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$	Ta=−40°C to +85°C	−10		10	μA
Standby Supply Current	I_{CCS}	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IH} \geq V_{CC}$ − 0.2V $V_{IL} \leq$ 0.2V				100	μA
Operating Supply Current	I_{CC}	t_{CLK} = 125 ns C_L = 0pF				8	mA

AC CHARACTERISTICS

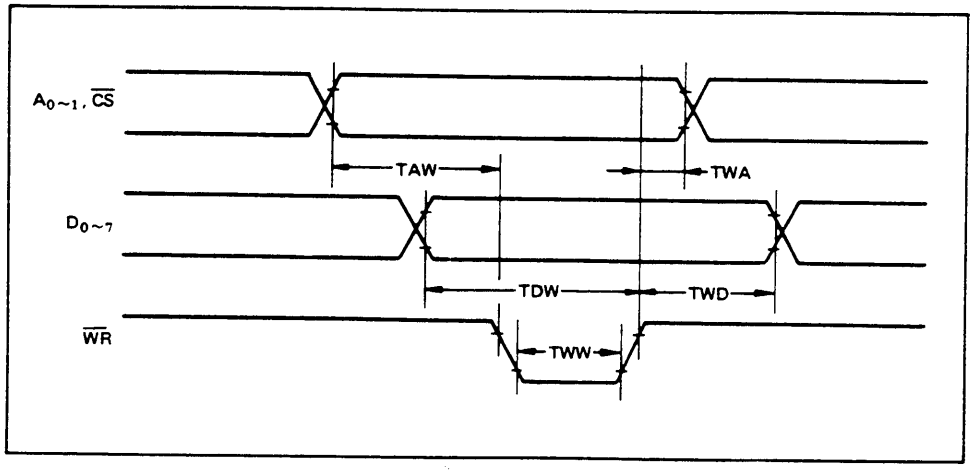
(V_{CC} = 4.5V ~ 5.5V, Ta = –40 ~ +85°C)

Parameter	Symbol	MSM82C53-2 Min.	MSM82C53-2 Max.	Unit	Conditions	
Address Set-up Time before reading	TAR	30		ns	Read cycle	C_L = 150pF
Address Hold Time after reading	TRA	0		ns		
Read Pulse Width	TRR	150		ns		
Read Recovery Time	TRVR	200		ns		
Address Set-up Time before writing	TAW	0		ns	Write cycle	
Address Hold Time after writing	TWA	20		ns		
Write Pulse Width	TWW	150		ns		
Data Input Set-up Time before writing	TDW	100		ns		
Data Input Hold Time after writing	TWD	20		ns		
Write Recovery time	TRVW	200		ns		
Clock Cycle Time	TCLK	125	D.C.	ns	Clock and gate timing	
Clock "H" Pulse Width	TPWH	60		ns		
Clock "L" Pulse Width	TPWL	60		ns		
"H" Gate Pulse Width	TGW	50		ns		
"L" Gate Pulse Width	TGL	50		ns		
Gate Input Set-up Time before clock	TGS	50		ns		
Gate Input Hold Time after clock	TGH	50		ns		
Output Delay Time after reading	TRD		120	ns	Delay time	
Output Floating Delay Time after reading	TDF	5	90	ns		
Output Delay Time after gate	TODG		120	ns		
Output Delay Time after clock	TOD		150	ns		
Output Delay Time after address	TAD		180	ns		

Note: Timing measured at V_L = 0.8V and V_H = 2.2V for both inputs and outputs.

TIME CHART

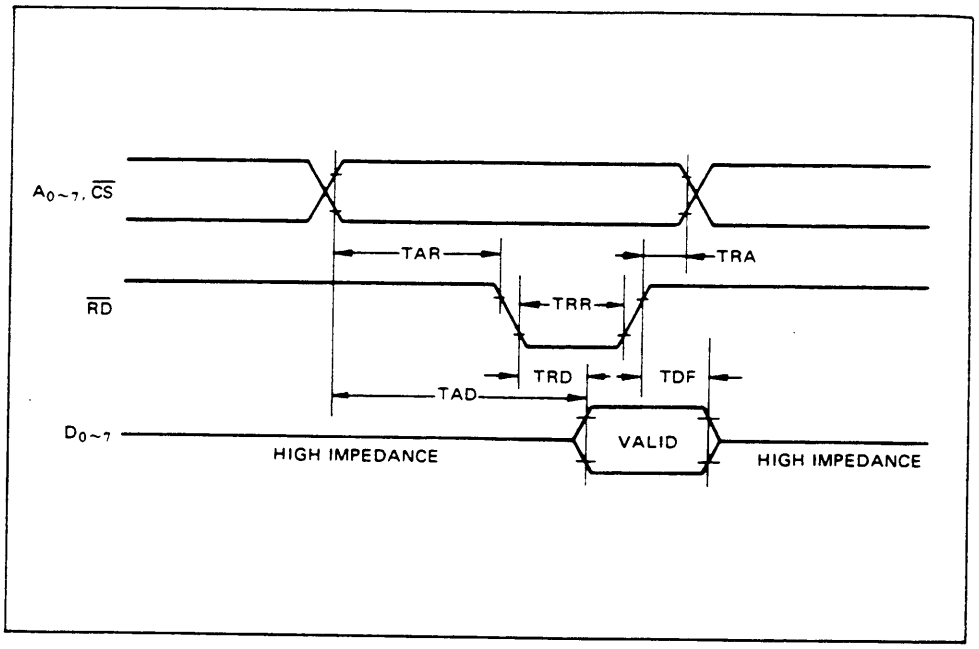
Write Timing



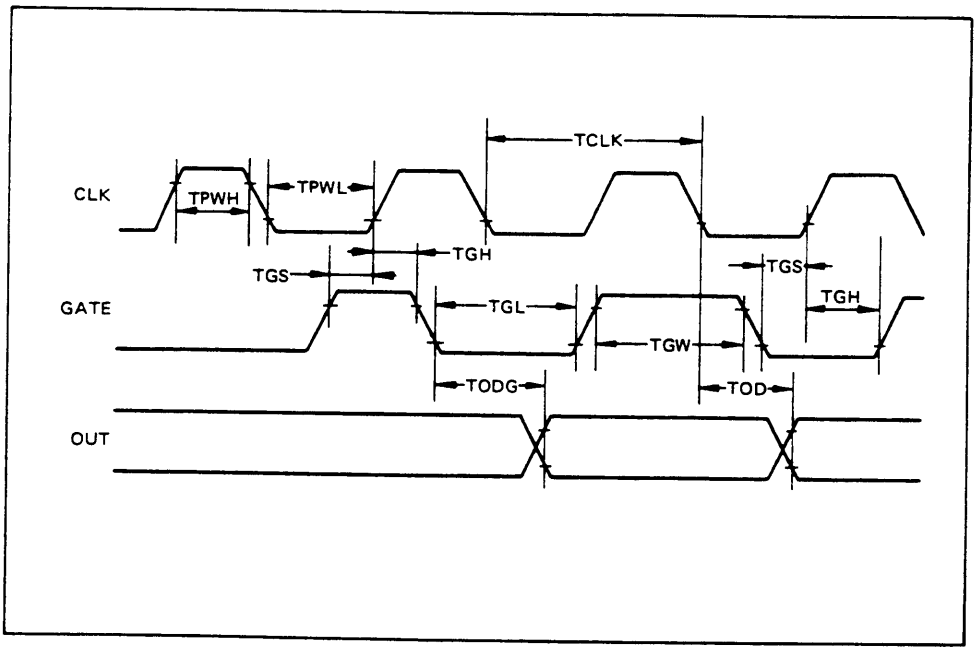
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■ MSM82C53-2RS/GS/JS ■

Read Timing



Clock & Gate Timing

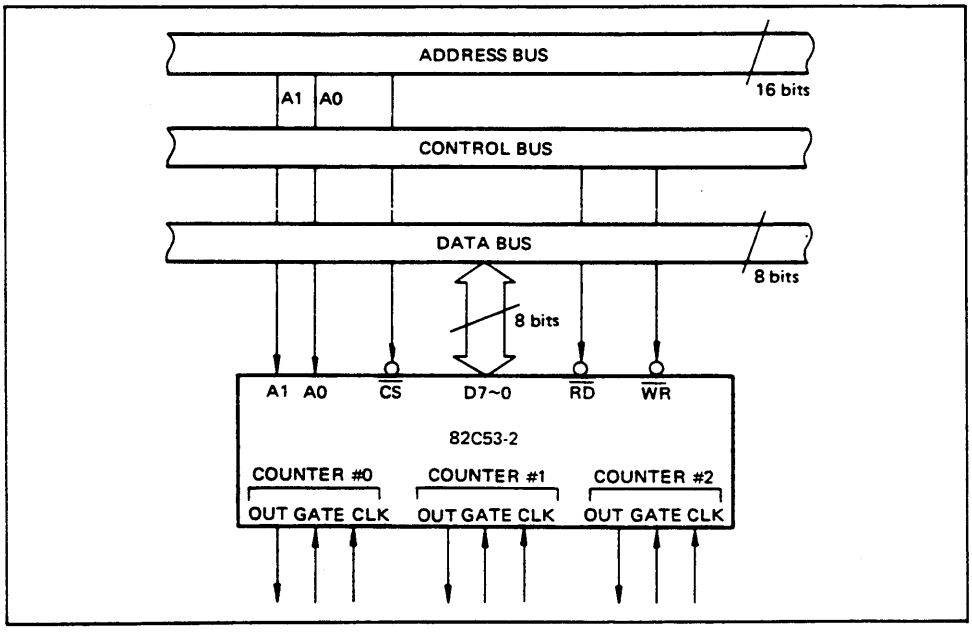


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DESCRIPTION OF PIN FUNCTIONS

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus (D_0 thru D_7) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged.
$\overline{RD}$	Read input	Input	Data can be transferred from MSM82C53 to CPU when this pin is at low level.
$\overline{WR}$	Write input	Input	Data can be transferred from CPU to MSM82C53 when this pin is at low level.
A0, A1	Address input	Input	One of the three internal counters or the control word register is selected by A0/A1 combination. These two pins are normally connected to the two lower order bits of the address bus.
CLK0~2	Clock input	Input	Supply of three clock signals to the three counters incorporated in MSM82C53.
GATE0~2	Gate input	Input	Control of starting, interruption, and restarting of counting in the three respective counters in accordance to the set control word contents.
OUT0~2	Counter output	Output	Output of counter output waveform in accordance with the set mode and count value.

SYSTEM INTERFACING



■ I/O·MSM82C53-2RS/GS/JS ■

DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Function
0	1	0	0	0	Data bus to counter # 0 Writing
0	1	0	0	1	Data bus to counter # 1 Writing
0	1	0	1	0	Data bus to counter # 2 Writing
0	1	0	1	1	Data bus to control word register Writing
0	0	1	0	0	Data bus from counter # 0 Reading
0	0	1	0	1	Data bus from counter # 1 Reading
0	0	1	1	0	Data bus from counter # 2 Reading
0	0	1	1	1	Data bus in high impedance status
1	x	x	x	x	
0	1	1	x	x	

x denotes "not specified".

DESCRIPTION OF OPERATION

82C53 functions are selected by a control word from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

Control Word and Count Value Program

Each counter operation mode is set by control word programming. The control word format is outlined below.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
Select Counter		Read/Load		Mode			BCD

($\overline{CS}$ = 0, A0, A1 = 1,1, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

- **Select Counter (SC0, SC1):** Selection of set counter

SC1	SC0	Set Contents
0	0	Counter # 0 selection
0	1	Counter # 1 selection
1	0	Counter # 2 selection
1	1	Illegal combination

- **Read/Load (RL1, RL0):** Count value Reading/Loading format setting

RL1	RL0	Set Contents
0	0	Counter Latch operation
0	1	Reading/Loading of Least Significant byte (LSB)
1	0	Reading/Loading of Most Significant byte (MSB)
1	1	Reading/Loading of LSB followed by MSB

- **Mode (M2, M1, M0):** Operation waveform mode setting

M2	M1	M0	Set Contents
0	0	0	Mode 0 (Interrupt on Terminal Count)
0	0	1	Mode 1 (Programmable One-Shot)
x	1	0	Mode 2 (Rate Generator)
x	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (Software Triggered Strobe)
1	0	1	Mode 5 (Hardware Triggered Strobe)

x denotes "not specified".

- **BCD:** Operation count mode setting

BCD	Set Contents
0	Binary Count (16-bits Binary)
1	BCD Count (4-decades Binary Coded Decimal)

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, counting is started immediately after the count value has been written). This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to OOOOH during control word setting. The counter value (OOOOH) can.t be read.

If the two bytes (LSB and MSB) are written at this stage (RL0 and RL1 = 1,1), take note of the following precaution.

Although the count values may be set in the three counters in any sequence after the control word has been set in each counter, count values must be set consecutively in the LSB – MSB order in any one counter.

- **Example of control word and count value setting**

  Counter # 0: Read/Load LSB only, Mode 3, Binary count, count value 3H
  Counter # 1: Read/Load MSB only, Mode 5, Binary count, count value AA00H
  Counter # 2: Read/Load LSB and MSB, Mode 0, BCD count, count value 1234

```
MVI A, 1EH
OUT n3          Counter #0 control word setting
MVI A, 6AH
OUT n3          Counter #1 control word setting
MVI A, B1H
OUT n3          Counter #2 control word setting
MVI A, 03H
OUT n0          Counter #0 count value setting
MVI A, AAH
OUT n1          Counter #1 count value setting
MVI A, 34H
OUT n2          Counter #2 count value setting
MVI A, 12H      (LSB then MSB)
OUT n2
```

Note: n0: Counter #0 address
n1: Counter #1 address
n2: Counter #2 address
n3: Control word register address

- **The minimum and maximum count values which can be counted in each mode are listed below.**

Mode	Min.	Max.	Remarks
0	1	0	0 executes 10000H count (ditto in other modes)
1	1	0	
2	2	0	1 cannot be counted
3	2	1	1 executes 10001H count
4	1	0	
5	1	0	

Mode Definition

- **Mode 0 (terminal count)**

The counter output is set to "L" level by the mode setting. If the count value is then written in the counter with the gate input at "H" level (that is, upon completion of writing the MSB when there are two bytes), the clock input counting is started. When the terminal count is reached, the output is switched to "H" level and is maintained in this status until the control word and count value are set again.

Counting is interrupted if the gate input is switched to "L" level, and restarted when switched back to "H" level.

When Count Values are written during counting, the operation is as follows:

1 byte Read/Load.... When the new count value is written, counting is stopped immediately, and then restarted at the new count value by the next clock.

2-byte Read/Load.... When byte 1 (LSB) of the new count value is written, counting is stopped immediately. Counting is restarted at the new count value when byte 2 (MSB) is written.

- **Mode 1 (programmable one-shot)**

The counter output is switched to "H" level by the mode setting. Note that in this mode, counting is not started if only the count value is written. Since counting has to be started in this mode by using the leading edge of the gate input as a trigger, the counter output is switched to "L" level by the next clock after the gate input trigger. This "L" level status is maintained during the set count value, and is switched back to "H" level when the terminal count is reached.

Once counting has been started, there is no interruption until the terminal count is reached, even if the gate input is switched to "L" level in the meantime. And although counting continues even if a new count value is written during the counting, counting is started at the new count value if another trigger is applied by the gate input.

- **Mode 2 (rate generator)**

The counter output is switched to "H" level by the mode setting. When the gate input is at "H" level, counting is started by the next clock after the count value has been written. And if the gate input is at "L" level, counting is started by using the rising edge of the gate input as a trigger after the count value has been set.

An "L" level output pulse appears at the counter output during a single clock duration once every n clock inputs where n is the set count value. If a new count value is written during while counting is in progress, counting is started at the new count value following output of the pulse currently being counted. And if the gate input is switched to "L" level during counting, the counter output is forced to switch to "H" level, the counting being restarted by the rising edge of the gate input.

- **Mode 3 (square waveform rate generator)**

The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 2 above.

The repeated square wave output appearing at the counter output contains half the number of counts as the set count value. If the set count value (n) is an odd number, the repeated square wave output consists of only (n + 1)/2 clock inputs at "H" level and (n – 1)/2 clock inputs at "L" level.

If a new count value is written during counting, the new count value is reflected immediately after the

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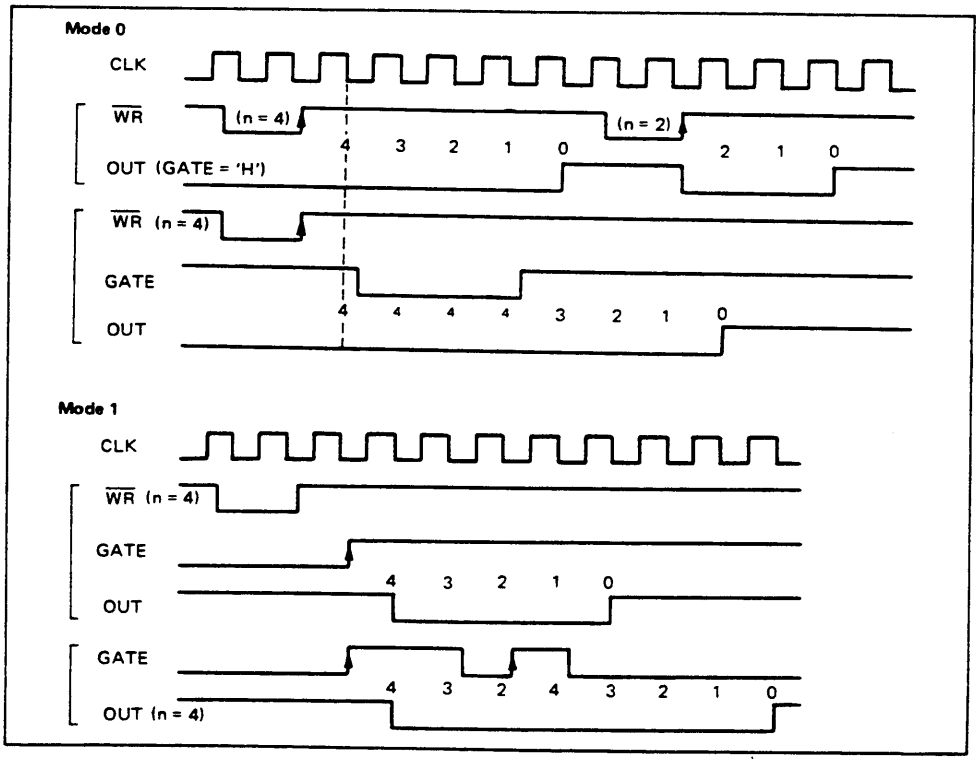
■ I/O·MSM82C53-2RS/GS/JS ■

change ("H" to "L" or "L" to "H") in the next counter output to be executed. The counting operation at the gate input is done the same as in mode 2.

- **Mode 4 (software trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 0. A single "L" pulse equivalent to one clock width is generated at the counter output when the terminal count is reached.
  This mode differs from 2 in that the "L" level output appears one clock earlier in mode 2, and that pulses are not repeated in mode 4. Counting is stopped when the gate input is switched to "L" level, and restarted from the set count value when switched back to "H" level.

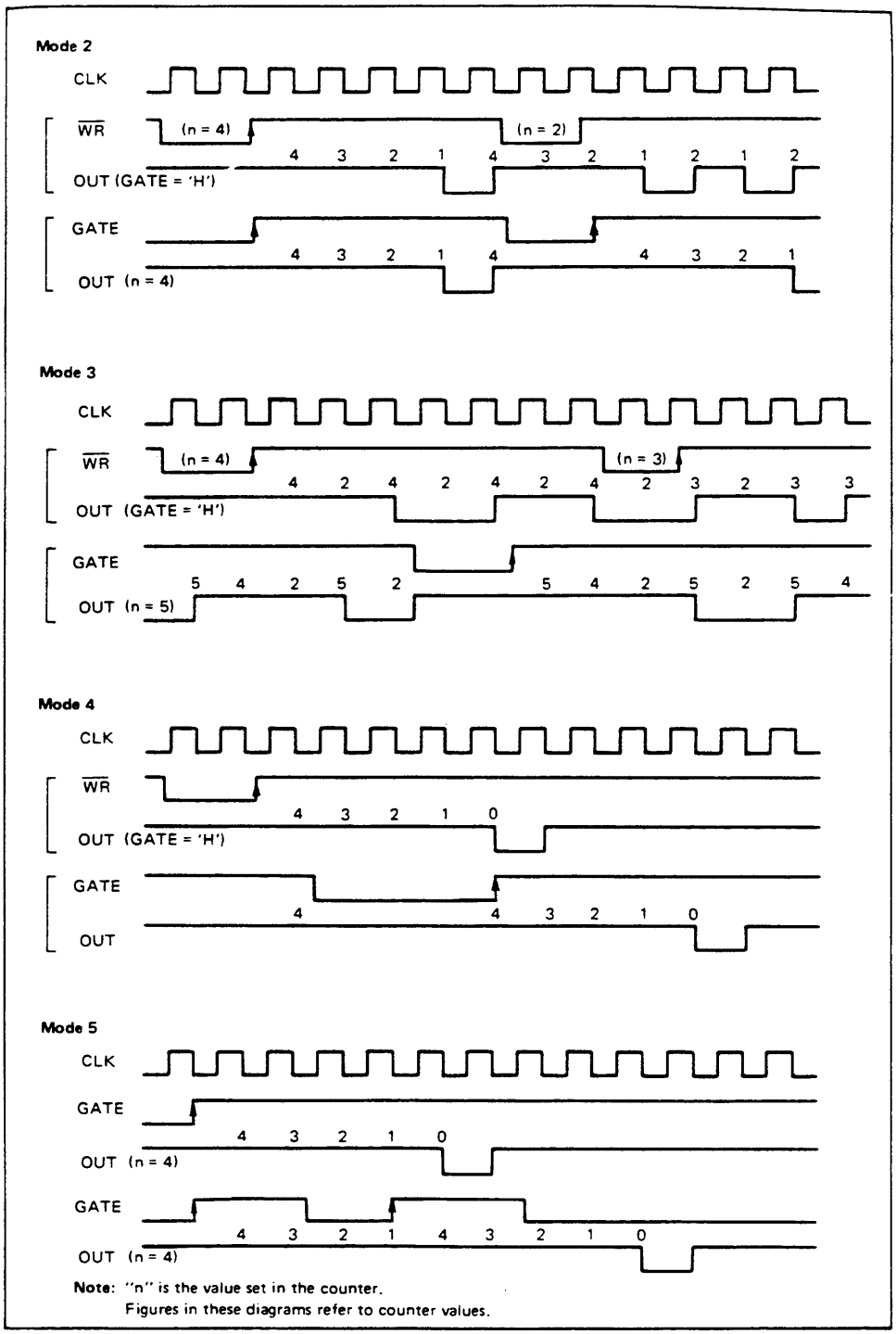
- **Mode 5 (hardware trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started, and the gate input used, in the same way as in mode 1.
  The counter output is identical to the mode 4 output.
  The various roles of the gate input signals in the above modes are summarized in the following table.

Mode \ Gate	"L" Level Falling Edge	Rising Edge	"H" Level
0	Counting not possible		Counting possible
1		(1) Start of counting (2) Retriggering	
2	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
3	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
4	Counting not possible		Counting possible
5		(1) Start of counting (2) Retriggering	



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Note: "n" is the value set in the counter.
Figures in these diagrams refer to counter values.

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Reading of Counter Values

All 82C53 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, and (2) counter latching ("read on the fly").

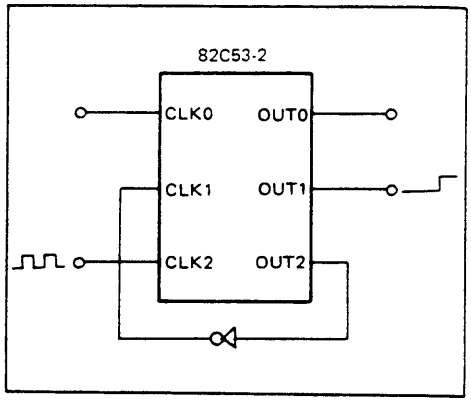
- **Direct reading**
  Counter values can be read by direct reading operations.
  Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.

- **Counter latching**
  In this method, the counter value is latched by writing a counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. An example of a counter latching program is given below.
  Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A  01 00 x x x x
            └── Denotes counter latching
OUT n3 ──┬── Write in control word address (n3)
         └── The counter value at this point is latched
IN n1  ──┬── Reading of the LSB of the counter value latched from counter #1.
         └── n1: Counter #1 address
MOV B, A
IN n1  ──── Reading of MSB from counter #1.
MOV C, A
```

Example of Practical Application

- 82C53 used as a 32-bit counter.



Use counter #1 and counter #2

Counter #1: mode 0, upper order 16-bit counter value

Counter #2: mode 2, lower order 16-bit counter value

This setting enables counting up to a maximum of 2^{32}.

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Appendix C
OKI 82C55A Data Sheet*

This appendix contains the manufacturer data sheet for the OKI 82C55A Programmable Peripheral Interface integrated circuit (OKI Semiconductor). This circuit is used on the Lab-PC+.

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OKI semiconductor

MSM82C55A-2RS/GS/VJS

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

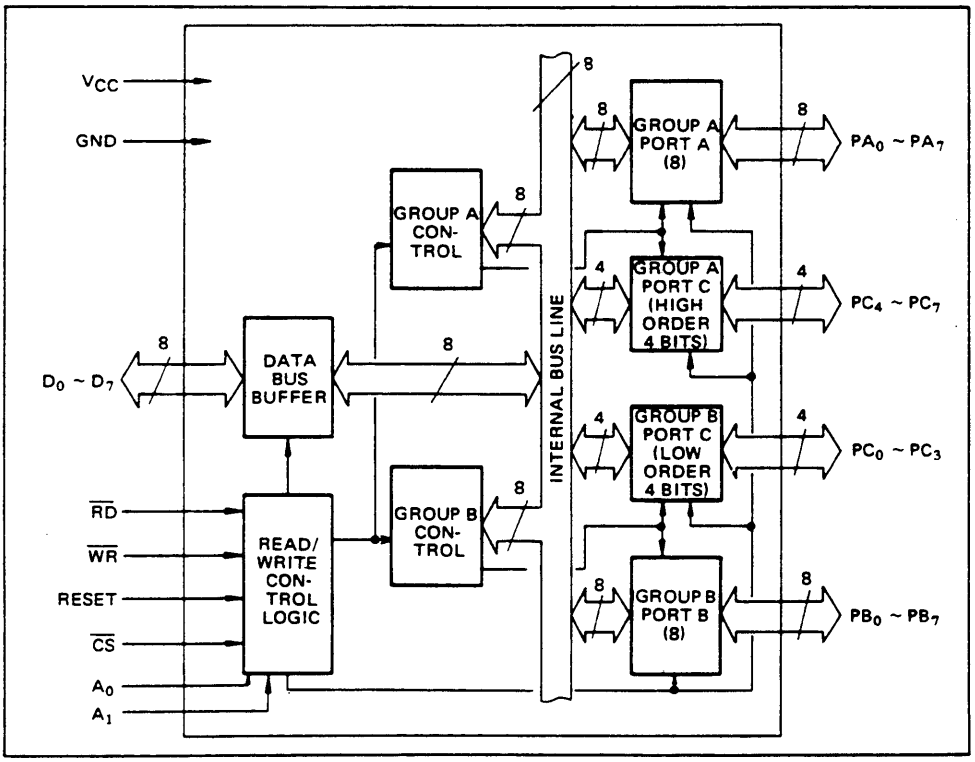
GENERAL DESCRIPTION

The MSM82C55A is a programmable universal I/O interface device which operates as high speed and on low power consumption due to 3 μ silicon gate CMOS technology. It is the best fit as an I/O port in a system which employs the 8-bit parallel processing MSM80C85A CPU. This device has 24-bit I/O pins equivalent to three 8-bit I/O ports and all inputs/outputs are TTL interface compatible.

FEATURES

- High speed and low power consumption due to 3 μ silicon gate CMOS technology
- 3 V to 6 V single power supply
- Full static operation
- Programmable 24-bit I/O ports
- Bidirectional bus operation (Port A)
- Bit set/reset function (Port C)
- TTL compatible
- Compatible with 8255A-5
- 40 pin Plastic DIP (DIP40-P-600)
- 44 pin PLCC (QFJ44-P-S650)
- 44 pin-V Plastic QFP (QFP44-P-910-VK)
- 44 pin-VI Plastic QFP (QFP44-P-910-VIK)

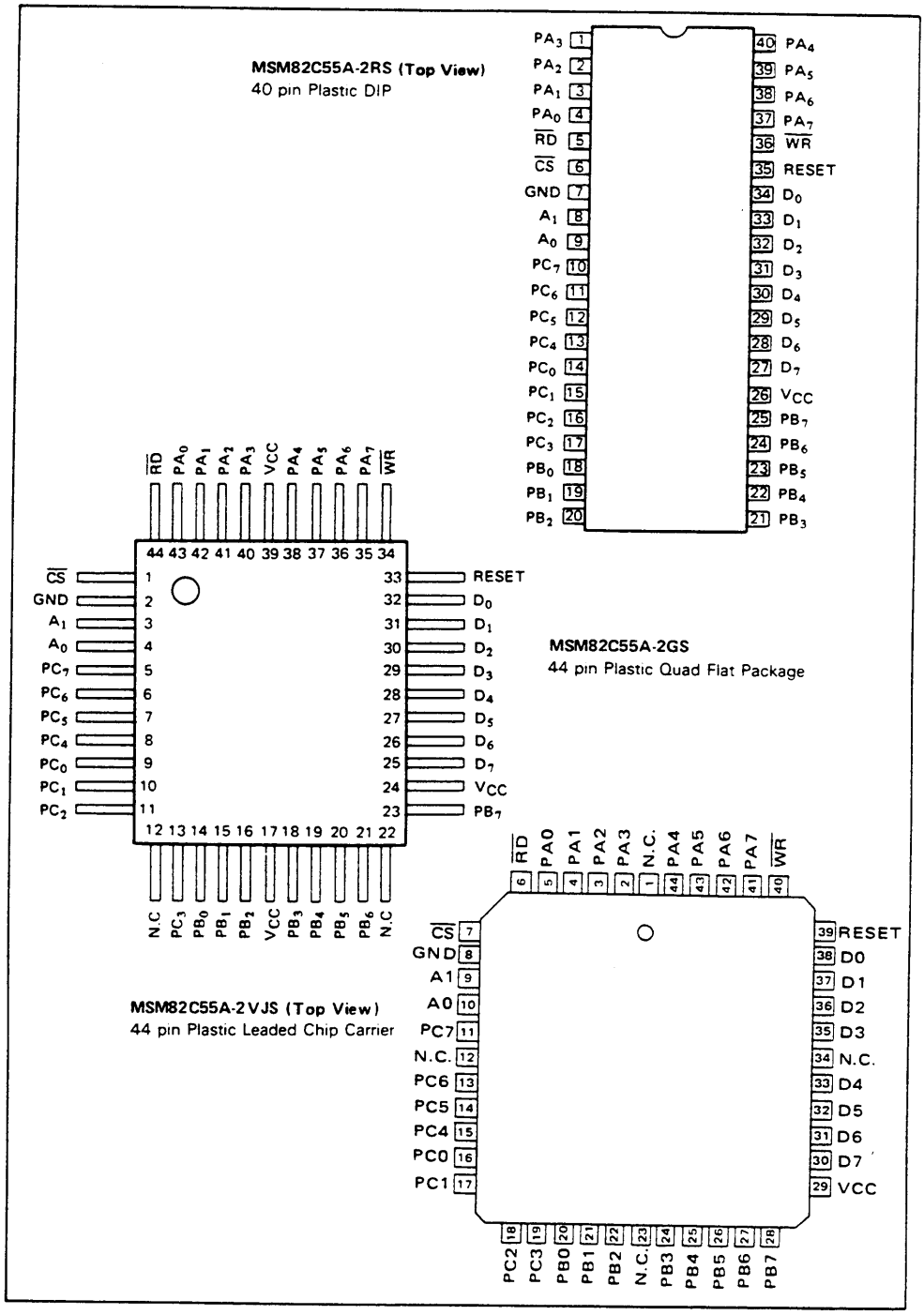
CIRCUIT CONFIGURATION



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PIN CONFIGURATION



I/O·MSM82C55A-2RS/GS/VJS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C55A-2RS	MSM82C55A-2GS	MSM82C55A-2VJS	
Ssupply Voltage	V_{CC}	Ta = 25°C with respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}	−	−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	−40 to 85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

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DC CHARACTERISTICS

Parameter	Symbol	Conditions		MSM82C55A-2 Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC} = 4.5V to 5.5V, Ta = −40°C to +85°C, (C_L = 0pF)			0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = −40 μA		4.2			V
		I_{OH} = −2.5 mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−1		1	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Supply Current (standby)	I_{CCS}	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IH} \geq V_{CC}$ −0.2V $V_{IL} \leq$ 0.2V			0.1	10	μA
Average Supply Current (active)	I_{CC}	I/O wire cycle 82C55A-2 ... 8MHz CPU timing				8	mA

■ I/O·MSM82C55A-2RS/GS/VJS ■

AC CHARACTERISTICS

(V_{CC} = 4.5 to 5.5V, Ta = -40 to +80°C)

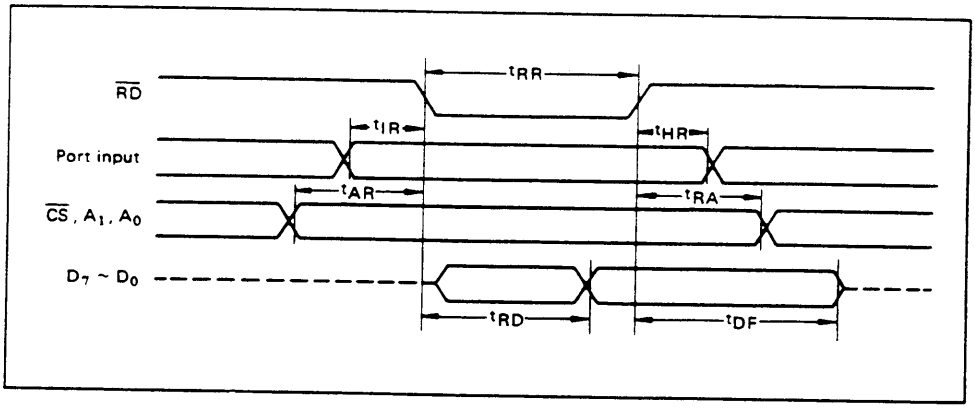
Parameter	Symbol	MSM82C55A-2		Unit	Remarks
		Min.	Max.		
Setup Time of address to the falling edge of $\overline{RD}$	t_{AR}	20		ns	
Hold Time of address to the rising edge of $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	100		ns	
Delay Time from the falling edge of $\overline{RD}$ to the output of defined data	t_{RD}		120	ns	
Delay Time from the rising edge of $\overline{RD}$ to the floating of data bus	t_{DF}	10	75	ns	
Time from the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next falling edge of $\overline{RD}$ or $\overline{WR}$	t_{RV}	200		ns	
Setup Time of address before the falling edge of $\overline{WR}$	t_{AW}	0		ns	
Hold Time of address after the rising edge or $\overline{WR}$	t_{WA}	20		ns	
$\overline{WR}$ Pulse Width	t_{WW}	150		ns	
Setup Time of bus data before the rising edge of $\overline{WR}$	t_{DW}	50		ns	
Holt Time of bus data after the rising edge of $\overline{WR}$	t_{WD}	30		ns	
Delay Time from the rising edge of $\overline{WR}$ to the output of defined data	t_{WB}		200	ns	
Setup Time of port data before the falling edge of $\overline{RD}$	t_{IR}	20		ns	
Hold Time of port data after the rising edge of $\overline{RD}$	t_{HR}	10		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	100		ns	
$\overline{STB}$ Pulse Width	t_{ST}	100		ns	Load 150 pF
Setup Time of port data before the rising edge of $\overline{STB}$	t_{PS}	20		ns	
Hold Time of port data after the rising edge of $\overline{STB}$	t_{PH}	50		ns	
Delay Time from the falling edge of $\overline{ACK}$ to the output of defined data	t_{AD}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the floating of port (Port A in mode 2)	t_{KD}	20	250	ns	
Delay Time from the rising edge of WR to the falling edge of $\overline{OBF}$	t_{WOB}		150	ns	
Delay Time from the falling edge of ACK to the rising edge of $\overline{OBF}$	t_{AOB}		150	ns	
Delay Time from the falling edge of STB to the rising edge of IBF	t_{SIB}		150	ns	
Delay Time from the rising edge of $\overline{RD}$ to the falling edge of IBF	t_{RIB}		150	ns	
Delay Time from the falling edge of $\overline{RD}$ to the falling edge of INTR	t_{RIT}		200	ns	
Delay Time from the rising edge of $\overline{STB}$ to the rising edge of INTR	t_{SIT}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the rising edge of INTR	t_{AIT}		150	ns	
Delay Time from the falling edge of $\overline{WR}$ to the falling edge of INTR	t_{WIT}		250	ns	

Note: Timing is measured at V_L = 0.8 V and V_H = 2.2 V for both input and outputs.

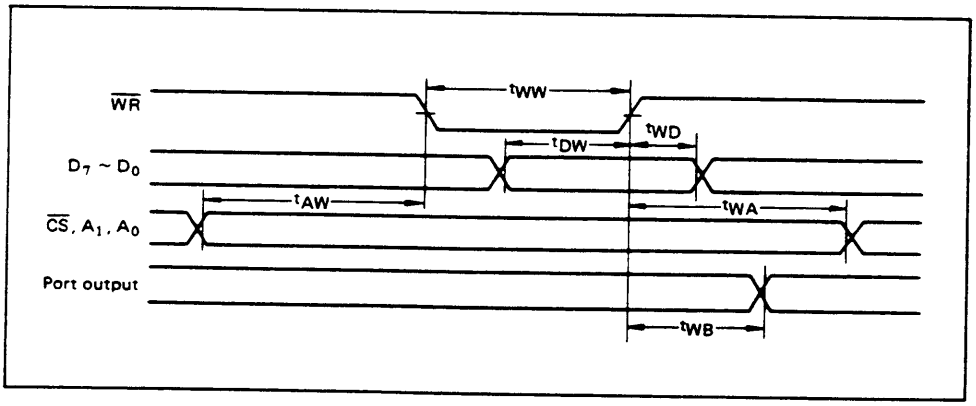
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Basic Input Operation (Mode 0)

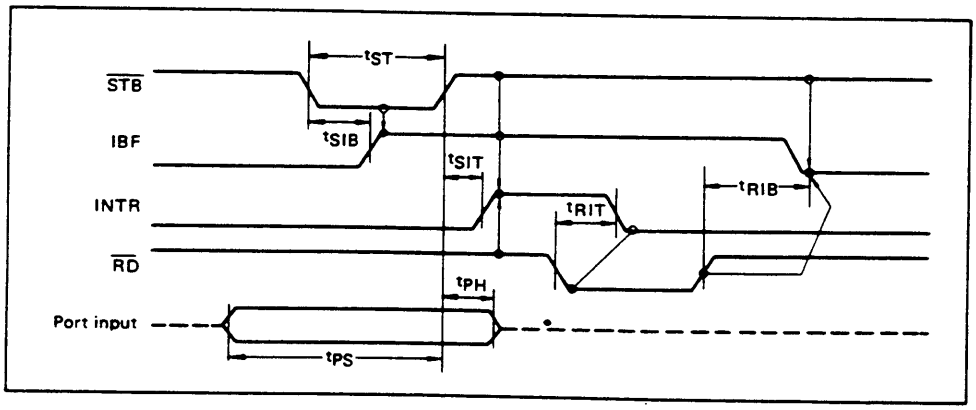


Basic Output Operation (Mode 0)



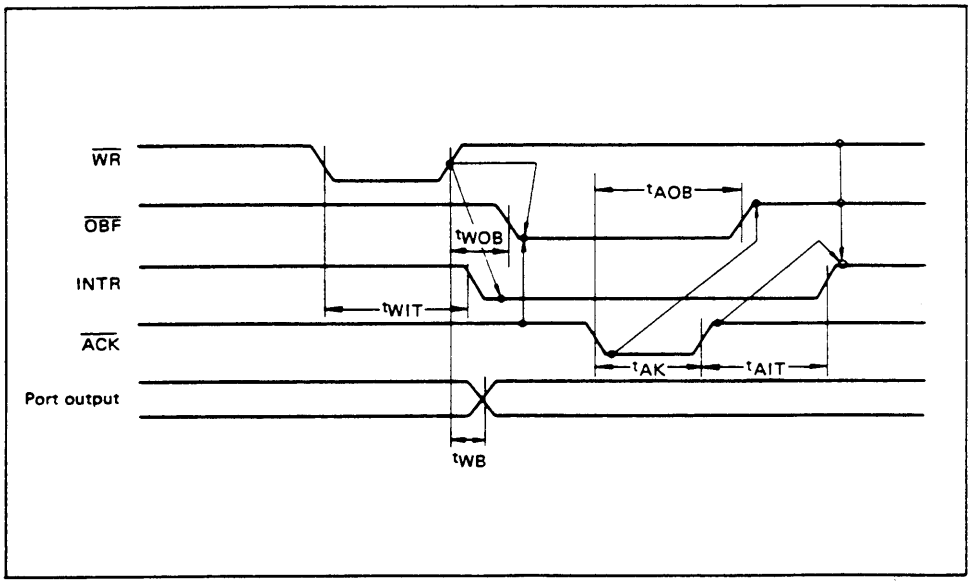
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Strobe Input Operation (Mode 1)

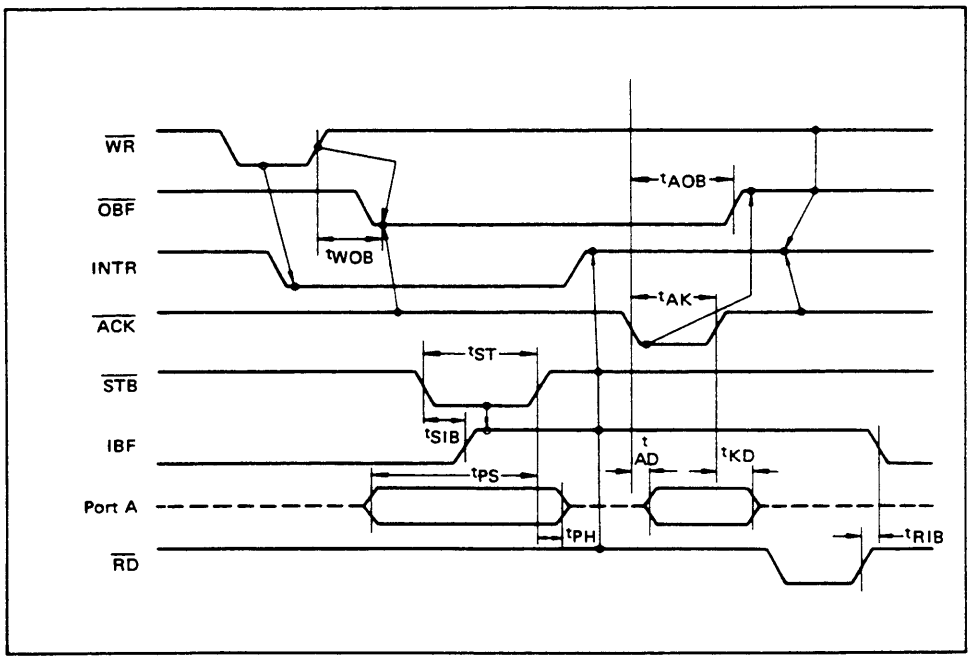


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Strobe Output Operation (Mode 1)

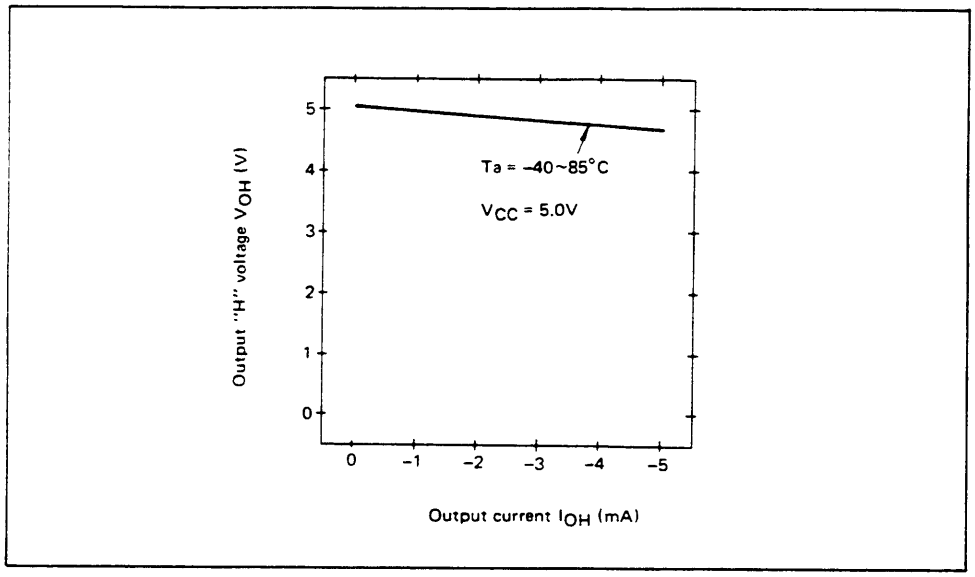


Bidirectional Bus Operation (Mode 2)

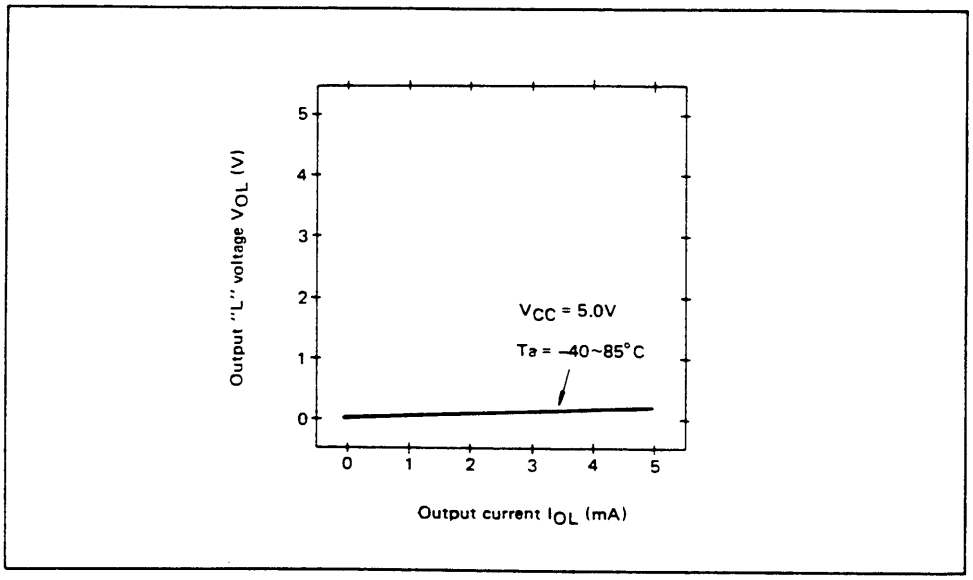


OUTPUT CHARACTERISTICS (REFERENCE VALUE)

1 **Output "H" Voltage (V_{OH}) vs. Output Current (I_{OH})**



2 **Output "L" Voltage (V_{OL}) vs. Output Current (I_{OL})**



Note: The direction of flowing into the device is taken as positive for the output current.

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■ I/O·MSM82C55A-2RS/GS/VJS ■

FUNCTIONAL DESCRIPTION OF PIN

Pin No.	Item	Input/Output	Function
D7 ~ D0	Bidirectional data bus	Input and output	These are three-state 8-bit bidirectional buses used to write and read data upon receipt of the $\overline{WR}$ and $\overline{RD}$ signals from CPU and also used when control words and bit set/reset data are transferred from CPU to MSM82C55A.
RESET	Reset input	Input	This signal is used to reset the control register and all internal registers when it is in high level. At this time, ports are all made into the input mode (high impedance status). all port latches are cleared to 0 and all ports groups are set to mode 0
$\overline{CS}$	Chip select input	Input	When the $\overline{CS}$ is in low level, data transmission is enabled with CPU. When it is in high level, the data bus is made into the high impedance status where no write nor read operation is performed. Internal registers hold their previous status, however.
$\overline{RD}$	Read input	Input	When RD is in low level, data is transferred from MSM82C55A to CPU.
$\overline{WR}$	Write input	Input	When WR is in low level, data or control words are transferred from CPU to MSM82C55A.
A0, A1	Port select input (address)	Input	By combination of A0 and A1, either one is selected from among port A, port B, port C, and control register. These pins are usually connected to low order 2 bits of the address bus.
PA7 ~ PA0	Port A	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word. Especially, port A can be used as a bidirectional port when it is set to mode 2.
PB7 ~ PB0	Port B	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word.
PC7 ~ PC0	Port C	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word as 2 ports with 4 bits each. When port A or port B is used in mode 1 or mode 2 (port A only), they become control pins. Especially when port C is used as an output port, each bit can be set/reset independently.
V_{CC}			+5 V power supply.
GND			GND

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BASIC FUNCTIONAL DESCRIPTION

Group A and Group B

When setting a mode to a port having 24 bits, set it by dividing it into two groups of 12 bits each.

Group A: Port A (8 bits) and high order 4 bits of port C (PC7 ~ PC4)

Group B: Port B (8 bits) and low order 4 bits of port C (PC3 ~ PC0)

Mode 0, 1, 2

There are 3 types of modes to be set by grouping as follows:

Mode 0: Basic input operation/output operation (Available for both groups A and B)

Mode 1: Strobe input operation/output operation (Available for both groups A and B)

Mode 2: Bidirectional bus operation (Available for group A only)

When used in mode 1 or mode 2, however, port C has bits to be defined as ports for control signal for operation ports (port A for group A and port B for group B) of their respective groups.

Port A, B, C

The internal structure of 3 ports is as follows:

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input)

Single bit set/reset function for port C

When port C is defined as an output port, it is possible to set (to turn to high level) or reset (to turn to low level) any one of 8 bits individually without affecting other bits.

OPERATIONAL DESCRIPTION

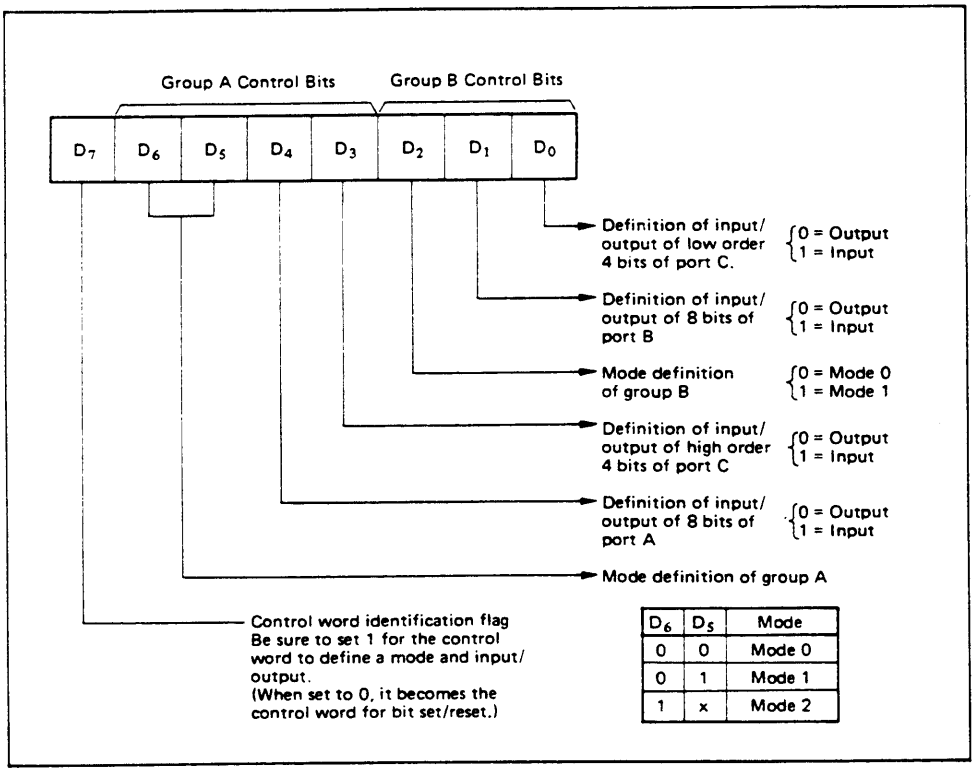
Control Logic

Operations by addresses and control signals, e.g., read and write, etc. are as shown in the table below:

Operation	A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Operation
Input	0	0	0	1	0	Port A → Data Bus
	0	1	0	1	0	Port B → Data Bus
	1	0	0	1	0	Port C → Data Bus
Output	0	0	0	0	1	Data Bus → Port A
	0	1	0	0	1	Data Bus → Port B
	1	0	0	0	1	Data Bus → Port C
Control	1	1	0	0	1	Data Bus → Control Register
Others	1	1	0	1	0	Illegal Condition
	x	x	1	x	x	Data bus is in the high impedance status.

Setting of Control Word

The control register is composed of 7-bit latch circuit and 1-bit flag as shown below.



D_6	D_5	Mode
0	0	Mode 0
0	1	Mode 1
1	x	Mode 2

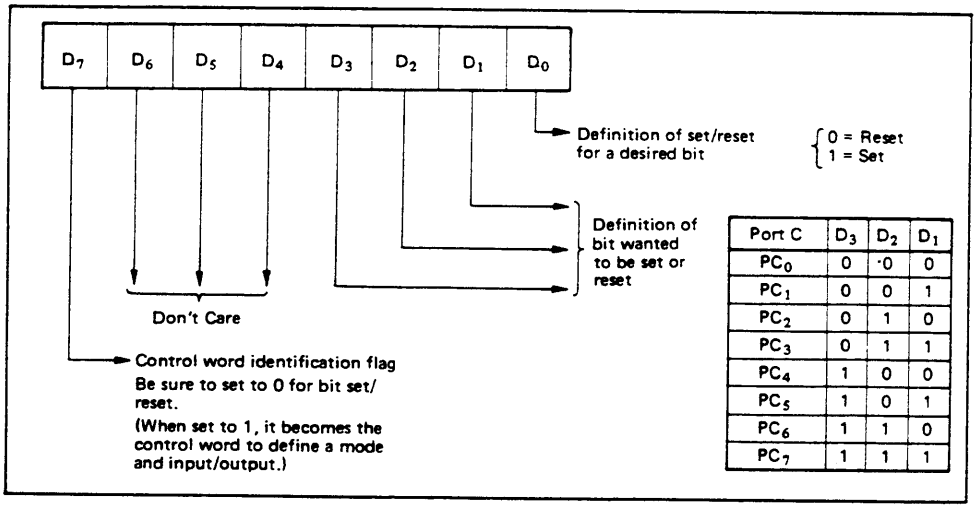
Precaution for mode selection

The output registers for ports A and C are cleared to ϕ each time data is written in the command register and the mode is changed, but the port B state is undefined.

Bit Set/Reset Function

When port C is defined as output port, it is possible to set (set output to 1) or reset (set output to 0) any one of 8 bits without affecting other bits as shown next page.

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Port C	D_3	D_2	D_1
PC_0	0	0	0
PC_1	0	0	1
PC_2	0	1	0
PC_3	0	1	1
PC_4	1	0	0
PC_5	1	0	1
PC_6	1	1	0
PC_7	1	1	1

Interrupt Control Function

When the MSM82C55A is used in mode 1 or mode 2, the interrupt signal for the CPU is provided. The interrupt request signal is output from port C. When the internal flip-flop INTE is set beforehand at this time, the desired interrupt request signal is output. When it is reset beforehand, however, the interrupt request signal is not output. The set/reset of the internal flip-flop is made by the bit set/reset operation for port C virtually.

Bit set → INTE is set → Interrupt allowed
Bit reset → INTE is reset → Interrupt inhibited

Operational Description by Mode

1. Mode 0 (Basic input/output operation)

Mode 0 makes the MSM82C55A operate as a basic input port or output port. No control signals such as interrupt request, etc. are required in this mode. All 24 bits can be used as two-8-bit ports and two 4-bit ports. Sixteen combinations are then possible for inputs/outputs. The inputs are not latched, but the outputs are.

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Type	Control Word								Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	High Order 4 Bits of Port C	Port B	Low Order 4 Bits of Port C
1	1	0	0	0	0	0	0	0	Output	Output	Output	Output
2	1	0	0	0	0	0	0	1	Output	Output	Output	Input
3	1	0	0	0	0	0	1	0	Output	Output	Input	Output
4	1	0	0	0	0	0	1	1	Output	Output	Input	Input
5	1	0	0	0	1	0	0	0	Output	Input	Output	Output
6	1	0	0	0	1	0	0	1	Output	Input	Output	Input
7	1	0	0	0	1	0	1	0	Output	Input	Input	Output
8	1	0	0	0	1	0	1	1	Output	Input	Input	Input
9	1	0	0	1	0	0	0	0	Input	Output	Output	Output
10	1	0	0	1	0	0	0	1	Input	Output	Output	Input
11	1	0	0	1	0	0	1	0	Input	Output	Input	Output
12	1	0	0	1	0	0	1	1	Input	Output	Input	Input
13	1	0	0	1	1	0	0	0	Input	Input	Output	Output
14	1	0	0	1	1	0	0	1	Input	Input	Output	Input
15	1	0	0	1	1	0	1	0	Input	Input	Input	Output
16	1	0	0	1	1	0	1	1	Input	Input	Input	Input

Note: When used in mode 0 for both groups A and B

2. Mode 1 (Strobe input/output operation)

In mode 1, the strobe, interrupt and other control signals are used when input/output operations are made from a specified port. This mode is available for both groups A and B. In group A at this time, port A is used as the data line and port C as the control signal.

Following is a descrption of the input operation in mode 1.

$\overline{STB}$ (Strobe input)

- When this signal is low level, the data output from terminal to port is fetched into the internal latch of the port. This can be made independent from the CPU, and the data is not output to the data bus until the RD signal arrives from the CPU.

IBF (Input buffer full flag output)

- This is the response signal for the $\overline{STB}$. This signal when turned to high level indicates that data is fetched into the input latch. This signal turns to high level at the falling edge of $\overline{STB}$ and to low level at the rising edge of $\overline{RD}$.

INTR (Interrupt request output)

- This is the interrupt request signal for the CPU of the data fetched into the input latch. It is indicated by high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{STB}$ (IBF = 1 at this time) and low level at the falling edge of the $\overline{RD}$ when the INTE is set.

$INTE_A$ of group A is set when the bit for PC_4 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Following is a description of the output operation of mode 1.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data is written to the specified port upon receipt of the $\overline{WR}$ signal from the CPU. This signal turns to low level at the rising edge of the WR and high level at the falling edge of the ACK.

$\overline{ACK}$ (Acknowledge input)

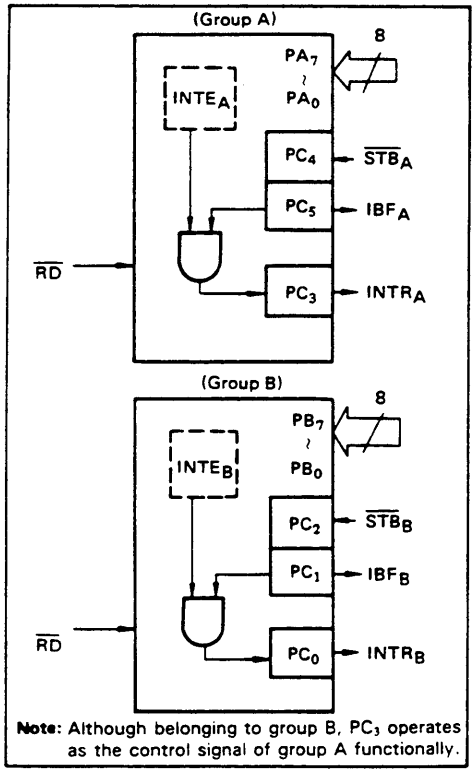
- This signal when turned to low level indicates that the terminal has received data.

INTR (Interrupt request output)

- This is the signal used to interrupt the CPU when a terminal receives data from the CPU via the MSM82C55A-5. It indicates the occurrence of the interrupt in high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{ACK}$ (OBF = 1 at this time) and low level at the falling edge of $\overline{WR}$ when the $INTE_B$ is set.

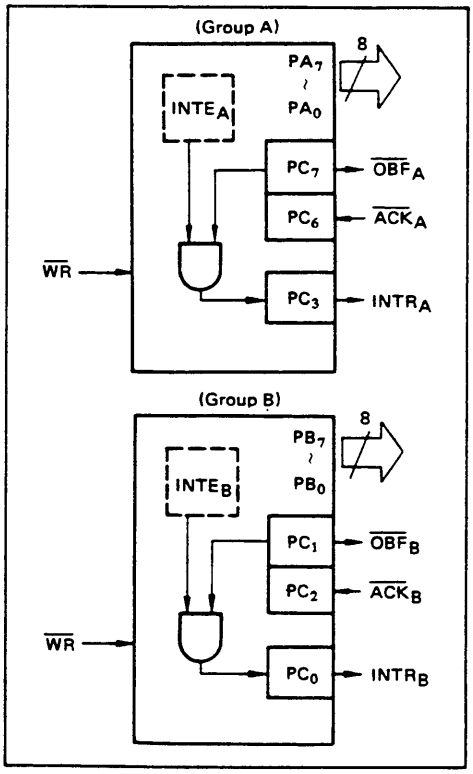
$INTE_A$ of group A is set when the bit for PC_6 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Mode 1 Input



Note: Although belonging to group B, PC_3 operates as the control signal of group A functionally.

Mode 1 output



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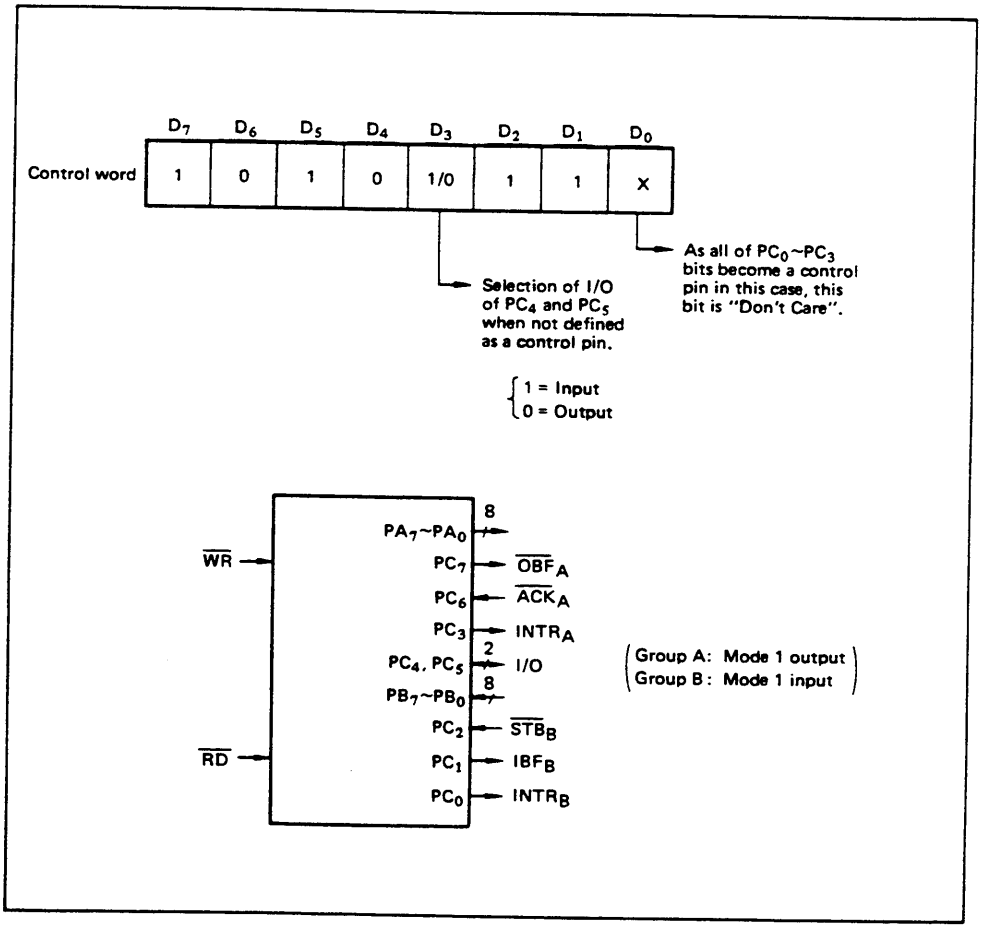
■ I/O·MSM82C55A-2RS/GS/VJS ■

Port C Function Allocation in Mode 1

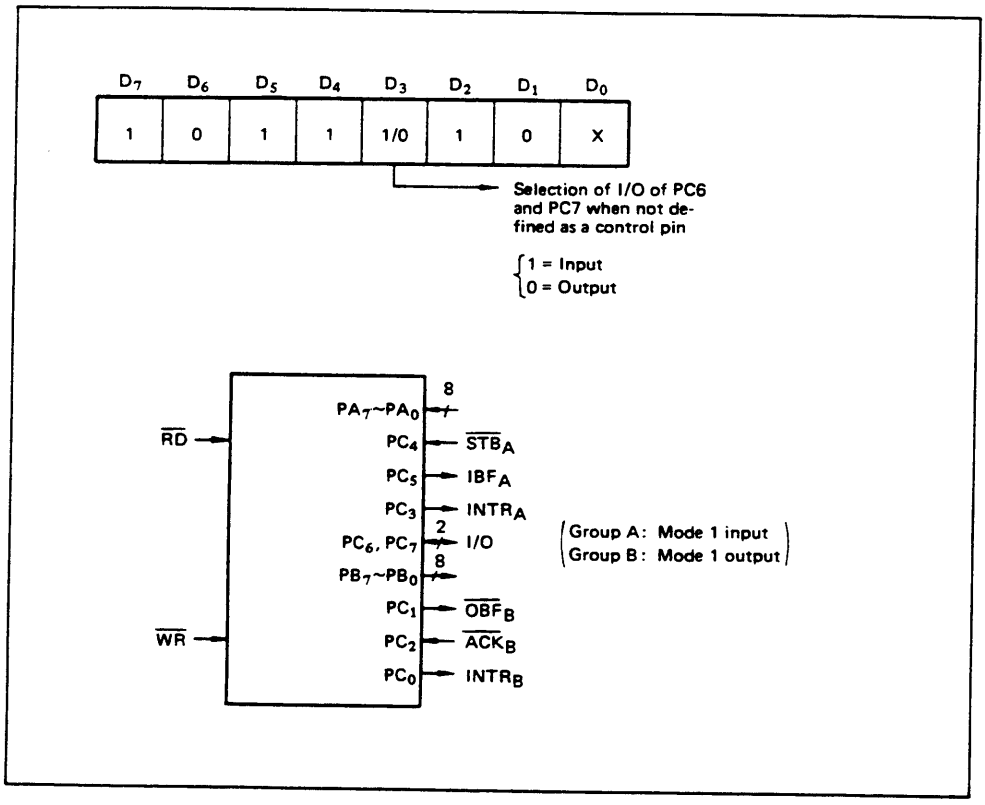
Combination of Input/Output / Port C	Group A: Input Group B: Input	Group A: Input Group B: Output	Group A: Output Group B: Input	Group A: Output Group B: Output
PC_0	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$
PC_1	IBF_B	$\overline{OBF}_B$	IBF_B	$\overline{OBF}_B$
PC_2	$\overline{STB}_B$	$\overline{ACK}_B$	$\overline{STB}_B$	$\overline{ACK}_B$
PC_3	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	$\overline{STB}_A$	$\overline{STB}_A$	I/O	I/O
PC_5	IBF_A	IBF_A	I/O	I/O
PC_6	I/O	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	I/O	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

Note: I/O is a bit not used as the control signal, but it is available as a port of mode 0.

Examples of the relation between the control words and pins when used in mode 1 is shown below:
(a) When group A is mode 1 output and group B is mode 1 input.



(b) When group A is mode 1 input and group B is mode 1 output.



3. Mode 2 (Strobe bidirectional bus I/O operation)

In mode 2, it is possible to transfer data in 2 directions through a single 8-bit port. This operation is akin to a combination between input and output operations. Port C waits for the control signal in this case, too. Mode 2 is available only for group A, however.

Next, a description is made on mode 2.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data has been written to the internal output latch upon receipt of the $\overline{WR}$ signal from the CPU. At this time, port A is still in the high impedance status and the data is not yet output to the outside. This signal turns to low level at the rising edge of the $\overline{WR}$ and high level at the falling edge of the $\overline{ACK}$.

$\overline{ACK}$ (Acknowledge input)

- When a low level signal is input to this pin, the high impedance status of port A is cleared, the buffer is enabled, and the data written to the internal output latch is output to port A. When the input returns to high level, port A is made into the high impedance status.

$\overline{STB}$ (Strobe input)

- When this signal turns to low level, the data output to the port from the pin is fetched into the internal input latch. The data is output to the data bus upon receipt of the RD signal from the CPU, but it remains in the high impedance status until then.

IBF (Input buffer full flag output)

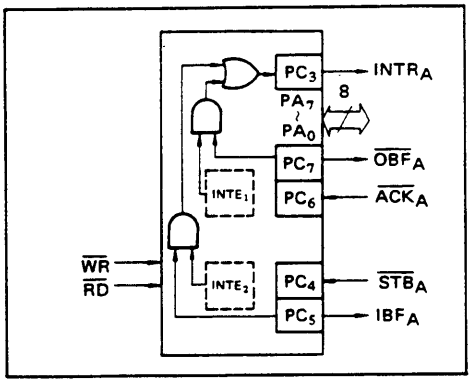
- This signal when turned to high level indicates that data from the pin has been fetched into the input latch. This signal turns to high level at the falling edge of the $\overline{STB}$ and low level at the rising edge of the $\overline{RD}$.

INTR (Interrupt request output)

- This signal is used to interrupt the CPU and its operation in the same as in mode 1. There are two INTE flip-flops internally available for input and output to select either interrupt of input or output operation. The INTE1 is used to control the interrupt request for output operation and it can be reset by the bit set for PC6. INTE2 is used to control the interrupt request for the input operation and it can be set by the bit set for PC4.

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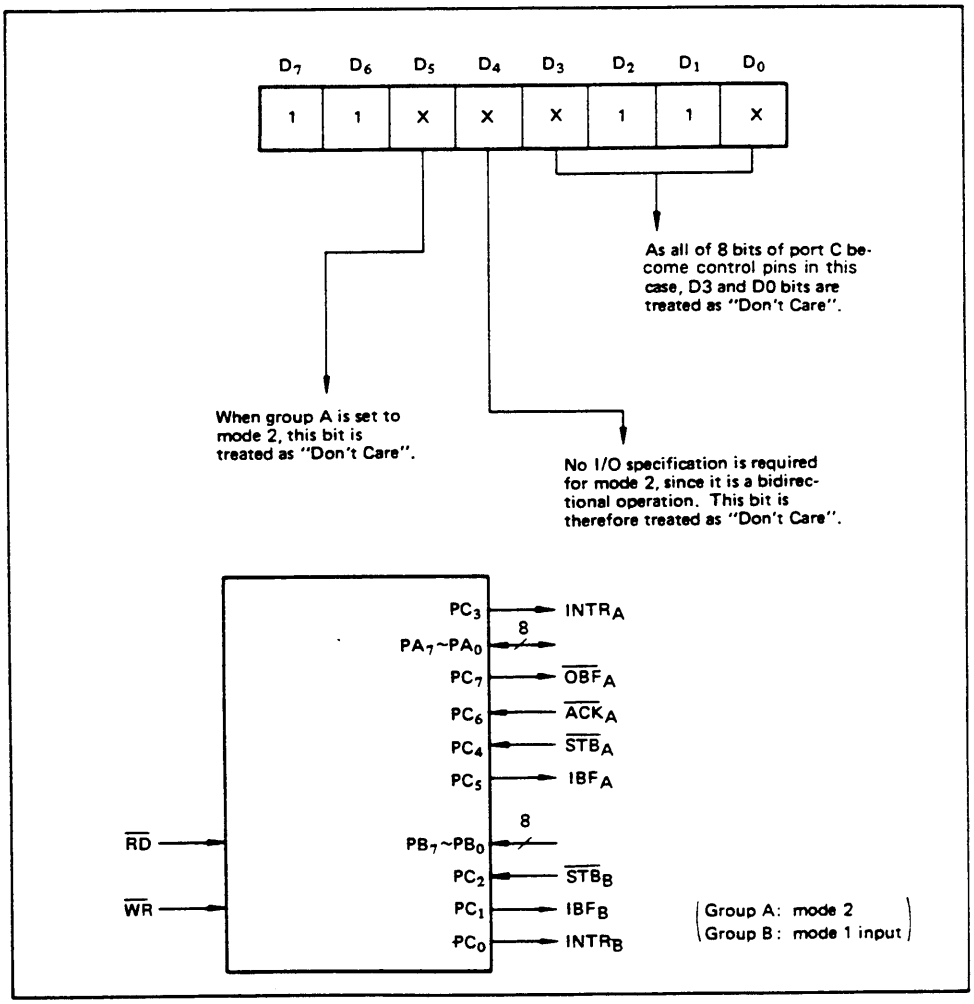
Mode 2 I/O Operation



Port C Function Allocation in Mode 2

Port C	Function
PC_0	Confirmed to the group B mode
PC_1	
PC_2	
PC_3	$INTR_A$
PC_4	$\overline{STB}_A$
PC_5	IBF_A
PC_6	$\overline{ACK}_A$
PC_7	$\overline{OBF}_A$

Following is an example of the relation between the control word and the pin when used in mode 2. When input in mode 2 for group A and in mode 1 for group B.



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4. **When Group A is Different in Mode from Group B**
Group A and group B can be used by setting them in different modes each other at the same time. When either group is set to mode1 or mode 2, it is possible to set the one not defined as a control pin in port C to both input and output as a port which operates in mode 0 at the 3rd and 0th bits of the control word.

(Mode combinations that define no control bit at port C)

	Group A	Group B	Port C							
			PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 0 output	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$\overline{STB}_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
			Controlled at the 3rd bit (D3) of the control word				Controlled at the 0th bit (D0) of the control word			

When the I/O bit is set to input in this case, it is possible to access data by the normal port C read operation.
When set to output, PC7 ~ PC4 bits can be accessed by the bit set/reset function only. Meanwhile, 3 bits from PC2 to PC0 can be accessed by normal write operation.

The bit set/reset function can be used for all of PC3 ~ PC0 bits. Note that the status of port C varies according to the combination of modes like this.

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5. Port C Status Read

When port C is used for the control signal, that is, in either mode 1 or mode 2, each control signal and bus status signal can be read out by reading the content of port C.
The status read out is as follows:

	Group A	Group B	Status read on the data bus							
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 1 output	Mode 0	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$INTE_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	I/O	I/O	I/O
10	Mode 2	Mode 1 input	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
11	Mode 2	Mode 1 output	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$

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6. Reset of MSM82C55A

Be sure to keep the RESET signal at power ON in the high level at least for 50 μs. Subsequently, it becomes the input mode at a high level pulse above 500 ns.

Note:

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After a write command is executed to the command register, the internal latch is cleared in PORTA PORTC. For instance, 00H is output at the beginning of a write command when the output port is assigned. However, if PORTB is not cleared at this time, PORTB is unstable. In other words, PORTB only outputs ineffective data (unstable value according to the device) during the period from after a write command is executed till the first data is written to PORTB.

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After a write command is executed to the command register, the internal latch is cleared in All Ports(PORTA,PORTB,PORTC) 00H is ontput at the beginning of a write command when the output port is assigned

Appendix D
Register Map and Descriptions

This appendix describes in detail the address and function of each of the Lab-PC+ registers.

Note: ***If you plan to use a programming software package such as NI-DAQ, NI-DSP, LabVIEW, or LabWindows/CVI with your Lab-PC+, you need not read this appendix. Refer to your software documentation for programming information.***

Register Map

The register map for the Lab-PC+ is given in Table D-1. This table gives the register name, the register address offset from the board's base address, the type of the register (read-only, write-only, or read-and-write), and the size of the register in bits.

Table D-1. Lab-PC+ Register Map

Register Name	Offset Address (Hex)	Type	Size
Configuration and Status Register Group			
Command Register 1	00	Write-only	8-bit
Status Register	00	Read-only	8-bit
Command Register 2	01	Write-only	8-bit
Command Register 3	02	Write-only	8-bit
Command Register 4	OF	Write-only	8-bit
Analog Input Register Group			
A/D FIFO Register	0A	Read-only	8-bit
A/D Clear Register	08	Write-only	8-bit
Start Convert Register	03	Write-only	8-bit
DMATC Interrupt Clear Register	0A	Write-only	8-bit
Analog Output Register Group			
DAC0 Low-Byte Register	04	Write-only	8-bit
DAC0 High-Byte Register	05	Write-only	8-bit
DAC1 Low-Byte Register	06	Write-only	8-bit
DAC1 High-Byte Register	07	Write-only	8-bit
8253 Counter/Timer Register Group A			
Counter A0 Data Register	14	Read-and-write	8-bit
Counter A1 Data Register	15	Read-and-write	8-bit
Counter A2 Data Register	16	Read-and-write	8-bit
Counter A Mode Register	17	Write-only	8-bit
Timer Interrupt Clear Register	0C	Write-only	8-bit
8253 Counter/Timer Register Group B			
Counter B0 Data Register	18	Read-and-write	8-bit
Counter B1 Data Register	19	Read-and-write	8-bit
Counter B2 Data Register	1A	Read-and-write	8-bit
Counter B Mode Register	1B	Write-only	8-bit
8255A Digital I/O Register Group			
Port A Register	10	Read-and-write	8-bit
Port B Register	11	Read-and-write	8-bit
Port C Register	12	Read-and-write	8-bit
Digital Control Register	13	Write-only	8-bit
Interval Counter Register Group			
Interval Counter Data Register	1E	Write-only	8-bit
Interval Counter Strobe Register	1F	Write-only	8-bit

Register Sizes

The Lab-PC+ registers are 8-bit registers. To transfer 16-bit data, two consecutive I/O readings or writings are needed. For example, to read the 16-bit A/D conversion result, two consecutive 8-bit readings of FIFO are needed. The first reading returns the low byte of the 16-bit data, and the second returns the high byte of the data.

Register Description

Table D-1 divides the Lab-PC+ registers into six different register groups. A bit description of each of the registers making up these groups is included later in this chapter.

The Configuration and Status Register Group controls the overall operation of the Lab-PC+ and the D/A circuitry. The Analog Input Register Group is used to read output from the 12-bit successive-approximation ADC. The Analog Output Register Group accesses the two 12-bit DACs. The two Counter/Timer Register Groups (A and B) access each of the two onboard 8253 Counter/Timer integrated circuits. The Digital I/O Register Group consists of the four registers of the onboard 8255A PPI integrated circuit used for digital I/O. The Interval Counter registers are used in the single-channel interval acquisition mode.

Register Description Format

The remainder of this register description chapter discusses each of the Lab-PC+ registers in the order shown in Table D-1. Each register group is introduced, followed by a detailed bit description of each register on the Lab-PC+. For a detailed bit description of each register concerning the 8253 (A or B) chip on the Lab-PC+, refer to Appendix B, *OKI 82C53 Data Sheet*, later in this manual. The individual register description gives the address, type, word size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the MSB (bit 7 for an 8-bit register) shown on the left, and the LSB (bit 0) shown on the right. A square is used to represent each bit. Each bit is labeled with a name inside its square. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic).

In many of the registers, several bits are labeled with an X, indicating *don't care bits*. When a register is read, these bits may appear set or cleared but should be ignored because they have no significance. When a register is written to, setting or clearing these bit locations has no effect on the Lab-PC+ hardware.

The bit map field for some write-only registers state *not applicable, no bits used*. Writing to these registers causes some event to occur on the Lab-PC+, such as clearing the analog input circuitry. The data is ignored when writing to these registers; therefore, any bit pattern will suffice.

Configuration and Status Register Group

The five registers making up the Configuration and Status Register Group allow general control and monitoring of the Lab-PC+ A/D and D/A circuitry. Command Register 1 and Command Register 2 contain bits that control the operation modes of the A/D and D/A circuitry. Command Register 3 enables or disables the interrupt and DMA operations. Command Register 4 is used to select the analog input mode, and also allows certain analog input conversion signals to be externally driven or received at the I/O connector. The Status Register reports the status of the A/D conversion, A/D conversion error, and the status of the interrupts. When you start up your PC, all bits of the Command Registers are cleared.

Bit descriptions for the registers in the Configuration and Status Register Group are given on the following pages.

Command Register 1

Command Register 1 indicates the input channel to be read, the gain for the analog input circuitry, and the range of the input signal (unipolar or bipolar).

Address: Base address + 00 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
SCANEN	GAIN2	GAIN1	GAIN0	TWOSCMP	MA2	MA1	MA0

Bit	Name	Description
7	SCANEN	This bit enables or disables multiple-channel scanning during data acquisition. If this bit is set, analog channels MA<2..0> through 0 are sampled alternately. If this bit is cleared, a single analog channel specified by MA<2..0> is sampled during the entire data acquisition operation. See *Programming Multiple A/D Conversions with Channel Scanning* in Appendix E, *Register-Level Programming,* for the correct sequence involved in setting this bit. For example, in the RSE or NRSE mode of operation, if MA<2..0> is 011 and SCANEN is set, analog input Channels 3 through 0 are sampled alternately during subsequent data conversions. If SCANEN is then cleared (with MA<2..0> still set to 011), only analog input Channel 3 is sampled during the subsequent data conversions.
6-4	GAIN<2..0>	These three bits select the gain setting as follows:

GAIN<2..0>	Selected Gain
000	1
001	1.25
010	2
011	5
100	10
101	20
110	50
111	100

Bit	Name	Description (continued)
3	TWOSCMP	This bit selects the format of the coding of the output of the ADC. If this bit is set, the 12-bit data from the ADC is sign-extended to 16 bits. If this bit is cleared, bits 12 through 15 return 0.
2-0	MA<2..0>	These three bits select which of the eight input channels are read. The analog input multiplexers depend on these bits and also on SCANEN and $\overline{SE}$/D (bit 3 of Command Register 4). Input channels are selected as follows:

MA<2..0>	Selected Analog Input Channels				
	Single-Ended	DIFF			
		Scan Disabled		Scan Enabled	
		(+)	(-)	(+)	(-)
000	0	0	1	0	1
001	1	0	1	2	3
010	2	2	3	4	5
011	3	2	3	6	7
100	4	4	5	0	1
101	5	4	5	2	3
110	6	6	7	4	5
111	7	6	7	6	7

In single-ended mode (RSE or NRSE), if SCANEN is set, analog channels MA<2..0> through 0 are sampled alternatively. If SCANEN is cleared, a single analog channel specified by MA<2..0> is sampled during the entire data acquisition operation.

In DIFF mode, if SCANEN is set, the analog channel pair corresponding to MA<2..0>, specified in the table, through (0,1) are sampled alternately.

In DIFF mode, if SCANEN is cleared, then a single analog channel pair specified by MA<2..0> is sampled during the entire data acquisition operation. Note that in this mode, MA<2..0> can hold the channel number of either of the channels that make the differential pair.

See *Programming Multiple A/D Conversions with Channel Scanning* in Appendix E, *Register-Level Programming*, for the correct sequence involved in setting the SCANEN bit.

Status Register

The Status Register indicates the status of the current A/D conversion. The bits in this register determine if a conversion is being performed or if data is available, whether any errors have been found, and the interrupt status.

Address: Base address + 00 (hex)

Type: Read-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Lab-PC/PC+	EXTGATA0	GATA0	DMATC	CNTINT	OVERFLOW	OVERRUN	DAVAIL

Bit	Name	Description
7	Lab-PC/PC+	This bit indicates whether the board is a Lab-PC or a Lab-PC+. If this bit is 0, a Lab-PC+ is present. If this bit is 1, a Lab-PC is present.
6	EXTGATA0	This bit indicates the status of the external trigger. If this bit is set, the external trigger signal has been received to trigger a data acquisition operation. This bit is cleared by writing to ADCLR Register.
5	GATA0	This bit indicates the status of the GATE 0 input on the counter/timer chip (Counter Group A). This bit can be used as a busy indicator for data acquisition operations because conversions are enabled as long as GATE 0 is high and Counter A0 is programmed appropriately.
4	DMATC	This bit reflects the status of the DMA terminal count. If this bit is set, and if the TCINTEN bit is set in Command Register 3, then the current interrupt is due to the detection of a DMA terminal counter pulse. This bit is cleared by writing to the DMATC Interrupt Clear Register.
3	CNTINT	This bit reflects the status of the interrupt caused by Counter A2 output or the EXTUPDATE signal. If the CNTINTEN bit in Command Register 3 is set, a low-to-high transition on Counter A2 output or on EXTUPDATE sets this bit and generates an interrupt request. This bit is cleared by writing to the CNTINTCLR Register.
2	OVERFLOW	This bit indicates if an overflow error has occurred. If this bit is cleared, no error was encountered. If this bit is set, the A/D FIFO has overflowed because the data acquisition servicing operation could not keep up with the sampling rate.

Bit	Name	Description (continued)
1	OVERRUN	This bit indicates if an overrun error has occurred. If this bit is cleared, no error occurred. This bit is set if a convert command is issued to the ADC while the last conversion is still in progress.
0	DAVAIL	This bit indicates whether conversion output is available. If this bit is set, the ADC is finished with the last conversion and the result can be read from the FIFO. This bit is cleared if the FIFO is empty. After writing to the ADCLR Register this bit is set. Two 8-bit readings of FIFO are needed to clear this bit.

Command Register 2

Command Register 2 contains eight bits that control Lab-PC+ analog input trigger modes and analog output modes.

Address: Base address + 01 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
LDAC1	LDAC0	2SDAC1	2SDAC0	TBSEL	SWTRIG	HWTRIG	PRETRIG

Bit	Name	Description
7	LDAC1	This bit is used to enable timer waveform generation from DAC1. If this bit is set, DAC1 updates its output at regular intervals as determined by Counter A2 or the EXTUPDATE* signal at the I/O connector. If this bit is cleared, then the voltage output of DAC1 is updated as soon as the data is loaded into its data register.
6	LDAC0	This bit is used to enable timer waveform generation from DAC0. If this bit is set, DAC0 updates its output at regular intervals as determined by Counter A2 or the EXTUPDATE* signal at the I/O connector. If this bit is cleared, then the voltage output of DAC0 is updated as soon as the data is loaded into its data register.
5	2SDAC1	This bit selects the binary coding scheme used for the DAC1 data. If this bit is set, a two's complement binary coding scheme is used for interpreting the 12-bit data. Two's complement is useful if a bipolar output range is selected. If this bit is cleared, a straight binary coding scheme is used. Straight binary is useful if a unipolar output range is selected.
4	2SDAC0	This bit selects the binary coding scheme used for the DAC0 data. If this bit is set, a two's complement binary coding scheme is used for interpreting the 12-bit data. Two's complement is useful if a bipolar output range is selected. If this bit is cleared, a straight binary coding scheme is used. Straight binary is useful if a unipolar output range is selected.
3	TBSEL	This bit is used to select the clock source for A/D conversions. If this bit is cleared, an internal 1 MHz clock drives the counter (Counter A0), and the interval between samples is the value loaded into Counter A0 multiplied by 1 µs. If this bit is set, then the output of user-programmable Counter B0 is used as a clock source. The timebase for Counter B0 is fixed at 2 MHz and cannot be changed. The interval between acquired samples is the value loaded into Counter A0 multiplied by the period of the output signal from Counter B0.

Bit	Name	Description (continued)
2	SWTRIG	This bit enables and disables a data acquisition operation that is controlled by Counter A0 and Counter A1. If Counter A0 is programmed for data acquisition, writing 1 to this bit enables Counter A0, and thus starts a data acquisition operation. A data acquisition process is terminated either by the terminal count signal of Counter A1 or by clearing SWTRIG. If SWTRIG is cleared, the Counter A0 is disabled, except when the HWTRIG mode is used.
1	HWTRIG	Setting this bit allows the external EXTTRIG signal to start a data acquisition operation that is controlled by Counter A0 and Counter A1. If this bit is set, a low-to-high transition on EXTTRIG enables Counter A0, and thus starts a data acquisition operation. To use this mode, the SWTRIG and PRETRIG bits should be cleared.
0	PRETRIG	This bit is used to set the pretriggering feature on the Lab-PC+. If this bit is set, a data acquisition operation is initialized by setting SWTRIG, but the Counter A1 (the sample counter) does not begin decrementing until a rising edge is detected on EXTTRIG. To use this mode, the HWTRIG bit should be cleared.

Command Register 3

The Command Register 3 contains six bits that enable and disable the interrupts and DMA operation.

Address: Base address + 02 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	FIFOINTEN	ERRINTEN	CNTINTEN	TCINTEN	DIOINTEN	DMAEN

Bit	Name	Description
7-6	X	Don't care bits.
5	FIFOINTEN	This bit enables and disables the generation of an interrupt when A/D conversion results are available. If FIFOINTEN is set, an interrupt is generated whenever an A/D conversion is available to be read from the FIFO.
4	ERRINTEN	This bit enables and disables the generation of an interrupt when an A/D error condition is detected. If an A/D error condition occurs, either OVERFLOW or OVERRUN is set in the Status Register. The interrupt is serviced by writing to the A/D Clear Register. If ERRINTEN is cleared, no error interrupts are generated.
3	CNTINTEN	This bit enables the Counter A2 output or the EXTUPDATE* signal to cause interrupts. If this bit is set, an interrupt occurs when either EXTUPDATE* or Counter A2 output makes a low-to-high transition. This interrupt is cleared by writing to the Timer Interrupt Clear Register. This interrupt allows waveform generation on the analog output because the same signal that sets the interrupt also updates the DAC output if the corresponding LDAC bit in Command Register 2 is set. If this bit is cleared, interrupts from EXTUPDATE* and Counter A2 output are ignored.
2	TCINTEN	This bit enables and disables the generation of an interrupt when a DMA terminal count pulse is received. If TCINTEN is set, an interrupt request is generated when the DMA Controller Transfer Count Register decrements from 0 to FFFF (hex). The interrupt is serviced by writing to the DMATCINT Clear Register.

Bit	Name	Description (continued)
1	DIOINTEN	This bit enables or disables generation of an interrupt when either Port A or Port B is ready to transfer data, and an interrupt request is set via PC3 or PC0 of 8255A. (See Appendix C, *OKI 82C55A Data Sheet*, for details.) If DIOINTEN is cleared, the interrupts from PC3 or PC0 are disabled.
0	DMAEN	This bit enables and disables the generation of DMA requests. If DMAEN is set, a DMA request is generated whenever an A/D conversion result is available to be read from the FIFO. If DMAEN is cleared, no DMA request is generated.

Command Register 4

This register allows multiplexing of certain A/D conversion logic signals. This enables the interval scanning and A/D conversion signals to be available at the I/O connector and allows the I/O connector pins to externally drive these signals.

Address: Base address + 0F (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	ECLKRCV	$\overline{SE}$/D	ECLKDRV	EOIRCV	INTSCAN

Bit	Name	Description
7-5	X	Don't care bits.
4	ECLKRCV	When cleared, this bit enables EXTCONV* pulses applied at the EXTCONV* pin on the connector to cause conversions when ECLKDRV is cleared. When set, ECLKRCV inhibits EXTCONV* pulses from causing conversions. This bit is cleared on board reset.
3	$\overline{SE}$/D	This bit along with jumper W4 selects the analog input mode of the Lab-PC+. When clear, it selects the single-ended mode. In this case, multiplexer 1 selects Channels 0-7 specified by the channel select bits, and multiplexer 2 selects AISENSE/AIGND. If W4 is configured in SE mode, AISENSE/AIGND gets tied to analog ground. This is the RSE mode. If W4 is configured as DIFF, AISENSE/AIGND does not get tied to analog ground. This is the NRSE mode. When this bit is set, the differential mode of input is selected. Now W4 must be in the DIFF setting. This is the DIFF mode. In this mode, Mux 1 and Mux 2 select channel pairs (0,1), (2,3), (4,5) or (6,7) depending on the channel selection bits. This bit defaults to zero on reset, thus choosing the single-ended mode. Refer to the following table for choosing the appropriate mode.

W4 Configuration	$\overline{SE}$/D (Bit 3)	Input Mode
RSE (A-B)	0	RSE (factory setting)
NRSE/DIFF (B-C)	0	NRSE
NRSE/DIFF (B-C)	1	DIFF

Bit	Name	Description (continued)
2	ECKDRV	This bit controls the direction of the EXTCONV* line on the I/O Connector. If this bit is clear, EXTCONV* is driven from the I/O Connector into the conversion circuitry. If this bit is set, a conditioned version of the output of counter A0 is driven onto the I/O Connector. Under most circumstances, this bit should be clear. This bit is cleared on reset.
1	EOIRCV	This bit is used to select the clock source for interval scanning. If this bit is clear, Counter B1 drives the interval scanning circuitry. If this bit is set, the signal present on the OUTB1 line on the I/O Connector drives the interval scanning circuitry. If INTSCAN is clear, EOIRCV does nothing more than disconnect the output of Counter B1 from the I/O Connector–if INTSCAN is clear, always clear EOIRCV. This bit is cleared on reset.
0	INTSCAN	This bit selects the DAQ mode. When you set this bit, the Lab-PC+ performs interval data acquisition. If you clear this bit, continuous channel scanning is selected. If interval channel scanning is selected, scan sequences occur during a programmed time interval, called a scan interval. The duration of the scan interval is determined by the output of Counter B1 or by the signal present on the OUTB1 line on the I/O Counter, as determined by EOIRCV. This bit also selects the clock source for Counter B1. If interval scanning is disabled (INTSCAN = 0), then Counter B1 is available for user applications. You can then drive CLKB1 externally at the I/O Connector. If interval scanning is enabled (INTSCAN = 1), the clock source for Counter A0 also drives CLKB1. The source can be further selected by using the TBSEL bit in command register 2. This bit is cleared on reset.

Analog Input Register Group

The four registers making up the Analog Input Register Group control the analog input circuitry and can be used to read the FIFO. Reading the FIFO Register returns stored A/D conversion results. Writing to the Start Convert Register initiates an A/D conversion. Writing to the A/D Clear Register clears the data acquisition circuitry. Writing to the DMATC Clear Register clears the interrupt request generated by a DMA terminal count pulse.

Bit descriptions for the registers making up the Analog Input Register Group are given on the following pages.

A/D FIFO Register

The 12-bit A/D conversion results are sign-extended to 16-bit data in either two's complement or straight binary format and are stored into a 512-word deep A/D FIFO buffer. Two consecutive 8-bit readings of the A/D FIFO Register return an A/D conversion value stored in the A/D FIFO. The first reading returns the low byte of the 16-bit value, and the second reading returns the high byte. The value read is removed from the A/D FIFO, thereby freeing space for another A/D conversion value to be stored.

The A/D FIFO is emptied when all values it contains are read. The Status Register should be read before the A/D FIFO Register is read. If the A/D FIFO contains one or more A/D conversion values, the DAVAIL bit is set in the Status Register, and the A/D FIFO Register can be read to retrieve a value. If the DAVAIL bit is cleared, the A/D FIFO is empty, in which case reading the A/D FIFO Register returns meaningless information.

The values returned by reading the A/D FIFO Register are available in two different binary formats: straight binary or two's complement binary. The binary format used is selected by the TWOSCMP bit in the Command Register 1. The bit pattern returned for either format is given below.

Address: Base address + 0A (hex)

Type: Read-only

Word Size: 8-bit

Bit Map: Straight binary mode

High Byte

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8
(0)	(0)	(0)	(0)				

Low Byte

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
High Byte		
7-0	D<15..8>	These bits contain the high byte of the straight binary result of a 12-bit A/D conversion. Bits D<15..12> are always 0 in straight binary mode. Values made up of D<11..0>, therefore, range from 0 to +4,095 decimal (0000 to 0FFF hex). Straight binary mode is useful for unipolar analog input readings because all values read reflect a positive polarity input signal.

Bit	Name	Description (continued)
Low Byte		
7-0	D<7..0>	These bits contain the low byte of the straight binary result of a 12-bit A/D conversion. The first of two consecutive readings of the A/D FIFO Register always return this byte.

Bit Map: Two's complement binary mode

High Byte

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8
{	Sign Extension Bits		}				

Low Byte

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
High Byte		
7-0	D<15..8>	These bits contain the high byte of the 16-bit, sign-extended two's complement result of a 12-bit A/D conversion. Values made up of D<15..0>, therefore, range from -2,048 to +2,047 decimal (F800 to 07FF hex). Two's complement mode is useful for bipolar analog input readings because the values read reflect the polarity of the input signal.
Low Byte		
7-0	D<7..0>	These bits contain the low byte of the 16-bit, sign-extended two's complement result of a 12-bit A/D conversion. The first of two consecutive readings of A/D FIFO Register always returns this byte.

A/D Clear Register

The ADC can be reset by writing to this register. This operation clears the FIFO and loads the last conversion value into the FIFO. All error bits in the Status Register are cleared as well. Notice that the FIFO contains one data word after reset, so two consecutive FIFO readings are necessary after reset to empty the FIFO. The data that is read should be ignored.

Address: Base address + 08 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map: Not applicable, no bits used

Start Convert Register

Writing to the Start Convert Register location initiates an A/D conversion.

Address: Base address + 03 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map: Not applicable, no bits used

Note: ***A/D conversions can be initiated in one of two ways: by writing to the Start Convert Register or by detecting an active low signal on either the Counter A0 output or the EXTCONV* signal. If the Start Convert Register is to initiate an A/D conversion, the Counter A0 output should be initialized to high state, which must be followed by an ADCLEAR operation, by writing to the ADCLEAR Register.***

DMATC Interrupt Clear Register

Writing to the DMA Terminal Count (DMATC) Clear Register clears the interrupt request asserted when a DMA terminal count pulse is detected.

Address: Base address + 0A (hex)

Type: Write-only

Word Size: 8-bit

Bit Map: Not applicable, no bits used

Analog Output Register Group

The four registers making up the Analog Output Register Group are used for loading the two 12-bit DACs in the two analog output channels. DAC0 controls analog output Channel 0. DAC1 controls analog output Channel 1. These DACs should be written to individually.

Bit descriptions of the registers making up the Analog Output Register Group are given on the following pages.

DAC0 Low-Byte (DAC0L), DAC0 High-Byte (DAC0H), DAC1 Low-Byte (DAC1L), and DAC1 High-Byte (DAC1H) Registers

Writing to DAC0L and then to DAC0H loads the analog output Channel 0. Writing to DAC1L and then to DAC1H loads the analog output Channel 1. The voltage generated by the analog output channels is updated immediately after the corresponding DAC*x*H register is written to, if the corresponding LDAC*x* bit is cleared in Command Register 2. If the LDAC*x* bit is set, the analog output is updated when an active low pulse occurs on the output of Counter A2 or on the EXTUPDATE* line on the I/O connector.

Address:	Base address + 04 (hex)	Load DAC0 low byte.
	Base address + 05 (hex)	Load DAC0 high byte.
	Base address + 06 (hex)	Load DAC1 low byte.
	Base address + 07 (hex)	Load DAC1 high byte.

Type: Write-only (all)

Word Size: 8-bit (all)

Bit Map:

DAC*x*H

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8
{	Sign Extension Bits		}				

DAC*x*L

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
DAC*x*H		
7-4	D<15..12>	Zero in straight binary mode, sign extension in two's complement mode.
3-0	D<11..8>	These four bits are loaded into the specified DAC high byte.
DAC*x*L		
7-0	D<7..0>	These eight bits are loaded into the specified DAC low byte. The low byte should be loaded first, followed by corresponding high byte loading.

8253 Counter/Timer Register Groups A and B

The nine registers making up the two Counter/Timer Register Groups access the two onboard 8253 Counter/Timers. Each 8253 has three counters. For convenience, the two Counter/Timer Groups and their respective 8253 integrated circuits have been designated A and B. The three counters of Group A control onboard data acquisition timing and waveform generation. The three counters of Group B are available for general-purpose timing functions.

Each 8253 has three independent 16-bit counters and one 8-bit Mode Register. The Mode Register is used to set the mode of operation for each of the three counters. Writing to the Timer Interrupt Clear Register clears the interrupt request asserted when a low pulse is detected on the output of Counter A2 or on the EXTUPDATE* line.

Bit descriptions for the registers in the Counter/Timer Register Groups are given in the following pages.

Counter A0 Data Register

The Counter A0 Data Register is used for loading and reading back contents of 8253(A) Counter 0.

Address: Base address + 14 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Counter A0 contents.

Counter A1 Data Register

The Counter A1 Data Register is used for loading and reading back contents of 8253(A) Counter 1.

Address: Base address + 15 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Counter A1 contents.

Counter A2 Data Register

The Counter A2 Data Register is used for loading and reading back contents of 8253(A)Counter A2.

Address: Base address + 16 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Counter A2 contents.

Counter A Mode Register

The Counter A Mode Register determines the operation mode for each of the three counters on the 8253(A) chip. The Counter A Mode Register selects the counter involved, its read/load mode, its operation mode (that is, any of the 8253's six operation modes), and the counting mode (binary or BCD counting).

The Counter A Mode Register is an 8-bit register. Bit descriptions for each of these bits are given in Appendix B, *OKI 82C53 Data Sheet*.

Address: Base address + 17 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Timer Interrupt Clear Register

Writing to the Timer Interrupt Clear Register clears the interrupt request asserted when a low pulse is detected on the Counter A2 output or on EXTUPDATE* line.

Address: Base address + 0C (hex)

Type: Write-only

Word Size: 8-bit

Bit Map: Not applicable, no bits used.

Counter B0 Data Register

The Counter B0 Data Register is used for loading and reading back the contents of 8253(B) Counter 0.

Address: Base address + 18 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Counter B0 contents.

Counter B1 Data Register

The Counter B1 Data Register is used for loading and reading back the contents of 8253(B) Counter 1.

Address: Base address + 19 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Counter B1 contents.

Counter B2 Data Register

The Counter B2 Data Register is used for loading and reading back the contents of 8253(B) Counter 2.

Address: Base address + 1A (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Counter B2 contents.

Counter B Mode Register

The Counter B Mode Register determines the operation mode for each of the three counters on the 8253(B) chip. The Counter B Mode Register selects the counter involved, its read/load mode, its operation mode (that is, any of the 8253's six operation modes), and the counting mode (binary or BCD counting).

The Counter Mode Register is an 8-bit register. Bit descriptions for each of these bits are given in Appendix B, *OKI 82C53 Data Sheet*, of this manual.

Address: Base address + 1B (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

8255A Digital I/O Register Group

Digital I/O on the Lab-PC+ uses an 8255A integrated circuit. The 8255A is a general-purpose peripheral interface containing 24 programmable I/O pins. These pins represent the three 8-bit I/O ports (A, B, and C) of the 8255A. These ports can be programmed as two groups of 12 signals or as three individual 8-bit ports.

Bit descriptions for the registers in the Digital I/O Register Group are given on the following pages.

Port A Register

Reading the Port A Register returns the logic state of the eight digital I/O lines constituting Port A, that is, PA<0..7>. If Port A is configured for output, the Port A Register can be written to in order to control the eight digital I/O lines constituting Port A. See *Programming the Digital I/O Circuitry* in Appendix E, *Register-Level Programming*, for information on how to configure Port A for input or output.

Address: Base address + 10 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Port A data.

Port B Register

Reading the Port B Register returns the logic state of the eight digital I/O lines constituting Port B, that is, PB<0..7>. If Port B is configured for output, the Port B Register can be written to in order to control the eight digital I/O lines constituting Port B. See *Programming the Digital I/O Circuitry* in Appendix E, *Register-Level Programming*, for information on how to configure Port B for input or output.

Address: Base address + 11 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Port B data.

Port C Register

Port C is special in the sense that it can be used as an 8-bit I/O port like Port A and Port B if neither Port A nor Port B is used in handshaking (latched) mode. If either Port A or Port B is configured for latched I/O, some of the bits in Port C are used for handshaking signals. See *Programming the Digital I/O Circuitry* in Appendix E, *Register-Level Programming,* for a description of the individual bits in the Port C Register.

Address: Base address + 12 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Port C data.

Digital Control Register

The Digital Control Register can be used to configure Port A, Port B, and Port C as inputs or outputs as well as selecting simple mode (basic I/O) or handshaking mode (strobed I/O) for transfers. See *Programming the Digital I/O Circuitry* in Appendix E, *Register-Level Programming*, for a description of the individual bits in the Digital Control Register.

Address: Base address + 13 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
CW7	CW6	CW5	CW4	CW3	CW2	CW1	CW0

Bit	Name	Description
7-0	CW<7..0>	8-bit control word.

Interval Counter Register Group

The 8-bit Interval Counter is used only in the single-channel interval mode (SCANEN = 0 and INTSCAN = 1) and consists of two 8-bit registers–the Interval Counter Data Register and the Interval Counter Strobe Register. The Interval Counter Data Register is loaded with the count. Writing to the Interval Counter Strobe Register loads this count into the Interval Counter. The Interval Counter decrements with each conversion. When the count reaches 0, the Interval Counter autoinitializes, restoring the original count value.

Bit descriptions for the registers in the Interval Counter Register Group are given on the following pages.

Interval Counter Data Register

The Interval Counter Data Register is loaded with the desired number of samples of a single channel that will be acquired between intervals. See *Programming Multiple A/D Conversions in Single-Channel Interval Acquisition Mode* in Appendix E, *Register-Level Programming*, for a description of the programming sequence.

Address: Base address + 1E (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	Interval Counter count.

Interval Counter Strobe Register

Writing to Interval Counter Strobe Register strobes the contents of the Interval Counter Data Register into the Interval Counter. This action arms the Interval Counter, which then decrements with each conversion pulse.

Address: Base address + 1F (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Bit	Name	Description
7-1	0	Each of these bits must be 0 for proper operation of the Lab-PC+.
0	1	This bit must be 1 for proper operation of the Lab-PC+.

Appendix E
Register-Level Programming

This appendix contains important information about programming the Lab-PC+.

Programming the Lab-PC+ involves writing to and reading from the various registers on the board. The programming instructions included here list the sequence of steps to take. The instructions are language independent; that is, they tell you to write a value to a given register, to set or clear a bit in a given register, or to detect whether a given bit is set or cleared, without presenting the actual code.

Register Programming Considerations

The Lab-PC+ can only be used for 8-bit I/O transfers, thus all the I/O read-and-write operations are 8-bit operations.

Several write-only registers on the Lab-PC+ contain bits that control several independent pieces of the onboard circuitry. In the set or clear instructions provided, specific register bits should be set or cleared without changing the current state of the remaining bits in the register. However, writing to these registers affects all register bits simultaneously. You cannot read these registers to determine which bits have been set or cleared in the past; therefore, you should maintain a software copy of the write-only registers. This software copy can then be read to determine the status of the write-only registers. To change the state of a single bit without disturbing the remaining bits, set or clear the bit in the software copy and then write the software copy to the register.

Initializing the Lab-PC+ Board

The Lab-PC+ hardware must be initialized in order for the Lab-PC+ circuitry to operate properly. To initialize the Lab-PC+ hardware, complete these steps:

1. Write 00 (hex) to the Command Register 1.
2. Write 00 (hex) to the Command Register 2.
3. Write 00 (hex) to the Command Register 3.
4. Write 00 (hex) to the Command Register 4.
5. Write 34 (hex) to Counter A Mode Register.
6. Write 0A (hex) to Counter A0 Data Register.
7. Write 00 (hex) to Counter A0 Data Register.

8. Write 00 (hex) to the DMATC Interrupt Clear Register.
9. Write 00 (hex) to the Timer Interrupt Clear Register.
10. Write 00 (hex) to the A/D Clear Register.
11. Read the data from the A/D FIFO Register (twice). Ignore the data.
12. Write 00 (hex) to the DAC0L, and then write 00 (hex) to the DAC0H if DAC0 is configured for unipolar output. Write 00 (hex) to the DAC0L, and then write 08 (hex) to the DAC0H if DAC0 is configured for bipolar output.
13. Write 00 (hex) to the DAC1L, and then write 00 (hex) to the DAC1H if DAC 1 is configured for unipolar output. Write 00 (hex) to the DAC1L, and then write 08 (hex) to the DAC1H if DAC1 is configured for bipolar output.

This sequence leaves the Lab-PC+ circuitry in the following state:

- Counter A0 output is high.
- Counter A1 output is high. This disables EXTCONV*.
- All interrupts are disabled.
- EXTTRIG is disabled.
- The timebase for Counter A0 is the onboard 1 MHz source.
- Analog input circuitry is initialized to RSE mode with a gain of 1 and Channel 0 selected.
- The A/D FIFO is cleared.
- The Command Registers are initialized to 00 (hex) on power up. Thus, straight binary coding is selected for both DACs.
- The analog output circuitry is initialized to 0.0 V on both channels.

For additional details concerning the 8253 Counter/Timer, see Appendix B, *OKI 82C53 Data Sheet*. For information about the 8255A PPI, see Appendix C, *OKI 82C55A Data Sheet.*

Programming the Analog Input Circuitry

This section describes the analog input circuitry programming sequence, how to program the binary mode of the A/D conversion result, and how to clear the analog input circuitry. Ensure that you have selected the appropriate analog input mode through jumper W4 and bit 3 of Command Register 4.

Analog Input Circuitry Programming Sequence

Programming the analog input circuitry for a single A/D conversion involves selecting the analog input channel and gain, initiating an A/D conversion, and reading the A/D conversion result.

1. Select analog input channel and gain.

   The analog input channel and gain are selected by writing to Command Register 1. See the Command Register 1 bit description earlier in this chapter for gain and analog input channel bit patterns. Set up the bits as given in the Command Register 1 bit description, and write to the Command Register 1.

   Command Register 1 needs to be written to only when the analog input channel, gain setting, input mode (unipolar/bipolar), or scanning mode need to be changed.

2. Initiate an A/D conversion.

   An A/D conversion can be initiated by an active low pulse on the Counter A0 output (OUTA0) or on the EXTCONV* line. To enable Counter A0 and the EXTCONV*, the SWTRIG bit in Command Register 2 must be set and OUTA1 must be low. Alternatively, a conversion can be performed by writing to the Start Convert Register.

   Once an A/D conversion is initiated, the ADC stores the result in the A/D FIFO at the end of its conversion cycle or after a rising edge on OUTA0, whichever occurs later. In case of EXTCONV* initiating the conversion, OUTA0 must be set high.

3. Read the A/D conversion result.

   A/D conversion results are obtained by reading the A/D FIFO Register. Before you read the A/D FIFO, however, you must read the Status Register to determine whether the A/D FIFO contains any results.

   To read the A/D conversion results, complete these steps:

   a. Read the Status Register (8-bit read).

   b. If the DAVAIL bit is set (bit 0), then read the A/D FIFO Register twice to obtain the result. The first reading returns the low byte of 16-bit data, and the second reading returns the high byte.

Reading the A/D FIFO Register removes the A/D conversion result from the A/D FIFO. The binary modes of the A/D FIFO output are explained in the next section, *A/D FIFO Output Binary Modes*.

The DAVAIL bit indicates whether one or more A/D conversion results are stored in the A/D FIFO. If the DAVAIL bit is cleared, the A/D FIFO is empty and reading the A/D FIFO Register returns meaningless data. Once an A/D conversion is initiated, the DAVAIL bit should be set after 12 µs or after a rising edge on OUTA0, whichever occurs later. If EXTCONV* is being used for A/D timing, the DAVAIL bit should be set after 12 µs or after a rising edge in EXTCONV*, whichever occurs later.

An A/D FIFO overflow condition occurs if more than 16 conversions are initiated and stored in the A/D FIFO before the A/D FIFO Register is read. If this condition occurs, the OVERFLOW bit is set in the Status Register to indicate that one or more A/D conversion results have been lost because of FIFO overflow. Writing to the A/D Clear Register resets this error flag. Two 8-bit dummy reads must be performed on the FIFO after an A/D Clear to reset the FIFO.

A/D FIFO Output Binary Modes

The A/D conversion result can be returned from the A/D FIFO as a 16-bit two's complement or straight binary value by setting or clearing the TWOSCMP bit in Command Register 1. If the analog input circuitry is configured for the input range 0 to +10 V, straight binary mode should be used (clear the TWOSCMP bit). Straight binary mode returns numbers between 0 and +4,095 (decimal) when the A/D FIFO Register is read. If the analog input circuitry is configured for the input range -5 to +5 V, two's complement mode is more appropriate (set the TWOSCMP bit). Two's complement mode returns numbers between -2,048 and +2,047 (decimal) when the A/D FIFO Register is read.

Table E-1 shows input voltage versus A/D conversion values for the 0 to +10 V input range. Table E-2 shows input voltage versus A/D conversion values for two's complement mode and -5 to +5-V input range.

Table E-1. Unipolar Input Mode A/D Conversion Values (Straight Binary Coding)

Input Voltage (Gain = 1)	**A/D Conversion Result Range: 0 to +10 V**	
	(Decimal)	**(Hex)**
0	0	0000
2.5	1,024	0400
5.0	2,048	0800
7.5	3,072	0C00
9.9976	4,095	0FFF

Table E-2. Bipolar Input Mode A/D Conversion Values (Two's Complement Coding)

Input Voltage (Gain = 1)	**A/D Conversion Result Range: -5 to +5 V**	
	Decimal	**Hex**
-5.0	-2,048	F800
2.5	-1,024	FC00
0	0	0000
2.5	1,024	0400
4.9976	2,047	07FF

Clearing the Analog Input Circuitry

The analog input circuitry can be cleared by writing to the A/D Clear Register, which leaves the analog input circuitry in the following state:

- Analog input error flags OVERFLOW and OVERRUN are cleared.
- Pending interrupt requests are cleared.
- A/D FIFO has one garbage word of data.

Empty the A/D FIFO before starting any A/D conversions by performing two 8-bit reads on the A/D FIFO Register and ignoring the data read. This operation guarantees that the A/D conversion results read from the A/D FIFO are the results from the initiated conversions rather than leftover results from previous conversions.

To clear the analog input circuitry and the A/D FIFO, complete these steps:

- Write 0 to the A/D Clear Register (8-bit write).
- Read the A/D FIFO Register twice and ignore the data (8-bit read).

Programming Multiple A/D Conversions on a Single Input Channel

A sequence of timed A/D conversions is referred to in this manual as a *data acquisition operation*. Two types of data acquisition operations are available on the Lab-PC+:

- Controlled acquisition mode
- Freerun acquisition mode

In controlled acquisition mode, two counters (Counters A0 and A1) are required for a data acquisition operation. Counter A0 is used as a sample interval counter, while Counter A1 is used as a sample counter. In this mode, a specified number of conversions are performed, after which the hardware shuts off the conversions. Counter A0 generates the conversion pulses, and Counter A1 gates off Counter A0 after the programmed count has expired. The number of conversions in a single data acquisition operation in this case is limited to a 16-bit count (on 65,535).

In freerun acquisition mode, only one counter is required for a data acquisition operation. Counter A0 continuously generates the conversion pulses as long as GATEA0 is held at a high logic level. The software keeps track of the number of conversions that have occurred and turns off Counter A0 after the required number of conversions have been obtained. The number of conversions in a single data acquisition operation in this case is unlimited. Counter A0 is clocked by a 1 MHz clock on start up.

Alternatively, a programmable timebase for Counter A0 is available through the use of Counter B0. If the TBSEL bit in Command Register 1 is set, then the timebase for Counter A0 is Counter B0. Counter B0 has a fixed, unalterable 2 MHz clock as its own timebase, so its period is the value stored in it multiplied by 500 ns. The minimum period that can be selected for Counter B0 is 1 µs. The period of Counter A0, or the sample period, is then equal to the period of Counter B0 multiplied by the value stored in Counter A0. Regardless of the timebase chosen, the minimum sample period of 16 µs must be observed for data integrity.

Programming in Controlled Acquisition Mode

The following programming steps are required for a data acquisition operation in controlled acquisition mode:

1. Select analog input channel, gain, and timebase source for Counter A0.

   The analog input channel and gain are selected by writing to Command Register 1. The SCANEN bit must be cleared for data acquisition operations on a single channel. See the Command Register 1 bit description earlier in this chapter for gain and analog input channel bit patterns. If Counter B0 is being used as a timebase for Counter A0, then the TBSEL bit in Command Register 2 should be set at this time.

   Command Register 1 needs to be written to only when the analog input channel, gain setting, or other function needs to be changed.

2. Program Counter B0 (if necessary).

   The following sequence should be used to program Counter B0 if it is being used. If Counter B0 is not being used, skip to step 3. All writes are 8-bit write operations. All values given are hexadecimal.

   a. Write 36 to the Counter B Mode Register (select Mode 3).

   b. Write the least significant byte of the timebase count to the Counter B Data Register.

   c. Write the most significant byte of the timebase count to the Counter B Data Register. For example, programming a timebase of 10 µs requires a timebase count of

      $$\frac{10\ \mu s}{0.5\ \mu s} = 20$$

3. Program Counters A0 and A1.

   This step involves programming Counter A0 (the sample interval counter) in rate generator mode (Mode 2) and programming Counter A1 to interrupt on terminal count mode (Mode 0).

   Counter A0 of the 8253(A) Counter/Timer is used as the sample interval counter. A high-to-low transition on the Counter A0 output initiates a conversion. Counter A0 can be programmed to generate a pulse once every *N* µs. *N* is referred to as the sample interval, that is, the time between successive A/D conversions. *N* can be between 2 and 65,535. The sample interval is equal to the period of the timebase clock used by Counter A0 multiplied by *N*. Two timebases are available: a 1 MHz clock and the output of Counter B0.

   Counter A1 of the 8253(A) Counter/Timer is used as a sample counter. The sample counter tallies the number of A/D conversions initiated by Counter A0 and stops Counter A0 when the desired sample count is reached. The sample count must be less than or equal to 65,535. The minimum sample count is 3.

   Use the following programming sequence to program the sample interval counter. All writes are 8-bit write operations. All values given are hexadecimal.

   a. Write 34 to the Counter A Mode Register (select Counter A0, Mode 2).
   b. Write the least significant byte of the sample interval to the Counter A0 Data Register.
   c. Write the most significant byte of the sample interval to the Counter A0 Data Register.

   Use the following sequence to program the sample counter:

   a. Write 70 to the Counter A Mode Register (select Counter A1, Mode 0).
   b. Write the least significant byte of (*M*-2), where *M* is the sample count, to the Counter A1 Data Register.
   c. Write the most significant byte of (*M*-2), where *M* is the sample count, to the Counter A1 Data Register.

   After you complete this programming sequence, Counter A1 is configured to count A/D conversion pulses and Counter A0 output is in a high state.

4. Clear the A/D circuitry.

   Before the data acquisition operation is started, the A/D FIFO must be emptied in order to clear out any old A/D conversion results. This emptying must be performed after the counters are programmed in case any spurious edges were caused while programming the counters. Write 0 to the A/D Clear Register to empty the FIFO (8-bit write), followed by two 8-bit reads from the A/D FIFO. Ignore the data obtained in the read.

5. Start and service the data acquisition operation.

   To start the data acquisition operation, set the SWTRIG bit in Command Register 2. This enables Counter A0 to start counting.

Once the data acquisition operation is started, the operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To do this, perform the following sequence until the desired number of conversion results have been read:

a. Read the Status Register (8-bit read).

b. If the DAVAIL bit is set (bit 0), then read the A/D FIFO Register to obtain the result.

DMA or interrupts can also be used to service the data acquisition operation. These topics are discussed in the *A/D Interrupt Programming* and *Programming DMA Operation* sections later in this appendix.

Two error conditions may occur during a data acquisition operation: an overflow error or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the DAVAIL bit.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is set.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is set. The minimum recommended sampling interval on the Lab-PC+ is 16 µs.

Both the OVERFLOW and OVERRUN bits in the Status Register are reset by writing to the A/D Clear Register.

Programming in Freerun Acquisition Mode

Freerun acquisition mode uses only Counter A0 as the sample interval counter. The number of A/D conversions that have occurred (that is, the sample count) is maintained by software in this case. With this arrangement, data acquisition operations can acquire more than 65,535 samples.

The following programming steps are required for a data acquisition operation in freerun acquisition mode:

1. Select analog input channel, gain, and timebase for Counter A0.

   The analog input channel and gain are selected by writing to the A/D Configuration Register. The SCANEN bit must be cleared for data acquisition operations on a single channel. See the Command Register 1 bit description earlier in this chapter for gain and analog input channel bit patterns. If Counter B0 is being used as a timebase for Counter A0, then the TBSEL bit in Command Register 1 should be set at this time.

   Command Register 1 needs to be written to only when the analog input channel, gain setting, or other function needs to be changed.

2. Program Counter B0 (if necessary).

   The following sequence should be used to program Counter B0 if it is being used. If Counter B0 is not being used, skip to step 3. All writes are 8-bit write operations. All values given are hexadecimal.

   a. Write 36 to the Counter B Mode Register (select Mode 3).

   b. Write the least significant byte of the timebase count to the Counter B Data Register.

   c. Write the most significant byte of the timebase count to the Counter B Data Register. For example, programming a timebase of 10 µs requires a timebase count of

   $$\frac{10\ \mu s}{0.5\ \mu s} = 20$$

3. Program the sample interval counter (Counter A0).

   Counter A0 of the 8253(A) Counter/Timer is used as the sample interval counter. A high-to-low transition on OUT0 (Counter A0 output) initiates a conversion. Counter A0 can be programmed to generate a pulse once every *N* µs. *N* is referred to as the sample interval, that is, the time between successive A/D conversions. *N* can be between 2 and 65,535. The sample interval is equal to the period of the timebase clock used by Counter A0 multiplied by *N*. A 1 MHz clock is internally connected to CLK0 (the clock used by Counter A0).

   Use the following programming sequence to program Counter A0, the sample interval counter. All writes are 8-bit write operations. All values given are hexadecimal.

   a. Write 34 to the Counter A Mode Register (select Counter A0, Mode 2).

   b. Write the least significant byte of the sample interval to the Counter A0 Data Register.

   c. Write the most significant byte of the sample interval to the Counter A0 Data Register.

4. Program Counter A1 to force OUT1 low.

   If OUT1 is high, Counter A0 is disabled. Write 70 (hex) to the Counter A Mode Register (select Counter A1, Mode 0) to force OUT1 low. Counter A0 can be used as the Sample Interval Counter.

5. Clear the A/D circuitry.

   Before you start the data acquisition operation, the A/D FIFO must be emptied in order to clear out any old A/D conversion results. This emptying must be performed after the counters are programmed in case any spurious edges were caused while programming the counters. Write 0 to the A/D Clear Register to empty the FIFO (8-bit write), followed by two 8-bit reads from the A/D FIFO. Ignore the data obtained in the read.

6. Start and service the data acquisition operation.

   To start the data acquisition operation, set the SWTRIG bit in Command Register 2. This enables Counter A0 to start counting.

   Once the data acquisition operation is started, the operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To do this, perform the following sequence until the desired number of conversion results have been read:

   a. Read the Status Register (8-bit read).

   b. If the DAVAIL bit is set (bit 0), then read the A/D FIFO Register to obtain the result.

DMA or interrupts can also be used to service the data acquisition operation. These topics are discussed in the *A/D Interrupt Programming* and *Programming DMA Operation* sections later in this appendix.

Two error conditions may occur during a data acquisition operation: an overflow error or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the DAVAIL bit.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is set.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is set. The minimum recommended sampling interval on the Lab-PC+ is 16 µs.

Both the OVERFLOW and OVERRUN bits in the Status Register are cleared by writing to the A/D Clear Register.

External Timing Considerations for Multiple A/D Conversions

Two external timing signals, EXTTRIG and EXTCONV*, can be used for multiple A/D conversions. EXTTRIG can be used to initiate a conversion sequence (posttrigger mode) or to terminate an ongoing conversion sequence (pretrigger mode), and the EXTCONV* signal can be used to time the individual A/D conversions from an external timing source. Chapter 3, *Signal Connections*, contains the EXTTRIG and EXTCONV* signal specifications. The posttrigger and pretrigger modes are described later in this appendix.

EXTCONV* is available on the 50-pin I/O connector to allow conversion to be controlled by an external source. A conversion occurs whenever an active-low pulse (the pulse width is 250 ns minimum) is detected on this TTL level line. EXTCONV* can be used for both single-channel conversion sequences and multiple-channel scanning sequences. The programming steps are similar to internal timing conversions except that Counter A0 is not used and its output should be high, and OUT1 of Counter A1 must be forced low. After setting the SWTRIG bit, the first EXTCONV* pulse starts the external conversion operation, but does not cause the A/D conversion; the second pulse starts the first A/D conversion.

Using the EXTTRIG Signal to Initiate a Multiple A/D Conversion Data Acquisition Operation (Posttrigger Mode)

If both the PRETRIG bit and the SWTRIG bit are cleared, and the HWTRIG bit is set in Command Register 2, EXTTRIG functions as a start trigger for a multiple A/D conversion data acquisition operation. In this mode, referred to as posttriggering, the sample interval counter is gated off until a low-to-high edge is sensed on EXTTRIG. No samples are collected until EXTTRIG makes its low-to-high transition. Transitions on the EXTCONV* line are also ignored until a low-to-high edge is sensed on EXTRIG followed by a low-to-high edge on EXTCONV* input.

Using the EXTTRIG Signal to Terminate a Multiple A/D Conversion Data Acquisition Operation (Pretrigger Mode)

If the PRETRIG bit is set and the HWTRIG bit is cleared in Command Register 2, EXTTRIG functions as a stop trigger for a multiple A/D conversion data acquisition operation. In this mode, referred to as pretriggering, the sample counter is gated off until a low-to-high edge is sensed on EXTTRIG. Counter A0 (the sample interval counter) starts as soon as the SWTRIG bit is set. However, Counter A1, the sample counter, does not start counting until the first rising edge on EXTTRIG. In this way, data is collected before the actual trigger rising edge. After the rising edge occurs, the number of points specified in Counter A1 are collected and the acquisition stops. You must allocate sufficient array space for all of the data, and specify both the number of points and the indeterminate number of points that may be collected before the pretrigger signal arrives. Alternatively, a *circular buffer* can be set up by the acquisition software so that data is repeatedly loaded into the same section of memory. Although this method does not require an indeterminate amount of memory, you can examine only samples acquired during a limited time period before and after the trigger occurs. Pretriggering is set up by setting PRETRIG in Command Register 2. PRETRIG supersedes HWTRIG; if both bits are set, then pretriggering is enabled.

Using the EXTCONV* Signal to Initiate A/D Conversions

As mentioned earlier, A/D conversions can be initiated by a falling edge on either OUTA0 or EXTCONV*. Setting the GATA0 bit low disables conversions from both OUTA0 and EXTCONV*. Setting the GATA0 bit high enables conversions from both OUTA0 and EXTCONV*. The GATA0 bit is set low whenever OUTA1 is high or SWTRIG in Command Register 1 is cleared. If OUTA1 is low, GATA0 can be set high at any time by either setting the SWTRIG bit or initiating a rising edge on EXTTRIG if the HWTRIG bit in Command Register 1 is set.

Programming Multiple A/D Conversions Using External Timing

A data acquisition operation using the external timing signals EXTCONV* or EXTTRIG can be in either controlled acquisition mode or freerun acquisition mode. In controlled acquisition mode, Counter A1 shuts off A/D conversions after the programmed count expires. In freerun acquisition mode, A/D conversions are disabled under software control.

Programming in Controlled Acquisition Mode

Posttrigger Mode

The following programming steps are required for a data acquisition operation in controlled acquisition mode using EXTCONV*. In the following programming sequence, EXTTRIG is used as a posttrigger signal; that is, data acquisition is not started until a rising edge is detected on the EXTTRIG input.

1. Disable EXTCONV* and EXTTRIG input.

   The EXTCONV* bit can be disabled by setting the GATA0 bit low. The GATA0 bit is low whenever OUTA1 is high, regardless of the settings for the SWTRIG or HWTRIG bits in Command Register 1 or the EXTTRIG signal. Writing 78 (hex) to the Counter A Mode Register sets OUTA1 high. This write disables EXTCONV* and EXTTRIG input; that is, any transitions on these two inputs are ignored.
2. Select analog input channel and gain and select posttrigger mode.

   The analog input channel and gain are selected by writing to Command Register 1. The SCANEN bit must be cleared for data acquisition operations on a single channel. See the bit description for Command Register 1 earlier in this chapter for gain and analog input channel bit descriptions. To use posttrigger mode, the PRETRIG bit and SWTRIG bit in Command Register 2 must be cleared.

3. Program Counter A0.

   Since a high-to-low transition on the Counter A0 output initiates an A/D conversion, Counter A0 output must be programmed to a high state. This ensures that Counter A0 does not cause any A/D conversions.

   Write 34 (hex) to the Counter A Mode Register (select Counter A0, Mode 2) to force OUT0 to a high state. This is an 8-bit operation.

4. Clear the A/D circuitry.

   Before the data acquisition operation is started, the A/D FIFO must be emptied in order to clear any old A/D conversion results. This emptying must be performed after the counters are programmed in case any spurious edges were caused while programming the counters. Write 0 to the A/D Clear Register to empty the FIFO (8-bit write) and read from the A/D FIFO (8-bit read) twice. Ignore the obtained data.

5. Program Counter A1.

   Counter A1 of the 8253(A) Counter/Timer is used as a sample counter. The sample counter counts the number of A/D conversions and disable conversions when the programmed count is reached. The sample count must be less than or equal to 65,535. The minimum sample count is three.

   To program the counters, use the following programming sequence:

   a. Write 70 (hex) to the Counter A Mode Register (select Counter A1, Mode 0). This step sets the output of Counter A1 (OUTA1) low.

   b. Write the least significant byte of (*M*-2), where *M* is the sample count, to the Counter A1 Data Register.

   c. Write the most significant byte of (*M*-2), where *M* is the sample count, to the Counter A1 Data Register.

6. Select posttrigger mode and enable EXTCONV* and EXTTRIG input.

   Set the HWTRIG bit in Command Register 2. This setting enables EXTTRIG and EXTCONV*; that is, the first rising edge on EXTTRIG starts the data acquisition sequence.

7. Service the data acquisition operation.

   Once the data acquisition operation is started by a rising edge on the EXTTRIG input, A/D conversions are initiated by falling edges on the EXTCONV* input. The operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To service the data acquisition, perform the following sequence until the desired number of conversion results have been read:

   a. Read the Status Register (8-bit read).

   b. If the DAVAIL bit is set (bit 0), read the A/D FIFO Register to obtain the result.

DMA or interrupts can also be used to service the data acquisition operation. These topics are discussed in the *A/D Interrupt Programming* and *Programming DMA Operation* sections later in this appendix.

Two error conditions may occur during a data acquisition operation: an overflow error or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the DAVAIL bit.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is cleared.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is low. The minimum recommended sampling interval on the Lab-PC+ is 16 µs.

Both the OVERFLOW and OVERRUN bits in the Status Register are reset by writing to the A/D Clear Register.

Pretrigger Mode

The following programming steps are required for a data acquisition operation in controlled acquisition mode using EXTCONV*. In the following programming sequence, EXTTRIG is used as a pretrigger signal; that is, A/D conversions are enabled but the sample count is not started until a rising edge is detected on the EXTTRIG input. Data acquisition remains enabled for the programmed count after the rising edge on the EXTTRIG input. Thus, data can be acquired before and after the trigger (EXTTRIG).

1. Select analog input channel and gain and select pretrigger mode.

   The analog input channel and gain are selected by writing to Command Register 1. The SCANEN bit must be cleared for data acquisition operations on a single channel. See the bit description for Command Register 1 earlier in this chapter for gain and analog input channel bit descriptions. To select pretrigger mode, set the PRETRIG bit and clear the HWTRIG bit in Command Register 2.

2. Program Counter A0.

   Since a high-to-low transition on the Counter A0 output initiates an A/D conversion, Counter A0 output must be programmed to a high state. This ensures that Counter A0 does not cause any A/D conversions.

   Write 34 (hex) to the Counter A Mode Register (select Counter A0, Mode 2) to force OUTO to a high state. This is an 8-bit operation.

3. Clear the A/D circuitry.

   Before the data acquisition operation is started, the A/D FIFO must be emptied in order to clear any old A/D conversion results. This emptying must be performed after the counters are programmed in case any spurious edges were caused while programming the counters. Write 0 to the A/D Clear Register to empty the FIFO (8-bit write) and to read from the A/D FIFO (8-bit read) twice. Ignore the data obtained. In pretrigger mode, a write to the A/D Clear Register also sets the GATA1 bit low. A/D conversions are not counted until GATA1 is set high by a rising edge on the EXTTRIG input.

4. Program Counter A1 and enable EXTCONV* input.

   Counter A1 of the 8253(A) Counter/Timer is used as a sample counter. The sample counter counts the number of A/D conversions and disable conversions when the programmed count is reached. The sample count must be less than or equal to 65,535. The minimum sample count is 2.

   To program the counters, use the following programming sequence.

   a. Write 70 (hex) to the Counter A Mode Register (select Counter A1, Mode 0). This step sets the output of Counter A1 (OUTA1) low, which in turn, enables EXTCONV*; that is, falling edges on EXTCONV* initiate A/D conversions.

   b. Write the least significant byte of (*M*), where *M* is the sample count, after the trigger to the Counter A1 Data Register.

   c. Write the most significant byte of (*M*), where *M* is the sample count, after the trigger to the Counter A1 Data Register.

   After you complete this programming sequence, counter A1 is configured to count A/D conversion pulses and EXTTRIG input is enabled.

5. Start and service the data acquisition operation.

   To start the data acquisition operation, set the SWTRIG bit in Command Register 2. After this setting, A/D conversions are initiated by a falling edge on EXTCONV* input, but the sample counter (Counter A1) is not gated on until a rising edge on EXTTRIG input. After a rising edge on EXTTRIG input is sensed, A/D conversions remain enabled for the programmed count, after which GATA0 is set low and EXTCONV* input is disabled. The operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To service the data acquisition, perform the following sequence until GATA0 bit in the Status Register is set low:

   a. Read the Status Register (8-bit read).

   b. If the DAVAIL bit is set (bit 0), read the A/D FIFO Register to obtain the result.

DMA or interrupts can also be used to service the data acquisition operation. These topics are discussed in the *A/D Interrupt Programming* and *Programming DMA Operation* sections later in this appendix.

Two error conditions may occur during a data acquisition operation: an overflow error or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the DAVAIL bit.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is cleared.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is low. The minimum recommended sampling interval on the Lab-PC+ is 16 μs.

Both the OVERFLOW and OVERRUN bits in the Status Register are reset by writing to the A/D Clear Register.

Programming in Freerun Acquisition Mode

Posttrigger Mode

A posttrigger data acquisition in freerun acquisition mode using EXTCONV* requires a programming sequence similar to controlled acquisition mode, except that steps 5b and 5c are not performed. The sample count is kept in software and conversions remain enabled until GATA0 is set low. GATA0 can be set low by writing 34 (hex) to the Counter A Mode Register after the required number of samples is obtained. This disables EXTCONV*, that is, further transitions on EXTCONV* are ignored.

Pretrigger Mode

Pretriggering mode requires that the A/D conversions be shut off at a programmed time by the hardware after the trigger on EXTTRIG. Therefore, pretriggered data acquisition is not possible in freerun acquisition mode.

Programming Multiple A/D Conversions with Channel Scanning

The data acquisition programming sequences given earlier in this chapter are for programming the Lab-PC+ for multiple A/D conversions on a single input channel. The Lab-PC+ can also be programmed for scanning analog input channels during the data acquisition operation. Analog channels *N* through 0 can be scanned, where *N* can be 1 through 7. Programming scanned multiple A/D conversions involves the same sequence of steps as single-channel data acquisition operations except that the SCANEN bit is set in Command Register 1. When the SCANEN bit is set in Command Register 1, the analog channel select bits MA<2..0> specify the highest numbered channel in the scan sequence. For example, if MA<2..0> is 011 (binary)–that is, Channel 3 is selected and the SCANEN bit is set–the following scan sequence is used:

Channel 3, Channel 2, Channel 1, Channel 0, Channel 3, Channel 2, Channel 1, Channel 0, Channel 3, and so on.

Note: ***Selecting the analog input channel and gain should be performed in the following order:***

1. ***Write the configuration value indicating the highest channel number in the scan sequence, the gain, and the input polarity to Command Register 1. The SCANEN bit must be*** *cleared* ***during this first write to Command Register 1.***
2. ***Write the same configuration value again to Command Register 1. The SCANEN bit, however, must be*** *set* ***during the second write to Command Register 1.***

Scanning can be enabled in either controlled or freerun acquisition mode. Either Counter A0 or EXTCONV* can be used to control the scanning interval.

Programming Multiple A/D Conversions with Interval Scanning

In addition to scanning multiple channels, the Lab-PC+ can also use interval scanning if more than one channel is being scanned. If the INTSCAN bit in the Configuration Register is set, interval scanning is enabled and a single *channel-scanning cycle* is performed for every pulse received on the OUTB1 line on the I/O connector. This signal may be driven by Counter B1 or by an external source. A *channel-scanning cycle* consists of the sequence of back-to-back conversions performed while channels *N* through 0 are sampled; the duration of a channel-scanning cycle is *N*+1 times the sample interval (determined by Counter A0 or EXTCONV*). An *interval-scanning cycle* consists of a channel-scanning cycle followed by a time period in which no conversions are performed. The duration of an interval-scanning cycle is equal to the period of the signal present on the OUTB1 line. The period of this signal must be at least as long as the channel-scanning cycle. While using the interval-scanning mode, the SCANEN bit in the Analog Configuration Register is used to gate the operation of the INTSCAN bit until the data

acquisition operation is fully configured. Use the following sequence to configure the Lab-PC+ for interval scanning:

1. Write the configuration value indicating the highest channel number in the scan sequence, the gain, and the input polarity to the Analog Configuration Register. The SCANEN bit must be *clear* during this first write to the Analog Configuration Register. Immediately write a 0 to the INTSCAN bit in the Command Register 4. The EOIRCV bit should be configured with the desired value. These two writes should be performed prior to any other configuration steps.

2. Configure the remainder of the data acquisition circuitry as specified in any of the previous outlines.

3. After programming the sample-interval counter (Counter A0) or configuring the circuitry to use EXTCONV*, configure the interval-scanning counter (Counter B1), if necessary. Use the following sequence to program this counter. All writes are 8-bit write operations. All values given are hexadecimal.

   a. Write 74 to the Counter B Mode Register (select Mode 2).

   b. Write the least significant byte of the scan-interval count to the Counter B1 Data Register.

   c. Write the most significant byte of the scan-interval count to the Counter B1 Data Register.

   If you intend to use Counter B1 to generate your scan-interval pulses, remember to connect a source to the CLKB1 line on the I/O connector.

4. Finally, take the Analog Configuration Register bit pattern used in step 1, set the SCANEN bit, and write the value to the Analog Configuration Register. As soon as this value is written, the interval-scanning circuitry is gated on. A channel-scanning cycle will commence immediately following the first rising edge that occurs on OUTB1 (after SCANEN is set). Subsequent channel-scanning cycles will then commence at the interval determined by the signal on OUTB1.

Programming Multiple A/D Conversions in Single-Channel Interval Acquisition Mode

The Lab-PC+ can perform interval sampling on a single input channel. You enable single-channel interval acquisition by setting the INTSCAN bit in Command Register 4 and clearing the SCANEN bit in Command Register 1. Counter B1 determines the interval, just as in the interval scan mode. You must program the number of samples to be taken between each interval in the Interval Counter. The interval counter is armed when you write a count of *N* in the Interval Counter Data Register and strobe the count into the counter. You must then program Counter B1 for the interval, which should be greater than (*N* * sample interval). A software trigger starts the sampling sequence. The Lab-PC+ takes *N* samples on the specified channel, after which acquisition halts until the next interval pulse is generated on OUTB1. The Lab-PC+ takes

another *N* samples and the cycle repeats. The operation stops when the sample counter (Counter A1) decrements to 0. Use the following sequence to configure the Lab-PC+ for single-channel interval acquisition mode.

1. Write the count to the Interval Counter Data Register and strobe it in the counter.

2. Write the channel number and gain in Command Register 1. Write 0 to the SCANEN bit.

3. Write 1 to the INTSCAN bit in Command Register 4. Configure the EOIRCV bit with the desired value.

4. Configure the remainder of the data acquisition circuitry as specified in any of the previous outlines.

5. After programming the sample-interval counter (Counter A0) and the sample counter (Counter A1), or configuring the circuitry to use EXTCONV*, configure the interval-scanning counter (Counter B1) if necessary. Use the following sequence to program the interval-scanning counter. All writes are 8-bit write operations. All values are hexadecimal.

   a. Write 74 to the Counter B Mode Register (select Mode 2).

   b. Write the least significant byte of the interval count to the Counter B1 Data Register.

   c. Write the most significant byte of the scan-interval count to the Counter B1 Data Register.

6. Use a software trigger to initiate the operation.

Note that you must program the sample counter (Counter A1) for the total number of samples desired. For example, if you want to acquire 2,000 samples in batches of 100, load the Interval Counter with 100 and load the sample counter with 2,000.

A/D Interrupt Programming

Two different interrupts are generated by the A/D circuitry:

- An interrupt whenever a conversion is available to be read for FIFO

- An interrupt whenever an error condition (overflow or overrun) is detected

These two interrupts are enabled individually.

To use the conversion interrupt, set the FIFOINTEN bit in Command Register 3. If this bit is set, an interrupt is generated whenever the DAVAIL bit in the Status Register is set. This interrupt condition is cleared when the FIFO is emptied by reading its contents.

To use the error interrupt, set the ERRINTEN bit in the Command Register 3. If this bit is set, an interrupt is generated whenever the OVERFLOW or the OVERRUN bit in the Status Register is set. This interrupt condition is cleared by writing to the A/D Clear Register.

Programming DMA Operation

The Lab-PC+ can be programmed so that the FIFO generates a DMA request signal every time one or more A/D conversion values are stored in the FIFO. To program the DMA operation, perform the following steps after the A/D circuitry is set up for a data acquisition operation and before the data acquisition operation begins:

1. Set the DMAEN bit in Command Register 3 to enable DMA request generation.

2. Program the DMA controller to service DMA requests from the Lab-PC+ board. Because the DMA transfer is an 8-bit operation, the transfer number written to the DMA Controller Count Register should be twice the number of conversions.

3. If a DMA terminal count is received after the DMA service, writing to the DMATC Clear Register clears the DMATC bit in the Status Register.

Once step 1 and step 2 are completed, the DMA controller automatically reads the FIFO Register whenever an A/D conversion result is available and then stores the result in a buffer in memory (the data type of the buffer can be 16-bit data).

A DMATC interrupt can be generated by a Lab-PC+ board. To use the DMA terminal count interrupt, set the DMAEN and TCINTEN bits in Command Register 3. If these bits are set, an interrupt is generated and the DMATC bit in the Status Register is set whenever the DMATC pulse is detected. Writing to the DMATC Clear Register clears this interrupt condition.

Programming the Analog Output Circuitry

The analog output circuitry on the Lab-PC+ uses double-buffered DACs. Thus, the voltage at the output pins (pins DAC0 OUT and DAC1 OUT on the Lab-PC+ I/O connector) does not have to be updated immediately with each write to the DAC Data Registers. The analog output can be updated in synchronization with Counter A2 output or the external update control signal EXTUPDATE*. This ability is useful for waveform generation applications because the timed update pulses eliminate the timing jitter associated with software writes to the DAC Data Registers.

The voltage at the analog output circuitry pins (pins DAC0 OUT and DAC1 OUT on the Lab-PC+ I/O connector) is controlled by loading the DAC in the analog output channel with a 12-bit digital code. The DACs can be loaded by writing the digital code to the DAC0 and DAC1 Data Registers (L and H). Writing to the DAC0 Data Register loads DAC0, and writing to the DAC1 Data Register loads DAC1. The analog output on pins DAC0 OUT or DAC1 OUT can be updated in one of three ways: immediately when the DAC0 or the DAC1 Data Register is written to, when a low level is detected on the EXTUPDATE* pin, or when a low level is detected on the output of Counter A (OUTA2). The LDAC bits in Command Register 2 determine which update method is used. If LDAC0 is set high, the analog output from DAC0 is

updated when a low level is detected on either EXTUPDATE* or OUTA2. If LDAC0 is set low, the analog output from DAC0 is updated as soon as the DAC0 Data Register is written to. LDAC1 controls the updating of DAC1 analog output in a similar manner.

The output voltage generated from the digital code depends on the configuration, unipolar or bipolar, of the associated analog output channel. Unipolar or bipolar configuration is determined by jumper settings described in Chapter 2, *Configuration and Installation*. Table E-3 shows the output voltage versus digital code for a unipolar analog output configuration. Table E-4 shows the voltage versus digital code for a bipolar analog output configuration.

The following formula calculates the voltage output versus digital code for a unipolar analog output configuration and straight binary coding:

$$V_{out} = 10.0 * \frac{\text{(digital code)}}{4{,}096}$$

The digital code in the preceding formula is a decimal value ranging from 0 to +4,095. Notice that straight binary coding is selected by clearing the 2SDAC bit in Command Register 2.

Table E-3. Analog Output Voltage Versus Digital Code
(Unipolar Mode, Straight Binary Coding)

Digital Code		**Voltage Output**
(Decimal)	**(Hex)**	
0	0000	0 V
1	0001	2.4414 mV
2,048	0800	5.0 V
4,095	0FFF	9.9976 V

The following formula calculates the voltage output versus digital code for a bipolar analog output configuration and two's complement coding:

$$V_{out} = 5.0 * \frac{(\text{digital code})}{2{,}048}$$

The digital code in the above formula is a decimal value ranging from -2,048 to +2,047. Notice that two's complement mode coding is selected by setting the 2SDAC bit high in Command Register 2.

Table E-4. Analog Output Voltage Versus Digital Code
(Bipolar Mode, Two's Complement Coding)

Digital Code		**Voltage Output**
(Decimal)	**(Hex)**	**(V_{ref} = 10 V)**
-2,048	F800	-5.0 V
-1,024	FC00	2.5 V
0	0000	0.0 V
1,024	0400	2.5 V
2,047	07FF	4.9976 V

Interrupt Programming for the Analog Output Circuitry

Interrupts can be used for writing successive values in a sequence to the DAC Data Registers during a waveform generation operation. The CNTINTEN bit in Command Register 3 enables and disables Counter A2 and EXTUPDATE* driven interrupts. See Chapter 3, *Signal Connections*, for timing requirements on the EXTUPDATE* signal.

The following programming steps are required for waveform generation using interrupts:

1. Set up Command Register 2.

   The LDAC0 bit must be set high for enabling OUTA2 or EXTUPDATE* driven updates on DAC0. LDAC1 bit must be set high for enabling OUTA2 or EXTUPDATE* driven updates on DAC1.

2. Program Counter A2.

   If EXTUPDATE* is being used to update the DACs, Counter A2 output (OUTA2) must be set high by writing B8 (hex) to the Counter A Mode Register. If OUTA2 is being used to update the DACs, EXTUPDATE* must be left unconnected or driven to a TTL-high level. Counter A2 must be programmed in Mode 2 with the appropriate update interval.

3. Enable timer interrupts.

   Timer interrupts refer to the interrupts generated by rising edges on OUTA2 or EXTUPDATE*. A rising edge on OUTA2 or EXTUPDATE* sets the CNTINT bit high in the Status Register. A timer interrupt is generated whenever the CNTINT bit in the Status Register and the CNTINTEN bit in Command Register 3 are set high. Set the CNTINTEN bit in Command Register 3 high to enable timer interrupts.

Programming the Digital I/O Circuitry

The digital I/O circuitry is designed around an 8255A integrated circuit. The 8255A is a general-purpose PPI containing 24 programmable I/O pins. These pins represent the three 8-bit I/O ports (A, B, and C) of the 8255A. These ports can be programmed as two groups of 12 signals or as three individual 8-bit ports. The following paragraphs include programming information for the Lab-PC+.

The three 8-bit ports are divided into two groups: Group A and Group B (two groups of 12 signals). One 8-bit configuration (or control) word specifies the mode of operation for each group. The control bits of Group A configure Port A (A0 through A7) and the upper 4 bits (nibble) of Port C (C4 through C7). The control bits of Group B configure Port B (B0 through B7) and the lower nibble of Port C (C0 through C3). These configuration bits are defined later in this chapter.

Register Descriptions and Programming Examples

The following figures show the two control-word formats used to completely program the 8255A. The control-word flag determines which control-word format is being programmed. When the control-word flag is 1, bits 0 through 6 specify the I/O characteristics of the 8255A's ports and the mode in which they are operating (that is, Mode 0, Mode 1, or Mode 2). When the control-word flag is 0, bits 3 through 0 specify the bit set/reset format of Port C.

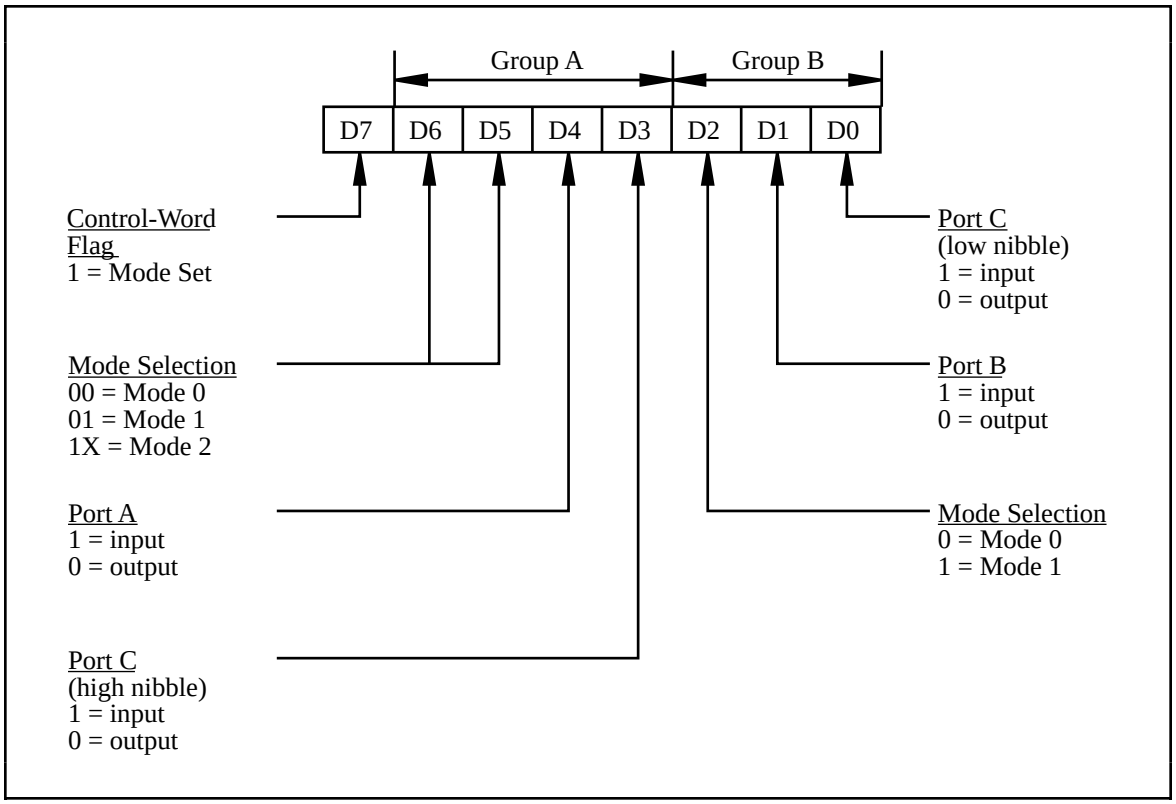


Figure E-1. Control-Word Format with Control-Word Flag Set to 1

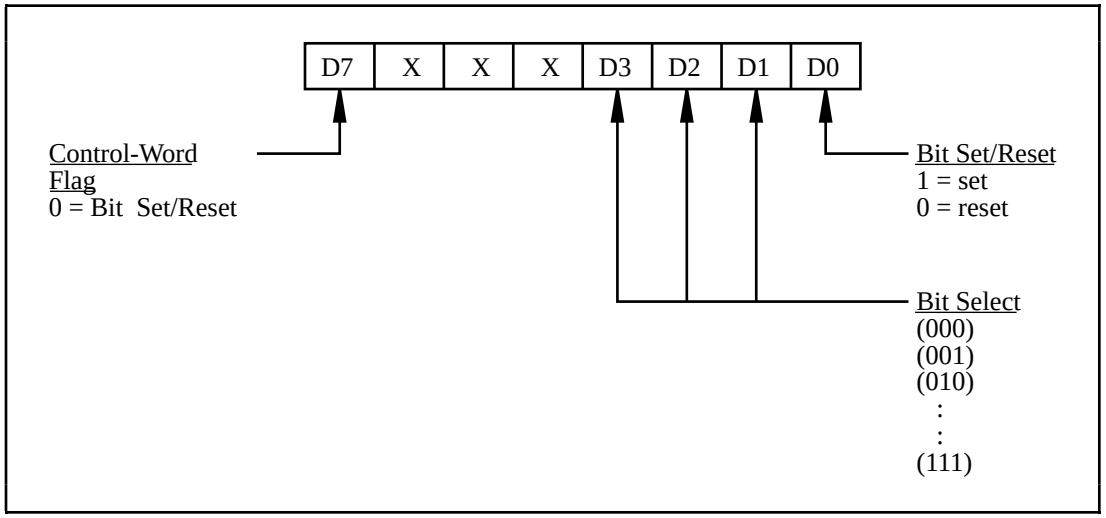


Figure E-2. Control-Word Format with Control-Word Flag Set to 0

This section describes the Digital Control Register, which is used to program the 8255A ports in any one of the three modes discussed earlier in this section. Specific control words for each mode are described later in this section along with programming examples for each mode.

Modes of Operation for the 8255A

The three basic modes of operation for the 8255A are as follows:

- Mode 0 – Basic I/O
- Mode 1 – Strobed I/O
- Mode 2 – Bidirectional bus

The 8255A also has a single bit set/reset feature for Port C. The 8-bit control word also programs this function. For additional information, refer to Appendix C, *OKI 82C55A Data Sheet*.

Mode 0

This mode is for simple I/O operations for each of the ports. No handshaking is required; data is simply written to or read from a specified port.

Mode 0 has the following features:

- Two 8-bit ports (A and B) and two 4-bit ports (upper and lower nibble of Port C).
- Any port can be input or output.
- Outputs are latched, but inputs are not latched.

Control Words

Mode 0 provides simple I/O functions for each of the three ports with no handshaking. Each port can be assigned as an input port or as an output port. The 16 possible I/O configurations are shown in Table E-5. Notice that bit 7 of the control word is set when programming the mode of operation for each port.

Table E-5. Mode 0 I/O Configurations

Control Word	Group A		Group B	
Bit 76543210	**Port A**	**Port C[1]**	**Port B**	**Port C[2]**
10000000	Output	Output	Output	Output
10000001	Output	Output	Output	Input
10000010	Output	Output	Input	Output
10000011	Output	Output	Input	Input
10001000	Output	Input	Output	Output
10001001	Output	Input	Output	Input
10001010	Output	Input	Input	Output
10001011	Output	Input	Input	Input
10010000	Input	Output	Output	Output
10010001	Input	Output	Output	Input
10010010	Input	Output	Input	Output
10010011	Input	Output	Input	Input
10011000	Input	Input	Output	Output
10011001	Input	Input	Output	Input
10011010	Input	Input	Input	Output
10011011	Input	Input	Input	Input

[1] Upper nibble of Port C
[2] Lower nibble of Port C

Programming Examples

Example 1. Configure all three ports (A, B, and C) as output ports in Mode 0:

- Write 80 (hex) to the Digital Control Register.
- Write 8-bit data to the Port A, Port B, or Port C Register as appropriate.

Example 2. Configure Port A for input, Port B and Port C for output:

- Write 90 (hex) to the Digital Control Register.
- Write 8-bit data to Port B or Port C. Read 8-bit data from Port A as appropriate.

Example 3. Configure Port A and Port C for output, Port B for input:

- Write 82 (hex) to the Digital Control Register.

Example 4. Configure Port A and B for output, Port C for input:

- Write 89 (hex) to the Digital Control Register.

Mode 1

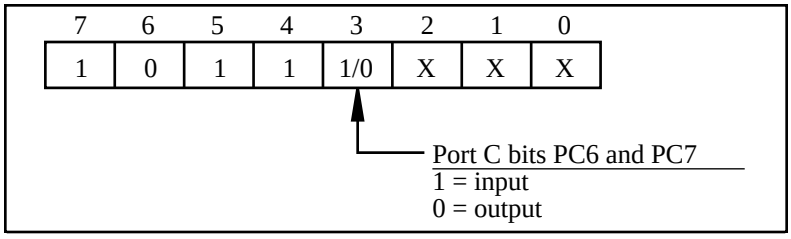
This mode is used for transferring data with handshake signals. Ports A and B use the eight lines of Port C to generate or receive the handshake signals. This mode divides the ports into two groups (Group A and Group B).

- Each group contains one 8-bit data port (Port A or Port B) and one 4-bit control/data port (upper or lower nibble of Port C).
- The 8-bit data ports can be either input or output, both of which are latched.
- The 4-bit ports are used for control and status of the 8-bit data ports.
- Interrupt generation and enable/disable functions are available.

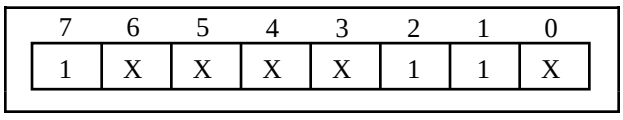
Input

In Mode 1, the digital I/O bits are divided into two groups: Group A and Group B. Each of these groups contains one 8-bit port and one 4-bit control/data port. The 8-bit port can be either an input port or an output port, and the 4-bit port is used for control and status information for the 8-bit port. The transfer of data is synchronized by handshaking signals in the 4-bit port.

The control word written to the Digital Control Register to configure Port A for input in Mode 1 is shown here. Bits PC6 and PC7 of Port C can be used as extra input or output lines.



The control word written to the Digital Control Register to configure Port B for input in Mode 1 is shown here. Notice that Port B is not provided with extra input or output lines from Port C.



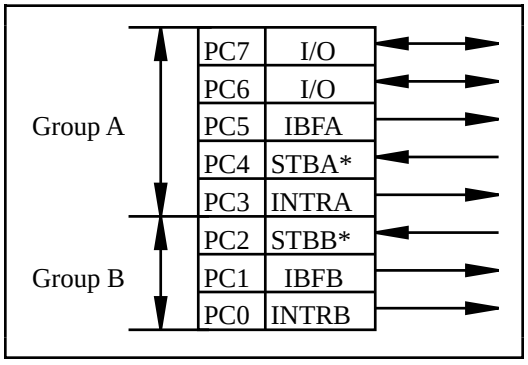
During a Mode 1 data read transfer, the status of the handshaking lines and interrupt signals can be obtained by reading Port C. The Port C status-word bit definitions for an input transfer are shown next.

Port C status-word bit definitions for input (Port A and Port B):

7	6	5	4	3	2	1	0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB

Bit	Name	Description
7-6	I/O	Extra I/O status lines when Port A is in Mode 1 input.
5	IBFA	Input buffer full for Port A. High indicates that data has been loaded into the input latch for Port A.
4	INTEA	Interrupt enable bit for Port A. Enables interrupts from the 8255A for Port A. Controlled by bit set/reset of PC4.
3	INTRA	Interrupt request status for Port A. When INTEA is high and IBFA is high, this bit is high, indicating that an interrupt request is asserted.
2	INTEB	Interrupt enable bit for Port B. Enables interrupts from the 8255A for Port B. Controlled by bit set/reset of PC2.
1	IBFB	Input buffer full for Port B. High indicates that data has been loaded into the input latch for Port B.
0	INTRB	Interrupt request status for Port B. When INTEB is high and IBFB is high, this bit is high, indicating that an interrupt request is asserted.

At the digital I/O connector, Port C has the following pin assignments when in Mode 1 input. Notice that the status of STBA* and STBB* is not provided in the Port C status word.



Programming Example

Example 1. Configure Port A as an input port in Mode 1:

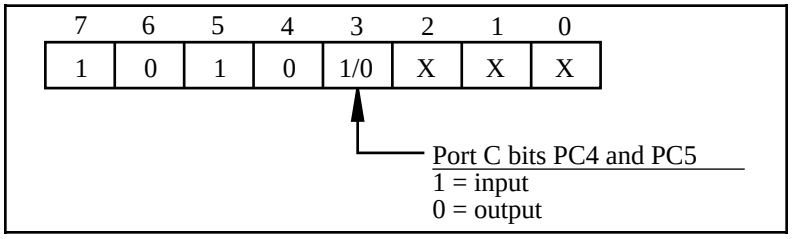
- Write B0 (hex) to the Digital Control Register.
- Wait for bit 5 of Port C (IBFA) to be set, indicating that data has been latched into Port A.
- Read data from Port A.

Example 2. Configure Port B as an input port in Mode 1:

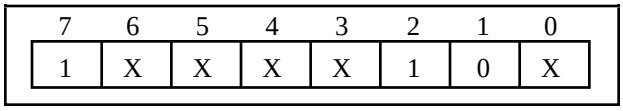
- Write 86 (hex) to the Digital Control Register.
- Wait for bit 1 of Port C (IBFB) to be set, indicating that data has been latched into Port B.
- Read data from Port B.

Output

The control word written to the Digital Control Register to configure Port A for output in Mode 1 is shown here. Bits PC4 and PC5 of Port C can be used as extra input or output lines when Port A uses Mode 1 output.



The control word written to the Digital Control Register to configure Port B for output in Mode 1 is shown here. Notice that Port B is not provided with extra input or output lines from Port C.



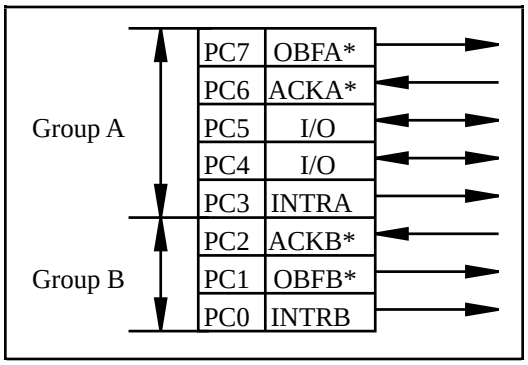
During a Mode 1 data write transfer, the status of the handshaking lines and interrupt signals can be obtained by reading Port C. Notice that the bit definitions are different for a write and a read transfer.

Port C status-word bit definitions for output (Port A and Port B):

7	6	5	4	3	2	1	0
OBFA*	INTEA	I/O	I/O	INTRA	INTEB	OBFB*	INTRB

Bit	Name	Description
7	OBFA*	Output buffer full for Port A. Low indicates that the CPU has written data out to Port A.
6	INTEA	Interrupt enable bit for Port A. If this bit is high, interrupts are enabled from the 8255A for Port A. Controlled by bit set/reset of PC6.
5,4	I/O	Extra I/O status line when Port A is in Mode 1 output.
3	INTRA	Interrupt request status for Port A. When INTEA is high and OBFA* is high, this bit is high, indicating that an interrupt request is asserted.
2	INTEB	Interrupt enable bit for Port B. If this bit is high, interrupts are enabled from the 8255A for Port B. Controlled by bit set/reset of PC2.
1	OBFB*	Output buffer full for Port B. Low indicates that the CPU has written data out to Port B.
0	INTRB	Interrupt request status for Port B. When INTEB is high and OBFB* is high, this bit is high, indicating that an interrupt request is asserted.

At the digital I/O connector, Port C has the following pin assignments when in Mode 1 output. Notice that the status of ACKA* and ACKB* is not provided when Port C is read.



Programming Example

Example 1. Configure Port A as an output port in Mode 1:

- Write A0 (hex) to the Digital Control Register.
- Wait for bit 7 of Port C (OBFA*) to be cleared, indicating that the data last written to Port A has been read.
- Write new data to Port A.

Example 2. Configure Port B as an output port in Mode 1:

- Write 84 (hex) to the Digital Control Register.
- Wait for bit 1 of Port C (OBFB*) to be cleared, indicating that the data last written to Port B has been read.
- Write new data to Port A.

Mode 2

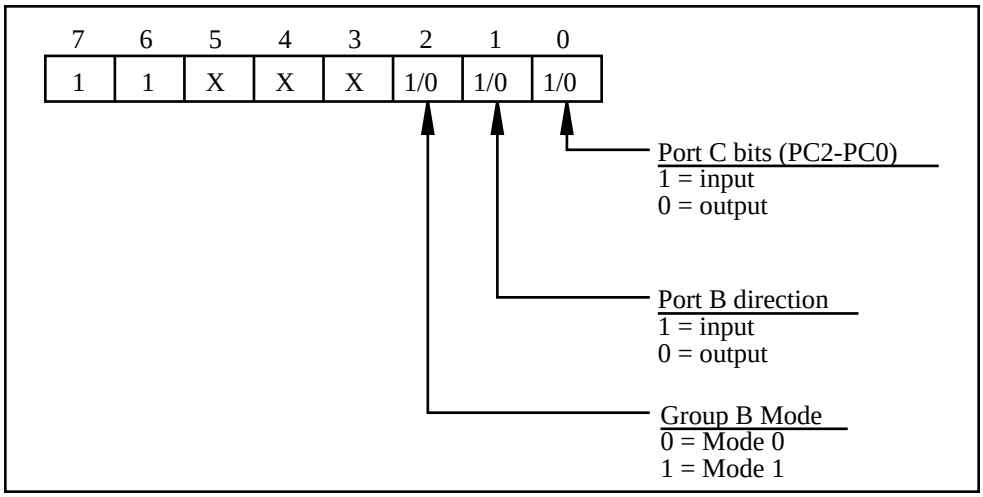
This mode is for communication over a bidirectional 8-bit bus. Handshake signals can be used in a manner similar to Mode 1. Interrupt generation and enable/disable functions are also available. Other features of this mode include the following:

- Used in Group A only (Port A and upper nibble of Port C).
- One 8-bit bidirectional port (Port A) and a 5-bit control status port (Port C).
- Both inputs and outputs are latched.

Control Words

In Mode 2, an 8-bit bus can be used for both input and output transfers without changing the configuration. The data transfers are synchronized with handshaking lines in Port C. This mode uses only Port A; however, Port B can be used in either Mode 0 or Mode 1 while Port A is configured for Mode 2.

The control word written to the Digital Control Register to configure Port A as a bidirectional data bus in Mode 2 is shown below. Because Mode 2 is for Port A only, Port B can be programmed to operate in Mode 0 or Mode 1. If Port B is configured for Mode 0, then PC2, PC1, and PC0 of Port C can be used as extra input or output lines.



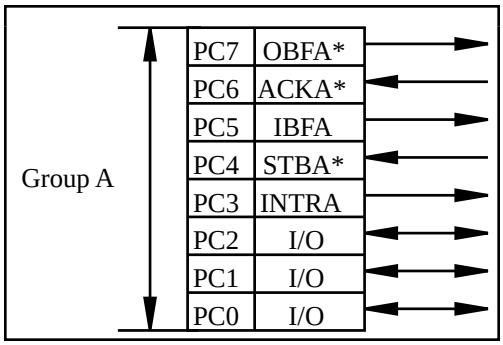
During a Mode 2 data transfer, the status of the handshaking lines and interrupt signals can be obtained by reading Port C. The Port C status-word bit definitions for a Mode 2 transfer are shown next.

Port C status-word bit definitions for bidirectional data path (Port A only):

7	6	5	4	3	2	1	0
OBFA*	INTE1	IBFA	INTE2	INTRA	I/O	I/O	I/O

Bit	Name	Description
7	OBFA*	Output buffer full. Low indicates that the CPU has written data out to Port A.
6	INTE1	Interrupt enable bit for output. If this bit is set, interrupts are enabled from the 8255A for OBF*. Controlled by bit set/reset of PC6.
5	IBFA	Input buffer full. High indicates that data has been loaded into the input latch of Port A.
4	INTE2	Interrupt enable bit for input. If this bit is set, interrupts are enabled from the 8255A for IBF. Controlled by bit set/reset of PC4.
3	INTRA	Interrupt request status. If INTE1 is high and IBFA is high, this bit is high, indicating that an interrupt request is asserted for input transfers. If INTE2 is high and OBFA* is high, this bit is high, indicating that an interrupt request is asserted for output transfers.
2-0	I/O	Extra I/O status lines available if Port B is not configured for Mode 1.

At the digital I/O connector, Port C has the following pin assignments when in Mode 2.



Programming Example

Example. Configure Port A in Mode 2:

- Write C0 (hex) to the Digital Control Register.
- Wait for bit 7 of Port C (OBFA*) to be cleared, indicating that the data last written to Port A has been read.
- Write new data to Port A.
- Wait for bit 5 of Port C (IBFA) to be set, indicating that data is available in Port A to be read.
- Read data from Port A.

Single Bit Set/Reset Control Words

Table E-6 shows the control words for setting or resetting each bit in Port C. Notice that bit 7 of the control word is cleared for programming the set/reset option for the bits of Port C.

Table E-6. Port C Set/Reset Control Words

Bit Set Control Word	Bit Reset Control Word	The Bit Set or Reset in Port C
0xxx0001	0xxx0000	xxxxxxxn
0xxx0011	0xxx0010	xxxxxxnx
0xxx0101	0xxx0100	xxxxxnxx
0xxx0111	0xxx0110	xxxxnxxx
0xxx1001	0xxx1000	xxxnxxxx
0xxx1011	0xxx1010	xxnxxxxx
0xxx1101	0xxx1100	xnxxxxxx
0xxx1111	0xxx1110	nxxxxxxx

Single Bit Set/Reset Feature

Any of the 8 bits of Port C can be set or reset with one control word. This feature is used to generate status and control for Port A and Port B when operating in Mode 1 or Mode 2.

Interrupt Programming for the Digital I/O Circuitry

Interrupts can be enabled on PC0, PC3, or both PC0 and PC3 by setting the DIOINTEN bit in Command Register 3. See the Command Register 3 description earlier in this chapter for corresponding bit positions.

An external signal can be used to generate an interrupt when Port A or B is in Mode 0. Program PC0 or PC3 for input and connect the external signal that should trigger an interrupt to PC0 or PC3. When the external signal becomes logic high, an interrupt request occurs. To negate the interrupt request, the external signal must become logic low.

Appendix F
Customer Communication

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Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

°	degrees
Ω	ohms
%	percent
A	amperes
A/D	analog-to-digital
AC	alternating current
ADC	A/D converter
AWG	American Wire Gauge
BCD	binary-coded decimal
C	Celsius
CMOS	complementary metallic oxide semiconductor
D/A	digital-to-analog
DAC	D/A converter
dB	decibels
DC	direct current
DIFF	differential
DIP	dual inline package
DMA	direct memory access
EISA	Extended Industry Standard Architecture
F	farads
FIFO	first-in-first-out
ft	feet
hex	hexadecimal
Hz	hertz
I/O	input/output
in.	inches
ksamples	1,000 samples
LED	light-emitting diode
LSB	least significant bit
M	megabytes of memory
m	meters
MSB	most significant bit

NRSE	non-referenced single-ended
PPI	programmable peripheral interface
ppm	parts per million
PS/2	IBM Personal System/2
R_{EXT}	external resistance
RSE	referenced single-ended
RTSI	Real-Time System Integration
s	seconds
SCXI	Signal Conditioning eXtensions for Instrumentation (bus)
SDK	System Development Kit
STC	system timing controller
TTL	transistor-to-transistor logic
V	volts
VDC	volts direct current
V_{EXT}	external volts
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{out}	output voltage
V_{ref}	reference voltage

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