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NB-AO-6
User Manual

Expansion Board for Macintosh NuBus Computers

July 1993 Edition

Part Number 320098-01

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Preface

This manual describes the mechanical and electrical aspects of the NB-AO-6 and contains information concerning its operation and programming. The NB-AO-6 is a high-performance analog output expansion board for Macintosh NuBus computers. The board contains six 12-bit DACs with voltage and current outputs and reference voltage inputs. The NB-AO-6 is one of the National Instruments NB Series boards for the Macintosh NuBus family of computers.

Organization of This Manual

The *NB-AO-6 User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the NB-AO-6, lists the contents of your NB-AO-6 kit, describes the optional software and optional equipment, and explains how to unpack your NB-AO-6.
- Chapter 2, *Configuration and Installation*, describes the jumper configuration, installation of the NB-AO-6 in the Macintosh, signal connections to the NB-AO-6, timing, field wiring, and cabling.
- Chapter 3, *Theory of Operation*, contains a functional overview of the NB-AO-6 and explains the operation of each functional unit making up the NB-AO-6.
- Chapter 4, *Programming*, describes in detail the address and function of each of the NB-AO-6 registers. This chapter also includes important information about programming the NB-AO-6 for DMA and timer operations.
- Chapter 5, *Calibration Procedures*, explains how to recalibrate the NB-AO-6 analog circuitry.
- Appendix A, *Specifications*, lists the specifications of the NB-AO-6.
- Appendix B, *I/O Connector*, shows the pinout and signal names for the 50-pin I/O connector on the NB-AO-6.
- Appendix C, *Customer Communication*, contains forms for you to complete to facilitate communication with National Instruments concerning our products.

Conventions Used in This Manual

The following conventions are used throughout this manual:

DMA board	DMA board refers to the NB-DMA-8-G board or the NB-DMA2800 board unless otherwise noted.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
Macintosh	Macintosh refers to all Macintosh II and Macintosh Quadra computers unless otherwise noted.

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Abbreviations

The following metric system prefixes are used with abbreviations for units of measure in this manual:

Prefix	Meaning	Value
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

The following abbreviations are used in this manual:

A	amperes
dB	decibels
°	degrees
ft	feet
hex	hexadecimal
in.	inches
I_{out}	output current
M	megabytes of memory
ppm	parts per million
sec	seconds
V	volts
V_{out}	volts out

Acronyms

The following acronyms are used in this manual:

AC	alternating current
AWG	American Wire Gauge
D/A	digital-to-analog
DAC	D/A converter
DC	direct current
DMA	direct memory access
FSK	frequency shift keying
LSB	least significant bit
MSB	most significant bit
ROM	read-only memory
RTSI	Real-Time System Integration
VDC	volts direct current
VI	virtual instrument

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Related Documentation

The following documents contain information that you may find helpful if you are writing your own Macintosh programs:

- The Macintosh II or Quadra *Owner's Manual*, *Getting Started* manual, or *Setting Up* manual

Consult the following National Instruments manuals if you plan to program DMA operations with this board:

- The *NB-DMA-8-G User Manual* (part number 320097-01)
- The *NB-DMA2800 User Manual* (part number 320240-01)

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix C, *Customer Communication*, at the end of this manual.

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Contents

Chapter 1
Introduction 1-1
- What Your Kit Should Contain 1-2
- Optional Software 1-2
- Optional Equipment 1-3
- Unpacking 1-3

Chapter 2
Configuration and Installation 2-1
- Board Configuration 2-1
  - Jumpers 2-1
    - Internal/External Reference 2-1
    - Bipolar/Unipolar Output 2-1
    - Offset Binary/Two's Complement 2-1
    - Local/Remote Sensing 2-1
- Installation 2-5
- Signal Connections 2-6
  - Output Connector 2-6
- Timing Diagrams 2-8
- Field Wiring and Cabling 2-10
  - Field Wiring Considerations 2-10
  - Cabling Considerations 2-10

Chapter 3
Theory of Operation 3-1
- Double Buffering 3-2
- Reference Inputs 3-3
- Voltage Output Connections 3-4
- Remote Sensing 3-4
- Driving High-Current Loads 3-6
- Current Loop Connections 3-8

Chapter 4
Programming 4-1
- Register Access 4-1
  - Slot Address Space 4-1
  - Register Map 4-1
  - Register Sizes 4-2
- Register Description 4-2
  - Register Description Format 4-2
  - Analog Output Register Group 4-3
    - D/A Registers 4-4
    - Update Register 4-8
  - Configuration Register Group 4-9
    - Configuration Register 4-10
  - RTSI Switch Register Group 4-11
    - RTSI Switch Shift Register 4-12

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RTSI Switch Strobe Register 4-13
Configuration ROM 4-14
Programming Considerations 4-15
Register Programming Considerations 4-15
RTSI Bus Trigger Line Programming Considerations 4-15
Programming the RTSI Switch 4-16
Programming DMA Operations 4-18

Chapter 5
Calibration Procedures 5-1
Voltage Reference 5-2
D/A Offsets 5-2
D/A Gains 5-3

Appendix A
Specifications A-1
Analog Outputs A-1
Throughput A-2
Power Requirements (from NuBus) A-2
Physical A-3
Operating Environment A-3
Storage Environment A-3

Appendix B
I/O Connector B-1

Appendix C
Customer Communication C-1

Figures

Figure 1-1. NB-AO-6 Interface Board 1-1

Figure 2-1. NB-AO-6 Parts Locator Diagram 2-2
Figure 2-2. Default Settings for Jumpers W1 through W6 2-3
Figure 2-3. Default Settings for Jumpers W7, W8, and W9 2-4
Figure 2-4. Default Settings for Jumpers W10, W11, and W12 2-4
Figure 2-5. Default Settings for Jumpers W13, W14, and W15 2-4
Figure 2-6. Default Settings for Jumpers W16, W17, and W18 2-5
Figure 2-7. Default Settings for Jumpers W19, W20, and W21 2-5
Figure 2-8. Default Settings for Jumpers W22, W23, and W24 2-5
Figure 2-9. NB-AO-6 I/O Connector 2-7
Figure 2-10. Falling-Edge Sensitive Timing 2-8
Figure 2-11. Rising-Edge Sensitive Timing 2-9
Figure 2-12. DMA Request Generation Timing 2-9

Figure 3-1. NB-AO-6 Block Diagram 3-1
Figure 3-2. Block Diagram of D/A Channel X 3-2
Figure 3-3. Remote-Sense Connections 3-5

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Figure 3-4. Driving a Heavy Load with an External Buffer 3-7
Figure 3-5. Using a Slow-Power Buffer 3-8
Figure 3-6. Output Sink Current Versus Output Voltage 3-9
Figure 3-7. Possible Current Loop Connection 3-9

Figure 4-1. RTSI Switch Control Pattern 4-17

Figure 5-1. NB-AO-6 Trimpot Locator Diagram 5-1

Figure B-1. NB-AO-6 I/O Connector B-1

Tables

Table 2-1. Jumper Settings 2-3

Table 4-1. Macintosh NuBus Slot Addresses 4-1
Table 4-2. NB-AO-6 Register Map 4-2
Table 4-3. Analog Output Voltage Versus Digital Code (Unipolar Mode) 4-5
Table 4-4. Analog Output Voltage Versus Digital Code (Bipolar, Straight Binary Mode) 4-6
Table 4-5. Analog Output Voltage Versus Digital Code (Bipolar, Two's Complement Mode) 4-7
Table 4-6. RTSI Switch Signal Connections 4-16

Table 5-1. Voltmeter Connections for Each DAC 5-3
Table 5-2. DAC Adjustment Potentiometers 5-4

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Chapter 1
Introduction

This chapter describes the NB-AO-6, lists the contents of your NB-AO-6 kit, describes the optional software and optional equipment, and explains how to unpack your NB-AO-6.

The NB-AO-6 is a high-performance analog output expansion board for Macintosh NuBus computers. The board has six identical DAC channels, each of which has a 4 to 20 mA current output and a voltage output. The voltage output of each channel is either bipolar or unipolar and is derived from one of the onboard references (2.5 V and 10 V) or from an external reference. The NB-AO-6 is interfaced to the National Instruments RTSI bus to provide DMA in conjunction with a DMA board for high-speed function generation.

The NB-AO-6 is designed to be used in environments such as automation of machine and process control, instrumentation, and electronic test signal generation. The analog voltage outputs can be used for functions such as 12-bit resolution voltage sourcing, analog function generation, and control signal output. The 4 to 20 mA current outputs can be used in industrial control loops or any application that would benefit from the inherent noise immunity of two-wire current loop communication. Detailed specifications for the NB-AO-6 are provided in Appendix A, *Specifications*.

Figure 1-1 shows the NB-AO-6 interface board.

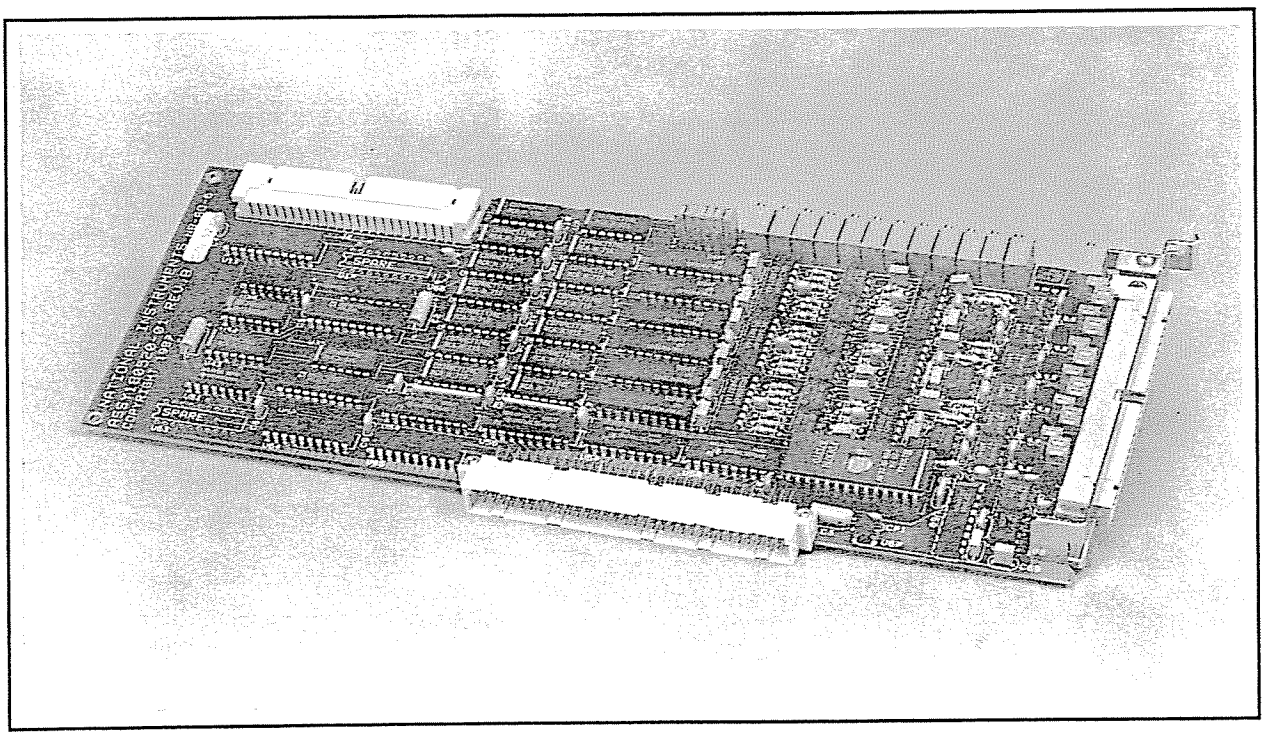


Figure 1-1. NB-AO-6 Interface Board

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What Your Kit Should Contain

The contents of the NB-AO-6 kit (part number 776160-01) are listed as follows.

Kit Component	Part Number
NB-AO-6 board	180520-01
NB-AO-6 User Manual	320098-01
NI-DAQ software for Macintosh, with manual	776181-01
NI-DAQ for Macintosh Software Reference Manual	320103-01

If your kit is missing any of the components, contact National Instruments.

Your NB-AO-6 is shipped with the NI-DAQ software for Macintosh. NI-DAQ has a library of functions that can be called from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer, SCXI, RTSI, and self-calibration. NI-DAQ maintains a consistent software interface among its different versions so you can switch between platforms with minimal modifications to your code. NI-DAQ comes with language interfaces for MPW C, THINK C, Pascal, and Microsoft QuickBASIC. Any language that uses Device Manager Toolbox calls can access NI-DAQ.

Optional Software

This manual contains complete instructions for directly programming the NB-AO-6. Normally, however, you should not need to read the low-level programming details in the user manual because the NI-DAQ software package for controlling the NB-AO-6 is included with the board. Using NI-DAQ is quicker and easier than and as flexible as using the low-level programming described in Chapter 4, *Programming*.

The NB-AO-6 can also be used with LabVIEW 2 (part number 776141-01), a software system that features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW 2 Data Acquisition VI Library, a series of VIs for using LabVIEW 2 with the Lab-LC and other National Instruments boards, is included with LabVIEW 2. The LabVIEW 2 Data Acquisition VI Library is functionally equivalent to the NI-DAQ for Macintosh software.

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Optional Equipment

Equipment	Part Number
NB-DMA2800 board	776305-01
NB-DMA-8-G board	776161-01
CB-50 I/O connector block–0.5-m cable	776164-01
CB-50 I/O connector block–1.0-m cable	776164-02
RTSI bus cable for	
2 boards	776188-02
3 boards	776188-03
4 boards	776188-04
5 boards	776188-05

Unpacking

Your NB-AO-6 is shipped in an antistatic package to prevent electrostatic damage to the board. Several components on the board can be damaged by electrostatic discharge. To avoid such damage in handling the board, take the following precautions:

- Touch the antistatic package to a metal part of your computer before removing the board from the package.
- Remove the board from the antistatic package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.

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Chapter 2
Configuration and Installation

This chapter describes the jumper configuration, installation of the NB-AO-6 in the Macintosh, signal connections to the NB-AO-6, timing, field wiring, and cabling.

Board Configuration

The NB-AO-6 contains 24 jumpers so that you can change the configuration of each analog output channel on the board. The jumpers are shown in the parts locator diagram in Figure 2-1.

Jumpers

Internal/External Reference

Each analog output channel of the NB-AO-6 can be configured to use either an internal or an external reference. The reference voltage determines the range of values that the output can assume. The internal reference is fixed at +10 V. Any value up to ±20 V can be used as an external reference, but the converter channels cannot output voltages much beyond ±10 V. A 2.5 VDC signal is available on the output connector for use as an external reference if needed. An AC signal can be used as a reference, although 12-bit accuracy is not maintained at frequencies above a few hundred hertz.

Bipolar/Unipolar Output

When a channel of the NB-AO-6 is configured in bipolar mode with reference voltage V_{ref}, its output can vary from $-V_{ref}$ to +2,047/2,048 V_{ref}. In unipolar mode, it can vary from 0 to +4,095/4,096 V_{ref}.

Offset Binary/Two's Complement

If a D/A channel is configured for bipolar output, one of two data coding methods must be chosen. In offset binary mode, a digital value of zero corresponds to a full scale negative output, a digital value of 2,048 corresponds to zero analog output, and a digital value of 4,095 corresponds to a full scale positive output. In two's complement mode, a digital value of -2,048 corresponds to a full scale negative output, a digital value of zero corresponds to zero analog output, and a digital value of 2,047 corresponds to a full scale positive output. If a D/A channel is configured for unipolar output, put the jumper in the offset binary position.

Local/Remote Sensing

When this jumper is in the local position for a given channel, the output voltage is sensed on the NB-AO-6 itself; any voltage drops in the off-board cabling is not compensated for. When it is in the remote position, the output voltage is sensed at the sense input for that channel. If the sense input is connected to the load with less than approximately 2 Ω resistance, line-loss errors are compensated for, even if the load impedance is low (for example, 600 Ω).

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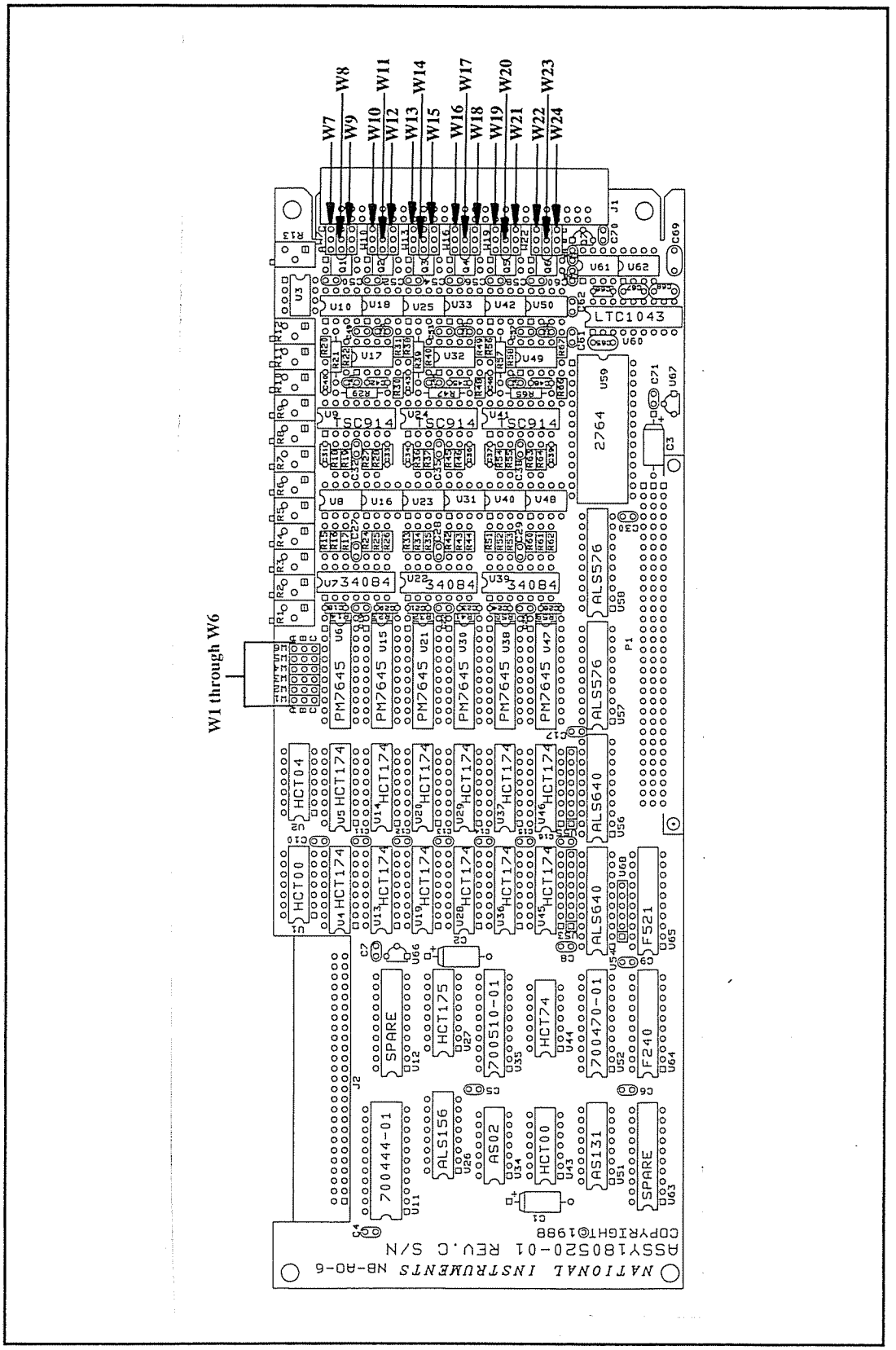


Figure 2-1. NB-AO-6 Parts Locator Diagram

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Table 2-1 lists the jumpers on the board.

Table 2-1. Jumper Settings

Channel	Input Coding	Reference Select	Polarity	Sense Mode
0	W6	W7	W8	W9
1	W5	W10	W11	W12
2	W4	W13	W14	W15
3	W3	W16	W17	W19
4	W2	W19	W20	W21
5	W1	W22	W23	W24
	two's complement: A-B* offset binary: B-C	internal: A-B* external: B-C	unipolar: A-B bipolar: B-C*	remote: A-B local: B-C*
* factory configuration				

Each jumper has three terminals: A, B, and C. In Figure 2-2, Terminal B connects to either Terminal A or to Terminal C, depending on the desired configuration shown in Table 2-1.

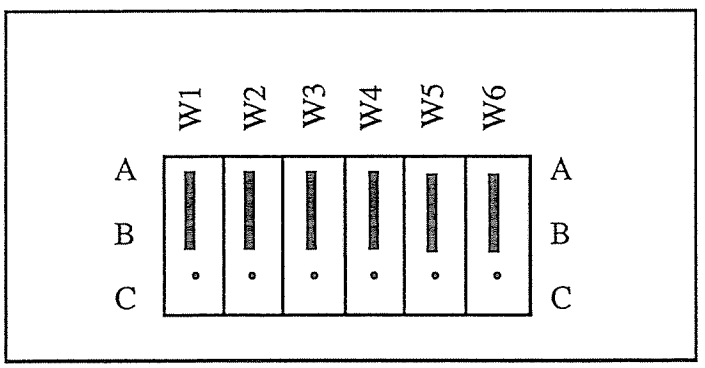


Figure 2-2. Default Settings for Jumpers W1 through W6

Figure 2-3 shows the default settings for jumpers W7, W8, and W9.

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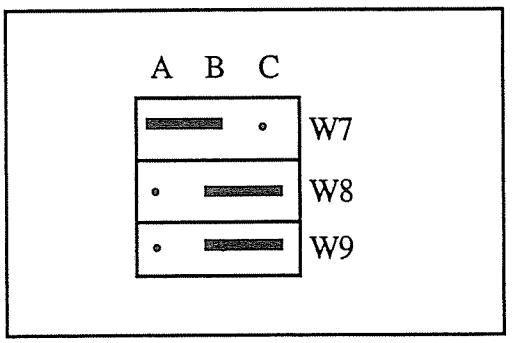


Figure 2-3. Default Settings for Jumpers W7, W8, and W9

Figure 2-4 shows the default settings for jumpers W10, W11, and W12.

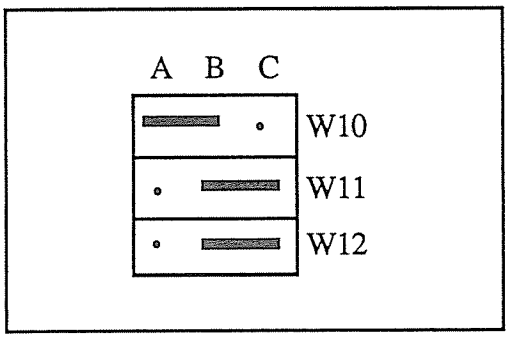


Figure 2-4. Default Settings for Jumpers W10, W11, and W12

Figure 2-5 shows the default settings for jumpers W13, W14, and W15.

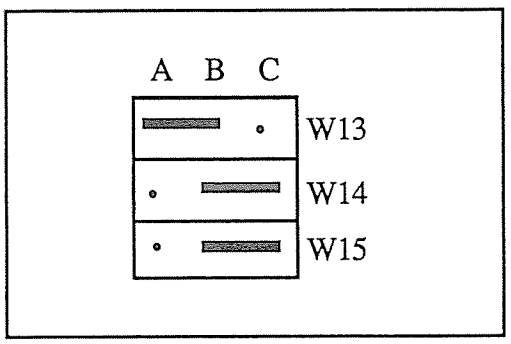


Figure 2-5. Default Settings for Jumpers W13, W14, and W15

Figure 2-6 shows the default settings for jumpers W16, W17, and W18.

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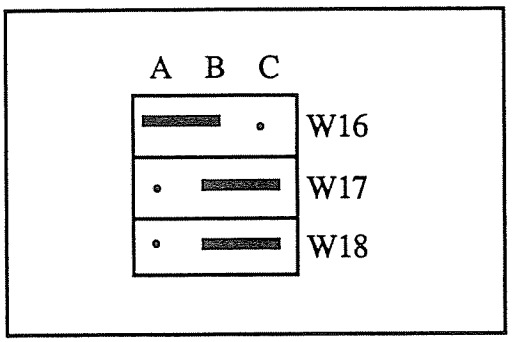


Figure 2-6. Default Settings for Jumpers W16, W17, and W18

Figure 2-7 shows the default settings for jumpers W19, W20, and W21.

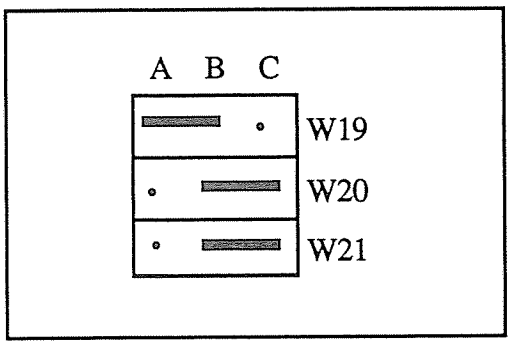


Figure 2-7. Default Settings for Jumpers W19, W20, and W21

Figure 2-8 shows the default settings for jumpers W22, W23, and W24.

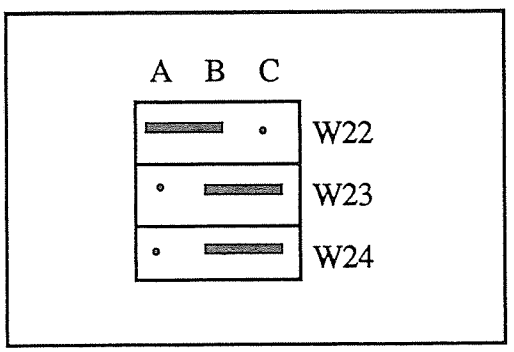


Figure 2-8. Default Settings for Jumpers W22, W23, and W24

Installation

Within the manual shipped with your Macintosh computer, read the instructions for installing the video card in the main unit. These instructions can be used as a universal board installation guide.

Read the entire installation procedure before installing the NB-A0-6 into the Macintosh.

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The lids of Quadra computers have board-holding clips that are attached to the lids. These clips are removable on a per slot basis. These clips are designed to hold the board in place, since the Quadra series are all towers-style computers.

After you install the NB-AO-6 in a NuBus slot, the board does not allow the lid to close easily. The clip rubs up against the blue trimpots of the plug-in board. If you install the board in slot *n*, please remove the clip in slot *n*.

Signal Connections

This section describes input and output signal connections to the NB-AO-6 via the NB-AO-6 I/O connector. This section also provides specifications and connection instructions for the signals provided on the NB-AO-6 I/O connector.

Warning: Connections that exceed any of the maximum ratings of input or output signals on the NB-AO-6 can result in damage to the NB-AO-6 board and to the Macintosh. This includes connecting any power signals to ground and vice versa. National Instruments is not liable for any damages resulting from any such signal connections.

Output Connector

The pin assignments for the 50-pin output connector are shown in Figure 2-3. These connections are easily made available on the external connector block, the CB-50. The CB-50, which can be rail-mounted, connects to the NB-AO-6 via a 50-wire ribbon cable and is available from National Instruments.

The pinout for the NB-AO-6 I/O connector is shown in Figure 2-9.

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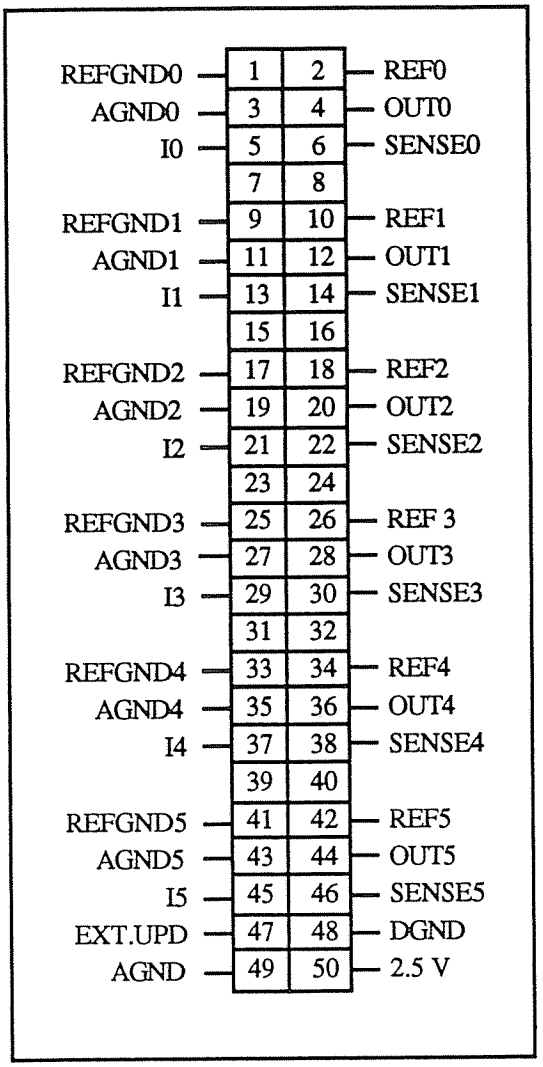


Figure 2-9. NB-AO-6 I/O Connector

Pins 4, 12, 20, 28, 36, and 44 (OUT0 - OUT5) are the voltage output signal pins. Pins 3, 11, 19, 27, 35, and 43 (AGND0 - AGND5) are their corresponding ground pins. Voltage outputs should be measured between a voltage output pin and its corresponding ground pin.

Pins 6, 14, 22, 30, 38, and 46 (SENSE0 - SENSE5) are the remote sense input pins. Each channel's sense pin does nothing unless that channel is configured for remote sensing. See *Local/Remote Sensing* earlier in this chapter, and Chapter 3, *Theory of Operation*, for more information on remote sensing.

Pins 2, 10, 18, 26, 34, and 42 (REF0 - REF5) are the external reference input pins. Pins 1, 9, 17, 25, 33, and 41 (REFGND0 - REFGND5) are their corresponding ground pins. Reference inputs should be applied between a reference input pin and its corresponding ground pin. A channel must be properly configured in order to use its external reference. See *Internal/External Reference* earlier in this chapter, and Chapter 3, *Theory of Operation*, for more information on using external references.

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Pins 5, 13, 21, 29, 37, and 45 (I0 - I5) are the current output pins. The external voltage source required to power the current loops should share a ground with the NB-AO-6. Any of the signal grounds work, but the system digital ground, pin 48, is recommended. Using this ground reduces the amount of noise coupled into the voltage outputs from the power supply.

Pin 50 is the 2.5 V reference output pin. Pin 49 is its corresponding ground pin. The 2.5 VDC signal available between pins 49 and 50 is exactly one-fourth of the internal 10 V reference, and can be used to calibrate the 10 V reference. For information concerning calibration procedures, refer to Chapter 5, *Calibration Procedures*.

Pin 47 is the external update pin. It is internally pulled high (to +5 V) with a 10 kΩ resistor. Switching this pin between 5 V and ground (for example, with an SPST switch to digital ground, pin 48) can trigger an UPDATE pulse on the NB-AO-6. See Chapter 3, *Theory of Operation*, and Chapter 4, *Programming*, for more information on generating UPDATE pulses and the EXT.UPD signal.

Signal connections for voltage and current output applications are given in Chapter 3, *Theory of Operation*.

Timing Diagrams

Both the EXT.UPD signal on the back panel connector and pin A0 of the RTSI switch, which connects to the RTSI bus, can trigger an UPDATE pulse on the NB-AO-6. As these two signals are internally ANDed together, their timing requirements are identical. In Figure 2-10, the pin A0 is held high (the RTSI switch provides pullup resistors for unprogrammed outputs), and the EXT.UPD signal is used to generate UPDATE pulses. If bit 3 of the Configuration Register is cleared, the UPDATE circuitry is falling-edge sensitive.

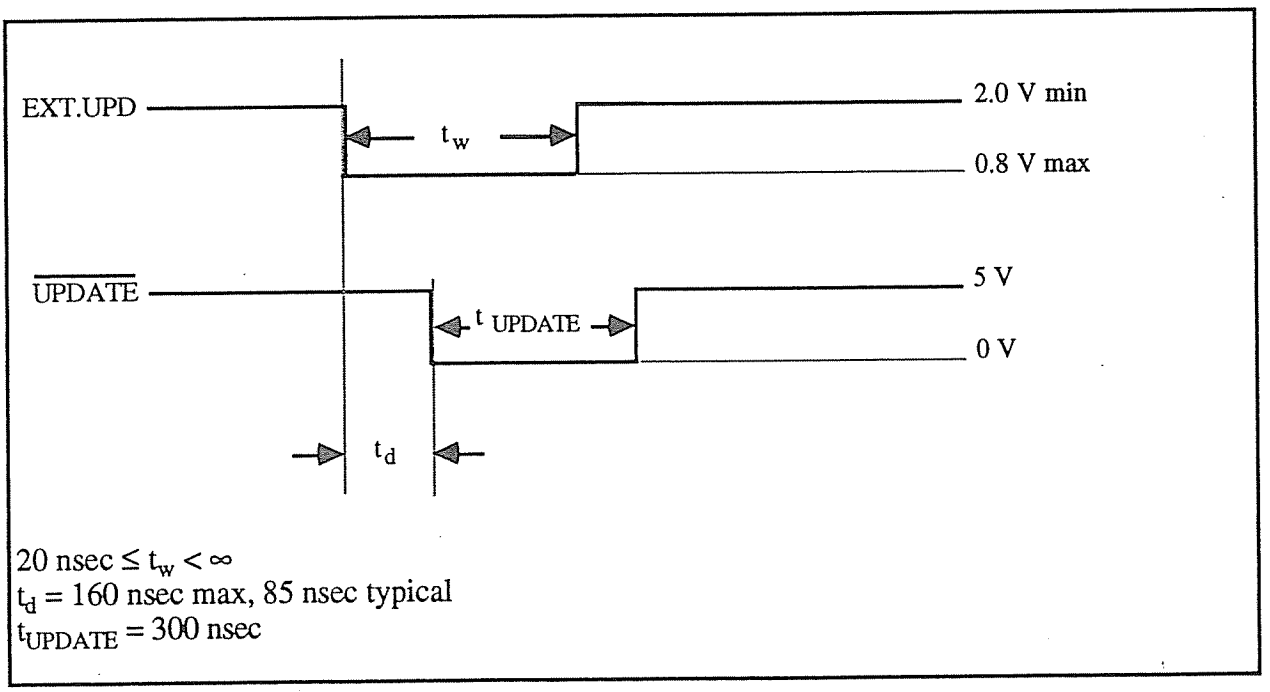


Figure 2-10. Falling-Edge Sensitive Timing

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If bit 3 of the Configuration Register is set, the UPDATE circuitry is rising-edge sensitive.

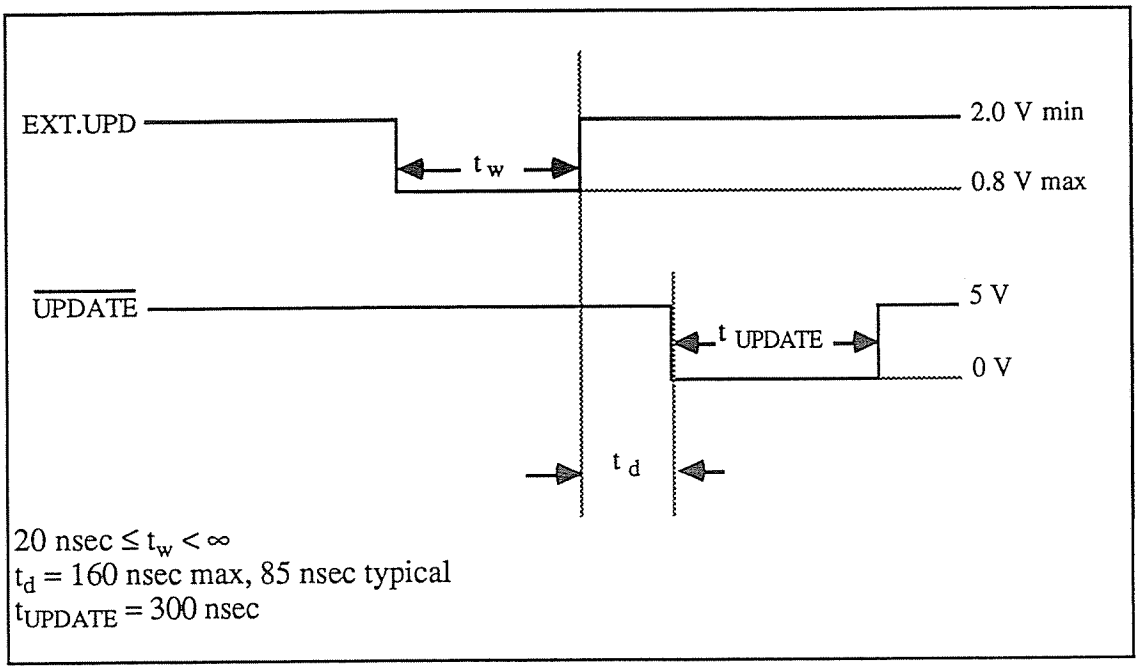


Figure 2-11. Rising-Edge Sensitive Timing

If DMA is enabled, the DMA request signal is generated directly from the UPDATE signal on the RTSI bus shown in Figure 2-12.

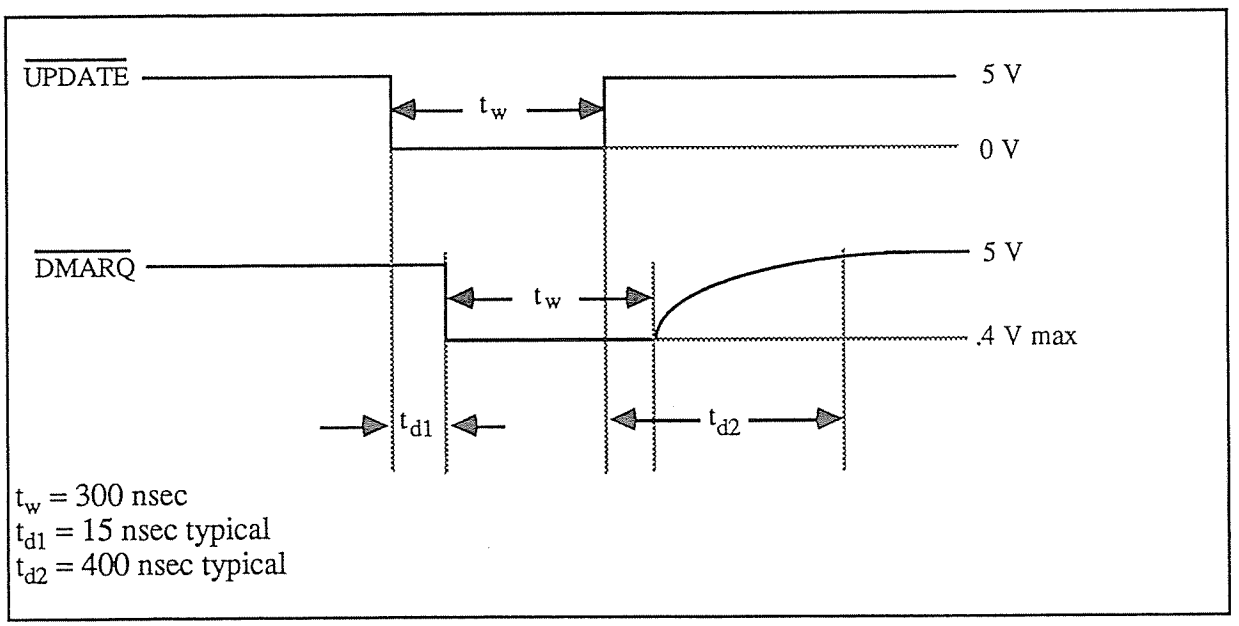


Figure 2-12. DMA Request Generation Timing

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Field Wiring and Cabling

This section discusses field wiring and cabling considerations for the NB-AO-6.

Field Wiring Considerations

Accuracy of signals generated by the NB-AO-6 can be seriously affected by environmental noise when signal wires are run to and from the NB-AO-6.

Noise pickup and crosstalk can be minimized and signal accuracy optimized if the following recommendations for analog signal connections are followed.

- Use individually shielded, twisted-pair connections for voltage output signals. In such cases, the voltage output and its corresponding analog ground signal wire are twisted together and the shield is connected to the analog ground at the NB-AO-6. The other end of the shield is left disconnected.
- If remote sensing is being used to help compensate for line loss, the sense signal wire should be twisted together with the voltage output and analog ground signals, and the shield should be connected to the analog ground at the NB-AO-6.
- Reference inputs should also be connected via shielded twisted-pair connection. The shield should be grounded at the signal source.
- Current outputs are relatively immune to line loss and noise pickup and should be used for signal transmission over long distances.
- All NB-AO-6 signal lines should be physically separated from high-current or high-voltage lines. These lines are capable of inducing currents into the NB-AO-6 signal lines if they are run in parallel paths at a close distance. Reduce the magnetic coupling by separating the lines by a reasonable distance if they run in parallel, or by running the lines at right angles to each other.
- Do not run NB-AO-6 signal lines through conduits that also contain power lines.
- Protect NB-AO-6 signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running the NB-AO-6 signal lines through special metal conduits if it is necessary to pass them through these areas.

Cabling Considerations

National Instruments provides a cable termination accessory, the CB-50, for use with the NB-AO-6. The CB-50 includes a terminated 50-conductor flat ribbon cable and a connector block. Signal input and output leads can be attached to screw terminals on the connector block and thereby connected to the NB-AO-6 I/O connector.

The CB-50 is useful for initially prototyping an application, or in situations where NB-AO-6 interconnections are frequently changed. When a final field wiring scheme has been developed, however, you may want to develop your own cable. This section provides information and guidelines for the design of such a cable.

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The NB-AO-6 I/O connector is a 50-pin male ribbon cable header connector. The manufacturer part numbers used by National Instruments for this connector are as follows:

Electronic Products Division/3M	part number 3596-5002
T&B/Ansley Corporation	part number 609-5007

The mating connector for the NB-AO-6 is a polarized 50-position, ribbon socket connector with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside-down connection to the NB-AO-6. Recommended manufacturer part numbers for this mating connector are as follows:

Electronic Products Division/3M	part number 3425-7650
T&B/Ansley Corporation	part number 609-5041CE

The following are standard ribbon cables (50 conductor, 28 AWG, stranded) that can be used with these connectors:

Electronic Products Division/3M	part number 3365/50
T&B/Ansley Corporation	part number 171-50

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Chapter 3
Theory of Operation

This chapter contains a functional overview of the NB-AO-6 and explains the operation of each functional unit making up the NB-AO-6.

A block diagram of the NB-AO-6, shown in Figure 3-1, shows the major functional blocks of the circuit.

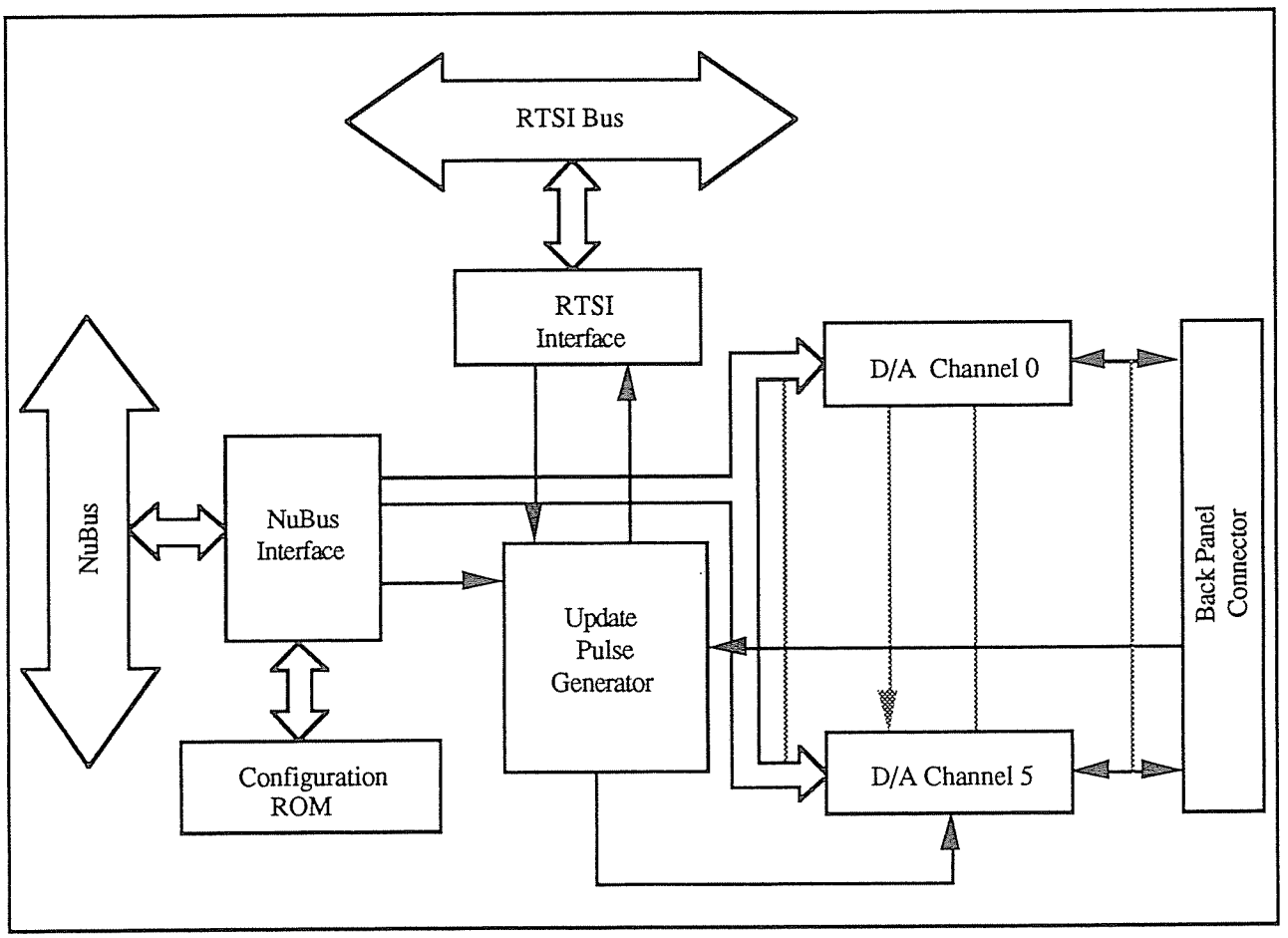


Figure 3-1. NB-AO-6 Block Diagram

The NuBus interface receives and buffers the signals sent between the board and the Macintosh. The RTSI interface is implemented with a software programmable crossbar switch. This switch allows any of the seven RTSI trigger lines to connect to any of the seven points on the board. The RTSI switch, on the NB-AO-6, is connected to trigger and receive UPDATE pulses (for a description of update pulses, refer to *Double Buffering* later in this chapter). The Configuration ROM contains information about the NB-AO-6 that is used by the Macintosh and the software to identify the board. Each of the six DAC channels is connected to the back panel connector.

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Each DAC channel, shown in Figure 3-2, consists of a 12-bit register, a 12-bit buffered D/A, some amplification, and a voltage-to-current converter. The presence of the register in front of the latched DAC in each channel implements double buffering. You can now simultaneously update the outputs of all six D/A channels. Double buffering also makes the precise output timing required for waveform generation possible.

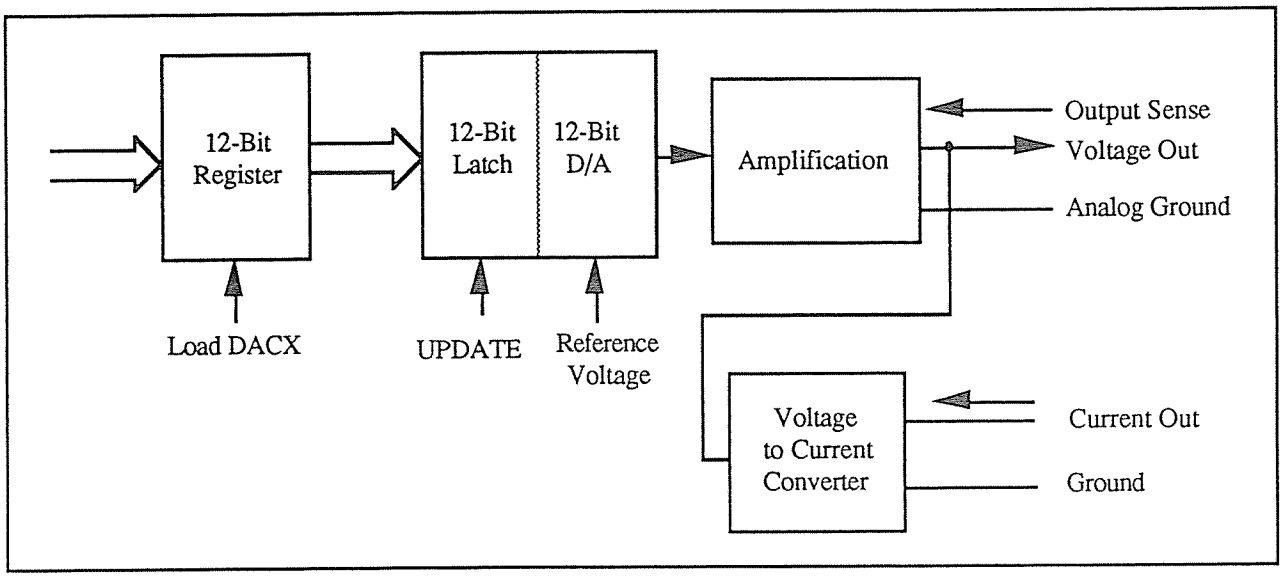


Figure 3-2. Block Diagram of D/A Channel X

Double Buffering

Double buffering is a standard feature of the NB-AO-6. With double buffering, two things must happen for an analog output change to occur:

1. New data that corresponds to the desired analog output must be written to the onboard register that buffers the desired output channel.

2. The D/A of the desired channel must be loaded with the contents of its register. This occurs when the D/A receives an UPDATE pulse. The UPDATE signal is common to all the D/A channels, but only those channels that have had new data loaded into their registers exhibit output changes.

The UPDATE pulse is derived from one of three sources: the host computer, the RTSI bus, or an external signal.

- *Host Computer* - If address bit 8 is set during a write operation to one of the D/A registers, an UPDATE pulse is generated with timing such that the data written to the register is immediately loaded into its D/A. In this case, double buffering is transparent. You need only to write to the correct address. Actually, any write to the correct slot with address bit 8 set and bits 17, 18, and 19 cleared generates an UPDATE pulse. Therefore, you can update the D/As regardless of how many have been provided with new data.

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- *RTSI Bus* - A signal on pin A0 of the trigger bus crossbar switch can cause an UPDATE pulse to be generated. This is an edge-triggered signal and can be programmed as either rising-edge or falling-edge sensitive. For this trigger to function, however, the external update pin on the output connector must be either disconnected or pulled high (2.4 to 5 V).

- *External Signal* - A signal on pin 48 of the output connector behaves just like the RTSI bus update trigger (in fact, the two signals are ANDed together). It is sensitive to the same edge, and the RTSI signal must either be high (2.4 to 5 V) or disabled by software control for this trigger to function. If a DMA board is included in the system, this signal makes it possible to generate waveforms that are synchronized to an external clock.

No matter how it is generated, the UPDATE pulse causes *all* of the D/As to be loaded with the data in their registers. To change the output of only one channel, make sure that the channel is the only one with new data in its register when the next update pulse is generated.

Reference Inputs

The reference voltage for each DAC is independently selected to be either the onboard 10 V reference or an external reference. A 2.5 V signal is available on the output connector to be used as external reference if desired. The external reference is applied at the reference input for each channel.

The reference inputs can be used to set the output span of each D/A. The D/As remain monotonic for reference voltages between -10 and -1 V and between +1 and +10 V; that is, an increase in the digital input code results in an increase (decrease for negative references) in the analog output voltage. Setting the appropriate jumpers on the board to select the external reference option and to select unipolar or bipolar output is necessary. Refer to Chapter 2, *Configuration and Installation,* for more information on jumper options.

The external reference can be an AC signal as well. In this case, the AC signal should be limited to ±10 V to avoid clipping on the output for large digital input codes. The D/A acts like a programmable attenuator and maintains its linearity for input frequencies up to several hundred hertz. There can be a very small output offset variation with digital input code (in the microvolts), but the gain of the D/A channel is monotonic for all input signal magnitudes. At low levels, however, noise can become a problem. A 12-bit linear D/A is capable of approximately 72 dB of attenuation control.

If a D/A channel is being used to generate a waveform, the reference input can be used to amplitude modulate that waveform. For example, a 200 Hz sinusoidal reference could modulate a 100 kHz square wave. The reference could also be generated on another D/A channel, in which case the two signals would be synchronous. This method can be used to easily generate waveforms that are the products of other waveforms, such as the product of a triangle wave and a sine wave, or a periodic parabola, which is the product of two ramps. Multiplying waveforms in this way has the effect of increasing the apparent resolution of the D/As, especially near 0 V output.

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Voltage Output Connections

The NB-A0-6 voltage outputs are capable of driving ±10 V into loads of 2 kΩ or greater, and can drive heavier loads with reduced output voltage swing. There are three standard input coding options available: unipolar binary, bipolar offset binary, and bipolar two's complement. These modes are jumper selectable. Refer to Chapter 2, *Configuration and Installation,* for more information on jumper settings.

In unipolar binary mode, the output voltage is defined by the following equation:

$$Vout = Vref * \frac{code}{4,096} \text{ where } 0 \leq code \leq 4,095$$

In offset binary mode, the output voltage is defined by the following equation:

$$Vout = Vref * \frac{code - 2,048}{2,048} \text{ where } 0 \leq code \leq 4,095$$

In two's complement mode, the output voltage is defined by the following equation:

$$Vout = Vref * \frac{code}{2,048} \text{ where } -2,048 \leq code \leq 2,047$$

Line-powered loads, such as some oscilloscopes and audio equipment, are often internally grounded, as is the NB-AO-6 through the Macintosh NuBus. Connecting the NB-AO-6 to such a load forms a ground loop and heavy currents (several milliamperes) can flow through the ground connections. Because these connections have nonzero resistance and inductance, the currents result in noise and offset errors at the load. Using a separate ground connection for each output helps keep these errors from affecting other channels. Connecting the chassis together with a separate low resistance wire also helps; current is diverted away from the signal ground paths. However, the only sure way to eliminate the errors is to eliminate the ground loop by using only floating loads (for example, battery powered or differential).

Remote Sensing

When the sense jumper of a D/A channel is in the remote position, the feedback loop of the output operational amplifier is opened and made available at the sense input of that channel. This input has an impedance of about 20 kΩ (bipolar mode) or 10 kΩ (unipolar mode). When driving low impedance loads (less than about 10 kΩ) a fairly long distance from the board (for example, the resistance of the connecting wire is as great as about 2 Ω), using the remote-sensing option to preserve gain accuracy is recommended. In this case, the voltage output terminal and the voltage sense terminal are connected together at the load as shown in Figure 3-3.

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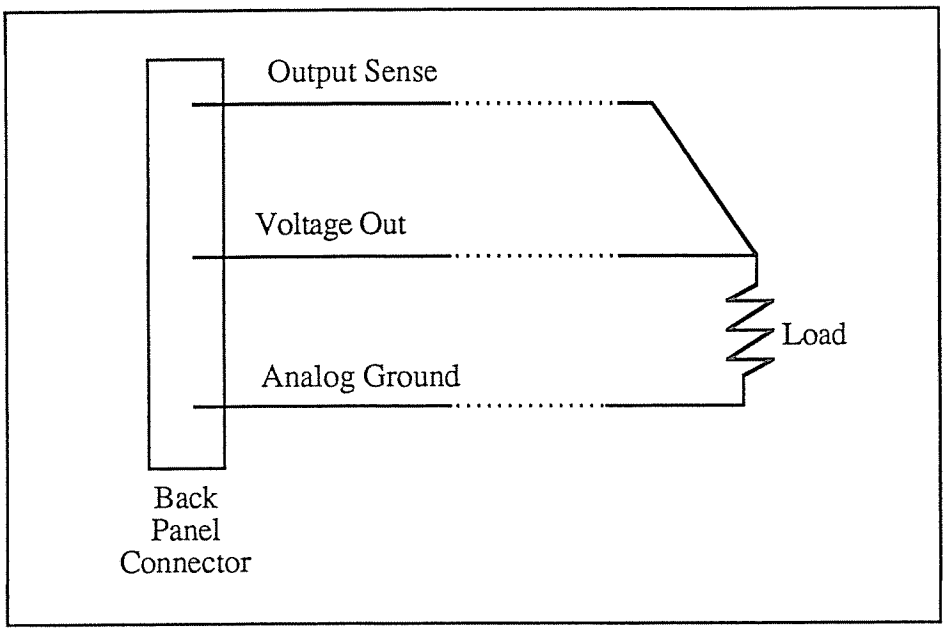


Figure 3-3. Remote-Sense Connections

Assuming zero ground wire resistance (use heavy wire for ground connections), if the resistance of the sense wire is less than 2.4 Ω (bipolar mode) or 1.2 Ω (unipolar mode), the output error will be less than 1/2 LSB for a properly calibrated board. (The resistance of 100 ft of 22 AWG stranded copper wire is about 1.5 Ω.) The actual equation for the voltage at the load is as follows:

$$V_L = V_O * \frac{(1 + R_{sense}/R_f)}{(1 + R_{gnd}/R_L)}$$

where

- V_L is the voltage appearing across the load
- V_O is the desired load voltage (the no-load local-sense output)
- R_{sense} is the resistance of the sense wire
- R_f is the input impedance of the sense terminal (10 or 20 kΩ)
- R_{gnd} is the resistance of the ground wire
- R_L is the load resistance

This equation shows that for excessive sense lead resistances, the voltage at the load will actually be too large. Keep in mind that to compensate for line losses in remote-sense mode, the output amplifier must exceed its normal output voltage swing. This means that the output swing available at the load is slightly reduced. This could be a problem only with large reference voltages and

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very low load impedances or very high resistance connections. The equation for the load voltage when using local-sense mode is as follows:

$$V_L = \frac{R_L}{(R_{force} + R_{gnd} + R_L)} * V_O$$

where

- V_L is the voltage appearing across the load
- V_O is the desired load voltage (the no-load local-sense output)
- R_L is the load resistance
- R_{gnd} is the resistance of the ground wire
- R_{force} is the resistance of the output wire

This equation, in conjunction with the previous equation, shows that for $R_{force} = R_{sense}$ and $R_{gnd} = 0$, the ratio of the remote-sense gain error to the local-sense gain error is simply R_L/R_f. Therefore, using remote-sensing does not gain anything unless R_L is significantly smaller than R_f.

Output line-load losses and local/remote sensing affect only gain error and have no effect on system offset. Transient response is also affected, with the possibility of instability with very long output leads in the remote sense configuration.

Driving High-Current Loads

Another application for which the remote-sense configuration is useful is when the NB-AO-6 is used in conjunction with external power buffers. In this case, remote sensing can be used to include the buffers inside the feedback loops of the NB-AO-6 output amplifiers, thereby eliminating errors resulting from offset, gain, and drift in the buffers. Such a connection is shown in Figure 3-4.

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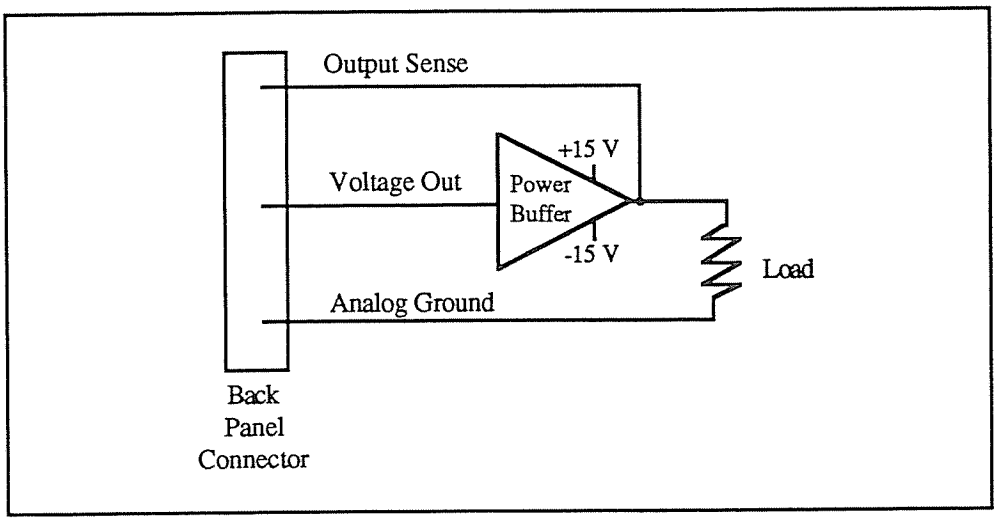


Figure 3-4. Driving a Heavy Load with an External Buffer

The buffer should be powered by external supplies because the Macintosh NuBus power supplies cannot supply enough current to drive heavy loads. The buffer should have voltage gain of about unity, and enough output current capability to drive the load. Too low a voltage gain or too great an offset voltage might require the NB-AO-6 output to swing beyond its limit to compensate for these errors.

Instability or oscillation can occur if the buffer is slower than the NB-AO-6 output because propagation delay through the buffer results in excessive phase shift in the feedback signal at high frequencies. Careful layout and power supply bypassing is important to prevent self-oscillation of high-speed buffers. Either discrete or integrated buffers can be used with this configuration.

If only a low-speed buffer is available, you may need to stabilize the system by providing a separate high-frequency feedback path for the NB-AO-6 output amplifier. This setup, with example component values, is shown in Figure 3-5.

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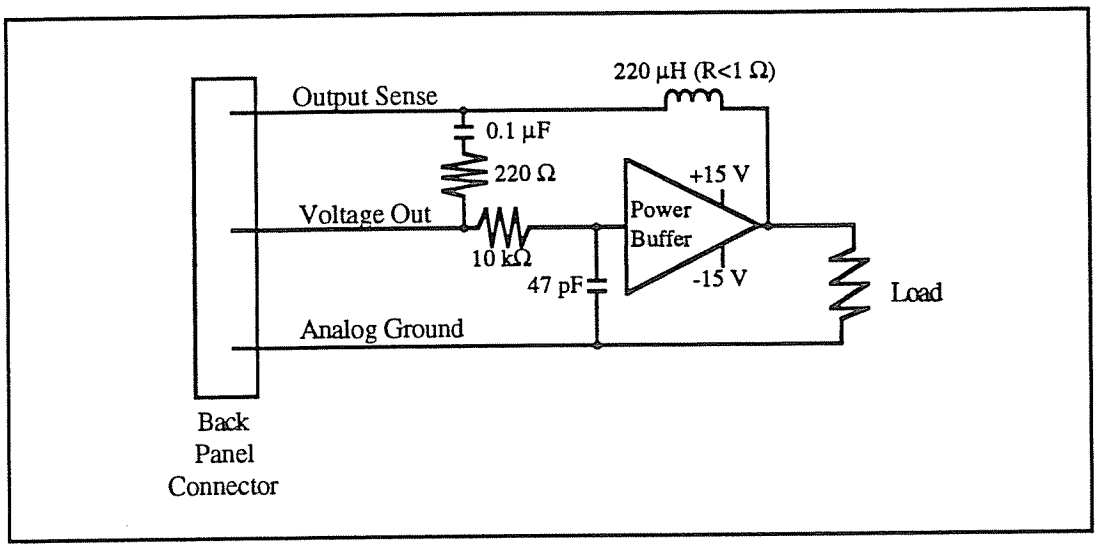


Figure 3-5. Using a Slow-Power Buffer

This configuration places the buffer inside the feedback loop of the NB-AO-6 at low frequencies and outside the loop at high frequencies, therefore providing accurate low-frequency buffering without causing high-frequency instability.

Current Loop Connections

Each channel of the NB-AO-6 includes a 4 to 20 mA current transmitter for use with industry standard 4 to 20 mA current loops. Each transmitter consists of an N-channel power MOSFET current sink to ground. The output sink current is related to the output voltage by the following equation:

$$I_{sink} = \frac{(V_{out} + 2.5)}{625}$$

where I_{sink} is the output current in amperes, and V_{out} is the output voltage in volts. This equation holds as long as the result is non-negative. The NB-AO-6 current outputs do not *source* current. For example, if the reference voltage is +10 V and the board is configured for unipolar output, an input digital code of zero yields an output voltage of 0 V and an output current as shown in the following equation:

$$\frac{(0 + 2.5)}{625\ A} = 4\ mA$$

With the same configuration, an input code of 4,095 yields an output voltage of 9.9976 V and an output current that is shown in the following equation:

$$\frac{(9.9976 + 2.5)}{625\ A} = 19.996\ mA$$

The transfer function relating output current to output voltage is graphed in Figure 3-6.

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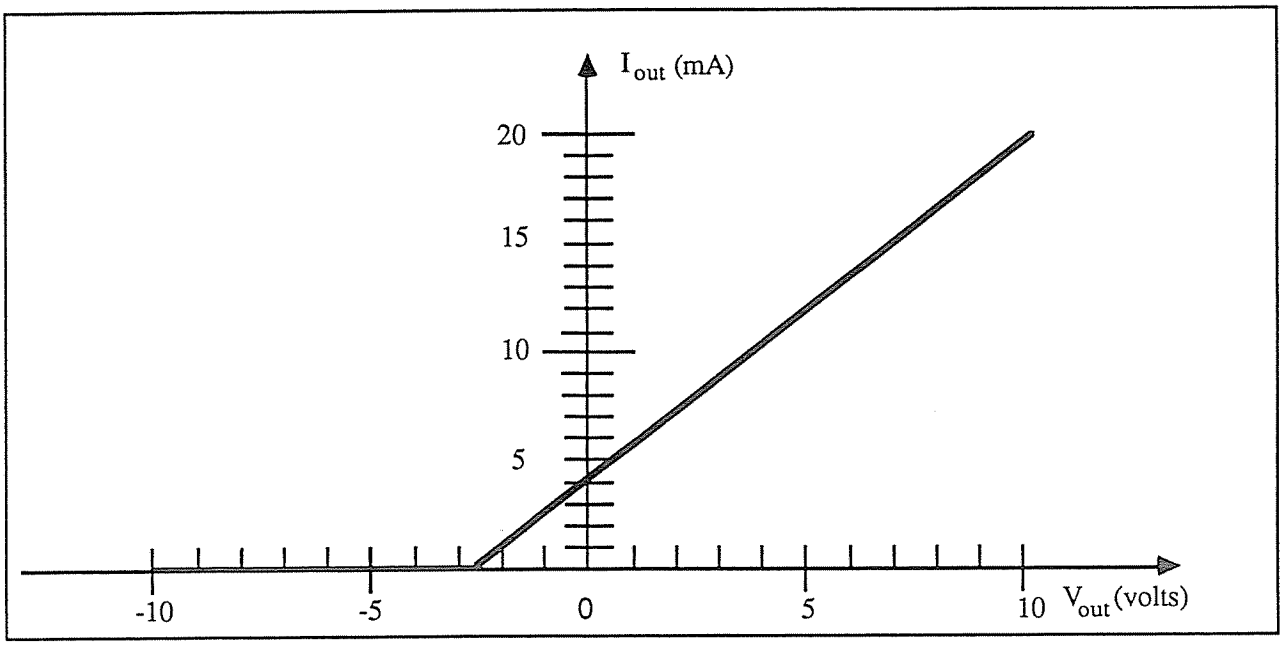


Figure 3-6. Output Sink Current Versus Output Voltage

Maintaining the voltage at the output within the specified range of 7 to 40 V is important. If the voltage is too low, the NB-AO-6 cannot sink the full 20 mA. If the voltage is too high, overheating can occur and the board can be damaged. Figure 3-7 shows a possible current loop connection.

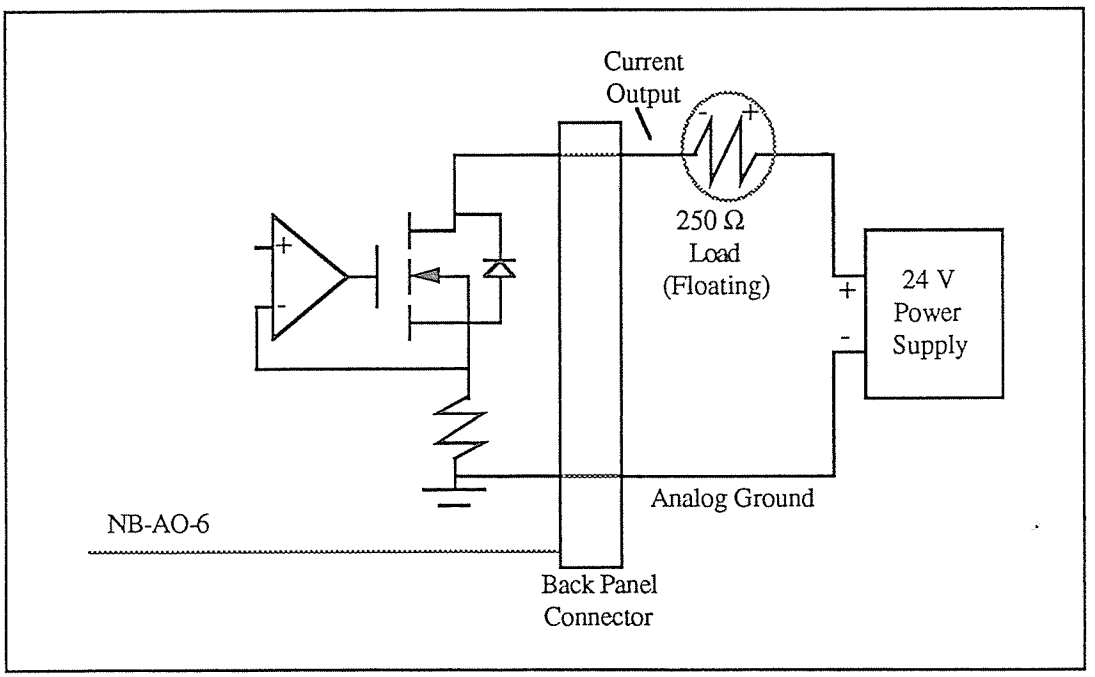


Figure 3-7. Possible Current Loop Connection

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The combination of power supply voltage and load impedance used in Figure 3-7 keeps the voltage at the connector between 19 V (20 mA) and 23 V (4 mA). The voltage at the connector is always as follows:

$$V_{conn} = V_{ext} - I_{out} * R_L$$

where

- V_{conn} is the voltage at the connector in volts
- V_{ext} is the external power supply voltage in volts
- I_{out} is the output sink current in mA
- R_L is the resistance of the load in kΩ

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Chapter 4
Programming

This chapter describes in detail the address and function of each of the NB-AO-6 registers. This chapter also includes important information about programming the NB-AO-6 for DMA and timer operations.

Register Access

The Macintosh uses memory mapping to access boards in the system. The following sections discuss accessing the various registers on the NB-AO-6.

Slot Address Space

Each slot in the Macintosh NuBus is allocated a block of Macintosh memory addresses known as the *slot address space*. All I/O boards plugged into Macintosh NuBus slots are therefore memory mapped. When an I/O board is plugged into a given slot, its registers can be accessed within that slot address space. The block of memory addresses allocated to each slot depends on the slot number. The slots, labeled 9 through E, are next to the slot connectors inside the Macintosh. Table 4-1 shows the slot address space for each slot.

Table 4-1. Macintosh NuBus Slot Addresses

Slot Number	Starting Address (hex)	Ending Address (hex)
9	90 0000	9F FFFF
A	A0 0000	AF FFFF
B	B0 0000	BF FFFF
C	C0 0000	CF FFFF
D	D0 0000	DF FFFF
E	E0 0000	EF FFFF

Register Map

The register map for the NB-AO-6 is shown in Table 4-2. This table gives the register name, the register address offset from the slot base address, the size of the register in bits, and the register type (read only, write only, or read and write).

Each register address is the offset address from the slot starting address. To calculate the absolute address of the register, add the slot starting address given in Table 4-1 to the register offset given in Table 4-2. For example, if the NB-AO-6 is plugged into slot B, D/A Register 3 is at address B0 0000 + 20, that is, address B0 0020 (hex).

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Table 4-2. NB-AO-6 Register Map

Register Name	Offset Address (hex)	Size	Type
Analog Output Register Group:			
D/A Register 0	4	16-bit	Write-only
D/A Register 1	8	16-bit	Write-only
D/A Register 2	10	16-bit	Write-only
D/A Register 3	20	16-bit	Write-only
D/A Register 4	40	16-bit	Write-only
D/A Register 5	80	16-bit	Write-only
Update Register	100	16-bit	Write-only
Configuration Register	A0000	8-bit	Write-only
RTSI Switch Register Group			
RTSI Shift Register	C0000	8-bit	Write-only
RTSI Strobe Register	C0004	8-bit	Write-only

Register Sizes

The Macintosh NuBus accepts three different memory word sizes for memory read and write operations: byte (8-bit), half-word (16-bit), and word (32-bit). Table 4-2 shows the word sizes of the NB-AO-6 registers.

Register Description

Table 4-2 divides the NB-AO-6 registers into three different register groups. A bit description of each of the registers making up these groups is given later in this chapter.

The Analog Output Register Group consists of seven registers that contain the data to be loaded into DACs upon receipt of an UPDATE command. The Configuration Register contains DMA channel selection bits and a bit related to hardware triggering of UPDATE pulses. With the RTSI Switch Register Group, the NB-AO-6 RTSI switch can be programmed for the routing of signals on the RTSI bus trigger lines to and from the NB-AO-6 signal lines.

Register Description Format

The remainder of this section discusses each of the NB-AO-6 registers in the order shown in Table 4-2. Each register group is introduced, followed by a detailed bit description of each register. Individual register descriptions give the address–*always* in hexadecimal, type, data size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the most significant bit (bit 31 for a 32-bit register, bit 15 for a 16-bit register, or bit 7 for an 8-bit register) shown on the left, and the least significant bit (bit 0) shown on the right. A square is used to represent each bit. Each bit is labeled with a name inside its square. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic).

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In many of the registers, several bits are labeled with an X indicating *don't care* bits. When a register is read, these bits can appear set or cleared but should be ignored because they have no significance. When a register is written to, setting or clearing these bit locations has no effect the NB-AO-6 hardware.

The bit map field for some write only addresses state *not applicable, no bits used.* Writing to these addresses generates a strobe in the NB-AO-6. These strobes are used to cause an onboard event to occur.

Analog Output Register Group

The seven registers making up the Analog Output Register Group contain the data that is loaded into DACs upon receipt of an UPDATE command. Base offset (relative to the base address of the board, which depends on its slot) is zero. These addresses are not decoded, so each channel corresponds to an address bit. Channel X is written to only when a word write is performed with address bit (X+2) set. Address bits 0 and 1 should be cleared, and address bits 9 through 16 are ignored. Address bit 8 is the update bit. If this bit is set during a write to a D/A channel, the output responds immediately. Otherwise, the output does not respond until an UPDATE pulse is generated (refer to Chapter 3, *Theory of Operation*). For example, to write data to Channel 3 to be output immediately, the correct offset is 120 hex (20 + 100). To write data to Channels 0 and 1 to be output later, the correct offset is C hex (4 + 8). D/A channels are numbered zero through five. These are write only registers.

The D/A Registers are 12 bits wide, and are written to with 16-bit word writes. Data bits 15 through 12 are ignored. Bit 11 is the MSB and bit 0 is the LSB. The same data is written to the registers regardless of whether the board is configured for offset binary or two's complement mode. MSB inversion, if jumper selected, takes place between the registers and their respective DACs. The registers are cleared at power up and system resets.

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D/A Registers

These registers contain the data that is loaded into the DACs upon receipt of an UPDATE command.

Address:	Slot starting address + 4 (hex)	D/A Register 0
	Slot starting address + 8 (hex)	D/A Register 1
	Slot starting address + 10 (hex)	D/A Register 2
	Slot starting address + 20 (hex)	D/A Register 3
	Slot starting address + 40 (hex)	D/A Register 4
	Slot starting address + 80 (hex)	D/A Register 5

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	D11	D10	D9	D8

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
15-12	X	Don't care bits.
11	D11	The most significant bit of data to be loaded into the DAC. If two's complement mode is jumper selected, this bit is inverted before it is loaded into the DAC.
10-0	D<10..0>	The other data bits to be loaded into the DAC.

The formula for the voltage output versus digital code for a unipolar analog output configuration is as follows:

$$Vout = Vref * \frac{(digital\ code)}{4,096}$$

where V_{ref} is the reference voltage applied to the analog output channel. The digital code in the above formula is a decimal value ranging from 0 to 4,095.

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Table 4-3. Analog Output Voltage Versus Digital Code (Unipolar Mode)

Digital Code		Voltage Output	
Decimal	**Hex**	**Vref**	**Vref = 10 V**
0	0	0	0 V
1	1	$\frac{Vref}{4,096}$	2.44 mV
1,024	0400	$\frac{Vref}{4}$	2.5 V
2,048	0800	$\frac{Vref}{2}$	5 V
3,072	0C00	$\frac{Vref * 3}{4}$	7.5 V
4,095	0FFF	$\frac{Vref * 4,095}{4,096}$	9.9976 V

The formula for the voltage output versus digital code for a bipolar, straight binary analog output configuration is

$$Vout = Vref * \frac{(digital\ code - 2,048)}{2,048}$$

where Vref is the reference voltage applied to the analog output channel. The digital code in the above formula is a decimal value ranging from 0 to 4,095.

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Table 4-4. Analog Output Voltage Versus Digital Code (Bipolar, Straight Binary Mode)

Digital Code		Voltage Output	
Decimal	**Hex**	**Vref**	**Vref = 10 V**
0	0	- Vref	- 10 V
1	1	$\frac{Vref(-2,047)}{2,048}$	-9.9951 V
1,024	0400	$\frac{-Vref}{2}$	- 5 V
2,047	07FF	$\frac{Vref}{2,048}$	- 4.88 mV
2,048	0800	0	0 V
2,049	0801	$\frac{Vref}{2,048}$	4.88 m V
3,072	0C00	$\frac{Vref}{2}$	5 V
4,095	0FFF	$\frac{Vref(2,047)}{2,048}$	9.9951 V

The formula for the voltage output versus digital code for a bipolar, two's complement analog output configuration is as follows:

$$Vout = Vref * \frac{\text{digital code}}{2,048}$$

where Vref is the reference voltage applied to the analog output channel. The digital code in the above formula is a decimal value ranging from -2,048 to 2,047.

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Table 4-5. Analog Output Voltage Versus Digital Code (Bipolar, Two's Complement Mode)

Digital Code		**Voltage Output**	
Decimal	**Hex**	**Vref**	**Vref = 10 V**
-2,048	800	-Vref	- 10 V
-2,047	801	$Vref * \frac{-2,047}{2,048}$	-9.9951 V
1,024	C00	$\frac{-Vref}{2}$	- 5 V
-1	FFF	$\frac{-Vref}{2,048}$	- 4.88 mV
0	0	0	0 V
1	1	$\frac{Vref}{2,048}$	4.88 mV
1,024	400	$\frac{Vref}{2}$	5 V
2,047	7FF	$Vref * \frac{2,047}{2,048}$	9.9951 V

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Update Register

When this register is written to, a 300 nsec UPDATE pulse is generated on the NB-AO-6, causing the data in the D/A Register to be loaded into the corresponding DAC.

Address: Slot starting address + 100 (hex)

Type: Write-only

Word size: 16-bit

Bit map: Not applicable, no bits are used.

This register can be simultaneously written to with any combination of D/A Registers. To do this, add the offsets of the desired D/A Registers and Update Register, and add the sum to the slot starting address. The data is loaded into the selected D/A Registers and immediately transferred to the DACs. For example, if the NB-AO-6 is plugged into slot B, D/A Channel 3 can be written to for immediate output updating by writing the desired data to address B0 0000 (slot) + 20 (D/A Register 3) + 100 (update), that is, address B0 0120.

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Configuration Register Group

This register contains DMA channel selection bits and a bit related to hardware triggering of UPDATE pulses. The offset of this register is A0000 hex. Address bits 0 and 1 should be cleared and address bits 2 through 16 are ignored. This is a write-only register.

Bits 2 through 0 of the 4-bit Configuration Register select which DMA channel is used for DMA requests; bit 2 is the MSB and bit 0 is the LSB. DMA requests are generated by every UPDATE pulse unless DMA is disabled. DMA is disabled when DMA address 4 is selected because there is no DMA Channel 4. DMA Channel 4 is the configuration at startup. Bit 3 of the Configuration Register selects the polarity of the external signal that triggers an UPDATE pulse. If bit 3 is set, a rising edge on the EXT.UPD pin of the output connector or line A0 of the RTSI switch triggers an UPDATE pulse. If bit 3 is cleared, then the circuitry is falling-edge sensitive. Falling-edge sensitive is the startup/reset condition. Changing the bit can cause an UPDATE pulse to be generated, but this should not be a problem as the bit is generally programmed before data has been written to the board.

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Configuration Register

This register contains DMA channel selection bits and a bit related to hardware triggering of UPDATE pulses.

Address: Slot starting address + A0000 (hex)

Type: Write-only

Word size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	X	EDGE	DMAA2	DMAA1	DMAA0

Bit	Name	Description
7-4	X	Don't care bits.
3	EDGE	If this bit is set, a rising edge on the EXT.UPD pin on the back panel or pin A0 of the RTSI switch causes an UPDATE pulse to be generated. If it is cleared, the circuitry is falling-edge sensitive. This is the startup/reset condition.
2-0	DMAA<2..0>	These three bits determine which DMA channel is to be used. Selecting DMA Channel 4 (DMAA<2..0>=100) inhibits DMA requests because there is no DMA Channel 4. This is the startup/reset condition. Selecting any other DMA channel causes each UPDATE pulse to generate a DMA request on that channel. This is useful in waveform generation applications.

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RTSI Switch Register Group

The two registers making up the RTSI Switch Register Group allow the NB-AO-6 RTSI switch to be programmed for the routing of signals on the RTSI bus trigger lines to and from NB-AO-6 signal lines. The RTSI switch is programmed by shifting a 56-bit routing pattern into the RTSI switch and then loading the internal RTSI Control Register. The routing pattern is shifted into the RTSI switch by writing one bit at a time to the RTSI Shift Register. The RTSI Control Register is then loaded by writing to the RTSI Strobe Register.

The base offset of the RTSI Switch Registers is C0000 hex. Address bit 2 selects either the input shift register or the control register of the chip. Address bits 0 and 1 should be cleared and address bits 3 through 16 are ignored. This is a write-only register.

The RTSI switch allows any RTSI bus trigger line to be connected to any of seven points on the card. On the NB-AO-6, line A0 is connected to be able to trigger an UPDATE pulse, and line A1 is driven by the UPDATE pulse itself. Lines A2 through A6 are unused. Writes to the RTSI switch should be byte-writes with only data bit 0 used.

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RTSI Switch Shift Register

The RTSI Switch Shift Register is written to in order to load the RTSI switch internal 56-bit control register with routing information for switching signals to and from the RTSI bus trigger lines. The Shift Register is a 1-bit register and must be written to 56 times to shift the 56 bits into the internal register.

Address: Slot starting address + C 0000 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	RSI

Bit	Name	Description
7-1	X	Don't care bits.
0	RSI	RTSI Switch Serial Input. This bit is the serial input to the RTSI switch. Each time the RTSI Shift Register is written to, the value of this bit is shifted into the RTSI switch. See *Programming the RTSI Switch* later in this chapter for more information.

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RTSI Switch Strobe Register

The RTSI Switch Strobe Register is written to in order to load the contents of the RTSI Shift Register into the RTSI Switch Control Register, thereby updating the RTSI switch routing pattern. The RTSI Switch Strobe Register is written to after shifting the 56-bit routing pattern into the RTSI Switch Shift Register.

Address: Slot starting address + C 0004 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map: Not applicable, no bits are used

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Configuration ROM

The Configuration ROM on the NB-AO-6 contains information pertinent to the NB-AO-6 board and is required by the Macintosh operating system to identify the boards in each slot. Accesses to this ROM should be byte-reads only. The Macintosh NuBus System Slot Manager reads the Configuration ROM upon system startup.

The Configuration ROM is mapped to address offset location F8000 through FFFFC (hex). The ROM is 8-bits (byte) wide and 8 kilobytes in length. Each byte of the ROM is mapped to every fourth address location on the NB-AO-6 board; for example, the first byte is read from slot address + F8000; the second byte is read from slot address + F8004; the third byte is read from slot address + F8008, and so on.

The base offset of the configuration is F8000 hex. Address bits 2 through 14 select one of 8 kilobytes that can be read. Address bits 0 and 1 should be cleared. Address bits 15 and 16 are ignored.

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Programming Considerations

A read from the Configuration ROM takes four NuBus clock cycles (400 nsec). All other board accesses take three clock cycles. When a D/A write occurs with address bit 8 set so that the output is to respond immediately, the UPDATE pulse starts as soon as the write cycle is over and lasts three more clock cycles. External triggering, on the other hand, causes the update pulse to start immediately. The NB-AO-6 has been designed so that triggering an UPDATE pulse before a previous one has finished just extends the pulse. However, the outputs should never need updating more than once every microsecond or so.

The NB-AO-6 is fully supported by the National Instruments LabVIEW programming environment under NI-DAQ for Macintosh, a software package available from National Instruments. NI-DAQ for Macintosh provides a library of VIs to write to the RTSI switch, to write to the Configuration Register, to write to a D/A channel for later update, to write to and update a D/A channel, to update all the D/A channels, and to clear all the D/A outputs. There is also a VI that returns a digital code based on a desired output voltage and the configuration of the board. These functions are also available as C subroutines.

Register Programming Considerations

Registers in the Macintosh NuBus are memory-mapped; to write to a register, a value is stored in a memory location. To read a register, a memory location is read. Only memory location reads and writes can be performed on the NB-AO-6 registers. Mathematical or logical operations *cannot* be directly applied to the NB-AO-6 registers. Attempting to do so results in unpredictable program behavior.

Several write-only registers on the NB-AO-6 contain bits that control several independent pieces of the onboard circuitry. In the set or clear instructions given, specific register bits should be set or cleared without changing the current state of the remaining bits in the register. However, writing to these registers affects all register bits simultaneously. Reading these registers to determine which bits have been set or cleared in the past is not possible; therefore, maintaining a software copy of the write-only registers is recommended. This software copy can then be read to determine the status of the write-only registers. To change the state of a single bit without disturbing the remaining bits, set or clear the bit in the software copy and write the software copy to the register.

RTSI Bus Trigger Line Programming Considerations

The RTSI switch allows connection of signals on the NB-AO-6 to the seven RTSI bus trigger lines. The RTSI switch has seven pins labeled A<6..0> connected to NB-AO-6 signals, and seven pins labeled B<6..0> connected to the seven RTSI bus trigger lines. The signal connected to each pin is shown in Table 4-6.

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Table 4-6. RTSI Switch Signal Connections

RTSI Switch Pin	Signal Name	Signal Direction
Side A:		
A0	$\overline{\text{TRIGUP}}$	Input
A1	$\overline{\text{UPDATE}}$	Output
A2	(no connection)	
A3	(no connection)	
A4	(no connection)	
A5	(no connection)	
A6	(no connection)	
Side B:		
B0	TRIGGER0	Bidirectional
B1	TRIGGER1	Bidirectional
B2	TRIGGER2	Bidirectional
B3	TRIGGER3	Bidirectional
B4	TRIGGER4	Bidirectional
B5	TRIGGER5	Bidirectional
B6	TRIGGER6	Bidirectional

Programming the RTSI Switch

The RTSI switch can be programmed to connect any of the signals on side A to any of the signals on side B and vice versa. To do this, a 56-bit pattern is shifted into the RTSI switch by writing one bit at a time to the RTSI Shift Register, and then writing to the RTSI Strobe Register to load the pattern into the RTSI switch.

The 56-bit pattern is made up of two 28-bit patterns, one for side A and one for side B of the RTSI switch. The low order 28 bits select the signal sources for side B pins. The high order 28 bits select the signal sources for side A pins. Each of the 28-bit patterns is made up of seven 4-bit fields, one for each pin. The 4-bit field selects the signal source and the output enable for the pin. Figure 4-1 shows the bit map of the RTSI switch 56-bit pattern.

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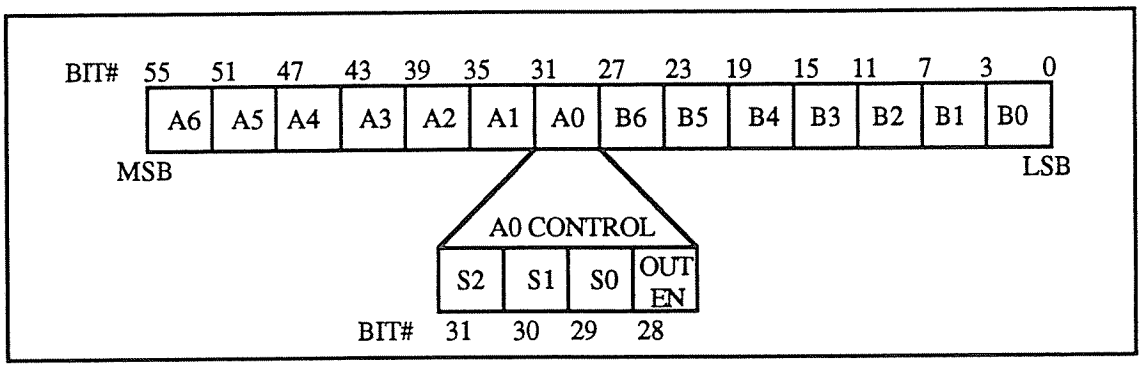


Figure 4-1. RTSI Switch Control Pattern

In Figure 4-1, the fields labeled A6 through A0 and B6 through B0 are the 4-bit control fields for each RTSI switch pin of the same name. The 4-bit control field for pin A0 is also shown in Figure 4-1.

The bits labeled S2 through S0 are the signal source selection bits for the pin. One of seven source signals can be selected. Pins A6 through A0 can select any of the pins B6 through B0 as signal sources. Pins B6 through B0 can select any of the pins A6 through A0 as signal sources. For example, the pattern 011 for S2 through S0 in the A0 control field would select the signal connected to pin B3 as the signal source for pin A0.

The bit labeled OUT EN is the output enable bit for that pin. If the OUT EN bit is set, the pin is driven by the selected source signal (pin acts as an output pin). If the OUT EN bit is cleared, the pin is not driven regardless of the source signal selected; instead, the pin can be used as an input pin.

If the A0 control field contains the pattern 0111, the signal connected to pin B3 (Trigger Line 3) appears at pin A0. On the NB-AO-6, this allows the TRIGUP* signal to be driven by Trigger Line 3. Conversely, if the B4 control field contains the pattern 0011, the UPDATE* signal appears at pin B4. In this way, boards connected via the RTSI bus can send signals to each other over the RTSI Bus Trigger Lines.

To program the RTSI switch:

1. Calculate the 56-bit pattern based on the desired signal routing.
   a. Clear the OUT EN bit for all input pins and for all unused pins.
   b. Specify the signal source pin for all output pins by setting bits S2 through S0 to the source pin number.
   c. Set the OUT EN bit for all output pins.
2. For $i = 0$ to 55, do the following:
   a. Copy bit i of the 56-bit pattern to bit 0 of an 8-bit temporary variable.
   b. Write the temporary variable to the RTSI Shift Register (8-bit write).

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3. Write zero to the RTSI Strobe Register (8-bit write). This loads the 56-bit pattern into the RTSI switch. At this point the new signal routing goes into effect.

Step 2 can be accomplished by first writing the low order eight bits of the 56-bit pattern to the RTSI Shift Register, then shifting the 56-bit pattern right once, and finally repeating this two-step operation 56 times. Only bit 0 of the word written to the RTSI Shift Register is used. The higher order bits are ignored.

Programming DMA Operations

DMA operations can be used to write to the analog outputs on the NB-AO-6 if a DMA board is included in the system and connected with the NB-AO-6 over the RTSI bus.

The NB-AO-6 can be programmed to generate a DMA request signal on each UPDATE pulse. Therefore, each time data is transferred to the D/As, a request is issued to refill the D/A Registers. In this way, new data can be loaded into the D/A at precisely timed intervals. The UPDATE pulses can be triggered by an external signal through the EXT.UPD pin or by the DMA board over the RTSI bus. To set up DMA operation on the NB-AO-6, perform the following steps:

1. Set the DMAA<2..0> bits in the Configuration Register to the DMA channel to be used. DMA Channels 0, 1, 2, 3, 4, 5, 6, and 7 are available; selecting DMA Channel 4 inhibits DMA requests.

2. Program the DMA board DMA controller to service DMA requests from the NB-AO-6.

3. Program the 9513 timer on the DMA board to trigger UPDATE pulses on the NB-AO-6 (optional). This involves programming the RTSI switches on both boards.

See the user manual that came with your DMA board for programming instructions. You need the following information to program the DMA Controller on the DMA board:

- The requestor is the NB-AO-6 board.
- The requestor device type is I/O device.
- Use requestor hold mode.
- The requestor address is the selected D/A Register NuBus address. This address is illustrated in the following table:

Slot Number	NB-AO-6 Requestor Address (Hex)
9	F9F0 0000 + D/A Register offset
A	FAF0 0000 + D/A Register offset
B	FBF0 0000 + D/A Register offset
C	FCF0 0000 + D/A Register offset
D	FDF0 0000 + D/A Register offset
E	FEF0 0000 + D/A Register offset

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- Transfer cycles are two-cycle.
- Data transfer mode is single-transfer mode.
- The requestor bus size is 16-bit.
- The transfer type is read transfer (read from target).
- The target device is a memory buffer (therefore a memory device).
- The target address is the program address of the memory buffer that is to be read from.
- Target address incrementing is recommended.
- Specifying a 32-bit bus size for the target device is recommended for efficiency.
- The byte count is the number of data points desired (for example, samples per waveform period) multiplied by two.
- Enabling auto-initialization to generate repeated cycles of a waveform is recommended.

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Chapter 5
Calibration Procedures

This chapter explains how to recalibrate the NB-AO-6 analog circuitry.

The NB-AO-6 is shipped fully calibrated and should seldom need recalibration. However, you should periodically check board accuracy and make adjustments if necessary. This should take place approximately once every year, or whenever one of the board's trim potentiometers could have accidentally had its setting changed. Changing jumper settings or reference voltages does not necessitate recalibration. If calibration is necessary, the recommended calibration procedure requires a voltmeter with 0.005% resolution and accuracy.

The procedures in this chapter require that certain values be output on each channel. If necessary, refer to Chapter 4, *Programming*.

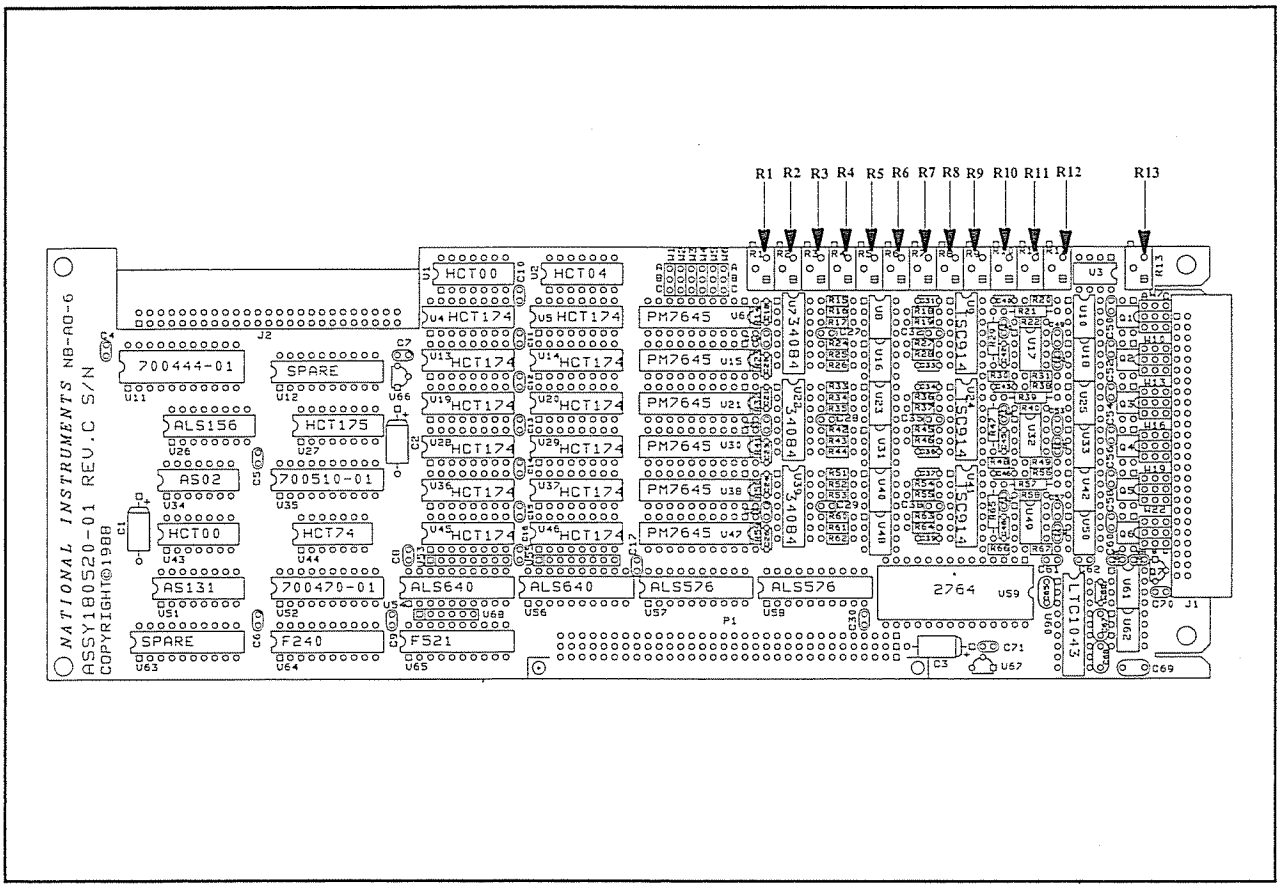


Figure 5-1. NB-AO-6 Trimpot Locator Diagram

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Voltage Reference

The NB-AO-6 has a built-in 5 V reference whose output is doubled and halved with the use of highly accurate flying-capacitor techniques to provide accurate 10 and 2.5 V references for the DACs. When the reference-select jumper for a given channel is in the internal position, the 10 V reference is selected for that channel. The 10 and 5 V signals are not available on the back connector, but the 2.5 V signal is. Because of the accuracy of the flying-capacitor voltage multiplication and division employed to derive the references, calibrating the 2.5 V signal calibrates the 10 V signal as well (typically within 10 ppm).

To calibrate the 2.5 V reference signal:

1. Connect the positive probe of the voltmeter to the 2.5 V output on the connector or connector block (pin 50). Connect the negative probe of the voltmeter to the corresponding analog ground pin (pin 49).

2. If necessary, adjust the voltage reference trim potentiometer (R13) to yield a reading of 2.5 V ± 0.25 mV.

D/A Offsets

When operating in unipolar mode, each channel is guaranteed to have an output offset of less than 200 µV. This corresponds to less than 1/2 LSB of a 2 V full-scale range. This offset is stable because it is obtained by the use of chopper stabilization – a technique that nulls offsets hundreds of times a second. For this reason, there is no offset trim for unipolar ranges. If the unipolar offset is greater than the guaranteed limit or drifts excessively, contact National Instruments.

There are offset trim potentiometers to null out bipolar mode offsets.

To trim the offset of a D/A channel (bipolar mode only) complete the following steps:

1. Supply a reference voltage to the channel of approximately 10 V. This reference can be either internal or external.

2. Connect the voltmeter to the desired DAC output as shown in Table 5-1.

3. Load the DAC with a value that should produce 0 V output–0 (two's complement) or 2,048 (offset binary).

4. If necessary, adjust the channel's offset potentiometer (see Table 5-2) to give a reading of 0 V ± 200 µV.

5. If the channel is to be used with an AC reference, the same procedure can be used to calibrate it, except that the offset should be adjusted to null out the AC signal. The AC reference should be several volts in magnitude but should not be above a few hundred hertz in frequency to ensure accurate calibration.

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D/A Gains

A channel's gain (full-scale span) can be easily calibrated after its offset has been trimmed.

To trim the gain of a D/A channel complete the following steps:

1. Provide the DAC with a precision +10 V reference, either the internal (calibrated) one or an external one.
2. Connect the voltmeter to the desired DAC output as shown in Table 5-1.
3. Load the DAC with a full-scale positive value: 4,095 (binary, offset binary) or 2,047 (two's complement).
4. If necessary, adjust the channel's gain potentiometer (see Table 5-2) to give a reading of 9.9976 V ± 1 mV (unipolar) or 9.9951 V ± 2 mV (bipolar).

Adjusting the gains with other reference voltages is also possible. In this example, the desired output is as follows:

$$\frac{4{,}095}{4{,}096\ V_{ref}} \text{ (unipolar) or } \frac{2{,}047}{2{,}048\ V_{ref}} \text{ (bipolar)}$$

Table 5-1. Voltmeter Connections for Each DAC

D/A Channel	+ Probe	- Probe
0	pin 4	pin 3
1	pin 12	pin 11
2	pin 20	pin 19
3	pin 28	pin 27
4	pin 36	pin 35
5	pin 44	pin 43

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Table 5-2. DAC Adjustment Potentiometers

D/A Channel	Bipolar Offset Trim	Gain
0	R12	R11
1	R10	R9
2	R8	R7
3	R6	R5
4	R4	R3
5	R2	R1

Note: Calibrating in bipolar mode also ensures accuracy in unipolar mode. The converse is not true, however, because a D/A channel's bipolar offset trim potentiometer also affects gain in unipolar mode. For this reason, calibration should be done in bipolar mode unless the channel to be calibrated is used only in unipolar mode.

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Appendix A
Specifications

This appendix lists the specifications of the NB-AO-6. These specifications are typical at 25° C unless otherwise stated. The operating temperature range is 0° to 70° C.

Analog Outputs

Number of channels	Six
Input data coding	Straight binary (unipolar), Offset binary or two's complement (bipolar)
Voltage outputs ranges	0 to +10 V, ±10 V, 0 to +2.5 V, ±2.5 V, 0 to $+V_{ref}$, $\pm V_{ref}$
V_{ref} input range	±10 V
V_{ref} input impedance	10 kΩ
current drive	±5 mA maximum
output impedance	0.1 Ω maximum
capacitive drive	500 pF maximum
protection	Short circuit to ground
gain error	Adjustable to zero
unipolar zero error	200 µV maximum
bipolar zero error	Adjustable to zero
accuracy	±0.025% FSR
settling time to 0.5 LSB 20 V step 10 V step 100 mV step	 4 µsec 3 µsec 2 µsec
slew rate	20 V/µsec min, 30 V/µsec typical
Current outputs type	4 to 20 mA current sink to ground
output resistance	10^9 Ω minimum

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excitation voltage	+7 to +40 VDC (at connector pins)
accuracy	±0.1% FSR
slew rate	7.5 mA/µsec
protection	Short circuit and open circuit

DAC

D/A type	PM7645HP
digital inputs	Double-buffered, with simultaneous update capability
resolution	12 bits (1 part in 4,096)
integral nonlinearity	± 0.5 LSB
differential nonlinearity	±1 LSB (guaranteed monotonic)

Thermal characteristics

unipolar zero drift	1 µV/°C
bipolar zero drift	±5 ppm of FSR/°C
gain drift	±5 ppm/°C typical ±10 ppm/°C maximum (excluding reference drift)
reference drift	±5 ppm/°C typical ±8.5 ppm/°C maximum
monotonicity	Monotonic, 0° to 70°C

Throughput

Single channel	350 kHz maximum
All six channels (limited by Macintosh memory access time)	58 kHz maximum

Power Requirements (from NuBus)

+5 VDC	0.35 A typical
+12 VDC	65 mA typical + load
-12 VDC	60 mA typical + load
	Load is ±5 mA maximum

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Physical

Dimensions	4.0 in. by 10.7 in.
I/O Connector	50-pin male ribbon cable connector

Operating Environment

Component temperature	0° to 70°C
Relative humidity	5% to 90%, noncondensing

Storage Environment

Temperature	-55° to 150°C
Relative humidity	5% to 90%, noncondensing

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Appendix B
I/O Connector

This appendix shows the pinout and signal names for the 50-pin I/O connector on the NB-AO-6.

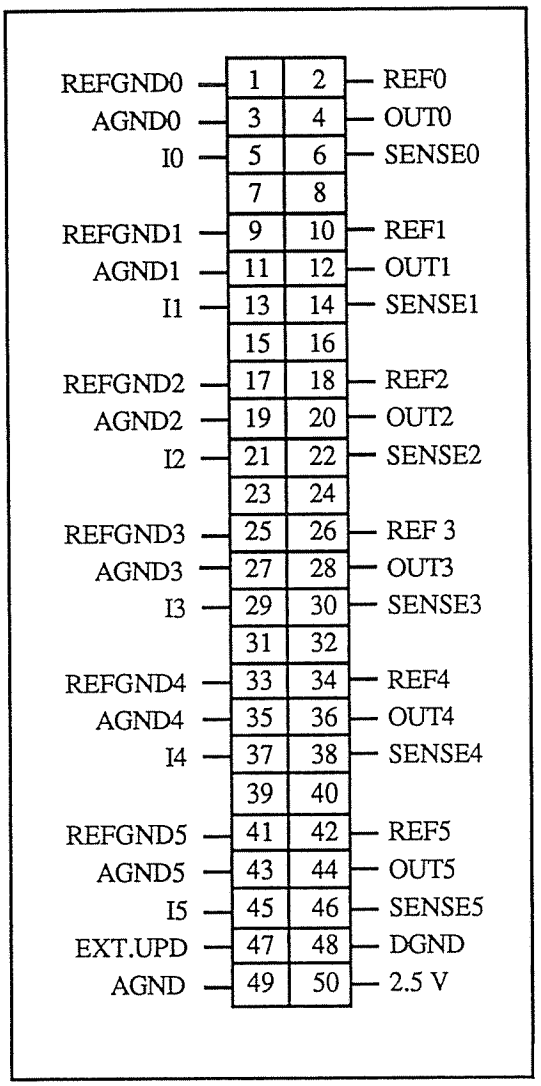


Figure B-1. NB-AO-6 I/O Connector

Detailed signal specifications are given in Chapter 2, *Configuration and Installation.*

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Appendix C
Customer Communication

For your convenience, this appendix contains a form to help you gather the information necessary to help us solve technical problems you might have as well as a form you can use to comment on the product documentation. Filling out a copy of the *Technical Support Form* before contacting National Instruments helps us help you better and faster.

National Instruments provides comprehensive technical assistance around the world. In the U.S. and Canada, applications engineers are available Monday through Friday from 8:00 a.m. to 6:00 p.m. (central time). In other countries, contact the nearest branch office. You may fax questions to us at any time.

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Switzerland	056/20 51 51	056/20 51 55
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Technical Support Form

Photocopy this form and update it each time you make changes to your software or hardware, and use the completed copy of this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name _____

Company _____

Address _____

_____

Fax (___)_____ Phone (___)_____

Computer brand _____ Model _____ Processor _____

Operating system _____

Speed _____MHz RAM _____M Display adapter _____

Mouse _____yes _____no Other adapters installed _____

Hard disk capacity _____M Brand _____

Instruments used _____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is _____

_____

_____

_____

_____

List any error messages _____

_____

_____

_____

_____

The following steps will reproduce the problem _____

_____

_____

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NB-AO-6 Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

National Instruments Products

- Revision Level of NB-AO-6 _____
- Slot (Base I/O Address) of NB-AO-6 _____
- Reference Voltage (Internal or External) _____
- Output Mode (Unipolar or Bipolar) _____
- Data Coding (Offset Binary or Two's Complement) _____
- DMA Server (NB-DMA-8-G, NB-DMA2800) _____
- NI-DAQ Version _____
- Programming Language _____

Other Products

- Computer Make and Model _____
- Microprocessor _____
- Clock Frequency _____
- Type of Video Board Installed _____
- DOS Version _____
- Programming Language Version _____
- Other Boards in System _____
- Base I/O Address of Other Boards _____
- DMA Channels of Other Boards _____
- Interrupt Level of Other Boards _____

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Documentation Comment Form

National Instruments encourages you to comment on the documentation supplied with our products. This information helps us provide quality products to meet your needs.

Title: **NB-AO-6 User Manual**

Edition Date: **July 1993**

Part Number: **320098-01**

Please comment on the completeness, clarity, and organization of the manual.

If you find errors in the manual, please record the page numbers and describe the errors.

Thank you for your help.

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