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DAQ

NB-MIO-16X

User Manual



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November 1993 Edition
Part Number 320157-01

NB-MIO-16X
User Manual

Multifunction I/O Board for Macintosh NuBus Computers

November 1993 Edition

Part Number 320157-01

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Preface

This manual describes the mechanical and electrical aspects of the NB-MIO-16X and contains information concerning its operation and programming. The NB-MIO-16X is a high-performance multifunction analog, digital, and timing input/output (I/O) board for Macintosh NuBus computers. The NB-MIO-16X contains a 16-bit analog-to-digital converter (ADC) with up to 16 analog inputs, two 12-bit digital-to-analog converters (DACs) with voltage outputs, eight lines of TTL-compatible digital I/O, and three 16-bit counter/timer channels for timing I/O. If additional analog inputs are required, you can use the AMUX-64T multiplexer board.

Organization of This Manual

The *NB-MIO-16X User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the NB-MIO-16X; lists the contents of your NB-MIO-16X kit, the optional software, and the optional equipment; and explains how to unpack the NB-MIO-16X.
- Chapter 2, *Configuration and Installation*, explains board configuration, installation of the NB-MIO-16X in the Macintosh NuBus computer, signal connections to the NB-MIO-16X, and cable wiring.
- Chapter 3, *Theory of Operation*, contains a functional overview of the NB-MIO-16X and explains the operation of each functional unit making up the NB-MIO-16X.
- Chapter 4, *Programming*, describes in detail the address and function of each of the NB-MIO-16X registers. This chapter also includes important information about programming the NB-MIO-16X.
- Chapter 5, *Calibration Procedures*, discusses the calibration procedures for the NB-MIO-16X analog input and analog output circuitry.
- Appendix A, *Specifications*, lists the specifications of the NB-MIO-16X.
- Appendix B, *I/O Connector*, contains the pinout and signal names for the NB-MIO-16X 50-pin I/O connector.
- Appendix C, *AMD Data Sheet*, contains the manufacturer data sheet for the Am9513A/ AmZ8073A System Controller (Advanced Micro Devices, Inc.) integrated circuit. This circuit is used on the NB-MIO-16X.
- Appendix D, *Customer Communication*, contains forms for you to complete to facilitate communication with National Instruments concerning our products.
- The *Index* contains an alphabetical list of key terms and topics used in this manual, including the page where each one can be found.

Conventions Used in This Manual

The following conventions are used in this manual:

DIFF	DIFF refers to differential input configuration.
DMA board	DMA board refers to the NB-DMA-8-G board or the NB-DMA2800 board unless otherwise noted.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
Macintosh	Macintosh refers to all Macintosh II and Macintosh Quadra computers unless otherwise noted.
NI-DAQ	NI-DAQ is used throughout this manual to refer to the NI-DAQ software for Macintosh unless otherwise noted.
NRSE	NRSE refers to non-referenced single-ended input configuration.
RSE	RSE refers to referenced single-ended input configuration.

Abbreviations

The following metric system prefixes are used with abbreviations for units of measure in this manual:

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

The following abbreviations are used in this manual:

A	amperes
C	Celsius
dB	decibels
°	degrees
F	farads
ft	feet
hex	hexadecimal
Hz	hertz
in.	inches

Abbreviations (continued)

m	meters
M	megabytes of memory
Ω	ohms
%	percent
ppm	parts per million
rms	root mean square
sec	seconds
V	volts
Vrms	volts root mean square

Acronyms

The following acronyms are used in this manual:

AC	alternating current
A/D	analog-to-digital
ADC	A/D converter
CMOS	complementary metallic oxide semiconductor
D/A	digital-to-analog
DAC	D/A converter
DMA	direct memory access
EPROM	electrical programmable read-only memory
FIFO	first-in-first-out
I/O	input/output
LSB	least significant bit
NMR	nonmaskable interrupt request
ROM	read-only memory
RTSI	Real-Time System Integration
TC	terminal count
TTL	transistor-transistor logic
VDC	volts direct current
VI	virtual instrument

Related Documentation

The following documents contain information that you may find helpful as you read this manual:

- The Macintosh II or Quadra *Owner's Manual*, *Getting Started* manual, or *Setting Up* manual

Consult the following manual if you plan to program the Am9513A Counter/Timer used on the NB-MIO-16X:

- *The Am9513A/Am9513 System Timing Controller* technical manual

Consult the following National Instruments manuals if you plan to program DMA operations with this board:

- The *NB-DMA-8-G User Manual* (part number 320097-01)
- The *NB-DMA2800 User Manual* (part number 320240-01)

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix D, *Customer Communication*, at the end of this manual.

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Chapter 1
Introduction

This chapter describes the NB-MIO-16X; lists the contents of your NB-MIO-16X kit, the optional software, and the optional equipment; and explains how to unpack the NB-MIO-16X.

The NB-MIO-16X is a high-performance multifunction analog, digital and timing I/O board for Macintosh NuBus computers. The NB-MIO-16X has the following features:

- Fast 16-bit ADC
  - 16 single-ended or 8 differential channels (expandable with AMUX-64T multiplexer board)
  - Programmable gains of 1, 10, 100, 500, or 1, 2, 4, 8
  - 42 µsec converter or 18 µsec converter
  - Guaranteed rates up to 55 ksamples/sec
  - 16-word FIFO A/D buffer to obtain the highest possible data acquisition rate
  - Internal or external A/D timing
- Two double-buffered multiplying 12-bit DACs
  - Unipolar and bipolar voltage output available
  - Onboard reference voltages of 5 V and 10 V
  - Onboard timer for waveform generation
- Eight digital I/O lines, each able to sink up to 24 mA current
- Three independent 16-bit counter/timers for frequency counting, event counting, and pulse output applications
- Timer-generated interrupts
- High-performance RTSI bus interface
  - Triggers for system-level timing
  - DMA operation over a RTSI bus with a DMA board

Figure 1-1 shows the NB-MIO-16X.

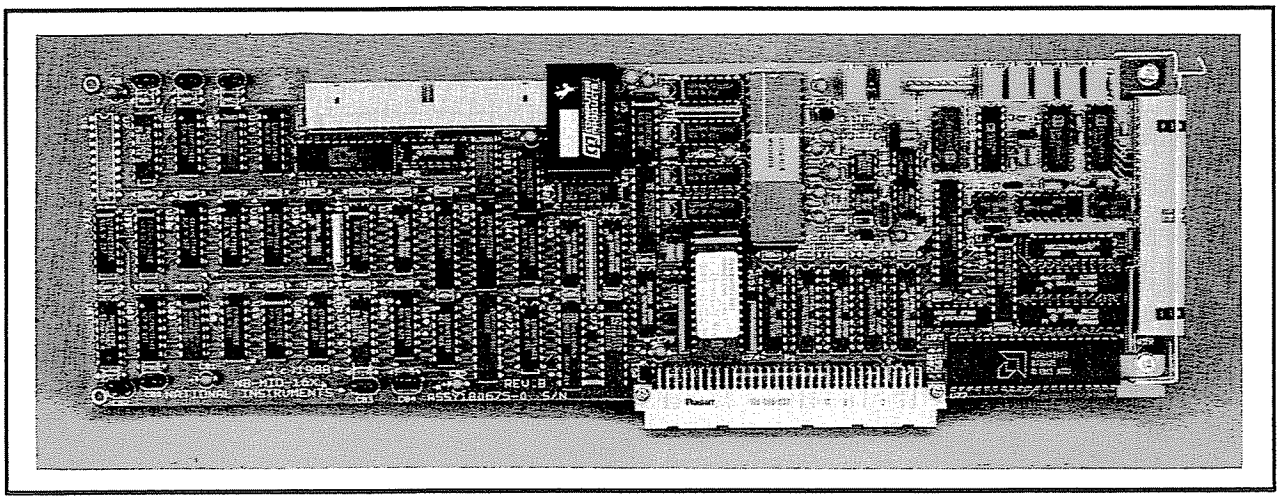


Figure 1-1. NB-MIO-16X Interface Board

The NB-MIO-16X, with its multifunction analog, digital, and timing I/O, can be used for automation of machine and process control, level monitoring and control, instrumentation, electronic test, and many other functions. The multichannel analog input can be used for signal and transient analysis, data logging, and chromatography. The two analog output channels can be used for machine and process control, analog function generation, 12-bit resolution voltage source, and programmable signal attenuation. The eight TTL-compatible digital I/O lines can be used for machine and process control, intermachine communication, and relay switching control. The three 16-bit counter/timers can be used for pulse and clock generation, timed control of laboratory equipment, and frequency, event, and pulse-width measurement. With all these functions on one board, laboratory processes can be automatically monitored and controlled. If additional analog inputs are required, you can use the AMUX-64T multiplexer board. This four-to-one multiplexer can process 64 single-ended inputs. Up to four AMUX-64T boards can be cascaded to obtain 256 single-ended inputs.

The NB-MIO-16X has an interface to the National Instruments RTSI bus. This bus sends timing signals between National Instruments NB Series boards. The NB-MIO-16X can send signals from the onboard counter/timer to another board, or another board can control single and multiple A/D conversions on the NB-MIO-16X.

The NB-MIO-16X is available in two conversion speeds and two gain ranges, for a total of four different versions:

- NB-MIO-16XL-18
- NB-MIO-16XL-42
- NB-MIO-16XH-18
- NB-MIO-16XH-42

The NB-MIO-16XL has software-programmable gain settings of 1, 10, 100, and 500 for low-level analog input signals. The NB-MIO-16XH has software programmable gain settings of 1, 2, 4, and 8 for high-level analog input signals. The NB-MIO-16X(L/H)-42 has an ADC capable of a 42 µsec conversion rate, which is about 24 kbytes/sec. The NB-MIO-16X(L/H)-18 has an ADC capable of an 18 µsec conversion rate, which is about 55 kbytes/sec.

Detailed specifications for the NB-MIO-16X are included in Appendix A, *Specifications*.

What Your Kit Should Contain

Each version of the NB-MIO-16X board has a different part number and kit part number, listed as follows.

Kit Name	Kit Part Number	Kit Component	Board Part Number
NB-MIO-16XL-18	776259-01	NB-MIO-16XL-18 board	180675-01
NB-MIO-16XL-42	776259-02	NB-MIO-16XL-42 board	180675-02
NB-MIO-16XH-18	776259-11	NB-MIO-16XH-18 board	180675-11
NB-MIO-16XH-42	776259-12	NB-MIO-16XH-42 board	180675-12

The board part number is printed on your board along the top edge on the component side. You can identify which version of the NB-MIO-16X board you have by looking up the part number in the preceding table.

In addition to the board, each version of the NB-MIO-16X kit contains the following components.

Kit Component	Part Number
NB-MIO-16X User Manual	320157-01
NI-DAQ software for Macintosh, with manuals	776181-01
NI-DAQ for Macintosh Software Reference Manual	320103-01

If your kit is missing any of the components or if you received the wrong version, contact National Instruments.

Your NB-MIO-16X is shipped with the NI-DAQ software for Macintosh. NI-DAQ has a library of functions that can be called from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer, SCXI, RTSI, and self-calibration. NI-DAQ maintains a consistent software interface among its different versions so you can switch between platforms with minimal modifications to your code. NI-DAQ comes with language interfaces for MPW C, THINK C, Pascal, and Microsoft QuickBASIC. Any language that uses Device Manager Toolbox calls can access NI-DAQ.

Optional Software

This manual contains complete instructions for directly programming the NB-MIO-16X. Normally, however, you should not need to read the low-level programming details in the user manual because the NI-DAQ software package for controlling the NB-MIO-16X is included with the board. Using NI-DAQ is quicker and easier than and as flexible as using the low-level programming described in Chapter 4, *Programming*.

The NB-MIO-16X can also be used with LabVIEW (part number 776141-01), a software system that features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with the NB-MIO-16X and other National Instruments boards, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software for Macintosh.

Optional Equipment

Equipment	Part Number
NB-DMA2800 board	776305-01
NB-DMA-8-G board	776161-01
CB-50 I/O connector block (50 screw terminals)	
with 0.5-m type NB1 cable	776164-01
with 1.0-m type NB1 cable	776164-02
NB Series RTSI bus cables for	
2 boards	776188-02
3 boards	776188-03
4 boards	776188-04
5 boards	776188-05
SCXI signal conditioning modules	
SCXI-1100 32-channel differential multiplexer/amplifier	776572-00
SCXI-1120 8-channel isolated analog input	776572-20
SCXI-1121 4-channel isolated transducer amplifier with excitation	776572-21
SCXI-1140 8-channel simultaneously sampling differential amplifier	776572-40
SCXI-1180 feedthrough panel	776572-80
SCXI-1181 breadboard	776572-81
AMUX-64T analog multiplexer board	
with 0.2-m ribbon cable	776366-02
with 0.5-m ribbon cable	776366-05
with 1.0-m ribbon cable	776366-10
with 2.0-m ribbon cable	776366-20

(continues)

Equipment	Part Number
SC-2050 cable adapter board for signal conditioning with 50-conductor cable	
0.5 m	776335-00
1.0 m	776335-10
SC-2060 optically isolated digital input board with 26-conductor cable	
0.2 m	776336-00
0.4 m	776336-10
SC-2061 optically isolated digital output board with 26-conductor cable	
0.2 m	776336-01
0.4 m	776336-11
SC-2062 electromechanical relay digital control board with 26-conductor cable	
0.2 m	776336-02
0.4 m	776336-12
SC-2070 general-purpose termination breadboard with 50-conductor cable	
0.5 m	776358-00
1.0 m	776358-10
BNC-2080 BNC adapter board with 50-conductor cable	
0.5 m	776579-05
1.0 m	776579-10
Digital signal conditioning modules	
SSR Series mounting rack and 0.4-m cable	
8-channel backplane with SC-205X cable	776290-18
5B Series signal conditioning backplane with 1.0-m cable	776291-01

Unpacking

Your NB-MIO-16X is shipped in an antistatic plastic bag to prevent electrostatic damage to the board. Several components on the board may be damaged by electrostatic discharge. To avoid such damage in handling the board, take the following precautions:

- Touch the plastic bag to a metal part of your computer before removing the board from the bag.
- Remove the board from the bag and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.

Chapter 2
Configuration and Installation

This chapter explains board configuration, installation of the NB-MIO-16X in the Macintosh NuBus computer, signal connections to the NB-MIO-16X, and cable wiring.

Board Configuration

The NB-MIO-16X has 10 jumpers that determine the analog input and analog output configurations of the board. The jumpers are shown in the parts locator diagram in Figure 2-1. Jumpers W3, W5, and W8 configure the analog input circuitry. Jumpers W1, W2, W4, W6, W7, W9, and W10 configure the analog output circuitry.

Jumper Settings

The NB-MIO-16X is shipped from the factory with the following configuration:

- Differential analog input (8 channels)
- 10 V input range
- ±10 V output range with internal 10 V reference selected
- Two's complement DAC input mode

Table 2-1 lists all the available jumper configurations for the NB-MIO-16X with the factory settings noted.

Table 2-1. Jumper Settings

	Configuration	Jumper Settings
Output CH0 Reference	Internal 10 V (factory setting) Internal 5 V External	**W2:** B-C **W4:** B-C **W2:** B-C **W4:** A-B **W2:** A-B
Output CH1 Reference	Internal 10 V (factory setting) Internal 5 V External	**W1:** B-C **W4:** B-C **W1:** B-C **W4:** A-B **W1:** A-B
Input Range	0 to 10 V or -10 to +10 V (factory setting) 0 to 5V or -5 to +5 V	**W8:** B-C **W8:** A-B
Input Mode	Differential (DIFF) (factory setting) Non-referenced single-ended (NRSE) Ground-referenced single-ended (RSE)	**W3:** A-C, B-D, E-F **W5:** A-B **W3:** A-B, C-E, G-H **W5:** B-C **W3:** A-B, C-D, G-H **W5:** B-C
Output CH0 Polarity	Unipolar Bipolar (factory setting)	**W6:** B-C **W6:** A-B
Output CH1 Polarity	Unipolar Bipolar (factory setting)	**W7:** B-C **W7:** A-B
DAC0 Input Mode	Straight binary mode Two's complement mode (factory setting)	**W9:** A-B **W9:** B-C
DAC1 Input Mode	Straight binary mode Two's complement mode (factory setting)	**W10:** A-B **W10:** B-C

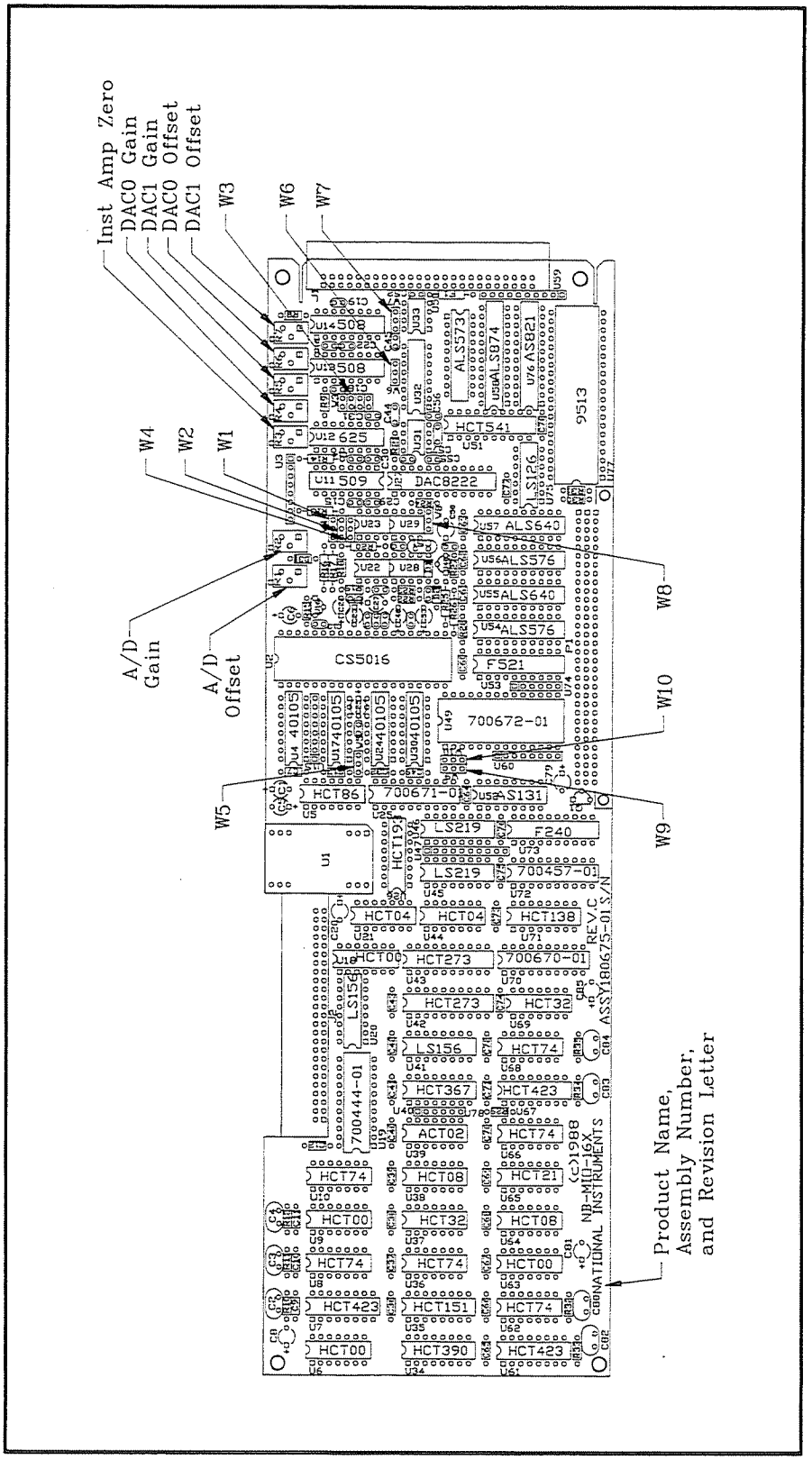


Figure 2-1. Parts Locator Diagram

Analog Input Configuration

You can select different analog input configurations by using the jumper settings shown in Table 2-1. The following paragraphs describe each of the analog input categories in detail. In the configuration illustrations throughout this chapter, the black bars show where to place jumpers.

Input Mode

The NB-MIO-16X offers three different input modes–referenced single-ended (RSE) input, non-referenced single-ended (NRSE) input, and differential (DIFF) input. The single-ended input configurations use 16 channels. The DIFF input configuration uses 8 channels. These configurations are described in Table 2-2.

Table 2-2. Input Configurations Available for the NB-MIO-16X

Configuration	Description
DIFF	Differential configuration. Provides 8 differential inputs with the negative (-) input of the instrumentation amplifier tied to the multiplexer output of Channels 8 through 15.
RSE	Referenced Single-Ended configuration. Provides 16 single-ended inputs with the negative (-) input of the instrumentation amplifier referenced to analog ground.
NRSE	Non-Referenced Single-Ended configuration. Provides 16 single-ended inputs with the negative (-) input of the instrumentation amplifier tied to AISENSE and *not* connected to ground.

While reading the following paragraphs, you may find it helpful to refer to *Analog Input Signal Connections* later in this chapter, which contains diagrams showing the signal paths for the three configurations.

DIFF Input (8 Channels, Factory Setting)

DIFF input means that each input signal has its own reference, and the difference between each signal and its reference is measured. The signal and its reference are each assigned an input channel. With this input configuration, the NB-MIO-16X can monitor eight different analog input signals. You select the DIFF input configuration by setting jumpers W3 and W5 as follows:

W3:

A - C Jumper is placed in standby position. (A and C are always connected together inside the board.)

B - D AI SENSE is tied to the instrumentation amplifier signal ground.

E - F Channels 0 through 7 are tied to the positive (+) input of the instrumentation amplifier. Channels 8 through 15 are tied to the negative (-) input of the instrumentation amplifier.

W5:

A - B Multiplexer is configured to control eight input channels.

This configuration is shown in Figure 2-2.

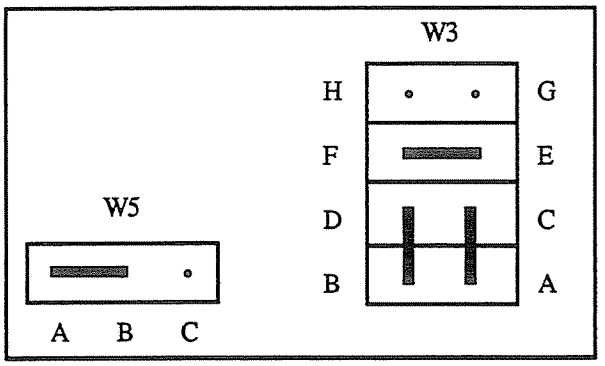


Figure 2-2. DIFF Input Configuration (Factory Setting)

Considerations for using the DIFF configuration are discussed under *Signal Connections* later in this chapter. Figure 2-17 shows a schematic diagram of this configuration.

RSE Input (16 Channels)

RSE input means that all input signals are referenced to a common ground point that is also tied to the analog input ground of the NB-MIO-16X board. The negative (-) input of the differential input amplifier is tied to analog ground. This configuration is useful when measuring floating signal sources. See *Types of Signal Sources* later in this chapter. With this input configuration, the NB-MIO-16X can monitor 16 different analog input signals. You select the RSE input configuration by setting jumpers W3 and W5 as follows:

W3:

A - B AI SENSE is tied to the negative (-) input of the instrumentation amplifier.

C - D The negative (-) input of the instrumentation amplifier is tied to the instrumentation amplifier signal ground.

G - H Multiplexer outputs are tied together into the positive (+) input of the instrumentation amplifier.

W5:

B - C Multiplexer control is configured for 16 input channels.

This configuration is shown in Figure 2-3.

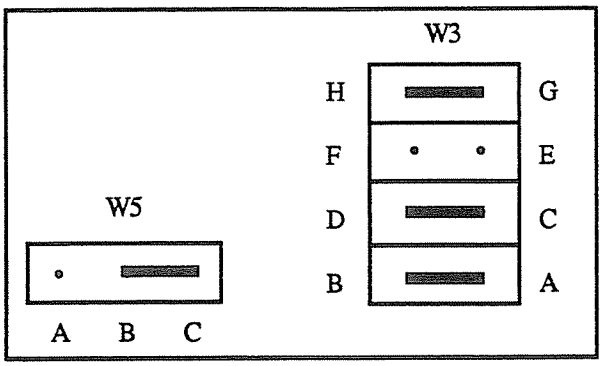


Figure 2-3. RSE Input Configuration

Considerations for using the RSE configuration are discussed under *Signal Connections* later in this chapter. Figure 2-18 shows a schematic diagram of this configuration.

NRSE Input (16 Channels)

NRSE input means that all input signals are referenced to the same common mode voltage but that this common mode voltage is allowed to float with respect to the analog ground of the NB-MIO-16X board. This common mode voltage is subsequently subtracted out by the input instrumentation amplifier. This configuration is useful when measuring ground-referenced signal sources. See *Types of Signal Sources* later in this chapter. With this input configuration, the NB-MIO-16X can measure 16 different analog input signals having the same ground reference. You select the NRSE input configuration by setting jumpers W3 and W5 as follows:

W3:

- A - B AI SENSE is tied to the negative (-) input of the instrumentation amplifier.
- C - E Jumper is placed in standby position. (C and E are always connected together inside the board.)
- G - H Multiplexer outputs are tied together into the positive (+) input of the instrumentation amplifier.

W5:

- B - C Multiplexer control is configured for 16 input channels.

This configuration is shown in Figure 2-4.

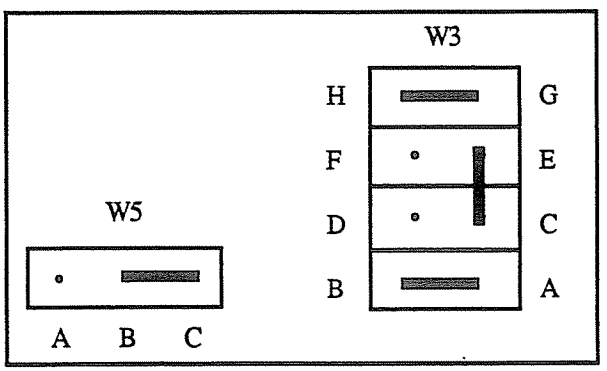


Figure 2-4. NRSE Input Configuration

Considerations for using the NRSE configuration are discussed under *Signal Connections* later in this chapter. Figure 2-19 shows a schematic diagram of this configuration.

Input Polarity and Input Range

The NB-MIO-16X has four different input ranges. You select the NB-MIO-16X input polarity and input range by setting jumper W8 and the BP*/UP bit in Command Register 1 (described in Chapter 4, *Programming*), as follows:

	5 V Range	10 V Range
Bipolar	Set W8 to A-B BP*/UP Cleared	Set W8 to B-C BP*/UP Cleared
Unipolar	Set W8 to A-B BP*/UP Set	Set W8 to B-C BP*/UP Set

If you are using NI-DAQ, the BP*/UP bit is automatically set to the correct value when you specify the input range and polarity in the AI_Config call.

Figures 2-5 and 2-6 show the jumper positions for the 5 V (0 to +5 V or -5 to +5 V) and 10 V (0 to +10 V or -10 V to +10 V) input range configurations, respectively.

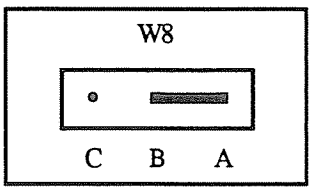


Figure 2-5. 5 V Input Configuration

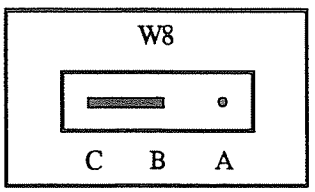


Figure 2-6. 10 V Input Configuration (Factory Setting)

Considerations for Selecting Input Ranges

Input polarity/range selection depends on the expected input range of the incoming signal. A large input range can accommodate a large signal variation but sacrifices voltage resolution. Choosing a smaller input range increases voltage resolution but may result in the input signal going out of range. For best results, the input range should be matched as closely as possible to the expected range of the input signal. For example, if the input signal is guaranteed to never go negative (below 0 V), a unipolar input is best. However, if the signal does go negative, inaccurate readings will occur and so a bipolar input range would be appropriate.

Software-programmable gain on the NB-MIO-16X increases overall flexibility by matching input signal ranges to those accommodated by the NB-MIO-16X ADC. The NB-MIO-16XH board has gains of 1, 2, 4, and 8 and is suited for high-level signals near the range of the ADC. The NB-MIO-16XL board is designed to measure low-level signals and has gains of 1, 10, 100, and 500. With the proper gain setting, the full resolution of the ADC can be used to measure the input signal. Table 2-3 shows the overall input range and precision according to the input range configuration and gain used.

Table 2-3. Actual Range and Measurement Precision Versus Input Range Selection and Gain

Range Configuration	Gain	Actual Input Range	Precision*
0 to +5V	1	0 to +5 V	76.3 µV
	2	0 to +2.5 V	38.1 µV
	4	0 to +1.25 V	19.1 µV
	8	0 to +0.625 V	9.54 µV
	10	0 to +0.5 V	7.63 µV
	100	0 to +0.05 V	763 nV
	500	0 to +10 mV	153 nV
0 to +10V	1	0 to +10 V	153 µV
	2	0 to +5 V	76.3 µV
	4	0 to +2.5 V	38.1 µV
	8	0 to +1.25 V	19.1 µV
	10	0 to +1 V	15.3 µV
	100	0 to +0.1 V	1.53 µV
	500	0 to +20 mV	305 nV
-5 to +5V	1	-5 to +5 V	153 µV
	2	-2.5 to +2.5 V	76.3 µV
	4	-1.25 to +1.25 V	38.1 µV
	8	-0.625 to +0.625 V	19.1 µV
	10	-0.5 to +0.5 V	15.3 µV
	500	-10 mV to +10 mV	305 nV
-10 to +10V	1	-10 to +10 V	305 µV
	2	-5 to +5 V	153 µV
	4	-2.5 to +2.5 V	76.3 µV
	8	-1.25 to +1.25 V	38.1 µV
	10	-1 to +1 V	30.5 µV
	100	-0.1 to +0.1 V	3.05 µV
	500	-20 mV to +20 mV	610 nV

* The value of 1 least significant bit (1 LSB) of the 16-bit ADC, that is, the voltage increment corresponding to a change of one count in the ADC 16-bit count.

Analog Output Configuration

You can select different analog output configurations by using the jumper settings shown in Table 2-1. The following paragraphs describe each of the analog output configurations in detail.

External and Internal Reference

Each analog output channel can be connected to the NB-MIO-16X internal reference of 10 V or to the external reference signal connected to the EXTREF pin (pin 22) on the I/O connector. Both channels need not be configured the same way, although only one of the internal references (5 V or 10 V) can be used at a time. (You cannot, for example, use the internal 10 V reference on Channel 0 and the internal 5 V reference on Channel 1.)

External Reference Selection

You select the external reference signal for each analog output channel by setting the following jumpers:

Analog Output Channel 0:	W2	A - B	External reference signal connected to DAC 0 reference input.
Analog Output Channel 1:	W1	A - B	External reference signal connected to DAC 1 reference input.

This configuration is shown in Figure 2-7.

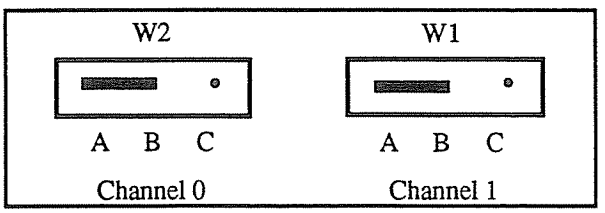


Figure 2-7. External Reference Configuration

Internal Reference Selection (Factory Setting)

You select the onboard reference for each analog output channel by setting the following jumpers:

Analog Output Channel 0:	W2	B - C	Onboard reference connected to DAC 0 reference input.
Analog Output Channel 1:	W1	B - C	Onboard reference connected to DAC 1 reference input.

This configuration is shown in Figure 2-8.

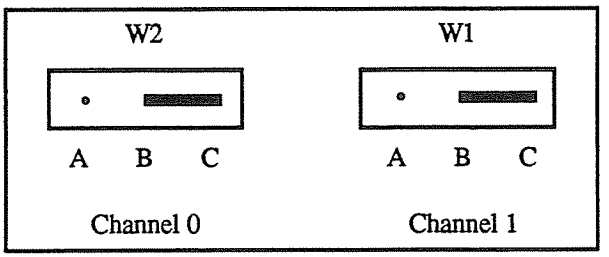


Figure 2-8. Internal Reference Configuration (Factory Setting)

Both channels must use the same internal reference. You select which internal reference to use by setting W4 as follows:

5 V internal reference: W4 A - B

10 V internal reference: W4 B - C (factory setting)

These configurations are shown in Figure 2-9.

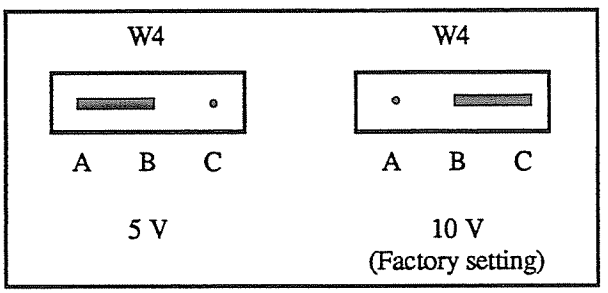


Figure 2-9. Reference Choice Configurations

Analog Output Polarity Selection

Each analog output channel can be configured for either unipolar or bipolar output. A unipolar configuration has a range of 0 to V_{ref} at the analog output. A bipolar configuration has a range of $-V_{ref}$ to V_{ref} at the analog output. V_{ref} is the voltage reference used by the DACs in the analog output circuitry and can either be the onboard reference or an externally supplied reference. Both channels need not be configured the same way; however, at the factory both channels are configured for bipolar output.

Bipolar Output Selection (Factory Setting)

You select the bipolar output configuration for each analog output channel by setting the following jumpers:

Analog Output Channel 0: W6 A - B

Analog Output Channel 1: W7 A - B

This configuration is shown in Figure 2-10.

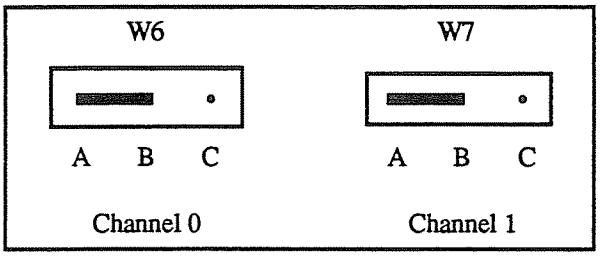


Figure 2-10. Bipolar Output Configuration (Factory Setting)

When you use the bipolar configuration, you need to select whether to write straight binary or two's complement to the DAC. In straight binary mode, data values written to the analog output channel range from 0 to 4095 decimal (0 to 0FFF hex). In two's complement mode, data values written to the the analog output channel range from -2048 to 2047 decimal (F800 to 07FF hex).

Straight Binary Mode

The data value written to each analog output channel is interpreted as a straight binary number when the following jumpers are set:

Analog Output Straight Binary for Channel 0: W9 A - B

Analog Output Straight Binary for Channel 1: W10 A - B

This configuration is shown in Figure 2-11.

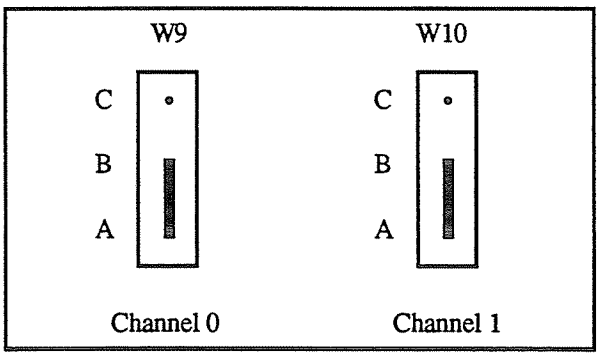


Figure 2-11. Straight Binary Mode

Two's Complement Mode (Factory Setting)

The data value written to each analog output channel is interpreted as a two's complement number when the following jumpers are set:

Analog Output Two's Complement for Channel 0: W9 B - C

Analog Output Two's Complement for Channel 1: W10 B - C

This configuration is shown in Figure 2-12.

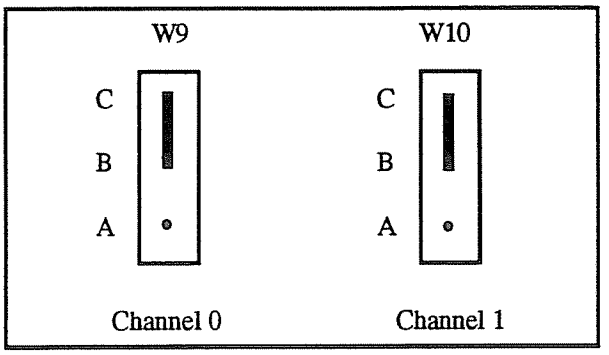


Figure 2-12. Two's Complement Mode (Factory Setting)

Unipolar Output Selection

You select the unipolar output configuration for each analog output channel by setting the following jumpers:

Analog Output Channel 0:	W6	B - C
Analog Output Straight Binary for Channel 0:	W9	A - B
Analog Output Channel 1:	W7	B - C
Analog Output Straight Binary for Channel 1:	W10	A - B

Notice that the straight binary format should be used when in unipolar output mode.

This configuration is shown in Figure 2-13.

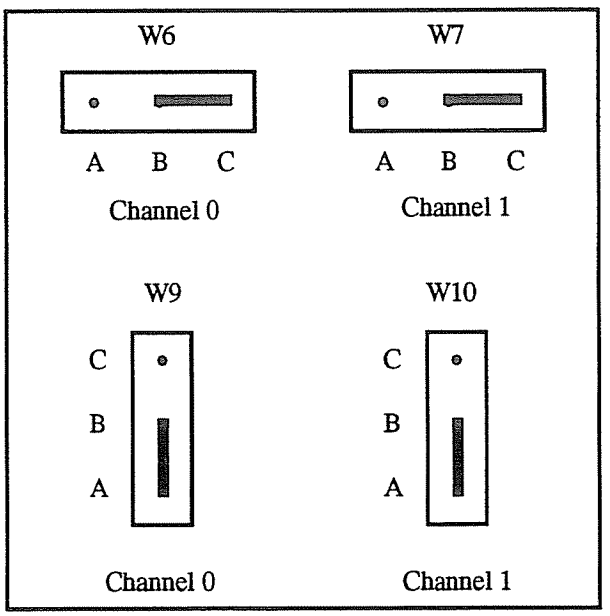


Figure 2-13. Unipolar Output Configuration

Note: If you are using a software package such as NI-DAQ or LabVIEW 2, you may need to reconfigure your software to reflect any changes in jumper or switch settings.

Installation

Within the manual shipped with your Macintosh computer, read the instructions for installing the video card in the main unit. These instructions can be used as a universal board installation guide.

Read the entire installation procedure before installing the NB-MIO-16X into the Macintosh. You can install the NB-MIO-16X in any of the Macintosh NuBus slots. However, to achieve best noise performance, you should leave as much room as possible between the NB-MIO-16X and other boards and hardware. For instance, if the video board is in Slot 1 and the NB-MIO-16X is the only other board in the computer, you should install it in Slot 3 or 4.

Signal Connections

This section describes input and output signal connections to the NB-MIO-16X board via the NB-MIO-16X I/O connector. This section includes connection instructions and some specifications for the signals provided on the NB-MIO-16X I/O connector.

Warning: Connections that exceed any of the maximum ratings of input or output signals on the NB-MIO-16X may result in damage to the NB-MIO-16X board and to the Macintosh computer. Maximum input ratings for each signal are given in this section under the discussion of that signal. National Instruments is not liable for any damages resulting from any such signal connections.

The pinout for the NB-MIO-16X I/O connector is shown in Figure 2-14.

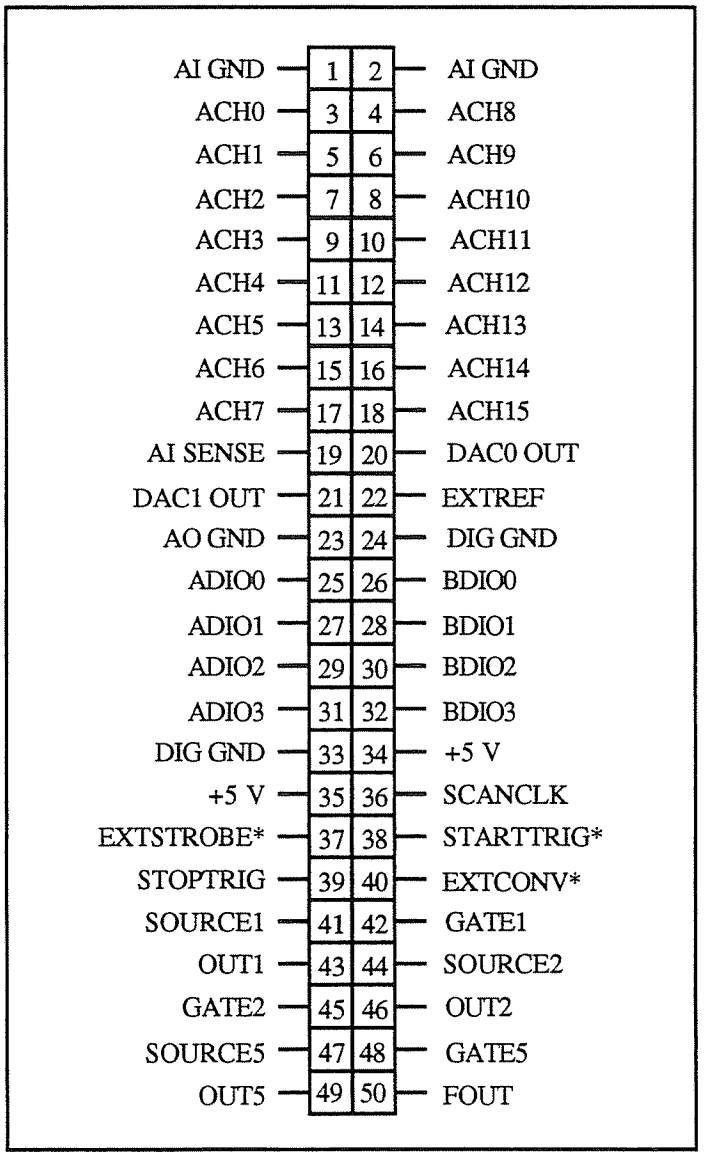


Figure 2-14. NB-MIO-16X I/O Connector

The signals on the connector can be classified as analog input signals, analog output signals, digital I/O signals, digital power connections, and timing I/O signals. The following sections have signal connection guidelines for each of these groups.

Analog Input Signal Connections

Pins 1 through 19 of the I/O connector are analog input signal pins. Pins 1 and 2 are AI GND signal pins. AI GND is an analog input common signal that is routed directly to the ground tie point on the NB-MIO-16X. These pins can be used for a general analog power ground tie point to the NB-MIO-16X if necessary. Pin 19 is the AI SENSE pin. In NRSE mode, this pin is connected internally to the negative (-) input of the NB-MIO-16X instrumentation amplifier. In DIFF mode, this signal is connected to the reference ground at the output of the instrumentation amplifier.

Pins 3 through 18 are ACH<15..0> signal pins. These pins are tied to the 16 analog input channels of the NB-MIO-16X. In single-ended mode, signals connected to ACH<15..0> are routed to the positive (+) input of the NB-MIO-16X instrumentation amplifier. In DIFF mode, signals connected to ACH<7..0> are routed to the positive (+) input of the NB-MIO-16X instrumentation amplifier, and signals connected to ACH<15..8> are routed to the negative (-) input of the NB-MIO-16X instrumentation amplifier.

The following input ranges and maximum ratings apply to inputs ACH<15..0>:

Differential Input Range	±10 V
Common Mode Input Range	±7 V with respect to NB-MIO-16X AGND
Input Range	±12 V with respect to NB-MIO-16X AGND
Maximum Input Voltage Rating	±20 V for NB-MIO-16X board powered off ±35 V for NB-MIO-16X board powered on

Warning: Exceeding the differential and common mode input ranges will result in distorted input signals. Exceeding the maximum input voltage rating may result in damage to the NB-MIO-16X board and to the Macintosh computer. National Instruments is not liable for any damages resulting from any such signal connections.

Connection of analog input signals to the NB-MIO-16X depends on the configuration of the NB-MIO-16X analog input circuitry and the type of input signal source. The different NB-MIO-16X configurations allow the NB-MIO-16X instrumentation amplifier to be used in different ways. Figure 2-15 shows a diagram of the NB-MIO-16X instrumentation amplifier.

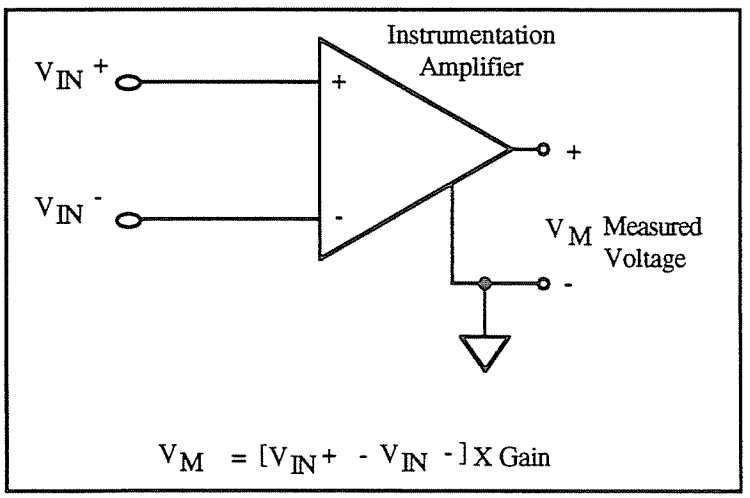


Figure 2-15. NB-MIO-16X Instrumentation Amplifier

The NB-MIO-16X instrumentation amplifier applies gain, common-mode voltage rejection, and high-input impedance to the analog input signals connected to the NB-MIO-16X board. Signals are routed to the positive (+) and negative (-) inputs of the instrumentation amplifier through input multiplexers on the NB-MIO-16X. The instrumentation amplifier converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the

amplifier. The amplifier output voltage is referenced to the NB-MIO-16X ground. The NB-MIO-16X ADC measures this output voltage when it performs A/D conversions.

All signals must be referenced to ground somewhere, either at the source device or at the NB-MIO-16X. If you have a floating source, you must use a ground-referenced input connection at the NB-MIO-16X. If you have a grounded source, you must use a non-referenced input connection at the NB-MIO-16X.

The following sections have connection guidelines for single-ended and differential configurations and for grounded and floating signal sources.

Types of Signal Sources

When configuring the input mode of the NB-MIO-16X and making signal connections, you must first determine whether the signal source is floating or ground-referenced. These two types of signals are described in the following sections.

Floating Signal Sources

A floating signal source is one that is not connected in any way to the building ground system but rather has an isolated ground reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. The ground reference of a floating signal must be tied to the NB-MIO-16X analog input ground in order to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies or appears to float. An instrument or device that provides an isolated output falls into the floating signal source category.

Ground-Referenced Signal Sources

A ground-referenced signal source is one that is connected in some way to the building system ground and is therefore already connected to a common ground point with respect to the NB-MIO-16X board, assuming that the Macintosh is plugged into the same power system. Non-isolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 mV and 100 mV, but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is measured improperly, this difference may show up as an error in the measurement. The following connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Input Configurations

The NB-MIO-16X can be configured for one of three input modes: NRSE, RSE, or DIFF. The following sections discuss the use of single-ended and differential measurements, and considerations for measuring both floating and ground-referenced signal sources. Table 2-4 summarizes the recommended input configuration for both types of signal sources.

Table 2-4. Recommended Input Configurations for Ground-Referenced and Floating Signal Sources

Type of Signal	Recommended Input Configuration
Ground-Referenced (non-isolated outputs, plug-in instruments)	DIFF NRSE
Floating (batteries, thermocouples, isolated outputs)	DIFF with bias resistors RSE

Differential Connection Considerations (DIFF Configuration)

Differential connections are those in which each NB-MIO-16X analog input signals has its own reference signal or signal return path. These connections are available when the NB-MIO-16X is configured in the DIFF mode. Each input signal is tied to the positive (+) input of the instrumentation amplifier, and its reference signal, or return, is tied to the negative (-) input of the instrumentation amplifier.

When the NB-MIO-16X is configured for DIFF input, each signal uses two of the multiplexer inputs–one for the signal and one for its reference signal. Therefore, only eight analog input channels are available when using the DIFF configuration. The DIFF input configuration should be used when any of the following conditions are present:

- Input signals are low-level (less than 1 V).
- Leads connecting the signals to the NB-MIO-16X are greater than 15 ft.
- Any of the input signals requires a separate ground reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce induced noise and increase common mode signal and noise rejection. They also permit input signals to float within the common mode limits of the input instrumentation amplifier.

Differential Connections for Grounded Signal Sources

Figure 2-16 shows how to connect a ground-referenced signal source to an NB-MIO-16X board configured for DIFF input. Configuration instructions are included under *Analog Input Configuration* earlier in this chapter.

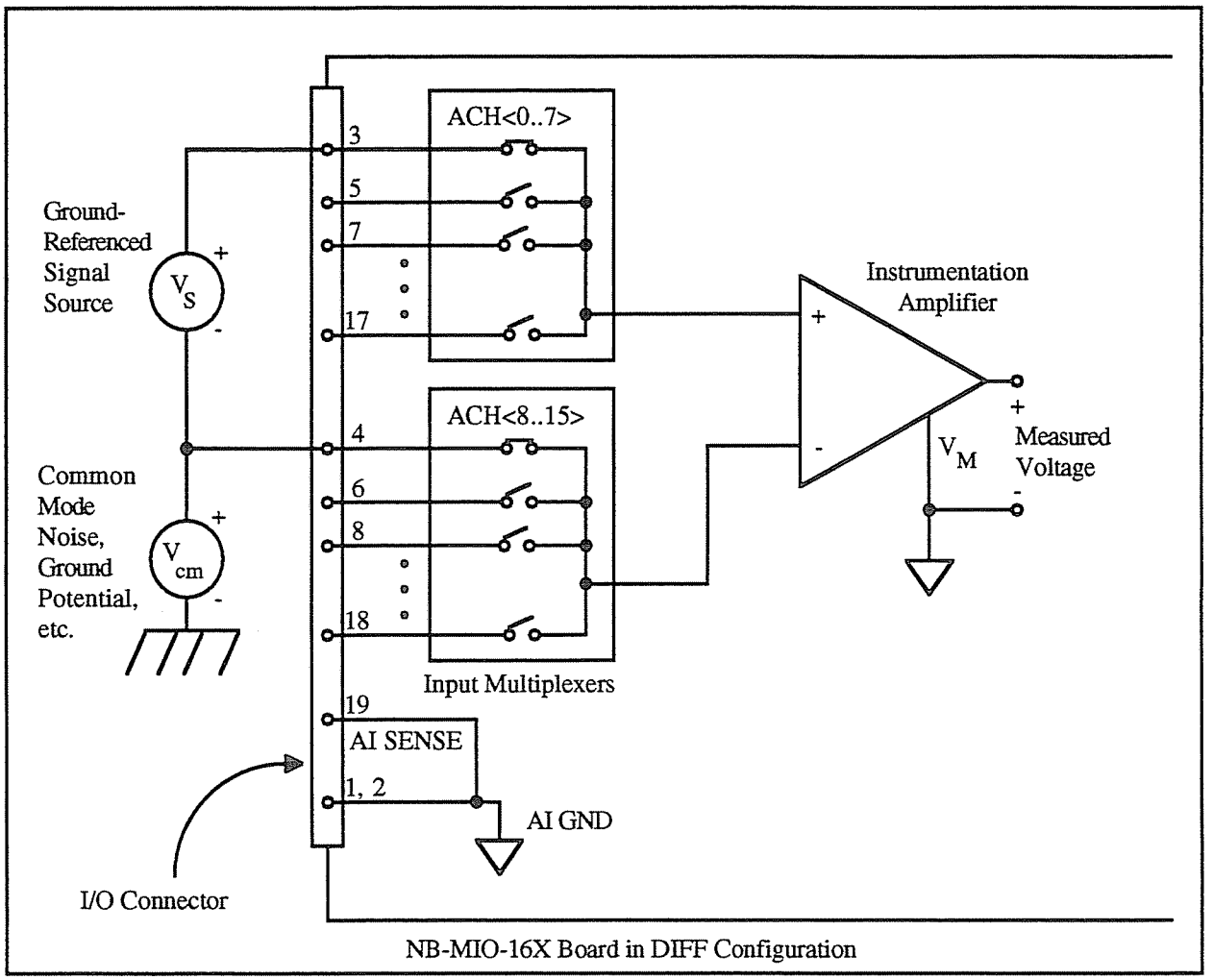


Figure 2-16. Differential Input Connections for Grounded Signal Sources

With this type of connection, the instrumentation amplifier rejects both the common mode noise in the signal and the ground potential difference between the signal source and the NB-MIO-16X ground (shown as V_{cm} in Figure 2-16).

Differential Connections for Floating Signal Sources

Figure 2-17 shows how to connect a floating signal source to an NB-MIO-16X board configured for DIFF input. Configuration instructions are described under *Analog Input Configuration* earlier in this chapter.

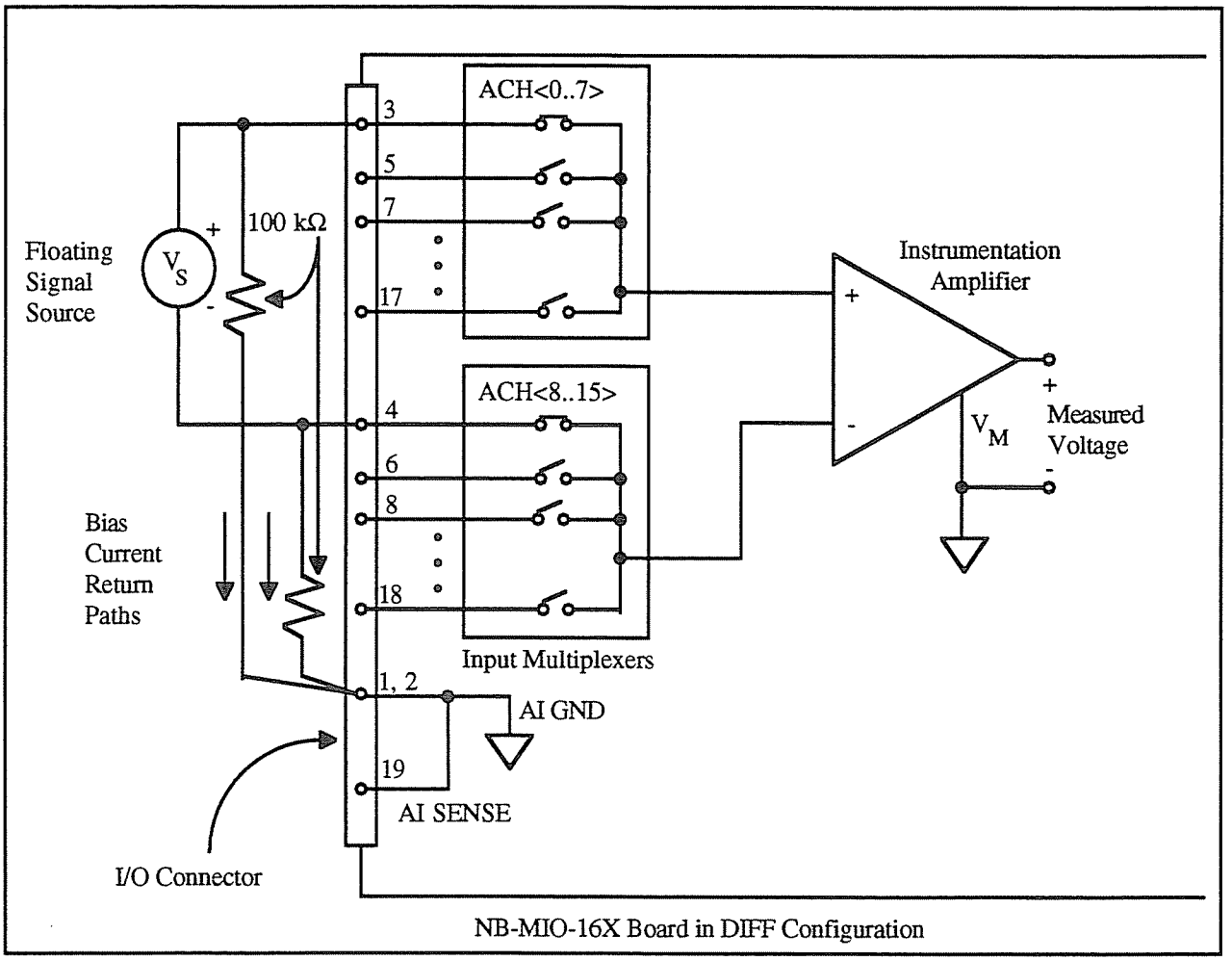


Figure 2-17. Differential Input Connections for Floating Sources

The 100 kΩ resistors shown in Figure 2-17 create a return path to ground for the bias currents of the instrumentation amplifier. If a return path is not provided, the instrumentation amplifier bias currents charge up stray capacitances, resulting in uncontrollable drift and possible saturation in the amplifier. Typically, values from 10 kΩ to 100 kΩ are used.

A resistor from each input to ground, as shown in Figure 2-17, provides bias current return paths for an AC-coupled input signal. This solution, although necessary for AC-coupled signals, lowers the input impedance of the analog input channel. In addition, the input offset current of the instrumentation amplifier contributes a DC offset voltage at the input. The amplifier has a maximum input offset current of ±15 nA and a typical offset current drift of ±20 pA/°C. Multiplied by the 100 kΩ resistor, this current contributes a maximum offset voltage of 1.5 mV and a typical offset voltage drift of 2 µV/°C at the input. Keep this in mind when you observe DC offsets with AC-coupled inputs.

If the input signal is DC-coupled, then only the resistor connecting the negative (-) signal input to ground is needed. This connection does not lower the input impedance of the analog input channel or cause an offset at the input.

Single-Ended Connection Considerations

Single-ended connections are those in which all NB-MIO-16X analog input signals are referenced to one common ground. The input signals are tied to the positive (+) input of the instrumentation amplifier, and their common ground point is tied to its negative (-) input.

When the NB-MIO-16X is configured for single-ended input (NRSE or RSE), 16 analog input channels are available. Single-ended input connections can be used when the following criteria are met by all input signals:

- Input signals are high-level (greater than 1 V).
- Leads connecting the signals to the NB-MIO-16X are less than 15 ft.
- All input signals share a common reference signal (at the source).

If any of the above criteria is not met, using DIFF input configuration is recommended.

The NB-MIO-16X can be jumper configured for two different types of single-ended connections–RSE configuration and NRSE configuration. The RSE configuration is used for floating signal sources. In this case, the NB-MIO-16X provides the reference ground point for the external signal. The NRSE configuration is used for ground-referenced signal sources. In this case, the external signal supplies its own reference ground point and the NB-MIO-16X should not supply one.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 2-18 shows how to connect a floating signal source to an NB-MIO-16X board configured for single-ended input. The NB-MIO-16X analog input circuitry must be configured for RSE input to make these types of connections. Configuration instructions are included under *Analog Input Configuration* earlier in this chapter.

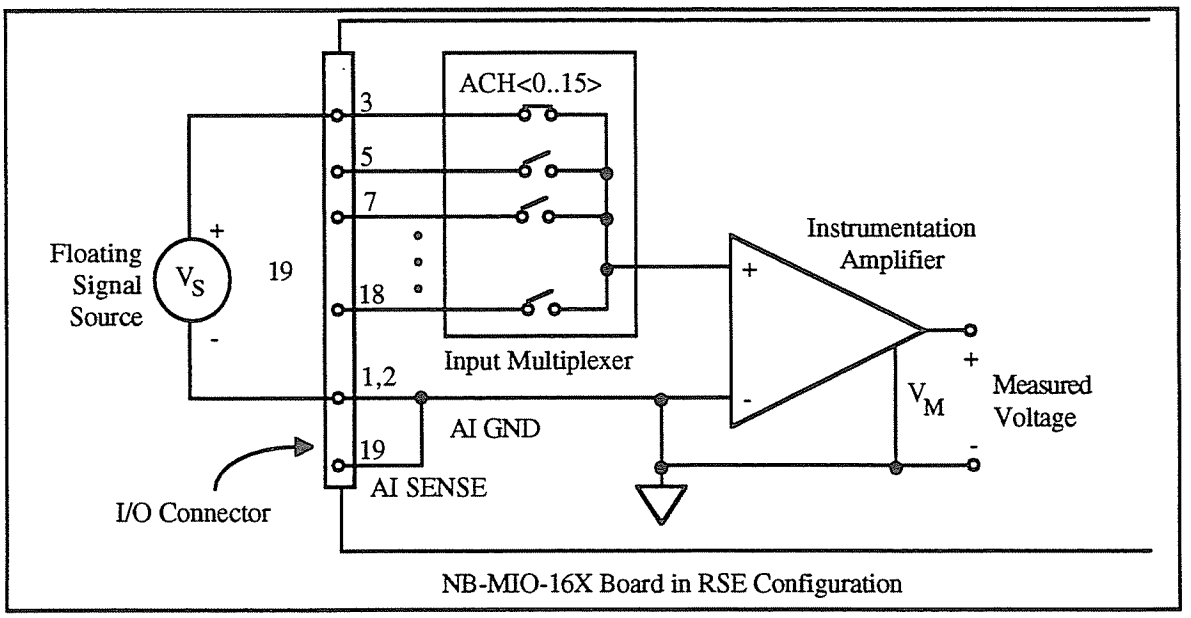


Figure 2-18. Single-Ended Input Connections for Floating Signal Sources

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

If a grounded signal source is to be measured with a single-ended configuration, then the NB-MIO-16X must be configured in the NRSE input configuration. The signal is connected to the positive (+) input of the NB-MIO-16X instrumentation amplifier and the signal local ground reference is connected to the negative (-) input of the NB-MIO-16X instrumentation amplifier. The ground point of the signal should therefore be connected to the AI SENSE pin. Any potential difference between the NB-MIO-16X ground and the signal ground appears as a common mode signal at both the positive (+) and negative (-) inputs of the instrumentation amplifier, and this difference is rejected by the amplifier. On the other hand, if the input circuitry of the NB-MIO-16X is referenced to ground, such as in the RSE configuration, this difference in ground potentials appears as an error in the measured voltage.

Figure 2-19 shows how to connect a grounded signal source to an NB-MIO-16X board configured in the NRSE configuration. Configuration instructions are included under *Analog Input Configuration* earlier in this chapter.

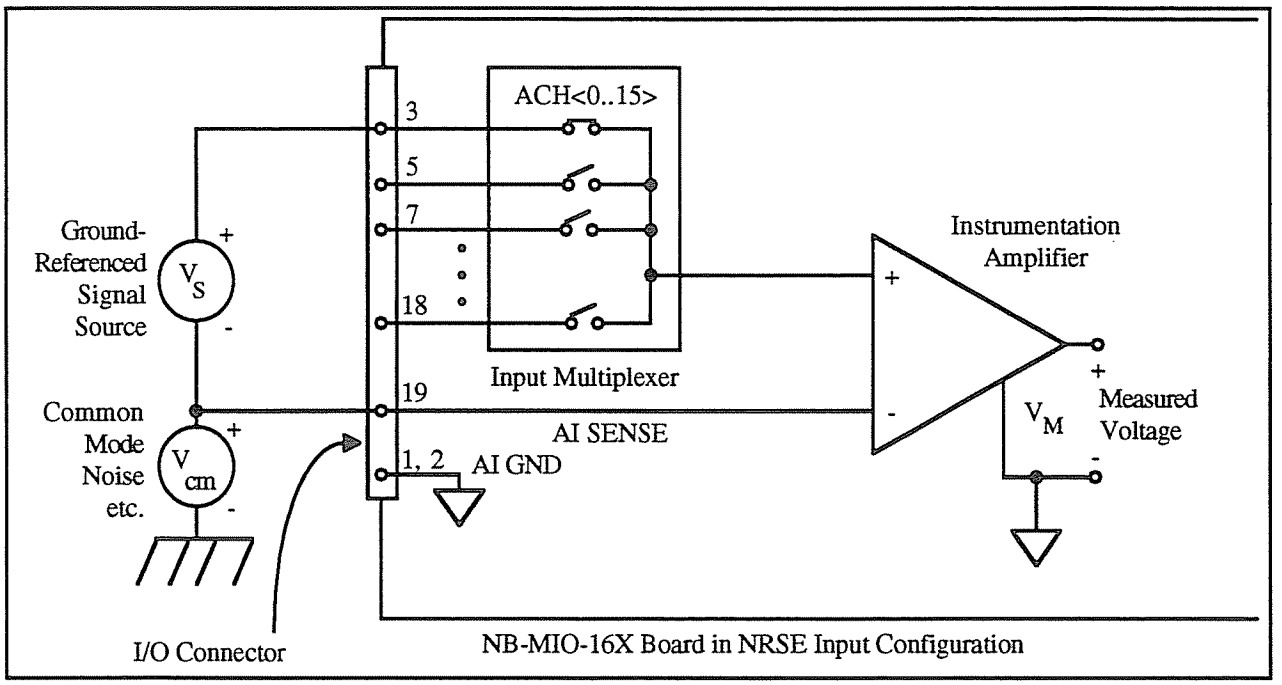


Figure 2-19. Single-Ended Input Connections for Grounded Signal Sources

Common Mode Signal Rejection Considerations

Figures 2-16 and 2-19 show connections for signal sources that are already referenced to some ground point with respect to the NB-MIO-16X. In these cases, the instrumentation amplifier can reject any voltage due to ground potential differences between the signal source and the NB-MIO-16X. In addition, with differential input connections, the instrumentation amplifier can reject common mode noise pickup in the leads connecting the signal sources to the NB-MIO-16X.

The common mode input range of the NB-MIO-16X instrumentation amplifier is defined as the magnitude of the greatest common mode signal that can be rejected.

The common mode input range for the NB-MIO-16X depends on the size of the differential input signal ($V_{diff} = V^+_{in} - V^-_{in}$) and the gain setting of the instrumentation amplifier. The exact formula for the allowed common mode input range is as follows:

$$V_{cm\text{-}max} = \pm (12V - \frac{V_{diff} * Gain}{2})$$

where the maximum value for V_{diff} is as follows:

±10 V range	$V_{diff\text{-}max} = \pm 10$ V
0 to +10 V range	$V_{diff\text{-}max} = 10$ V
±5 V range	$V_{diff\text{-}max} = \pm 5$ V

For example, for a differential voltage as large as 20 mV and a gain of 500, the largest common mode voltage that can be rejected is ±7 V. However, if the differential signal is 10 mV with a gain of 500, ±9.5 V common mode voltage can be rejected.

The common mode voltage is measured with respect to the NB-MIO-16X ground and can be calculated by the following formula:

$$V_{cm\text{-}actual} = \frac{(V^+_{in} + V^-_{in})}{2}$$

where V^+_{in} is the signal at the positive (+) input of the instrumentation amplifier and V^-_{in} is the signal at the negative (-) input of the instrumentation amplifier.

If the input signal common mode range exceeds ±7 V with respect to the NB-MIO-16X ground, you need to limit the amount of floating that occurs between the signal ground and the NB-MIO-16X ground.

Analog Output Signal Connections

Pins 20 through 23 of the I/O connector are analog output signal pins.

Pins 20 and 21 are the DAC0 OUT and DAC1 OUT signals pins. DAC0 OUT is the voltage output signal for analog output channel 0. DAC1 OUT is the voltage output signal for analog output channel 1.

Pin 22, EXTREF, is the external reference input for both analog output channels. Each analog output channel must be configured individually for external reference selection in order for the signal applied at the external reference input to be used by that channel. Analog output configuration instructions are described under *Analog Output Configuration* earlier in this chapter.

The following ranges and ratings apply to the EXTREF input:

Useful input voltage range:	±10 V peak with respect to AO GND
Absolute maximum ratings:	±25 V peak with respect to AO GND

Pin 23, AO GND, is the ground reference point for both analog output channels and for the external reference signal.

Figure 2-20 shows how to make analog output connections and the external reference input connection to the NB-MIO-16X board. If neither channel is configured to use an external reference signal, do not connect anything to the EXTREF pin.

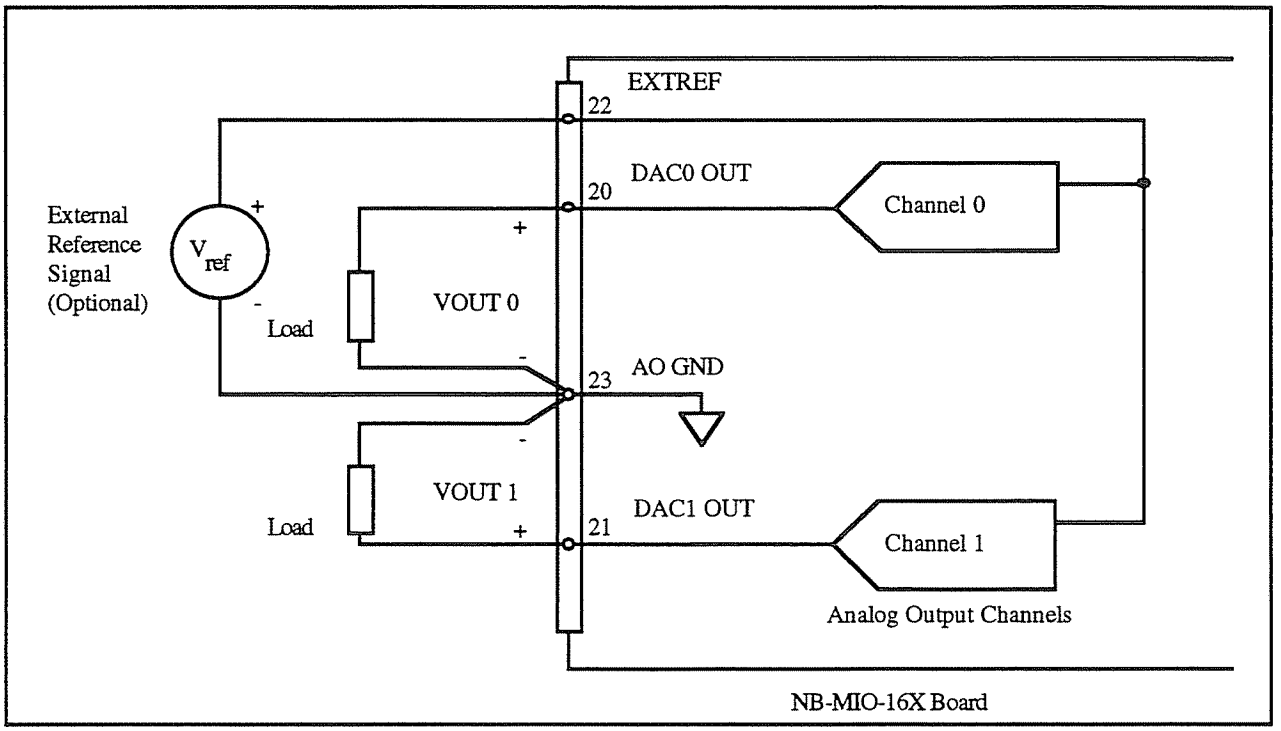


Figure 2-20. Analog Output Connections

The external reference signal can be either a DC or an AC signal. This reference signal is multiplied by the DAC code to generate the output voltage.

Digital I/O Signal Connections

Pins 24 through 32 of the I/O connector are digital I/O signal pins.

Pins 25, 27, 29, and 31 are connected to the digital lines ADIO<3:0> for digital I/O port A. Pins 26, 28, 30, and 32 are connected to the digital lines BDIO<3:0> for digital I/O port B. Pin 24, DIG GND, is the digital ground pin for both digital I/O ports. Ports A and B can be programmed individually to be inputs or outputs.

The following specifications and ratings apply to the digital I/O lines:

Absolute maximum voltage input rating: 5.5 V with respect to DIG GND

Digital Input Specifications (referenced to DIG GND):

V_{IH} input logic high voltage:	2 V minimum
V_{IL} input logic low voltage:	0.8 V maximum
I_{IH} input current load, logic high input voltage:	40 µA maximum
I_{IL} input current load, logic low input voltage:	-120 µA maximum

Digital Output Specifications (referenced to DIG GND):

V_{OH} output logic high voltage:	2.4 V minimum
V_{OL} output logic low voltage:	0.5 V maximum
I_{OH} output source current, logic high:	2.6 mA maximum
I_{OH} output sink current, logic low:	24 mA maximum

With these specifications, each digital output line can drive 11 standard TTL loads and over 50 LS TTL loads.

Figure 2-21 depicts signal connections for three typical digital I/O applications.

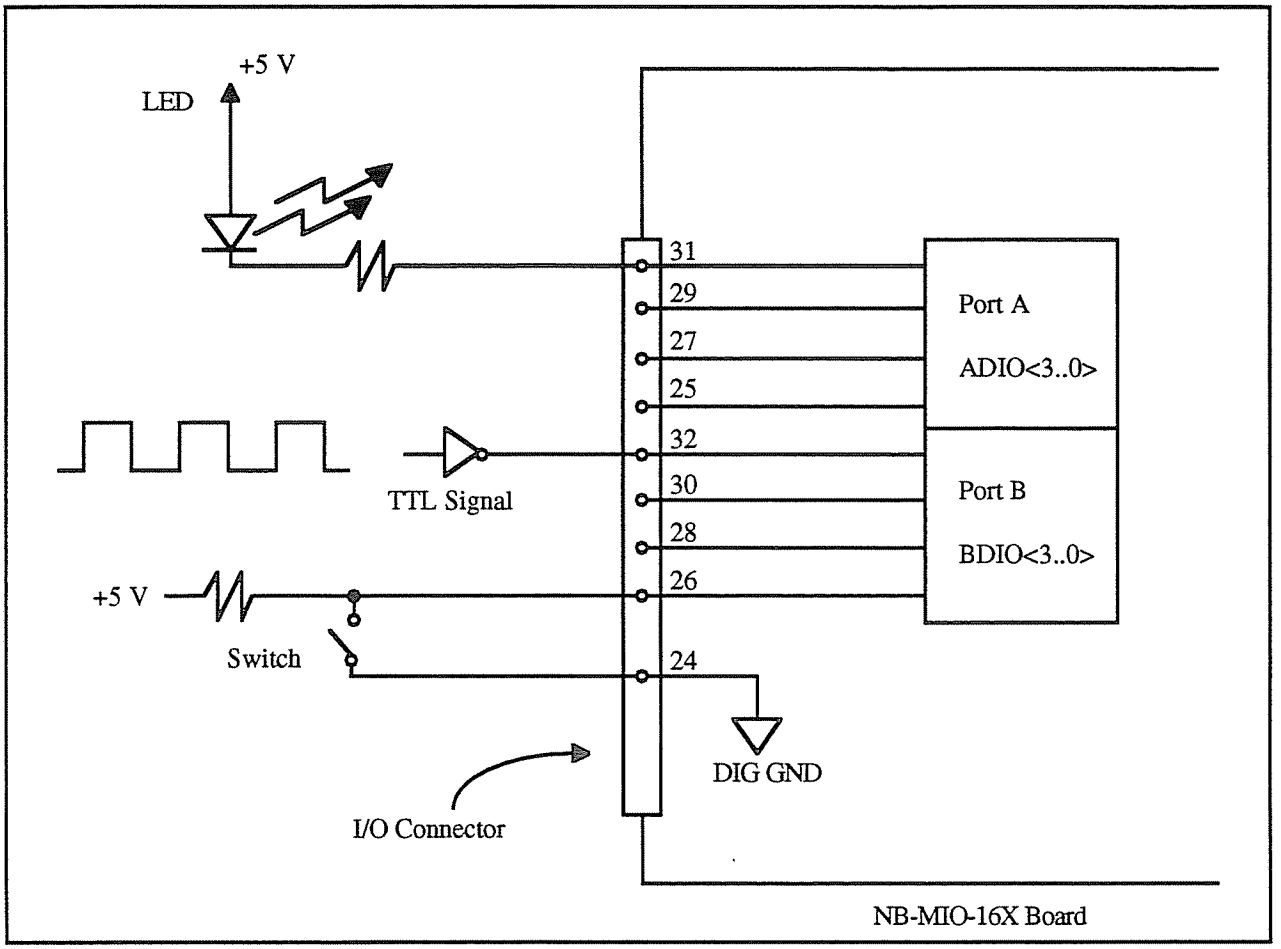


Figure 2-21. Digital I/O Connections

In Figure 2-21, port A is configured for digital output, and port B is configured for digital input. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch in Figure 2-21. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 2-21.

Power Connections

Pins 34 and 35 of the I/O connector provide +5 V from the Macintosh power supply. These pins are referenced to DIG GND and can be used to power external digital circuitry.

Power rating: 0.5 A at +5 V ± 10%

Warning: *Under no circumstances* should these +5 V power pins be connected directly to analog or digital ground or to any other voltage source on the NB-MIO-16X or any other device. Doing so may damage the NB-MIO-16X and the Macintosh. National Instruments is not liable for damage resulting from such a connection.

Timing Connections

Pins 36 through 50 of the I/O connector are connections for timing I/O signals. Pins 36 through 40 carry signals used for data acquisition timing. These signals are explained under *Data Acquisition Timing Connections* later in this chapter. Pins 41 through 50 carry general-purpose timing signals provided by the onboard Am9513A Counter/Timer. These signals are explained under *General-Purpose Timing Signal Connections* later in this chapter.

Data Acquisition Timing Connections

The data acquisition timing signals are SCANCLK, EXTSTROBE*, STARTTRIG*, STOPTRIG, and EXTCONV*.

SCANCLK is an output signal that generates a low-to-high edge whenever an A/D conversion begins. SCANCLK pulses only when scanning is enabled on the NB-MIO-16X. SCANCLK is normally high and pulses low for approximately 1 µsec before the A/D conversion begins. The low-to-high edge can be used to clock external analog input multiplexers. The SCANCLK signal is driven by one LS TTL gate.

A low pulse is generated on the EXTSTROBE* pin when the External Strobe Register is loaded (see *External Strobe Register* in Chapter 4, *Programming*). Figure 2-22 shows the timing for the EXTSTROBE* signal.

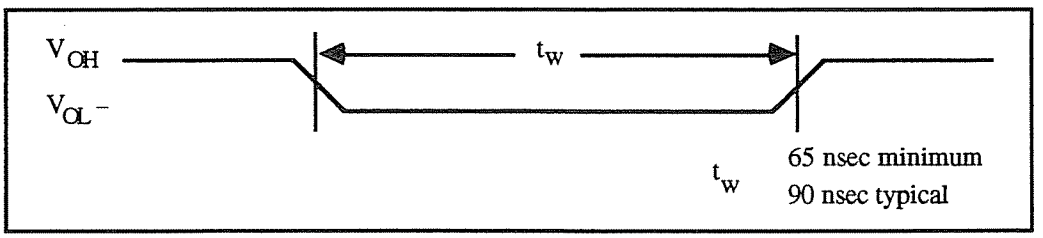


Figure 2-22. EXTSTROBE* Signal Timing

The pulse is typically 90 nsec and is a minimum 65 nsec in width. The EXTSTROBE* signal is an LS TTL signal that can be used by an external device to latch signals or trigger events.

A/D conversions can be externally triggered with the EXTCONV* pin. Applying an active low pulse to the EXTCONV* initiates an A/D conversion. The A/D conversion is initiated by the low-to-high edge of the applied pulse. Figure 2-23 shows the timing requirements for the EXTCONV* signal.

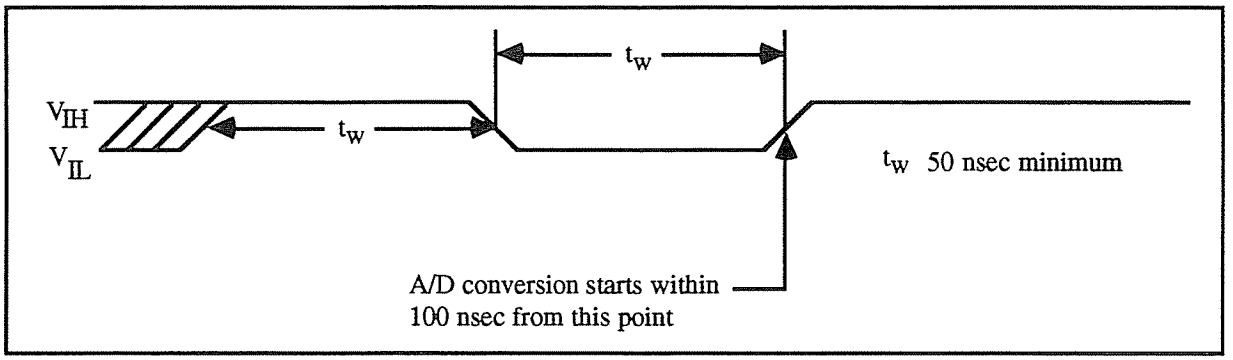


Figure 2-23. EXTCONV* Signal Timing

The minimum allowed pulse width is 50 nsec. An A/D conversion starts within 100 nsec of the low-to-high edge. There is no maximum pulse width limitation. EXTCONV* should be high for at least 50 nsec before going low. The EXTCONV* signal is one LS TTL load and is pulled up to +5 V through a 4.7 kΩ resistor.

Note: EXTCONV* is also driven by the output of Counter 3 of the Am9513A Counter/Timer. This counter is also referred to as the sample-interval counter. The output of Counter 3 must be disabled to a high-impedance state if A/D conversions are to be controlled by pulses applied to the EXTCONV* pin. If Counter 3 is used to control A/D conversions, its output signal can be monitored at the EXTCONV* pin.

Any data acquisition sequence controlled by the onboard sample-interval and sample counters can be initiated by an external trigger applied to the STARTTRIG* pin. If conversions are generated by the EXTCONV* signal, STARTTRIG* does not affect the acquisition timing. Once the two counters are initialized and armed, applying a falling edge to the STARTTRIG* pin starts the counters, thereby initiating a data acquisition sequence.

The data acquisition operation is initiated by the high-to-low edge of the applied pulse. Figure 2-25 shows the timing requirements for the STARTTRIG* signal.

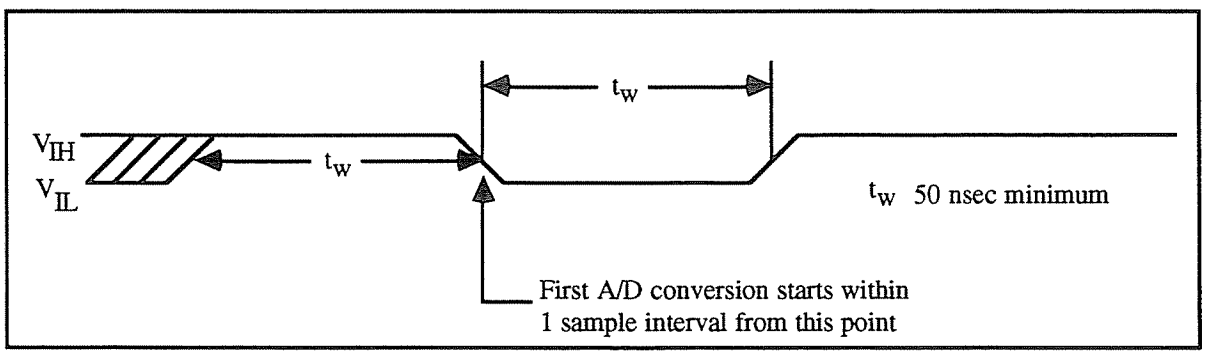


Figure 2-24. STARTTRIG* Signal Timing

The minimum allowed pulse width is 50 nsec. The first A/D conversion starts within one sample interval from the high-to-low edge. The sample interval is controlled by Counter 3. This clock period is the clock period of the timebase or source signal used by the sample-interval counter.

There is no maximum pulse width limitation; however, STARTTRIG* should be high for at least 50 nsec before going low. The STARTTRIG* signal is one LS TTL load and is pulled up to +5 V through a 4.7 kΩ resistor.

The STOPTRIG pin is used during NB-MIO-16X pretriggered data acquisition operations. In pretriggered mode, the data acquisition operation is started but no sample counting occurs until a rising edge is applied to the STOPTRIG pin. The acquisition then completes when the sample counter decrements to 0. This mode acquires data both before and after a hardware trigger is received. Figure 2-25 shows the timing requirements for the STOPTRIG signal.

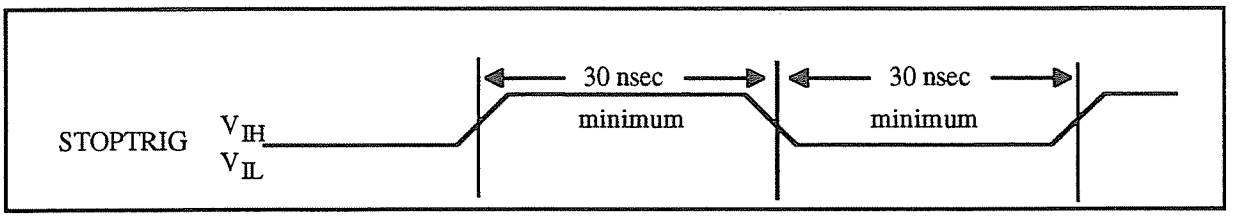


Figure 2-25. STOPTRIG Signal Timing

The STOPTRIG signal is pulled up to +5 V through a 4.7 kΩ resistor.

General-Purpose Timing Signal Connections

The general-purpose timing signals include the GATE, SOURCE, and OUT signals for the Am9513A Counters 1, 2, and 5, and the FOUT signal generated by the Am9513A. Counters 1, 2, and 5 of the Am9513A Counter/Timer can be used for general-purpose applications such as pulse and square wave generation, event counting, and pulse-width, time-lapse, and frequency measurements. For these applications, SOURCE and GATE signals can be directly applied to the counters from the I/O connector, and the counters are programmed for various operations.

The Am9513A Counter/Timer is described briefly in Chapter 3, *Theory of Operation*. For detailed programming information, consult the Am9513A data sheet in Appendix C, *AMD Data Sheet*. For detailed applications information, consult the technical manual *The Am9513A/Am9513 System Timing Controller* published by Advanced Micro Devices, Inc.

Pulses and square waves can be produced by programming Counter 1, 2, or 5 to generate a pulse signal at its OUT output pin or to toggle the OUT signal each time the counter reaches the terminal count.

For event counting, one of the counters is programmed to count rising or falling edges applied to any of the Am9513A SOURCE inputs. The counter value can then be read to determine the number of edges that have occurred. Counter operation can be gated on and off during event counting. Figure 2-26 shows connections for a typical event-counting operation where a switch is used to gate the counter on and off.

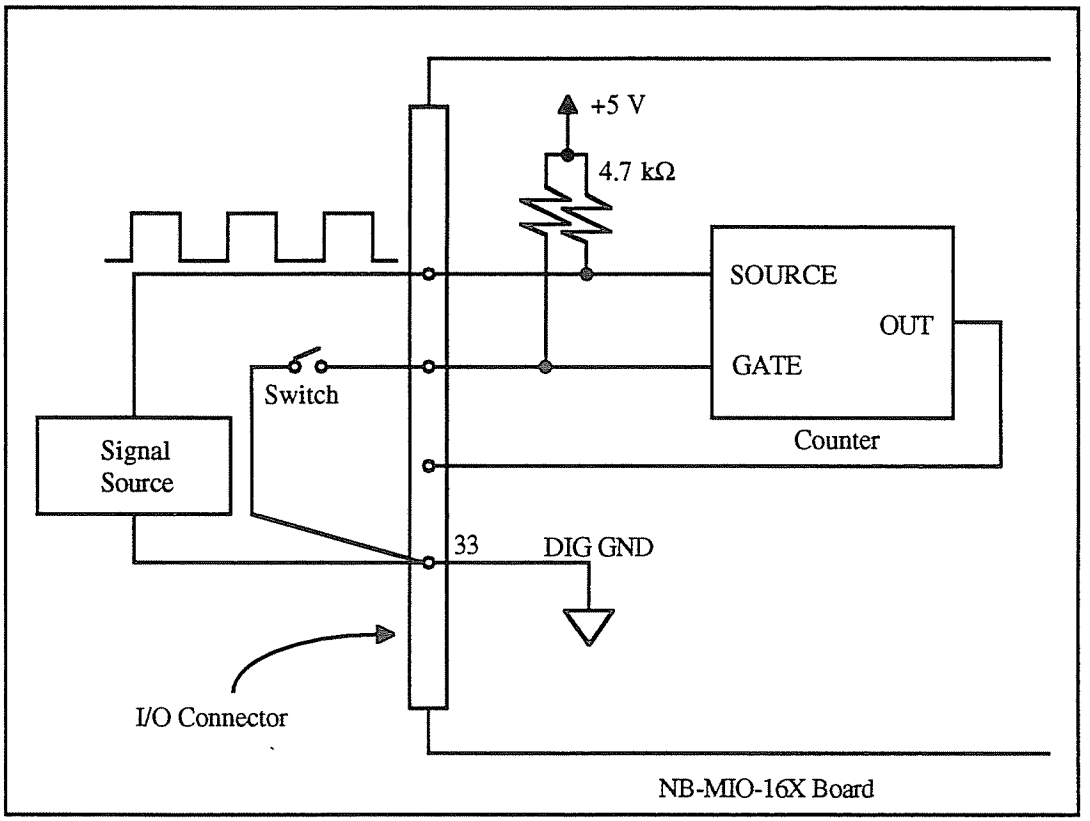


Figure 2-26. Event-Counting Application with External Switch Gating

To perform pulse-width measurement, a counter is programmed to be level gated. The pulse to be measured is applied to the counter GATE input. The counter is programmed to count while the signal at the GATE input is either high or low. If the counter is programmed to count an internal timebase, then the pulse width is equal to the counter value multiplied by the timebase period.

For time-lapse measurement, a counter is programmed to be edge gated. An edge is applied to the counter GATE input to start the counter. The counter can be programmed to start counting after receiving either a high-to-low edge or a low-to-high edge. If the counter is programmed to count an internal timebase, then the time lapse since receiving the edge is equal to the counter value multiplied by the timebase period.

To measure frequency, a counter is programmed to be level gated and the rising or falling edges are counted in a signal applied to a SOURCE input. The gate signal applied to the counter GATE input is of some known duration. In this case, the counter is programmed to count either rising or falling edges at the SOURCE input while the gate is applied. The frequency of the input signal is then the count value divided by the known gate period. Figure 2-27 shows the connections for a frequency measurement application. A second counter could also be used to generate the gate signal in this application.

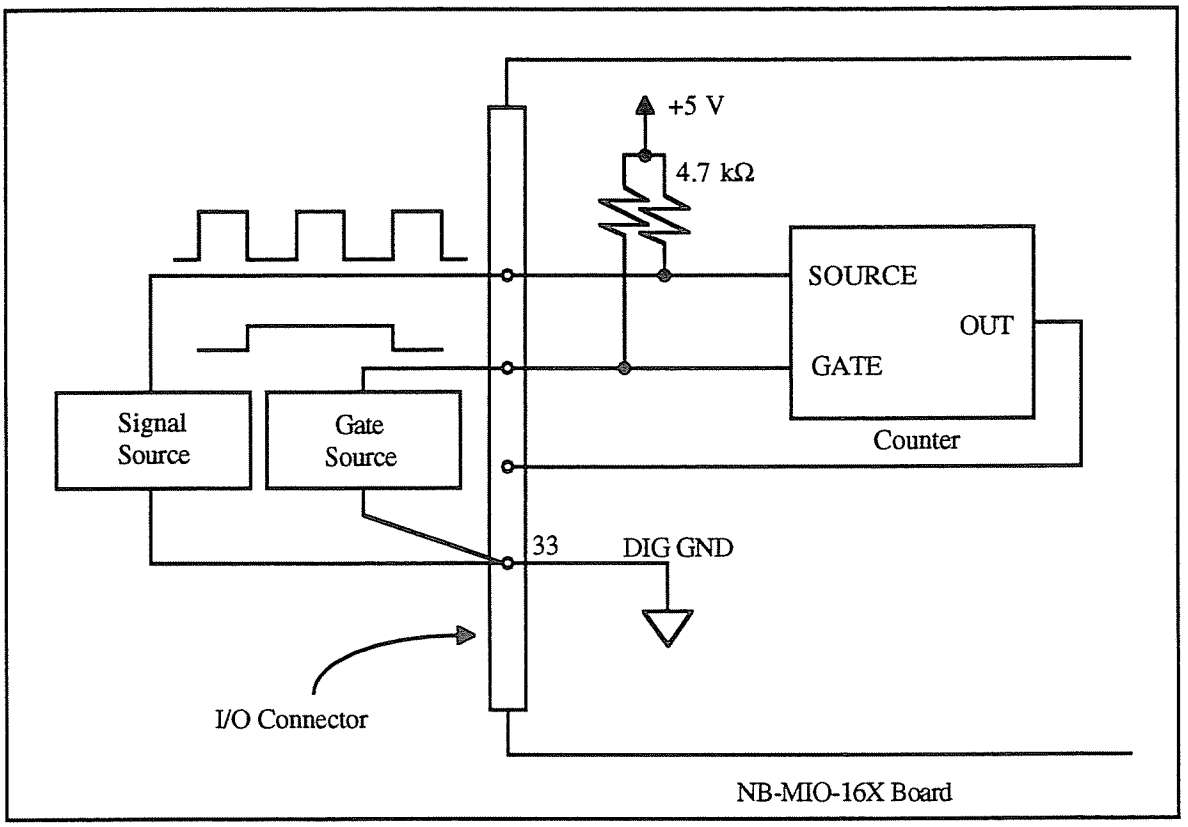


Figure 2-27. Frequency Measurement Application

Two or more counters can be concatenated by tying the OUT signal from one counter to the SOURCE signal of another counter. The counters can then be treated as one 32-bit or 48-bit counter for most counting applications.

The GATE, SOURCE, and OUT signals for Counters 1, 2, and 5, and the FOUT output signal are tied directly from the Am9513A input and output pins to the I/O connector. In addition, the GATE and SOURCE pins are pulled up to +5 V through a 4.7 kΩ resistor.

The following specifications and ratings apply to the Am9513A I/O signals:

Absolute maximum voltage input rating: -0.5 V to +7.0 V with respect to DIG GND

Am9513A Digital Input Specifications (referenced to DIG GND):

V_{IH} input logic high voltage: 2.2 V minimum

V_{IL} input logic low voltage: 0.8 V maximum

Input load current: ±10 µA maximum

Am9513A Digital Output Specifications (referenced to DIG GND):

V_{OH} output logic high voltage: 2.4 V minimum

V_{OL} output logic low voltage:	0.4 V maximum
I_{OH} output source current, at V_{OH}:	200 µA maximum
I_{OH} output sink current, at V_{OL}:	3.2 mA maximum
Output current, high-impedance state:	±25 µA maximum

Figure 2-28 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of the Am9513A.

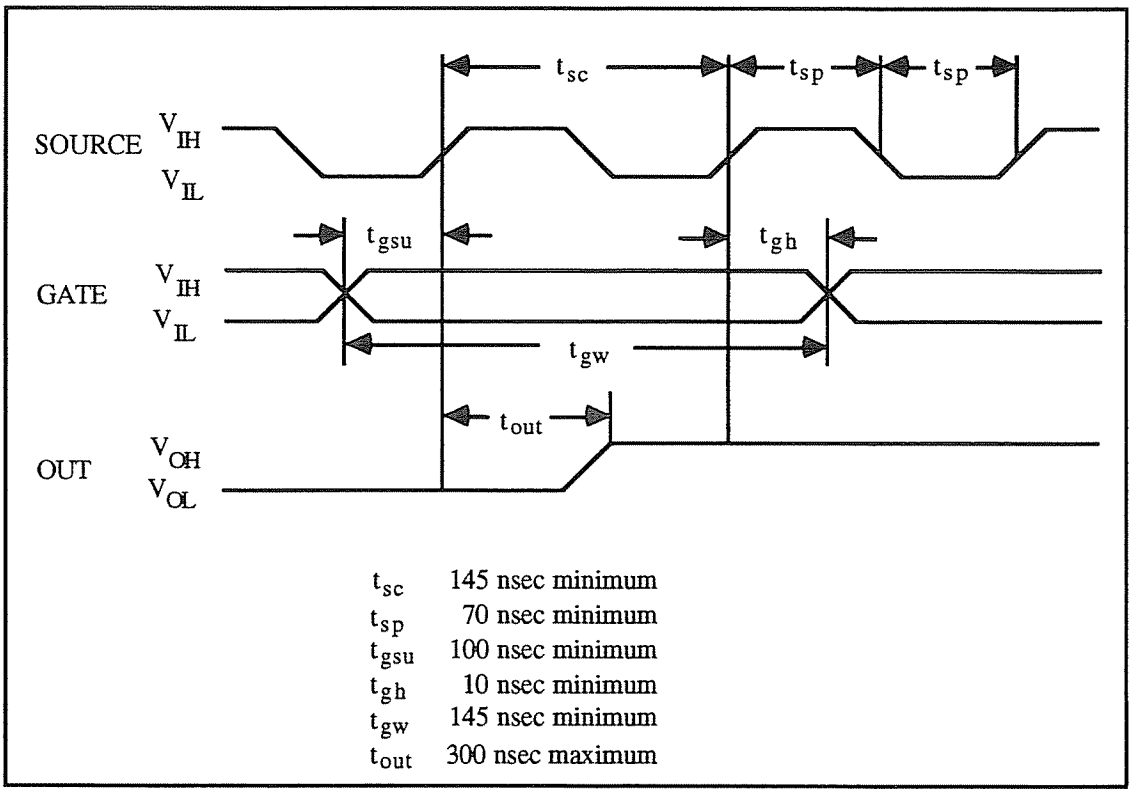


Figure 2-28. General-Purpose Timing Signals

The GATE and OUT signal transitions in Figure 2-28 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, with the source signal inverted and referenced to the falling edge of the source signal, applies to the case in which the counter is programmed to count falling edges.

The signal applied at a SOURCE input can be used as a clock source by any of the Am9513A counter/timers and by the Am9513A frequency division output FOUT. The signal applied to a SOURCE input must not exceed a frequency of 6 MHz for proper operation of the Am9513A. The Am9513A counters can be individually programmed to count rising or falling edges of signals applied at any of the Am9513A SOURCE or GATE input pins.

In addition to the signals applied to the SOURCE and GATE inputs, the Am9513A generates five internal timebase clocks from the clock signal supplied by the NB-MIO-16X. These clocks can be used as counting sources, and they have a maximum skew of 75 nsec between them. The SOURCE signal shown in Figure 2-28 represents any of the signals applied at the SOURCE inputs, GATE inputs, or internal timebase clocks. See the Am9513A data sheet in Appendix C, *AMD Data Sheet*, for further details.

Specifications for signals at the GATE input are referenced to the signal at the SOURCE input or one of the Am9513A internally generated signals. Figure 2-28 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) at least 100 nsec before the rising or falling edge of a source signal for the gate to take effect at that source edge (as shown by t_{gsu} and t_{gh} in Figure 2-28). Similarly, the gate signal must be held for at least 10 nsec after the rising or falling edge of a source signal for the gate to take effect at that source edge. The gate high or low period must be at least 145 nsec in duration. If an internal timebase clock is used, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement provides an uncertainty of one source clock period with respect to unsynchronized gating sources.

Signals generated at the OUT output are referenced to the signal at the SOURCE input or to one of the Am9513A internally generated clock signals. Figure 2-28 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 300 nsec after the source signal rising or falling edge.

Cabling and Field Wiring

This section discusses cabling and field wiring guidelines for the NB-MIO-16X board.

Field Wiring Considerations

Accuracy of measurements made with the NB-MIO-16X can be seriously affected by environmental noise if proper considerations are not taken into account when running signal wires between signal sources and the NB-MIO-16X board. The following recommendations apply mainly to analog input signal routing to the NB-MIO-16X board, though they are applicable for signal routing in general.

Noise pickup can be minimized and measurement accuracy maximized by doing the following:

- Use individually shielded, twisted-pair wires to connect analog input signals to the NB-MIO-16X. With this type of wire, the signals attached to the CH+ and CH- inputs are twisted together and then covered with a shield. This shield is then connected at only one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Use differential analog input connections to reject common mode noise.

The following recommendations apply for all signal connections to the NB-MIO-16X:

- Physically separate NB-MIO-16X signal lines from high-current or high-voltage lines. These lines are capable of inducing currents in or voltages on the NB-MIO-16X signal lines if they run in parallel paths at a close distance. Reduce the magnetic coupling between lines by separating them by a reasonable distance if they run in parallel, or by running the lines at right angles to each other.

- Do not run NB-MIO-16X signal lines through conduits that also contain power lines.
- Protect NB-MIO-16X signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running the NB-MIO-16X signal lines through special metal conduits.

Cabling Considerations

National Instruments has a cable termination accessory, the CB-50, for use with the NB-MIO-16X board. This kit includes a terminated 50-conductor flat ribbon cable and a connector block. Signal I/O leads can be attached to screw terminals on the connector block and thereby connected to the NB-MIO-16X I/O connector.

The CB-50 is useful for prototyping an application or in situations where NB-MIO-16X interconnections are frequently changed. Once a final field wiring scheme has been developed, however, you may wish to develop your own cable. This section contains information and guidelines for design of such a cable.

The NB-MIO-16X I/O connector is a 50-pin male ribbon cable header. Recommended manufacturer part numbers for this header are as follows:

3M Scotchflex	part number 3596-5002
T&B Corporation/Ansley Electronics Division	part number 609-5007

The mating connector for the NB-MIO-16X is a 50-position, ribbon socket connector, polarized, with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside down connection to the NB-MIO-16X. Recommended manufacturer part numbers for this mating connector are as follows:

3M Scotchflex	part number 3425-7650
T&B Corporation/Ansley Electronics Division	part number 609-5041CE

A standard ribbon cable (50-conductor, 28 AWG, stranded) can be used with these connectors. Recommended manufacturer part numbers for this ribbon cable are as follows:

3M Scotchflex	part number 3365/50
T&B Corporation/Ansley Electronics Division	part number 171-50

In making your own cabling, you may want to shield your cables. The following guidelines may help:

- For the analog input signals, shielded twisted-pair wires for each analog input pair yield the best results, assuming that differential inputs are used. Tie the shield for each signal pair to the ground reference at the source.
- The analog lines, pins 1 through 23, should be routed separately from the digital lines, pins 24 through 50.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so will result in noise from switching digital signals coupling into the analog signals.

Chapter 3
Theory of Operation

This chapter contains a functional overview of the NB-MIO-16X and explains the operation of each functional unit making up the NB-MIO-16X.

Functional Overview

The block diagram in Figure 3-1 is a functional overview of the NB-MIO-16X board.

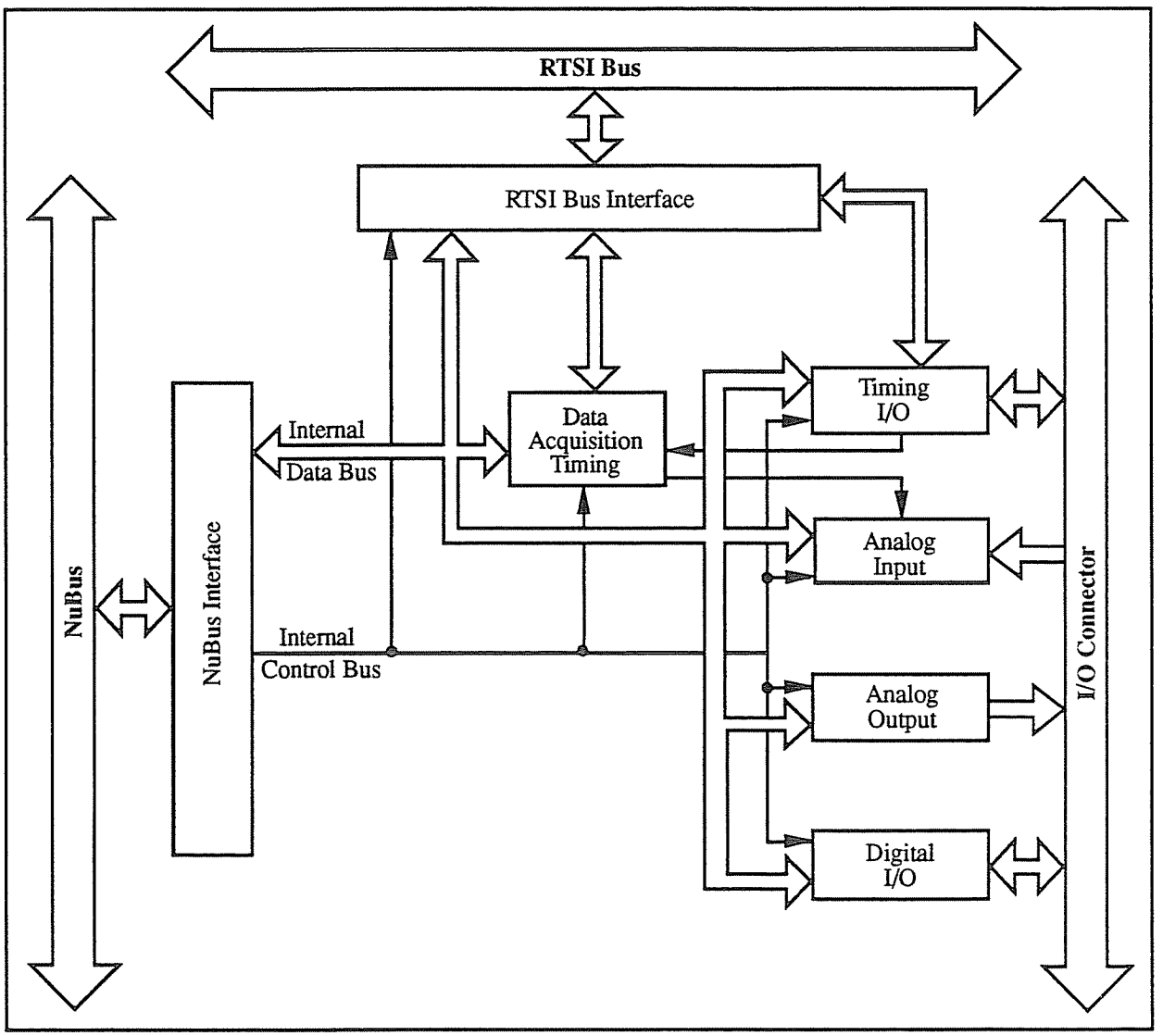


Figure 3-1. NB-MIO-16X Block Diagram

The following are the major constituents of the NB-MIO-16X board:

- NuBus interface circuitry
- Analog input and data acquisition circuitry
- Analog output circuitry
- Digital I/O circuitry
- Timing I/O circuitry
- RTSI bus interface circuitry

The internal data and control buses interconnect the components. The theory of operation of each of these components is explained in the remainder of this chapter.

NuBus Interface Circuitry

The NB-MIO-16X is a full-sized 16-bit NuBus slave board. The NuBus is a 32-bit address and data bus with a 10 MHz clock. In addition, the NuBus provides interface signals for read and write operations, and an interrupt line that may be driven by boards in NuBus slots. The components making up the NB-MIO-16X NuBus interface circuitry are shown in Figure 3-2.

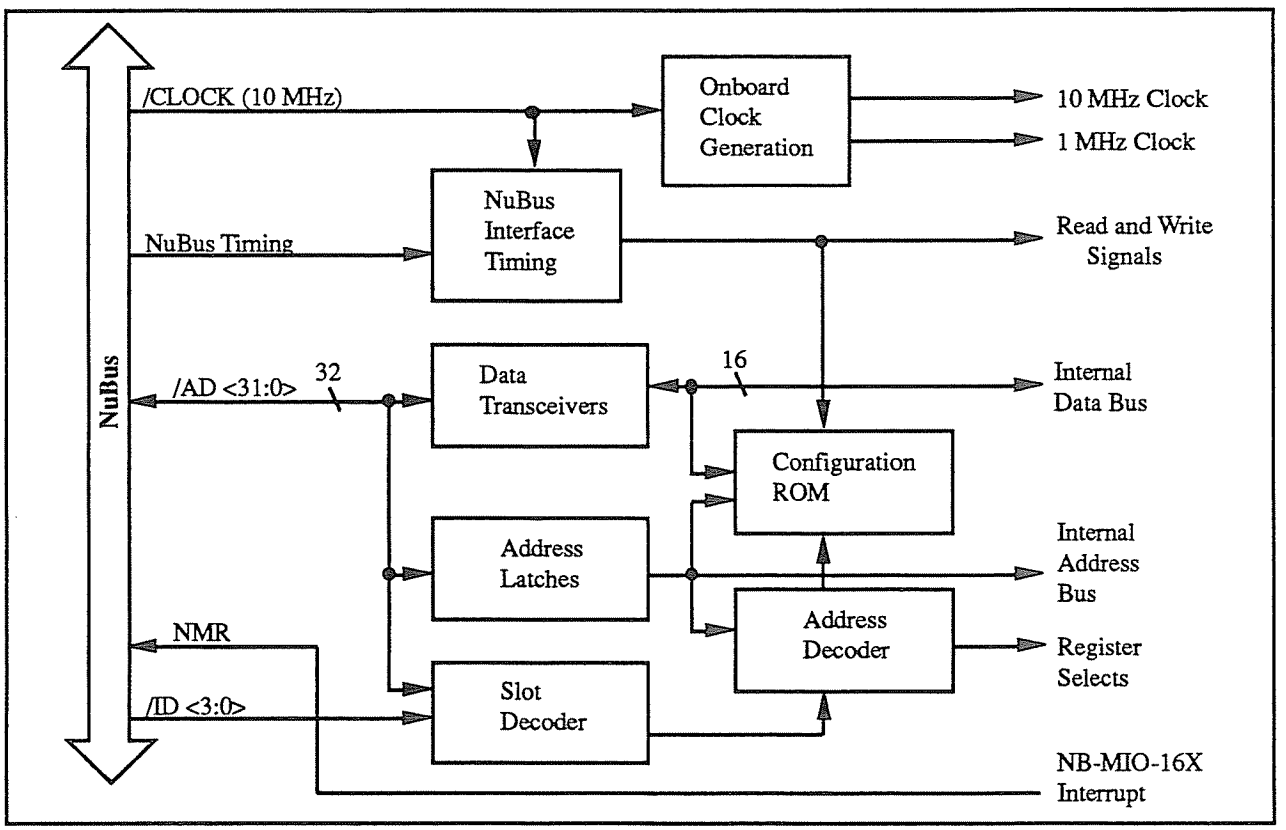


Figure 3-2. NuBus Interface Circuitry Block Diagram

The NuBus interface circuitry consists of slot-decoding circuitry, address latches, data transceivers, interface timing signals, address decoding circuitry, EPROM, NMR interrupt circuitry, and circuitry to generate onboard 10 MHz and 1 MHz clocks. This interface circuitry generates the signals necessary to control and monitor the operation of the NB-MIO-16X multiple function circuitry.

The slot-decoding circuitry on the NB-MIO-16X matches NuBus address lines 24 through 27 to slot ID lines provided by the slot in which the board resides. This matching is used by the board to determine when the slot that it occupies is being addressed. Each slot in the Macintosh NuBus has a unique slot address. The NuBus address lines 0 through 19 are latched by the onboard address latches. These address lines are decoded by the NB-MIO-16X address-decoding circuitry in order to generate *select* signals for the onboard configuration ROM and other registers. Address lines 20 through 23 are left undecoded by the NB-MIO-16X board so that the NB-MIO-16X is compatible with both the 24-bit and 32-bit bus modes used by the Macintosh NuBus.

The NB-MIO-16X is a 16-bit interface board and therefore uses only 16 of the 32 data lines on the NuBus. The NuBus interface timing signals are decoded by the NB-MIO-16X NuBus interface timing circuitry, which generates the proper read and write signals for the remaining NB-MIO-16X circuitry. The NuBus 10 MHz clock is used to clock the NuBus interface timing circuitry. This clock is also buffered onboard, and generates a 1 MHz clock for the counter/timer and 2, 5, and 10 MHz clocks for running the ADC.

The configuration ROM is an 8 kilobyte EPROM that contains information pertinent to the NB-MIO-16X board. This ROM is read by the Macintosh Slot Manager at system startup. It is required by the NuBus and is used by the Macintosh operating system and other software to identify the board.

The NB-MIO-16X is able to cause interrupts in the Macintosh NuBus by driving the NuBus NMR interrupt line.

Analog Input and Data Acquisition Circuitry

The NB-MIO-16X handles 16 channels of analog input with software-programmable gain and 16-bit A/D conversion. In addition, the NB-MIO-16X contains data acquisition circuitry for automatic timing of multiple A/D conversions and includes advanced options such as external triggering, gating, and clocking. Figure 3-3 shows a block diagram of the analog input and data acquisition circuitry.

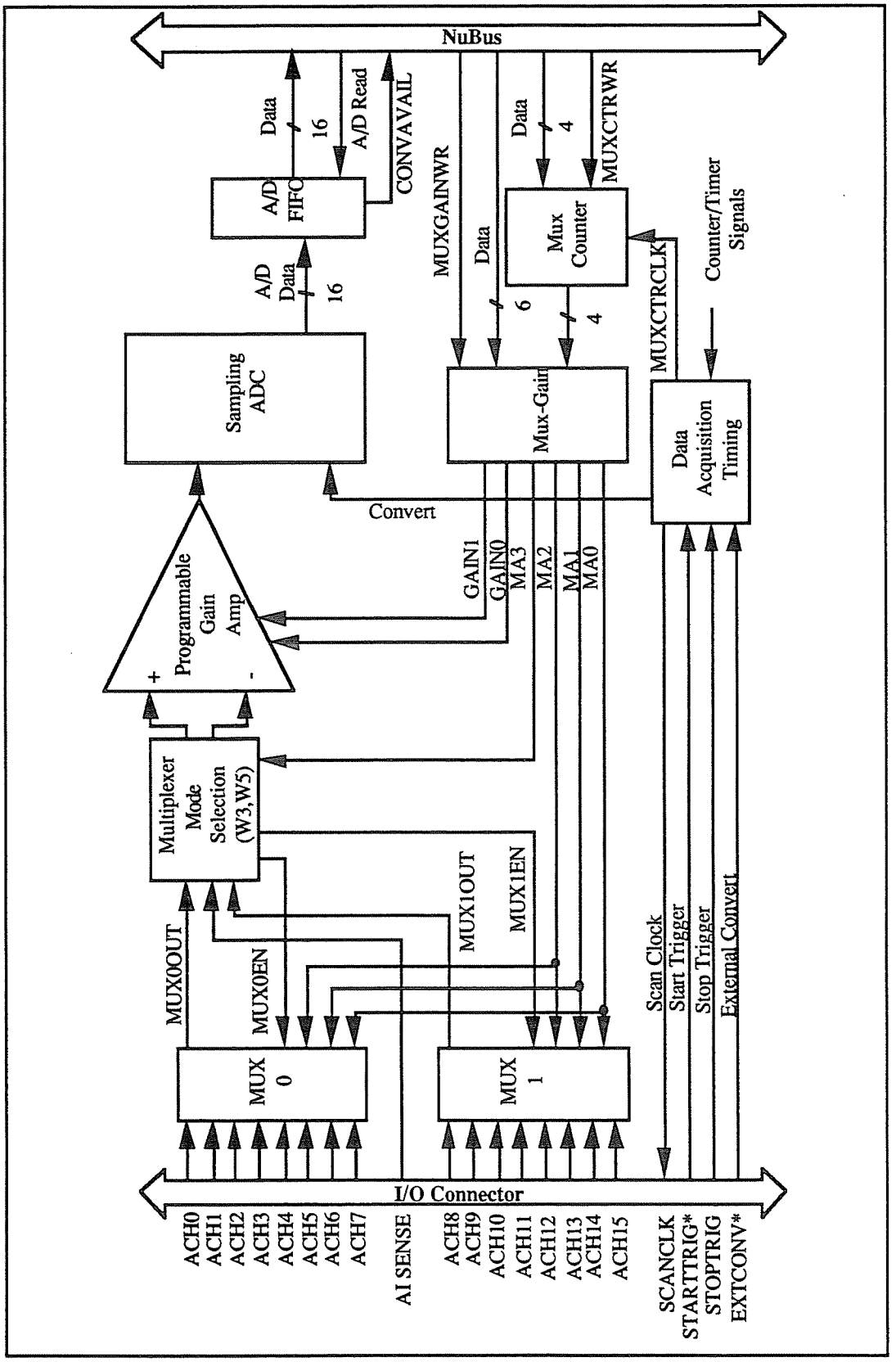


Figure 3-3. Analog Input and Data Acquisition Circuitry Block Diagram

Analog Input Circuitry

The analog input circuitry consists of an input multiplexer, multiplexer mode selection jumpers, a software-programmable gain instrumentation amplifier, a 16-bit ADC, and a 16-bit FIFO.

The input multiplexer consists of two CMOS analog input multiplexers and has 16 analog input channels. Multiplexer MUX0 is connected to analog input channels 0 through 7. Multiplexer MUX1 is connected to analog input channels 8 through 15. The input multiplexers provide input overvoltage protection of ±35 V powered on and ±20 V powered off.

The multiplexer mode selection jumpers configure the analog input channels as 16 single-ended inputs or 8 differential inputs. When single-ended mode is selected, the outputs of the two multiplexers are tied together and routed to the positive (+) input of the instrumentation amplifier. The negative (-) input of the instrumentation amplifier is tied to the NB-MIO-16X ground for RSE input or to the analog return of the input signals via the AISENSE input on the I/O connector for NRSE input. When DIFF mode is selected, the output of MUX0 is routed to the positive (+) input of the instrumentation amplifier, and the output of MUX1 is routed to the negative (-) input of the instrumentation amplifier.

The instrumentation amplifier fulfills two purposes on the NB-MIO-16X board. It converts a differential input signal into a single-ended signal with respect to the NB-MIO-16X ground for a minimum input common mode rejection ratio of 75 dB. This conversion allows the input analog signal to be extracted from any common mode voltage or noise before being sampled and converted. The instrumentation amplifier also applies gain to the input signal, allowing an input analog signal to be amplified before being sampled and converted, and thus increasing measurement resolution and accuracy. The gain of the instrumentation amplifier is selected under software control. The NB-MIO-16XL (L stands for low-level signals) provides gains of 1, 10, 100, and 500. The NB-MIO-16XH (H stands for high-level signals) provides gains of 1, 2, 4, and 8.

Selection of the analog input channel and the gain settings is controlled by the mux-gain memory. The mux-gain memory provides two gain control bits to the instrumentation amplifier and four multiplexer address bits to the input multiplexers and multiplexer mode selection circuitry that select the analog input channels. Operation of the mux-gain memory is explained in more detail under *Data Acquisition Timing Circuitry* later in this chapter.

The ADC is a 16-bit successive approximation sampling ADC. The 16-bit resolution of the converter allows the ADC to resolve its input range into 65536 different steps. This resolution also provides a 16-bit digital word that represents the value of the input voltage level with respect to the converter input range. The ADC supports four input ranges that can be selected by setting jumpers on the board and setting a software bit: -10 to +10 V, -5 to +5 V, 0 to +10 V, and 0 to +5 V. The NB-MIO-16X ADC is available in two different maximum conversion times: 42 or 18 µsec.

When an A/D conversion is complete, the ADC clocks the result into the A/D FIFO. The A/D FIFO is 16 bits wide and 16 words deep. This FIFO serves as a buffer to the ADC and provides two benefits. Any time an A/D conversion is complete, the value is saved in the A/D FIFO for later reading, and the ADC is free to start a new conversion. Secondly, the A/D FIFO can collect up to 16 A/D conversion values before any information is lost, thus allowing software or DMA extra time (16 times the sample interval) to catch up with the hardware. If more than 16 values are stored in the A/D FIFO and the A/D FIFO is not read, an error condition called A/D FIFO overflow occurs and A/D conversion information is lost.

The A/D FIFO generates a signal that indicates when it contains A/D conversion data. The state of this signal can be read from the NB-MIO-16X Status Register. This signal can be used to generate a DMA request signal or to generate an interrupt.

The NB-MIO-16X can be programmed to generate either straight binary numbers or two's complement numbers. Straight binary numbers range from 0 to 65535; two's complement numbers range from -32768 to +32767. Two's complement numbers are generated on the board from straight binary numbers by inverting the most significant bit.

Data Acquisition Timing Circuitry

A data acquisition operation refers to the process of taking a sequence of A/D conversions with the sample interval (the time between successive A/D conversions) carefully timed. The data acquisition timing circuitry consists of various clocks and timing signals. Three types of data acquisition are supported by the NB-MIO-16X board: single-channel data acquisition, multiple-channel data acquisition with continuous scanning, and multiple-channel data acquisition with interval scanning.

Scanned data acquisition uses the mux counter and the mux-gain memory to automatically switch between analog input channels during data acquisition. Continuous scanning cycles through the mux-gain memory without any delays between cycles. Interval scanning assigns a time interval called the *scan interval* to each cycle through the mux-gain memory. The scan interval is basically the time between starts for each cycle through the mux-gain memory.

Data acquisition timing consists of signals that initiate a data acquisition operation, initiate individual A/D conversions, gate the data acquisition operation, and generate scanning clocks. The sources for these signals can be supplied by timers on the NB-MIO-16X board, by signals connected to the NB-MIO-16X I/O connector, or by signals from other NB Series boards connected to the RTSI bus.

Single A/D conversions can be initiated by applying an active low pulse to the EXTCONV* input on the I/O connector or writing to the Start Convert Register on the NB-MIO-16X board. During data acquisition, the onboard sample-interval counter (Counter 3 of the Am9513A Counter/Timer) generates pulses that initiate A/D conversions. The sample interval can be controlled externally by applying a stream of pulses at the EXTCONV* input. In this case, you have complete external control over the sample interval and the number of A/D conversions performed.

The sample-interval timer is a 16-bit down counter that can be used with the five internal timebases of the Am9513A to generate sample intervals from 2 µsec to 6 sec (see *Timing I/O Circuitry* later in this chapter). The sample-interval timer can also use any of the external clock inputs to the Am9513A as a timebase. During data acquisition, the sample interval counts down at the rate given by the internal timebase or external clock. Each time the sample-interval timer reaches 0, it generates a pulse and reloads with the programmed sample-interval count. This operation continues until data acquisition halts.

Data acquisition can be controlled by the onboard sample counter. This counter is loaded with the number of samples to be taken during a data acquisition operation. The sample counter can be 16-bit for counts up to 65535 or 32-bit for counts up to $(2^{32} - 1)$. If a 16-bit counter is needed, Counter 4 of the Am9513A Counter/Timer is used. If more than 16 bits are needed, Counter 4 is concatenated with Counter 5 of the Am9513A to form a 32-bit counter. The sample counter decrements its count each time the sample-interval counter generates an A/D conversion pulse, and the sample counter stops the data acquisition process when it counts down to 0.

The sample counter can be triggered externally with the STOPTRIG input on the NB-MIO-16X I/O connector. The counter does not begin counting the A/D conversion pulses until a rising edge signal occurs on STOPTRIG. With this method, A/D conversion samples can be collected both before and after a hardware trigger is received.

The data acquisition process can be initiated by writing to the Start DAQ Register on the NB-MIO-16X board or by applying an active low pulse to the STARTTRIG* input on the NB-MIO-16X I/O connector. These triggers start the sample-interval and sample counters. The sample-interval counter then manages the data acquisition process until the sample counter reaches 0.

Single-Channel Data Acquisition

During single-channel data acquisition, the mux-gain memory is set up to select the gain and analog input channel before data acquisition is initiated. These gain and multiplexer settings remain constant during the entire data acquisition process; therefore, all A/D conversion data is read from a single channel.

Multiple-Channel (Scanned) Data Acquisition

Multiple-channel data acquisition is performed by enabling scanning during data acquisition. Multiple-channel scanning is controlled by the mux counter and the mux-gain memory.

The mux-gain memory consists of 16 words of memory. Each word of memory contains a multiplexer address (4 bits) for input analog channel selection, a gain setting (2 bits), and a bit indicating if the entry is the last in the scan sequence. The mux-gain memory address is controlled by the mux counter. Whenever a mux-gain memory address location is selected, the multiplexer and gain control bits contained in that memory location are applied to the analog input circuitry. For scanning operations, the mux counter steps through successive locations in the mux-gain memory at a rate determined by the scan clock. The mux-gain memory, therefore, allows an arbitrary sequence of channels (16 maximum), with a separate gain setting for each channel to be clocked through during a scanning operation.

Both the mux counter and the mux-gain memory can be directly written to through NB-MIO-16X registers. For writing purposes, the mux counter serves as a pointer to the mux-gain memory. The counter can be loaded with any 4-bit value to point to any mux-gain memory location. This counter also allows scanning to start at any location in the mux-gain memory.

The SCANCLK signal is generated from the sample-interval counter. This signal pulses once at the beginning of each A/D conversion. The SCANCLK signal is supplied at the I/O connector. During multiple-channel scanning, the mux counter is incremented repeatedly, thereby sequencing through the mux-gain memory and automatically selecting new channel and gain settings during data acquisition. The MUXCTRCLK signal is generated from the SCANCLK and provides the pulses that increment the mux counter. MUXCTRCLK can be identical to SCANCLK, incrementing the mux counter once after every A/D conversion. MUXCTRCLK can also be generated by dividing SCANCLK by Counter 1 of the Am9513A Counter/Timer. This method allows the mux counter to be incremented once every *N* A/D conversions such that *N* conversions can be performed on a single channel and gain selection before switching to the next channel and gain selection.

Analog Output Circuitry

The NB-MIO-16X provides two channels of 12-bit D/A output. Each analog output channel provides options such as unipolar or bipolar output and internal or external reference voltage selection. Figure 3-4 shows a block diagram of the analog output circuitry.

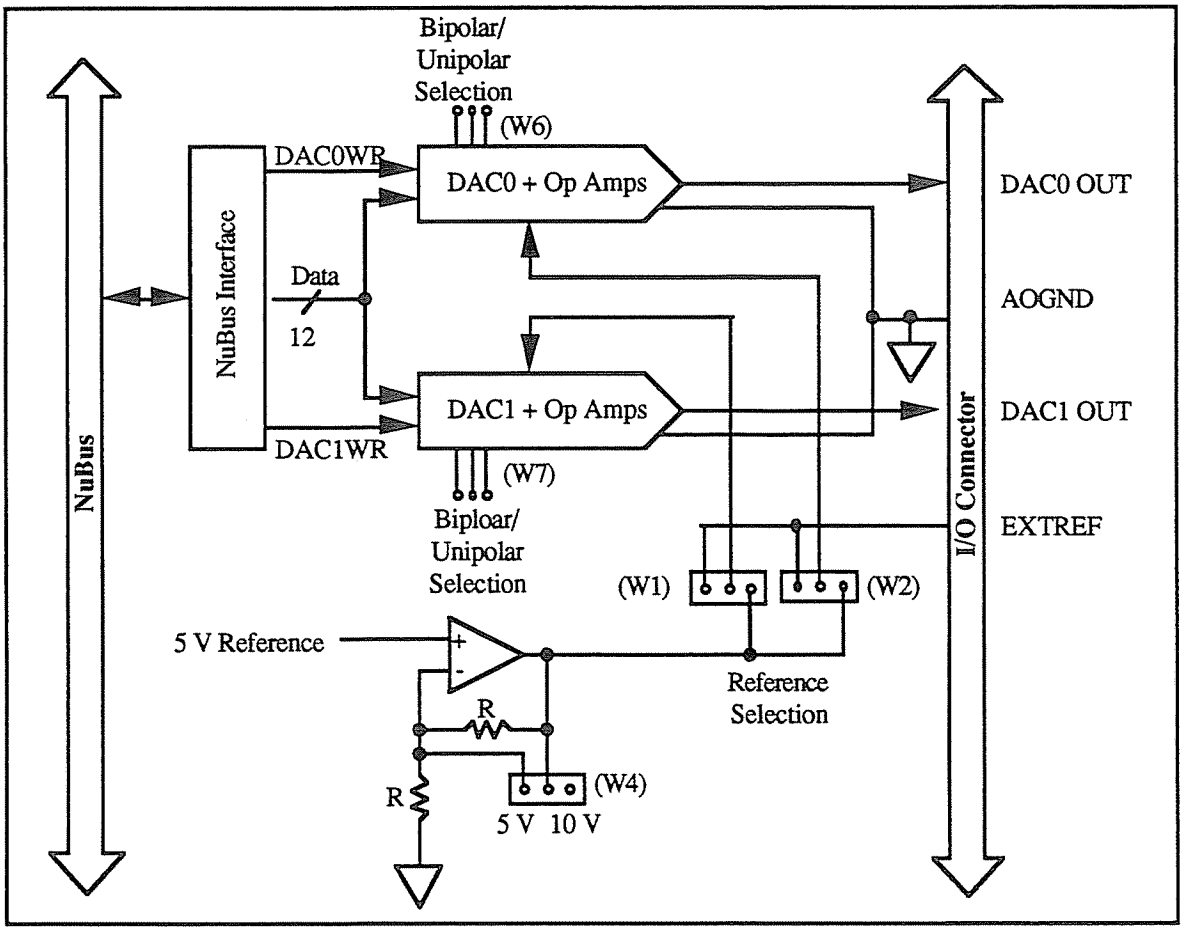


Figure 3-4. Analog Output Circuitry Block Diagram

Each analog output channel contains a 12-bit DAC, output operational amplifiers (op amps), reference selection jumpers, and unipolar/bipolar output selection jumpers.

The DAC in each analog output channel generates a current proportional to the input voltage reference (V_{ref}) multiplied by the digital code loaded into the DAC. Each DAC can be loaded with a 12-bit digital code by writing to registers on the NB-MIO-16X board. The output op amps convert the DAC current output to a voltage output provided at the NB-MIO-16X I/O connector DAC0 OUT and DAC1 OUT pins. The analog output of the DACs is updated to reflect the loaded 12-bit digital code in any of four ways–immediately when the 12-bit code is written to the DACs, when an active low pulse occurs on the Am9513A OUT2 pin, when an external active low pulse drives the OUT2 signal on the back connector, or when an active low pulse is received from the RTSI bus. The update method used is selected by the RTSIWGEN and TMRWGEN bits in Command Register 1.

The DAC output op amps can be jumper configured to provide either a unipolar or bipolar voltage output range. A unipolar output has an output voltage range of 0 to $+V_{ref}$ - 1 LSB V. A bipolar output provides an output voltage range of $-V_{ref}$ to $+V_{ref}$ -1 LSB V. For unipolar output, 0 V output corresponds to a digital code word of 0. For bipolar output, the form of the digital code input is jumper selectable. If straight binary form is selected, 0 V output corresponds to a digital code word of 2,048. If two's complement form is selected, 0 V output corresponds to a digital code word of 0. One LSB is the voltage increment corresponding to an LSB change in the digital code word.

For unipolar output, use the following formula:

$$1\ \text{LSB} = \frac{V_{ref}}{4{,}096}$$

For bipolar output, use the following formula:

$$1\ \text{LSB} = \frac{V_{ref}}{2{,}048}$$

The voltage reference source for each DAC is jumper selectable and can be supplied either externally at the EXTREF input or internally. The external reference can be either a DC or an AC signal. If an AC reference is applied, the analog output channel acts as a signal attenuator, and the AC signal appears at the output attenuated by the digital code divided by 4,096 for unipolar output.

Bipolar output with an AC reference provides four-quadrant multiplication, which means that the signal is inverted for digital codes -2,048 through -1, and not inverted for digital codes 1 through 2,047. In two's complement mode, a digital code word of 0 attenuates the input signal to 0 V. This attenuation is equivalent to multiplying the signal by (digital code word) / 2,048.

The internal voltage reference is a buffered version of the 5 V reference supplied by the ADC. This buffer either produces 5 V or multiplies its input by 2 to give 10 V. Using the internal reference supplies an output voltage range of 0 to 4.9988 V in steps of 1.22 mV or 0 to 9.9976 V in steps of 2.44 mV for unipolar output and an output voltage range of -5 V to +4.9976 V in steps of 2.44 mV or -10 V to +9.9951 V in steps of 4.88 mV for bipolar output.

Digital I/O Circuitry

The NB-MIO-16X provides eight digital I/O lines. These lines are divided into two ports of four lines each and are located at pins ADIO<3..0> and BDIO<3..0> on the I/O connector. Figure 3-5 shows a block diagram of the digital I/O circuitry.

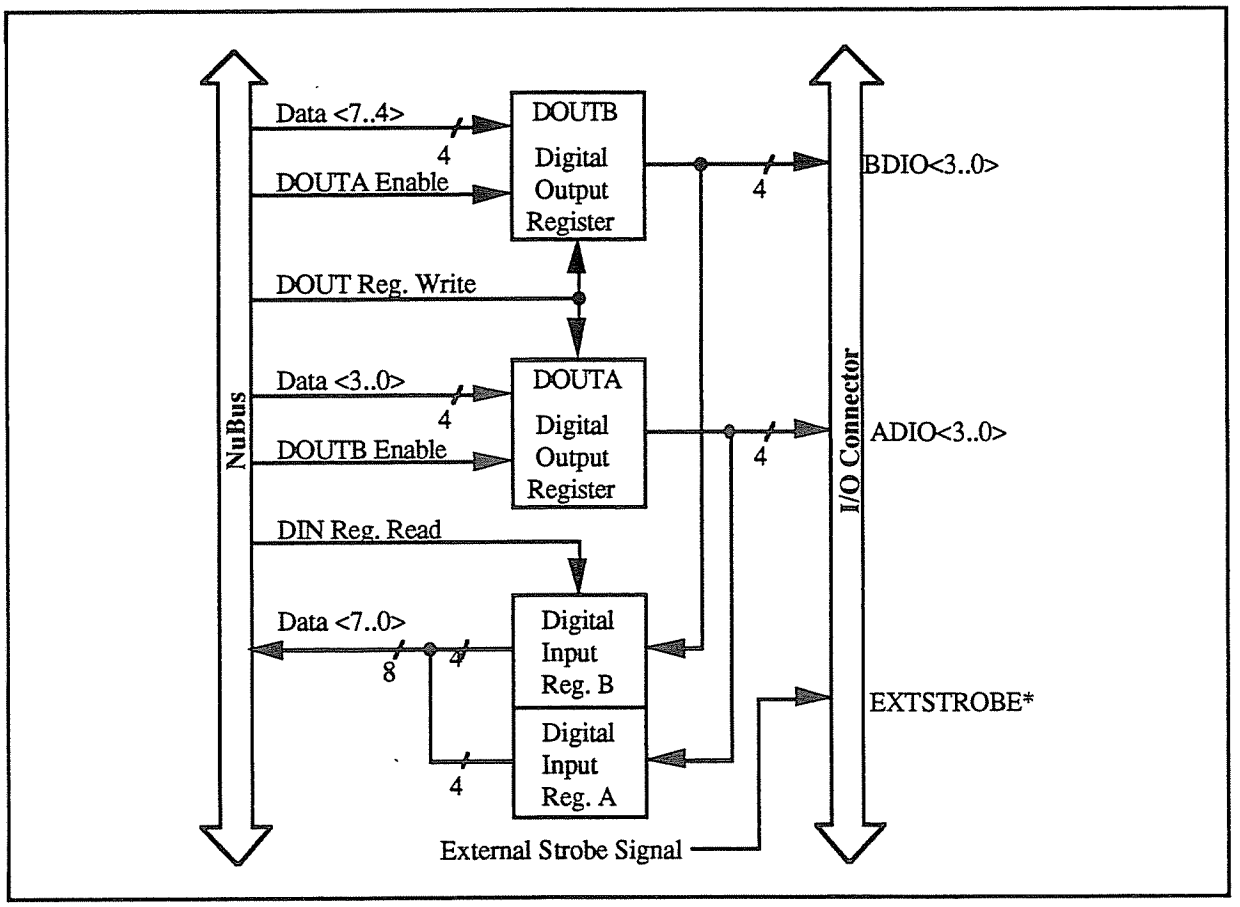


Figure 3-5. Digital I/O Circuitry Block Diagram

The digital I/O lines are controlled by the Digital Output Register and monitored by the Digital Input Register. The Digital Output Register is an 8-bit register that contains the digital output values for both ports A and B. When port A is enabled, bits <3..0> in the Digital Output Register are driven onto digital output lines ADIO<3..0>. When port B is enabled, bits <7..4> in the Digital Output Register are driven onto digital output lines BDIO<3..0>.

Reading the Digital Input Register returns the state of the digital I/O lines. Digital I/O lines ADIO<3..0> are connected to bits <3..0> of the Digital Input Register. Digital I/O lines BDIO<3..0> are connected to bits <7..4> of the Digital Input Register. When a port is enabled, the Digital Input Register serves as a read-back register, returning the digital output value of the port. When a port is not enabled, reading the Digital Input Register returns the state of the digital I/O lines as driven by an external device.

Both the digital input and output registers are TTL compatible. The digital output ports, when enabled, are capable of sinking 24 mA of current and sourcing 2.6 mA of current on each digital I/O line. When the ports are not enabled, the digital I/O lines act as high-impedance inputs.

The external strobe signal EXTSTROBE*, shown in Figure 3-5, is a general-purpose strobe signal. Writing to an address location on the NB-MIO-16X board generates an active low 90 nsec pulse on this output pin. EXTSTROBE* is not necessarily part of the digital I/O circuitry but is shown here because it can be used to latch digital output from the NB-MIO-16X into an external device.

Timing I/O Circuitry

The NB-MIO-16X uses an Am9513A Counter/Timer for data acquisition timing and for general-purpose timing I/O functions. Figure 3-6 shows a block diagram of the timing I/O circuitry.

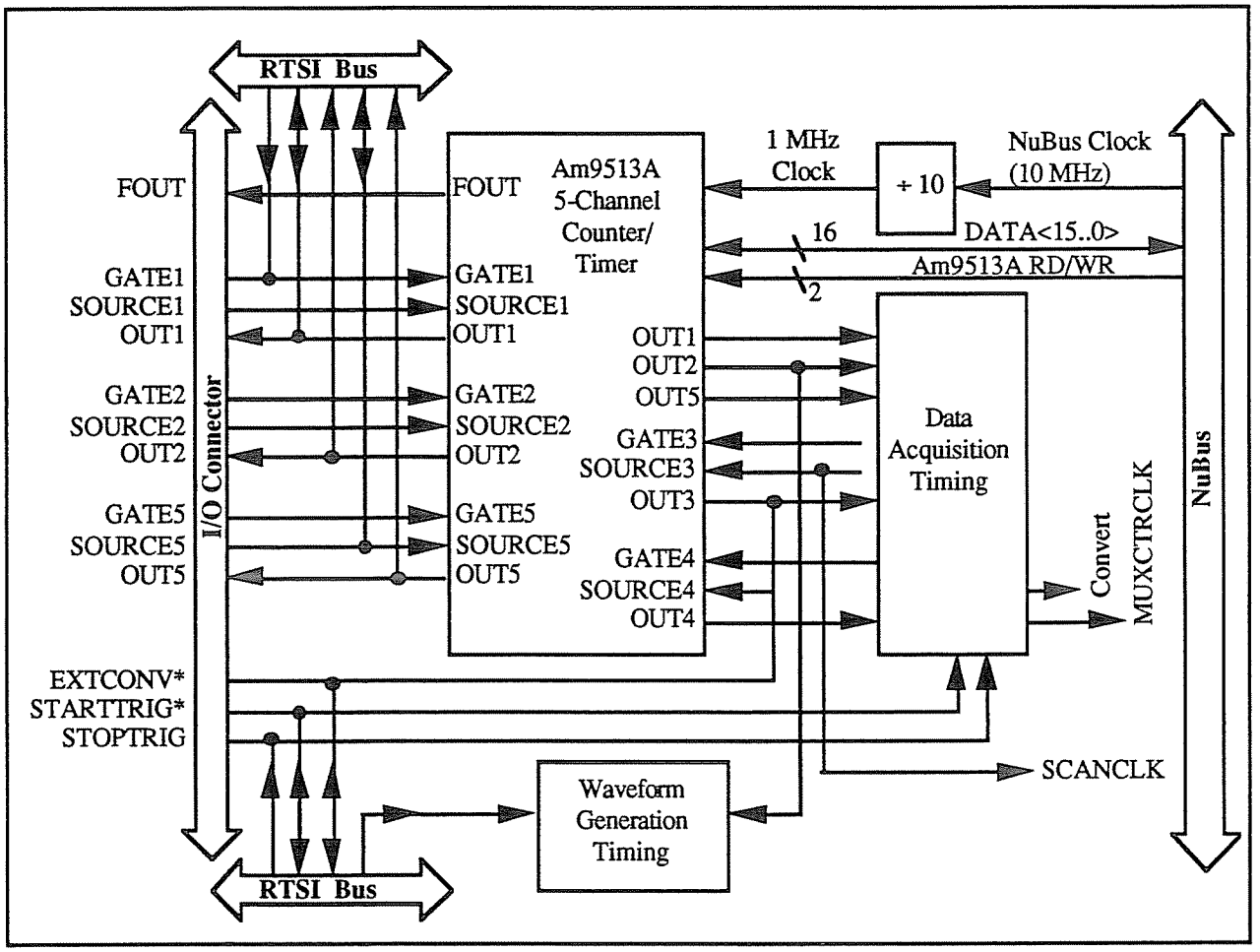


Figure 3-6. Timing I/O Circuitry Block Diagram

The Am9513A contains five independent 16-bit counter/timers, a 4-bit frequency output channel, and five internally generated timebases. The five counter/timers can be programmed to operate in several timing modes. The programming and operation of the Am9513A are presented in detail in Appendix C, *AMD Data Sheet.*

The Am9513A clock input is a 1 MHz clock generated from the NuBus 10 MHz clock. The Am9513A uses this clock input to generate five internal timebases. These timebases can be used as clocks by the counter/timers and by the frequency output channel. The five internal timebases normally used for NB-MIO-16X timing functions are 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz.

The 16-bit counters in the Am9513A are diagrammed as shown in Figure 3-7.

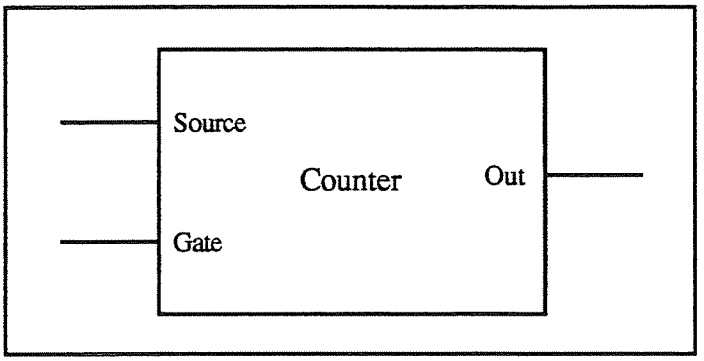


Figure 3-7. Counter Block Diagram

Each counter has a SOURCE input pin, a GATE input pin, and an output pin labeled OUT. The Am9513A counters are numbered 1 through 5, and their GATE, SOURCE, and OUT pins are labeled GATE *N*, SOURCE *N*, and OUT *N*, where *N* is the counter number.

For counting operations, the counters can be programmed to use any of the five internal timebases, any of the five GATE and five SOURCE inputs to the Am9513A, and the output of the previous counter (Counter 4 uses Counter 3 output, and so on). A counter can be configured to count either falling or rising edges of the selected input.

The counter GATE input allows counter operation to be gated. Once a counter is configured for an operation through software, a signal at the GATE input can be used to start and stop counter operation. There are five gating modes supported by the Am9513A: no gating, level gating active high, level gating active low, low-to-high edge gating, and high-to-low edge gating. A counter can also be active high level gated by a signal at GATE *N*+1 and GATE *N*-1, where *N* is the counter number.

The counter generates timing signals at its OUT output pin. The OUT output pin can also be set to a high-impedance state or a grounded output state. The counters generate two types of output signals during counter operation: terminal count (TC) pulse output, and TC toggle output. A counter reaches TC when it counts up or down and rolls over. In many counter applications, the counter reloads from an internal register when it reaches TC. In TC pulse output mode, the counter generates a pulse during the cycle that it reaches TC and reloads. In TC toggle output mode, the counter output changes state after it reaches TC and reloads. In addition, the counters can be configured for positive logic output or negative (inverted) logic output for a total of four possible output signals generated for one timing mode.

The SOURCE, GATE, and OUT pins for Counters 1, 2, and 5 of the onboard Am9513A are located on the NB-MIO-16X I/O connector. A rising edge signal on the STOPTRIG pin of the I/O connector sets the flip-flop output signal connected to the GATE4 input of the Am9513A and can be used as an additional gate input. The flip-flop output connected to GATE4 is cleared when the sample counter reaches TC, when an overflow or overrun occurs, or when the A/D Clear Register is written to.

The Am9513A SOURCE5 pin is connected to the NB-MIO-16X RTSI switch, which means that a signal from the RTSI trigger bus can be used as a counting source for the Am9513A counters.

The Am9513A OUT2 pin can be used in several different ways. If the TMRWGEN bit is set in Command Register 1, an active low pulse on OUT2 updates the analog output on the two DACs. OUT2 can also be used to trigger interrupt requests. If this bit is set, an interrupt occurs when a rising edge signal is detected on OUT2. This interrupt can be used to update the DACs or to interrupt on an external signal connected to OUT2 through the I/O connector.

Counters 3 and 4 of the Am9513A are dedicated to data acquisition timing and therefore are not made available for general-purpose timing applications. Signals generated at OUT3 and OUT4 are provided to the data acquisition timing circuitry. GATE3 is controlled by the data acquisition timing circuitry.

Counter 5 is used by the data acquisition timing circuitry and concatenated with Counter 4 to form a 32-bit sample counter whenever the 16*/32CNT bit in Command Register 1 is set high. The SCANCLK signal is connected to the SOURCE3 input of the Am9513A. OUT1 can be used to divide the SCANCLK signal for generating the MUXCTRCLK signal (see *Data Acquisition Timing Circuitry* earlier in this chapter).

Counter 2 is sometimes used by the data acquisition timing circuitry to assign a time interval to each cycle through the scan sequence programmed in the mux-gain memory. This mode is called interval channel scanning. See *Multiple-Channel (Scanned) Data Acquisition* earlier in this chapter.

The Am9513A 4-bit programmable frequency output channel is provided at the I/O connector FOUT pin. Any of the five internal timebases and any of the counter SOURCE or GATE inputs can be selected as the frequency output source. The frequency output channel divides the selected source by its 4-bit programmed value and provides the divided-down signal at the FOUT pin.

RTSI Bus Interface Circuitry

The NB-MIO-16X is interfaced to the National Instrument RTSI bus. The RTSI bus has seven trigger lines, seven DMA request lines, and eight interrupt lines. All National Instruments NB Series boards with RTSI bus connectors can be wired together inside the Macintosh and share these signals. A block diagram of the RTSI bus interface circuitry is shown in Figure 3-8.

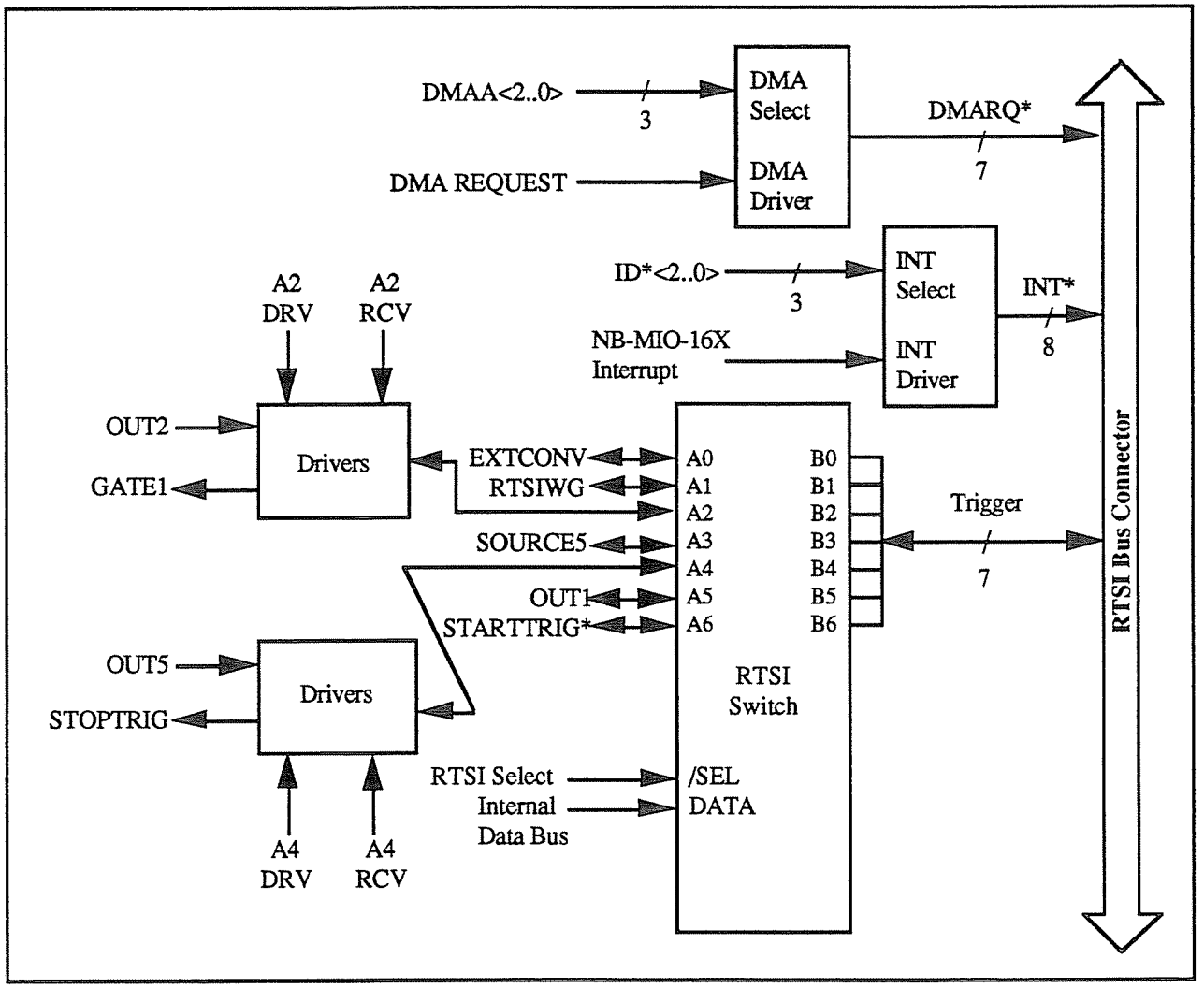


Figure 3-8. RTSI Bus Interface Circuitry Block Diagram

Figure 3-8 shows the DMA driver circuitry, the interrupt driver circuitry, and the RTSI switch. These drivers and the RTSI switch route NB-MIO-16X signals to and from the RTSI bus.

The seven RTSI DMA request lines are driven by the DMA driver circuitry. The DMA driver routes the NB-MIO-16X DMA request signal onto the DMA request line selected by the bits DMAA<2..0>. DMAA<2..0> are controlled by an NB-MIO-16X register.

The eight RTSI interrupt lines are driven by the interrupt driver circuitry. The interrupt driver routes the NB-MIO-16X interrupt signal onto the interrupt line selected by the bits ID*<2..0>. ID*<2..0> are provided at the NuBus connector and are unique to each NuBus slot; therefore the RTSI interrupt line selected is determined by the slot containing the NB-MIO-16X board.

The RTSI switch is a National Instruments custom integrated circuit that acts as a seven by seven crossbar switch. Pins B<6..0> are connected to the seven RTSI bus trigger lines. Pins A<6..0> are connected to seven signals on the board. The RTSI switch can drive any of the signals at pins A<6..0> onto any one or more of the seven RTSI bus trigger lines and can drive any of the seven trigger line signals onto any one or more of the pins A<6..0>. This capability provides a

completely flexible signal interconnection scheme for any NB Series board sharing the RTSI bus. The RTSI switch is programmed via its select and data inputs.

On the NB-MIO-16X board, nine signals are connected to pins A<6..0> of the RTSI switch with the aid of additional drivers. The signals GATE1, OUT1, OUT2, OUT5, and STOPTRIG are shared with the NB-MIO-16X I/O connector and Am9513A Counter/Timer. The SOURCE5 signal is connected to the Am9513A SOURCE5 pin. The EXTCONV* and STARTTRIG* signals are shared with the I/O connector and the data acquisition timing circuitry. The RTSIWG signal is connected to the D/A circuitry to permit use of timing signals from the RTSI for waveform generation. These onboard interconnections allow NB-MIO-16X general-purpose and data acquisition timing to be controlled over the RTSI bus as well as externally and allow the NB-MIO-16X and the I/O connector to provide timing signals to other NB Series boards connected to the RTSI bus.

Chapter 4
Programming

This chapter describes in detail the address and function of each of the NB-MIO-16X registers. This chapter also includes important information about programming the NB-MIO-16X.

Register Access

The Macintosh uses memory mapping to access boards in the system. The following sections discuss how to access the various registers on the NB-MIO-16X.

Slot Address Space

Each slot in the Macintosh is allocated a block of Macintosh memory addresses known as the *slot address space.* All I/O boards plugged into Macintosh NuBus slots are therefore memory mapped. When an I/O board is plugged into a given slot, the board's registers can be accessed within that slot address space. The block of memory addresses allocated to each slot depends on the slot number and whether the Macintosh memory manager is in 24-bit or 32-bit addressing mode. Consult your Macintosh manual to determine the slot numbers used in your computer. Table 4-1 shows the slot address space for each slot, both for 24-bit mode and for 32-bit mode.

Table 4-1. Macintosh Slot Addresses

Slot Number	Starting Address (Hex)	Ending Address (Hex)
24-Bit Mode		
9	0090 0000	009F FFFF
A	00A0 0000	00AF FFFF
B	00B0 0000	00BF FFFF
C	00C0 0000	00CF FFFF
D	00D0 0000	00DF FFFF
E	00E0 0000	00EF FFFF
32-Bit Mode		
0	F000 0000	F0FF FFFF
1	F100 0000	F1FF FFFF
2	F200 0000	F2FF FFFF
3	F300 0000	F3FF FFFF
4	F400 0000	F4FF FFFF
5	F500 0000	F5FF FFFF
6	F600 0000	F6FF FFFF
7	F700 0000	F7FF FFFF
8	F800 0000	F8FF FFFF
9	F900 0000	F9FF FFFF
A	FA00 0000	FAFF FFFF
B	FB00 0000	FBFF FFFF
C	FC00 0000	FCFF FFFF
D	FD00 0000	FDFF FFFF
E	FE00 0000	FEFF FFFF

Register Map

The register map for the NB-MIO-16X is shown in Table 4-2. This table lists the register name, the register address offset from the slot starting address, the type of the register (read only, write only, or read and write), and the size of the register in bits.

Each register address in Table 4-2 is the offset address from the slot starting address. To calculate the absolute address of the register, add the register offset given in Table 4-2 to the slot starting address given in Table 4-1. For example, if the NB-MIO-16X is plugged into slot B and the memory manager is in 24-bit mode, the A/D Clear Register is at address 00 0018 + B0 0000, that is, address B0 0018 (hex). If the NB-MIO-16X is plugged into slot B and the memory manager is in 32-bit mode, the RTSI Switch Strobe Register is at address C 0004 + FB00 0000, that is, address FB0C 0004.

The address decoding circuitry on the NB-MIO-16X is such that using a slot starting address of Fss0 0000 (where the *s* is replaced by the slot number) properly accesses all registers in both memory modes.

Table 4-2. NB-MIO-16X Register Map

Register Name	Address (Hex)	Type	Size
Configuration and Status Register Group:			
Status Register	Base address + 0	Read-only	16-bit
Command Register 1	Base address + 0	Write-only	16-bit
Command Register 2	Base address + 4	Write-only	16-bit
Event Strobe Register Group:			
Start Convert Register	Base address + 10	Write-only	16-bit
Start DAQ Register	Base address + 14	Write-only	16-bit
A/D Clear Register	Base address + 18	Write-only	16-bit
External Multiplexer Strobe Register	Base address + 1C	Write-only	16-bit
Internal Calibration Register	Base address + 2 0000	Write-only	16-bit
Analog Output Register Group:			
DAC0 Register	Base address + 20	Write-only	16-bit
DAC1 Register	Base address + 24	Write-only	16-bit
TMRINTCL Register	Base address + 4 0000	Write-only	16-bit
Analog Input Register Group:			
Mux-Counter Register	Base address + 8	Write-only	16-bit
Mux-Gain Register	Base address + C	Write-only	16-bit
A/D FIFO Register	Base address + 2C	Read-only	16-bit
Am9513A Counter/Timer Register Group:			
Am9513A Data Register	Base address + 30	Read-and-write	16-bit
Am9513A Command Register	Base address + 34	Write-only	16-bit
Am9513A Status Register	Base address + 34	Read-only	16-bit
Digital I/O Register Group:			
Digital Input Register	Base address + 38	Read-only	16-bit
Digital Output Register	Base address + 38	Write-only	16-bit
RTSI Switch Register Group:			
RTSI Switch Shift Register	Base address + C 0000	Write-only	8-bit
RTSI Switch Strobe Register	Base address + C 0004	Write-only	8-bit

Register Sizes

The Macintosh supports three different memory word sizes for memory read and write operations: byte (8-bit), half-word (16-bit), and word (32-bit). Table 4-2 shows the word sizes of the NB-MIO-16X registers. For example, reading the A/D FIFO Memory Register requires a 16-bit (half-word) read operation at the specified address, whereas writing to the RTSI Switch Strobe Register requires an 8-bit (byte) write operation at the specified address.

Register Description

Table 4-2 divides the NB-MIO-16X registers into seven different register groups. A bit description of each of the registers making up these groups is included later in this chapter.

The Configuration and Status Register Group controls the overall operation of the NB-MIO-16X hardware. The Event Strobe Group is a group of registers that, when written to, generate some events on the NB-MIO-16X board. The registers in the Analog Output Group access the NB-MIO-16X DACs. The Analog Input Group allows the ADC output to be read. The Counter/Timer Group consists of the three registers of the onboard Am9513A Counter/Timer chip. The registers in the Digital I/O Group access the onboard digital input and output lines. The registers in the RTSI Switch Group control the onboard RTSI switch. Finally, the configuration EPROM is not a set of registers but rather onboard read-only memory that contains information required by the Macintosh operating system.

Register Description Format

The remainder of this register description section discusses each of the NB-MIO-16X registers in the order shown in Table 4-2. Each register group is introduced, followed by a detailed bit description of each register. The individual register description gives the address, type, word size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the most significant bit (bit 15 for a 16-bit register, bit 7 for an 8-bit register) shown on the left, and the least significant bit (bit 0) shown on the right. A rectangle is used to represent each bit. Each bit is labeled with a name inside its rectangle. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic).

In many of the registers, several bits are labeled with an X, indicating that these bits are *don't care bits*. When a register is read, these bits may appear set or cleared but should be ignored because they are not used. When a register is written to, setting or clearing these bit locations has no effect on the NB-MIO-16X hardware.

The bit map field for some write-only registers may contain the message *not applicable, no bits used.* Writing to these registers generates a strobe in the NB-MIO-16X. These strobes are used to cause some onboard events to occur. For example, they can be used to clear the analog input circuitry or to start a data acquisition operation. The data itself is actually ignored when writing to these registers; therefore, any bit pattern will suffice.

Configuration and Status Register Group

The three registers making up the Configuration and Status Register Group allow general control and monitoring of the NB-MIO-16X hardware. Command Registers 1 and 2 contain bits that control operation of several different pieces of the NB-MIO-16X hardware. The Status Register can be used to read the state of different parts of the NB-MIO-16X hardware.

Bit descriptions of the three registers making up the Configuration and Status Group are given on the following pages.

Status Register

The Status Register contains 14 bits of NB-MIO-16X hardware status information, including interrupt and analog input status.

Address: Base address + 0 (hex)

Type: Read-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
INT*	CMPLINT	CONVAVAIL	X	DAQPROG	X	OVERFLOW	OVERRUN

7	6	5	4	3	2	1	0
GAIN1	GAIN0	TIMERUP	MUX1EN	MUX0EN	MA2	MA1	MA0

Bit	Name	Description
15	INT*	This bit reflects the overall state of interrupts generated by the NB-MIO-16X board. If INT* is cleared, the NB-MIO-16X is asserting an interrupt request that has not yet been serviced. If INT* is set, no interrupt is pending. This bit is normally set.
14	CMPLINT	This bit reflects the status of the CMPLINT interrupt. If CMPLINT is set, the current interrupt is due to the completion of a data acquisition operation. CMPLINT is cleared by writing to the A/D Clear Register. CMPLINT interrupts are enabled by the CMPLINTEN bit in Command Register 1.
13	CONVAVAIL	This bit reflects the state of the A/D FIFO. If CONVAVAIL is set, one or more A/D conversion results are available to be read from the A/D FIFO. If conversion interrupts are enabled (CONVINTEN set) and CONVAVAIL is set, the current interrupt indicates that A/D conversion data is available in the A/D FIFO. If CONVAVAIL is cleared, the A/D FIFO is empty and no conversion interrupt request has been asserted.
12	X	Don't care bit.
11	DAQPROG	If DAQPROG is set, a data acquisition operation is in progress. If DAQPROG is cleared, a data acquisition operation is not in progress. This bit is meaningful only for data acquisition operations that are timed internally. For instance, if EXTCONV* is being used to time data acquisition, then DAQPROG does not indicate anything.
10	X	Don't care bit.

Bit	Name	Description (continued)
9	OVERFLOW	This bit indicates whether the A/D FIFO has overflowed during a sample run. OVERFLOW is an error condition that occurs if the FIFO fills up with A/D conversion data and A/D conversions continue. If OVERFLOW is set, A/D conversion data has been lost because of FIFO overflow. If OVERFLOW is cleared, no overflow has occurred. This bit can be reset by writing to the A/D Clear Register.
8	OVERRUN	This bit indicates whether an A/D conversion was initiated before the previous A/D conversion was complete. OVERRUN is an error condition that may occur if the data acquisition sample interval is too small (sample rate is too high). If OVERRUN is set, one or more conversions were skipped. If OVERRUN is cleared, no overrun condition has occurred. This bit can be reset by writing to the A/D Clear Register.
7-6	GAIN<1..0>	These two bits show the current gain setting for the programmable gain amplifier (see Mux-Gain Register).
5	TIMERUP	This bit reflects the status of the TMRINT interrupt. If it is set and TMRINTEN has been set, the current interrupt is due to a rising edge on the OUT2 signal. TIMERUP is cleared by writing to the TMRINTCL Register, or by writing to either DAC0 or DAC1. TIMERUP is set whenever a rising edge on OUT2 is detected; this condition generates an interrupt request only if the TMRINTEN bit in Command Register 1 is set. If that bit is not set, TIMERUP still indicates that there been a rising edge edge on OUT2, but an interrupt is not generated.
4	MUX1EN	This bit indicates the state of Multiplexer 1, which selects analog input channels 8 through 15. If this bit is set, then this multiplexer is enabled; otherwise, it is disabled. In single-ended mode, this bit is set if any of channels 8 through 15 are selected. In DIFF mode, this bit is always set.
3	MUX0EN	This bit indicates the state of Multiplexer 0, which selects analog input channels 0 through 7. If this bit is set, then this multiplexer is enabled; otherwise, it is disabled. In single-ended mode, this bit is set if any of channels 0 through 7 are selected. In DIFF mode, this bit is always set.
2-0	MA<2..0>	These three bits give the low-order three bits of the analog input channel address. MA stands for multiplexer address. These three bits, in conjunction with the MUX1EN and MUX0EN bits, indicate which analog input channel is currently selected. In single-ended mode, the analog input channel selected is determined by the value of MA<2..0> if MUX0EN is set, and by the value of MA<2..0> plus eight if MUX1EN is set. In DIFF mode, two analog input channels are selected simultaneously. The two channels are MA<2..0> and MA<2..0> plus eight.

Command Register 1

Command Register 1 contains 16 bits that control NB-MIO-16X interrupts, DMA, and some analog input and output modes.

Address: Base address + 0 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
RTSIWGEN	TMRWGEN	TMRINTEN	SCN2	BP*/UP	CLK2	CLK1	CLK0

7	6	5	4	3	2	1	0
CMPLINTEN	CONVINTEN	DMAEN	DAQEN	SCANEN	SCANDIV	16*/32CNT	2SCADC*

Bit	Name	Description
15	RTSIWGEN	This bit enables or disables control of output waveform generation (using the DACs) by signals on the RTSI bus.
14	TMRWGEN	This bit enables or disables control of output waveform generation by the OUT2 signal from the Am9513A.
13	TMRINTEN	This bit enables or disables the generating of interrupts by Counter 2 on the Am9513A. If enabled, an interrupt is generated on the rising edge of OUT2. This bit can be used in conjunction with TMRWGEN so that an interrupt service routine updates the DACs automatically or it may be used by itself. Interrupts generated from OUT2 are cleared by the TMRINTCL register, to be discussed later.
12	SCN2	This bit selects the data acquisition scanning mode used when scanning multiple A/D channels. If SCN2 is cleared, continuous channel scanning is used. In this mode, scan sequences are repeated with no delays between cycles. If SCN2 is set, interval channel scanning is used. In this mode, scan sequences occur during a programmed time interval, called a *scan interval*. One cycle of the scan sequence occurs during each scan interval.
11	BP*/UP	This bit sets, in part, the input range of the ADC. If this bit is set, the A/D is set in unipolar mode (0 to 10 V or 0 to 5 V). If it is cleared, the A/D is set in bipolar mode (-10 to +10 V or -5 to +5 V).

Bit	Name	Description (continued)
10-8	CLK<2..0>	These three bits select the internal clock rate for the ADC. CLK<2..0> should be set to 0 0 1 for the NB-MIO-16X-42 and 0 1 0 for the NB-MIO-16X-18. Setting them to 0.0.0 generates a slow internal clock rate, which produces unreliable conversions, and so this combination should not be used. Setting them to 0 1 1 results in a very high internal clock rate. This setting permits the ADC on the NB-MIO-16X-18 to sample as fast as about 10 µsec, but at reduced and unspecified accuracy.
7	CMPLINTEN	This bit enables or disables generation of an interrupt at the completion of a data acquisition operation. A data acquisition operation is a multiple A/D conversion sequence that is timed and controlled by the NB-MIO-16X onboard counter/timers. The onboard sample counter generates this interrupt when it counts down to 0 and the A/D conversion scan sequence is complete. If external conversion timing is used, this interrupt does not occur. If this bit is set, an interrupt is generated whenever a data acquisition operation completes. If this bit is cleared, no interrupt is generated. Notice that the CMPLINT interrupt is asserted when the last conversion of a data acquisition operation is started, not when the last conversion is finished.
6	CONVINTEN	This bit enables and disables the generation of an interrupt when A/D conversion results are available. If CONVINTEN is set, an interrupt is generated whenever an A/D conversion is available to be read from the A/D FIFO. If CONVINTEN is cleared, no interrupt is generated.
5	DMAEN	This bit enables and disables the generation of DMA requests. If DMAEN is set, a DMA request is generated whenever an A/D conversion result is available to be read from the A/D FIFO. If DMAEN is cleared, no DMA request is generated.
4	DAQEN	This bit enables and disables a data acquisition operation that is controlled by the onboard sample-interval and sample counters. If DAQEN is set, a software or start trigger starts the counters (assuming that the counters are programmed and enabled), thereby starting a data acquisition operation. If DAQEN is cleared, software and start triggers are ignored.
3	SCANEN	This bit enables and disables multiple-channel scanning during data acquisition. If SCANEN is set, alternate analog input channels are sampled during data acquisition under control of the mux-gain memory. If SCANEN is cleared, a single analog input channel is sampled during the entire data acquisition operation.
2	SCANDIV	This bit enables and disables division of the mux-counter clock during data acquisition. The mux-counter clock controls sequencing of the mux-gain memory. If SCANDIV is set, the mux-counter clock is controlled by Counter 1 of the Am9513A Counter/Timer. If SCANDIV is cleared, the mux-counter clock generates one pulse per conversion.

Bit	Name	Description (continued)
1	16*/32CNT	This bit selects the count resolution for the number of A/D conversions to be performed in a data acquisition operation. If 16*/32CNT is cleared, a 16-bit count mode is selected and Counter 4 of the Am9513A Counter/Timer controls conversion counting. If 16*/32CNT is set, a 32-bit count mode is selected and Counter 4 is concatenated with Counter 5 to control conversion counting. A 16-bit count mode can be used if the number of A/D sample conversions to be performed is less than or equal to 65,536. A 32-bit count mode should be used if the number of A/D sample conversions to be performed is greater than or equal to 65,536.
0	2SCADC*	This bit selects the binary format for the 16-bit data word read from the A/D FIFO. If 2SCADC* is set, a straight binary format is used and the data read from the A/D FIFO ranges from 0 to +65,535 decimal (0 to FFFF hex). This mode is useful if a unipolar input range is used. If 2SCADC* is cleared, a 16-bit two's complement mode is used and the data read from the ADC ranges from -32,768 to +32,767 decimal (8000 to 7FFF hex). This mode is useful if a bipolar input range is used.

Command Register 2

Command Register 2 contains 10 bits that control NB-MIO-16X digital output drivers and scan modes used by the data acquisition circuitry.

Address: Base address + 4 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	DOUTBEN	DOUTAEN

7	6	5	4	3	2	1	0
NBINTDIS	DMAA2	DMAA1	DMAA0	A4RCV	A4DRV	A2RCV	A2DRV

Bit	Name	Description
15-10	X	Don't care bits.
9	DOUTBEN	This bit enables and disables driving of the 4-bit digital output Port B by the Digital Output Register. If DOUTBEN is set, the Digital Output Register drives the digital lines. If DOUTBEN is cleared, the Digital Output Register drivers are set to a high-impedance state, thereby allowing an external device to drive the digital lines.
8	DOUTAEN	This bit enables and disables driving of the 4-bit digital output Port A by the Digital Output Register. If DOUTAEN is set, the Digital Output Register drives the digital lines. If DOUTAEN is cleared, the Digital Output Register drivers are set to a high-impedance state, thereby allowing an external device to drive the digital lines.
7	NBINTDIS	This bit disables or enables driving of the NuBus NMR interrupt line by the NB-MIO-16X interrupt line. If this bit is cleared, the NuBus NMR line is driven by the NB-MIO-16X interrupt line. If this bit is set, no interrupts are ever asserted onto the NuBus by the NB-MIO-16X. **Note:** This bit is normally cleared, which means that interrupts are normally gated onto the NuBus.
6-4	DMAA<2..0>	These three bits specify which RTSI bus DMA channel is to be used, and specify the RTSI DMA request line for routing DMA requests. For example, to select DMA channel 2, set bits 6 through 4 to 0 1 0 (binary), respectively. DMA requests generated by the NB-MIO-16X are then gated onto DMA request line 2 of the RTSI bus. DMA operation is enabled by setting the DMAEN bit in Command Register 1.

Bit	Name	Description (continued)
3	A4RCV	This bit controls a driver that allows the STOPTRIG signal to be driven from pin A4 of the RTSI switch. This bit allows a signal to be received from one of the RTSI bus trigger lines and driven onto the STOPTRIG line. If A4RCV is set, pin A4 of the RTSI switch drives the STOPTRIG signal. If A4RCV is cleared, the STOPTRIG signal is not driven by the RTSI switch.
2	A4DRV	This bit controls a driver that allows the OUT5 signal to drive pin A4 of the RTSI switch. This driver allows the OUT5 signal to be driven onto one of the RTSI bus trigger lines. If A4DRV is set, pin A4 of the RTSI switch is driven by OUT5. If A4DRV is cleared, the pin A4 is not driven.
1	A2RCV	This bit controls a driver that allows the GATE1 signal to be driven from pin A2 of the RTSI switch. This driver allows a signal to be received from one of the RTSI bus trigger lines and driven onto the GATE1 line. If A2RCV is set, pin A2 of the RTSI switch drives the GATE1 signal. If A2RCV is cleared, the GATE1 signal is not driven by the RTSI switch.
0	A2DRV	This bit controls a driver that allows the OUT2 signal to drive pin A2 of the RTSI switch. This driver allows the OUT2 signal to be driven onto one of the RTSI bus trigger lines. If A2DRV is set, pin A2 of the RTSI switch is driven by OUT2. If A2DRV is cleared, pin A2 is not driven.

The Event Strobe Register Group

The Event Strobe Register Group consists of five registers that, when written to, cause certain events to occur on the NB-MIO-16X board, such as clearing flags and starting A/D conversions. They are the Start Convert, Start DAQ, A/D Clear, Internal Calibration, and External Multiplexer Strobe Registers.

Descriptions of the these registers are given on the following pages.

Start Convert Register

Writing to the Start Convert Register location initiates an A/D conversion.

Address: Base address + 10 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

Note: A/D conversions are initiated in one of two ways: when the Start Convert Register is written to, or when an active low signal is detected on the EXTCONV* signal. The EXTCONV* signal is connected to pin 40 on the I/O connector, to OUT3 of the Am9513A, and to pin A0 of the RTSI bus switch. If EXTCONV* is driven low by any one of these sources, it prevents the Start Convert Register from initiating an A/D conversion. If the Start Convert Register is to initiate A/D conversions, the OUT3 signal should be initialized to a high-impedance state, any signal connected to pin 40 of the I/O connector should be in a high-impedance or high state, and the A0 pin of the RTSI bus switch should be configured as an input pin.

Start DAQ Register

Writing to the Start DAQ Register location initiates a multiple A/D conversion data acquisition operation.

Note: Several other pieces of NB-MIO-16X circuitry must be set up before a data acquisition run can occur. See *Programming Multiple A/D Conversions on a Single Input Channel* later in this chapter.

Address: Base address + 14 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

Note: Multiple A/D conversion data acquisition operations are initiated in one of two ways: when the Start DAQ Register is written to, or when an active low signal is detected on the STARTTRIG* signal. The STARTTRIG* signal is connected to pin 38 on the I/O connector and to pin A6 of the RTSI bus switch. If STARTTRIG* is driven low by either of these sources, it prevents the Start DAQ Register from initiating a multiple A/D conversion data acquisition operation. If the Start DAQ Register is to initiate multiple A/D conversions, any signal connected to pin 38 of the I/O connector should be in a high-impedance or high state and the A6 pin of the RTSI bus switch should be configured as an input pin.

A/D Clear Register

Writing to the A/D Clear Register location clears the data acquisition circuitry. The following specific events occur:

- Any data acquisition operation in progress is canceled.
- The A/D FIFO is emptied.
- The overrun flag is cleared.
- The overflow flag is cleared.
- Any pending CONV interrupt is cleared.
- Any pending CMPL interrupt is cleared.
- Any pending DMA request is cleared.

Address: Base address + 18 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

External Multiplexer Strobe Register

Writing to the External Multiplexer Strobe Register location generates an active low, approximately 100 nsec strobe pulse at the EXTSTROBE* output at the I/O connector. This pulse may be useful for several applications, including generating external general-purpose triggers and latching data into external devices (from the digital output port, for example).

Address: Base address + 1C (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

Internal Calibration Register

Writing to the Internal Calibration Register location initiates a calibration sequence in the ADC on the NB-MIO-16X. Calibration is necessary for the board to operate within specification because the ADC must manipulate some internal bit-weights to achieve high linearity. Before the Internal Calibration Register is written to, the CLK<2..0> bits should be set to 0 0 1. Afterwards they may be set as desired, preferably as indicated in their description (under Command Register 1).

Address: Base address + 2 0000 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

Analog Output Register Group

Two of the three registers making up the Analog Output Register Group load the two analog output channels. DAC0 controls analog output Channel 0. DAC1 controls analog output Channel 1. These DACs are written to individually, and the analog output can be updated immediately or each time an active low pulse is detected on the OUT2 bit of the Am9513A Counter/Timer. The update method is selected with the TMRWGEN and RTSIWGEN bits in Command Register 1.

The third register in the Analog Output Register Group is the TMRINTCL Register. The NB-MIO-16X can be programmed to interrupt when it detects a rising edge signal on the OUT2 pin of the Am9513A Counter/Timer. This interrupt can be cleared by writing to DAC0, DAC1, or the TMRINTCL Register.

The following pages contain descriptions of the registers making up the Analog Output Register Group.

DAC0, DAC1 Registers

Writing to DAC0 or DAC1 loads the corresponding analog output channel DAC. The voltages generated by the analog output channels are updated either immediately or when an active low pulse occurs on OUT2 or on pin A1 of the RTSI switch. The update method is selected by the TMRWGEN and RTSIWGEN bits in Command Register 1. Writing to DAC0 or DAC1 also clears interrupts enabled by TMRINTEN.

Address: Base address + 20 (hex) loads DAC0
Base address + 24 (hex) loads DAC1

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				MSB											LSB

Bit	Name	Description
15-12	X	Don't care bits.
11-0	D<11..0>	These twelve bits are loaded into the DAC and update the voltage generated by the analog output channel in one of two ways–immediately, or upon an OUT2 pulse. See *Programming the Analog Output Circuitry* later in this chapter for a table mapping digital values to output voltage.

TMRINTCL Register

Writing to TMRINTCL clears the interrupt request asserted when an OUT2 pulse is detected.

Address: Base address + 4 0000 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

Analog Input Register Group

The three registers making up the Analog Input Register Group control the analog input circuitry and allow the A/D FIFO to be read from. The Mux-Counter Register generates addresses for the mux-gain memory. The Mux-Gain Register controls the current multiplexer and gain settings and allows the mux-gain memory to be written to. Reading the A/D FIFO Register returns stored A/D conversion results.

The following pages contain bit descriptions for the registers making up the Analog Input Register Group.

Mux-Counter Register

The Mux-Counter Register loads the counter that sequences through the mux-gain memory.

Address: Base address + 8 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	MC3	MC2	MC1	MC0

Bit	Name	Description
15-4	X	Don't care bits.
3-0	MC<3..0>	These four bits are loaded into the mux counter by writing to the Mux-Counter Register. The mux counter generates addresses for the mux-gain memory; therefore, writing to the Mux-Counter Register allows a specific location in the mux-gain memory to be addressed. The mux-gain memory contains a sequence of multiplexer addresses and gain settings. For example, writing 0.0.0.4 hex to the Mux-Counter Register loads the mux counter with the value 4, and thus addresses mux-gain memory location 4. The analog circuitry is then controlled by the multiplexer address and gain settings in mux-gain memory location 4 (see the Mux-Gain Register description later in this chapter).

Mux-Gain Register

The Mux-Gain Register controls the multiplexer and gain settings, and, when used in conjunction with the Mux-Counter Register, allows a scan sequence to load into the mux-gain memory.

Address: Base address + C (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
GAIN1	GAIN0	X	LASTONE	MA3	MA2	MA1	MA0

Bit	Name	Description
15-8	X	Don't care bits.
7-6	GAIN<1..0>	This 2-bit field controls the gain setting of the input instrumentation amplifier. The actual amplifier gains depend on the type of NB-MIO-16X board. The following gains can be selected on the NB-MIO-16XH board:

GAIN<1..0>	Actual Gain
00	1
01	2
10	4
11	8

The following gains can be selected on the NB-MIO-16XL board:

GAIN<1..0>	Actual Gain
00	1
01	10
10	100
11	500

5	X	Don't care bit.
4	LASTONE	This bit should be left clear normally and set only in the last entry of the scan sequence loaded into the mux-gain memory. Setting this bit tells the NB-MIO-16X that this entry is the last in the sequence.

Bit	Name	Description (continued)
3-0	MA<3..0>	This 4-bit field controls the multiplexer address setting of the input multiplexers, thereby allowing the analog input channel to be selected. In single-ended mode (NRSE or RSE), only one analog input channel is selected. In DIFF mode, two analog input channels are selected. The analog input channel selected for either mode is shown here:

MA<3..0>	Selected Analog Input Channels	
	Single-Ended	DIFF (+) (-)
0 0 0 0	0	0 & 8
0 0 0 1	1	1 & 9
0 0 1 0	2	2 & 10
0 0 1 1	3	3 & 11
0 1 0 0	4	4 & 12
0 1 0 1	5	5 & 13
0 1 1 0	6	6 & 14
0 1 1 1	7	7 & 15
1 0 0 0	8	0 & 8
1 0 0 1	9	1 & 9
1 0 1 0	10	2 & 10
1 0 1 1	11	3 & 11
1 1 0 0	12	4 & 12
1 1 0 1	13	5 & 13
1 1 1 0	14	6 & 14
1 1 1 1	15	7 & 15

Writing to the Mux-Gain Register updates the current analog input channel selection and the current gain setting. The mux-gain memory is also loaded by writing to the Mux-Gain Register. The mux counter is written to in order to address a specific location in the mux-gain memory. Any subsequent value written to the Mux-Gain Register is then stored in that memory location as well as applied to the analog input multiplexer and gain circuitry.

A/D FIFO Register

Reading the A/D FIFO Register returns the oldest A/D conversion value stored in the A/D FIFO. Whenever the A/D FIFO is read, the value read is removed from the A/D FIFO, thereby leaving space for another A/D conversion value to be stored. Values are stored into the A/D FIFO by the ADC whenever an A/D conversion is complete.

The A/D FIFO is emptied when all values it contains are read. The Status Register should be read before the A/D FIFO Register is read. If the A/D FIFO contains one or more A/D conversion values, the CONVAVAIL bit is set in the Status Register and the A/D FIFO Register can be read to retrieve a value. If the CONVAVAIL bit is cleared, the A/D FIFO is empty, in which case reading the A/D FIFO Register returns meaningless information.

The values returned by reading the A/D FIFO Register are available in two different binary formats: straight binary, which generates only positive numbers, or two's complement binary, which generates both positive and negative numbers. The binary format used is selected by the 2SCADC* bit in Command Register 1. The bit pattern returned for either format is as follows.

Address: Base address + 2C (hex)

Type: Read-only

Word Size: 16-bit

Bit Map: Straight binary mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB															LSB

Bit	Name	Description
15-0	D<15..0>	These bits are the straight binary result of a 16-bit A/D conversion. Values read, therefore, range from 0 to 65,535 decimal (0000 to FFFF hex). Straight binary mode is useful for unipolar analog input readings because all values that are read reflect a positive polarity input signal.

Bit Map: Two's complement binary mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15*	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB															LSB

Bit	Name	Description
15-0	D<15..0>	These bits are the two's complement result of a 16-bit A/D conversion. The difference between this encoding and straight binary is that bit D15 is inverted. Values read, therefore, range from -32,768 to +32,767 decimal (8000 to 7FFF hex). Two's complement mode is useful for bipolar analog input readings because the values read reflect the polarity of the input signal.

Am9513A Counter/Timer Register Group

The three registers making up the Am9513A Counter/Timer Register Group access the onboard Am9513A Counter/Timer. The Am9513A controls onboard data acquisition timing as well as general-purpose timing for the user.

The Am9513A registers described here are the Am9513A Data Register, the Am9513A Command Register, and the Am9513A Status Register. The Am9513A contains 18 additional internal registers. These internal registers are accessed through the Am9513A Data Register. A detailed register description of all Am9513A registers is included in Appendix C, *AMD Data Sheet.*

Bit descriptions for the Am9513A Counter/Timer Register Group registers are given in the following pages.

Am9513A Data Register

The Am9513A Data Register allows any of the 18 internal registers of the Am9513A to be written to or read from. The Am9513A Command Register must be written to in order to select the register to be accessed by the Am9513A Data Register. The internal registers accessed by the Am9513A Data Register are as follows:

- Counter Mode Registers for Counters 1, 2, 3, 4, and 5
- Counter Load Registers for Counters 1, 2, 3, 4, and 5
- Counter Hold Registers for Counters 1, 2, 3, 4, and 5
- The Master Mode Register
- The Compare Registers for Counters 1 and 2

All these registers are 16-bit registers. Bit descriptions for each of these registers are included in Appendix C, *AMD Data Sheet.*

Address: Base address + 30 (hex)

Type: Read-or-write

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
15-0	D<15..0>	These 16 bits are loaded into the Am9513A Internal Register currently selected. See Appendix C, *AMD Data Sheet*, for the detailed bit descriptions of the 18 registers accessed through the Am9513A Data Register.

Am9513A Command Register

The Am9513A Command Register controls the overall operation of the Am9513A Counter/Timer and controls selection of the internal registers accessed through the Am9513A Data Register.

Address: Base address + 34 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	C7	C6	C5	C4	C3	C2	C1	C0

Bit	Name	Description
15-8		These bits must always be set when writing to the Am9513A Command Register.
7-0	C<7..0>	These eight bits are loaded into the Am9513A Command Register. See Appendix C, *AMD Data Sheet*, for the detailed bit description of the Am9513A Command Register.

Am9513A Status Register

The Am9513A Status Register provides information about the output pin status of each counter in the Am9513A.

Address: Base address + 34 (hex)

Type: Read-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	OUT5	OUT4	OUT3	OUT2	OUT1	BYTEPTR

Bit	Name	Description
15-6	X	Don't care bits.
5-1	OUT<5..1>	Each of these five bits returns the logic state of the associated counter output pin. For example, if OUT4 is set, then the output pin of Counter 4 is at a logic high state.
0	BYTEPTR	This bit represents the state of the Am9513A Byte Pointer Flip-Flop. This bit has no significance for NB-MIO-16X operation because the Am9513A should always be used in 16-bit mode on the NB-MIO-16X.

Digital I/O Register Group

The two registers making up the Digital I/O Register Group monitor and control the NB-MIO-16X digital I/O lines. The Digital Input Register returns the digital state of the eight digital I/O lines. A pattern written to the Digital Output Register is driven onto the digital I/O lines when the digital output drivers are enabled (see the description for Command Register 2).

Bit descriptions for the registers making up the Digital I/O Register Group are given on the following pages.

Digital Input Register

The Digital Input Register, when read, returns the logic state of the eight NB-MIO-16X digital I/O lines.

Address: Base address + 38 (hex)

Type: Read-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
BDI3	BDI2	BDI1	BDI0	ADI3	ADI2	ADI1	ADI0

Bit	Name	Description
15-8	X	Don't care bits.
7-4	BDI<3..0>	These four bits represent the logic state of the digital lines BDIO<3..0>.
3-0	ADI<3..0>	These four bits represent the logic state of the digital lines ADIO<3..0>.

Digital Output Register

Writing to the Digital Output Register controls the eight NB-MIO-16X digital I/O lines. The Digital Output Register controls both Ports A and B. When either digital port is enabled, the pattern contained in the Digital Output Register is driven onto the lines of the digital port.

Address: Base address + 38 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
BD03	BD02	BD01	BD00	AD03	AD02	AD01	AD00

Bit	Name	Description
15-8	X	Don't care bits.
7-4	BDO<3..0>	These four bits control the digital lines BDIO<3..0>. The bit DOUTBEN in Command Register 2 must be set for BDO<3..0> to be driven onto the digital lines BDIO<3..0>.
3-0	ADO<3..0>	These four bits control the digital lines ADIO<3..0>. The bit DOUTAEN in Command Register 2 must be set for ADO<3..0> to be driven onto the digital lines ADIO<3..0>.

The RTSI Switch Register Group

The two registers making up the RTSI Switch Register Group allow the NB-MIO-16X RTSI switch to be programmed for routing of signals on the RTSI bus trigger lines to and from several NB-MIO-16X signal lines. The RTSI switch is programmed by shifting a 56-bit routing pattern into the RTSI switch and then loading the internal RTSI Switch Control Register. The routing pattern is shifted into the RTSI switch by writing one bit at a time to the RTSI Switch Shift Register. The RTSI Switch Control Register is then loaded by writing to the RTSI Switch Strobe Register.

Bit descriptions for the registers making up the RTSI Switch Register Group are given on the following pages.

RTSI Switch Shift Register

The RTSI Switch Shift Register is written to in order to load the RTSI switch internal 56-bit control register with routing information for switching signals to and from the RTSI bus trigger lines. The RTSI Switch Shift Register is a 1-bit register and must be written to 56 times to shift the 56 bits into the internal register.

Address: Base address + C 0000 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	RSI

Bit	Name	Description
7-1	X	Don't care bits.
0	RSI	The name of this bit stands for RTSI switch serial input. This bit is the serial input to the RTSI switch. Each time the RTSI Switch Shift Register is written to, the value of this bit is shifted into the RTSI switch. See *Programming the RTSI Switch* later in this chapter for more information.

RTSI Switch Strobe Register

The RTSI Switch Strobe Register is written to in order to load the contents of the RTSI Switch Shift Register into the RTSI Switch Control Register, thereby updating the RTSI switch routing pattern. The RTSI Switch Strobe Register is written to after shifting the 56-bit routing pattern into the RTSI Switch Shift Register.

Address: Base address + C 0004 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map: Not applicable, no bits used

The Configuration EPROM

The Configuration EPROM on the NB-MIO-16X contains information pertinent to the NB-MIO-16X board and is required by the Macintosh. The Macintosh system Slot Manager reads the Configuration EPROM upon system startup.

The Configuration EPROM is mapped to address offset locations F 8000 through F FFFC (hex). The EPROM is 8 bits (one byte) wide and 8 kilobytes in length. Each byte of the EPROM is mapped to every fourth address location on the NB-MIO-16X board–the first byte is read from slot address + F 8000; the second byte is read from slot address + F 8004; the third byte is read from slot address + F 8008, and so on.

Programming Considerations

This section contains programming instructions for operating the circuitry on the NB-MIO-16X board. Programming the NB-MIO-16X involves writing to and reading from the various registers on the board. The programming instructions are language-independent; that is, they instruct you to write a value to a given register, to set or clear a bit in a given register, or to detect whether a given bit is set or cleared without presenting the actual code.

Register Programming Considerations

Several write-only registers on the NB-MIO-16X contain bits that control independent pieces of the onboard circuitry. In the instructions for setting or clearing bits, specific register bits should be set or cleared without changing the current state of the remaining bits in the register. However, writing to these registers affects all register bits simultaneously. You cannot read these registers to determine which bits have been set or cleared in the past; therefore, you should maintain a software copy of the write-only registers. This software copy can then be read to determine the status of the write-only registers. To change the state of a single bit without disturbing the remaining bits, set or clear the bit in the software copy and write the software copy to the register.

Initializing the NB-MIO-16X Board

The NB-MIO-16X hardware must be initialized for the NB-MIO-16X circuitry to operate properly. Use the following procedure to initialize the NB-MIO-16X hardware.

1. Write 0100 (hex) to Command Register 1 (16-bit write) for an NB-MIO-16X-42. This step selects the 2 MHz internal clock rate for the ADC.
2. Write 0080 (hex) to Command Register 2 (16-bit write). This step disables all interrupts from the NB-MIO-16X.
3. Write 0 to the Mux-Gain Register (16-bit write).
4. Initialize the RTSI bus switch (described in the following pages).
5. Initialize the Am9513A (described in the following pages).
6. Perform an internal A/D calibration (described in the following pages).
7. Write 0 to the TMRINTCL Register (16-bit write).
8. Initialize the analog output circuitry (described in the following pages).
9. Write 0 to the Digital Output Register (16-bit write).

This sequence leaves the NB-MIO-16X circuitry in the following state:

- DMA disabled.
- All interrupts disabled.
- Outputs of counter/timers in high-impedance state.
- Analog input circuitry initialized.
- Analog output circuitry initialized.
- ADC calibrated.
- A/D FIFO cleared.
- Analog input channel 0 selected.
- Gain of 1 selected.
- All pins on the RTSI switch configured as input pins.
- Digital output circuitry initialized.

Initializing the RTSI Bus Switch

This procedure configures all signals to the RTSI bus switch as read signals. This configuration guarantees that the RTSI bus switch is not driving the signals connected to it, which may cause undesirable results. All writes are 8-bit operations. Use the following procedure to initialize the RTSI bus switch.

1. For i = 0 to 55 (decimal), write 0 to the RTSI Shift Register (base address + C 0000 hex) to load the RTSI switch with the program data pattern.
2. Write 0 to the RTSI Switch Strobe Register (base address + C 0004 hex) to load the pattern into the RTSI switch.

Initializing the Am9513A

Use the following procedure to initialize the Am9513A Counter/Timer. All writes are 16-bit operations.

1. Issue a master reset by writing FFFF (hex) to the Am9513A Command Register.
2. Set up Am9513A 16-bit mode by writing FFEF (hex) to the Am9513A Command Register.
3. Point to the Am9513A Master Mode Register by writing FF17 (hex) to the Am9513A Command Register.
4. Load the master mode value into the Am9513A Master Mode Register by writing F000 (hex) to the Am9513A Data Register.

5. Initialize all five counters. For *ctr* = 1 through 5, follow these steps:

   a. Write FF00 (hex) + *ctr* to the Am9513A Command Register to select the Counter Mode Register.

   b. Write 0004 (hex) to the Am9513A Data Register to store the counter mode value.

   c. Write FF08 (hex) + *ctr* to the Am9513A Command Register to select the Counter Load Register.

   d. Write 3 to the Am9513A Data Register to store an inactive count value in the Counter Load Register.

6. Load all counters with their Counter Load Register values by writing FF5F (hex) to the Am9513A Command Register.

7. Wait at least 50 µsec, in case an A/D conversion is inadvertently initiated by writing to the Am9513A registers.

8. Write 0 to the A/D Clear Register to reset the board. This ensures that the A/D FIFO is cleared in case a conversion was initiated inadvertently.

After this sequence of writes, the Am9513A Counter/Timer is in the following state:

- 16-bit mode is enabled.
- BCD scalar division is selected.
- The FOUT signal is turned off.
- All counter OUT output pins are set to high-impedance output state.
- All counters are loaded with a non-terminal count value.

For additional details concerning the Am9513A Counter/Timer, see Appendix C, *AMD Data Sheet.*

Note: If a data acquisition operation is executed *and* Counter 4 of Am9513A is not used, then write 0000 (hex) to the Am9513A Data Register (instead of 0004 hex) when *ctr* = 4. Writing 0000 (hex) to the Am9513A Data Register causes the output of Counter 4 to be low and therefore prevents improper termination of the data acquisition operation.

Performing an Internal ADC Calibration

Use the following procedure to internally calibrate the ADC. This takes roughly 0.75 sec. No other activity should be taking place on the board other than reading the Status Register to verify if the calibration is finished.

1. Write 0 to the Internal Calibration Register.

2. Repeatedly read the Status Register (16-bit read) until the CONVAVAIL bit is set.

3. Write 0 to the A/D Clear Register.

Initializing the Analog Output Circuitry

The NB-MIO-16X starts up with the analog output circuitry at an unknown voltage. For most applications, the analog output circuitry should be initialized to 0 V.

If the analog output channel is configured for unipolar operation, write 0 to the DAC Register (16-bit write) for that channel.

If the analog output channel is configured for two's complement bipolar output, write 0 to the DAC Register (16-bit write) for that channel.

If the analog output channel is configured for straight binary bipolar output, write 2,048 (07FF hex) to the DAC Register (16-bit write) for that channel.

Programming the Analog Input Circuitry

To program the analog input circuitry to obtain a single A/D conversion, follow these steps:

1. Select analog input channel and gain.
2. Initiate an A/D conversion.
3. Read the A/D conversion result.

In addition, the binary format of the A/D conversion result can be programmed and the analog input circuitry can be reset.

1. Select analog input channel and gain.

The analog input channel and gain are selected by writing to the Mux-Gain Register. Bits 7 and 6 control the gain, and bits 3 through 0 select the analog input channel. See the Mux-Gain Register bit description earlier in this chapter for gain and analog input channel bit patterns. Set up the bits as given in the Mux-Gain Register bit description and write to the Mux-Gain Register.

Once the Mux-Gain Register is set up, it needs to be written to only when the analog input channel or gain setting needs to be changed.

2. Initiate an A/D conversion.

An A/D conversion can be initiated in one of two ways–a software-generated pulse, or a hardware pulse.

- To initiate an A/D conversion through software, write 0 to the A/D Start Convert Register.
- To initiate an A/D conversion through hardware, apply an active low pulse to the EXTCONV* pin on the NB-MIO-16X I/O connector. See *Data Acquisition Timing Connections* in Chapter 2, *Configuration and Installation*, for EXTCONV* signal specifications.

Once an A/D conversion is initiated, the ADC automatically stores the result in the A/D FIFO at the end of its conversion cycle.

3. Read the A/D conversion result.

A/D conversion results are obtained by reading the A/D FIFO Register. Before reading the A/D FIFO, however, the Status Register should be read to determine whether the A/D FIFO contains any results.

To read the A/D conversion result, follow these steps:

a. Read the Status Register (16-bit read).

b. If the CONVAVAIL bit is set, then read the A/D FIFO Register to obtain the result.

Reading the A/D FIFO Register removes the A/D conversion result from the A/D FIFO. The binary modes of the A/D FIFO output are explained later in this chapter.

The CONVAVAIL bit indicates whether one or more A/D conversion results are stored in the A/D FIFO. If the CONVAVAIL bit is not set, the A/D FIFO is empty and reading the A/D FIFO Register returns meaningless data. Once an A/D conversion is initiated, the CONVAVAIL bit is set within 100 µsec, indicating that the data conversion result can be read from the FIFO.

An A/D FIFO overflow condition occurs if more than 16 conversions are initiated and stored in the A/D FIFO before the A/D FIFO Register is read. If this condition occurs, the OVERFLOW bit is set in the Status Register to alert you that one or more A/D conversion results have been lost because of FIFO overflow. Writing to the A/D Clear Register clears this error flag and empties the A/D FIFO.

A/D FIFO Output Binary Formats

The A/D conversion result can be returned from the A/D FIFO as a two's complement or straight binary value by setting or clearing the 2SCADC* bit in Command Register 1. If the analog input circuitry is configured for either of the unipolar input ranges (0 to +5 V or 0 to +10 V), straight binary format is recommended (set the 2SCADC* bit). Straight binary format returns numbers between 0 and 65,535 (decimal) when the A/D FIFO Register is read. If the analog input circuitry is configured for either of the bipolar input ranges (-5 to +5 V or -10 to +10 V), two's complement format is recommended (clear the 2SCADC* bit). Two's complement format returns numbers between -32,768 and +32,767 (decimal) when the A/D FIFO Register is read.

Table 4-3 shows input voltage versus A/D conversion value for straight binary format for 0 to +5 V and 0 to +10 V input ranges. Table 4-4 shows input voltage versus A/D conversion value for two's complement format for -5 to +5 V and -10 to +10 V input ranges. The factory default input range is -10 to +10 V.

Table 4-3. Straight Binary Mode A/D Conversion Values

Input Voltage (Gain = 1)	A/D Conversion Result			
	Range: 0 to +5 V		Range: 0 to +10 V	
	Decimal	Hex	Decimal	Hex
0	0	0000	0	0000
2.5	32,768	8000	16,384	4000
4.999924	65,535	FFFF	—	—
5.0	—	—	32,768	8000
7.5	—	—	49,152	C000
9.999847	—	—	65,535	FFFF

In straight binary mode, the data from the ADC FIFO can be converted to the input voltage measured using the following formulas:

$$0 \text{ to } +5\text{V Range} = \frac{\text{A/D Count}}{65{,}536} * \frac{5\text{ V}}{\text{Gain}}$$

$$0 \text{ to } +10\text{V Range} = \frac{\text{A/D Count}}{65{,}536} * \frac{10\text{ V}}{\text{Gain}}$$

Table 4-4. Two's Complement Mode A/D Conversion Values

Input Voltage (Gain = 1)	A/D Conversion Result			
	Range: -5 to +5 V		Range: -10 to +10 V	
	Decimal	Hex	Decimal	Hex
10.0	—	—	-32,768	8000
-5.0	-32,768	8000	-16,384	C000
-2.5	-16,384	C000	-8,192	E000
0	0	0000	0	0000
2.5	16,384	4000	8,192	2000
4.999847	32,767	7FFF	—	—
5.0	—	—	16,384	4000
9.999695	—	—	32,767	FFFF

In two's complement mode, the data from the A/D FIFO can be converted to the input voltage measured using the following formulas:

$$+5\text{V Range} = \frac{\text{A/D Count}}{32{,}768} * \frac{5\text{ V}}{\text{Gain}}$$

$$+10\text{V Range} = \frac{\text{A/D Count}}{32{,}768} * \frac{10\text{ V}}{\text{Gain}}$$

Clearing the Analog Input Circuitry

The analog input circuitry can be cleared by writing 0 to the A/D Clear Register. This operation leaves the analog input circuitry in the following state:

- Analog input error flags OVERFLOW and OVERRUN are cleared.
- Pending interrupt requests are cleared.
- A/D FIFO is emptied.

The A/D FIFO should be emptied before any A/D conversions are started. This action guarantees that the A/D conversion results read from the A/D FIFO are the results from the initiated conversions, not results remaining from previous conversions.

Programming Multiple A/D Conversions on a Single Input Channel

The NB-MIO-16X board can be programmed to execute a multiple A/D conversion sequence with the following options:

- A/D conversions can be initiated either by pulses generated by the onboard sample-interval counter or by pulses applied to the EXTCONV* input. These pulses control the conversion rate.
- The entire conversion sequence can be started by a software write operation to the board or by a signal applied to the STARTTRIG* input.
- You can select either posttrigger or pretrigger operation. In posttrigger operation, the sample counter begins decrementing with each conversion pulse once the conversion sequence is started. When the sample counter reaches 0, the conversion sequence terminates. Thus, all acquired data is received after the trigger or software start. In pretrigger operation, the sample counter does not decrement until a trigger signal is applied to the STOPTRIG input. When the conversion sequence terminates, some of the acquired data is received before the trigger signal and some is received after this signal.

The most commonly used configuration is for the onboard sample-interval and sample counters to control the entire data acquisition operation. Programming this configuration is explained here. The other timing configurations are explained under *External Timing Considerations for Multiple A/D Conversions* later in this chapter. Multiple-channel scanning is discussed under *Programming Multiple A/D Conversions with Channel Scanning* later in this chapter.

The following programming sequences for sample counts less than 65,537 allow the data acquisition circuitry to be retriggered. The sample-interval and sample counters are reloaded at the end of the data acquisition to prepare for another data acquisition operation. The counters do not need reprogramming, and the next data acquisition operation starts when a trigger is received.

Programming multiple A/D conversions on a single channel requires the following programming steps:

1. Select analog input channel and gain.
2. Program the sample-interval counter.

3. Program the sample counter.
4. Clear the A/D circuitry.
5. Enable the data acquisition operation.
6. Apply a trigger.
7. Service the data acquisition operation.

Each of these programming steps is described in detail on the following pages.

1. Select analog input channel and gain.

The analog input channel and gain are selected by writing to the Mux-Gain Register. Bits 7 and 6 control the gain, and bits 3 through 0 select the analog input channel. See the Mux-Gain Register bit description earlier in this chapter for gain and analog input channel bit patterns. Set up the bits as given in the Mux-Gain Register bit description, and write to the Mux-Gain Register.

The Mux-Gain Register needs to be written to only when the analog input channel or gain setting needs to be changed.

2. Program the sample-interval counter.

Counter 3 of the Am9513A Counter/Timer is used as the sample-interval counter. Counter 3 can be programmed to generate a pulse once every *N* counts. *N* is referred to as the sample interval, that is, the time between successive A/D conversions. *N* can be between 2 and 65,536. One count is equal to the period of the timebase clock used by the counter. The following clocks are available internal to the Am9513A: 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz. In addition, the sample-interval timer can use signals connected to any of the Am9513A SOURCE input pins.

To program the sample-interval counter, use the following programming sequence. All writes are 16-bit operations.

a. Write FF03 (hex) to the Am9513A Command Register to select the Counter 3 Mode Register.

b. Write the mode value to the Am9513A Data Register to store the Counter 3 mode value. Use one of the following hex mode values:

   8B25 – Selects 1-MHz clock
   8C25 – Selects 100-kHz clock
   8D25 – Selects 10-kHz clock
   8E25 – Selects 1-kHz clock
   8F25 – Selects 100-Hz clock
   8525 – Selects signal at SOURCE5 input as clock (counts the rising edge of the signal, 6 MHz maximum)

c. Write FF0B (hex) to the Am9513A Command Register to select the Counter 3 Load Register.

d. Write 2 to the Am9513A Data Register to store the Counter 3 load value.

e. Write FF44 (hex) to the Am9513A Command Register to load Counter 3.

f. Write FFF3 (hex) to the Am9513A Command Register to step Counter 3 down to 1.

g. Write the desired sample interval to the Am9513A Data Register to store the Counter 3 load value:

- If the sample interval is between 2 and FFFF (hex) (65,535 decimal), write the sample interval to the Am9513A Data Register.
- If the sample interval is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

h. Write FFF3 (hex) to the Am9513A Command Register twice to step Counter 3 twice.

i. Write FF24 (hex) to the Am9513A Command Register to arm Counter 3.

After you complete this programming sequence, Counter 3 is configured to generate A/D conversion pulses as soon as application of a trigger causes it to be enabled.

3. Program the sample counter.

Counters 4 and 5 of the Am9513A Counter/Timer are used as the sample counter. The sample counter tallies the number of A/D conversions initiated by Counter 3 and stops Counter 3 when the desired sample count is reached. If the desired sample count is 65,536 or less, only Counter 4 needs to be used, making Counter 5 available for general-purpose timing applications. If the desired sample count is greater than 65,536, both Counters 4 and 5 must be used.

Sample Counts 2 through 65,536

Use this procedure to program the sample counter for sample counts up to 65,536. The minimum permitted sample count is 2. All writes are 16-bit operations.

a. Write FF04 (hex) to the Am9513A Command Register to select the Counter 4 Mode Register.

b. Write 1025 (hex) to the Am9513A Data Register to store the Counter 4 mode value.

c. Write FF0C (hex) to the Am9513A Command Register to select the Counter 4 Load Register.

d. Write the sample count value to the Am9513A Data Register to store the Counter 4 load value:

- If the sample count is between 2 and FFFF (hex) (65,535 decimal), write the sample count to the Am9513A Data Register.
- If the sample count is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

e. Write FF48 (hex) to the Am9513A Command Register to load Counter 4.

f. Write FFF4 (hex) to the Am9513A Command Register to decrement Counter 4.

g. Write FF28 (hex) to the Am9513A Command Register to arm Counter 4.

h. Clear the 16*/32 CNT bit in Command Register 1 to notify the hardware that only Counter 4 will be used as the sample counter.

After you complete this programming sequence, Counter 4 is configured to count A/D conversion pulses generated by Counter 3 and turns off the data acquisition operation when Counter 4 decrements to 0.

Sample Counts Greater than 65,536

Use this procedure to program the sample counter for sample counts greater than 65,536. The lower 16 bits of the sample count are stored in Counter 4, and the upper 16 bits of the sample count are stored in Counter 5. All writes are 16-bit operations.

a. Write FF04 (hex) to the Am9513A Command Register to select the Counter 4 Mode Register.

b. Write 1025 (hex) to the Am9513A Data Register to store the Counter 4 mode value.

c. Write FF0C (hex) to the Am9513A Command Register to select the Counter 4 Load Register.

d. Write the least significant 16 bits of the sample count value minus 1 to the Am9513A Data Register to store the Counter 4 load value.

   - If the least significant 16 bits are all 0, write FFFF (hex).

e. Write FF48 (hex) to the Am9513A Command Register to load Counter 4.

f. Write 0 to the Am9513A Data Register to store 0 into the Load Register for Counter 4 reloading.

g. Write FF28 (hex) to the Am9513A Command Register to arm Counter 4.

h. Write FF05 (hex) to the Am9513A Command Register to select the Counter 5 Mode Register.

i. Write 25 (hex) to the Am9513A Data Register to store the Counter 5 mode value.

j. Write FF0D (hex) to the Am9513A Command Register to select the Counter 5 Load Register.

k. Take the most significant 16 bits of the sample count and do the following:

   - If the least significant 16 bits of the sample count are all 0 or all 0 except for a 1 in the least significant bit, write the most significant 16 bits to the Am9513A Data Register to store the Counter 5 load value.

   - Otherwise, add 1 to the most significant 16 bits of the sample count and write that value to the Am9513A Data Register to store the Counter 5 load value.

l. Write FF70 (hex) to the Am9513A Command Register to load and arm Counter 5.

m. Set the 16*/32 CNT bit in Command Register 1 to notify the hardware that both Counters 4 and 5 will be used as the sample counter.

After you complete this programming sequence, Counter 4 is configured to count A/D conversion pulses generated by Counter 3, and Counter 5 decrements every time Counter 4 reaches 0. The data acquisition operation is terminated when both Counters 4 and 5 reach 0.

4. Clear the A/D circuitry.

Before you start the data acquisition operation, the A/D FIFO must be emptied to clear out any old A/D conversion results. This emptying must be done after the counters are programmed in case any spurious edges were caused while programming the counters. Write 0 to the A/D Clear Register to empty the FIFO.

5. Enable the data acquisition operation.

To enable the data acquisition operation so that A/D conversions begin when a trigger is received, set the DAQEN bit in Command Register 1.

6. Apply a trigger.

Once set up by the preceding steps, the data acquisition operation is initiated when a trigger is received. A trigger can be provided in one of two ways: through software or through hardware.

To initiate the data acquisition operation through software, write 0 to the Start DAQ Register (16-bit write).

To initiate the data acquisition operation through hardware, apply an active low pulse to the STARTTRIG* pin on the NB-MIO-16X I/O connector. See *Data Acquisition Timing Connections* in Chapter 2, *Configuration and Installation*, for STARTTRIG* signal specifications.

Once the trigger is applied, Counter 3 generates pulses initiating A/D conversions once every sample interval until the sample counter reaches 0.

7. Service the data acquisition operation.

Once the data acquisition operation is started by application of a trigger, the operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To do this, perform the following sequence until the desired number of conversion results have been read:

a. Read the Status Register (16-bit read).

b. If the CONVAVAIL bit is set, read the A/D FIFO Register to obtain the result.

Interrupts or DMA can also be used to service the data acquisition operation. These topics are discussed later in this chapter.

Two error conditions may occur during a data acquisition operation–an overflow error, or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the CONVAVAIL bit. If either of these error conditions occurs, the data acquisition operation stops.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is set.

An overrun condition occurs if an A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is set. See Table 4-5 for NB-MIO-16X maximum recommended single-channel data acquisition rates.

Table 4-5. Single-Channel Data Acquisition Rates

Board	Acquisition Rate
NB-MIO-16X(H/L)-42	23.8 ksamples/sec
NB-MIO-16X(H/L)-18	55.6 ksamples/sec

Both the OVERFLOW and OVERRUN bits in the Status Register are cleared by writing to the A/D Clear Register.

External Timing Considerations for Multiple A/D Conversions

There are two ways you can use external timing for multiple A/D conversions–using the STOPTRIG input to control the sample counter, and applying pulses to the EXTCONV* input. In addition, STARTTRIG provides external synchronization of the start of a multiple A/D conversion sequence.

Pretriggering with the STOPTRIG Signal

In this case, the sample-interval counter starts counting when a rising edge signal is applied to the STOPTRIG input on the NB-MIO-16X I/O connector. The sample counter should be programmed for active high level gating on Gate 4. The data acquisition operation is initiated by writing to the Start DAQ Register or by a pulse on the STARTTRIG* input. The sample count register does not begin counting samples until a rising edge is applied to STOPTRIG.

To perform this operation, complete these steps:

1. Select analog input channel and gain.
2. Program the sample-interval counter.
3. Program the sample counter.
4. Clear the A/D circuitry.
5. Apply a trigger.
6. Service the data acquisition operation.

1. Select analog input channel and gain.

The analog input channel and gain are selected by writing to the Mux-Gain Register. Bits 7 and 6 control the gain, and bits 3 through 0 select the analog input channel. See the Mux-Gain Register bit description earlier in this chapter for gain and analog input channel bit patterns. Set up the bits as given in the Mux-Gain Register bit description, and write to the Mux-Gain Register.

Once set up with an initial value, the Mux-Gain Register needs to be written to only when the analog input channel or gain setting needs to be changed.

2. Program the sample-interval counter.

Counter 3 of the Am9513A Counter/Timer is used as the sample-interval counter. Counter 3 can be programmed to generate a pulse once every *N* counts. *N* is referred to as the sample interval, that is, the time between successive A/D conversions. *N* can be between 2 and 65,536. One count is equal to the period of the timebase clock used by the counter. The following clocks are available internal to the Am9513A: 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz. In addition, the sample-interval timer can use signals connected to any of the Am9513A SOURCE input pins.

To program the sample-interval counter, use the following programming sequence. All writes are 16-bit operations.

a. Write FF03 (hex) to the Am9513A Command Register to select the Counter 3 Mode Register.

b. Write the mode value to the Am9513A Data Register to store the Counter 3 mode value. Use one of the following hex mode values:

   8B25 – Selects 1-MHz clock
   8C25 – Selects 100-kHz clock
   8D25 – Selects 10-kHz clock
   8E25 – Selects 1-kHz clock
   8F25 – Selects 100-Hz clock
   8525 – Selects signal at SOURCE5 input as clock (counts the rising edge of the signal, 6 MHz maximum)

c. Write FF0B (hex) to the Am9513A Command Register to select the Counter 3 Load Register.

d. Write 2 to the Am9513A Data Register to store the Counter 3 load value.

e. Write FF44 (hex) to the Am9513A Command Register to load Counter 3.

f. Write FFF3 (hex) to the Am9513A Command Register to step Counter 3 down to 1.

g. Write the desired sample interval to the Am9513A Data Register to store the Counter 3 load value:

   - If the sample interval is between 2 and FFFF (hex) (65,535 decimal) inclusive, write the sample interval to the Am9513A Data Register.
   - If the sample interval is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

h. Write FF24 (hex) to the Am9513A Command Register to arm Counter 3.

After you complete this programming sequence, Counter 3 is configured to generate A/D conversion pulses as soon as application of a trigger causes it to be enabled.

3. Program the sample counter.

Counters 4 and 5 of the Am9513A Counter/Timer are used as the sample counter. The sample counter tallies the number of A/D conversions initiated by Counter 3 and stops Counter 3 when the desired sample count is reached. If the desired sample count is 65,536 or less, only Counter 4 needs to be used, making Counter 5 available for general-purpose timing applications. If the desired sample count is greater than 65,536, both Counters 4 and 5 must be used.

Sample Counts 2 through 65,536 Use this procedure to program the sample counter for sample counts up to 65,536. The minimum permitted sample count is 2. All writes are 16-bit operations.

a. Write FF04 (hex) to the Am9513A Command Register to select the Counter 4 Mode Register.

b. Write 9025 (hex) to the Am9513A Data Register to store the Counter 4 mode value.

c. Write FF0C (hex) to the Am9513A Command Register to select the Counter 4 Load Register.

d. Write the sample count value to the Am9513A Data Register to store the Counter 4 load value:

   - If the sample count is between 2 and FFFF (hex) (65,535 decimal), write the sample count to the Am9513A Data Register.
   - If the sample count is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

e. Write FF48 (hex) to the Am9513A Command Register to load Counter 4.

f. Write FFF4 (hex) to the Am9513A Command Register to decrement Counter 4.

g. Write FF28 (hex) to the Am9513A Command Register to arm Counter 4.

h. Clear the 16*/32 CNT bit in Command Register 1 to notify the hardware that only Counter 4 will be used as the sample counter.

After you complete this programming sequence, Counter 4 is configured to count A/D conversion pulses generated by Counter 3 and to turn off the data acquisition operation when Counter 4 decrements to 0. Counter 4 begins counting A/D conversion pulses when a rising edge signal is received on the STOPTRIG input. A/D conversion data stored before receipt of the STOPTRIG signal are pretrigger samples.

Sample Counts Greater than 65,536 Use this procedure to program the sample counter for sample counts greater than 65,536. The lower 16 bits of the sample count are stored in Counter 4, and the upper 16 bits of the sample count are stored in Counter 5. All writes are 16-bit operations.

a. Write FF04 (hex) to the Am9513A Command Register to select the Counter 4 Mode Register.

b. Write 9025 (hex) to the Am9513A Data Register to store the Counter 4 mode value.

c. Write FF0C (hex) to the Am9513A Command Register to select the Counter 4 Load Register.

d. Write the least significant 16 bits of the sample count value minus 1 to the Am9513A Data Register to store the Counter 4 load value.

   - If the least significant 16 bits are all 0, write FFFF(hex) .

e. Write FF48 (hex) to the Am9513A Command Register to load Counter 4.

f. Write 0 (hex) to the Am9513A Data Register to store 0 into the Load Register for Counter 4 reloading.

g. Write FF28 (hex) to the Am9513A Command Register to arm Counter 4.

h. Write FF05 (hex) to the Am9513A Command Register to select the Counter 5 Mode Register.

i. Write 25 (hex) to the Am9513A Data Register to store the Counter 5 mode value.

j. Write FF0D (hex) to the Am9513A Command Register to select the Counter 5 Load Register.

k. Take the most significant 16 bits of the sample count and do the following:

   - If the least significant 16 bits of the sample count are all 0 or all 0 except for a 1 in the least significant bit, write the most significant 16 bits to the Am9513A Data Register to store the Counter 5 load value.

   - Otherwise, add 1 to the most significant 16 bits of the sample count and write that value to the Am9513A Data Register to store the Counter 5 load value.

l. Write FF70 (hex) to the Am9513A Command Register to load and arm Counter 5.

m. Set the 16*/32 CNT bit in Command Register 1 to notify the hardware that both Counters 4 and 5 will be used as the sample counter.

After you complete this programming sequence, Counter 4 is configured to count A/D conversion pulses generated by Counter 3, and Counter 5 decrements every time Counter 4 reaches 0. The data acquisition operation is terminated when both Counters 4 and 5 reach 0. Counters 4 and 5 begin counting A/D conversion pulses when a rising edge signal is received on the STOPTRIG input. A/D conversion data stored before receipt of the STOPTRIG signal are pretrigger samples.

4. Clear the A/D circuitry.

Before you start the data acquisition operation, the A/D FIFO must be emptied to clear out any old A/D conversion results. This emptying must be done after the counters are programmed in case any spurious edges were caused while programming the counters. Write 0 to the A/D Clear Register to empty the FIFO (16-bit write).

5. Apply a trigger.

Once set up by the preceding steps, the data acquisition operation is initiated when a trigger is received. A trigger can be provided in one of two ways–through software, or through hardware.

- To initiate the data acquisition operation through software, write 0 to the Start DAQ Register (16-bit write).
- To initiate the data acquisition operation through hardware, apply an active low pulse to the STARTTRIG* pin on the NB-MIO-16X I/O connector. See *Data Acquisition Timing Connections* in Chapter 2, *Configuration and Installation*, for STARTTRIG* signal specifications.

Once the trigger is applied, Counter 3 generates pulses initiating A/D conversions once every sample interval until the sample counter reaches 0.

6. Service the data acquisition operation.

Once the data acquisition operation is started by application of a trigger, the operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To do this, perform the following sequence until the desired number of conversion results have been read:

a. Read the Status Register (16-bit read).

b. If the CONVAVAIL bit is set, read the A/D FIFO Register to obtain the result.

Interrupts or DMA can also be used to service the data acquisition operation. These topics are discussed later in this chapter.

Two error conditions may occur during a data acquisition operation–an overflow error, or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the CONVAVAIL bit. If either of these error conditions occurs, the data acquisition operation stops.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is set.

An overrun condition occurs if an A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is set. See Table 4-5 for NB-MIO-16X maximum data acquisition rates.

Both the OVERFLOW and OVERRUN bits in the Status Register are cleared by writing to the A/D Clear Register.

When steps 1 through 5 of this sequence are completed, Counter 3 is armed and begins generating pulses. The sample counter does not begin counting until a rising edge signal is detected on the STOPTRIG input. When the sample count decrements to 0, the data acquisition operation halts. Chapter 2, *Configuration and Installation*, contains the STOPTRIG signal specifications.

Controlling Multiple A/D Conversions with the EXTCONV* Signal

When you use EXTCONV* to control multiple A/D conversions, none of the onboard counters need to be used, but the sample counters can still be used to stop the data acquisition operation when the terminal count is reached. Pulses applied to the EXTCONV* input initiate the A/D conversions. To perform this operation, complete these steps:

1. Select analog input channel and gain.
2. (Optional) Program the sample counter (see *Programming Multiple A/D Conversions on a Single Input Channel* earlier in this chapter).
3. Clear the A/D circuitry.
4. Service the data acquisition operation.

First, make certain that Counter 3 is reset as described under *Resetting the Hardware after a Data Acquisition Operation* later in this chapter. If Counter 3 is not reset, it may be driving the EXTCONV* line and therefore prevent another signal from successfully driving the line high or low.

1. Select analog input channel and gain.

The analog input channel and gain are selected by writing to the Mux-Gain Register. Bits 7 and 6 control the gain, and bits 3 through 0 select the analog input channel. See the Mux-Gain Register bit description earlier in this chapter for gain and analog input channel bit patterns. Set up the bits as given in the Mux-Gain Register bit description, and write to the Mux-Gain Register.

The Mux-Gain Register needs to be written to only when the analog input channel or gain setting needs to be changed.

2. Clear the A/D circuitry.

Before starting the data acquisition operation, the A/D FIFO must be emptied to clear out any old A/D conversion results. Write 0 to the A/D Clear Register to empty the FIFO.

3. Service the data acquisition operation.

Once an external trigger starts the data acquisition operation, the operation is serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To do this, perform the following sequence until the desired number of conversion results have been read:

a. Read the Status Register (16-bit read).

b. If the CONVAVAIL bit is set, read the A/D FIFO Register to obtain the result.

Interrupts or DMA can also be used to service the data acquisition operation. These topics are discussed later in this chapter.

Two error conditions may occur during a data acquisition operation: an overflow error or an overrun error. These error conditions are reported through the Status Register and should be

checked every time the Status Register is read to check the CONVAVAIL bit. If either of these error conditions occurs, the data acquisition operation stops.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is set.

An overrun condition occurs if an A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is set. See Table 4-5 for NB-MIO-16X maximum data acquisition rates.

Both the OVERFLOW and OVERRUN bits in the Status Register are cleared by writing to the A/D Clear Register.

An A/D conversion is initiated and stored in the A/D FIFO every time a low-to-high edge is detected on the EXTCONV* input. See Chapter 2, *Configuration and Installation*, for EXTCONV* signal specifications.

Programming Multiple A/D Conversions with Channel Scanning

The data acquisition programming sequences described earlier program the NB-MIO-16X for multiple A/D conversion on a single input channel. The NB-MIO-16X can also be programmed for scanning analog input channels and switching gain settings during the data acquisition operation. The sequence of A/D channels and gain settings, called the *scan sequence*, is programmed into the mux-gain memory.

There are two types of multiple A/D conversions with channel scanning–continuous channel scanning, and interval channel scanning. *Continuous channel scanning* cycles through the scan sequence in the mux-gain memory and repeats the scan sequence until the sample counter terminates the data acquisition. There is no delay between the cycles of the scan sequence. Continuous channel scanning can be thought of as a *round-robin* approach to scanning multiple channels.

Interval channel scanning gives each scan sequence a programmed time interval, called a *scan interval*. Each cycle of the scan sequence begins at the time interval specified by the scan interval. If the sample-interval counter is programmed for the minimum time required to complete an A/D conversion, interval channel scanning can be thought of as a *pseudo-simultaneous* scanning of multiple channels; that is, all channels in the scan sequence are read as quickly as possible at the beginning of each scan interval.

Multiple A/D Conversions with Continuous Channel Scanning (Round-Robin)

To program continuous scanning of multiple A/D conversions, follow these steps:

1. Set up the analog channel and gain selection sequence.
2. Program the sample-interval counter.
3. Program the sample counter.
4. Clear the A/D circuitry and reset the mux counter.
5. Enable the scanning data acquisition operation.
6. Apply a trigger.
7. Service the data acquisition operation.

Setting the SCANEN bit in Command Register 1 enables scanning during multiple A/D conversions. This bit must be set regardless of the type of scanning used; otherwise, only a single channel is scanned. In addition, a channel and gain scan sequence must be stored in the mux-gain memory.

1. Set up the analog channel and gain selection sequence.

During a scanning data acquisition operation, a selected number of locations in the mux-gain memory are clocked through. A new mux-gain memory location is selected after each A/D conversion. The first conversion is performed on the first channel and gain setting in the memory. The second conversion is performed on the second channel and gain setting, and so on. The last entry written to the mux-gain memory must have the LASTONE bit set (see the Mux-Gain Register description earlier in this chapter). This bit marks the end of the scan sequence. After the last conversion is performed, the scan sequence starts over. If there are *X* entries in the mux-gain memory, every *X*th conversion in the data collected is performed on the same channel and gain setting.

Multiple conversions can be performed on each entry in the mux-gain memory before incrementing to the next entry in the scan sequence. If the SCANDIV bit in Command Register 1 is set, the mux-gain memory increments to the next entry when an active low pulse is detected on the Am9513A Counter/Timer OUT1 signal. If the SCANDIV bit is cleared, the mux-gain memory is incremented to the next entry after every conversion.

The mux-gain memory must be loaded with the desired scan sequence before data acquisition begins. To load the mux-gain memory, perform the following write operations where *X* is the number of entries in the scan sequence:

For $i = 0$ to $X-1$, follow these steps:

a. Write *i* to the Mux-Counter Register to select the mux-gain memory location.

b. Write the desired analog channel selection and gain setting to the Mux-Gain Register to load the mux-gain memory at location *i*.

c. If $i = X-1$, also set the LASTONE bit when writing to the Mux-Gain Register.

2. Program the sample-interval counter.

Counter 3 of the Am9513A Counter/Timer is used as the sample-interval counter. Counter 3 can be programmed to generate a pulse once every *N* counts. *N* is referred to as the sample interval, that is, the time between successive A/D conversions. *N* can be between 2 and 65,536. One count is equal to the period of the timebase clock used by the counter. The following clocks are available internal to the Am9513A: 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz. In addition, the sample-interval timer can use signals connected to any of the Am9513A SOURCE input pins.

To program the sample-interval counter, use the following programming sequence. All writes are 16-bit operations.

a. Write FF03 (hex) to the Am9513A Command Register to select the Counter 3 Mode Register.

b. Write the mode value to the Am9513A Data Register to store the Counter 3 mode value. Use one of the following hex mode values:

   8B25 – Selects 1-MHz clock
   8C25 – Selects 100-kHz clock
   8D25 – Selects 10-kHz clock
   8E25 – Selects 1-kHz clock
   8F25 – Selects 100-Hz clock
   8525 – Selects signal at SOURCE5 input as clock (counts the rising edge of the signal, 6 MHz maximum)

c. Write FF0B (hex) to the Am9513A Command Register to select the Counter 3 Load Register.

d. Write 2 to the Am9513A Data Register to store the Counter 3 load value.

e. Write FF44 (hex) to the Am9513A Command Register to load Counter 3.

f. Write FFF3 (hex) to the Am9513A Command Register to step Counter 3 down to 1.

g. Write the desired sample interval to the Am9513A Data Register to store the Counter 3 load value:

   - If the sample interval is between 2 and FFFF (hex) (65,535 decimal), write the sample interval to the Am9513A Data Register.
   - If the sample interval is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

h. Write FF24 (hex) to the Am9513A Command Register to arm Counter 3.

After you complete this programming sequence, Counter 3 is configured to generate A/D conversion pulses as soon as application of a trigger causes it to be enabled.

3. Program the sample counter.

Counters 4 and 5 of the Am9513A Counter/Timer are used as the sample counter. The sample counter tallies the number of A/D conversions initiated by Counter 3 and stops Counter 3 when the desired sample count is reached. The sample count should be programmed as a multiple of the number of entries in the mux-gain memory. If the desired sample count is 65,536 or less, only Counter 4 needs to be used, making Counter 5 available for general-purpose timing applications. If the desired sample count is greater than 65,536, both Counters 4 and 5 must be used.

Sample Counts 2 through 65,536 Use this procedure to program the sample counter for sample counts up to 65,536. The minimum permitted sample count is 2. All writes are 16-bit operations.

a. Write FF04 (hex) to the Am9513A Command Register to select the Counter 4 Mode Register.

b. Write 1025 (hex) to the Am9513A Data Register to store the Counter 4 mode value.

c. Write FF0C (hex) to the Am9513A Command Register to select the Counter 4 Load Register.

d. Write the sample count value to the Am9513A Data Register to store the Counter 4 load value:

   - If the sample count is between 2 and FFFF (hex) (65,535 decimal), write the sample count minus 1 to the Am9513A Data Register.
   - If the sample count is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

e. Write FF48 (hex) to the Am9513A Command Register to load Counter 4.

f. Write FFF4 (hex) to the Am9513A Command Register to decrement Counter 4.

g. Write FF28 (hex) to the Am9513A Command Register to arm Counter 4.

h. Clear the 16*/32 CNT bit in Command Register 1 to notify the hardware that only Counter 4 will be used as the sample counter.

After you complete this programming sequence, Counter 4 is configured to count A/D conversion pulses generated by Counter 3 and to turn off the data acquisition operation when Counter 4 reaches 0.

Sample Counts Greater than 65,536 Use this procedure to program the sample counter for sample counts greater than 65,536. The lower 16 bits of the sample count are stored in Counter 4, and the upper 16 bits of the sample count are stored in Counter 5. All writes are 16-bit operations.

a. Write FF04 (hex) to the Am9513A Command Register to select the Counter 4 Mode Register.

b. Write 1025 (hex) to the Am9513A Data Register to store the Counter 4 mode value.

c. Write FF0C (hex) to the Am9513A Command Register to select the Counter 4 Load Register.

d. Write the least significant 16 bits of the sample count value minus 1 to the Am9513A Data Register to store the Counter 4 load value.

   - If the least significant 16 bits are all 0, write FFFF (hex).

e. Write FF48 (hex) to the Am9513A Command Register to load and arm Counter 4.

f. Write 0 to the Am9513A Data Register to store 0 into the Load Register for Counter 4 reloading.

g. Write FF28 (hex) to the Am9513A Command Register to arm Counter 4.

h. Write FF05 (hex) to the Am9513A Command Register to select the Counter 5 Mode Register.

i. Write 25 (hex) to the Am9513A Data Register to store the Counter 5 mode value.

j. Write FF0D (hex) to the Am9513A Command Register to select the Counter 5 Load Register.

k. Take the most significant 16 bits of the sample count and do the following:

- If the least significant 16 bits of the sample count are all 0 or all 0 except for a 1 in the least significant bit, write the most significant 16 bits to the Am9513A Data Register to store the Counter 5 load value.
- Otherwise, add 1 to the most significant 16 bits of the sample count and write that value to the Am9513A Data Register to store the Counter 5 load value.

l. Write FF70 (hex) to the Am9513A Command Register to load and arm Counter 5.

m. Set the 16*/32 CNT bit in Command Register 1 to notify the hardware that both Counters 4 and 5 will be used as the sample counter.

After you complete this programming sequence, Counter 4 is configured to count A/D conversion pulses generated by Counter 3, and Counter 5 increments every time Counter 4 reaches 0. The data acquisition operation is terminated when both Counters 4 and 5 reach 0 and the last entry in the mux-gain memory is served.

4. Clear the A/D circuitry and reset the mux counter.

Before starting the data acquisition operation, the A/D FIFO must be emptied to clear out any old A/D conversion results. This emptying must be done after the counters are programmed in case any spurious edges were caused while programming the counters. Write 0 to the A/D Clear Register to empty the FIFO.

Write 0 to the Mux-Counter Register to set the analog input circuitry to the first channel and gain setting of the scan sequence.

5. Enable the scanning data acquisition operation.

To enable the scanning data acquisition operation so that A/D conversions begin when a trigger is received, set the DAQEN bit and the SCANEN bit in Command Register 1.

6. Apply a trigger.

Once set up by the preceding steps, the data acquisition operation is initiated when a trigger is received. A trigger can be provided in one of two ways–through software, or through hardware.

- To initiate the data acquisition operation through software, write 0 to the Start DAQ Register.
- To initiate the data acquisition operation through hardware, apply an active low pulse to the STARTTRIG* pin on the NB-MIO-16X I/O connector. See *Data Acquisition Timing Connections* in Chapter 2, *Configuration and Installation*, for STARTTRIG* signal specifications.

Once the trigger is applied, Counter 3 generates pulses initiating A/D conversions once every sample interval until the sample counter reaches 0.

7. Service the data acquisition operation.

Once the data acquisition operation is started by application of a trigger, the operation is serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To do this, perform the following sequence until the desired number of conversion results have been read:

a. Read the Status Register (16-bit read).

b. If the CONVAVAIL bit is set, read the A/D FIFO Register to obtain the result.

Interrupts or DMA can also be used to service the data acquisition operation. These topics are discussed later in this chapter.

Two error conditions may occur during a data acquisition operation–an overflow error, or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the CONVAVAIL bit. If either of these error conditions occurs, the data acquisition operation stops.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is set.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is set.

Scanned data acquisition requires slower data acquisition rates than single-channel data acquisition because signals must settle each time channels are switched. See Table 4-6 for the maximum recommended multiple-channel data acquisition rates.

Both the OVERFLOW and OVERRUN bits in the Status Register are cleared by writing to the A/D Clear Register.

Multiple A/D Conversions with Interval Channel Scanning (Pseudo-Simultaneous)

To program scanned multiple A/D conversions with a scan interval, follow these steps:

1. Set up the analog channel and gain selection sequence.
2. Program the sample-interval counter.
3. Program the sample counter.
4. Program the scan-interval counter.
5. Clear the A/D circuitry and reset the mux counter.
6. Enable the scanning data acquisition operation.
7. Apply a trigger.
8. Service the data acquisition operation.

Setting the SCANEN bit in Command Register 1 enables scanning during multiple A/D conversions. This bit must be set regardless of the type of scanning used; otherwise, only a single channel is scanned. In addition, a channel and gain scan sequence must be stored in the mux-gain memory.

Setting the SCN2 bit in Command Register 1 enables the use of a scan interval during multiple A/D conversions. The scan-interval counter gives each cycle through the scan sequence a time interval. The scan-interval counter begins counting at the start of the scan sequence programmed into the mux-gain memory. When the scan sequence completes, the next cycle through the scan sequence does not begin until the scan-interval counter has reached its terminal count. Be sure that the scan-interval counter allows enough time for all conversions in a scan sequence to occur so that conversions are not missed.

1. Set up the analog channel and gain selection sequence.

During a scanning data acquisition operation, a selected number of locations in the mux-gain memory are clocked through. A new mux-gain memory location is selected after each A/D conversion. The first conversion is performed on the first channel and gain setting in the memory. The second conversion is performed on the second channel and gain setting, and so on. The last entry written to the mux-gain memory must have the LASTONE bit set. This bit marks the end of the scan sequence. After the last conversion is performed, the scan sequence starts over. If there are *X* entries in the mux-gain memory, every *X*th conversion in the data collected is performed on the same channel and gain setting.

Multiple conversions can be performed on each entry in the mux-gain memory before incrementing to the next entry in the scan sequence. If the SCANDIV bit in Command Register 1 is set, the mux-gain memory increments to the next entry when an active low pulse is detected on the Am9513A Counter/Timer OUT1 signal. If the SCANDIV bit is cleared, the mux-gain memory is incremented to the next entry after every conversion.

The mux-gain memory must be loaded with the desired scan sequence before data acquisition begins. To load the mux-gain memory, perform the following write operations where *X* is the number of entries in the scan sequence.

For $i = 0$ to X-1, follow these steps:

a. Write i to the Mux-Counter Register to select the mux-gain memory location.

b. Write the desired analog channel selection and gain setting to the Mux-Gain Register to load the mux-gain memory at location i.

c. If $i = X$-1, also set the LASTONE bit when writing to the Mux-Gain Register.

2. Program the sample-interval counter.

Counter 3 of the Am9513A Counter/Timer is used as the sample-interval counter. Counter 3 can be programmed to generate a pulse once every N counts. N is referred to as the sample interval, that is, the time between successive A/D conversions. N can be between 2 and 65,536. One count is equal to the period of the timebase clock used by the counter. The following clocks are available internal to the Am9513A: 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz. In addition, the sample-interval timer can use signals connected to any of the Am9513A SOURCE input pins.

To program the sample-interval counter, use the following programming sequence. All writes are 16-bit operations.

a. Write FF03 (hex) to the Am9513A Command Register to select the Counter 3 Mode Register.

b. Write the mode value to the Am9513A Data Register to store the Counter 3 mode value. Use one of the following hex mode values:

8B25 – Selects 1-MHz clock
8C25 – Selects 100-kHz clock
8D25 – Selects 10-kHz clock
8E25 – Selects 1-kHz clock
8F25 – Selects 100-Hz clock
8525 – Selects signal at SOURCE5 input as clock (counts the rising edge of the signal, 6 MHz maximum)

c. Write FF0B (hex) to the Am9513A Command Register to select the Counter 3 Load Register.

d. Write 2 to the Am9513A Data Register to store the Counter 3 load value.

e. Write FF44 (hex) to the Am9513A Command Register to load Counter 3.

f. Write FFF3 (hex) to the Am9513A Command Register to step Counter 3 down to 1.

g. Write the desired sample interval to the Am9513A Data Register to store the Counter 3 load value:

- If the sample interval is between 2 and FFFF (hex) (65,535 decimal), write the sample interval to the Am9513A Data Register.
- If the sample interval is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

h. Write FF24 (hex) to the Am9513A Command Register to arm Counter 3.

After you complete this programming sequence, Counter 3 is configured to generate A/D conversion pulses as soon as application of a trigger causes it to be enabled.

3. Program the sample counter.

Counters 4 and 5 of the Am9513A Counter/Timer are used as the sample counter. The sample counter tallies the number of A/D conversions initiated by Counter 3 and stops Counter 3 when the desired sample count is reached. The sample count should be programmed as a multiple of the number of entries in the mux-gain memory. If the desired sample count is 65,536 or less, only Counter 4 needs to be used, making Counter 5 available for general-purpose timing applications. If the desired sample count is greater than 65,536, both Counters 4 and 5 must be used.

Sample Counts 2 through 65,536 Use this procedure to program the sample counter for sample counts up to 65,536. The minimum permitted sample count is 2. All writes are 16-bit operations.

a. Write FF04 (hex) to the Am9513A Command Register to select the Counter 4 Mode Register.

b. Write 1025 (hex) to the Am9513A Data Register to store the Counter 4 mode value.

c. Write FF0C (hex) to the Am9513A Command Register to select the Counter 4 Load Register.

d. Write the sample count value to the Am9513A Data Register to store the Counter 4 load value:

   - If the sample count is between 2 and FFFF (hex) (65,535 decimal), write the sample count minus 1 to the Am9513A Data Register.

   - If the sample count is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

e. Write FF48 (hex) to the Am9513A Command Register to load Counter 4.

f. Write FFF4 (hex) to the Am9513A Command Register to decrement Counter 4.

g. Write FF28 (hex) to the Am9513A Command Register to arm Counter 4.

h. Clear the 16*/32 CNT bit in Command Register 1 to notify the hardware that only Counter 4 will be used as the sample counter.

When this procedure is completed, Counter 4 is configured to count A/D conversion pulses generated by Counter 3 and to turn off the data acquisition operation when Counter 4 reaches 0.

Sample Counts Greater than 65,536 Use this procedure to program the sample counter for sample counts greater than 65,536. The lower 16 bits of the sample count are stored in Counter 4, and the upper 16 bits of the sample count are stored in Counter 5. All writes are 16-bit operations.

a. Write FF04 (hex) to the Am9513A Command Register to select the Counter 4 Mode Register.

b. Write 1025 (hex) to the Am9513A Data Register to store the Counter 4 mode value.

c. Write FF0C (hex) to the Am9513A Command Register to select the Counter 4 Load Register.

d. Write the least significant 16 bits of the sample count value minus 1 to the Am9513A Data Register to store the Counter 4 load value.

   - If the least significant 16 bits are all 0, write FFFF(hex) .

e. Write FF48 (hex) to the Am9513A Command Register to load Counter 4.

f. Write 0 to the Am9513A Data Register to store 0 into the Load Register for Counter 4 reloading.

g. Write FF28 (hex) to the Am9513A Command Register to arm Counter 4.

h. Write FF05 (hex) to the Am9513A Command Register to select the Counter 5 Mode Register.

i. Write 25 (hex) to the Am9513A Data Register to store the Counter 5 mode value.

j. Write FF0D (hex) to the Am9513A Command Register to select the Counter 5 Load Register.

k. Take the most significant 16 bits of the sample count and do the following:

   - If the least significant 16 bits of the sample count are all 0 or all 0 except for a 1 in the least significant bit, write the most significant 16 bits to the Am9513A Data Register to store the Counter 5 load value.

   - Otherwise, add 1 to the most significant 16 bits of the sample count and write that value to the Am9513A Data Register to store the Counter 5 load value.

l. Write FF70 (hex) to the Am9513A Command Register to load and arm Counter 5.

m. Set the 16*/32 CNT bit in Command Register 1 to notify the hardware that both Counters 4 and 5 will be used as the sample counter.

After you complete this programming sequence, Counter 4 is configured to count A/D conversion pulses generated by Counter 3, and Counter 5 increments every time Counter 4 reaches 0. The data acquisition operation is terminated when both Counters 4 and 5 reach 0 and the last entry in the mux-gain memory is served.

4. Program the scan-interval counter.

Counter 2 of the Am9513A Counter/Timer is used as the scan-interval counter. Counter 2 can be programmed to generate a pulse once every *N* counts. *N* is referred to as the scan interval, that is, the time between successive scan sequences programmed into the mux-gain memory. *N* can be between 2 and 65,536. One count is equal to the period of the timebase clock used by the counter. The following clocks are available internal to the Am9513A: 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz. In addition, the scan-interval timer can use signals connected to any of the Am9513A SOURCE input pins.

To program the scan-interval counter, use the following programming sequence. All writes are 16-bit operations.

a. Write FF02 (hex) to the Am9513A Command Register to select the Counter 2 Mode Register.

b. Write the mode value to the Am9513A Data Register to store the Counter 2 mode value. Use one of the following hex mode values:

   8B25 – Selects 1-MHz clock
   8C25 – Selects 100-kHz clock
   8D25 – Selects 10-kHz clock
   8E25 – Selects 1-kHz clock
   8F25 – Selects 100-Hz clock
   8525 – Selects signal at SOURCE5 input as clock (counts the rising edge of the signal, 6 MHz maximum)

c. Write FF0A (hex) to the Am9513A Command Register to select the Counter 2 Load Register.

d. Write 3 to the Am9513A Data Register to store the Counter 2 load value.

e. Write FF42 (hex) to the Am9513A Command Register to load Counter 2.

f. Write FFF2 (hex) o the Am9513A Command Register to step Counter 2 down to 1.

g. Entries stored in the mux-gain memory should be scanned once during a scan interval. The following condition must be satisfied:

   scan interval $\geq$ 2 µsec + sample interval * x

   where x is the number of entries in the scan sequence.

   Write the desired scan interval to the Am9513A Data Register to store the Counter 2 load value:

   - If the scan interval is between 2 and FFFF (hex) (65,535 decimal), write the scan interval to the Am9513A Data Register.
   - If the scan interval is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

h. Write FF22 (hex) to the Am9513A Command Register to arm Counter 2.

After you complete this programming sequence, Counter 2 is configured to assign a time interval to scan sequences once the trigger to enable A/D conversions is detected.

5. Clear the A/D circuitry and reset the mux counter.

Before starting the data acquisition operation, the A/D FIFO must be emptied to clear out any old A/D conversion results. This emptying must be done after the counters are programmed in case any spurious edges were caused while programming the counters. Write 0 to the A/D Clear Register to empty the FIFO (16-bit write).

Write 0 to the Mux-Counter Register to set the analog input circuitry to the first channel and gain setting of the scan sequence.

Write 0 to the TMRINTCL Register to clear any spurious edge caused by programming Counter 2.

6. Enable the scanning data acquisition operation.

To enable the scanning data acquisition operation such that A/D conversions begin when a trigger is received, set the DAQEN bit and the SCANEN bit in Command Register 1. To enable the scan interval timing, set the SCN2 bit in Command Register 2.

7. Apply a trigger.

Once set up by the preceding steps, the data acquisition operation is initiated when a trigger is received. A trigger can be provided in one of two ways–through software, or through hardware.

- To initiate the data acquisition operation through software, write 0 to the Start DAQ Register.
- To initiate the data acquisition operation through hardware, apply an active low pulse to the STARTTRIG* pin on the NB-MIO-16X I/O connector. See *Data Acquisition Timing Connections* in Chapter 2, *Configuration and Installation*, for STARTTRIG* signal specifications.

Once the trigger is applied, Counter 3 generates pulses initiating A/D conversions once every sample interval until the sample counter reaches 0 and the last scan cycle is completed. Counter 2 generates a scan interval for each cycle through the scan sequence in the mux-gain memory.

8. Service the data acquisition operation.

Once the data acquisition operation is started by application of a trigger, the operation is serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To do this, perform the following sequence until the desired number of conversion results have been read:

a. Read the Status Register (16-bit read).

b. If the CONVAVAIL bit is set, read the A/D FIFO Register to obtain the result.

Interrupts or DMA can also be used to service the data acquisition operation. These topics are discussed later in this chapter.

Two error conditions may occur during a data acquisition operation–an overflow error, or an overrun error. These error conditions are reported through the Status Register and should be checked every time the Status Register is read to check the CONVAVAIL bit. If either of these error conditions occurs, the data acquisition operation stops.

An overflow condition occurs if more than 16 A/D conversions have been stored in the A/D FIFO without the A/D FIFO being read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is set.

An overrun condition occurs if a second A/D conversion is initiated before the previous conversion is finished. This condition may result in one or more missing A/D conversions. This condition occurs if the sample interval is too small (sample rate is too high). An overrun condition has occurred if the OVERRUN bit in the Status Register is set.

Scanned data acquisition requires slower acquisition rates than single-channel data acquisition because signals must settle each time channels are switched. See Table 4-6 for the maximum recommended multiple-channel data acquisition rates.

Table 4-6. Multiple-Channel Data Acquisition Rates

Board	Gain	Data Acquisition Rate		
		0.01% Settling	0.005% Settling	$^1/_2$ LSB Settling
NB-MIO-16X(H/L)-42	1,2,4,8,10 100 500	23.8 ksamples/sec 20 ksamples/sec 20 ksamples/sec	20 ksamples/sec 20 ksamples/sec 10 ksamples/sec	5 ksamples/sec 2 ksamples/sec 2 ksamples/sec
NB-MIO-16X(H/L)-18	1,2,4,8,10 100 500	33.3 ksamples/sec 20 ksamples/sec 20 ksamples/sec	20 ksamples/sec 20 ksamples/sec 10 ksamples/sec	5 ksamples/sec 2 ksamples/sec 2 ksamples/sec

Both the OVERFLOW and OVERRUN bits in the Status Register are cleared by writing to the A/D Clear Register.

External Timing Considerations for Scanned Data Acquisition

After you follow the programming instructions listed under *External Timing Considerations for Multiple A/D Conversions* earlier in this chapter, complete these additional steps:

1. Set up the analog channel and gain sequence as previously described.
2. Set the SCANEN bit in Command Register 1.
3. Set the mux counter to 0 before starting the data acquisition operation.

Resetting the Hardware after a Data Acquisition Operation

After a data acquisition operation is complete, if no errors occurred and the sample count was less than or equal to 1 0000 hex, then the NB-MIO-16X is left in the same state as it was at the beginning of the data acquisition operation. The counters do not need to be reprogrammed; another data acquisition operation begins when a trigger is received. If the next data acquisition operation requires the counters to be programmed differently, the Am9513A counters that were used must be disarmed and reset.

Resetting Counter 2

To reset Counter 2, use the following programming sequence. All writes are 16-bit operations.

1. Write FFC2 (hex) to the Am9513A Command Register to disarm Counter 2.
2. Write FF02 (hex) to the Am9513A Command Register to select the Counter 2 Mode Register.
3. Write 4 to the Am9513A Data Register to store the Counter 2 mode value such that counter output becomes high-impedance.
4. Write FF0A (hex) to the Am9513A Command Register to select the Counter 2 Load Register.
5. Write 3 to the Am9513A Data Register to store the non-terminal count value in the Counter 2 Load Register.
6. Write FF42 (hex) to the Am9513A Command Register to load Counter 2.
7. Write FF42 (hex) to the Am9513A Command Register a second time to load Counter 2 again to guarantee that Counter 2 is not left in a terminal count state.

Resetting Counter 3

To reset Counter 3, use the following programming sequence. All writes are 16-bit operations.

1. Write FFC4 (hex) to the Am9513A Command Register to disarm Counter 3.
2. Write FF03 (hex) to the Am9513A Command Register to select the Counter 3 Mode Register.
3. Write 4 to the Am9513A Data Register to store the Counter 3 mode value such that counter output becomes high-impedance.
4. Write FF0B (hex) to the Am9513A Command Register to select the Counter 3 Load Register.
5. Write 3 to the Am9513A Data Register to store the non-terminal count value in the Counter 3 Load Register.
6. Write FF44 (hex) to the Am9513A Command Register to load Counter 3.
7. Write FF44 (hex) to the Am9513A Command Register a second time to load Counter 3 again to guarantee that Counter 3 is not left in a terminal count state.

Resetting Counter 4

To reset Counter 4, use the following programming sequence. All writes are 16-bit operations.

1. Write FFC8 (hex) to the Am9513A Command Register to disarm Counter 4.
2. Write FF04 (hex) to the Am9513A Command Register to select the Counter 4 Mode Register.
3. Write 4 to the Am9513A Data Register to store the Counter 4 mode value such that counter output becomes high-impedance. If Counter 4 is not to be used during the next data acquisition operation, write 0 to the Am9513A Data Register to drive the output low.
4. Write FF0C (hex) to the Am9513A Command Register to select the Counter 4 Load Register.
5. Write 3 to the Am9513A Data Register to store the non-terminal count value in the Counter 4 Load Register.
6. Write FF48 (hex) to the Am9513A Command Register to load Counter 4.
7. Write FF48 (hex) to the Am9513A Command Register a second time to load Counter 4 again to guarantee that Counter 4 is not left in a terminal count state.

Resetting Counter 5

To reset Counter 5, use the following programming sequence. All writes are 16-bit operations.

1. Write FFD0 (hex) to the Am9513A Command Register to disarm Counter 5.
2. Write FF05 (hex) to the Am9513A Command Register to select the Counter 5 Mode Register.
3. Write 4 to the Am9513A Data Register to store the Counter 5 mode value such that counter output becomes high-impedance.
4. Write FF0D (hex) to the Am9513A Command Register to select the Counter 5 Load Register.
5. Write 3 to the Am9513A Data Register to store the non-terminal count value in the Counter 5 Load Register.
6. Write FF50 (hex) to the Am9513A Command Register to load Counter 5.
7. Write FF50 (hex) to the Am9513A Command Register a second time to load Counter 5 again to guarantee that Counter 5 is not left in a terminal count state.

After resetting the counters, write 0 to the A/D Clear Register to clear all error conditions and to empty the A/D FIFO.

Programming the Analog Output Circuitry

The voltage at the analog output circuitry output pins (pins DAC0 OUT and DAC1 OUT on the NB-MIO-16X I/O connector) is controlled by loading the DAC in the analog output channel with a 12-bit digital code. This DAC is loaded by writing the digital code to the DAC0 and DAC1 Registers. Writing to the DAC0 Register controls the voltage at the DAC0 OUT pin on the NB-MIO-16X I/O connector. Writing to the DAC1 Register controls the voltage at the DAC1 OUT pin. The analog output on pins DAC0 OUT and DAC1 OUT can be updated in one of three ways–immediately when DAC0 or DAC1 is written to, when an active low pulse is detected on the OUT2 pin of the Am9513A Counter/Timer, or when an active low pulse is received from the RTSI bus. Two bits in Command Register 1 specify which update method is used. If RTSIWGEN is set, then updating is controlled by the RTSI bus. If TMRWGEN is set, then updating is controlled by the OUT2 signal. If neither of these bits is set, then a DAC is updated immediately as it is written to.

The output voltage generated from the digital code depends on the configuration, unipolar or bipolar, of the associated analog output channel. This configuration is determined by configuration jumpers on the NB-MIO-16X board. In bipolar mode, configuration jumpers also determine if the digital code written to the DACs is in straight binary form or in a two's complement form. The factory default is the bipolar configuration in two's complement mode. See *Analog Input Configuration* in Chapter 2, *Configuration and Installation*, for more information. Table 4-7 shows the output voltage versus digital code for a unipolar analog output configuration. Table 4-8 shows the voltage versus digital code for a bipolar analog output configuration.

The formula for the voltage output versus digital code for a unipolar analog output configuration is as follows:

$$V_{out} = V_{ref} * \frac{(\text{digital code})}{4,096}$$

where V_{ref} is the reference voltage applied to the analog output channel. The digital code in the preceding formula is a decimal value ranging from 0 to 4,095.

Table 4-7. Analog Output Voltage Versus Digital Code (Unipolar Mode)

Digital Code		Voltage Output	
Decimal	**Hex**	**V_{ref} = 10 V**	**V_{out}**
0	0	0	0 V
1	1	$\frac{V_{ref}}{4,096}$	2.44 mV
1,024	0400	$\frac{V_{ref}}{4}$	2.5 V
2,048	0800	$\frac{V_{ref}}{2}$	5 V
3,072	0C00	$\frac{V_{ref} * 3}{4}$	7.5 V
4,095	0FFF	$\frac{V_{ref} * 4,095}{4,096}$	9.9976 V

The formula for the voltage output versus digital code for a bipolar analog output configuration in straight binary form is as follows:

$$V_{out} = V_{ref} * \frac{(\text{digital code} - 2,048)}{2,048}$$

where V_{ref} is the reference voltage applied to the analog output channel. The digital code in the preceding formula is a decimal value ranging from 0 to 4,095.

The formula for the voltage output versus digital code for a bipolar analog output configuration in two's complement form is as follows:

$$V_{out} = V_{ref} * \frac{(\text{digital code})}{2,048}$$

where V_{ref} is the positive reference voltage applied to the analog output channel. The digital code in the preceding formula is a decimal value ranging from -2,048 to +2,047.

Table 4-8. Analog Output Voltage Versus Digital Code (Bipolar Mode)

Digital Code				Voltage Output	
Straight Binary		Two's Complement			
Decimal	Hex	Decimal	Hex	V_{ref} = 10 V	V_{out}
0	0	-2,048	F800	0	-10 V
1	1	-2,047	F801	$\frac{V_{ref} * (-2,047)}{2,048}$	-9.9951 V
1,024	0400	-1,024	FC00	$\frac{-V_{ref}}{2}$	-5 V
2,047	07FF	-1	FFFF	$\frac{-V_{ref}}{2,048}$	-4.88 mV
2,048	0800	0	0	0	0 V
2,049	0801	1	1	$\frac{V_{ref}}{2,048}$	4.88 mV
3,072	0C00	1,024	0400	$\frac{V_{ref}}{2}$	5 V
4,095	0FFF	2,047	07FF	$\frac{V_{ref} * 2,047}{2,048}$	9.9951 V

Programming the Digital I/O Circuitry

The digital input circuitry is controlled and monitored using the Digital Input Register, the Digital Output Register, and the two bits DOUTAEN and DOUTBEN in Command Register 2. See the register bit descriptions earlier in this chapter for more information.

To enable digital output port A, set the DOUTAEN bit in Command Register 2. To enable digital output port B, set the DOUTBEN bit in Command Register 2. When a digital output port is enabled, the contents of the Digital Output Register are driven onto the digital lines corresponding to that port. The digital output for both ports 0 and 1 are updated by writing the desired pattern to the Digital Output Register.

In order for an external device to drive the digital I/O lines, the input ports must be enabled. Clear the DOUTAEN bit in Command Register 2 if an external device is driving digital I/O lines ADIO<3..0>. Clear the DOUTBEN bit in Command Register 2 if an external device is driving digital I/O lines BDIO<3..0>. The Digital Input Register can then be read to monitor the state of the digital I/O lines as driven by the external device.

The logic state of all eight digital I/O lines can be read from the Digital Input Register. If the digital output ports are enabled, the Digital Input Register serves as a read-back register; that is, you can determine how the NB-MIO-16X is driving the digital I/O lines by reading the Digital Input Register.

If any digital I/O line is not driven, it floats to an indeterminate value. If more than one device is driving any digital I/O line, the voltage at that line may also be indeterminate. In these cases, the digital line has no meaningful logic value, and reading the Digital Input Register may return either 1 or 0 for the state of the digital line.

Programming the Am9513A Counter/Timer

Counters 1, 2, and 5 of the Am9513A Counter/Timer are available for general-purpose timing applications. The programmable frequency output pin FOUT is also available as a timing signal source. These applications and a general description of the Am9513A Counter/Timer are included in *Data Acquisition Timing Connections* in Chapter 2, *Configuration and Installation. Timing I/O Circuitry* in Chapter 3, *Theory of Operation*, explains how the Am9513A is used on the NB-MIO-16X board.

Initialization of the Am9513A as required by the NB-MIO-16X and specific programming requirements for the sample-interval and sample counters are given earlier in this chapter. For general programming details for Counters 1, 2 and 5, and the programmable frequency output, refer to Appendix C, *AMD Data Sheet.*

In programming the Master Mode Register, keep the following considerations in mind:

- The Am9513A must be used in 16-bit bus mode.
- The scalar control should be set to BCD division for correct operation of the clocks as described under *Programming Multiple A/D Programming Conversions on a Single Input Channel* earlier in this chapter.

RTSI Bus Trigger Line Programming Considerations

The RTSI switch connects signals on the NB-MIO-16X to the seven RTSI bus trigger lines. The RTSI switch has seven pins labeled A<6:0> connected to NB-MIO-16X signals, and seven pins labeled B<6:0> connected to the seven RTSI bus trigger lines. Table 4-9 shows the signals connected to each pin.

Table 4-9. RTSI Switch Signal Connections

RTSI Switch Pin	Signal Name	Signal Direction
A Side:		
A0	EXTCONV*	Bidirectional
A1	RTSIWG	Input
A2	OUT2	Output
A2	GATE1	Input
A3	SOURCE5	Bidirectional
A4	OUT5	Output
A4	STOPTRIG	Input
A5	OUT1	Bidirectional
A6	STARTTRIG*	Bidirectional
B Side:		
B0	TRIGGER0	Bidirectional
B1	TRIGGER1	Bidirectional
B2	TRIGGER2	Bidirectional
B3	TRIGGER3	Bidirectional
B4	TRIGGER4	Bidirectional
B5	TRIGGER5	Bidirectional
B6	TRIGGER6	Bidirectional

Figure 3-8 in Chapter 3, *Theory of Operation*, diagrams the NB-MIO-16X RTSI switch connections.

NB-MIO-16X RTSI Signal Connection Considerations

The NB-MIO-16X board has a total of nine signals connected to the seven A-side pins of the RTSI switch. These same signals also appear at the NB-MIO-16X I/O connector. As shown in Table 4-8, two NB-MIO-16X signals are connected to pin A2, and two signals are connected to pin A4. The routing of these signals is further controlled by the bits A4DRV, A4RCV, A2DRV, and A2RCV in Command Register 2.

- To drive the RTSI switch pin A2 with the signal OUT2, set the A2DRV bit in Command Register 2. Otherwise, clear the A2DRV bit.
- To drive the signal GATE1 from pin A2 of the RTSI switch, set the A2RCV bit in Command Register 2. Otherwise, clear the A2RCV bit.

Note: If both the A2DRV and A2RCV bits are set, the GATE1 signal is driven by the signal OUT2. This arrangement is probably not desirable.

- To drive the RTSI switch pin A4 with the signal OUT5, set the A4DRV bit in Command Register 2. Otherwise, clear the A4DRV bit.
- To drive the signal STOPTRIG from pin A4 of the RTSI switch, set the A4RCV bit in Command Register 2. Otherwise, clear the A4RCV bit.

Note: If both the A4DRV and A4RCV bits are set, the STOPTRIG signal is driven by the signal OUT5. This arrangement is probably not desirable.

Programming the RTSI Switch

The RTSI switch can be programmed to connect any of the signals on the A side to any of the signals on the B side and vice versa. To do this, a 56-bit pattern is shifted into the RTSI switch by writing one bit at a time to the RTSI Switch Shift Register and then writing to the RTSI Switch Strobe Register to load the pattern into the RTSI switch.

The 56-bit pattern is made up of two 28-bit patterns–one for each side (A and B) of the RTSI switch. The low-order 28 bits select the signal sources for the B-side pins. The high-order 28 bits select the signal sources for the A-side pins. Each of the 28-bit patterns are made up of seven 4-bit fields, one for each pin. The 4-bit field selects the signal source and the output enable for the pin. Figure 4-1 shows the bit map of the RTSI switch 56-bit pattern.

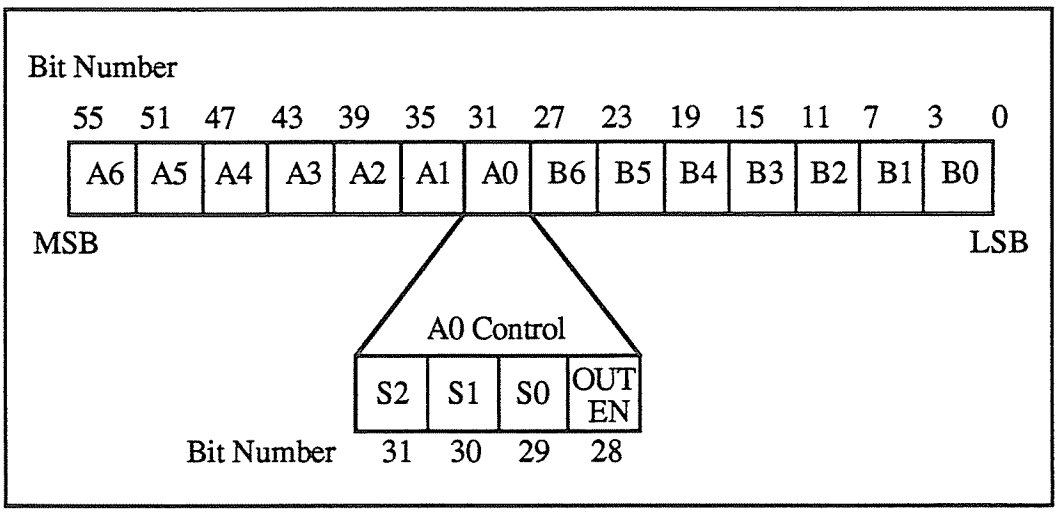


Figure 4-1. RTSI Switch Control Pattern

In Figure 4-1, the fields labeled A6 through A0 and B6 through B0 are the 4-bit control fields for each RTSI switch pin of the same name. The 4-bit control field for pin A0 is shown in Figure 4-1.

The bits labeled S2 through S0 are the signal source selection bits for the pin. One of seven source signals can be selected. Pins A6 through A0 can select any of the pins B6 through B0 as signal sources. Pins B6 through B0 select any of the pins A6 through A0 as signal sources. For example, the pattern 011 for S2 through S0 in the A0 control field selects the signal connected to pin B3 as the signal source for pin A0.

The bit labeled OUTEN is the output enable bit for that pin. If the OUTEN bit is set, the pin is driven by the selected source signal (the pin acts as an output pin). If the OUTEN bit is cleared, the pin is not driven regardless of the source signal selected; instead, the pin can be used as an input pin.

If the A0 control field in Figure 4-1 contains the pattern 0111, the signal connected to pin B3 (Trigger Line 3) appears at pin A0. On the NB-MIO-16X board, this arrangement allows the EXTCONV* signal to be driven by Trigger Line 3. Conversely, if the B4 control field contains the pattern 1011, the signal connected to pin A5 appears at pin B4. This arrangement allows Trigger Line 4 to be driven by the NB-MIO-16X OUT1 signal. In this way, boards connected via the RTSI bus can send signals to each other over the RTSI bus trigger lines.

To program the RTSI switch, complete these steps:

1. Calculate the 56-bit pattern based on the desired signal routing.
   a. Clear the OUTEN bit for all input pins and for all unused pins.
   b. Specify the signal source pin for all output pins by setting bits S2 through S0 to the source pin number.
   c. Set the OUTEN bit for all output pins.
2. For $i = 0$ to 55, do the following.
   a. Copy bit i of the 56-bit pattern to bit 0 of an 8-bit temporary variable.
   b. Write the temporary variable to the RTSI Switch Shift Register (8-bit write).
3. Write 0 to the RTSI Switch Strobe Register (8-bit write). This operation loads the 56-bit pattern into the RTSI switch. At this point, the new signal routing takes effect.

Step 2 above can be completed by simply writing the low-order 8 bits of the 56-bit pattern to the RTSI Switch Shift Register, then shifting the 56-bit pattern right once, and repeating this two-step operation a total of 56 times. Only bit 0 of the word written to the RTSI Switch Shift Register is used. The higher-order bits are ignored.

Programming DMA Operations

DMA operations can be used for servicing the A/D FIFO during a data acquisition operation if a DMA board is used in the system and if it is connected with the NB-MIO-16X board over the RTSI bus.

The NB-MIO-16X can be programmed such that the A/D FIFO generates a DMA request signal every time one or more A/D conversion values are stored in the A/D FIFO. To program the NB-MIO-16X for DMA operation, perform the following steps after the circuitry on the NB-MIO-16X is set up for a data acquisition operation and before the data acquisition operation begins:

1. Program the DMA board DMA controller to service DMA requests from the NB-MIO-16X board.
2. Set the DMAA<2..0> bits in Command Register 2 to the DMA channel to be used. DMA channels 0, 1, 2, 3, 5, 6, and 7 are available. DMA channel 4 is not available over the RTSI bus.
3. Set the DMAEN bit in Command Register 1 to enable DMA request generation.

When you have completed these steps, the DMA controller automatically reads the A/D FIFO Register whenever an A/D conversion result is available and stores the result in a buffer in memory.

Programming instructions for a DMA board are included in the manual that came with your DMA board. You need the following information to program the DMA Controller on a DMA board:

- The requestor is the NB-MIO-16X board.
- The requestor device type is an I/O device.
- The requestor hold bit should be set to hold.
- The requestor address is the A/D FIFO Register NuBus address, as shown in the following table.

Slot Number	NB-MIO-16X Requestor Address (Hex)
9	F9F0 002C
A	FAF0 002C
B	FBF0 002C
C	FCF0 002C
D	FDF0 002C
E	FEF0 002C

- Transfer cycle mode is two-cycle (fetch-and-deposit).
- Data transfer mode is single transfer mode.
- The requestor bus size is 16-bit.
- The transfer type is write transfer (write to target).
- The target device is a memory buffer (and therefore a memory device).
- The target address is the program address of the memory buffer that is to be written to.
- The target address bit should be set to increment.
- The target device bus size should be set to a 32-bit bus, which is more efficient.
- The byte count is two times the desired number of samples (sample count) minus 1.

Interrupt Programming

Three different interrupts are generated by the NB-MIO-16X board:

- An interrupt is generated whenever a conversion is available to be read from the A/D FIFO.
- An interrupt is generated whenever a data acquisition operation completes or an acquisition error occurs.
- An interrupt is generated whenever a rising edge occurs on the OUT2 pin of the Am9513A.

Interrupts can be used for servicing the A/D FIFO during a data acquisition operation. Two different interrupts are generated by the NB-MIO-16X board–an interrupt that is generated whenever a conversion is available to be read from the A/D FIFO, and an interrupt that is generated whenever the acquisition process terminates. The data acquisition process terminates whenever the sample counter terminates or an error occurs. These two interrupts are enabled individually.

To use the conversion interrupt, set the CONVINTEN bit in Command Register 1. A conversion interrupt has occurred if the following three conditions are met–the CONVINTEN bit is set, an interrupt occurs from the NB-MIO-16X board, and the CONVAVAIL bit in the Status Register is set. Reading from the A/D FIFO Register clears this interrupt condition. Writing to the A/D Clear Register also clears the conversion interrupt.

To use the data acquisition completion interrupt, set the CMPLINTEN bit in Command Register 1. A data acquisition completion interrupt has occurred if the following three conditions are met–the CMPLINTEN bit is set, an interrupt occurs from the NB-MIO-16X board, and the CMPLINT bit in the Status Register is set. Writing to the A/D Clear Register clears the conversion interrupt and also empties the A/D FIFO; therefore, read all remaining A/D conversion results from the A/D FIFO Register before writing to the A/D Clear Register.

Note: This interrupt is generated at the beginning of the last conversion of a data acquisition sequence. Thus, an interrupt service routine may be called even before the last conversion is finished. You should wait until the last conversion is finished (100 µsec is a safe period) before reading the FIFO or terminating the DMA process, if one is being used.

Interrupts can also be generated at programmed intervals using Counter 2 of the Am9513A. This kind of interrupt is useful for timer-controlled DAC waveform generation. To use the OUT2 interrupt, set the TMRINTEN bit in Command Register 1. If enabled, an OUT2 interrupt occurs on the rising edge of OUT2, at which time the TIMERUP bit is set. Writing to the TMRINTCL register or writing to either of the DACs clears the interrupt and clears the TIMERUP bit. For more information, see *Programming the Analog Output Circuitry* earlier in this chapter.

The NBINTDIS bit in Command Register 2 must be cleared for these interrupts to be driven onto the NuBus.

Refer to your Macintosh documentation for information about initializing and servicing interrupts in the Macintosh.

Chapter 5
Calibration Procedures

This chapter discusses the calibration procedures for the NB-MIO-16X analog input and analog output circuitry.

The NB-MIO-16X is calibrated at the factory before shipment. To maintain accuracy of the NB-MIO-16X analog input and analog output circuitry, recalibration at six-month intervals is recommended. Factory calibration is performed with the NB-MIO-16X in its default factory configuration:

- DIFF analog input mode
- -10 to +10 V analog input range (bipolar)
- -10 to +10 V analog output range (bipolar with internal 10 V reference selected)

Recalibration of your NB-MIO-16X board is recommended any time you change your board configuration.

Calibration Equipment Requirements

For best measurement results, the NB-MIO-16X should be calibrated so that its measurement accuracy is within ±0.01 percent of its input range. According to standard practice, the equipment used to calibrate the NB-MIO-16X should have ±0.001 percent rated accuracy. To calibrate the NB-MIO-16X board, you need the following equipment:

- For analog input calibration, you need a precision variable DC voltage source (usually a calibrator) with these attributes:

  Accuracy: ±0.001%

  Range: ±10 V or greater

  Resolution: 100 µV in ±10 V range (5½ digits)

- For analog output calibration, you need a voltmeter with these attributes:

  Accuracy: ±0.001% recommended
  ±0.003% sufficient

  Range: ±10 V or greater

  Resolution: 100 µV in ±10 V range (5½ digits)

Calibration Trimpots

There are seven trimpots on the NB-MIO-16X for calibration. The locations of these trimpots on the NB-MIO-16X board are shown in the partial diagram of the board in Figure 5-1.

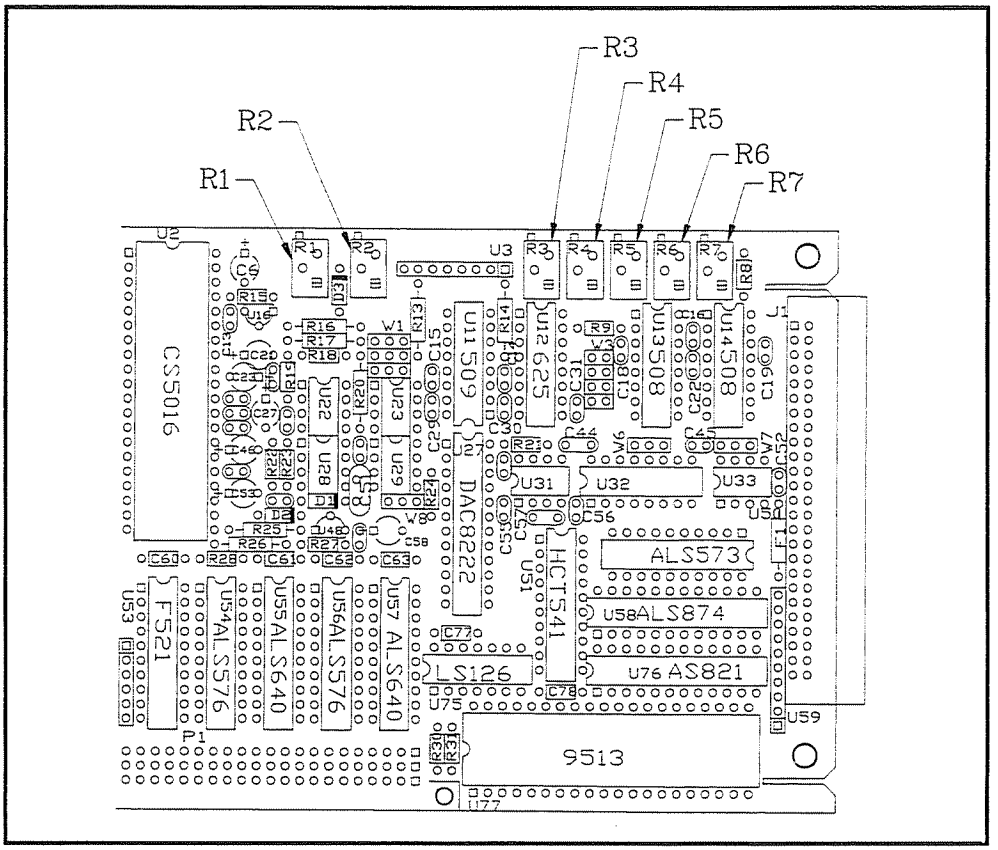


Figure 5-1. Calibration Trimpot Location Diagram

The following trimpots are used to calibrate the analog input circuitry:

- R1 – Offset trim, analog input
- R2 – Gain trim, analog input
- R3 – Instrumentation amplifier input offset trim

The following trimpots are used to calibrate the analog output circuitry:

- R4 – Gain trim, analog output Channel 0
- R5 – Gain trim, analog output Channel 1
- R6 – Offset trim, analog output Channel 0
- R7 – Offset trim, analog output Channel 1

Analog Input Calibration

To null out error sources that compromise the quality of measurements, you should calibrate the analog input circuitry by adjusting the following potential sources of error:

- Offset error at the input of the instrumentation amplifier
- Offset error at the input of the ADC
- Gain error of the analog input circuitry

Offsets at the input to the instrumentation amplifier contribute gain-dependent error to the analog input system. This offset is multiplied by the gain of the instrumentation amplifier. To calibrate this offset, you should ground the analog input, read it at two different gain settings, and adjust a trimpot until the readings match at the two different gain settings.

Offset error at the input of the ADC is the total of the voltage offsets contributed by the circuitry from the output of the instrumentation amplifier to the ADC input (including the ADC's own offsets). Offset errors appear as a voltage added to the input voltage being measured. To calibrate this offset, you should ground the analog input and adjust a trimpot until the ADC returns readings of 0.

All the stages up to and including the input of the ADC contribute to the gain error of the analog input circuitry. With the instrumentation amplifier set to a gain of 1, the gain of analog input circuitry is ideally 1. The gain error is the deviation of the gain from 1 and appears as a multiplication of the input voltage being measured. To calibrate this offset, you should apply near V_{+fs} to the analog input circuitry and adjust a potentiometer until the ADC returns readings near the corresponding ADC code. We recommend using V_{+fs} - 16 LSB.

Sample Averaging

At 16-bit resolution, calibration becomes complicated by the presence of even small amounts of noise. The NB-MIO-16X itself contributes about 1 to 2 LSB rms of noise to the signal when the range is -10 to +10 V. To resolve to greater precision than can be achieved with single readings, you should take a few hundred samples (with a data acquisition sequence) and average the samples. Averaging the samples reduces the amount of noise present in each sample by a factor of approximately the square root of the number of samples averaged. For example, if 100 samples are averaged, the amount of noise in the average is about $1\backslash_{10}$ of the noise in a single sample.

Board Configuration

Calibration procedure differs depending on the input ranges and input configuration modes selected. This section describes two analog input calibration procedures–one for the bipolar input configurations (-10 to +10 V and -5 to +5 V), and one for the unipolar input configurations (0 to +10 V and 0 to +5 V).

The calibration procedures presented here assume that your NB-MIO-16X board is configured for DIFF input. If necessary, reconfigure your board for DIFF input before using the following calibration procedures.

If you wish to calibrate your board with a nondifferential input setting, the procedure is similar to the procedures outlined in this section with the following exception–the procedures in this section apply the input calibration voltages across the positive (+) and negative (-) inputs for differential channel 0. For single-ended input, apply your calibration voltages between the channel 0 positive (+) input and the ground system you are using. Refer to Chapter 2, *Configuration and Installation*, for instructions on using single-ended input connections.

Bipolar Input Calibration Procedure

If your board is configured for bipolar input (-5 to +5 V or -10 to +10 V range), then complete the following procedure in sequence. This procedure assumes that ADC readings are in the range -32,768 to +32,767.

1. Adjust the programmable gain amplifier input offset.

To adjust the amplifier input offset, follow these steps:

a. Connect both ACH0 (pin 3 on the I/O connector) and ACH8 (pin 4) to AIGND (pin 1 or 2).

b. Take analog input readings from Channel 0 at the following gains:

- Both 1 and 100 for the NB-MIO-16XL
- Both 1 and 8 for the NB-MIO-16XH

c. Adjust trimpot R3 until the readings match to within one LSB of each other.

2. Adjust the ADC input offset.

To adjust the ADC input offset, follow these steps:

a. Connect both ACH0 (pin 3 on the I/O connector) and ACH8 (pin 4) to AIGND (pin 1 or 2).

b. Take analog input readings from Channel 0 at a gain of 1, and adjust trimpot R1 until the ADC readings are within one LSB of 0.

3. Adjust the analog input gain.

Adjust the analog input gain by applying an input voltage across ACH0 and ACH8. This input voltage should be V_{+fs} - 16 LSB and depends on the input range selected:

Input Range	Calibration Voltage
-10 to +10 V	+9.995117 V
- 5 to +5 V	+4.997559 V

a. Connect the calibration voltage across ACH0 (pin 3 on the I/O connector) and ACH8 (pin 4). Connect the ground point on the calibration voltage source to AIGND (pin 1 or 2).

b. Take analog input readings from Channel 0 at a gain of 1, and adjust trimpot R2 until the ADC readings are within one LSB of 32752.

Unipolar Input Calibration Procedure

If your board is configured for unipolar input (0 to +5 V or 0 to +10 V range), then complete the following procedure in sequence. This procedure assumes that ADC readings are in the range 0 to +65,535.

1. Adjust the amplifier input offset.

To adjust the amplifier input offset, follow these steps:

a. Connect both ACH0 (pin 3 on the I/O connector) and ACH8 (pin 4) to AIGND (pin 1 or 2).

b. If you are calibrating for a unipolar range, take analog input readings from Channel 0 at a gain of 1, and adjust trimpot R1 until a reading of roughly ten LSBs is returned. This step is necessary because in unipolar mode, the ADC cannot return readings below 0.

c. Take analog input readings from Channel 0 at the following gains:

- Both 1 and 100 for the NB-MIO-16XL
- Both 1 and 8 for the NB-MIO-16XH

d. Adjust trimpot R3 until the readings at each gain setting match to within one LSB of each other.

2. Adjust the ADC input offset.

Adjust the ADC input offset by applying an input voltage across ACH0 and ACH8. This input voltage should be 0 V + 16 LSB, and depends on the input range selected:

Input Range	Calibration Voltage
0 to +10 V	+0.002441 V
0 to +5 V	+0.001221 V

a. Connect the calibration voltage across ACH0 (pin 3 on the I/O connector) and ACH8 (pin 4). Connect the ground point on the calibration voltage source to AI SENSE (pin 19).

b. Take analog input readings from Channel 0 at a gain of 1, and adjust trimpot R1 until the ADC readings are within one LSB of 16.

3. Adjust the analog input gain.

Adjust the analog input gain by applying an input voltage across ACH0 and ACH8. This input voltage should be V_{+fs} - 16 LSB, and depends on the input range selected:

Input Range	Calibration Voltage
0 to +10 V	+9.997559 V
0 to +5 V	+4.998779 V

a. Connect the calibration voltage (+9.99634 V) across ACH0 (pin 3 on the I/O connector) and ACH8 (pin 4). Connect the ground point on the calibration voltage source to AI SENSE (pin 19).

b. Take analog input readings from Channel 0 at a gain of 1, and adjust trimpot R2 until the ADC readings are within one LSB of 65,520.

Analog Output Calibration

To null out error sources that affect the accuracy of the output voltages generated, you should calibrate the analog output circuitry by adjusting the following potential sources of error:

- Analog output offset error
- Analog output gain error

Offset error in the analog output circuitry is the total of the voltage offsets contributed by each component in the circuitry. This error appears as a voltage difference between the desired voltage and the actual output voltage generated, and is independent of the D/A setting. To correct this offset gain error, set the D/A to negative full-scale and adjust a trimpot until the output voltage is the negative full-scale value ±0.5 LSB.

Gain error in the analog output circuitry is the product of the gains contributed by each component in the circuitry. This error appears as a voltage difference between the desired voltage and the actual output voltage generated, which depends on the D/A setting. This gain error is corrected by setting the D/A to positive full-scale minus 1 LSB and adjusting a trimpot until the output voltage corresponds to the positive full-scale value minus 1 LSB ±0.5 LSB.

Board Configuration

The calibration procedures in this section assume that the internal voltage reference +10 V is selected for the analog output channel to be calibrated.

If you wish to calibrate your board to an external reference input (DC only), you should recalculate the desired output voltages to calibrate to the following values:

- For bipolar output:

$$1\ LSB = \frac{V_{extref}}{2,048} \text{ (therefore, } 0.5\ LSB = \frac{V_{extref}}{4,096})$$

$V_{-fs} = -V_{extref}$
$V_{+fs} = V_{extref}$

- For unipolar output:

$$1\ LSB = \frac{V_{extref}}{4,096} \text{ (therefore, } 0.5\ LSB = \frac{V_{extref}}{8,192})$$

$V_{-fs} = 0\ V$
$V_{+fs} = V_{extref}$

In calibrating to your own external reference, you should write your own procedures using the following procedures as a guide. Substitute your calculated voltages for those given.

If you are programming the board yourself, then you should clear the TMRWGEN and RTSIWGEN bits in Command Register 1 so that the outputs of the DACs are updated immediately after they are written to.

The calibration procedure differs if you select either bipolar or unipolar output configuration. This section has a procedure for each configuration.

Bipolar Output Calibration Procedure

If your board is configured for bipolar output (-10 to +10 V range), then complete the following procedure in sequence.

1. Adjust the analog output offset.

Adjust the analog output offset by measuring the output voltage generated with the DACs set at negative full-scale. This output voltage should be V_{-fs} ±0.5 LSB. For bipolar output, V_{-fs} = -10 V, and 0.5 LSB = 2.44 mV.

- For analog output Channel 0:

  a. Connect the voltmeter between DAC0 OUT (pin 20 on the I/O connector) and AOGND (pin 23).

  b. Set the analog output channel to -10 V by writing -2,048 to DAC0.

  c. Adjust trimpot R6 until the output voltage read is -10 V ±2.44 mV, that is, between -10.00244 V and -9.99756 V.

- For analog output Channel 1:

  a. Connect the voltmeter between DAC1 OUT (pin 21 on the I/O connector) and AOGND (pin 23).

  b. Set the analog output channel to -10 V by writing -2,048 to DAC1.

  c. Adjust trimpot R7 until the output voltage read is -10V ± 2.44 mV, that is, between -10.00244 V and -9.99756 V.

2. Adjust the analog output gain.

Adjust the analog output gain by measuring the output voltage generated with the DACs set at positive full-scale. This output voltage should be (V_{+fs} - 1 LSB) ±0.5 LSB. For bipolar output, V_{+fs} - 1 LSB = +9.99512 V, and 0.5 LSB = 2.44 mV.

- For analog output Channel 0:

  a. Connect the voltmeter between DAC0 OUT (pin 20 on the I/O connector) and AOGND (pin 23).

  b. Set the analog output channel to +9.99512 V by writing 2,047 to DAC0.

  c. Adjust trimpot R4 until the output voltage read is +9.99512 V ±2.44 mV, that is, between 9.99268 V and 9.99756 V.

- For analog output Channel 1:

  a. Connect the voltmeter between DAC1 OUT (pin 21 on the I/O connector) and AOGND (pin 23).

  b. Set the analog output channel to +9.99512 V by writing 2,047 to DAC1.

  c. Adjust trimpot R5 until the output voltage read is +9.99512 V ±2.44 mV, that is, between 9.99268 V and 9.99756 V.

Unipolar Output Calibration Procedure

If your analog output channel is configured for unipolar output (0 to +10 V range), then calibrate your board according to the following procedure.

1. Adjust the analog output offset.

Adjust the analog output offset by measuring the output voltage generated with the DACs set at 0. This output voltage should be V_{-fs} ±0.5 LSB. For unipolar output, V_{-fs} = 0 V, and 0.5 LSB = 1.22 mV.

- For analog output Channel 0:

  a. Connect the voltmeter between DAC0 OUT (pin 20 on the I/O connector) and AOGND (pin 23).

  b. Set the analog output channel to 0 V by writing 0 to DAC0.

  c. Adjust trimpot R6 until the output voltage read is 0 V ±1.22 mV.

- For analog output Channel 1:

  a. Connect the voltmeter between DAC1 OUT (pin 21 on the I/O connector) and AOGND (pin 23).

  b. Set the analog output channel to 0 V by writing 0 to DAC1.

  c. Adjust trimpot R7 until the output voltage read is 0 V ±1.22 mV.

2. Adjust the analog output gain.

Adjust the analog output gain, by measuring the output voltage generated with the DACs set at positive full-scale. This output voltage should be (V_{+fs} - 1 LSB) ±0.5 LSB. For unipolar output, V_{+fs} - 1 LSB = +9.99756 V, and 0.5 LSB = 1.22 mV.

- For analog output Channel 0:

  a. Connect the voltmeter between DAC0 OUT (pin 20 on the I/O connector) and AOGND (pin 23).

  b. Set the analog output channel to +9.99756 V by writing 4,095 to DAC0.

  c. Adjust trimpot R4 until the output voltage read is +9.99756 V ±1.22 mV, that is, between 9.99634 V and 9.99878 V.

- For analog output Channel 1:

  a. Connect the voltmeter between DAC1 OUT (pin 21 on the I/O connector) and AOGND (pin 23).

  b. Set the analog output channel to +9.99756 V by writing 4,095 to DAC1.

  c. Adjust trimpot R5 until the output voltage read is +9.99756 V ±1.22 mV, that is, between 9.99634 V and 9.99878 V.

Appendix A
Specifications

This appendix lists the specifications of the NB-MIO-16X. These specifications are typical at 25° C, unless otherwise stated. The operating temperature range is 0° C to 70° C.

Analog Input

Number of input channels	16 single-ended, 8 differential
Analog resolution	16-bit, 1 in 65,536
Type of ADC	successive approximation
Relative accuracy (nonlinearity and quantization error)	±1.5 LSB maximum over temperature
Integral nonlinearity (see *Explanation of Analog Input Specifications* later in this appendix)	±1 LSB maximum over temperature, ±0.5 LSB, typical
Differential nonlinearity	±1 LSB maximum (no missing codes over temperature), ±0.25 LSB, typical
Differential analog input ranges	±10 V, ±5 V, 0 to +10 V, or 0 to +5 V, jumper-selectable
Analog input range	±12 V
Common mode range	±7 V for ±10 V or 0 to +10 V differential analog input range ±9.5 V for ±5 V or 0 to +5 V differential analog input range
Instrumentation amplifier	
Common mode rejection ratio	75 dB minimum, DC through 100 Hz
Input bias current	±25 nA maximum
Input offset current	±15 nA maximum
Input impedance	1 GΩ in parallel with 50 pF
System noise (figures are for 20 V range; multiply by 2 for 10 V range, by 4 for 5 V range)	1.5 LSB rms for gains 1 to 10 2 LSB rms for gain 100 4 LSB rms for gain 500

Gains available	1, 2, 4, and 8 for NB-MIO-16XH, 1, 10, 100, and 500 for NB-MIO-16XL, software-selectable
Gain adjustment range	+5.5%, -1.2% of fullscale
Gain accuracy (for gain > 1, when gain error has been adjusted to 0 at gain = 1)	±0.08% of fullscale, adjustable to 0
Instrumentation amp input offset voltage adjustment range	±50 mV for gain 1, adjustable to 0 ±25 mV for gain 2 ±15 mV for gain 4 ±10 mV for gain 8 ±5 mV for gain 10 ±2 mV for gain 100 ±1.5 mV for gain 500
A/D offset voltage adjustment range	±4.5 mV
Offset voltage error: (applies only when using DMA at 18 µsec or 42 µsec)	-2 LSB, maximum

This offset voltage occurs when sampling synchronously with DMA operations and does not occur at any other frequencies.

Data transfers	DMA, programmed I/O, interrupts

Explanation of Analog Input Specifications

The *integral nonlinearity* specification is a measure of the fidelity of the the ADC. Because of noise in the system, an ADC reading is really a sample of a statistical distribution whose ideal mean is the digital code (possibly fractional) corresponding to the voltage input to the board. *Integral nonlinearity* guarantees that the real mean of the distribution from which the sample comes does not deviate from the ideal by more than the specified amount. The ideal analog-input-to-digital-output transfer is a straight line connecting the endpoints, and thus is independent of the calibration. If the NB-MIO-16X were perfectly calibrated, however, *integral nonlinearity* would indicate the absolute accuracy of the system.

Differential nonlinearity is a measure of the deviation of code widths from their theoretical value of 1 LSB. The width of a given code is the size of the range of analog values that can be input to produce that code, ideally 1 LSB. A specification of ±1 LSB differential nonlinearity ensures that no code has a width of 0 LSBs (that is, no missing codes) and that no code width exceeds 2 LSBs.

System noise is the amount of noise typically seen by the ADC when there is no signal present at the input of the board. The noise is additive (with zero mean), is fairly Gaussian, and has typically the variance specified (in units LSB's rms).

Analog Data Acquisition Rates

Single-Channel Acquisition Rates

The following are the maximum data acquisition rates for each version of the NB-MIO-16X.

Board	Maximum Rate
NB-MIO-16X(H/L)-42	24 ksamples/sec
NB-MIO-16X(H/L)-18	55 ksamples/sec

Multiple-Channel Acquisition Rates

The following are the maximum recommended scan rates for each version of the NB-MIO-16X:

Board	Gain	Data Acquisition Rate		
		0.01% Settling	0.005% Settling	$^1/_2$ LSB Settling
NB-MIO-16X(H/L)-42	1,2,4,8,10	23.8 ksamples/sec	20 ksamples/sec	5 ksamples/sec
	100	20 ksamples/sec	20 ksamples/sec	2 ksamples/sec
	500	20 ksamples/sec	10 ksamples/sec	2 ksamples/sec
NB-MIO-16X(H/L)-18	1,2,4,8,10	33.3 ksamples/sec	20 ksamples/sec	5 ksamples/sec
	100	20 ksamples/sec	20 ksamples/sec	2 ksamples/sec
	500	20 ksamples/sec	10 ksamples/sec	2 ksamples/sec

Recommended multiple-channel scanning rates are slower than single-channel acquisition rates for higher gains, because as gain is increased, the NB-MIO-16X circuitry takes longer to settle from one channel voltage to the next. Also, the larger the voltage difference between two analog input channels, the longer it takes for the NB-MIO-16X circuitry to settle to within a given accuracy of the new channel voltage. A full-scale difference between input channels is the worst-case switching condition for channel scanning settling time, with one channel at the positive end of the full-scale range and the other channel at the negative end of the full-scale range. At a gain of 1, the full-scale voltage difference is 20 V, and the half full-scale voltage difference is 10 V.

The lower the analog input source impedance, the better the settling time performance. The measurements in the preceding table were made using a low noise, low impedance voltage source. The settling times were in response to a full-scale voltage difference (20 V for unity gain) between channels.

Analog Output

Number of output channels	2
Type of DAC	12-bit, multiplying, double-buffered
Integral nonlinearity	±0.5 LSB maximum, ±0.25 LSB typical
Differential nonlinearity	±1 LSB maximum (monotonic over temperature), ±0.2 LSB typical
Gain adjustment range	±0.44% of fullscale
Offset voltage adjustment range	±64 mV bipolar mode ±32 mV unipolar mode
Internal voltage reference (can be multiplied by 2)	5 V; adjustable from 4.725 to 5.060 V 20 ppm/°C drift
Output voltage ranges	0 to 5 V or 0 to 10 V, unipolar mode; ±5 V or ±10 V, bipolar mode, jumper-selectable
Current drive capability	±2 mA
Output settling time to 0.01%	15 µsec for 20 V step
Output slew rate	2.5 V/µsec
Output noise	12 mV rms, DC to 20 MHz
Data transfers	programmed I/O, interrupts
Output impedance	0.1 Ω maximum

Explanation of Analog Output Specifications

Integral nonlinearity in a D/A system is the worst-case deviation from the ideal digital-input-to-analog-output transfer (a straight line), excepting noise. If a D/A system has been calibrated perfectly, then the relative accuracy specification reflects its worst-case absolute error.

Differential nonlinearity in a D/A system is a measure of deviation of code width from 1 LSB. In this case, code width is the difference between the analog values produced by consecutive digital codes. A specification of ±1 LSB differential nonlinearity ensures that the code width is always greater than 0 LSBs (guaranteeing monotonicity) and is always less than 2 LSBs.

Digital I/O

Compatibility	TTL-compatible
Output current source capability	Can source 2.6 mA and maintain V_{OH} at 2.4 V
Output current sink capability	Can sink 24 mA and maintain V_{OL} at 0.5 V

Timing I/O

Number of channels	4: 3 counter/timers and 1 frequency output
Resolution	16-bit for 3 counter/timers, 4-bit for frequency output channel
Base clock available	1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz
Base clock accuracy	±0.01%
Compatibility	TTL-compatible inputs and outputs. Counter gate and source inputs are pulled up with onboard 4.7 KΩ resistors
Counter input frequency	6.9 MHz maximum (145 nsec period) with a minimum pulse width of 70 nsec

Power Requirement (from Macintosh NuBus)

Power consumption	1.4 A at +5 VDC 30 mA at +12 VDC 36 mA at -12 VDC

Physical

Board dimensions	12.8 by 4 in.
I/O connector	50-pin male ribbon cable connector

Operating Environment

Component temperature	0° to 70° C
Relative humidity	5% to 90% noncondensing

Storage Environment

Temperature	-55° to 150° C
Relative humidity	5% to 90% noncondensing

Appendix B
I/O Connector

Figure B-1 contains the pinout and signal names for the NB-MIO-16X 50-pin I/O connector.

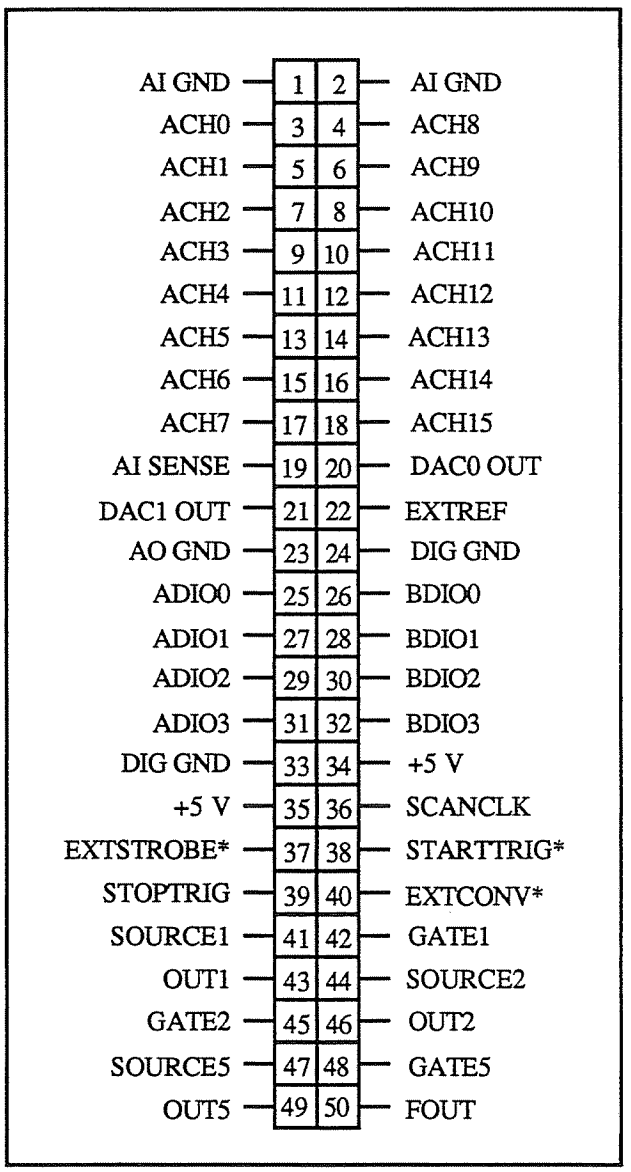


Figure B-1. NB-MIO-16X I/O Connector

Detailed signal specifications are included in Chapter 2, *Configuration and Installation.*

Appendix C
AMD Data Sheet*

This appendix contains the manufacturer data sheet for the Am9513A/AmZ8073A System Controller (Advanced Micro Devices, Inc.) integrated circuit. This circuit is used on the NB-MIO-16X.

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Advanced Micro Devices, Inc. 1985 Data Book *MOS Microprocessors and Peripherals.*

Am9513A/AmZ8073A

Am9513A/AmZ8073A

System Timing Controller

DISTINCTIVE CHARACTERISTICS

- Five independent 16-bit counters
- High speed counting rates
- Up/down and binary/BCD counting
- Internal oscillator frequency source
- Tapped frequency scaler
- Programmable frequency output
- 8-bit or 16-bit bus interface
- Time-of-day option
- Alarm comparators on counters 1 and 2
- Complex duty cycle outputs
- One-shot or continuous outputs
- Programmable count/gate source selection
- Programmable input and output polarities
- Programmable gating functions
- Retriggering capability
- +5 volt power supply
- Standard 40-pin package

GENERAL DESCRIPTION

The Am9513A System Timing Controller is an LSI circuit designed to service many types of counting, sequencing and timing applications. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digital one-shots, time-of-day clocking, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watching timing, event count accumulation, waveform analysis, etc. A variety of programmable operating modes and control features allow the Am9513A to be personalized for particular applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-high or active-low input polarity. Both hardware and software gating of each counter is available. Three-state outputs for each counter provide pulses or levels and can be active-high or active-low. The counters can be programmed to count up or down in either binary or BCD. The host processor may read an accumulated count at any time without disturbing the counting process. Any of the counters may be internally concatenated to form any effective counter length up to 80 bits.

The AmZ8073A* is functionally equivalent to the Am9513A with timing enhancements which allow it to be fully speed compatible with the AmZ8001 and AmZ8002 microprocessors.

BLOCK DIAGRAM

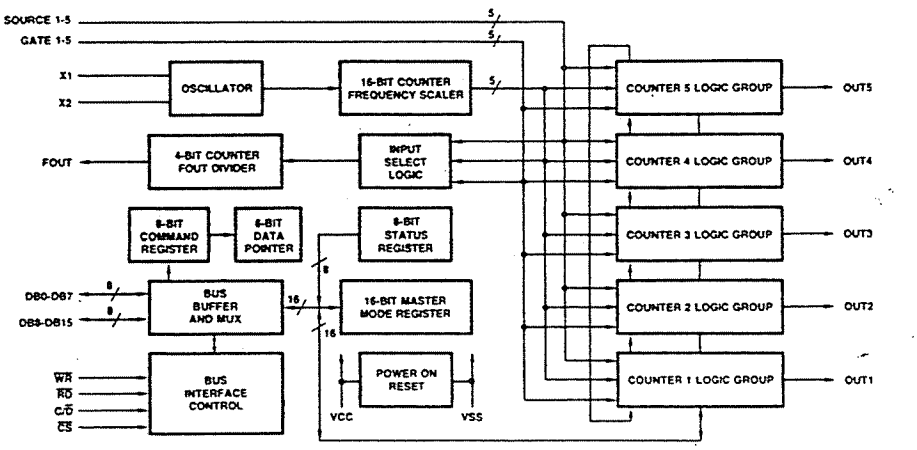
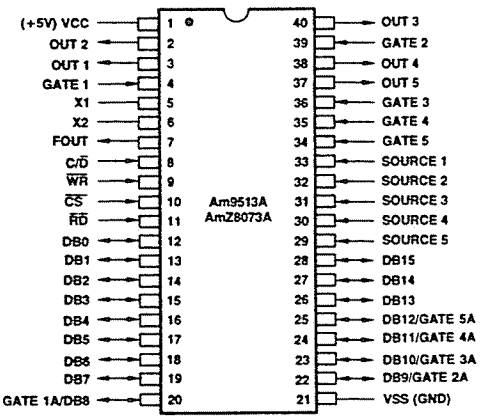


Figure 1-1.

*Z8000 is a trademark of Zilog, Inc.

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CONNECTION DIAGRAM
Top View

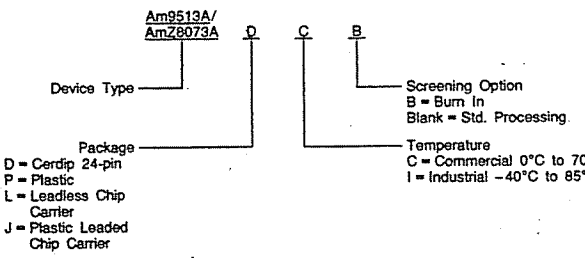


CD005210

Note: Pin 1 is marked for orientation

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am9513A/ AmZ8073A	DC, DCB, DI, DIB, PC, PCB, PI, PIB, LC, LCB, LI, LIB, /BQA

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

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Refer to page 7-1 for Essential Information on Military Devices

Am9513A/AmZ8073A

PIN DESCRIPTION

Pin No.	Name	I/O	Description
1	V_{CC}		+5V Power Supply.
21	V_{SS}		Ground.
5, 6	X1, X2	O, I	(Crystal). X1 and X2 are the connections for an external crystal used to determine the frequency of the internal oscillator. The crystal should be a parallel-resonant, fundamental-mode type. An RC or LC or other reactive network may be used instead of a crystal. For driving from an external frequency source, X1 should be left open and X2 should be connected to a TTL source and a pull-up resistor.
7	FOUT	O	(Frequency Out). The FOUT output is derived from a 4-bit counter that may be programmed to divide its input by any integer value from 1 through 16 inclusive. The input to the counter is selected from any of 15 sources, including the internal scaled oscillator frequencies. FOUT may be gated on and off under software control and when off will exhibit a low impedance to ground. Control over the various FOUT options resides in the Master Mode register. After power-up, FOUT provides a frequency that is 1/16 that of the oscillator. The input source on power-up is F1.
4, 39, 36-34	GATE1 - GATE5	I	(Gate). The Gate inputs may be used to control the operations of individual counters by determining when counting may proceed. The same Gate input may control up to three counters. Gate pins may also be selected as count sources for any of the counters and for the FOUT divider. The active polarity for a selected Gate input is programmed at each counter. Gating function options allow level-sensitive gating or edge-initiated gating. Other gating modes are available including one that allows the Gate input to select between two counter output frequencies. All gating functions may also be disabled. The active Gate input is conditioned by an auxiliary input when the unit is operating with an external 8-bit data bus. See Data Bus description. Schmitt-trigger circuitry on the GATE inputs allows slow transition times to be used.
33-29	SRC1 - SRC5	I	(Source).The Source inputs provide external signals that may be counted by any of the counters. Any Source line may be routed to any or all of the counters and the FOUT divider. The active polarity for a selected SRC input is programmed at each counter. Any duty cycle waveform will be accepted as long as the minimum pulse width is at least half the period of the maximum specified counting frequency for the part. Schmitt-trigger circuitry on the SRC inputs allows slow transition times to be used.
3, 2, 40, 38, 37	OUT1 - OUT5	O	(Counter). Each 3-state OUT signal is directly associated with a corresponding individual counter. Depending on the counter configuration, the OUT signal may be a pulse, a square wave, or a complex duty cycle waveform. OUT pulse polarities are individually programmable. The output circuitry detects the counter state that would have been all bits zero in the absence of a reinitialization. That information is used to generate the selected waveform type. An optional output mode for Counters 1 and 2 overrides the normal output mode and provides a true OUT signal when the counter contents match the contents of an Alarm register.
12-19, 20, 22-28	DB0 - DB7, DB8 - DB15	I/O	(Data Bus). The 16 bidirectional Data Bus lines are used for information exchanges with the host processor. HIGH on a Data Bus line corresponds to one and LOW corresponds to zero. These lines act as inputs when $\overline{WR}$ and $\overline{CS}$ are active and as outputs when $\overline{RD}$ and $\overline{CS}$ are active. When $\overline{CS}$ is inactive, these pins are placed in a high-impedance state. After power-up or reset, the data bus will be configured for 8-bit width and will use only DB0 through DB7. DB0 is the least significant and DB7 is the most significant bit position. The data bus may be reconfigured for 16-bit width by changing a control bit in the Master Mode register. This is accomplished by writing an 8-bit command into the low-order DB lines while holding the DB13 - DB15 lines at a logic high level. Thereafter, all 16 lines can be used, with DB0 as the least significant and DB15 as the most significant bit position. When operating in the 8-bit data bus environment, DB8 - DB15 will never be driven active by the Am9513A. DB8 through DB12 may optionally be used as additional Gate inputs (see Figure 1-3). If unused, they should be held HIGH. When pulled LOW, a GATENA signal will disable the action of the corresponding counter N gating. DB13 - DB15 should be held HIGH in 8-bit bus mode whenever $\overline{CS}$ and $\overline{WR}$ are simultaneously active.
10	$\overline{CS}$	I	(Chip Select). The active-low Chip Select input enables Read and Write operations on the data bus. When Chip Select is HIGH, the Read and Write inputs are ignored. The first Chip Select signal after power-up is used to clear the power-on reset circuitry. If Chip Select is tied to ground permanently, the power-on reset circuitry may not function. In such a configuration, the software reset command must be issued following power-up to reset the Am9513A.
11	$\overline{RD}$	I	(Read). The active-low Read signal is conditioned by Chip Select and indicates that internal information is to be transferred to the data bus. The source will be determined by the port being addressed and, for Data Port reads, by the contents of the Data Pointer register. $\overline{WR}$ and $\overline{RD}$ should be mutually exclusive.
9	$\overline{WR}$	I	(Write). The active-low Write signal is conditioned by Chip Select and indicates that data bus information is to be transferred to an internal location. The destination will be determined by the port being addressed and, for Data Port writes, by the contents of the Data Pointer register. $\overline{WR}$ and $\overline{RD}$ should be mutually exclusive.
8	C/$\overline{D}$	I	(Control/Data). The Control/Data signal selects source and destination locations for Read and Write operations on the data bus. Control Write operations load the Command register and the Data Pointer. Control Read operations output the Status register. Data Read and Data Write transfers communicate with all other internal registers. Indirect addressing at the data port is controlled internally by the Data Pointer register.

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Signal	Abbreviation	Type	Pins
+ 5 Volts	VCC	Power	1
Ground	VSS	Power	1
Crystal	X1, X2	O, I	2
Read	$\overline{RD}$	Input	1
Write	$\overline{WR}$	Input	1
Chip Select	$\overline{CS}$	Input	1
Control/Data	C/$\overline{D}$	Input	1
Source N	SRC	Input	5
Gate N	GATE	Input	5
Data Bus	DB	I/O	16
Frequency Out	FOUT	Output	1
Out N	OUT	Output	5

Figure 1-2. Interface Signal Summary

Figure 1-2 summarizes the interface signals and their abbreviations for the STC.

Package Pin	Data Bus Width (MM14)	
	16 Bits	8 Bits
12	DB0	DB0
13	DB1	DB1
14	DB2	DB2
15	DB3	DB3
16	DB4	DB4
17	DB5	DB5
18	DB6	DB6
19	DB7	DB7
20	DB8	GATE 1A
22	DB9	GATE 2A
23	DB10	GATE 3A
24	DB11	GATE 4A
25	DB12	GATE 5A
26	DB13	(VIH)
27	DB14	(VIH)
28	DB15	(VIH)

Figure 1-3. Data Bus Assignments

Interface Considerations

All of the input and output signals for the Am9513A are specified with logic levels compatible with those of standard TTL circuits. In addition to providing TTL compatible voltage levels, other output conditions are specified to help configure non-standard interface circuitry. The logic level specifications take into account all worst-case combinations of the three variables that affect the logic level thresholds: ambient temperature, supply voltage and processing parameters. A change in any of these toward nominal values will improve the actual operating margins and will increase noise immunity.

Unprotected open gate inputs of high quality MOS transistors exhibit very high resistances on the order of perhaps 10^{14} ohms. It is easy, therefore, in some circumstances, for charge to enter the gate node of such an input faster than it can be discharged and consequently, for the gate voltage to rise high enough to break down the oxides and destroy the transistor. All inputs to the Am9513A include protection networks to help prevent damaging accumulations of static charge. The protection circuitry is designed to slow the transitions of incoming current surges and to provide low-impedance discharge paths for voltages beyond the normal operating levels. Note, however, that input energy levels can nonetheless be too high to be successfully absorbed. Conventional design, storage, and handling precautions should be observed so that the protection networks themselves are not overstressed.

Within the limits of normal operation, the input protection circuitry is inactive and may be modeled as a lumped series RC as shown in Figure 1-4(a). The functionally active input connection during normal operation is the gate of a MOS transistor. No active sources or drains are connected to the inputs so that neither transient nor steady-state currents are impressed on the driving signals other than the charging or discharging of the input capacitance and the accumulated leakage associated with the protection network and the input circuit.

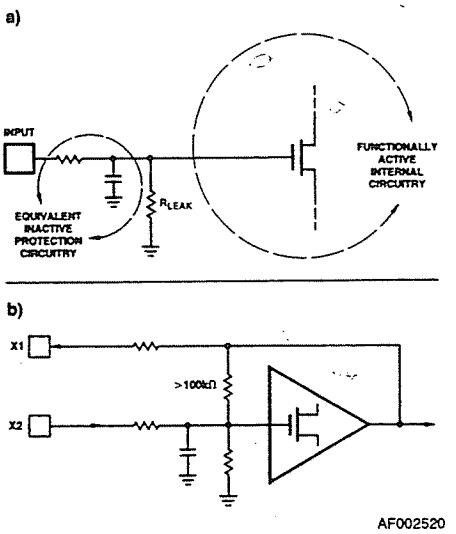


Figure 1-4. Input Circuitry

The only exception to the purely capacitive input case is the X2 crystal input. As shown in Figure 1-4(b) an internal resistor connects X1 and X2 in addition to the protection network. The resistor is a modestly high value of more than 100kohms.

Fanout from the driving circuitry into the Am9513A inputs will generally be limited by transition time considerations rather than DC current limitations when the loading is dominated by conventional MOS circuits. In an operating environment, all inputs should be terminated so they do not float and therefore will not accumulate stray static charges. Unused inputs should be tied directly to Ground or VCC, as appropriate. An input in use will have some type of logic output driving it, and termination during operation will not be a problem. Where inputs are driven from logic external to the card containing this chip, however, on-board termination should be provided to protect the chip when the board is unplugged (the input would otherwise float). A pull-up resistor or a simple inverter or gate will suffice.

DETAILED DESCRIPTION

The Am9513A System Timing Controller (STC) is a support device for processor oriented systems that is designed to enhance the available capability with respect to counting and timing operations. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digital timing functions, time-of-day clocking, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watching timing, event count accumulation, waveform analysis and many more. A variety of programmable operating modes and control features allow the Am9513A to be personalized for particular applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-high or active-low input polarity. Both hardware and software gating of each counter is available. Three-state outputs for each counter provide either pulses or levels. The counters can be programmed to count up or down in either binary or BCD. The accumulated count may be read without disturbing the counting process. Any of the counters may be internally concatenated to form an effective counter length of up to 80 bits.

The Am9513A block diagrams indicate the interface signals and the basic flow of information. Internal control lines and the internal data bus have been omitted. The control and data registers are all connected to a common internal 16-bit bus. The external bus may be 8- or 16-bits wide; in the 8-bit mode, the internal 16-bit information is multiplexed to the low order data bus pins DB0 through DB7.

An internal oscillator provides a convenient source of frequencies for use as counter inputs. The oscillator's frequency is controlled at the X1 and X2 interface pins by an external reactive network such as a crystal. The oscillator output is divided by the Frequency Scaler to provide several sub-frequencies. One of the scaled frequencies (or one of ten input signals) may be selected as an input to the FOUT divider and then comes out of the chip at the FOUT interface pin.

The STC is addressed by the external system as two locations: a Control port and a Data port. The Control port provides direct access to the Status and Command registers, as well as allowing the user to update the Data Pointer register. The Data port is used to communicate with all other addressable internal locations. The Data Pointer register controls the Data port addressing.

Among the registers accessible through the Data port are the Master Mode register and five Counter Mode registers, one for each counter. The Master Mode register controls the programmable options that are not controlled by the Counter Mode registers.

Each of the five general-purpose counters is 16-bits long and is independently controlled by its Counter Mode register. Through this register, a user can software select one of 16 sources as the counter input, a variety of gating and repetition modes, up or down counting in binary or BCD and active-high or active-low input and output polarities.

Associated with each counter are a Load register and a Hold register, both accessible through the Data port. The Load register is used to automatically reload the counter to any predefined value, thus controlling the effective count period. The Hold register is used to save count values without disturbing the count process, permitting the host processor to read intermediate counts. In addition, the Hold register may be used as a second Load register to generate a number of complex output waveforms.

All five counters have the same basic control logic and control registers. Counters 1 and 2 have additional Alarm registers and comparators associated with them, plus the extra logic necessary for operating in a 24-hour time-of-day mode. For real-time operation, the time-of-day logic will accept 50Hz, 60Hz or 100Hz input frequencies.

Each general counter has a single dedicated output pin. It may be turned off when the output is not of interest or may be configured in a variety of ways to drive interrupt controllers, Darlington buffers, bus drivers, etc. The counter inputs, on the other hand, are specifically not dedicated to any given interface line. Considerable versatility is available for configuring both the input and the gating of individual counters. This not only permits dynamic reassignment of inputs under software control, but also allows multiple counters to use a single input and a single gate pin to control more than one counter. Indeed, a single pin can be the gate for one counter and, at the same time, the count source for another.

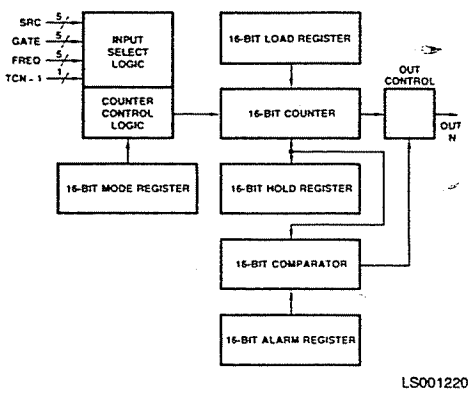


Figure 1-5. Counter Logic Groups 1 and 2

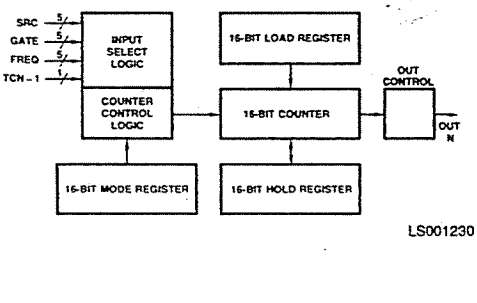


Figure 1-6. Counter Logic Groups 3, 4 and 5

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Refer to page 7-1 for Essential Information on Military Devices

A powerful command structure simplifies user interaction with the counters. A counter must be armed by one of the ARM commands before counting can commence. Once armed, the counting process may be further enabled or disabled using the hardware gating facilities. The ARM and DISARM commands permit software gating of the count process in some modes.

The LOAD command causes the counter to be reloaded with the value in either the associated Load register or the associated Hold register. It will often be used as a software retrigger or as counter initialization prior to active hardware gating.

The DISARM command disables further counting independent of any hardware gating. A disarmed counter may be reloaded using the LOAD command, may be incremented or decremented using the STEP command and may be read using the SAVE command. A count process may be resumed using an ARM command.

The SAVE command transfers the contents of a counter to its associated Hold register. This command will overwrite any previous Hold register contents. The SAVE command is designed to allow an accumulated count to be preserved so that it can be read by the host CPU at some later time.

Two combinations of the basic commands exist to either LOAD AND ARM or to DISARM AND SAVE any combination of counters. Additional commands are provided to: step an individual counter by one count; set and clear an output toggle; issue a software reset; clear and set special bits in the Master Mode register; and load the Data Pointer register.

Note: Separate LOAD and ARM commands should be used for asynchronous operations.

Power Supply

The Am9513A requires only a single 5V power supply. Maximum supply currents are specified in the electrical specification at the high end of the voltage tolerance and the low end of the temperature range. In addition, the current specifications take into account the worstcase distribution of processing parameters that may be encountered during the manufacturing life of the product. Typical supply current values, on the other hand, are specified at a nominal +5.0 volts, a nominal ambient temperature of 25°C, and nominal processing parameters. Supply current always decreases with increasing ambient temperature: thermal run-away is not a problem.

Supply current will vary somewhat from part to part, but a given unit at a given operating temperature will exhibit a nearly constant power drain. There is no functional operating region that will cause more than a few percent change in the supply current. Decoupling of VCC, then, is straightforward and will generally be used to isolate the Am9513A from VCC noise originating externally

CONTROL PORT REGISTERS

The STC is addressed by the external system as only two locations: a Control port and a Data port. Transfers at the Control port (C/$\overline{D}$ = HIGH) allow direct access to the Command register when writing and the Status register when reading. All other available internal locations are accessed for both reading and writing via the Data port (C/$\overline{D}$ = LOW). Data port transfers are executed to and from the location currently addressed by the Data Pointer register. Options available in the Master Mode register and the Data Pointer control structure allow several types of transfer sequencing to be used. See Figure 1-7.

Transfers to and from the Control port are always 8-bits wide. Each access to the Control port will transfer data between the Command register (writes) or Status register (reads) and Data Bus pins DB0-DB7, regardless of whether the Am9513A is in 8- or 16-bit bus mode. When the Am9513A is in 8-bus mode, Data Bus pins DB13-DB15 should be held at a logic high whenever $\overline{CS}$ and WR are both active.

Command Register

The Command register provides direct control over each of the five general counters and controls access through the Data port by allowing the user to update the Data Pointer register. The "Command Description" section of this data sheet explains the detailed operation of each command. A summary of all commands appears in Figure 1-20. Six of the command types are used for direct software control of the counting process. Each of these six commands contains a 5-bit S field. In a linear-select fashion, each bit in the S field corresponds to one of the five general counters (S1 = Counter 1, S2 = Counter 2, etc.). When an S bit is a one, the specified operation is performed on the counter so designated; when an S bit is a zero, no operation occurs for the corresponding counter.

Data Pointer Register

The 6-bit Data Pointer register is loaded by issuing the appropriate command through the Control port to the Command register. As shown in Figure 1-7, the contents of the Data Pointer register are used to control the Data port multiplexer, selecting which internal register is to be accessible through the Data port.

The Data Pointer consists of a 3-bit Group Pointer, a 2-bit Element Pointer and a 1-bit Byte Pointer, depicted in Figure 1-8. The Byte Pointer bit indicates which byte of a 16-bit register is to be transferred on the next access through the Data port. Whenever the Data Pointer is loaded, the Byte Pointer bit is set to one, indicating a least-significant byte is expected. The Byte Pointer toggles following each 8-bit data transfer with an 8-bit data bus (MM13 = 0), or it always remains set with the 16-bit data bus option (MM13 = 1). The Element and Group pointers are used to select which internal register is to be accessible through the Data port. Although the contents of the Element and Group Pointer in the Data Pointer register cannot be read by the host processor, the Byte Pointer is available as a bit in the Status register.

Random access to any available internal data location can be accomplished by simply loading the Data Pointer using the command shown in Figure 1-9 and then initiating a data read or data write. This procedure can be used at any time, regardless of the setting of the Data Pointer Control bit (MM14). When the 8-bit data bus configuration is being used (MM13 = 0), two bytes of data would normally be transferred following the issuing of the "Load Data Pointer" command.

To permit the host processor to rapidly access the various internal registers, automatic sequencing of the Data Pointer is provided.

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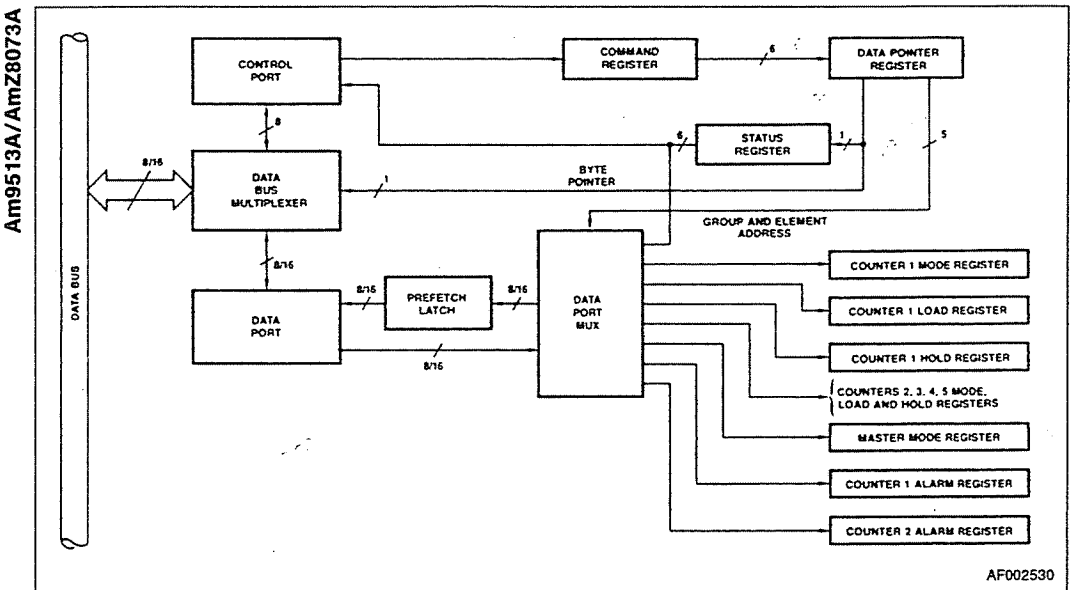


Figure 1-7. Am9513A Register Access

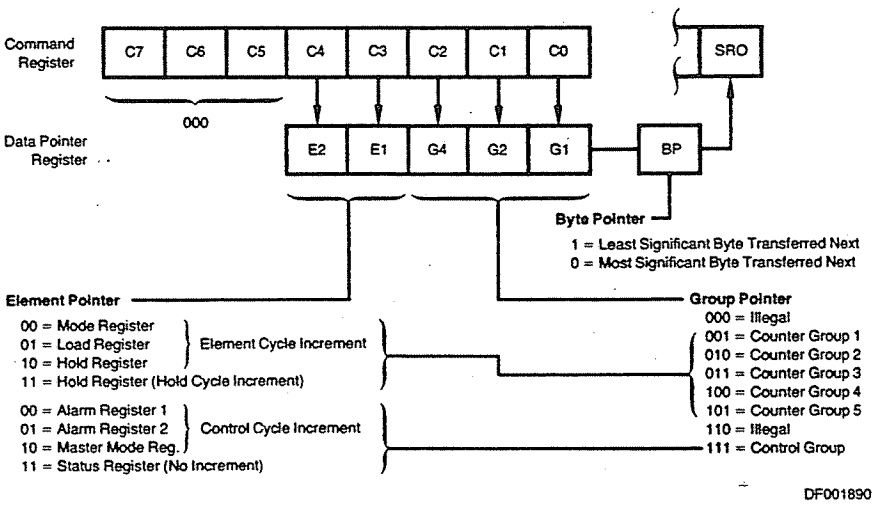


Figure 1-8. Data Pointer Register

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	Element Cycle			Hold Cycle
	Mode Register	Load Register	Hold Register	Hold Register
Counter 1	FF01	FF09	FF11	FF19
Counter 2	FF02	FF0A	FF12	FF1A
Counter 3	FF03	FF0B	FF13	FF1B
Counter 4	FF04	FF0C	FF14	FF1C
Counter 5	FF05	FF0D	FF15	FF1D
Master Mode Register = FF17 Alarm 1 Register = FF07 Alarm 2 Register = FF0F Status Register = FF1F				

Notes:
1. All codes are in hex.
2. When used with an 8-bit bus, only the two low order hex digits should be written to the command port; the 'FF' prefix should be used only for a 16-bit data bus interface.

Figure 1-9. Load Data Pointer Commands

Sequencing is enabled by clearing Master Mode bit 14 (MM14) to zero. As shown in Figure 1-10 several types of sequencing are available depending on the data bus width being used and the initial Data Pointer value entered by command.

When E1 = 0 or E2 = 0 and G4, G2, G1 points to a Counter Group, the Data Pointer will proceed through the Element cycle. The Element field will automatically sequence through the three values 00, 01 and 10 starting with the value entered. When the transition from 10 to 00 occurs, the Group field will also be incremented by one. Note that the Element field in this case does not sequence to a value of 11. The Group field circulates only within the five Counter Group codes.

If E2, E1 = 11 and a Counter Group are selected, then only the Group field is sequenced. This is the Hold cycle. It allows the Hold registers to be sequentially accessed while bypassing the Mode and Load registers. The third type of sequencing is the Control cycle. If G4, G2, G1 = 111 and E2, E1 ≠ 11, the Element Pointer will be incremented through the values 00, 01 and 10, with no change to the Group Pointer.

When G4, G2, G1 = 111 and E2, E1 = 11, no incrementing takes place and only the Status register will be available through the Data port. Note that the Status register can also always be read directly through the Control port.

For all these auto-sequencing modes, if an 8-bit data bus is used, the Byte pointer will toggle after every data transfer to allow the least and most significant bytes to be transferred before the Element or Group fields are incremented.

Prefetch Circuit

To minimize the read access time to internal Am9513A registers, a prefetch circuit is used for all read operations through the Data port. Following each read or write operation through the Data port, the Data Pointer register is updated to point to the next register to be accessed. Immediately following this update, the new register data is transferred to a special prefetch latch at the interface pad logic. When the user performs a subsequent read of the Data port, the data bus drivers are enabled, outputting the prefetched data on the bus. Since the internal data register is accessed prior to the start of the read operation, its access time is transparent to the user. To keep the prefetched data consistent with the Data Pointer, prefetches are also performed after each write to the Data port and after execution of the "Load Data Pointer" command. The following rules should be kept in mind regarding Data port Transfers.

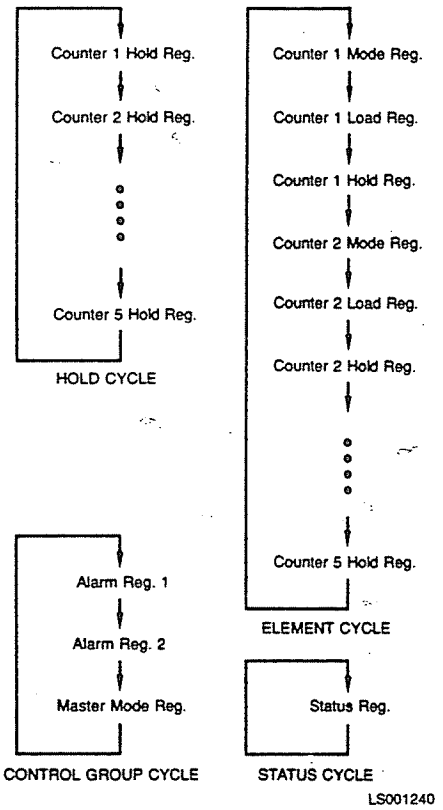


Figure 1-10. Data Pointer Sequencing

1. The Data Pointer register should always be reloaded before reading from the Data port if a command, other than "Load Data Pointer," was issued to the Am9513A following the last Data port read or write. The Data Pointer does not have to be loaded again if the first Data port transaction after a command entry is a write, since the Data port write will automatically cause a new prefetch to occur.

2. Operating modes N, O, Q, R and X allow the user to save the counter contents in the Hold register by applying an active-going gate edge. If the Data Pointer register had been pointing to the Hold register in question, the prefetched value will not correspond to the new value saved in the Hold Register. To avoid reading an incorrect value, a new "Load Data Pointer" command should be issued before attempting to read the saved data. A Data port write (to another register) will also initiate a prefetch; subsequent reads will access the recently saved Hold register data. Many systems will use the "saving" gate edge to interrupt the host CPU. In systems such as this, the interrupt service routine should issue a "Load Data Pointer" command prior to reading the saved data.

Status Register

The 8-bit read-only Status register indicates the state of the Byte Pointer bit in the Data Pointer register and the state of the OUT signal for each of the general counters. See Figures 1-11 and 1-18. The OUT signals reported are those internal to the

chip after the polarity-select logic and just before the 3-state interface buffer circuitry. Bits SR6 and SR7 may be 0 or 1.

The Status register OUT bit reflects an active-high or active-low TC output, or a TC Toggled output, as programmed in the Output Control Field of the Counter Mode register. That is, it reflects the exact state of the OUT pin. When the low-impedance to Ground Output option (CM2-CM0 = 000) is selected, the Status register will reflect an active-high TC Output. When a high-impedance Output option (CM2-CM0 = 100) is selected, the Status register will reflect an active-low TC output.

For Counters 1 and 2, the OUT pin will reflect the comparator output if the comparators are enabled. The Status register bit and OUT pin are active-high if CM2 = 0 and active-low if CM2 = 1. When the high-impedance option is selected and the comparator is enabled, the status register bit will reflect an active-high comparator output. When the low-impedance to Ground option is selected and the comparator is enabled, the status register bit will reflect an active-low comparator output.

The Status register is normally accessed by reading the Control port (see Figure 1-7) but may also be read via the Data port as part of the Control Group.

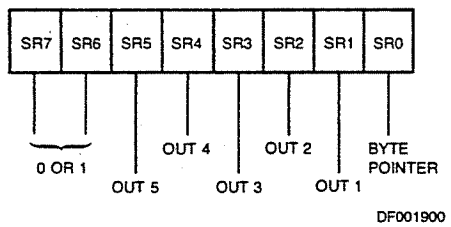


Figure 1-11. Status Register Bit Assignments

DATA PORT REGISTERS

Counter Logic Groups

As shown in Figures 1-5 and 1-6, each of the five Counter Logic Groups consists of a 16-bit general counter with associated control and output logic, a 16-bit Load register, a 16-bit Hold register and a 16-bit Mode register. In addition, Counter Groups 1 and 2 also include 16-bit Comparators and 16-bit Alarm registers. The comparator/alarm functions are controlled by the Master Mode register. The operation of the Counter Mode registers is the same for all five counters. The host CPU has both read and write access to all registers in the Counter Logic Groups through the Data port. The counter itself is never directly accessed.

Load Register

The 16-bit read/write Load register is used to control the effective length of the general counter. Any 16-bit value may be written into the Load register. That value can then be transferred into the counter each time the Terminal Count (TC) occurs. "Terminal Count" is defined as that period of time when the counter contents would have been zero if an external value had not been transferred into the counter. Thus, the terminal count frequency can be the input frequency divided by the value in the Load register. In all operating modes, either the Load or Hold register will be transferred into the counter when TC occurs. In cases where values are being accumulated in the counter, the Load register action can become transparent by filling the Load register with all zeros.

Hold Register

The 16-bit read/write Hold register is dual-purpose. It can be used in the same way as the Load register, thus offering an alternate source for module definition for the counter. The Hold register may also be used to store accumulated counter values for later transfer to the host processor. This allows the count to be sampled while the counting process proceeds without interruption. Transfer of the counter contents into the Hold register is accomplished by the hardware interface in some operating modes or by software commands at any time.

Counter Mode Register

The 16-bit read/write Counter Mode register controls the gating, counting, output and source select functions within each Counter Logic Group. The "Counter Mode Control Options" section of this document describes the detailed control options available. Figure 1-17 shows the bit assignments for the Counter Mode registers.

Alarm Registers and Comparators

Added functions are available in the Counter Logic Groups for Counters 1 and 2 (see Figure 1-5). Each contains a 16-bit Alarm register and a 16-bit Comparator. When the value in the counter reaches the value in the Alarm register, the Comparator output will go true. The Master Mode register contains control bits to individually enable/disable the comparators. When enabled, the comparator output appears on the OUT pin of the associated counter in place of the normal counter output. The output will remain true as long as the comparison is true, that is, until the next input causes the count to change. The polarity of the Comparator output will be active-high if the Output Control field of the Counter Mode register is 001 or 010 and active-low if the Output Control field is 101.

MASTER MODE CONTROL OPTIONS

The 16-bit Master Mode (MM) register is used to control those internal activities that are not controlled by the individual Counter Mode registers. This includes frequency control, Time-of-Day operation, comparator controls, data bus width and data pointer sequencing. Figure 1-12 shows the bit assignments for the Master Mode register. This section describes the use of each control field.

Master Mode register bits MM12, MM13 and MM14 can be individually set and reset using commands issued to the Command register. In addition, they can all be changed by writing directly to the Master Mode register.

After power-on reset or a Master Reset command, the Master Mode register is cleared to an all zero condition. This results in the following configuration:

Time-of-Day disabled
Both Comparators disabled
FOUT Source is frequency F1
FOUT Divider set for divide-by-16
FOUT gated on
Data Bus 8 bits wide
Data Pointer Sequencing enabled
Frequency Scaler divides in binary

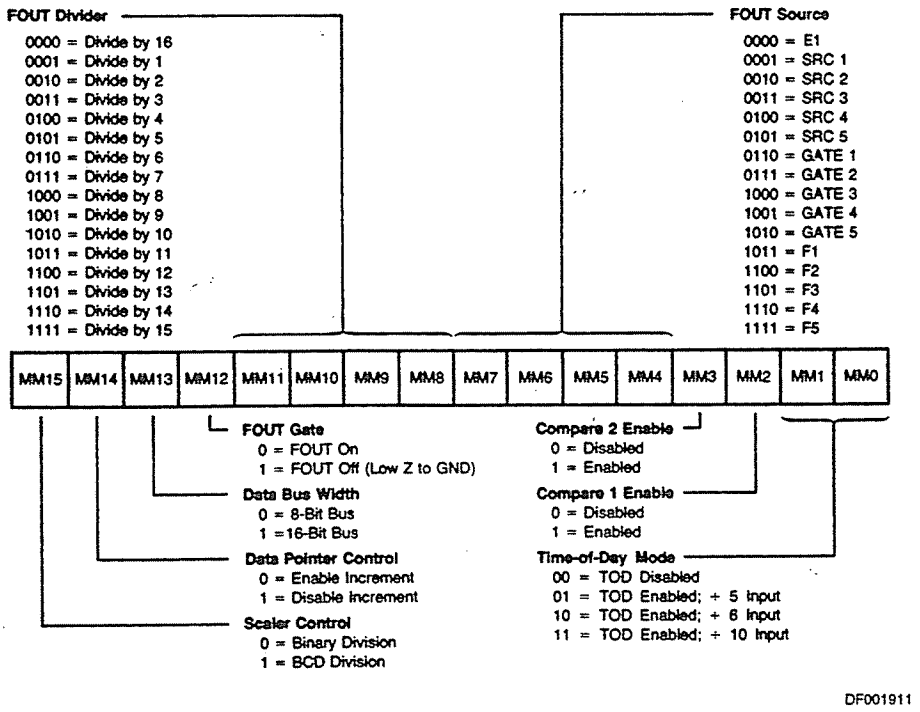


Figure 1-12. Master Mode Register Bit Assignments

Time-of-Day

Bits MM0 and MM1 of the Master Mode register specify the Time-of-Day (TOD) options. When MM0 = 0 and MM1 = 0, the special logic used to implement TOD is disabled, and Counters 1 and 2 will operate in exactly the same way as Counters 3, 4 and 5. When MM0 = 1 or MM1 = 1, additional counter decoding and control logic is enabled on Counters 1 and 2, which causes their decades to turn over at the counts that generate appropriate 24-hour TOD accumulations. For additional information, see the Time-of-Day chapter in the 9513A System timing controller technical manual.

Comparator Enable

Bits MM2 and MM3 control the Comparators associated with Counters 1 and 2. When a Comparator is enabled, its output is substituted for the normal counter output on the associated OUT1 or OUT2 pin. The comparator output will be active-high if the output control field of the Counter Mode register is 001 or 010 and active-low for a code of 101. Once the compare output is true, it will remain so until the count changes and the comparison therefore goes false.

The two Comparators can always be used individually in any operating mode. One special case occurs when the Time-of-Day option is revoked and both Comparators are enabled. The operation of Comparator 2 will then be conditioned by Comparator 1 so that a full 32-bit compare must be true in order to generate a true signal on OUT2. OUT1 will continue, as usual, to reflect the state of the 16-bit comparison between Alarm 1 and Counter 1.

FOUT Source

Master Mode bits MM4 through MM7 specify the source input for the FOUT divider. Fifteen inputs are available for selection, and they include the five Source pins, the five Gate pins and the five internal frequencies derived from the oscillator. The 16th combination of the four control bits (all zeros) is used to assure that an active frequency is available at the input to the FOUT divider following reset.

FOUT Divider

Bits MM8 through MM11 specify the dividing ratio for the FOUT Divider. The FOUT source (selected by bits MM4 through MM7) is divided by an integer value between 1 and 16, inclusive, and is then passed to the FOUT output buffer. After power-on or reset, the FOUT divider is set to divide-by-16.

FOUT Gate

Master Mode bit MM12 provides a software gating capability for the FOUT signal. When MM12 = 1, FOUT is off and in a low-impedance state to ground. MM12 may be set or cleared in conjunction with the loading of the other bits in the Master Mode register; alternatively, there are commands that allow MM12 to be individually set or cleared directly without changing any other Master Mode bits. After power-up or reset, FOUT is gated on.

When changing the FOUT divider ratio or FOUT source, transient pulses as short as half the period of the FOUT source may appear on the FOUT pin. Turning the FOUT gate on or off can also generate a transient. This should be considered when using FOUT as a system clock source.

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Bus Width

Bit MM13 controls the multiplexer at the data bus interface in order to configure the part for an 8-bit or 16-bit external bus. The internal bus is always 16-bits wide. When MM13 = 1, 16-bit data is transferred directly between the internal bus and all 16 of the external bus lines. In this configuration, the Byte Pointer bit in the Data Pointer register remains set at all times. When MM13 = 0, 16-bit internal data is transferred a byte at a time to and from the eight low-order external data bus lines. The Byte Pointer bit toggles with each byte transfer in this mode.

When the Am9513A is set to operate with an 8-bit data bus width, pins DB8 through DB15 are not used for the data bus and are available for other functions. Pins DB13 through DB15 should be tied high. Pins DB8 through DB12 are used as auxiliary gating inputs and are labeled GATE1A through GATE5A respectively. The auxiliary gate pin, GATENA, is logically ANDed with the gate input to Counter N, as shown in Figure 1-13. The output of the AND gate is then used as the gating signal for Counter N.

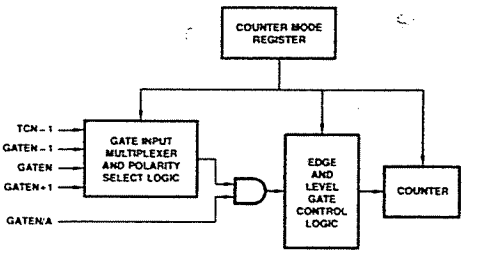


Figure 1-13. Gating Control

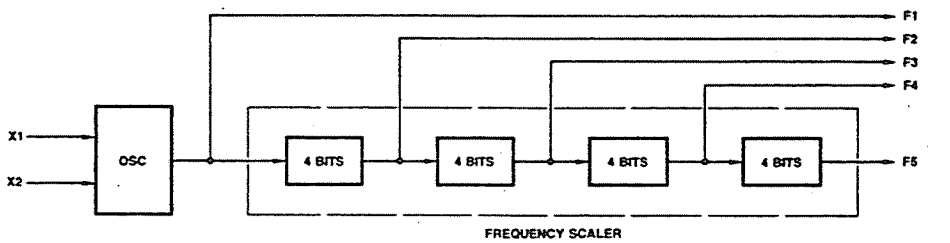
Data Pointer Sequencing

Bit MM14 controls the Data Pointer logic to enable or disable the automatic sequencing functions. When MM14 = 1, the contents of the Data Pointer can be changed only directly by entering a command. When MM14 = 0, several types of automatic sequencing of the Data Pointer are available. These are described in the Data Pointer register section of this document.

Thus, the host processor, by controlling MM14, may repetitively read/write a single internal location, or may sequentially read/write groups of locations. Bit MM14 can be loaded by writing to the Master Mode register or can be set or cleared by software command.

Scaler Ratios

Master Mode bit MM15 controls the counting configuration of the Frequency Scaler counter. When MM15 = 0, the Scaler divides the oscillator frequency in binary steps so that each subfrequency is 1/16 of the preceding frequency. When MM15 = 1, the Scaler divides in BCD steps so that adjacent frequencies are related by ratios of 10 instead of 16 (see Figure 1-14).



Frequency	BCD Scaling MM15 = 1	Binary Scaling MM15 = 0
F1	OSC	OSC
F2	F1 ÷ 10	F1 ÷ 16
F3	F1 ÷ 100	F1 ÷ 256
F4	F1 ÷ 1,000	F1 ÷ 4,096
F5	F1 ÷ 10,000	F1 ÷ 65,536

Figure 1-14. Frequency Scaler Ratios

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Counter Mode	A	B	C	D	E	F	G	H	I	J	K	L
Special Gate (CM7)	0	0	0	0	0	0	0	0	0	0	0	0
Reload Source (CM6)	0	0	0	0	0	0	1	1	1	1	1	1
Repetition (CM5)	0	0	0	1	1	1	0	0	0	1	1	1
Gate Control (CM15-CM13)	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE
Count to TC once, then disarm	X	X	X									
Count to TC twice, then disarm							X	X	X			
Count to TC repeatedly without disarming				X	X	X				X	X	X
Gate input does not gate counter input	X			X			X			X		
Count only during active gate level		X			X			X			X	
Start count on active gate edge and stop count on next TC			X			X						
Start count on active gate edge and stop count on second TC									X			X
No hardware retriggering	X	X	X	X	X	X	X	X	X	X	X	X
Reload counter from Load register on TC	X	X	X	X	X	X						
Reload counter on each TC, alternating reload source between Load and Hold registers							X	X	X	X	X	X
Transfer Load register into counter on each TC that gate is LOW, transfer Hold register into counter on each TC that gate is HIGH.												
On active gate edge transfer counter into Hold register and then reload counter from Load register												

Counter Mode	M	N	O	P	Q	R	S	T	U	V	W	X
Special Gate (CM7)	1	1	1	1	1	1	1	1	1	1	1	1
Reload Source (CM6)	0	0	0	0	0	0	1	1	1	1	1	1
Repetition (CM5)	0	0	0	1	1	1	0	0	0	1	1	1
Gate Control (CM15-CM13)	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE
Count to TC once, then disarm		X	X									
Count to TC twice, then disarm							X					
Count to TC repeatedly without disarming					X	X				X		X
Gate input does not gate counter input							X			X		
Count only during active gate level		X			X							
Start count on active gate edge and stop count on next TC			X			X						X
Start count on active gate edge and stop count on second TC												
No hardware retriggering							X			X		X
Reload counter from Load register on TC		X	X		X	X						X
[1]Reload counter on each TC, alternating reload source between Load and Hold registers.												
Transfer Load register into counter on each TC that gate is LOW, transfer Hold register into counter on each TC that gate is HIGH.							X			X		
On active gate edge transfer counter into Hold register and then reload counter from Load register		X	X		X	X						
On active gate edge transfer counter into Hold register, but counting continues												X

Notes: 1. Counter modes M, P, T, U and W are reserved and should not be used.
2. Mode X is available for Am9513A only.

Figure 1-15 Counter Mode Operating Summary

COUNTER MODE DESCRIPTIONS

Counter Mode register bits CM15-CM13 and CM7-CM5 select the operating mode for each counter (see Figure 1-15). To simplify references to a particular mode, each mode is assigned a letter from A through X. Representative waveforms for the counter modes are illustrated in Figures 1-16a through 1-16v. (Because the letter suffix in the figure number is keyed to the mode, Figures 1-16m, 1-16p, 1-16t, 1-16u and 1-16w do not exist.) The figures assume down counting on rising source edges. Those modes which automatically disarm the counter (CM5 = 0) are shown with the $\overline{WR}$ plus entering the required ARM command; for modes which count repetitively (CM5 = 1), the ARM command is omitted. The retriggering modes (N, O, Q and R) are shown with one retrigger operation. Both a TC output waveform and a TC Toggled output waveform are shown for each mode. The symbols L and H are used to represent count values equal to the Load and Hold register contents, respectively. The symbols K and N represent arbitrary count values. For each mode, the required bit pattern in the Counter Mode register is shown; "don't care" bits are marked "X." These figures are designed to clarify the mode descriptions; the Am9513A Electrical Specification should be used as the authoritative reference for timing relationships between signals.

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To keep the following mode descriptions concise and to the point, the phrase "source edges" is used to refer to active-going source edges only, not to inactive-going edges. Similarly, the phrase "gate edges" refers only to active-going gate edges. Also, again to avoid verbosity and euphuism, the descriptions of some modes state that a counter is stopped or disarmed "on a TC, inhibiting further counting." As is fully explained in the TC section of this document, for these modes the counter is actually stopped or disarmed following the active-going source edge which drives the counter out of TC. In other words, since a counter in the TC state always counts, irrespective of its gating or arming status, the stopping or disarming of the count sequence is delayed until TC is terminated.

MODE A

Software-Triggered Strobe with No Hardware Gating

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
0	0	0	X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	0	0	X	X	X	X	X

Mode A, shown in Figure 1-16a, is one of the simplest operating modes. The counter will be available for counting source edges when it is issued an ARM command. On each TC, the counter will reload from the Load register and automatically disarm itself, inhibiting further counting. Counting will resume when a new ARM command is issued.

MODE B

Software-Triggered Strobe with Level Gating

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
LEVEL			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	0	0	X	X	X	X	X

Mode B, shown in Figure 1-16b, is identical to Mode A except that source edges are counted only when the assigned Gate is active. The counter must be armed before counting can occur. Once armed, the counter will count all source edges which occur while the Gate is active and disregard those edges which occur while the Gate is inactive. This permits the Gate to turn the count process on and off. On each TC the counter will reload from the Load register and automatically disarm itself, inhibiting further counting until a new ARM command is issued.

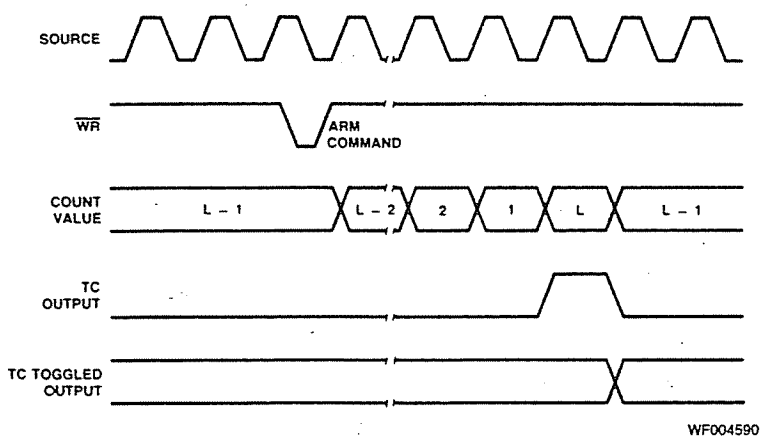


Figure 1-16a. Mode A Waveforms

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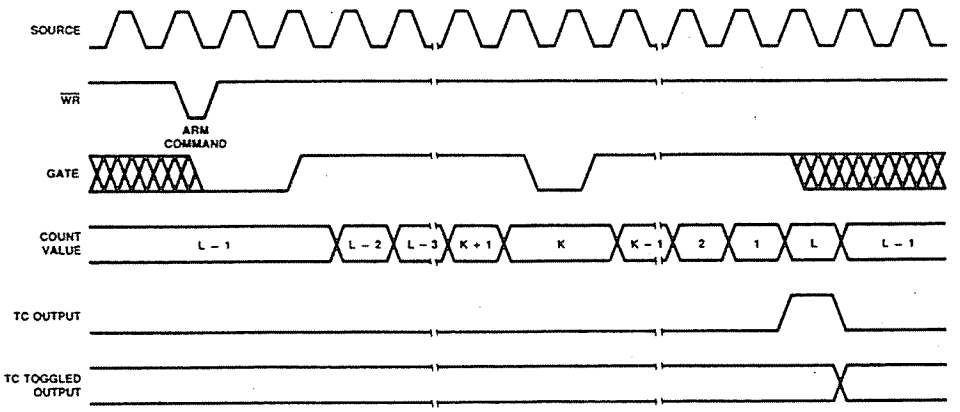


Figure 1-16b. Mode B Waveforms

MODE C

Hardware-Triggered Strobe

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
EDGE			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	0	0	X	X	X	X	X

Mode C, shown in Figure 1-16c, is identical to Mode A, except that counting will not begin until a Gate edge is applied to the armed counter. The counter must be armed before application of the triggered Gate edge; Gate edges applied to a disarmed counter are disregarded. The counter will start counting on the first source edge after the triggering Gate edge and will continue counting until TC. At TC, the counter will reload from the Load register and automatically disarm itself. Counting will then remain inhibited until a new ARM command and a new Gate edge are applied in that order. Note that after application of a triggered Gate edge, the Gate input will be disregarded for the remainder of the count cycle. This differs from Mode B, where the Gate can be modulated throughout the count cycle to stop and start the counter.

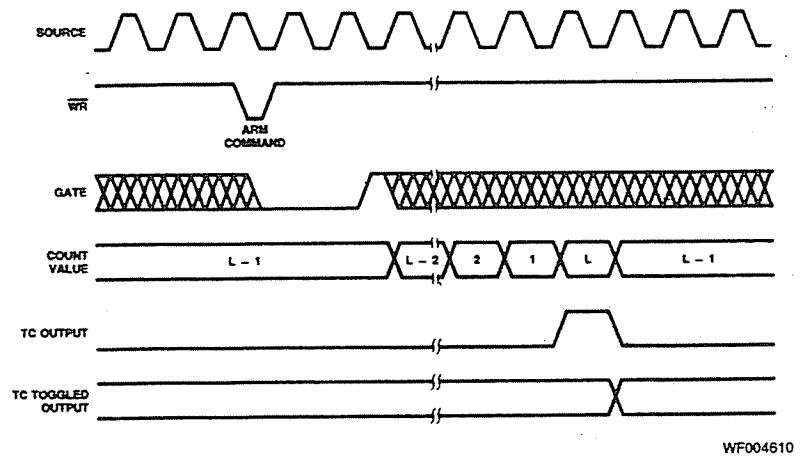


Figure 1-16c. Mode C Waveforms

MODE D

Rate Generator with No Hardware Gating

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
0	0	0	X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	0	1	X	X	X	X	X

Mode D, shown in Figure 1-16d, is typically used in frequency generation applications. In this mode, the Gate input does not affect counter operation. Once armed, the counter will count to TC repetitively. On each TC, the counter will reload itself from the Load register; hence, the Load register value determines the time between TCs. A square wave rate generator may be obtained by specifying the TC Toggled output mode in the Counter Mode register.

MODE E

Rate Generator with Level Gating

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
LEVEL			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	0	1	X	X	X	X	X

Mode E, shown in Figure 1-16e, is identical to Mode D, except the counter will only count those source edges which occur while the Gate input is active. This feature allows the counting process to be enabled and disabled under hardware control. A square wave rate generator may be obtained by specifying the TC Toggled output mode.

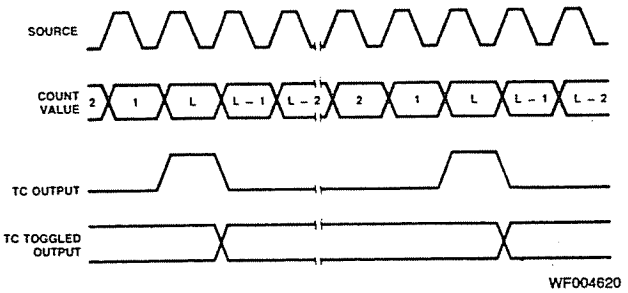


Figure 1-16d. Mode D Waveforms

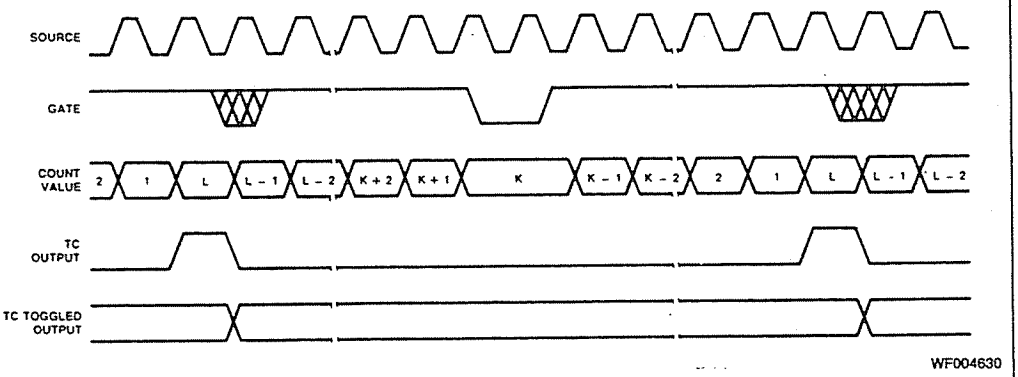


Figure 1-16e. Mode E Waveforms

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MODE F

Non-Retriggerable One-Shot

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
EDGE			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	0	1	X	X	X	X	X

Mode F, shown in Figure 1-16f, provides a non-retriggerable one-shot timing function. The counter must be armed before it will function. Application of a Gate edge to the armed counter will enable counting. When the counter reaches TC, it will reload itself from the Load register. The counter will then stop counting, awaiting a new Gate edge. Note that unlike Mode C, a new ARM command is not needed after TC, only a new Gate edge. After application of a triggering Gate edge, the Gate input is disregarded until TC.

MODE G

Software-Triggered Delayed Pulse One-Shot

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
0	0	0	X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	1	0	X	X	X	X	X

In Mode G, the Gate does not affect the counter's operation. Once armed, the counter will count to TC twice and then automatically disarm itself. For most applications, the counter will initially be loaded from the Load register either by a LOAD command or by the last TC of an earlier timing cycle. Upon counting to the first TC, the counter will reload itself from the Hold register. Counting will proceed until the second TC, when the counter will reload itself from the Load register and automatically disarm itself, inhibiting further counting. Counting can be resumed by issuing a new ARM command. A software-triggered delayed pulse one-shot may be generated by specifying the TC Toggled output mode in the Counter Mode register. The initial counter contents control the delay from the ARM command until the output pulse starts. The Hold register contents control the pulse duration. Mode G is shown in Figure 1-16g.

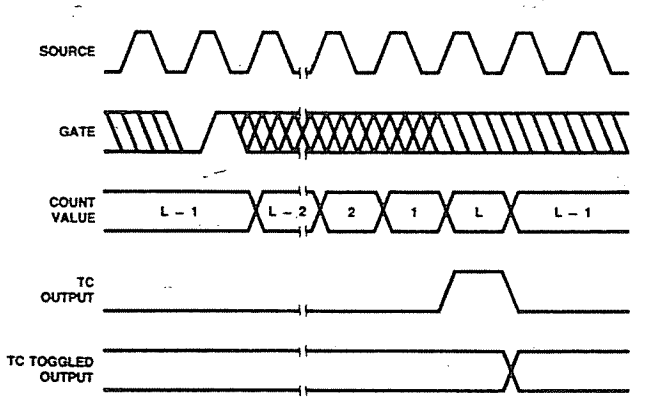


Figure 1-16f. Mode F Waveforms

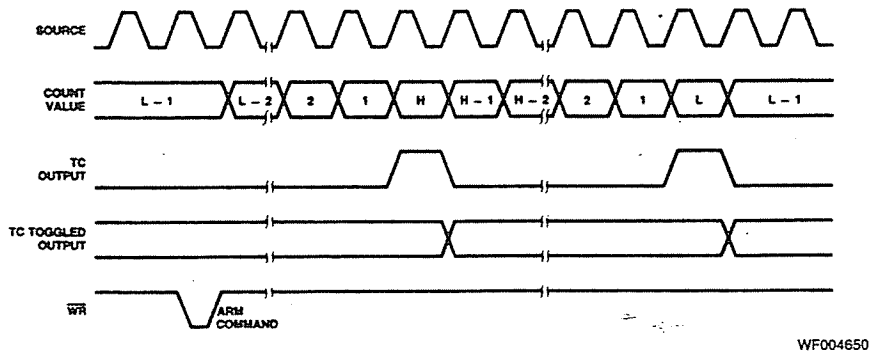


Figure 1-16g. Mode G Waveforms

MODE H

Software-Triggered Delayed Pulse One-Shot with Hardware Gating

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
LEVEL			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	1	0	X	X	X	X	X

Mode H, shown in Figure 1-16h, is identical to Mode G except that the Gate input is used to qualify which source edges are to be counted. The counter must be armed for counting to occur. Once armed, the counter will count all source edges that occur while the Gate is inactive. This permits the Gate to turn the count process on and off. As with Mode G, the counter will be reloaded from the Hold register on the first TC and reloaded from the Load register and disarmed on the second TC. This mode allows the Gate to control the extension of both the initial output delay time and the pulse width.

MODE I

Hardware-Triggered Delayed Pulse Strobe

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
EDGE			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	1	0	X	X	X	X	X

Mode I, shown in Figure 1-16i, is identical to Mode G, except that counting will not begin until a Gate edge is applied to an armed counter. The counter must be armed before application of the triggering Gate edge; Gate edges applied to a disarmed counter are disregarded. An armed counter will start counting on the first source edge after the triggering Gate edge. Counting will then proceed in the same manner as in Mode G. After the second TC, the counter will disarm itself. An ARM command and Gate edge must be issued in this order to restart counting. Note that after application of a triggering Gate edge, the Gate input will be disregarded until the second TC. This differs from Mode H, where the Gate can be modulated throughout the count cycle to stop and start the counter.

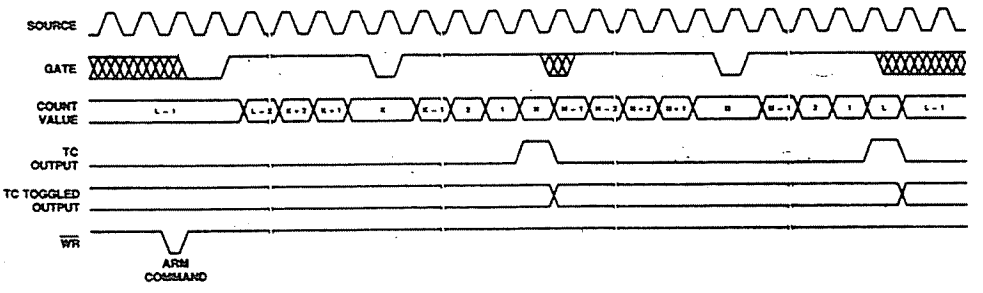


Figure 1-16h. Mode H Waveforms

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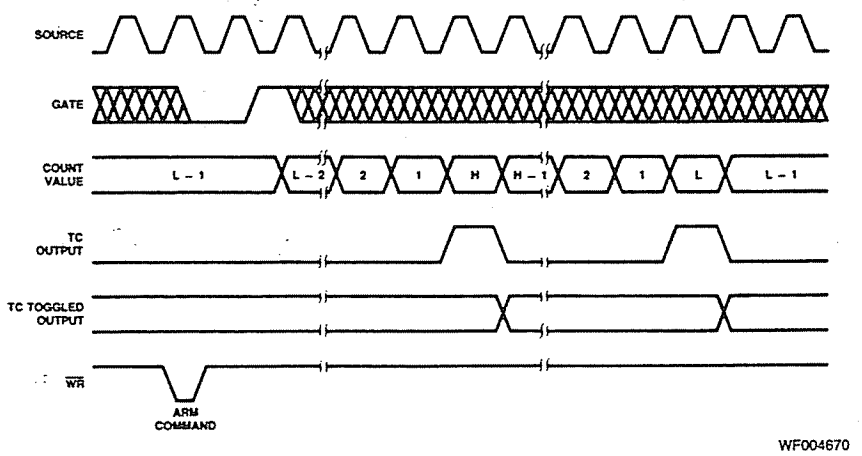


Figure 1-16l. Mode I Waveforms

MODE J

Variable Duty Cycle Rate Generator with No Hardware Gating

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
0	0	0	X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	1	1	X	X	X	X	X

Mode J, shown in Figure 1-16i, will find the greatest usage in frequency generation applications with variable duty cycle requirements. Once armed, the counter will count continuously until it is issued a DISARM command. On the first TC, the counter will be reloaded from the Hold register. Counting will then proceed until the second TC at which time the counter will be reloaded from the Load register. Counting will continue, with the reload source alternating on each TC, until a DISARM command is issued to the counter. (The third TC reloads from the Hold register, the fourth TC reloads from the Load register, etc.) A variable duty cycle output can be generated by specifying the TC Toggled output in the Counter Mode register. The Load and Hold values then directly control the output duty cycle, with high resolution available when relatively high count values are used.

MODE K

Variable Duty Cycle Rate Generator with Level Gating

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
LEVEL			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	1	1	X	X	X	X	X

Mode K, shown in Figure 1-16k, is identical to Mode J, except that source edges are only counted when the Gate is active. The counter must be armed for counting to occur. Once armed, the counter will count all source edges which occur while Gate is active and disregard those source edges which occur while the Gate is inactive. This permits the Gate to turn the count process on and off. As with Mode J, the reload source used will alternate on each TC, starting with the Hold register on the first TC after any ARM command. When the TC Toggled output is used, this mode allows the Gate to modulate the duty cycle of the output waveform. It can affect both the HIGH and LOW portions of the output waveform.

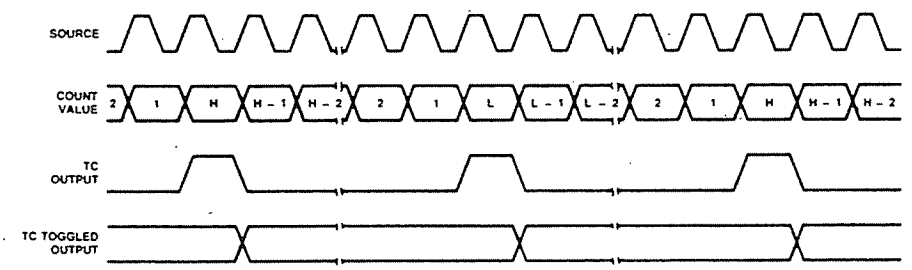


Figure 1-16j. Mode J Waveforms

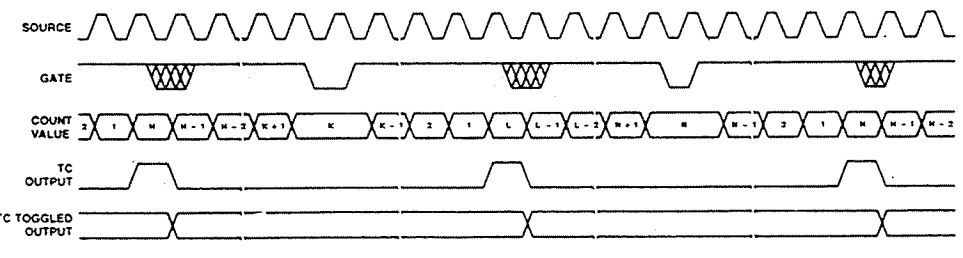


Figure 1-16k. Mode K Waveforms

MODE L

Hardware-Triggered Delayed Pulse One-Shot

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
EDGE			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	1	1	X	X	X	X	X

Mode L, shown in Figure 1-16l, is similar to Mode J except that counting will not begin until a Gate edge is applied to an armed counter. The counter must be armed before application of the triggering Gate edge; Gate edges applied to a disarmed counter are disregarded. The counter will start counting source edges after the triggering Gate edge, and counting will proceed until the second TC. Note that after application of a triggering Gate edge, the Gate input will be disregarded for the remainder of the count cycle. This differs from Mode K, where the gate can be modulated throughout the count cycle to stop and start the counter. On the first TC after application of the triggering Gate edge, the counter will be reloaded from the Hold register. On the second TC, the counter will be reloaded from the Load register, and counting will stop until a new gate edge is issued to the counter. Note that unlike Mode K, new Gate edges are required after every second TC to continue counting.

MODE N

Software-Triggered Strobe with Level Gating and Hardware Retriggering

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
LEVEL			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	0	0	X	X	X	X	X

Mode N, shown in Figure 1-16n, provides a software-triggered strobe with level gating that is also hardware retriggerable. The counter must be issued an ARM command before counting can occur. Once armed, the counter will count all source edges which occur while the gate is active and disregard those source edges which occur while the Gate is inactive. This permits the Gate to turn the count process on and off. After the issuance of the ARM command and the application of an active Gate, the counter will count to TC. Upon reaching TC, the counter will reload from the Load register and automatically disarm itself, inhibiting further counting. Counting will resume upon the issuance of a new ARM command. All active-going Gate edges issued to an armed counter will cause a retrigger operation. Upon application of the Gate edge, the counter contents will be saved in the Hold register. On the first qualified source edge after application of the retriggering gate edge, the contents of the Load register will be transferred into the counter. Counting will resume on the second qualified source edge after the retriggering Gate edge. Qualified source edges are active-going edges which occur while the Gate is active.

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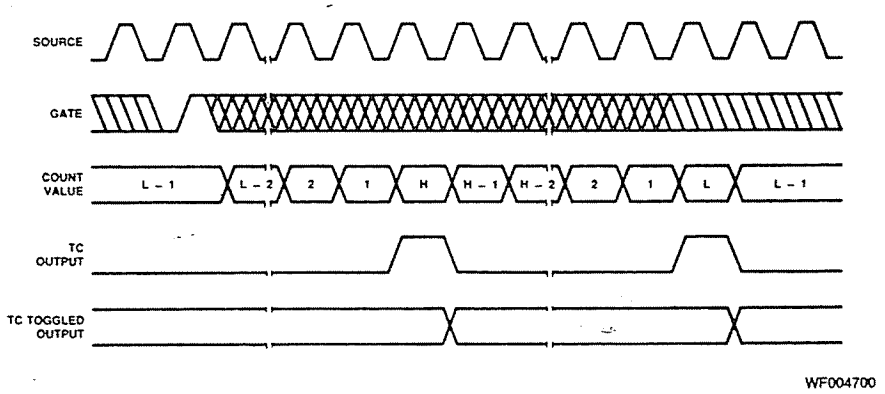


Figure 1-16l. Mode L Waveforms

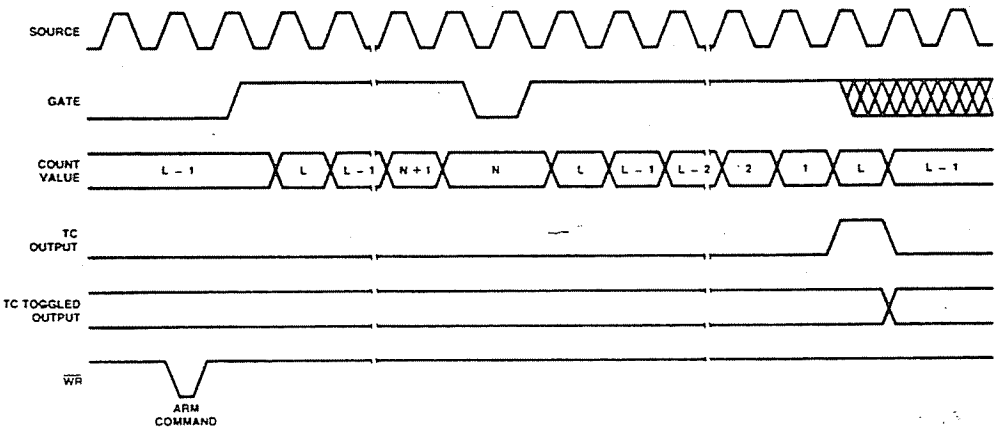


Figure 1-16n. Mode N Waveforms

MODE O

Software-Triggered Strobe with Edge Gating and Hardware Retriggering

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
EDGE			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	0	0	X	X	X	X	X

Mode O, shown in Figure 1-16o, is similar Mode N, except that counting will not begin until an active-going Gate edge is applied to an armed counter and the Gate level is not used to modulate counting. The counter must be armed before application of the triggering Gate edge; Gate edges applied to a disarmed counter are disregarded. Irrespective of the Gate level, the counter will count all source edges after the triggering Gate edge until the first TC. On the first TC, the counter will be reloaded from the Load register and disarmed. A new ARM command and a new Gate edge must be applied in that order to initiate a new counting cycle. Unlike Modes C, F, I and L, which disregard the Gate input once counting starts, in Mode O the count process will be retriggered on all active-going Gate edges, including the first Gate edge used to start the counter. On each retriggering Gate edge, the counter contents will be transferred into the Hold register. On the first source edge after the retriggering Gate edge, the Load register contents will be transferred into the counter. Counting will resume on the second-source edge after a retrigger.

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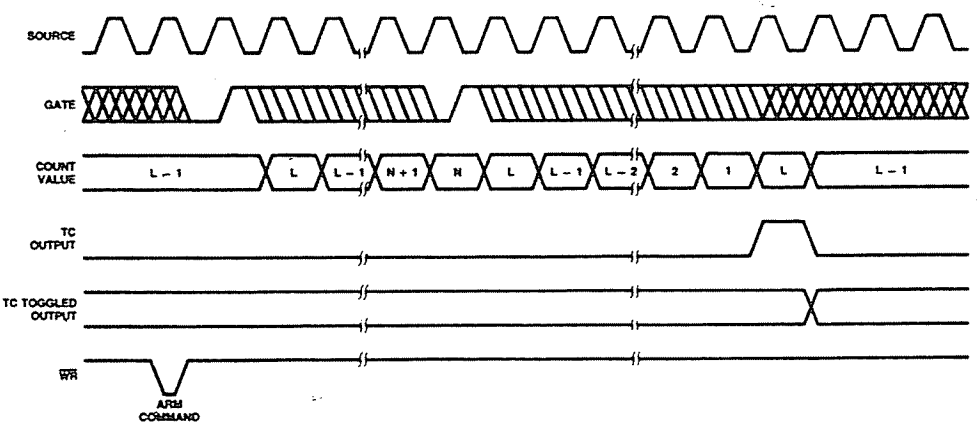


Figure 1-16o. Mode O Waveforms

MODE Q

Rate Generator with Synchronization (Event Counter with Auto-Read/Reset)

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
LEVEL			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	0	1	X	X	X	X	X

Mode Q, shown in Figure 1-16q, provides a rate generator with synchronization or an event counter with auto-read/reset. The counter must first be issued an ARM command before counting can occur. Once armed, the counter will count all source edges which occur while the Gate is active and disregard those edges which occur while the Gate is inactive. This permits the Gate to turn the count process on and off. After the issuance of an ARM command and the application of an active Gate, the counter will count to TC repetitively. On each TC,the counter will reload itself from the Load register. The counter may be retriggered at any time by presenting an active-going Gate edge to the Gate input. The retriggering Gate edge will transfer the contents of the counter into the Hold register. The first qualified source edge after the retriggering Gate edge will transfer the contents of the Load register into the Counter. Counting will resume on the second qualified source edge after the retriggering Gate edge. Qualified source edges are active-going edges which occur while the Gate is active.

MODE R

Retriggerable One-Shot

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
EDGE			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	0	1	X	X	X	X	X

Mode R, shown in Figure 1-16r, is similar to Mode Q, except that edge gating rather than level gating is used. In other words, rather than use the Gate level to qualify which source edges to count, Gate edges are used to start the counting operation. The counter must be armed before application of the triggering Gate edge; Gate edges applied to a disarmed counter are disregarded. After application of a Gate edge, an armed counter will count all source edges until TC, irrespective of the Gate level. On the first TC, the counter will be reloaded from the Load register and stopped. Subsequent counting will not occur until a new Gate edge is applied. All Gate edges applied to the counter, including the first used to trigger counting, initiate a retrigger operation. Upon application of a Gate edge, the counter contents are saved in the Hold register. On the first source edge after the retriggering Gate edge, the Load register contents will be transferred into the counter. Counting will resume on the second source edge after the retriggering Gate edge.

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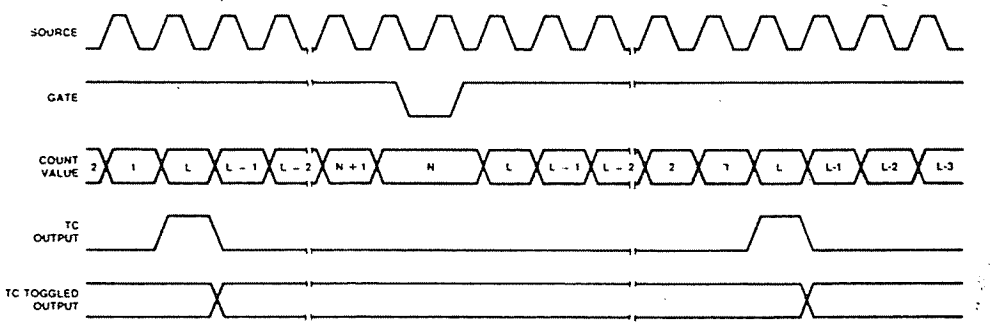


Figure 1-16q. Mode Q Waveforms

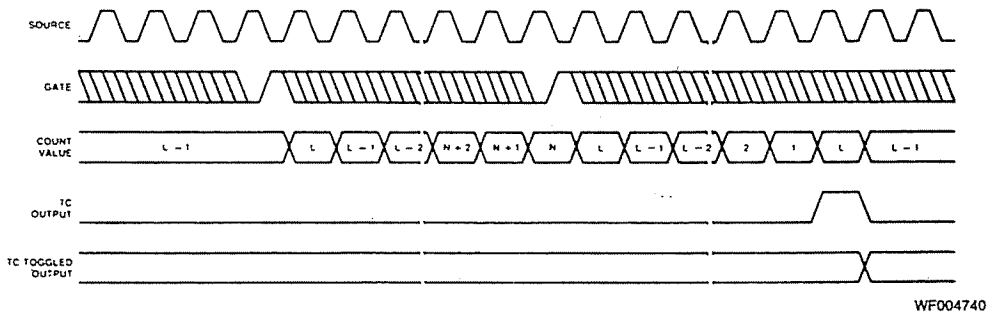


Figure 1-16r. Mode R Waveforms

MODE S

RELOAD SOURCE

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
0	0	0	X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	1	0	X	X	X	X	X

In this mode, the reload source for LOAD commands (irrespective of whether the counter is armed or disarmed) and for TC-initiated reloads is determined by the Gate input. The Gate input in Mode S is used only to select the reload source, not to start or modulate counting. When the Gate is Low, the Load register is used; when the Gate is High, the Hold register is used. Note the Low-Load, High-Hold mnemonic convention. Once armed, the counter will count to TC twice and then disarm itself. On each TC, the counter will be reloaded from the reload source selected by the Gate. Following the second TC, an ARM command is required to start a new counting cycle. Mode S is shown in Figure 1-16s.

MODE V

Frequency-Shift Keying

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
0	0	0	X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	1	1	X	X	X	X	X

Mode V, shown in Figure 1-16v, provides frequency-shift keying modulation capability. Gate operation in this mode is identical to that in Mode S. If the Gate is Low, a LOAD command or a TC-induced reload will reload the counter from the Load register. If the Gate is HIGH, LOADs and reloads will occur from the Hold register. The polarity of the Gate only selects the reload source; it does not start or modulate counting. Once armed, the counter will count repetitively to TC. On each TC, the counter will reload itself from the register determined by the polarity of the Gate. Counting will continue in this manner until a DISARM command is issued to the counter. Frequency shift keying may be obtained by specifying a TC Toggled output mode in the Counter Mode register. The switching of frequencies is achieved by modulating the Gate.

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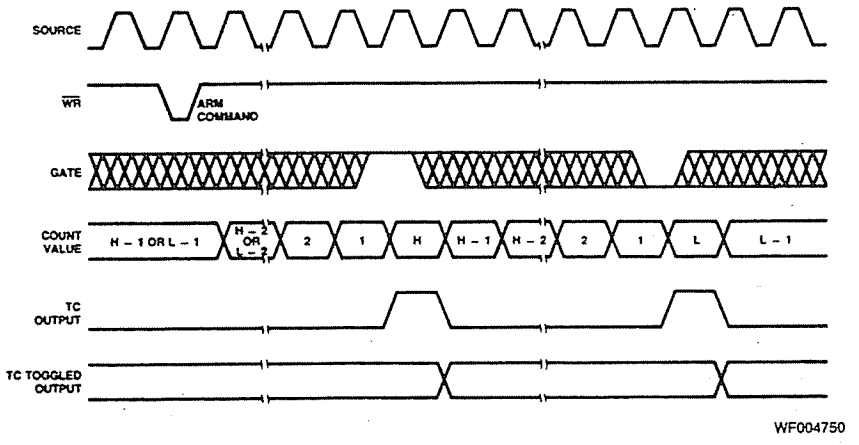


Figure 1-16s. Mode S Waveforms

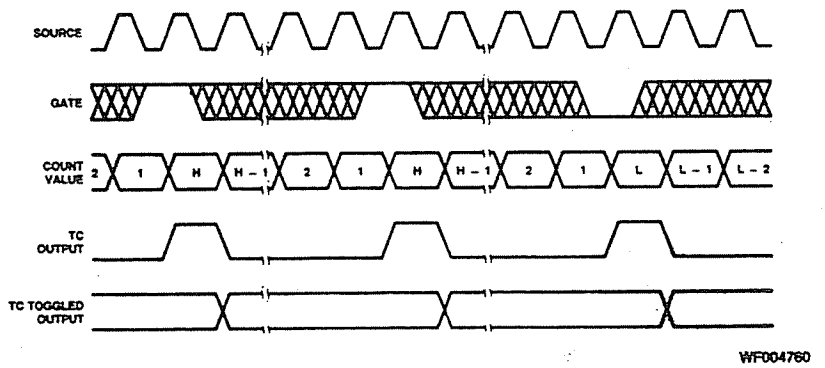


Figure 1-16v. Mode V Waveforms

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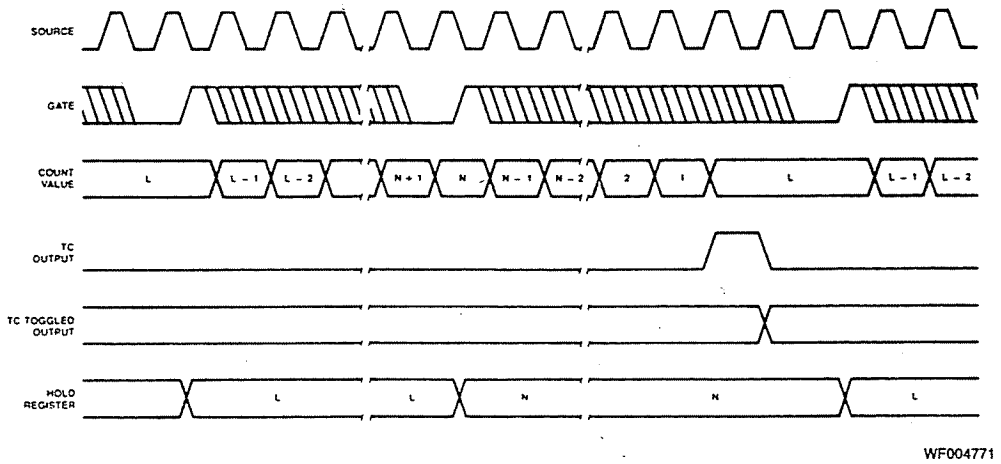


Figure 1-16x. Mode X Waveforms

MODE X

Hardware Save (available in Am9513A only)

CM15	CM14	CM13	CM12	CM11	CM10	CM9	CM8
Edge			X	X	X	X	X

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	1	1	X	X	X	X	X

Mode X, as shown in Figure 1-16x, provides a hardware sampling of the counter contents without interrupting the count. A LOAD AND ARM command or a LOAD command followed by an ARM command is required to initialize the counter. Once armed, a Gate edge starts the counting operation; Gate edges applied to a disarmed counter are disregarded. After application of the Triggering Gate edge, the counter will count all qualified source edges until the first TC, irrespective of the gate level. All gate edges applied during the counting sequence will store the current count in the Hold register, but they will not interrupt the counting sequence. On each TC, the counter will be reloaded from the Load register and stopped. Subsequent counting requires a new triggering Gate edge; counting resumes on the first source edge following the triggering Gate edge.

Note: Mode X is only available in the Am9513'A' devices.

COUNTER MODE CONTROL OPTIONS

Each Counter Logic Group includes a 16-bit Counter Mode (CM) register used to control all of the individual options available with its associated general counter. These options include output configuration, count control, count source and gating control. Figure 1-17 shows the bit assignments for the Counter Mode registers. This section describes the control options in detail. Note that generally each counter is independently configured and does not depend on information outside its Counter Logic Group. The Counter Mode register should be loaded only when the counter is Disarmed. Attempts to load the Counter Mode register when the counter is armed may result in erratic counter operation.

After power-on reset or a Master Reset command, the Counter Mode registers are initialized to a preset condition. The value entered is 0B00 hex and results in the following control configuration:

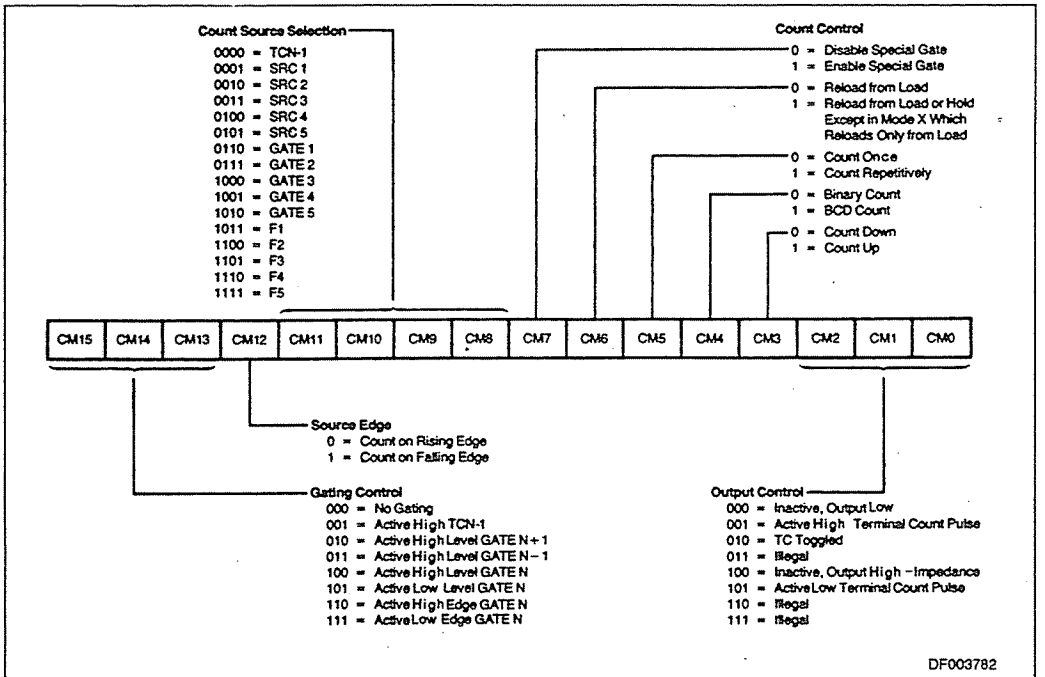
Output low-impedance to ground
Count down
Count binary
Count once
Load register selected
No retriggering
F1 input source selected
Positive-true input polarity
No gating

Output Control

Counter mode bits CM0 through CM2 specify the output control configuration. Figure 1-18 shows a schematic representation of the output control logic. The OUT pin may be off (a high-impedance state), or it may be inactive with a low-impedance to ground. The three remaining valid combinations represent the active-high, active-low or TC Toggle output waveforms.

One output form available is called Terminal Count (TC) and represents the period in time that the counter reaches an equivalent value of zero. TC will occur on the next count when the counter is at 0001 for down counting, at 9999 (BCD) for BCD up counting or at FFFF (hex) for binary up counting. Figure 1-19 shows a Terminal Count pulse and an example context that generated it. The TC width is determined by the period of the counting source. Regardless of any gating input or whether the counter is Armed or Disarmed, the terminal count will go active for only one clock cycle. Figure 1-19 assumes active-high source polarity, counter armed, counter decrementing and an external reload value of K.

The counter will always be loaded from an external location when TC occurs; the user can choose the source location and the value. If a non-zero value is picked, the counter will never really attain a zero state, and TC will indicate the counter state that would have been zero had no parallel transfer occurred.



Note: See Figure 1-16 for restrictions on Count Control and Gating Control bit combinations.

Figure 1-17. Counter Mode Register Bit Assignments

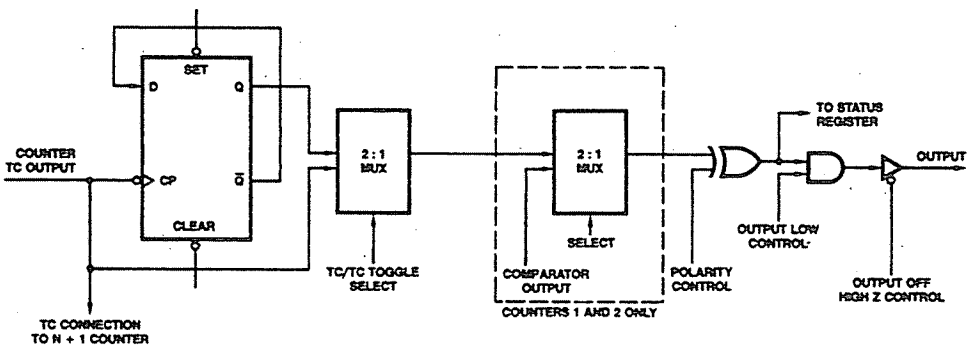


Figure 1-18. Output Control Logic

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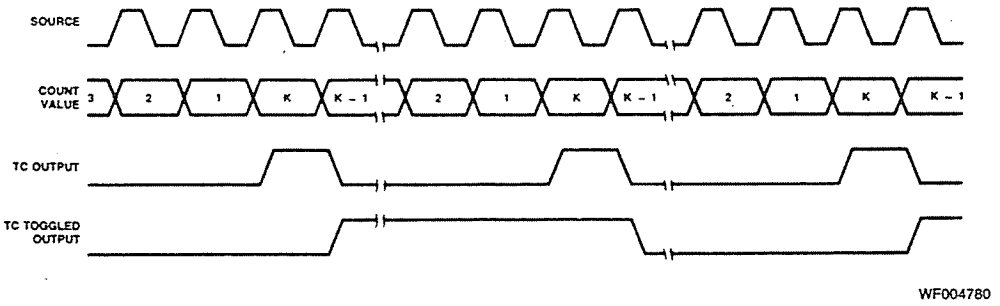


Figure 1-19. Counter Output Waveforms

The other output form, TC Toggled, uses the trailing edge of TC to toggle a flip-flop to generate an output level instead of a pulse. The toggle output is 1/2 the frequency of TC. The TC Toggled output will frequently be used to generate variable duty-cycle square waves in Operating Modes G through K.

In Mode L the TC Toggled output can be used to generate a one-shot function, with the delay to the start of the output pulse and the width of the output pulse separately programmable. With selection of the minimum delay to the start of the pulse, the output will toggle on the second source pulse following application of the triggering Gate edge.

Note that the TC Toggled output form contains no implication about whether the output is active-high or active-low. Unlike the TC output, which generates a transient pulse which can clearly be active-high or active-low, the TC Toggled output waveform only flips the state of the output on each TC. The sole criterion of whether the TC Toggled output is active-high or active-low is the level of the output at the start of the count cycle. This can be controlled by the Set and Clear Output commands. (See Figure 1-20.)

TC (Terminal Count)

On each Terminal Count (TC), the counter will reload itself from the Load or Hold register. TC is defined as that period of time when the counter contents would have been zero had no reload occurred. Some special conditions apply to counter operation immediately before and during TC.

1. In the clock cycle before TC, an internal signal is generated that commits the counter to go to TC on the next count, and retriggering by a hardware Gate edge (Modes N, O, Q and R) or a software LOAD or LOAD AND ARM command will not extend the time to TC. Note that the "next count" driving the counter to TC can be caused by the application of a count source edge (in level gating modes, the edge must occur while the gate is active, or it will be disregarded), by the application of a LOAD or LOAD AND ARM command (see 2 below) or by the application of a STEP command.
2. If a LOAD or LOAD AND ARM command is executed during the cycle preceding TC, the counter will immediately go to TC. If these commands are issued during TC, the TC state will immediately terminate.
3. When TC is active, the counter will always count the next source edge issued to it, even if it is disarmed or gated off during TC. This means that TC will never be active for longer than one count period and it may, in fact, be shorter if a STEP command or a LOAD or LOAD AND ARM command is applied during TC (see item 2 above). This also means that a counter that is disarmed or stopped on TC is actually disarmed/stopped immediately following TC.

This may cause count sequences different from what a user might expect. Since the counter is always reloaded at the start of TC and since it always counts at the end of TC, the counter contents following TC will differ by one from the reloaded value, irrespective of the operating mode used.

If the reloaded value was 0001 for down counting, 9999 (BCD) for BCD up counting or FFFF (hex) for binary up counting, the count at the end of TC will drive the counter into TC again regardless of whether the counter is gated off or disarmed. As long as these values are reloaded, the TC output will stay active. If a TC Toggled output is selected, it will toggle on each count. Execution of a LOAD, LOAD AND ARM or STEP command with these counter contents will act the same as application of a source pulse, causing TC to remain active and a TC Toggled output to toggle.

Count Control

Counter Mode bits CM3 through CM7 specify the various options available for direct control of the counting process. CM3 and CM4 operate independently of the others and control up/down and BCD/binary counting. They may be combined freely with other control bits to form many types of counting configurations. The other three bits and the Gating Control field interact in complex ways. Bit CM5 controls the repetition of the count process. When CM5 = 1, counting will proceed in the specified mode until the counter is disarmed. When CM5 = 0, the count process will proceed only until one full cycle of operation occurs. This may occur after one or two TC events. The counter is then disarmed automatically. The single or double TC requirement will depend on the state of other control bits. Note that even if the counter is automatically disarmed upon a TC, it always counts the count source edge which generates the trailing TC edge.

When TC occurs, the counter is always reloaded with a value from either the Load register of the Hold register. Bit CM6 specifies the source options for reloading the counter. When CM6 = 0, the contents of the Load register will be transferred into the counter at every occurrence of TC. When CM6 = 1, the counter reload location will be either the Load or Hold Register. The reload location in this case may be controlled externally by using a Gate pin (Modes S and V) or may alternate on each TC (Modes G through L). With alternating sources and with the TC Toggled output selected, the duty cycle of the output waveform is controlled by the relative Load and Hold values and very fine resolution of duty cycles ratios may be achieved.

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Bit CM7 controls the special gating functions that allow retriggering and the selection of Load or Hold sources for counter reloading. The use and definition of CM7 will depend on the status of the Gating Control field and bits CM5 and CM6.

Hardware Retriggering

Whenever hardware retriggering is enabled (Modes N, O, Q, and R), all active-going Gate edges initiate retrigger operations. On application of the Gate edge, the counter contents will be transferred to the Hold register. On the first qualified source edge after application of the retriggering Gate edge, the Load register contents will be transferred into the counter. (Qualified source edges are edges which occur while the counter is gated on and Armed.)

This means that, if level gating is used, the edge occurring on active-going gate transitions will initiate a retrigger. Similarly, when edge gating is enabled, an edge used to start the counter will also initiate a retrigger. The first count source edge applied after the Gate edge will not increment/decrement the counter but retrigger it.

If a LOAD, LOAD AND ARM, or a STEP Command occurs between the retriggering Gate edge and the first qualified source edge, it will be interpreted as a source edge and transfer the Load register contents into the counter. Thereafter, the counter will count all qualified source edges.

When some form of Gating is specified, CM7 controls hardware retriggering. In this case, when CM7 = 0, hardware retriggering does not occur; when CM7 = 1, the counter is retriggered any time an active-going Gate edge occurs. Retriggering causes the counter value to be saved in the Hold register and the Load register contents to be transferred into the counter.

When No Gating is specified, the definition of CM7 changes. In this case, when CM7 = 0, the Gate input has no effect on the counting; when CM7 = 1, the Gate input specifies the source (selecting either the Load or Hold register) used to reload the counter when TC occurs. Figure 1-15 shows the various available control combinations for these interrelated bits.

Count Source Selection

Counter Mode bits CM8 through CM12 specify the source used as input to the counter and the active edge that is counted. Bit CM12 controls the polarity for all the sources; logic zero counts rising edges and logic one counts falling edges. Bits CM8 through CM11 select 1 of 16 counting sources to route to the counter input. Five of the available inputs are internal frequencies derived from the internal oscillator (see Figure 1-14 for frequency assignments). Ten of the available inputs are interface pins; five are labeled SRC and five are labeled GATE.

The 16th available input is the TC output from the adjacent lower-numbered counter. (The Counter 5 TC wraps around to the Counter 1 input.) This option allows internal concatenating that permits very long counts to be accumulated. Since all five counters may be concatenated, it is possible to configure a counter that is 80-bits long on one Am9513A chip. When TCN-1 is the source, the count ripples between the connected counters. External connections can also be made, and can use the toggle bit for even longer counts. This is easily accomplished by selecting a TC Toggled output mode and wiring OUTN to one of the SRC inputs.

Gating Control

Counter Mode bits CM15, CM14, CM13 specify the hardware gating options. When "no gating" is selected (000),the counter will proceed unconditionally as long as it is armed. For any other gating mode, the count process is conditioned by the specified gating configuration.

For a code of 100 in this field, counting can proceed only when the pin labeled GATEN associated with Counter N is at a logic high level. When it goes LOW, counting is simply suspended until the Gate goes HIGH again. A code of 101 performs the same function with an opposite active polarity. Codes 010 and 011 offer the same function as 100, but specify alternate input pins as Gating Sources. This allows any of three interface pins to be used as gates for a given counter. On Counter 4, for example, pin 34, pin 35 or pin 36 may be used to perform the gating function. This also allows a single Gate pin to simultaneously control up to three counters. Counters 1 and 5 are considered adjacent when using TCN - 1 (001), Gate N +1 (010) and Gate N –1 (011) controls.

For codes of 110 or 111 in this field, counting proceeds after the specified active Gate edge until one or two TC events occur. Within this interval, the Gate input is ignored, except for the retriggering option. When repetition is selected, a cycle will be repeated as soon as another Gate edge occurs. With repetition selected, any Gate edge applied after TC goes active will start a new count cycle. Edge gating is useful when implementing a digital single-shot since the gate can serve as a convenient firing trigger.

A 001 code in this field selects the TC (not TOGGLE) output from the adjacent lower-numbered counter as the gate. This is useful for synchronous counting when adjacent counters are concatenated.

COMMAND DESCRIPTIONS

The command set for the Am9513A allows the host processor to customize and manage the operating modes and features for particular applications, to initialize and update both the internal data and control information, and to manipulate operating bits during operation. Commands are entered directly into the 8-bit Command register by writing into the Control port (see Figure 1-7).

All available commands are described in the following text. Figure 1-20 summarizes the command codes and includes a brief description of each function. Figure 1-21 shows all the unused code combinations; unused codes should not be entered into the Command register since undefined activities may occur.

Six of the command types are used for direct software control of the counting process and they each contain a 5-bit S field. In a linear-select fashion, each bit in the S field corresponds to one of five general counters (S1 = Counter 1, S2 = Counter 2, etc.). When an S bit is a one, the specified operation is performed on the counter so designated; when an S bit is a zero, no operation occurs for the corresponding counter. This type of command format has three basic advantages. It saves host software by allowing any combination of counters to be acted on by a single command. It allows simultaneous action on multiple counters where synchronization of commands is important. It allows counter-specific service routines to control individual counters without needing to be aware of the operating context of other counters.

Three of the commands use a 3-bit binary code (N4, N2, N1) to identify the affected counter (a 001 programs counter 1, etc.). Unlike the previously mentioned commands, these commands allow you to program only one counter at a time.

Command Code								Command Description
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	E2	E1	G4	G2	G1	Load Data Pointer register with contents of E and G fields. (G ≠ 000, G ≠ 110)
0	0	1	S5	S4	S3	S2	S1	Arm counting for all selected counters
0	1	0	S5	S4	S3	S2	S1	Load contents of specified source into all selected counters
0	1	1	S5	S4	S3	S2	S1	Load and Arm all selected counters*
1	0	0	S5	S4	S3	S2	S1	Disarm and Save all selected counters
1	0	1	S5	S4	S3	S2	S1	Save all selected counters in Hold register
1	1	0	S5	S4	S3	S2	S1	Disarm all selected counters
1	1	1	0	1	N4	N2	N1	Set Toggle out (HIGH) for counter N (001 ≤ N ≤ 101)
1	1	1	0	0	N4	N2	N1	Clear Toggle out (LOW) for counter N (001 ≤ N ≤ 101)
1	1	1	1	0	N4	N2	N1	Step counter N (001 ≤ N ≤ 101)
1	1	1	0	1	0	0	0	Set MM14 (Disable Data Pointer Sequencing)
1	1	1	0	1	1	1	0	Set MM12 (Gate off FOUT)
1	1	1	0	1	1	1	1	Set MM13 (Enter 16-bit bus mode)
1	1	1	0	0	0	0	0	Clear MM14 (Enable Data Pointer Sequencing)
1	1	1	0	0	1	1	0	Clear MM12 (Gate on FOUT)
1	1	1	0	0	1	1	1	Clear MM13 (Enter 8-bit bus mode)
1	1	1	1	1	0	0	0	Enable Prefetch for Write operations (Am9513'A' only)
1	1	1	1	1	0	0	1	Disable Prefetch for Write operations (Am9513'A' only)
1	1	1	1	1	1	1	1	Master reset

*Not to be used for asynchronous operations.

Figure 1-20. Am9513A Command Summary

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	0	0	0	0
1	1	1	1	0	1	1	0
1	1	1	1	0	1	1	1
0	0	0	X	X	1	1	0
0	0	0	X	X	0	0	0
*1	1	1	1	1	X	X	X

*Unused except when XXX = 111, 001 or 000.

Figure 1-21. Am9513A Unused Command Codes

Arm Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	1	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified by the S field, will be enabled for counting. A counter must be armed before counting can commerce. Once armed, the counting process may be further enabled or disabled using the hardware gating facilities. This command can only arm or do nothing for a given counter; a zero in the S field does not disarm the counter.

ARM and DISARM commands can be used to gate counter operation on and off under software control. DISARM commands entered while a counter is in the TC state will not take effect until the counter leaves TC. This ensures that the counter never latches up in a TC state. (The counter may leave the TC state because of application of a count source edge, execution of a LOAD or LOAD AND ARM command, or execution of a STEP command.)

In modes which alternate reload sources (Modes G-L), the ARMing operation is used as a reset for the logic which determines which reload source to use on the upcoming TC. Following each ARM or LOAD AND ARM command, a counter in one of these modes will reload from the Hold register on the first TC and alternate reload sources thereafter (reload from the Load register on the second TC, the Hold register on the third, etc.).

Load Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	0	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified in the S field, will be loaded with previously entered values. The source of information for each counter will be either the associated Load register or the associated Hold register, as determined by the operating configuration in the Mode register. The Load/Hold contents are not changed. This command will cause a transfer independent of any current operating configuration for the counter. It will often be used as a software retrigger or as counter initialization prior to active hardware gating.

If a LOAD or LOAD AND ARM command is executed during the cycle preceding TC, the counter will go immediately to TC. This occurs because the LOAD operation is performed by generating a pseudo-count pulse internal to the Am9513A, and the Am9513A is expecting to go into TC on the next count pulse. The reload source used to reload the counter will be the same as that which would have been used if the TC were generated by a source edge rather than by the LOAD operation.

Execution of a LOAD or LOAD AND ARM command while the counter is in TC will cause the TC to end. For Armed counters in all modes except S or V, the LOAD source used will be that to be used for the upcoming TC. (The LOADing operation will not alter the selection of reload source for the upcoming TC.) For Disarmed counters in modes except S or V, the reload sources used will be the LOAD register. For modes S or V, the reload source will be selected by the GATE input, regardless of whether the counter is Armed or Disarmed.

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Refer to page 7-1 for Essential Information on Military Devices

Special considerations apply when modes with alternating reload sources are used (Modes G-L). If a LOAD command drives the counter to TC in these modes, the reload source for the next TC will be from the opposite reload location. In other words, the LOAD-generated TC will cause the reload sources to alternate just as a TC generated by a source edge would. Note that if a second LOAD command is issued during the LOAD-generated TC (or during any other TC, for that matter), the second LOAD command will terminate the TC and cause a reload from the source designated for use with the next TC. The second LOAD will not alter the reload source for the next TC since the second LOAD does not generate a TC; reload sources alternate on TCs only, not on LOAD commands.

Load and Arm Counters*

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	1	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified in the S field, will be first loaded and then armed. This command is equivalent to issuing a LOAD command and then an ARM command.

A LOAD AND ARM command which drives a counter to TC generates the same sequence of operations as execution of a LOAD command and then an ARM command. In modes which disarm on TC (Modes A-C and N-O, and Modes G-I and S if the current TC is the second in the cycle), the ARM part of the LOAD AND ARM command will re-enable counting for another cycle. In modes which alternate reload sources (Modes G-L), the ARMing operation will cause the next TC to reload from the HOLD register, irrespective of which reload source the current TC used.

*This command should not be used during asynchronous operations.

Disarm Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	0	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified by the S field, will be disabled from counting. A disarmed counter will cease all counting independent of other conditions. The only exception to this is that a counter in the TC state will always count once, in order to leave TC, before DISARMing. This count may be generated by a source edge, by a LOAD or LOAD AND ARM command (the LOAD AND ARM command will negate the DISARM command) or by a STEP command. A disarmed counter may be updated using the LOAD command and may be read using the SAVE command. A count process may be resumed using an ARM command. See the ARM command description for further details.

Save Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	0	1	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified by S field, will have their contents transferred into their associated Hold register. The transfer takes place without interfering with any counting that may be underway. This command will overwrite any previous Hold register contents. The SAVE command is designed to allow an accumulated count to be preserved so that it can be read by the host CPU at some later time.

Disarm and Save Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	0	0	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified by the S field, will be disarmed, and the contents of the counter will be transferred into the associated Hold registers. This command is identical to issuing a DISARM command followed by a SAVE command.

Set TC Toggle Output

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	1	N4	N2	N1

(001 ≤ N ≤ 101)

Description: The initial output level for TC Toggle mode is set (HIGH) for counter N selected by N4, N2, N1 = 001 (Counter 1) thru 101 (Counter 5) respectively. This command conditions the TC Toggle flip-flop (see Figure 1-18), but does not appear at the counter output unless TC Toggle mode (CM2, CM1, CM0 = 010) is selected.

Clear TC Toggle Output

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	0	N4	N2	N1

(001 ≤ N ≤ 101)

Description: The initial output level for TC Toggle mode is Cleared (LOW) for counter N selected by N4, N2, N1 = 001 (Counter 1) thru 101 (Counter 5) respectively. This command conditions the TC Toggle flip-flop (see Figure 1-18, but does not appear at the counter output unless TC Toggle mode (CM2, CM1, CM0 = 010) is selected.

Step Counter

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	0	N4	N2	N1

(001 ≤ N ≤ 101)

Description: Counter N is incremented or decremented by one, depending on its operating configuration. If the Counter Mode register associated with the selected counter has its CM3 bit cleared to zero, this command will cause the counter to decrement by one. If CM3 is set to a logic high, this command will increment the counter by one. The STEP command will take effect even on a disarmed counter.

Load Data Pointer Register

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	E2	E1	G4	G2	G1

(G4, G2, G1 ≠ 000, ≠ 110)

Description: Bits in the E and G fields will be transferred into the corresponding Element and Group fields of the Data Pointer register as shown in Figure 1-8. The Byte Pointer bit in the Data Pointer register is set. Transfers into the Data Pointer only occur for G field values of 001, 010, 011, 100, 101 and 111. Values of 000 and 110 for G should not be used. See the "Setting the Data Pointer Register" section of this document for additional details.

Disable Data Pointer Sequencing

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	1	0	0	0

Description: This command sets Master Mode bit 14 without affecting other bits in the Master Mode register. MM14 controls the automatic sequencing of the Data Pointer register. Disabling the sequencing allows repetitive host processor access to a given internal location without repetitive updating of the Data Pointer. MM14 may also be controlled by loading a full word into the Master Mode register.

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Refer to page 7-1 for Essential Information on Military Devices

Enable Data Pointer Sequencing

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	0	0	0	0

Description: This command clears Master Mode bit 14 without affecting other bits in the Master Mode register. MM14 controls the automatic sequencing of the Data Pointer register. Enabling the sequencing allows sequential host processor access to several internal locations without repetitive updating of the Data Pointer. MM14 may also be controlled by loading a full word into the Master Mode register. See the "Data Pointer Register" section of this document for additional information on Data Pointer sequencing

Enable 16-Bit Data Bus

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	1	1	1	1

Description: This command sets Master Mode bit 13 without affecting other bits in the Master Mode register. MM13 controls the multiplexer in the data bus buffer. When MM13 is set, no multiplexing takes place and all 16 external data bus lines are used to transfer information into and out of the STC. MM13 may also be controlled by loading the full Master Mode register in parallel.

Enable 8-Bit Data Bus

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	0	1	1	1

Description: This command clears Master Mode bit 13 without affecting other bits in the Master Mode register. MM13 controls the multiplexer in the data bus buffer. When MM13 is cleared, the multiplexer is enabled and 16-bit internal information is transferred eight bits at a time to the eight low-order external data bus lines. MM13 may also be controlled by loading the full Master Mode register in parallel.

Gate Off FOUT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	1	1	1	0

Description: This command sets Master Mode bit 12 without affecting other bits in the Master Mode register. MM12 controls the output state of the FOUT signal. When gated off, the FOUT line will exhibit a low-impedance to ground. MM12 may also be controlled by loading the full Master Mode register in parallel.

Gate On FOUT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	0	1	1	0

Description: This command clears Master Mode bit 12 without affecting other bits in the Master Mode register. MM12 controls the output status of the FOUT signal. When MM12 is cleared, FOUT will become active and will drive out the selected and divided FOUT signal. MM12 may also be controlled by loading the full Master Mode register in parallel. When FOUT is gated on or off, a transient pulse may be generated on the FOUT signal.

Disable Prefetch for Write Operations

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	1	0	0	1

Description: This command disables the prefetch circuitry during Write operations (if does not affect Read operations). This reduces the write recovery time and allows the user to use block move instructions for initialization of the Am9513A registers. Once prefetch is disabled for writing, an Enable Prefetch for Write or a Reset command is necessary to re-enable the prefetch circuitry for writing. Note: This command is only available in Am9513'A' devices; it is an illegal command in the "non-A Am9513" device.

Enable Prefetch for Write Operations

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	1	0	0	0

Description: This command re-enables the prefetch circuitry for Write operations. It is used only to terminate the Disable Prefetch Command. Note: This command is only available in Am9513'A' devices; it is an illegal command in the "non-A Am9513" device.

Master Reset

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	1	1	1	1

Description: The Master Reset command duplicates the action of the power-on reset circuitry. It disarms all counters, enters 0000 in the Master Mode, Load and Hold registers and enters 0B00 (hex) in the Counter Mode registers.

Following either a power-up or software reset, the LOAD command should be applied to all the counters to clear any that may be in a TC state. The Data Pointer register should also be set to a legal value, since reset does not initialize it. A complete reset operation follows.

1. Using the procedure given in the "Command Initiation" section of this document, enter the FF (hex) command to perform a software reset.
2. Using the "Command Initiation" procedure, enter the LOAD command for all counters, opcode 5F (hex).
3. Using the procedure given in the "Setting the Data Pointer Register" section of this document, set the Data Pointer to a valid code. The legal Data Pointer codes are given in Figure 1-9.

The Master Mode, Counter Mode, Load and Hold registers can now be initialized to the desired values.

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Refer to page 7-1 for Essential Information on Military Devices

Am9513A/Am8073A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
VCC with Respect to VSS ..... −0.5V to +7.0V
All Signal Voltages
with Respect to VSS ..... −0.5V to +7.0V
Power Dissipitation (Package Limitation) 1.5W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

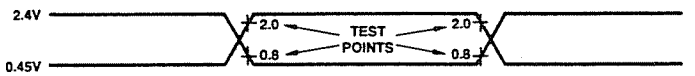
Grade	T_A	V_{CC}	V_{SS}
Commercial	0°C to 70°C	5V ±5%	0V
Industrial	−40°C to 85°C	5V ±10%	0V

Operating ranges define those limits over which the functionality of the device is guaranteed.

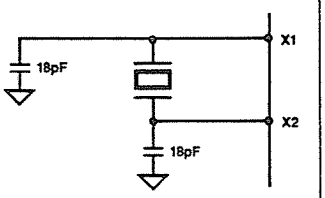
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description		Test Conditions	Min	Typ	Max	Units
VIL	Input Low Voltage	All Inputs Except X2		VSS − 0.5		0.8	Volts
		X2 Input		VSS − 0.5		0.8	
VIH	Input High Voltage	All Input Except X2		2.2V		VCC	Volts
		X2 Input		3.8		VCC	
VITH	Input Hysteresis (SRC and GATE Inputs Only)			0.2	0.3		Volts
VOL	Output Low Voltage		IOL = 3.2mA			0.4	Volts
VOH	Output High Voltage		IOH = −200μA	2.4			Volts
IIX	Input Load Current (Except X2)		VSS ≤ VIN ≤ VCC			±10	μA
IIX	Input Load Current X2					±100	μA
IOZ	Output Leakage Current (Except X1)		VSS + 0.4 ≤ VOUT ≤ VCC High-Impedance State			±25	μA
ICC	VCC Supply Current (Steady State)		T_A = −55°C			275	mA
			T_A = 0°C			255	
			T_A = +25°C		190	235	
CIN	Input Capacitance		f = 1MHz, T_A = +25°C. All pins not under test at 0V.			10	pF
COUT	Output Capacitance					15	
CIO	IN/OUT Capacitance					20	

SWITCHING TEST INPUT/OUTPUT WAVEFORMS



WF004810



TC002000

Crystal is fundamental mode parallel resonant 32pF load capacitance less than 100Ω ESR C_o less than 100pF.

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SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 2, 3, 4)

Parameters	Description		Figure	Am9513A Min	Am9513A Max	AmZ8073A Min	AmZ8073A Max	Units
TAVRL	C/$\overline{D}$ Valid to Read Low		23	25		25		ns
TAVWH	C/$\overline{D}$ Valid to Write High		23	170		170		ns
TCHCH	X2 High to X2 High (X2 Period)		24	145		145		ns
TCHCL	X2 High to X2 Low (X2 High Pulse Width)		24	70		70		ns
TCLCH	X2 Low to X2 High (X2 Low Pulse Width)		24	70		70		ns
TDVWH	Data In Valid to Write High		23	80		80		ns
TEHEH	Count Source High to Count Source High (Source Cycle Time) (Note 10)		24	145		145		ns
TEHEL TELEH	Count Source Pulse Duration (Note 10)		24	70		70		ns
TEHFV	Count Source High to FOUT Valid (Note 10)		24		500		500	ns
TEHGV	Count Source High to Gate Valid (Level Gating Hold Time) (Notes 10, 12, 13)		24	10		10		ns
TEHRL	Count Source High to Read Low (Set-up Time) (Notes 5, 10)		23	190		190		ns
TEHWH	Count Source High to Write High (Set-up Time) (Notes 6, 10)		23	-100		-100		ns
TEHYV	Count Source High to Out Valid (Note 10)	TC Output	24		300		300	ns
		Immediate or Delayed Toggle Output	24		300		300	
		Comparator Output	24		350		350	
TFN	FN High to FN + 1 Valid (Note 14)		24		75		75	ns
TGVEH	Gate Valid to Count Source High (Level Gating Set-up Time) (Notes 10, 12, 13)		24	100		100		ns
TGVGV	Gate Valid to Gate Valid (Gate Pulse Duration) (Notes 11, 13)		24	145		145		ns
TGVWH	Gate Valid to Write High (Notes 6, 13)		23	-100		-100		ns
TRHAX	Read High to C/$\overline{D}$ Don't Care		23	0		0		ns
TRHEH	Read High to Count Source High (Notes 7, 10)		23	0		0		ns
TRHQX	Read High to Data Out Invalid		23	10		10		ns
TRHQZ	Read High to Data Out at High-Impedance (Data Bus Release Time)		23		85		85	ns
TRHRL	Read High to Read Low (Read Recovery Time)		23	1000		1000		ns
TRHSH	Read High to $\overline{CS}$ High (Note 15)		23	0		0		ns
TRHWL	Read High to Write Low (Read Recovery Time)		23	1000		1000		ns
TRLQV	Read Low to Data Out Valid		23		110		110	ns
TRLQX	Read Low to Data Bus Driven (Data Bus Drive Time)		23	20		20		ns
TRLRH	Read Low to Read High (Read Pulse Duration) (Note 15)		23	160		160		ns
TSLRL	$\overline{CS}$ Low to Read Low (Note 15)		23	20		20		ns
TSLWH	$\overline{CS}$ Low to Write High (Note 15)		23	170		170		ns
TWHAX	Write High to C/$\overline{D}$ Don't Care		23	20		20		ns
TWHDX	Write High to Data In Don't Care		23	20		20		ns
TWHEH	Write High to Count Source High (Notes 8, 10, 17)		23	550		550		ns
TWHGV	Write High to Gate Valid (Notes 8, 13, 17)		23	475		475		ns
TWHRL	Write High to Read Low (Write Recovery Time)		23	1500*		1000		ns
TWHSH	Write High to $\overline{CS}$ High (Note 15)		23	20		20		ns
TWHWL	Write High to Write Low (Write Recovery Time)		23	1500*		1000		ns
TWHYV	Write High to Out Valid (Note 9, 17)		23		650		650	ns
TWLWH	Write Low to Write High (Write Pulse Duration) (Note 15)		23	150		150		ns

*In short data write mode TWHRL and TWHWL minimun = 1000ns.

Notes:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Test conditions assume transition times of 10ns or less, timing reference levels of 0.8V and 2.0V and output loading of one TTL gate plus 100pF, unless otherwise noted.
3. Abbreviations used for the switching parameter symbols are given as the letter T followed by four or five characters. The first and third characters represent the signal names on which the measurements start and end. Signal abbreviations used are:

A (Address) = C/$\overline{D}$
C (Clock) = X2
D (Data In) = DB0-DB15
E (Enabled counter source input) = SRC1-SRC5, GATE1-GATE5, F1-F5,TCN-1
F = FOUT
G (Counter gate input) = GATE1-GATE5, TCN-1
Q (Data Out) = DB0-DB15
R (Read) = $\overline{RD}$
S (Chip Select) = $\overline{CS}$
W (Write) = $\overline{WR}$
Y (Output) = OUT1-OUT5

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The second and fourth letters designate the reference states of the signals named in the first and third letters respectively, using the following abbreviations.

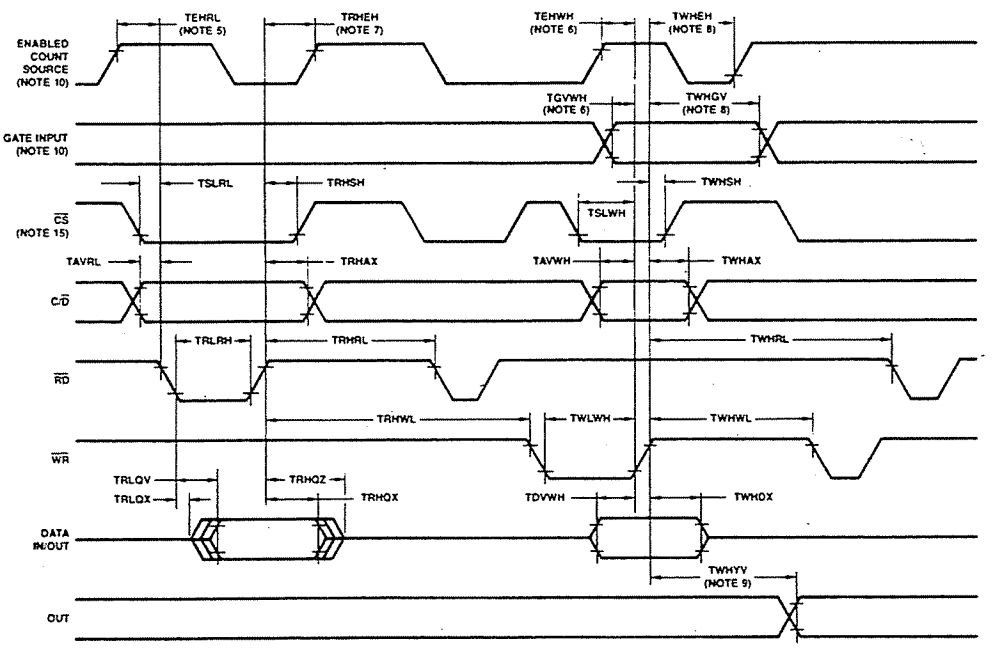
H = HIGH
L = LOW
V = VALID
X = Unknown or Don't care
Z = High-Impedance

4. Switching parameters are listed in alphabetical order.
5. Any input transition that occurs before this minimum setup requirement will be reflected in the contents read from the status register.
6. Any input transition that occurs before this minimum setup requirement will act on the counter before the execution of the operation initiated by the write and the counter may be off by one count.
7. Any input transition that occurs after this minimum hold time is guaranteed to not influence the contents read from the status register on the current read operation.
8. Any input transition that occurs after this minimum hold time is guaranteed to be seen by the counter as occurring after the action initiated by the write operation and the counter may be off by one count.
9. This parameter applies to cases where the write operation causes a change in the output bit.
10. The enabled count source is one of F1-F5, TCN-1 SRC1-SRC5 or GATE1-GATE 5, as selected in the applicable Counter Mode register. The timing diagram assumes the counter counts on rising source edges. The timing specifications are the same for falling-edge counting.
11. This parameter applies to edge gating (CM15-CM13 = 110 or 111) and gating when both CM7 = 1 and CM15-CM13 ≠ 000. This parameter represents the minimum GATE pulse width needed to ensure that the pulse initiates counting or counter reloading.
12. This parameter applies to both edge and level gating (CM15-CM13 = 001 through 111) and gating when both CM7 = 1 and CM15-CM13 = 000. This parameter represents the minimum setup or hold times to ensure that the Gate input is seen at the intended level on the active source edge and the counter may be off by one count.
13. This parameter assumes that the GATENA input is unused (16-bit bus mode) or is tied high. In cases where the GATENA input is used, this timing specification must be met by both the GATE and GATENA inputs.
14. Signals F1-F5 cannot be directly monitored by the user. The phase difference between these signals will manifest itself by causing counters using two different F signals to count at different times on nominally simultaneous transitions in the F signals. F1 = X2.
15. This timing specification assumes that $\overline{CS}$ is active whenever $\overline{RD}$ or $\overline{WR}$ are active. $\overline{CS}$ may be held active indefinitely.
16. This parameter assumes X2 is driven from an external gate with a square wave.
17. This parameter assumes that the write operation is to the command register.

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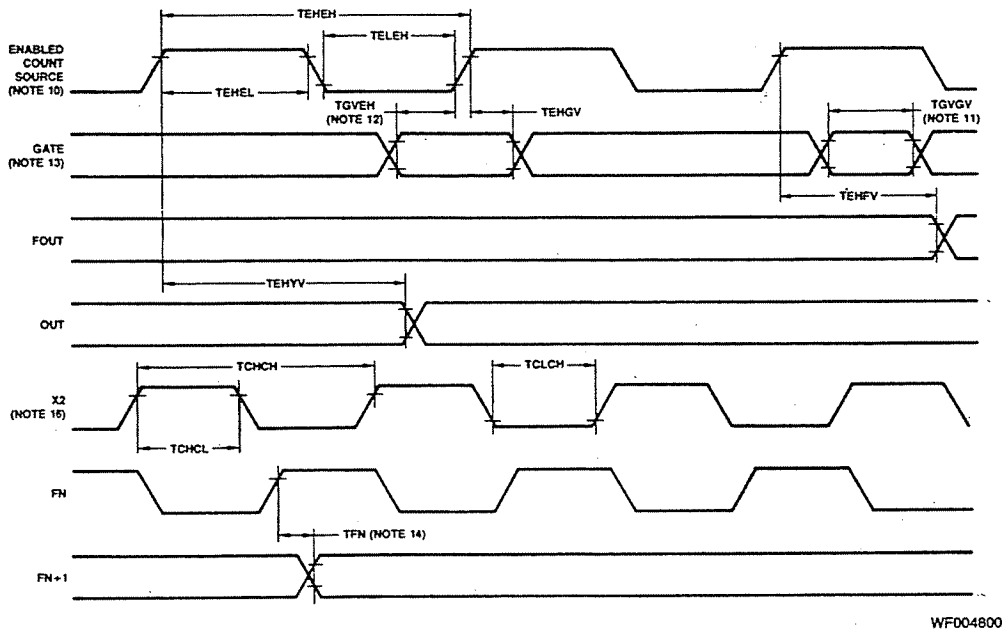
Refer to page 7-1 for Essential Information on Military Devices

BUS TRANSFER SWITCHING WAVEFORMS



WF004790

COUNTER SWITCHING WAVEFORMS



WF004800

01731D

Refer to page 7-1 for Essential Information on Military Devices

Appendix D
Customer Communication

For your convenience, this appendix contains a form to help you gather the information necessary to help us solve technical problems you might have as well as a form you can use to comment on the product documentation. Filling out a copy of the *Technical Support Form* before contacting National Instruments helps us help you better and faster.

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_____

Fax (___)_____ Phone (___)_____

Computer brand _____ Model _____ Processor _____

Operating system _____

Speed _____ MHz RAM _____ MB Display adapter _____

Mouse _____ yes _____ no Other adapters installed _____

Hard disk capacity _____ MB Brand _____

Instruments used _____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is _____

_____

_____

_____

_____

List any error messages _____

_____

_____

_____

_____

The following steps will reproduce the problem _____

_____

_____

NB-MIO-16X Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

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Title: **NB-MIO-16X User Manual**

Edition Date: **November 1993**

Part Number: **320157-01**

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