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PC-AO-2DC/
DAQCard™-AO-2DC
User Manual

Analog Output and Digital I/O Boards for the PC and Macintosh

April 1996 Edition

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About This Manual

This manual describes the electrical and mechanical aspects of the PC-AO-2DC and DAQCard-AO-2DC and contains information concerning their installation and operation. The PC-AO-2DC is fully compatible with the industry-standard Intel-Microsoft Plug and Play Specification version 1.0a. The DAQCard-AO-2DC is for computers equipped with a PCMCIA Type II slot.

The PC-AO-2DC and DAQCard-AO-2DC are analog output and digital I/O devices for PC/XT/AT and IBM Personal System 2 (PS/2) models 25 and 30 computers. You can also use the DAQCard-AO-2DC with Macintosh computers equipped with PCMCIA Type II slots. These devices are designed for low-cost data acquisition and control for applications in laboratory testing, production testing, and industrial process monitoring and control.

Organization of This Manual

The *PC-AO-2DC/DAQCard-AO-2DC User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the PC-AO-2DC and DAQCard-AO-2DC; lists what you need to get started; describes the optional software and optional equipment; and explains how to unpack your AO-2DC.
- Chapter 2, *Installation and Configuration*, contains instructions for installing the PC-AO-2DC and DAQCard-AO-2DC, installing the NI-DAQ software, and cabling.
- Chapter 3, *Signal Connections*, describes the pin arrangement, signal names, and signal connections on the PC-AO-2DC and DAQCard-AO-2DC.
- Chapter 4, *Theory of Operation*, describes the theory of operation for analog output and digital I/O using the PC-AO-2DC and DAQCard-AO-2DC.
- Appendix A, *Specifications*, lists the specifications of the PC-AO-2DC and DAQCard-AO-2DC.
- Appendix B, *X25020 Data Sheet*, contains a manufacturer data sheet for the X25020 SPI serial EEPROM (Xicor). This EEPROM is used on both the PC-AO-2DC and DAQCard-AO-2DC.
- Appendix C, *Connector Block Pin Map*, gives the pin assignments for the CB-50 LP or CB-50 I/O connector blocks when using the PSH27-50F-D1 cable with the DAQCard-AO-2DC.
- Appendix D, *Register-Level Programming*, describes in detail the address and function of each of the PC-AO-2DC and DAQCard-AO-2DC registers.
- Appendix E, *Calibration*, discusses the calibration procedures for the PC-AO-2DC and DAQCard-AO-2DC. You can perform calibration only at the register level.
- Appendix F, *Power-Management Modes*, describes the power-management modes of the DAQCard-AO-2DC.

- Appendix G, *PCMCIA Questions and Answers*, contains a list of common questions and answers relating to PCMCIA card operation.
- Appendix H, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* alphabetically lists the topics in this manual, including the page where you can find the topic.

Conventions Used in This Manual

The following conventions are used in this manual:

AO-2DC	AO-2DC denotes either or both the PC-AO-2DC and DAQCard-AO-2DC.
bold	Bold text denotes menus, menu items, or dialog box buttons or options.
bold italic	Bold italic text denotes a note, caution, or warning.
italic	Italic text denotes emphasis on a specific board or on other important information, a cross reference, or an introduction to a key concept.
`monospace`	Text in this font denotes text or characters that are to be literally input from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, variables, filenames, and extensions, and for statements and comments taken from program code.
Mac	Mac refers to Macintosh computers.
NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles and Macintosh computers unless otherwise noted.
PC	PC refers to PC/XT/AT and IBM PS/2 models 25 and 30 computers.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ devices.
82C55A	82C55A refers to the OKI Semiconductor 82C55A programmable peripheral interface.

♦	The ♦ symbol indicates that the following text applies only to a specific device.
< >	Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit, port, or signal name (for example, ACH<0..7> stands for ACH0 through ACH7).

Abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms are listed in the *Glossary*.

National Instruments Documentation

The *PC-AO-2DC/DAQCard-AO-2DC User Manual* is one piece of the documentation set for your data acquisition system. You could have any of several types of manuals depending on the hardware and software in your system. Use the manuals you have as follows:

- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.
- Software manuals—Examples of software manuals you may have are the LabVIEW and LabWindows® /CVI manual sets. After you set up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) manuals or the NI-DAQ manuals that came with other DAQ devices to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software manuals before you configure your hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides or accessory board user manuals. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.

Related Documentation

The following documents contain information that you may find helpful as you read this manual:

- Your online NI-DAQ software manuals (hardcopy available upon request)
- Your computer operating system manual

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix H, *Customer Communication*, at the end of this manual.

Chapter 1
Introduction

This chapter describes the PC-AO-2DC and DAQCard-AO-2DC; lists what you need to get started; describes the optional software and optional equipment; and explains how to unpack your AO-2DC.

About Your AO-2DC Device

Thank you for purchasing the PC-AO-2DC or DAQCard-AO-2DC, which are analog output and digital I/O devices for PC/XT/AT, IBM Personal System 2 (PS/2) models 25 and 30 and Macintosh computers equipped with PCMCIA Type II slot. Each device has two 12-bit DACs and current output circuitry providing two channels of voltage or current outputs. You can use the voltage or current outputs in set-point types of applications. Each device also provides 16 bits of digital I/O lines. You can install the PC-AO-2DC in any 8-bit or 16-bit expansion slot on a PC, while the DAQCard-AO-2DC is for PCs and Macintosh computers equipped with a PCMCIA Type II slot.

The low cost of a system based on the PC-AO-2DC or DAQCard-AO-2DC makes them ideal for laboratory work in industrial and academic environments. You can use the analog output channels to generate experimental stimuli, to control machines and processes, and to generate analog functions. You can use the digital I/O lines to switch external devices, such as transistors and solid-state relays, and to read the status of external digital logic.

Your AO-2DC device, used in conjunction with the computer, is a versatile, cost-effective platform for laboratory test, measurement, and control. The additional advantages of small size, light weight, and low power consumption make the DAQCard-AO-2DC ideal for use in portable computers. This portability makes remote data acquisition practical. The DAQCard-AO-2DC requires very little power when operating, thus extending the life of the computer batteries.

Detailed specifications of the PC-AO-2DC and DAQCard-AO-2DC are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your AO-2DC device, you will need the following:

❑ One of the following devices:
PC-AO-2DC
DAQCard-AO-2DC

❑ *PC-AO-2DC/DAQCard-AO-2DC User Manual*

❑ One of the following software packages and documentation:
LabVIEW for Macintosh (DAQCard-AO-2DC only)
LabVIEW for Windows
LabWindows/CVI for Windows
NI-DAQ software for Macintosh (DAQCard-AO-2DC only)
NI-DAQ software for PC compatibles

❑ One of the following connector blocks (must be purchased separately):
CB-50 LP (low cost) or CB-50 (DIN-rail mountable) I/O connector blocks with NB1 cable (PC-AO-2DC)
CB-27 I/O connector block with PR27-30F cable (DAQCard-AO-2DC)

❑ Your computer

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use LabVIEW, LabWindows/CVI, or NI-DAQ.

LabVIEW and LabWindows/CVI Application Software

LabVIEW and LabWindows/CVI are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows enhances traditional programming languages. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Libraries are functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition libraries are functionally equivalent to the NI-DAQ software.

Using LabVIEW or LabWindows/CVI software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Figure 1-1 illustrates the relationship between NI-DAQ and LabVIEW and LabWindows/CVI. You can see that the data acquisition parts of LabVIEW and LabWindows/CVI are functionally equivalent to the NI-DAQ software.

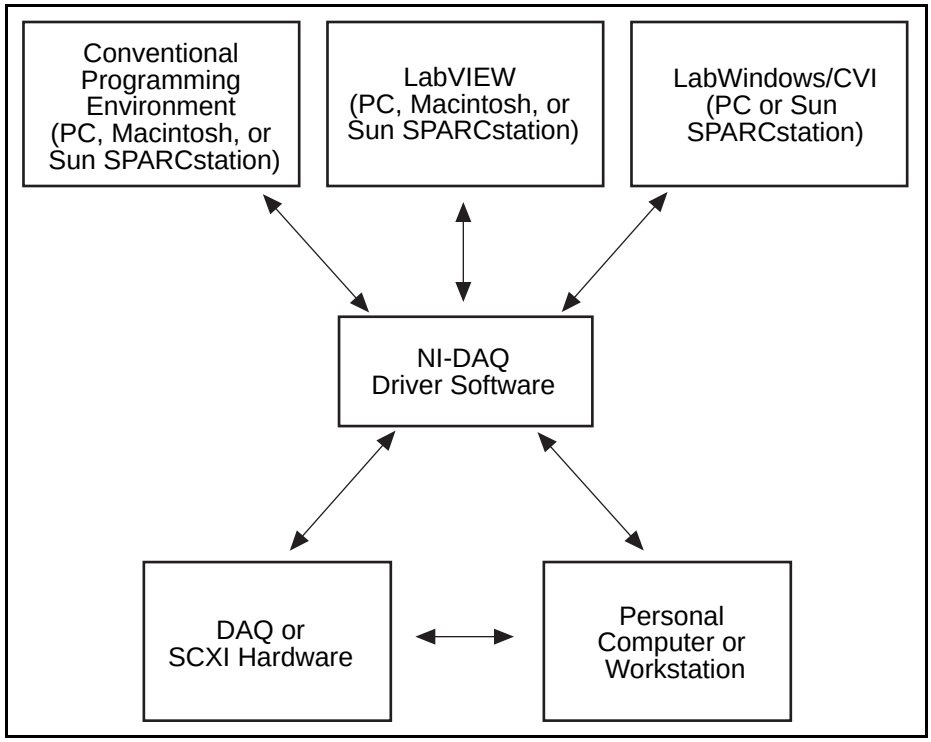


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using NI-DAQ, LabVIEW, or LabWindows/CVI to program your National Instruments DAQ hardware. Using the NI-DAQ, LabVIEW, or LabWindows/CVI software is as easy and as flexible as register-level programming and can save weeks of development time.

Optional Equipment

You can use the following National Instruments product with your PC-AO-2DC board:

- CB-50 LP or CB-50 I/O connector block with 0.5 m or 1.0 m NB-1 connector cable

You can use the following National Instruments product with your DAQCard-AO-2DC device:

- CB-27 I/O connector block with PR27-30F 1.0 m connector cable

Note: ***The CB-50 connector block with PSH27-50F-D1 I/O cable is not recommended for use with the DAQCard-AO-2DC. The PSH27-50F-D1 is optimized for use with the DAQCard-DIO-24.***

For more information about optional equipment available from National Instruments, refer to your National Instruments catalog or call the office nearest you.

Custom Cables

National Instruments currently offers cable termination accessories, the CB-50 LP and CB-50, for use with the PC-AO-2DC. A terminated, 50-conductor, flat ribbon cable is necessary to connect the board to the termination accessory. For the DAQCard-AO-2DC, National Instruments supplies the CB-27 kit, a 27-pin terminal block. A special cable is required to connect the card and accessory. You can attach signal input and output wires to screw terminals on the connector blocks and thereby connect to your AO-2DC device I/O connector.

The CB-50 LP, CB-50, and CB-27 are useful for initial prototyping of an application or in situations where your AO-2DC device interconnections are frequently changed. The CB-50 LP is the low-cost version of the CB-50, whereas the CB-50 is DIN-rail mountable for field wiring. When you develop a final field wiring scheme, however, you may want to develop your own cable. This section contains information and guidelines for designing custom cables.

♦ PC-AO-2DC

The PC-AO-2DC I/O connector is a 50-pin male ribbon cable header. The manufacturer part numbers used by National Instruments for this header are as follows:

- Electronic Products Division/3M (part number 3596-5002)
- T&B/Ansley Corporation (part number 609-500)

The mating connector for the PC-AO-2DC is a 50-position, polarized, ribbon socket connector with strain relief. National Instruments uses a polarized (keyed) connector to

prevent inadvertent upside-down connection to the PC-AO-2DC. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

The following are the standard ribbon cables (50-conductor, 28 AWG, stranded) that can be used with these connectors:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

♦ DAQCard-AO-2DC

The DAQCard-AO-2DC I/O connector is a 25-pin female PCMCIA I/O connector. The manufacturer part number of the connector National Instruments uses is as follows:

- AMP Manufacturing (part number 746288-7)

The following are the standard ribbon cables (30-conductor, 28 AWG, stranded) that work with the 30-pin connectors:

- Electronic Products Division/3M (part number 3365-30)
- T&B/Ansley Corporation (part number 171-30)

Unpacking

Your AO-2DC device is shipped in an antistatic envelope to prevent electrostatic damage. Electrostatic discharge can damage several components on the device. To avoid damage in handling the device, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the package to a metal part of your computer chassis before removing the device from the package.
- Remove the device from the package and inspect the device for loose components or any other sign of damage. Notify National Instruments if the device appears damaged in any way. *Do not* install a damaged device into your computer.
- *Never* touch the exposed pins of connectors.
- Store your AO-2DC device in the antistatic envelope when not in use.

Chapter 2
Installation and Configuration

This chapter contains instructions for installing the PC-AO-2DC and DAQCard-AO-2DC, installing the NI-DAQ software, and cabling.

Hardware Installation

- PC-AO-2DC

  You can install the PC-AO-2DC in any available 8-bit or 16-bit expansion slot in your computer. The following are general installation instructions, but consult your PC user manual or technical reference manual for specific instructions and warnings.

  Warning: ***To prevent electrical SHOCK HAZARD, make sure that the power switch is off and the power cord has been removed from the power entry module.***

  1. Turn off your computer.
  2. Remove the top cover or access port to the I/O channel.
  3. Remove the expansion slot cover on the back panel of the computer.
  4. Record the PC-AO-2DC serial and revision numbers on the Hardware and Software Configuration form in Appendix H, *Customer Communication*. You will need these numbers when you install and configure your device.
  5. Insert the PC-AO-2DC into an 8-bit or a 16-bit slot.
  6. Screw the mounting bracket of the PC-AO-2DC to the back panel rail of the computer.
  7. Check the installation.
  8. Replace the cover.

  The PC-AO-2DC board is installed. You are ready to install your software and configure your board for the programming system you are using.

- DAQCard-AO-2DC

  You can install the DAQCard-AO-2DC in any available Type II PCMCIA slot in your computer.

  The PCMCIA software configures the card for your computer and automatically determines the base address. The following are general installation instructions, but consult your computer user manual or technical reference manual for specific instructions and warnings.

  1. Turn off your computer. If your computer supports hot insertion, you may insert or remove the DAQCard-AO-2DC at any time, whether the computer is powered on or off.

  2. Remove the PCMCIA slot cover on your computer.

  3. Insert the 68-pin PCMCIA bus connector of the DAQCard-AO-2DC into the PCMCIA slot. The card is keyed so that you can insert it only one way.

  4. Attach the I/O cable. The optional PR27-30F cable available for the DAQCard-AO-2DC plugs into the 25-pin I/O connector on the other end of the card. This cable allows connection to other National Instruments products. When plugging and unplugging the cable, always grasp the cable by the connector. Never pull directly on the I/O cable to unplug it from the DAQCard-AO-2DC.

  The DAQCard-AO-2DC is installed.

Configuration

Whether you are using NI-DAQ, LabVIEW, or LabWindows/CVI, your AO-2DC devices are completely software configurable. Refer to your software documentation to install and configure your software.

If you are a register-level programmer, refer to Appendix D, *Register-Level Programming*, of this manual.

- PC-AO-2DC

  Two types of configuration are performed on the PC-AO-2DC—bus related and data acquisition related. Bus-related configuration includes setting the base I/O address. Data acquisition-related configuration includes such settings as analog output polarity selection, range selection, and digital I/O configuration.

Bus-Related Configuration

The PC-AO-2DC works in either a Plug and Play mode or a switchless mode. These modes dictate how the base I/O address is determined and assigned to the board.

Plug and Play Mode

The PC-AO-2DC is fully compatible with the industry-standard Intel/Microsoft Plug and Play Specification version 1.0. A Plug and Play system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers. These resources include the board base I/O address. The PC-AO-2DC is configured at the factory to request these resources from the Plug and Play Configuration Manager.

The Configuration Manager receives all of the resource requests at start up, compares the available resources to those requested, and assigns the available resources as efficiently as possible to the Plug and Play boards. Application software can query the Configuration Manager to determine the resources assigned to each board without your involvement. The Plug and Play software is installed as a device driver or as an integral component of the computer BIOS.

If you have the Windows 95 operating system on your PC, it will configure your PC-AO-2DC. Refer to your NI-DAQ documentation for more information.

Switchless Mode

You can use the PC-AO-2DC in a non-Plug and Play system as a switchless DAQ board. A non-Plug and Play system is a system in which the Configuration Manager has not been installed and which does not contain any non-National Instruments Plug and Play products. You use a configuration utility to enter the base address, and the application software assigns it to the board.

Note: ***Avoid resource conflicts with non-National Instruments devices. For example, do not configure two devices for the same base address.***

Base I/O Address Selection

You can configure the PC-AO-2DC to use base addresses in the range of 100 to 3E0 hex. The PC-AO-2DC occupies 32 bytes of address space and must be located on a 32-byte boundary. Therefore, valid addresses include 100, 120, 140, ..., 3C0, 3E0 hex. This selection is software configured and does not require you to manually change any settings on the board.

- DAQCard-AO-2DC

  If you are using a PC, Windows 95 will automatically configure your DAQCard-AO-2DC.

  If you are using a Macintosh with National Instruments software such as NI-DAQ or LabVIEW, see the *Using the NI-DAQ Control Panel to Configure Your Hardware* section in your *NI-DAQ Software Reference Manual*.

  You can test the hardware configuration by using the `NI-DAQ Configuration Utility` or `WDAQCONF` if you are using a PC.

Data Acquisition-Related Configuration

The AO-2DC devices supply two channels of analog output voltage and two channels of analog output current sinks at the I/O connector. You can select the range for the analog output circuitry though software. The range can be either bipolar or unipolar.

Analog Output Polarity Selection

You can configure each analog output voltage channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to +10 V at the voltage outputs. A bipolar configuration has a range of -5 to +5 V at the voltage outputs. You do not need to configure both channels for the same range.

Note: ***As a power-on condition, both channels power up as unipolar outputs. The output voltage will be ±0.5 V maximum within 100 ms of power up.***

Current Outputs

For current outputs, the analog polarity selection should be unipolar.

The AO-2DC devices provide two channels of current sinks for current loop applications. You can program the current outputs for 0 to 20 mA current loops. You have to provide the voltage source for completing the current loop.

Note: ***As a power-on condition, both channels provide no current sink at power up.***

Digital I/O Configuration

The AO-2DC devices contain 16 lines of digital I/O for general use. These lines are available as two 8-bit I/O ports. You may configure these ports as either an input port or an output port.

Note: ***As a power-on condition, all the digital lines are configured as digital inputs at power up. These lines have internal weak pull ups.***

Chapter 3
Signal Connections

This chapter describes the pin arrangement, signal names, and signal connections on the PC-AO-2DC and DAQCard-AO-2DC.

Warning: ***Connections that exceed any of the maximum ratings of input or output signals on the PC-AO-2DC or DAQCard-AO-2DC may damage your AO-2DC device and your computer. This warning includes connecting any power signals to ground and vice versa. National Instruments is NOT liable for any damages resulting from any such signal connections.***

I/O Connectors

Figure 3-1 shows the pin assignments for the PC-AO-2DC I/O connector. You can use the CB-50 LP or CB-50 I/O connector block and the NB1 cable with the PC-AO-2DC for your prototyping needs.

Figure 3-2 shows the pin assignments for the DAQCard-AO-2DC I/O connector. This connector is located on the edge of the DAQCard-AO-2DC and is accessible at the slot opening of your computer after the card has been properly installed.

Figure 3-3 shows the screw terminal assignments for the CB-27 accessory when connected to the DAQCard-AO-2DC using the PR27-30F ribbon cable.

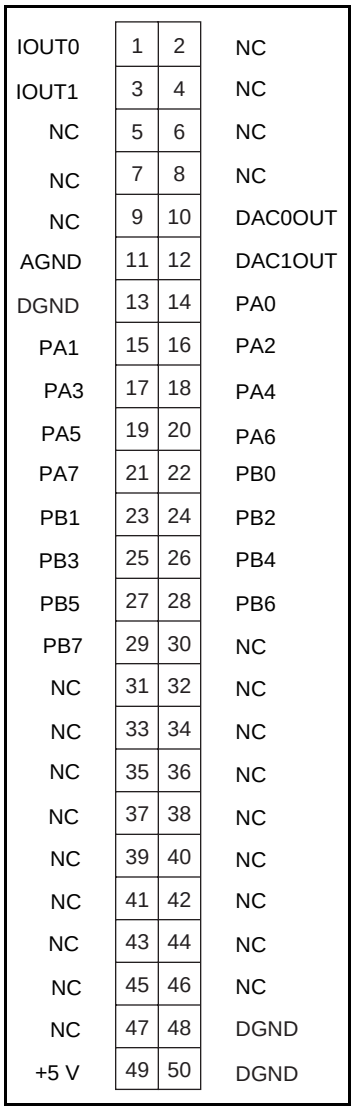


Figure 3-1. PC-AO-2DC I/O Connector Pin Assignments

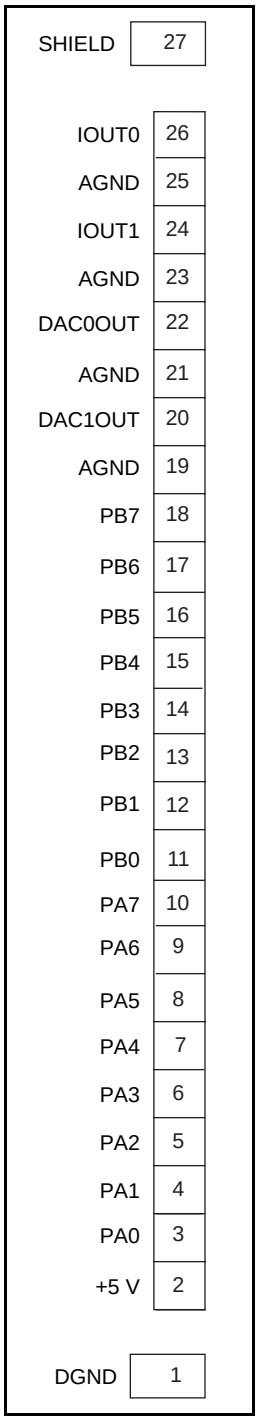


Figure 3-2. DAQCard-AO-2DC I/O Connector Pin Assignments

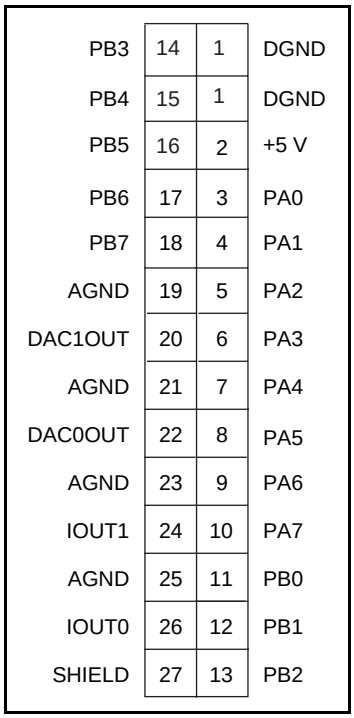


Figure 3-3. Screw Terminal Assignments for the CB-27 I/O Connector Block

Signal Connection Descriptions

- **PC-AO-2DC**

Pin	Signal Name	Description
1	IOUT0	Current Out 0—This signal is the current output for channel 0.
2, 4–9, 30–48	NC	Not connected.
3	IOUT1	Current Out 1—This signal is the current output for channel 1.
10	DAC0OUT	DAC0 Out—This signal is the voltage output for channel 0.
11	AGND	Analog Ground—This is the ground reference for analog output signals.
12	DAC1OUT	DAC1 Out—This is the voltage output signal for channel 1.
13, 50	DGND	Digital Ground—This is the ground reference for digital output/input signals.
14–21	PA<0..7>	Port A0 through Port A7—These signals are the bidirectional digital data lines for port A. PA7 is the MSB; PA0 is the LSB.
22–29	PB<0..7>	Port B0 through Port B7—These signals are the bidirectional digital data lines for port B. PB7 is the MSB; PB0 is the LSB.
49	+5 V	+5 V—This output signal carries 1 A maximum. This has an internal resettable fuse.

♦ **DAQCard-AO-2DC**

Pin	Signal Name	Description
1	DGND	Ground—This pin is connected to the computer ground and digital ground signals.
2	+ 5 V	+5 V—This output signal carries 500 mA maximum and has an internal non-resettable wire fuse.*
3–10	PA<0..7>	Port A0 through Port A7—These signals are bidirectional digital data lines for port A. PA7 is the MSB; PA0 is the LSB.
11–18	PB<0..7>	Port B0 through Port B7—These signals are bidirectional digital data lines for port B. PB7 is the MSB; PB0 is the LSB.
19, 21, 23, 25	AGND	Analog Ground—This is the ground reference for analog output signals.
20	DAC1OUT	DAC1 Out—This is the voltage output signal for channel 1.
22	DAC0OUT	DAC0 Out—This is the voltage output signal for channel 0.
24	IOUT1	Current Out for Channel 1—This signal is the current output for channel 1.
26	IOUT0	Current Out for Channel 0—This signal is the current output for channel 0.
27	SHIELD	Shield—This pin is connected to the card shield and computer ground.

* The DAQCard-AO-2DC fuse is a non-resettable 500 mA, 32 V, fast-acting fuse manufactured by Little Fuse (part number LIT 418.500).

You can use the CB-27 I/O connector block and the PR27-30F cable with the DAQCard-AO-2DC for your prototyping needs.

Analog Output Signal Connections

The PC-AO-2DC uses pins 1, 3, and 10–12 for analog output. The DAQCard-AO-2DC uses pins 20–26 for analog output. The DAQCard-AO-2DC provides individual grounds for each current/voltage output. You can connect each AO-2DC output channel independently for either voltage output or current output. Figure 3-4 shows how to make these signal connections.

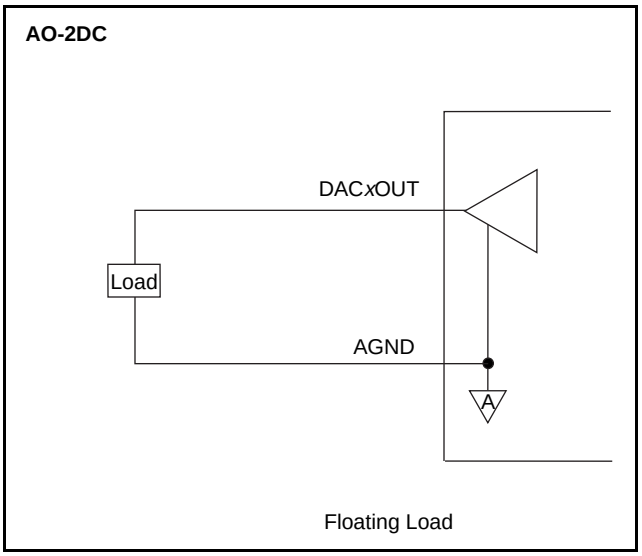


Figure 3-4. DAC Channel Connection as Voltage Output

Voltage Output

A floating load may be connected to your AO-2DC device at the voltage output channel.

Warning: ***Because the AO-2DC device is not optically or magnetically isolated from high voltages, a load with high common mode voltages may damage the AO-2DC device. National Instruments is NOT liable for any damages resulting from any such signal connections.***

Your AO-2DC device may be configured in unipolar range of 0.0 to +10.0 V or in bipolar range of -5.0 to +5.0 V. The polarity is software programmable.

Maximum load current = ±1.0 mA for 12-bit linearity

Power-up Condition

- Range: Unipolar
- Output voltage: ±500 mV maximum within 100 ms of power up

Current Output

A floating load may be connected to your AO-2DC device at the current output channel. An external floating power supply is needed to complete the controlled current loop. You may control the current loop from 0 to 20 mA. The compliance for the current loop is +7.0 V to 40 VDC.

Warning: ***Because the AO-2DC device is not optically or magnetically isolated from high voltages, a load with high common mode voltages may damage the AO-2DC device. National Instruments is NOT liable for any damages resulting from any such signal connections.***

Your AO-2DC device has to be configured in unipolar range of 0.0 to +10.0 V for the current outputs to function correctly. When you use an external supply, the order of the supply and load does not matter as long as you do not create a second loop through which current flows.

- External loop supply voltage: +7.0 V to +40.0 VDC

Power-up Condition

- Range: Unipolar
- Output current: 0 mA

Figure 3-5 shows how to connect a DAC channel as a current output using an external loop supply.

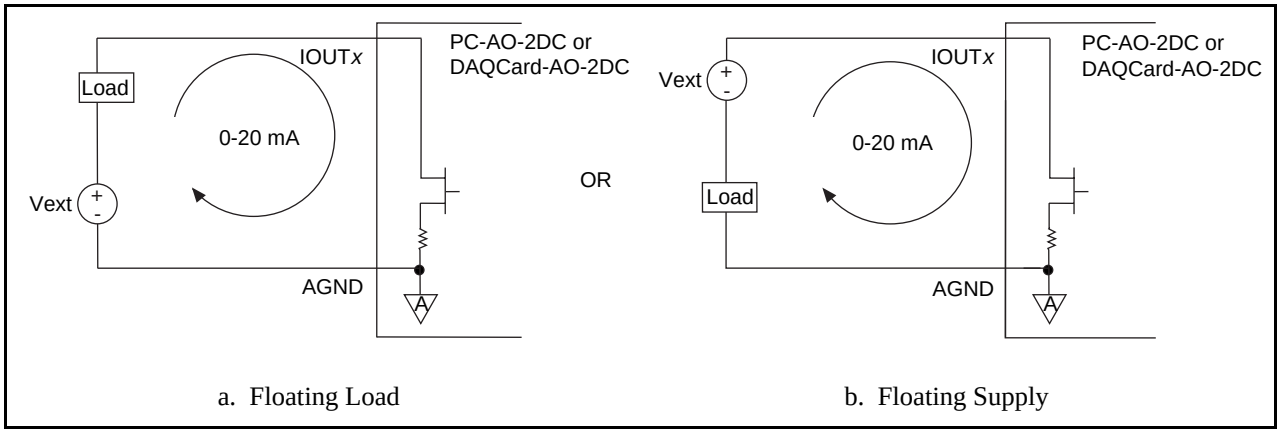


Figure 3-5. DAC Channel Connection as Current Output, External Loop Supply

Figure 3-6 shows an example of a circuit with a second loop; this circuit does not work.

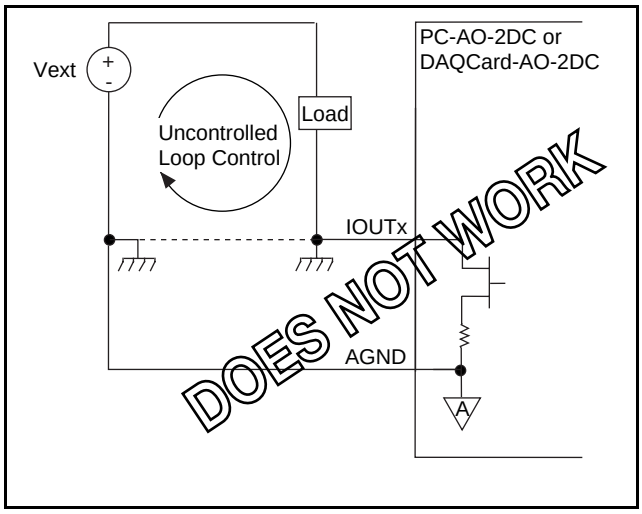


Figure 3-6. Current Loop Connection, Load and External Supply Grounded

Digital I/O Signal Connections

The PC-AO-2DC uses pins 13–29 and pin 50 for digital I/O; the DAQCard-AO-2DC uses pins 1–18 for digital I/O. Figure 3-7 illustrates signal connections for three typical digital I/O applications.

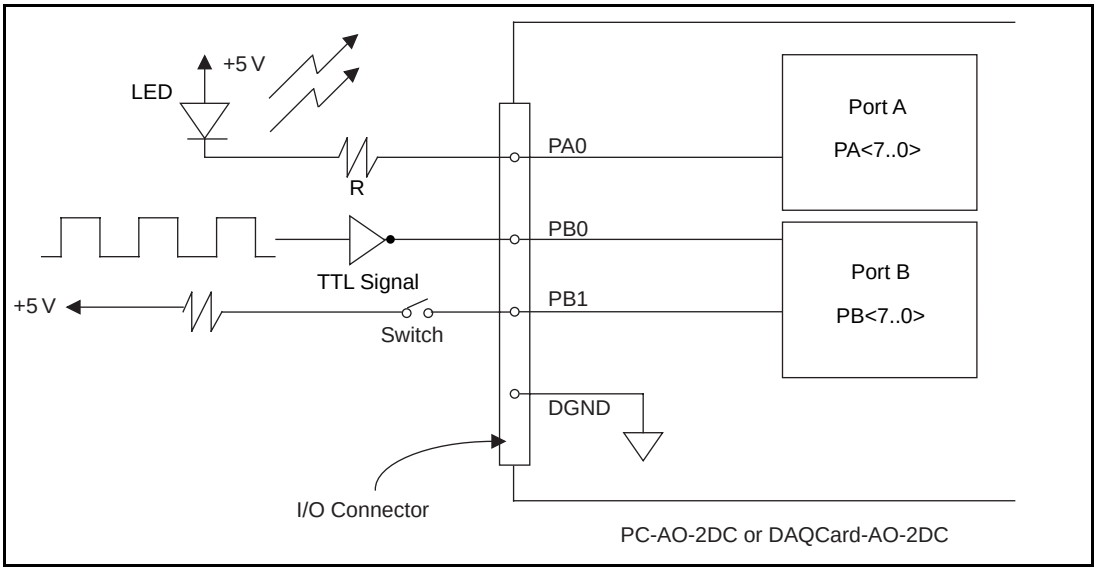


Figure 3-7. Digital I/O Connections

In Figure 3-7, port A is configured for digital output and port B is configured for digital input.

Digital input applications include receiving TTL signals and sensing external device states such as the switch in Figure 3-7. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 3-7.

Refer to Appendix A, *Specifications*, for a list of the digital I/O signal ratings.

Power-up Condition

At power up, both port A and port B of the digital I/O circuitry on the PC-AO-2DC and DAQCard-AO-2DC are configured as input ports. Also, these ports have weak internal pull ups.

Chapter 4
Theory of Operation

This chapter describes the theory of operation for analog output and digital I/O using the PC-AO-2DC and DAQCard-AO-2DC.

Functional Overview

The block diagram in Figure 4-1 shows a functional overview of the PC-AO-2DC and DAQCard-AO-2DC.

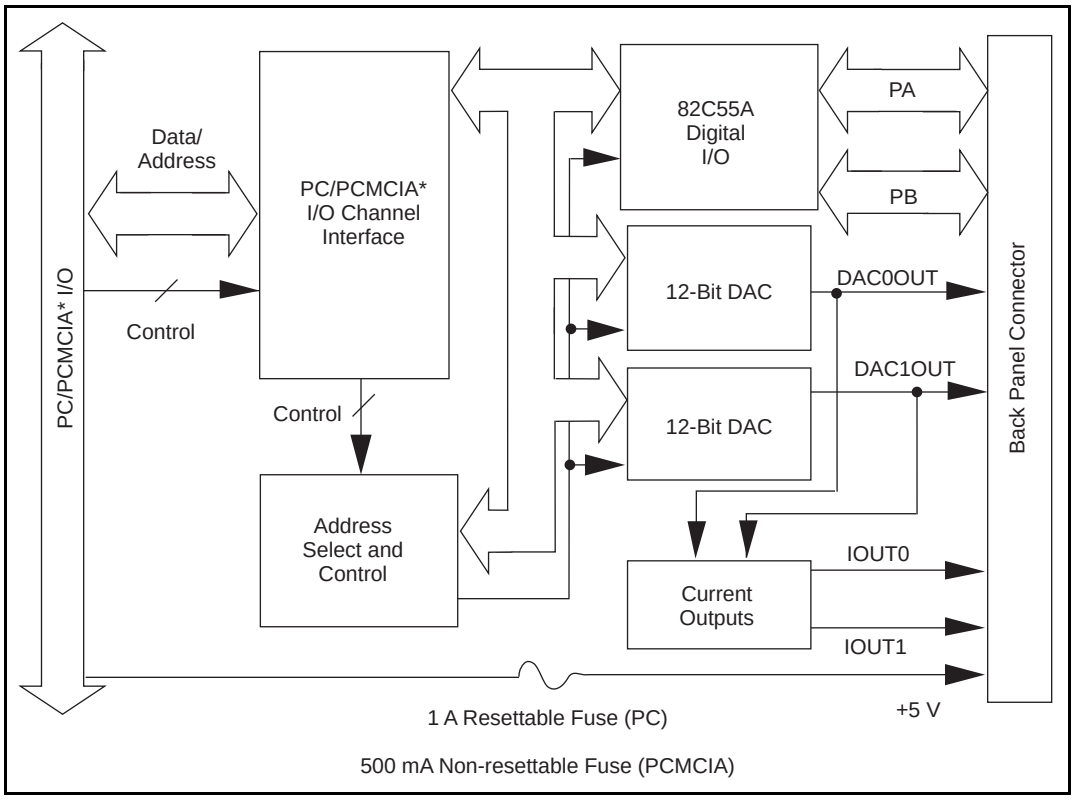


Figure 4-1. PC-AO-2DC and DAQCard-AO-2DC Block Diagram

* PC I/O Channel for PC-AO-2DC; PCMCIA I/O Channel for DAQCard-AO-2DC

Your AO-2DC device consists of the following major components:

- I/O channel interface circuitry
- Analog output circuitry
- Digital I/O circuitry

You can execute data acquisition functions by using the analog output circuitry and the digital I/O circuitry, which are described in detail in the *Analog Output* and *Digital I/O* sections later in this chapter. The internal data and control buses interconnect the components.

I/O Channel Interface Circuitry

The I/O channel interface circuitry consists of address decoders, data buffers, and I/O channel interface timing control circuitry. The circuitry monitors the address lines and timing signals to generate the device select, register select, control, and read/write signals. The data buffers provide larger drive and control the direction of data transfer on the bidirectional data lines based on whether the transfer is a read or write.

♦ PC-AO-2DC

The PC I/O channel of the PC-AO-2DC consists of an address bus, a data bus, and several control and support signals. The components making up the PC I/O channel interface circuitry is shown in Figure 4-2.

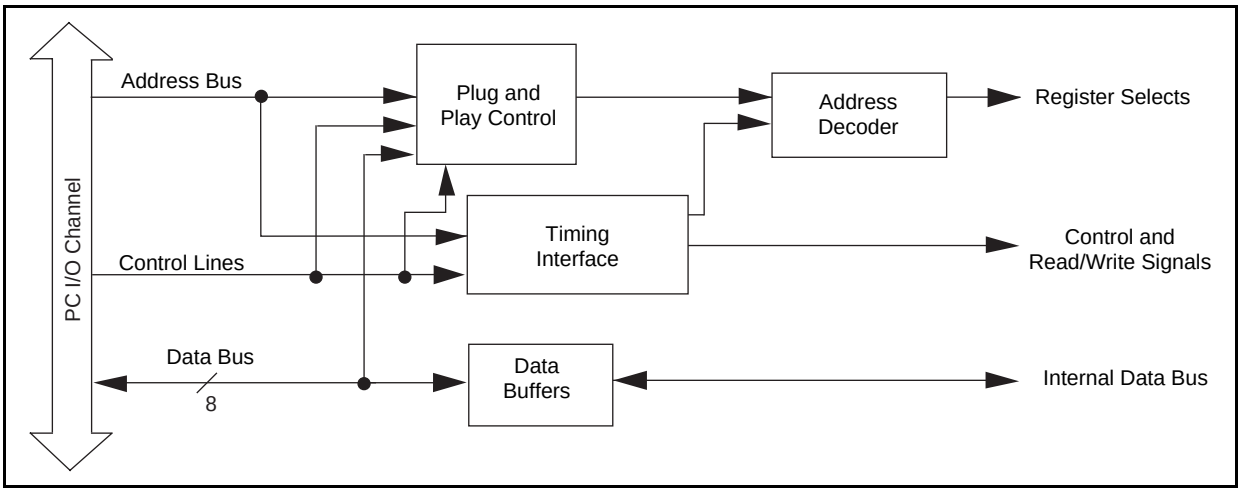


Figure 4-2. PC I/O Interface Circuitry Block Diagram of PC-AO-2DC

♦ DAQCard-AO-2DC

The PCMCIA I/O channel of the DAQCard-AO-2DC consists of an address bus, a data bus, and several control and support signals. The components making up the PCMCIA I/O channel interface circuitry are shown in Figure 4-3.

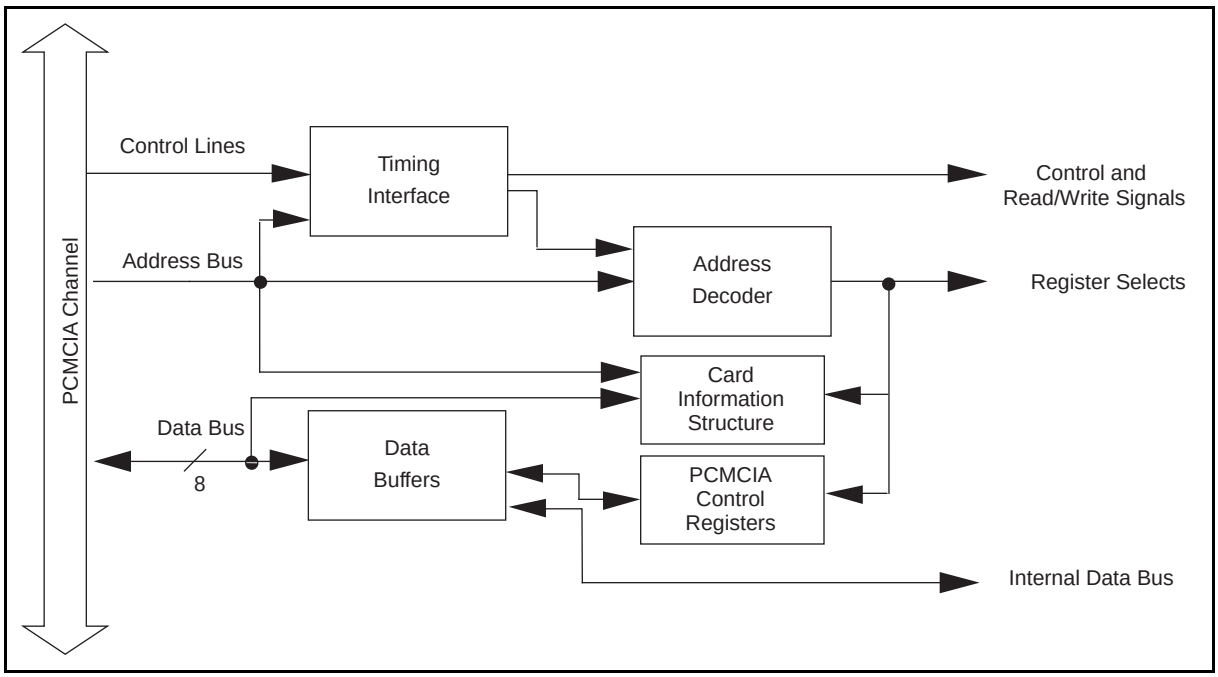


Figure 4-3. PCMCIA I/O Interface Circuitry Block Diagram of DAQCard-AO-2DC

Analog Output

Analog outputs supported by the PC-AO-2DC and DAQCard-AO-2DC consist of two channels of voltage or current output. The theory of operation and signal connections of the analog output circuitry are described in this section.

Your AO-2DC device provides two channels of analog output through two 12-bit DACs. Each analog output channel can provide a unipolar or bipolar voltage output or current output. Figure 4-4 shows a block diagram of the analog output circuitry.

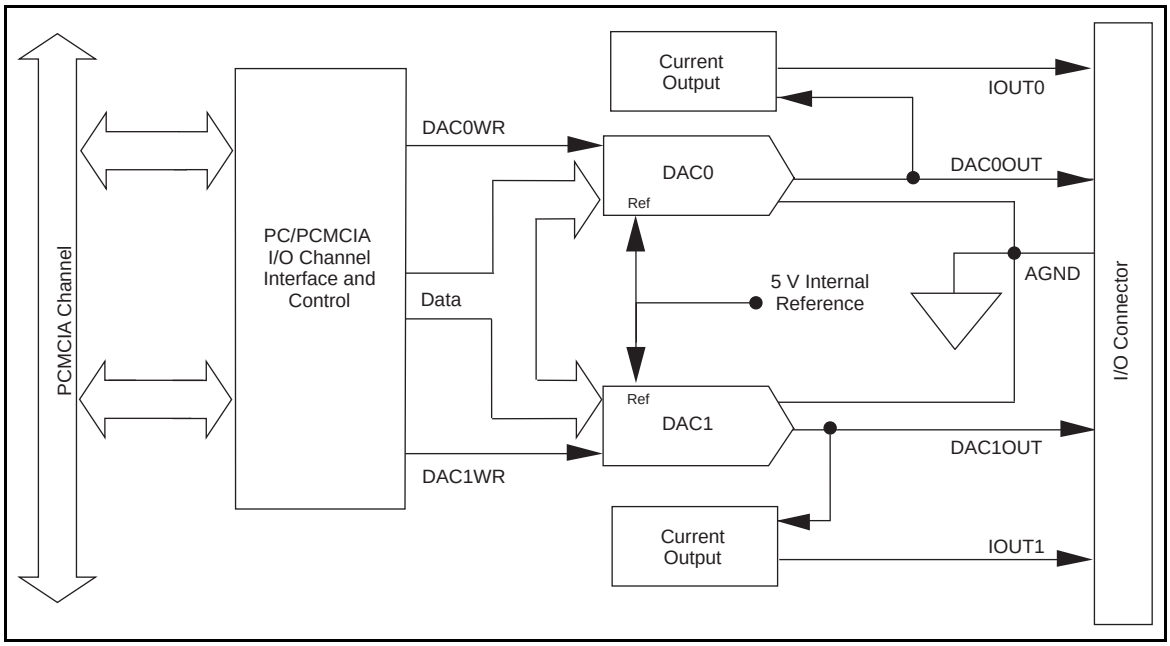


Figure 4-4. Analog Output Circuitry Block Diagram

Each analog output channel contains a 12-bit DAC and voltage-to-current conversion circuitry.

Each DAC channel can be software-configured for either a unipolar voltage output or a bipolar voltage output range. A unipolar output gives an output voltage range of 0.0 to +10.0 V. A bipolar output gives an output voltage range of -5.0 to +5.0 V. You can generate the desired voltage using applicable NI-DAQ function calls. For the proper connection for voltage output, refer to Chapter 3, *Signal Connections*.

Each DAC channel can be software-configured for current outputs. The voltage-to-current conversion circuitry of each analog output channel can create a 0 to 20 mA current sink using an external current loop supply of 7 to 40 V. The current sink converts the voltage from the output of DACs. For the current sink to operate properly, you must use the unipolar voltage output mode. You can use the current output with industry standard 0 to 20 mA or 4 to 20 mA current loops. You can generate the desired current loop using applicable NI-DAQ function calls. For proper connections for current outputs, refer to Chapter 3, *Signal Connections*.

Digital I/O

Your AO-2DC device supports 16-bit digital I/O. The 16 bits are configured as two 8-bit ports that can each be used either as an input port or an output port.

The digital I/O circuitry is designed around the 82C55A general-purpose programmable peripheral interface (PPI). Two of the ports, port A and port B, are used in the AO-2DC devices.

The pins that correspond to these ports are PA<0..7> and PB<0..7> on the AO-2DC connectors. Figure 4-5 shows a block diagram of the digital I/O circuitry. For performing and configuring digital I/O operations, use applicable NI-DAQ function calls.

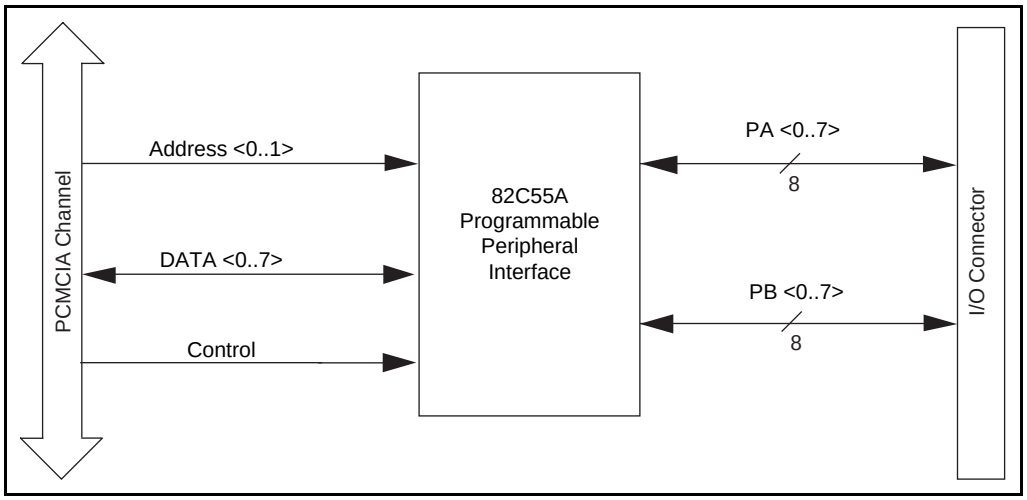


Figure 4-5. Digital I/O Circuitry Block Diagram

All ports on the 82C55A are TTL-compatible. When enabled, the digital output ports are capable of sinking 2.5 mA of current and sourcing 2.5 mA of current on each digital I/O line. When the ports are not enabled, the digital I/O lines act as high-impedance inputs, which have been pulled up by weak pull-up resistors.

Power-down Mode

DAQCard-AO-2DC only

You can power down your DAQCard-AO-2DC by using the power-down utility provided with your NI-DAQ software. This utility will put your DAQCard-AO-2DC in a low-power consumption mode. The effects of power-down mode are as follows:

- The analog output values will not be maintained. For example, if you have set up your voltage output channel to unipolar mode and you are outputting +9.000 V, then after power-down mode the output levels will fall to an unknown level.
- The digital I/O will not be functional.
- After you bring your DAQCard-AO-2DC back from power-down mode to power-up mode, you are required to set up your analog outputs again.

If you are using a PC, bring your DAQCard-AO-2DC to power-down mode by typing: `daqpower D` and to power-up your DAQCard-AO-2DC again, type: `daqpower U.`

If you are using a Mac, refer to your NI-DAQ for Macintosh documentation to use the power-down utilities for PCMCIA cards.

Refer to the configuration utility online documentation that is shipped with your PCMCIA card for more information on power-down features.

Appendix A
Specifications

This appendix lists the specifications of the PC-AO-2DC and DAQCard-AO-2DC. These specifications are typical at 25° C and 50% relative humidity unless otherwise stated.

Analog Output

Output Characteristics

Number of channels ..... Two voltage and two current
Resolution..... 12 bits
Type of DAC..... Double buffered
Data transfers ..... Programmed I/O

Transfer Characteristics

Relative accuracy (INL) of the DAC ..... ±0.5 LSB max[1]
DNL ..... ±1 LSB max
Monotonicity ..... Guaranteed over temperature

Voltage Output

Ranges ..... 0 to 10 VDC, ±5 V, software selectable
Output coupling..... DC
Output impedance ..... 0.5 Ω
Current drive ..... ±2.0 mA max[2]
Absolute accuracy ..... 0.05% FSR[3]
Protection ..... Short circuit to ground
Power-on state ..... ±500 mV within 100 ms, unipolar mode[4]

Current Output

Range ..... 0 to 20 mA
Type ..... Sink to GND, requires external current loop supply
Output impedance ..... 1 GΩ
Excitation voltage range..... +7 to +40 VDC
Absolute accuracy ..... 0.15% FSR
Protection ..... Short circuit to ground
Power-on state ..... 0 A within 100 ms[4]

[1] The relative accuracy for the software corrected DAC is ±1.53 LSB max.
[2] This limit is for the ±5 V range. For unipolar 0–10 VDC range, the current drive is ±1 mA max.
[3] The FSR for either unipolar or bipolar mode is 10 V.
[4] The output level is unknown in the first 100 ms after power up.

Dynamic Characteristics

Settling time ..... 100 µs 0 to 10 VDC
70 µs -5 to +5 VDC
Slew rate..... 0.30 V/µs
Noise..... 45 µVrms, 0 to 22 kHz

Stability

Recommended warm-up time ..... 15 minutes
Offset temperature coefficient..... -60 µV/°C
Gain temperature coefficient..... ±26 ppm/°C

Digital I/O

Number of channels ..... 16 digital I/O available as two 8-bit ports
Compatibility ..... TTL
Power-on state..... Configured as inputs and internally pulled up
Digital logic levels .....

Level	Min	Max
Input low voltage	-0.3 V	0.8 V
Input high voltage	2.2 V	5.0 V
Input leak current ($0 < V_{in} < 5$ V)	-1.0 µA	1 µA
Output low voltage (Iout = 2.5 mA)	0.0 V	0.4 V
Output high voltage (Iout = 2.5 mA)	3.7 V	5.0 V

Transfer rate (1 word = 8 bits)[5]
Input ..... 1 MHz max
Output..... 1 MHz max

Bus Interface

Type ..... Slave

Power Requirements

- PC-AO-2DC
  +5 VDC (±5%)..... 350 mA max
  +12 VDC (±5%)..... 30 mA max
  -12 VDC (±5%) ..... 30 mA max

[5] These limits on the transfer rates are set by the digital I/O circuitry on the card. Actual transfer rates may be lower than these limits, depending on the type of computer, CPU speed, operating system, and the software used.

- DAQCard-AO-2DC

  +5 VDC (±5%)..... 89 mA typ
  95 mA max
  26 mA power-down mode

Note: ***These specifications do not include power consumed by devices connected to the fused +5 V supply pin on the I/O connector.***

Physical

- PC-AO-2DC

  Dimensions ..... 11.3 by 9.9 cm (4.45 by 3.90 in.)
  I/O connector..... 50-pin male

- DAQCard-AO-2DC

  PCMCIA card type ..... Type II
  I/O connector..... 25-pin female PCMCIA I/O connector on card

Environment

Operating..... 0° to 50° C
Temperature ..... -55° to 125° C
Relative humidity..... 5% to 90% noncondensing

Appendix B
X25020 Data Sheet*

This appendix contains a manufacturer data sheet for the X25020 SPI serial EEPROM (Xicor). This EEPROM is used on both the PC-AO-2DC and the DAQCard-AO-2DC.

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Xicor, Inc. *1995 Data Book.*

2K X25020 256 x 8 Bit

SPI Serial E²PROM With BLOCK LOCK™ PROTECTION

FEATURES

- 1MHz Clock Rate
- 256 X 8 Bits
  - —4 Byte Page Mode
- Low Power CMOS
  - —150µA Standby Current
  - —2mA Active Write Current
- 2.7V To 5.5V Power Supply
- Block Lock Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down protection circuitry
  - —Write Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5mS Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 cycles per byte
  - —Data Retention: 100 Years
  - —ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Pin SOIC Package

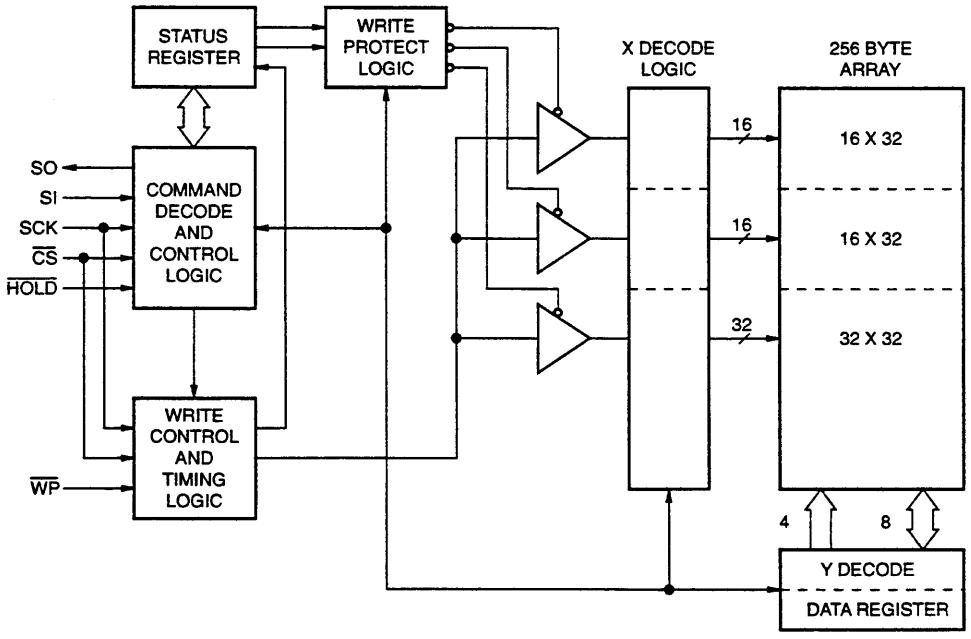
DESCRIPTION

The X25020 is a CMOS 2048 bit serial E²PROM, internally organized as 256 x 8. The X25020 features a serial interface and software protocol allowing operation on a simple three wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25020 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25020 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25020 disabling all write attempts; thus providing a mechanism for limiting end user capability of altering the memory.

The X25020 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



3834 FHD F01

Direct Write™ and Block Lock™ Protection is a trademark of Xicor, Inc.

©Xicor, 1994 Patents Pending
3834-1.1 1/5/95 T0/C11/D0 TD

Characteristics subject to change without notice

X25020

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push-pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select (CS)

When $\overline{CS}$ is high, the X25020 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway the X25020 will be in the standby power mode. $\overline{CS}$ low enables the X25020, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{CS}$ is required prior to the start of any operation.

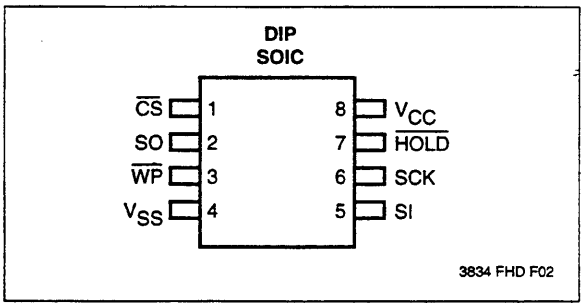
Write Protect (WP)

When WP is low, nonvolatile writes to the X25020 are disabled, but the part otherwise functions normally. When WP is held high, all functions, including nonvolatile writes operate normally. WP going low while $\overline{CS}$ is still low will interrupt a write to the X25020. If the internal write cycle has already been initiated, WP going low will have no affect on write.

Hold (HOLD)

HOLD is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, HOLD may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, HOLD must be brought low while SCK is Low. To resume communication, HOLD is brought high, again while SCK is low. If the pause feature is not used, HOLD should be held high at all times.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
WP	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
HOLD	Hold Input

3834 PGM T01

X25020

PRINCIPLES OF OPERATION

The X25020 is a 256 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of the popular 6805 and 68HC11 microcontroller families.

The X25020 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be low and the HOLD and WP inputs must be high during the entire operation.

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input to place the X25020 into a "PAUSE" condition. After releasing HOLD, the X25020 will resume operation from the point when HOLD was first asserted.

Write Enable (WREN) and Write Disable (WRDI)

The X25020 contains a write enable latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-on condition and after the completion of a byte, page, or status register write cycle. The latch is also reset if WP is brought low.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BL1	BL0	WEL	WIP

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The **Write-In-Process (WIP)** bit indicates whether the X25020 is busy with a write operation. When set to a "1" a write is in progress, when set to a "0" no write is in progress. During a write all other bits are set to "1". This bit is read only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a "1" the latch is set, when set to a "0" the latch is reset. This bit is read only.

The **Block Lock (BL0 and BL1)** bits indicate the extent of protection employed. These bits are set by the user issuing the WRSR instruction.

Write Status Register (WRSR)

The write status register instruction allows the user to select one of four levels of protection. The X25020 is divided into four 512-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses
BL1	BL0	Locked
0	0	None
0	1	CO–$FF (1/4)
1	0	$80–$FF (1/2)
1	1	$00–$FF (all)

3834 PGM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Block Lock Bits)
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

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*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

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DEVICE OPERATION

Clock and Data Timing

Data input on the SI line is sampled and latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

The $\overline{CS}$ line is first pulled low to select the device. The 8 bit read opcode is transmitted to the X25020, followed by the 8 bit byte address. After the read opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($FF) the address counter rolls over to address $00 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high. Refer to the read operation sequence illustrated in Figure 1.

Write Sequence

Prior to any attempt to write data into the X25020 the write enable latch must first be set by issuing the WREN instruction. (See Fig. 2) $\overline{CS}$ is first taken low, then the instruction is clocked into the X25020. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken high. If the user continues the write operation without taking $\overline{CS}$ high after issuing the WREN instruction the write operation will be ignored.

Once the write enable latch is set, the user may proceed by issuing the write instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation. $\overline{CS}$ must go low and remain low for the duration of the operation. The host may continue to write up to four bytes of data to the X25020. The only restriction is the four bytes must reside on the same page. A page address begins with address XXXX XX00 and ends with XXXX XX11. If the byte address counter reaches XXXX XX11 and the clock continues the counter will roll back to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought high after the twenty-fourth, thirty-second, fortieth or forty-eighth clock. If it is brought high at any other time the write operation will not be completed. Refer to Figure 4 below for a detailed illustration of the page write sequence and time frames in which $\overline{CS}$ going high are valid.

While the write is in progress the status register may be read to check the WIP bit. During this time the WIP bit will be high and all other bits in the status register will be high.

Hold Operation

The HOLD input should be high (at V_{IH}) under normal operation. If a data transfer is to be interrupted HOLD can be pulled low to suspend the transfer until it can be resumed. The only restriction is the SCK input must be low when HOLD is first pulled low and SCK must also be low when HOLD is released.

X25020

The HOLD input may be tied high either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25020 powers-on in the following state:

- The device is in the low power standby state. .
- A high to low transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The write enable latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The write enable latch is reset upon power-up.
- A write enable instruction must be issued to set the write enable latch.
- $\overline{CS}$ must come high at the proper clock count in order to start a write cycle.

The write enable latch is reset when WP is brought low.

Figure 1. Read Operation Sequence

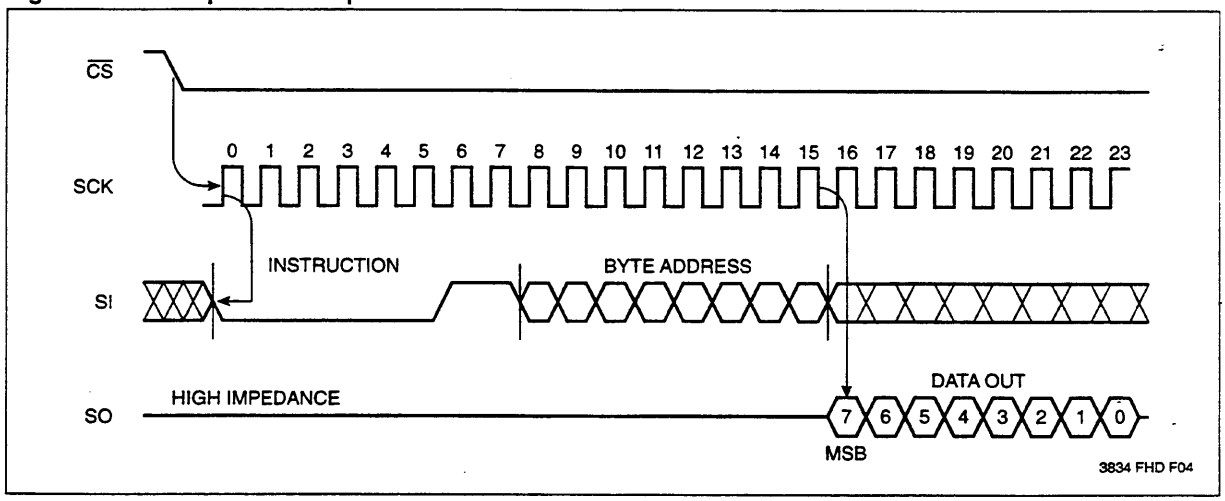
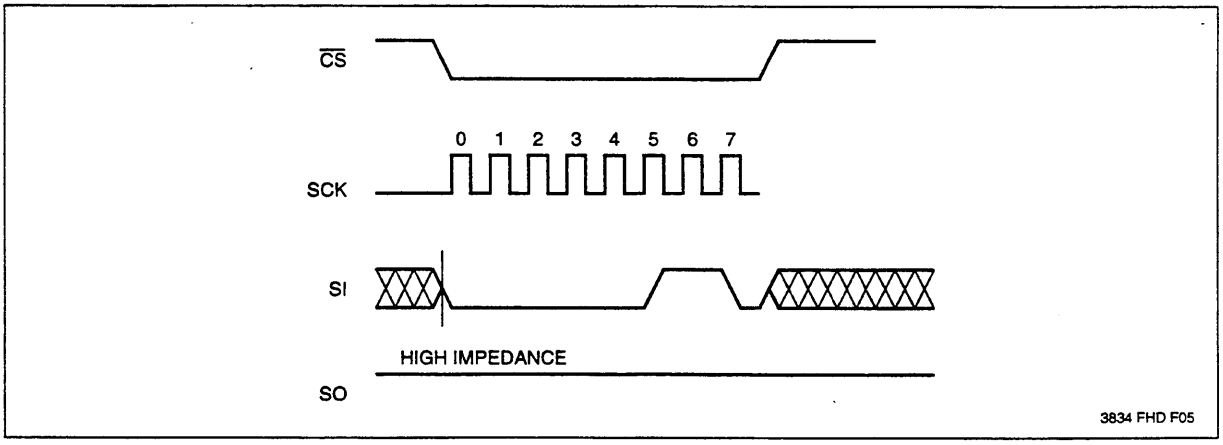


Figure 2. Write Enable Latch



X25020

Figure 3. Write Operation Sequence

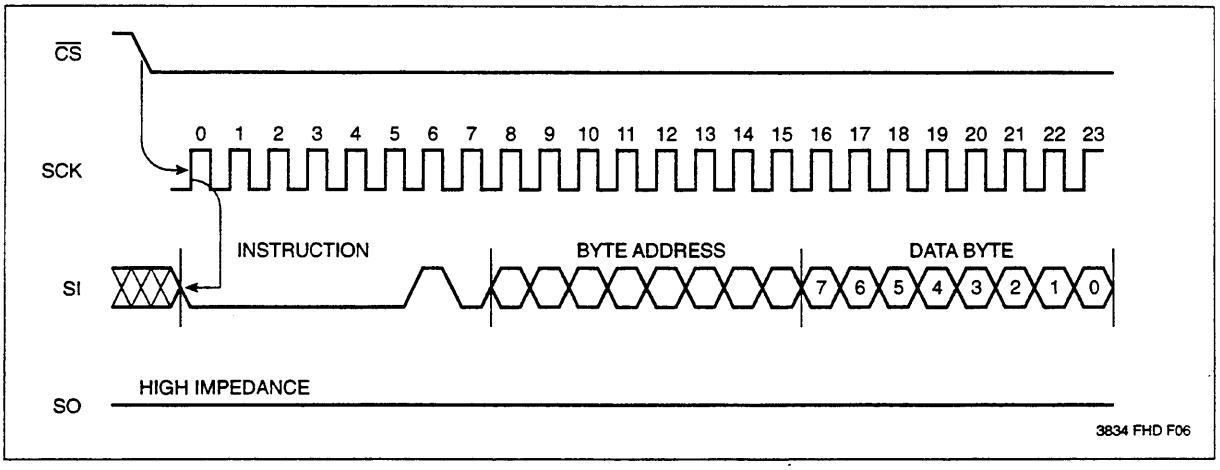
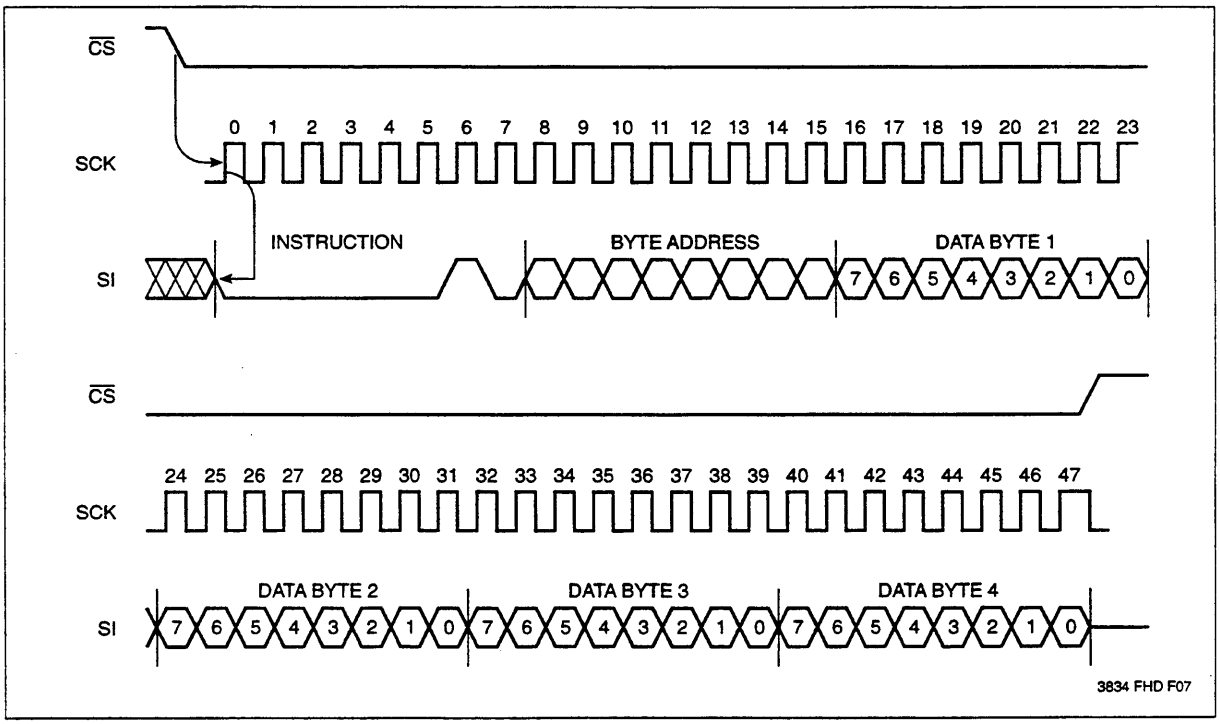


Figure 4. Page Write Operation Sequence



X25020

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to Ground –1.0V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3834 PGM T05

Supply Voltage	Limits
X25020	5V ± 10%
X25020-3	3V to 5.5V
X25020 - 2.7	2.7V to 5.5V

3834 PGM T06

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = OPEN
I_{SB}	V_{CC} Supply Current (Standby)		150	µA	$\overline{CS}$ = V_{CC}, V_{IN} = Gnd or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(1)	Input Low Voltage	–1.0	V_{CC} • 0.3	V	
V_{IH}(1)	Input High Voltage	V_{CC} • 0.7	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	V_{CC}–0.8		V	I_{OH} = –1.0mA

3834 PGM T07

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

3834 PGM T08

CAPACITANCE T_A = 25°C, f = 1.0MHz, V_{CC} = 5V.

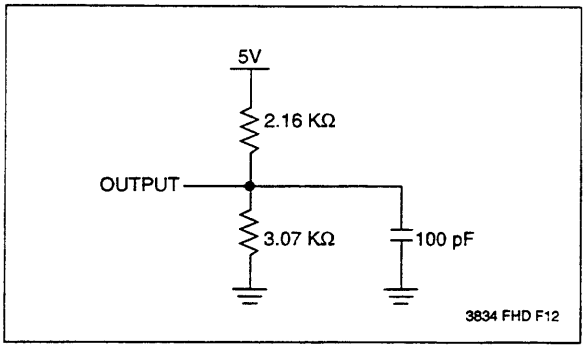
Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, WP, HOLD)	6	pF	V_{IN} = 0V

3834 PGM T09

Notes: (1) V_{IL} Min and V_{IH} Max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

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EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

3834 PGM T10

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock High Time	400		ns
t_{WL}	Clock Low Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}	Data In Rise Time		2.0	µs
t_{FI}	Data In Fall Time		2.0	µs
t_{HD}	HOLD Setup Time	200		ns
t_{CD}	HOLD Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(3)	Write Cycle Time		10	ms

3834 PGM T11

Data Output Timing

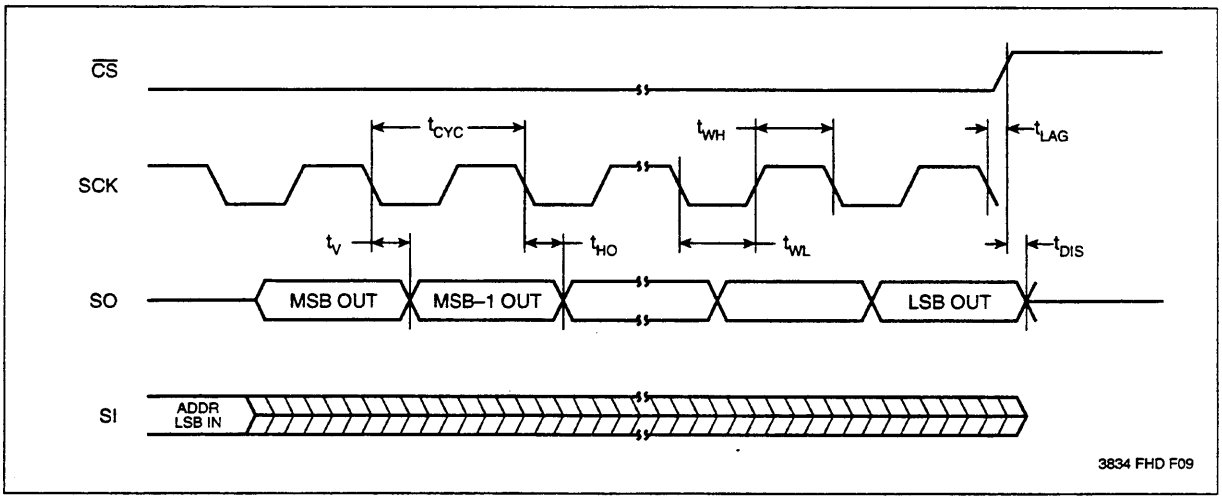
Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from clock Low		360	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}	Output Rise Time		300	ns
t_{FO}	Output Fall Time		300	ns
t_{LZ}	HOLD High to Output in Low Z	100		ns
t_{HZ}	HOLD Low to Output in High Z	100		ns

3834 PGM T12

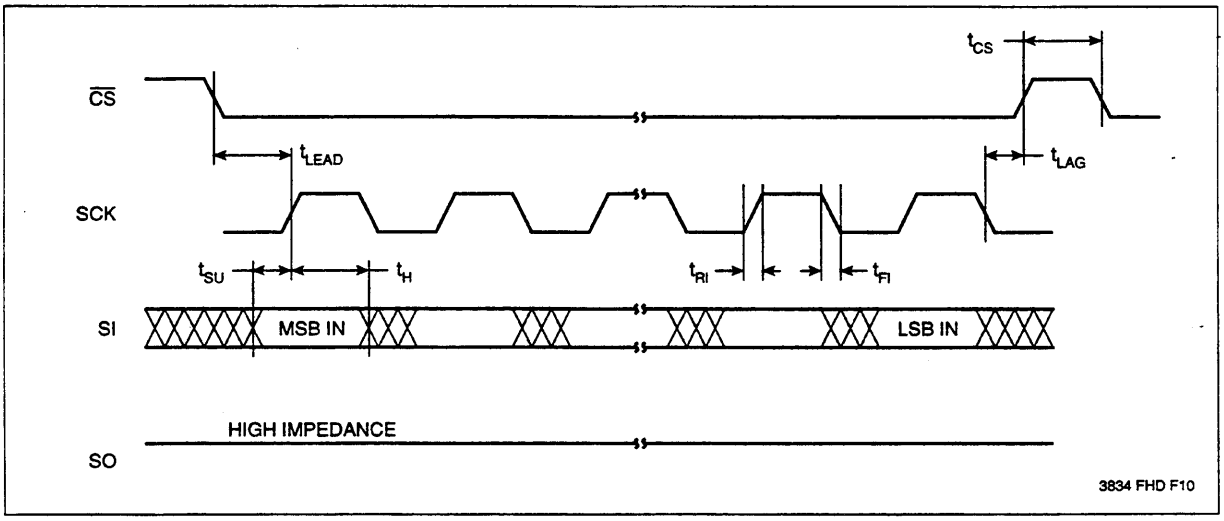
Notes: (3) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

X25020

Serial Output Timing

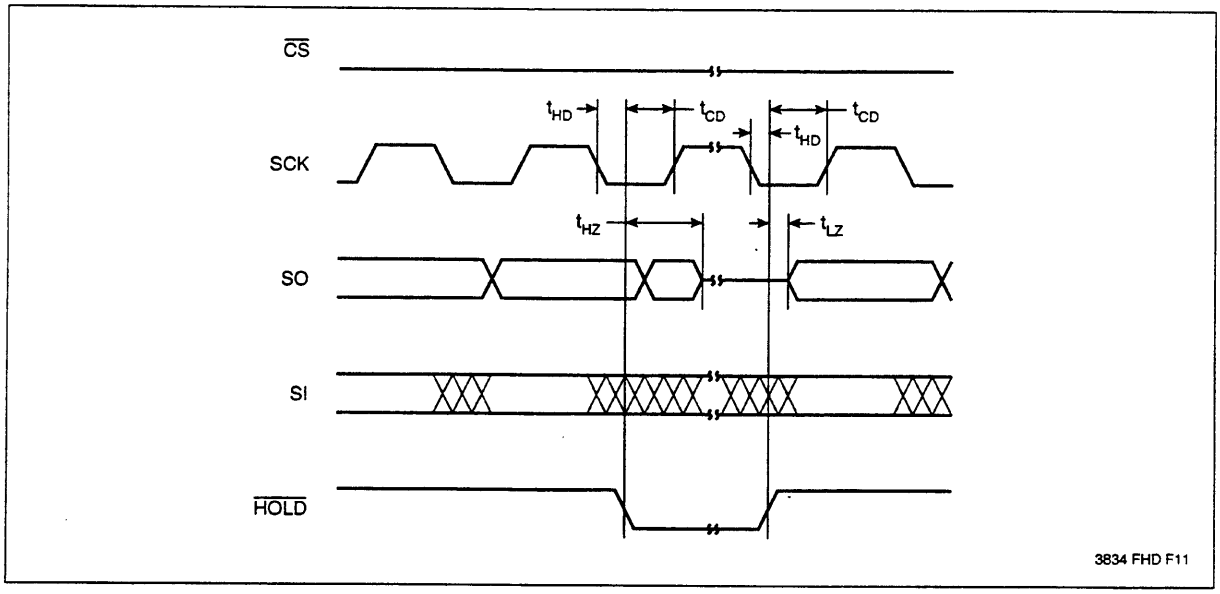


Serial Input Timing



X25020

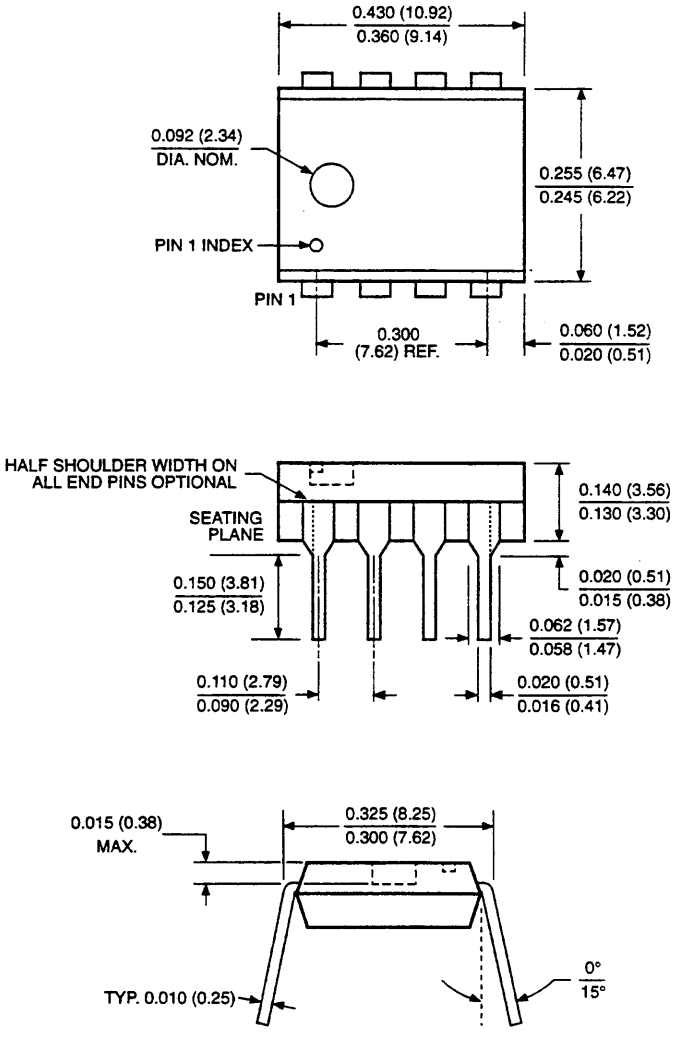
Hold Timing



X25020

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

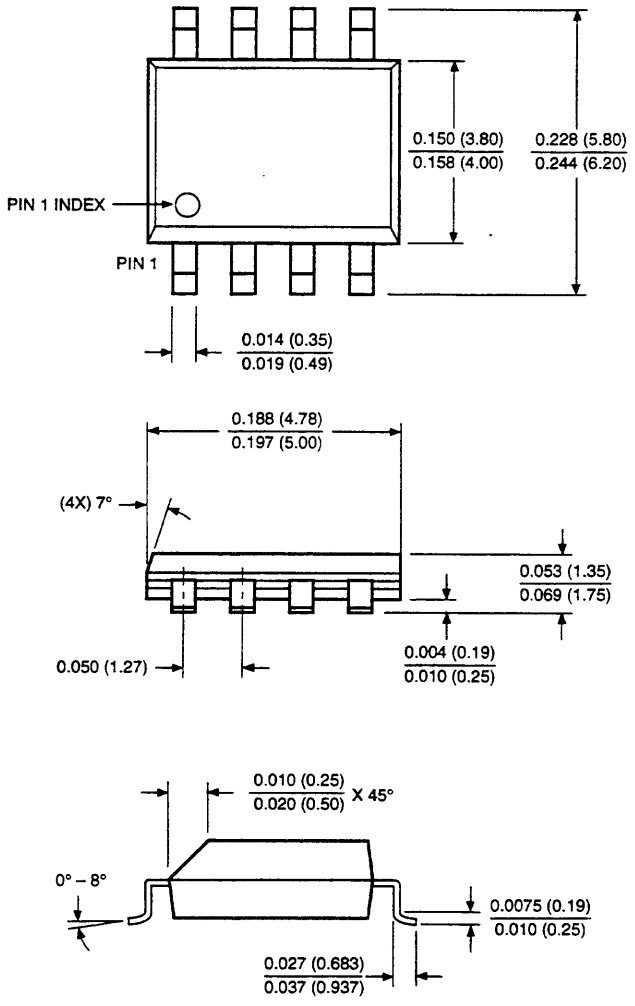


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

X25020

PACKAGING INFORMATION

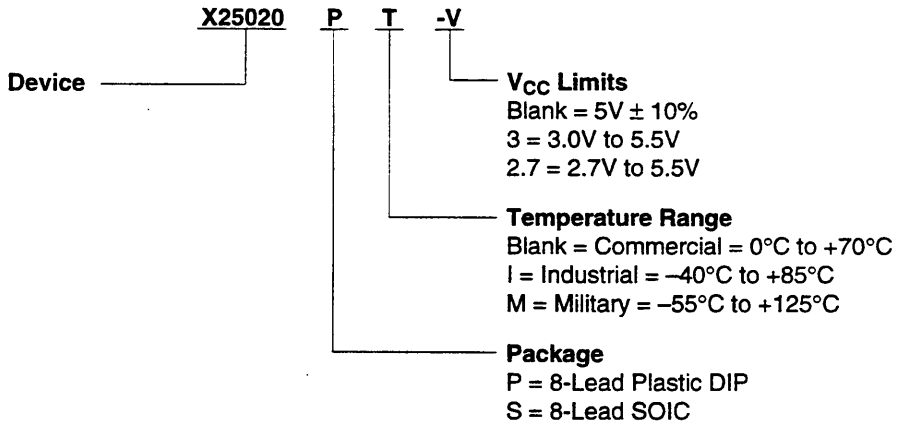
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



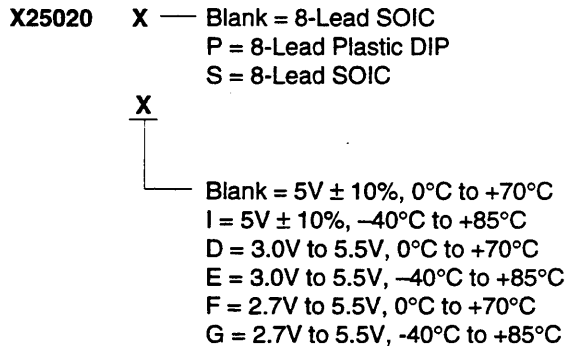
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESIS IN MILLIMETERS)

X25020

ORDERING INFORMATION



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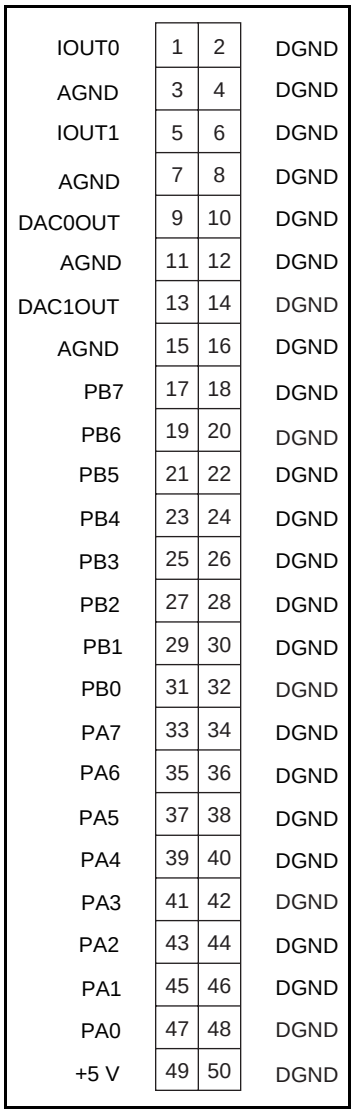
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Appendix C
Connector Block Pin Map

This appendix gives the pin assignments for the CB-50 LP or CB-50 I/O connector blocks when using the PSH27-50F-D1 with the DAQCard-AO-2DC.

If you are using the CB-50 LP or CB-50 I/O connector block and the PSH27-50F-D1 cable with the DAQCard-AO-2DC, the signals will not map at the same pin numbers as the pin numbers shown for the CB-50 I/O connector block for the PC-AO-2DC. For these pin numbers refer to Figure C-1.

Note: ***Using the PSH27-50F-D1 cable with the DAQCard-AO-2DC is not recommended because the PSH27-50F-D1 design is optimized for the DAQCard-DIO-24.***



IOUT0	1	2	DGND
AGND	3	4	DGND
IOUT1	5	6	DGND
AGND	7	8	DGND
DAC0OUT	9	10	DGND
AGND	11	12	DGND
DAC1OUT	13	14	DGND
AGND	15	16	DGND
PB7	17	18	DGND
PB6	19	20	DGND
PB5	21	22	DGND
PB4	23	24	DGND
PB3	25	26	DGND
PB2	27	28	DGND
PB1	29	30	DGND
PB0	31	32	DGND
PA7	33	34	DGND
PA6	35	36	DGND
PA5	37	38	DGND
PA4	39	40	DGND
PA3	41	42	DGND
PA2	43	44	DGND
PA1	45	46	DGND
PA0	47	48	DGND
+5 V	49	50	DGND

Figure C-1. CB-50 LP and CB-50 Pin Assignments for the DAQCard-AO-2DC Using the PSH27-50F-D1 Cable

Appendix D
Register-Level Programming

This document describes in detail the address and function of each of the PC-AO-2DC and DAQCard-AO-2DC registers.

Note: ***If you plan to use a programming software package such as NI-DAQ or LabWindows/CVI with your PC-AO-2DC and DAQCard-AO-2DC, you need not read this chapter.***

Base I/O Address Selection

♦ PC-AO-2DC

You can configure your PC-AO-2DC board to use base addresses in the range of 100 to 3E0 hex. Your PC-AO-2DC board occupies 32 bytes of address space and must be located on a 32-byte boundary. Therefore, valid addresses include 100, 120, 140, ..., 3C0, 3E0 hex. This selection is software configured and does not require you to manually change any settings on the board.

The PC-AO-2DC board is fully compatible with the industry standard Intel-Microsoft Plug and Play Specification version 1.0a. A Plug and Play system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers.

There are different ways of assigning the base address to your board:

- Windows 95 automatically assigns the base address.
- You can use a standard configuration utility like Intel ISA Configuration Utility (ICU). ICU dynamically assigns the base address to your board when you boot up the computer. You can also lock the board resources when you use ICU. For additional information on ICU, contact Intel Corporation for a copy of Plug and Play Specification version 1.0a.
- You can use `DAQCONF` or `WDAQCONF` to assign the board resources. If a standard configuration utility is present in the system, you will not be able to modify the board resources.

♦ DAQCard-AO-2DC

- If you are using a PC, you can use Windows 95, `DAQCONF`, or `WDAQCONF` to assign the device resources. If a standard configuration utility is present in the system, you will not be able to modify the device resources. Consult the document, *PCMCIA Card and Socket Services Specifications*, which explains how to configure a card using system-level calls. Request an I/O window, an interrupt level, and a configuration. In the configuration, set the configuration index to 01 hex for normal operation.

- If you are using a Mac, refer to your NI-DAQ for Macintosh documentation for PCMCIA card configuration information. Consult the document, *PCMCIA Card and Socket Services Specifications*, which explains how to configure a card using system-level calls, and the *PC Card Development Kit* (available from Apple through APDA), which explains how to interface with the Apple PC Card Manager software that is part of your PC Card expansion interface. Request a configuration and an I/O window. In the configuration, set the configuration index to 01 hex for normal operation.

Register Map

Table D-1 gives the register map for the PC-AO-2DC and DAQCard-AO-2DC.

Table D-1. PC-AO-2DC and DAQCard-AO-2DC Register Map

Register Name	Offset Address (Hex)	Type	Size
Configuration and Calibration Register Group			
Command Register 1	01	Write-only	8-bit
Command Register 2	0E	Write-only	8-bit
Calibration Command Register 3	1C	Write-only	8-bit
Calibration EEPROM Register	1D	Read-only	8-bit
Analog Output Register Group			
DAC0 Low-Byte Register	04	Write-only	8-bit
DAC0 High-Byte Register	05	Write-only	8-bit
DAC1 Low-Byte Register	06	Write-only	8-bit
DAC1 High-Byte Register	07	Write-only	8-bit
82C55A Digital I/O Register Group			
Port A Register	10	Read-and-write	8-bit
Port B Register	11	Read-and-write	8-bit
Digital Control Register	13	Write-only	8-bit

Register Description

Table D-1 divides the PC-AO-2DC and DAQCard-AO-2DC registers into three different register groups. A bit description of each register is included later in this chapter. The Configuration and Calibration Register Group controls the overall operation of the PC-AO-2DC or DAQCard-AO-2DC. The Analog Output Register Group accesses the two 12-bit DACs. The Digital I/O Register Group consists of the three registers of the onboard 82C55A PPI integrated circuit used for digital I/O.

Register Description Format

The remainder of this chapter discusses each of the PC-AO-2DC and DAQCard-AO-2DC registers in the order shown in Table D-1. Each register group section begins with a brief introduction, followed by a detailed bit description of each register on the AO-2DC devices. Each register description gives the address, type, word size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the MSB (bit 7 for an 8-bit register) shown on the left, and the LSB (bit 0) shown on the right. Each bit is represented by a square with the bit name inside. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic). An X represents a *don't care* state; in other words, the logic may be digital 0 or 1 and this bit should be ignored.

Configuration and Calibration Register Group

The four registers making up the Configuration and Calibration Register Group allow general control of the PC-AO-2DC and DAQCard-AO-2DC D/A circuitry. Command Register 1 and Command Register 2 contain bits that control the operation modes of the D/A circuitry. Command Register 3 is for writing to the EEPROM. The EEPROM Register gives access to the EEPROM. When you start up your PC, all bits of the Command Registers are cleared except Command Register 2, where bits 2 and 3 are set during power up.

Bit descriptions for the registers in the Configuration and Calibration Register Group are given on the following pages.

Command Register 1

Command Register 1 contains two bits that control PC-AO-2DC and DAQCard-AO-2DC analog output modes.

Address: Base address + 01 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
0	0	2SDAC1	2SDAC0	0	0	0	0

Bit	Name	Description
7, 6, 3–0	0	Write zeroes to these bits.
5	2SDAC1	Two’s complement DAC1—This bit selects the binary coding scheme used for the DAC1 data. If this bit is set, a two's complement binary coding scheme is used for interpreting the 12-bit data. Two's complement is useful if a bipolar output range is selected. If this bit is cleared, a straight binary coding scheme is used. Straight binary is useful if a unipolar output range is selected.
4	2SDAC0	Two’s complement DAC0—This bit selects the binary coding scheme used for the DAC0 data. If this bit is set, a two's complement binary coding scheme is used for interpreting the 12-bit data. Two's complement is useful if a bipolar output range is selected. If this bit is cleared, a straight binary coding scheme is used. Straight binary is useful if a unipolar output range is selected.

Command Register 2

Command Register 2 configures the D/A circuitry.

Address: Base address + 0E (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
0	0	0	0	DAC1UNI/BI*	DAC0UNI/BI*	0	0

Bit	Name	Description
7–4,	0	Write zeroes to these bits.
3	DAC1UNI/BI*	DAC1 Unipolar/Bipolar—This bit sets the analog voltage output range for DAC1. Set this bit to configure DAC1 for a unipolar (0 to +10 V) output voltage range. Clear this bit to configure DAC1 for bipolar (-5 to +5 V) output voltage range.
2	DAC0UNI/BI*	DAC0 Unipolar/Bipolar—This bit sets the analog voltage output range for DAC0. Set this bit to configure DAC0 for a unipolar (0 to +10 V) output voltage range. Clear this bit to configure DAC0 for bipolar (-5 to +5 V) output voltage range.

Note: ***At power up, both the DACs are configured for unipolar output voltage range.***

Command Register 3

This register is used to write to the onboard Calibration EEPROM.

Address: Base address + 1C (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
EEPROMCS	SDATA	SCLK	0	0	WRTPRT	0	0

Bit	Name	Description
7	EEPROMCS	EEPROM Chip Select—This bit enables and disables the EEPROM. You can enable the EEPROM for both read and write operations by setting this bit. You can disable the EEPROM by clearing this bit.
6	SDATA	Serial Data—This bit is a serial input for the calibration EEPROM.
5	SCLK	Serial Clock—This bit is a serial clock for the calibration EEPROM. A low-to-high transition of this bit clocks data into the EEPROM (during a write operation). A high-to-low transition of the bit clocks data out of the EEPROM (during a read operation).
4, 3, 1, 0	0	Write zeroes to these bits.
2	WRTPRT	Write Protect—This bit controls the write protect input signal for the EEPROM. When you set this bit, normal write operations are enabled. When you clear this bit, write operations are disabled.

Note: ***To program the X25020 EEPROM, refer to the data sheets in Appendix B,*** *X25020 Data Sheet****.***

Calibration EEPROM Register

The Calibration EEPROM Register gives access to the output of the EEPROM.

Address: Base address + 1D (hex)

Type: Read-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	PROMOUT

Bit	Name	Description
7–1	X	Don't care bit—You can mask these bits when reading the EEPROM.
0	PROMOUT	EEPROM Output—This bit allows access to the serial output pin of the EEPROM. During calibration procedures, the calibration data is read from the EEPROM through PROMOUT.

Note: ***To program the X25020 EEPROM, refer to the data sheets in Appendix B,*** *X25020 Data Sheet.*

Analog Output Register Group

The four registers making up the Analog Output Register Group are used for loading the two 12-bit DACs in the two analog output channels. DAC0 controls analog output Channel 0. DAC1 controls analog output channel 1. These DACs should be written to individually.

The DAC in each analog output channel generates a voltage proportional to the input V_{ref} multiplied by the digital code loaded into the DAC. The DACs have an 8-bit loading interface. Each DAC can be loaded with a 12-bit digital code by writing first to the low byte and then to the high byte. The voltage outputs from the two DACs are updated at the PC-AO-2DC or DAQCard-AO-2DC I/O connector at the DAC0OUT and DAC1OUT pins as soon as the high byte is written to the DAC*x* registers.

Bit descriptions of the registers making up the Analog Output Register Group are given on the following page.

Programming the Analog Outputs

Voltage Outputs

Use the pseudocode for generating a desired voltage at the output of a channel or refer to the *Programming Example* section later in this appendix:

1. Write to the Command Register 1 to select the binary coding scheme to be used for DAC data. You can choose the two's complement scheme for bipolar outputs and straight binary is used for unipolar output.

2. Select the polarity of the DAC by writing to Command Register 2. This will select unipolar output or bipolar output.

   Note: ***Power-up default is unipolar output on both channels.***

3. Perform calibration if desired. Refer to Appendix E, *Calibration*, for more information. You will have to write to Calibration Command Register 3 to write to the EEPROM.

4. Read the calibration coefficients and calculate the binary pattern to be written to the DAC to generate the desired voltage output.

   Note: ***Refer to Appendix E,*** *Calibration****, to find the formula to calculate digital value to be written to DAC for a desired voltage.***

5. Write the LSB of the digital value to the DAC0L/DAC1L and then write the MSB of the digital value to the DAC0H/DAC1H. When you finish writing to DAC*x*H, the output will be updated.

Current Outputs

The pseudocode is identical to that for voltage outputs except Step 2, where the unipolar range should always be selected for current outputs.

DAC0 Low-Byte (DAC0L), DAC0 High-Byte (DAC0H), DAC1 Low-Byte (DAC1L), and DAC1 High-Byte (DAC1H) Registers

Writing to DAC0L and then to DAC0H loads the analog output channel 0. Writing to DAC1L and then to DAC1H loads the analog output channel 1. The voltage generated by both of the analog output channels is updated immediately after either DAC*x*H register is written to.

Address:	Base address + 04 (hex)	Load DAC0 low byte.
	Base address + 05 (hex)	Load DAC0 high byte.
	Base address + 06 (hex)	Load DAC1 low byte.
	Base address + 07 (hex)	Load DAC1 high byte.

Type: Write-only (all)

Word Size: 8-bit (all)

Bit Map:

DAC*x*H

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8

{——————Sign Extension Bits——————}

DAC*x*L

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
DAC*x*H		
7–4	D<15..12>	Data bits 15 through 12—These bits are set to zero in straight binary mode and to sign extension in two's complement mode.
3–0	D<11..8>	Data bits 11 through 8—These four bits are loaded into the specified DAC high byte.
DAC*x*L		
7–0	D<7..0>	Data bits 7 through 0—These eight bits are loaded into the specified DAC low byte. The low byte should be loaded first, followed by corresponding high byte loading.

82C55A Digital I/O Register Group

Digital I/O on the PC-AO-2DC and DAQCard-AO-2DC uses an 82C55A integrated circuit. The 82C55A is a general-purpose programmable peripheral interface (PPI). Two ports, port A and port B, are used in the PC-AO-2DC and DAQCard-AO-2DC. These ports are programmed as two groups of eight signals for either input or output.

Bit descriptions for the registers in the Digital I/O Register Group are given on the following pages.

Note: ***Interrupts are not supported on PC-AO-2DC or DAQCard-AO-2DC.***

Port A Register

Reading the Port A Register returns the logic state of the eight digital I/O lines constituting port A, that is, PA<0..7>. If port A is configured for output, the Port A Register can be written to in order to control the eight digital I/O lines constituting port A. See *Programming the Digital I/O Circuitry* later in this appendix for information on how to configure port A for input or output.

Address: Base address + 10 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data bits 7 through 0—These bits are 8-bit port A data.

Port B Register

Reading the Port B Register returns the logic state of the eight digital I/O lines constituting port B, that is, PB<0..7>. If port B is configured for output, the Port B Register can be written to in order to control the eight digital I/O lines constituting port B. See *Programming the Digital I/O Circuitry* later in this appendix for information on how to configure port B for input or output.

Address: Base address + 11 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7–0	D<7..0>	Data bits 7 through 0—These bits are 8-bit port B data.

Digital Control Register

The Digital Control Register can be used to configure port A and port B as inputs or outputs. See *Programming the Digital I/O Circuitry* later in this appendix for a description of the individual bits in the Digital Control Register.

Address: Base address + 13 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
CW7	CW6	CW5	CW4	CW3	CW2	CW1	CW0

Bit	Name	Description
7–0	CW<7..0>	Control Word 7 through 0—These bits are 8-bit control word data.

Programming the Digital I/O Circuitry

The PC-AO-2DC and DAQCard-AO-2DC support only Mode 0 basic I/O operations with ports A and B of the 82C55A PPI. With Mode 0, no handshaking is required; data is simply written to or read from a specified port. Port A and port B can be used for either input or output.

Control Words

Both port A and port B can be assigned either as an input port or an output port. Figure D-1 shows the control-word format used to completely program the 82C55A on the PC-AO-2DC and the DAQCard-AO-2DC.

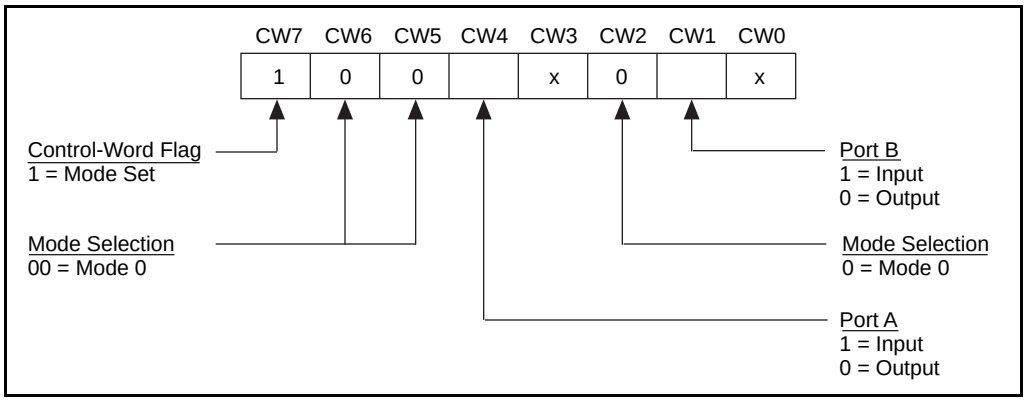


Figure D-1. Control Word Format

The four possible I/O configurations are shown in Table D-2. Notice that bit 7 of the control word is set when programming the mode of operation of each port.

Table D-2. Digital I/O Configurations

Control Word CW <7..0>	Port A	Port B
1000X00X	Output	Output
1000X01X	Output	Input
1001X00X	Input	Output
1001X01X	Input	Input

Use the following pseudocode for digital I/O on port A or port B or refer to the *Programming Example* section:

1. Write the appropriate digital value to the Digital Control Register to configure that port as input or output.
2. Write the desired digital value to the corresponding port register to generate the control signals at that port.

   Or, read the port to read the logic level present at that port input.

   Note: ***Configuring one of the ports resets the other port, so you may want to configure both ports before starting the digital I/O.***

Programming Example

The following example shows how to configure the 82C55A for various combinations of mode 0 input and output. This code is strictly an example and is not intended to be used without modification in a practical situation. The base address used may not correspond to the base address of the card in your system. For more information, refer to the *Base I/O Address Selection* section earlier in this appendix.

```
Main() {

/* Set PC to 1 if you are using a PC, or set MAC to 1 if you are using a
Mac.*/
#define         PC                0
#define         MAC               0

/* If MAC = 1, set base address and define rd and wrt. */
#if             MAC
#define         BASE_ADDRESS      0xa0000000L
#define         rd(a)     ((unsigned char) *((unsigned char *) (a)))
#define         wrt(a,d)  (*((unsigned char *) (a)) = ((unsigned char) (d)))

/* Else if PC = 1, set base address and define rd and wrt. */
#elif           PC
#define         BASE_ADDRESS      0x0220
#define         rd(a)     ((unsigned char) inp(((unsigned int) (a))))
#define         wrt(a,d)  (outp(((unsigned int) (a)), ((unsigned char) (d))))
#end


#define PORTAoffset       0x10      /* Offset for port A */
#define PORTBoffset       0x11      /* Offset for port B */
#define PORTCoffset       0x12      /* Offset for port C */
#define CNFGoffset        0x13      /* Offset for CNFG   */

unsigned long porta, portb, portc, cnfg
char valread;                    /* Variable to store data read from a port*/
/*  Calculate register addresses. */
porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;

/* EXAMPLE 1*/
wrt(cnfg,0x80);                  /* Ports A, B, and C are outputs. */
wrt(porta,0x12);                 /* Write data to port A. */
wrt(portb,0x34);                 /* Write data to port B. */
wrt(portc,0x56);                 /* Write data to port C. */

/* EXAMPLE 2*/
wrt(cnfg,0x90);                  /* Port A is input; ports B and C */
                                 /* are outputs. */
wrt(portb,0x22);                 /* Write data to port B. */
wrt(portc,0x55);                 /* Write data to port C. */
valread = rd(porta);             /* Read data from port A. */
```

```
/* EXAMPLE 3 */
wrt(cnfg,0x82);                 /* Ports A and C are outputs; port B */
                                /* is an input. */

/* EXAMPLE 4 */
wrt(cnfg,0x89);                 /* Ports A and B are outputs; port C */
                                /* is an input. */

}
```

Appendix E
Calibration

This appendix discusses the calibration procedures for the PC-AO-2DC and DAQCard-AO-2DC. You can perform calibration only at the register level.

Note: ***Neither NI-DAQ nor LabVIEW supports calibration for the AO-2DC devices.***

Overview

The PC-AO-2DC and DAQCard-AO-2DC have been calibrated at the factory for maximum accuracy. All output ranges have some unknown offset and gain error, which can be calibrated.

In addition, known offset and gain errors have been added to ensure that each range can output voltages or currents throughout the nominal output range. The current outputs cannot produce negative currents and thus have a different output characteristic. Typical output characteristics for a channel in unipolar voltage, bipolar voltage, and current output are shown in Figure E-1.

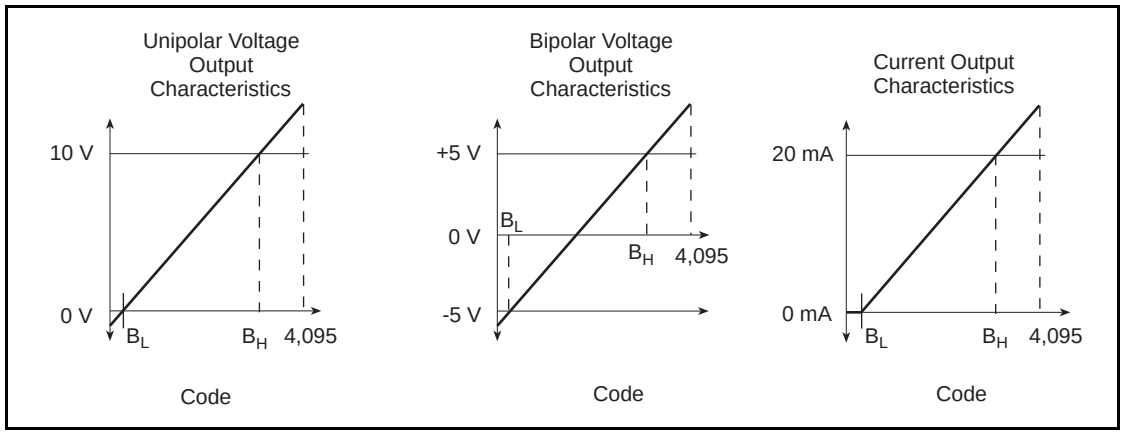


Figure E-1. PC-AO-2DC and DAQCard-AO-2DC Output Characteristics

The graphs in Figure E-1 show the values B_L and B_H. B_L is the code that you write to the DAC when you want the channel to output its nominal minimum output, which is 0 V for unipolar voltage output, -5 V for bipolar voltage output, and 0 mA for current output. B_H is the code that you write to the DAC when you want the channel to output its nominal maximum output, which is 10 V (actually 9.9975 V) for unipolar voltage output, +5 V (actually 4.9987 V) for bipolar voltage output, and 20 mA (actually 19.9951 V) or current output. With these actual values, you can use the following formula to compute the bit value to write to the DAC to get any output within the nominal range:

$$B_U = B_L + (O_U - O_L) * (B_H - B_L)/(O_H - O_L)$$

where

B_L = bit pattern you write to get the low value of the range
B_H = bit pattern you write to get the high value of the range
O_L = low value of the range (-5 V, 0 V, or 0 mA)
O_H = high value of the range (4.9987 V, +9.9975 V, or 19.9951 mA)
O_U = output you want
B_U = necessary bit pattern you write to get O_U (rounded to the nearest integer)

Each channel and each range has different values for B_L and B_H. Each B_L and B_H is stored in EEPROM as an LSB and MSB. There are two channels and three ranges, which makes 12 pairs of calibration constants to characterize the module. These constants are determined at the factory and stored in the onboard EEPROM. The factory constants are the numbers that National Instruments software uses to calculate bit patterns. When the module is shipped, the load constants are the same as the factory constants. Information on the structure of these tables is in the *EEPROM Map* section, later in this appendix. This appendix describes how to determine the calibration constants.

Notes: ***Never overwrite the Factory Area in the EEPROM.***

If you want to ignore software correction of the DACs, you will have to write 0 to the B_L and 4095 to the B_H for all ranges into the EEPROM. You can do this only if you do register-level programming.

Calibration Methods

Two-Point Calibration Method

With the two-point calibration method, you program a channel with two different DAC codes, measure the circuit output for each code, and calculate the calibration constants.

To calibrate the PC-AO-2DC or DAQCard-AO-2DC, perform the following steps:

1. For the range and channel that you are calibrating, write the code, C_1, to the DAC, where $0 \le C_1 \le 4{,}095$.

2. Measure the output voltage or current, O_1.

3. For the same range and channel that you are calibrating, write the code, C_2, to the DAC, where $0 \le C_2 \le 4{,}095$.

4. Measure the output voltage or current, O_2.

5. Calculate B_L from the following formula:

$$B_L = C_1 + (O_L - O_1) * (C_2 - C_1)/(O_2 - O_1)$$

where O_L is the low end of the output range (-5 V for bipolar; 0 V for unipolar; 0 mA for current output), and B_L is the necessary bit pattern to write (rounded to the nearest integer) to get O_L.

6. Calculate B_H from the following formula:

$$B_H = C_1 + (O_H - O_1)*(C_2 - C_1)/(O_2 - O_1)$$

where O_H is the high end of the output range (4.9987 V, 9.9975 V, or 19.9951 mA), and B_H is the necessary bit pattern you write (rounded to the nearest integer) to get O_H.

Voltage Calibration Method

When you calibrate a voltage output, use the codes 0 and 4,095 to achieve the best calibration with the two-point calibration method described previously. There are two reasons why 0 and 4,095 are the preferred codes.

First, when you calibrate using 0 and 4,095, you measure the transfer characteristic of the entire DAC. By choosing two points far apart, you minimize the error due to the DAC nonlinearity. In general, it is better to use two points that are far apart rather than two points that are close together. Figure E-2 illustrates why.

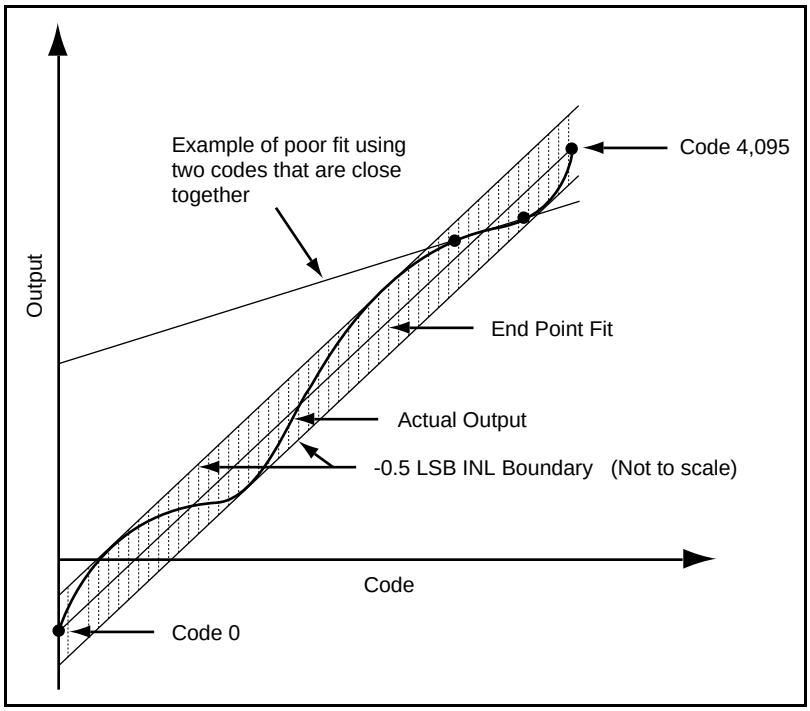


Figure E-2. DAC Characteristics

Second, the INL of the DAC is specified on an endpoint fit. The PC-AO-2DC and DAQCard-AO-2DC DACs have an INL of ±0.5 LSB. Therefore, all of the DAC outputs will fall within 0.5 LSB of the line drawn between the two endpoints, as shown in Figure E-2. If you calibrate with a point other than the endpoint, the point you measure may be up to 0.5 LSB off from the true INL curve.

When you calibrate voltage using codes 0 and 4,095, you have the following errors to account for when you output a voltage:

- Calibration constant rounding error—When you calculate B_L and B_H, you may get up to 0.5 LSB of rounding error. You can reduce this error to nearly zero by not rounding and keeping B_L and B_H as real numbers. However, when storing the constants to the EEPROM, you must round the values to the nearest integer.
- INL error—This adds another 0.5 LSB of error to the output.
- Code rounding error—When you want to output a voltage, you must write an integer bit pattern. This pattern can introduce up to 0.5 LSB of error. Most analog output devices do not include this error because it is an inherent characteristic of a DAC. However, when hardware calibration is used, the zero crossing offset can typically be trimmed to zero. You cannot do this with the PC-AO-2DC or DAQCard-AO-2DC software calibration. Therefore, the code rounding error is included in the error specification.

Your total error after calibration will be:

(1.5 LSB/4,095 LSB) * 1.020 = 0.0376% of full scale

The extra factor of 1.020 is in the formula because the actual range of the circuit is 2% larger than the nominal range. This accounts for the few LSB that you lose at the top and bottom of the range. For a particular calibration, it is more accurate to use the number $4{,}095/(B_H - B_L)$ in place of 1.020. You must also add any errors from your calibration equipment.

Current Calibration Method

When you calibrate a current output, use the two-point calibration method described previously. When you calibrate a current output, you cannot use 0 as a code. Because the current output curve has a bend (see Figure E-1), you must use two codes that are on the sloped portion of the curve. You should use 4,095 as the upper code. For the lower code, using the code 255 is recommended for simplicity. This code is guaranteed to be on the sloped portion of the curve but is still far away from 4,095. You can iterate the calibration procedure and use a code a few bits above the B_L, but this only improves your accuracy by, at most, 7 ppm of full scale.

The sources of error for current calibration are the same as for voltage calibration, plus an additional error for using a point that is not an endpoint. This additional error is:

$0.5 \text{ LSB} * (4{,}095 - B_L) / (4{,}095 - C_1), C_1 - B_L$

For C_1 = 255 and a typical B_L of 37, the additional error is approximately 0.53 LSB. Your total error after calibration will be:

(2.03 LSB/4,095 LSB) * 1.020 = 0.05% of full scale

The extra factor of 1.020 is in the formula because the actual range of the circuit is 2% larger than the nominal range. This accounts for the few LSB that you lose at the top and bottom of the range. For a particular calibration, it is more accurate to use the number 4,095/(B_H - B_L) instead of 1.020. You must also add any errors from your calibration equipment.

Note: ***In current output mode the DAC should be configured for unipolar output.***

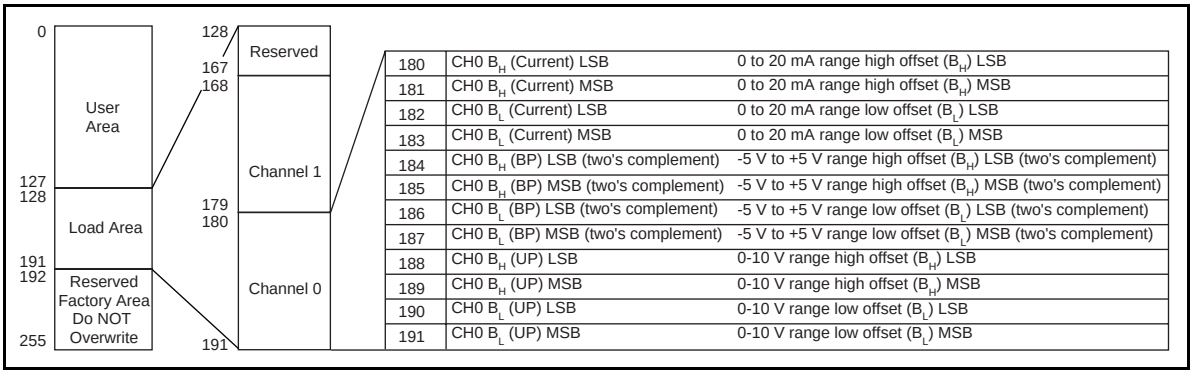
Measurement Technique

When you measure voltage or current from the PC-AO-2DC or DAQCard-AO-2DC, you should use a voltmeter or current meter that integrates its readings to reduce errors due to noise. If you use a DAQ device that does not use an integrating ADC, you should average a few hundred readings. Remember that any errors from your calibration measurements must be added to the error described in the calibration sections.

EEPROM Map

Figure E-3 shows the EEPROM map on the PC-AO-2DC and DAQCard-AO-2DC. The load area contains a copy of the factory calibration constants. You can recalibrate the AO-2DC devices and store the calibration constants in the user area. You can also use the user area for scratch work. You can do this only if you use register-level programming.

Note: ***Do not overwrite the reserved factory area. NI-DAQ uses the factory area to read the constants for the device calibration. The factory area is software protected.***



180	CH0 B_H (Current) LSB	0 to 20 mA range high offset (B_H) LSB
181	CH0 B_H (Current) MSB	0 to 20 mA range high offset (B_H) MSB
182	CH0 B_L (Current) LSB	0 to 20 mA range low offset (B_L) LSB
183	CH0 B_L (Current) MSB	0 to 20 mA range low offset (B_L) MSB
184	CH0 B_H (BP) LSB (two's complement)	-5 V to +5 V range high offset (B_H) LSB (two's complement)
185	CH0 B_H (BP) MSB (two's complement)	-5 V to +5 V range high offset (B_H) MSB (two's complement)
186	CH0 B_L (BP) LSB (two's complement)	-5 V to +5 V range low offset (B_L) LSB (two's complement)
187	CH0 B_L (BP) MSB (two's complement)	-5 V to +5 V range low offset (B_L) MSB (two's complement)
188	CH0 B_H (UP) LSB	0-10 V range high offset (B_H) LSB
189	CH0 B_H (UP) MSB	0-10 V range high offset (B_H) MSB
190	CH0 B_L (UP) LSB	0-10 V range low offset (B_L) LSB
191	CH0 B_L (UP) MSB	0-10 V range low offset (B_L) MSB

Figure E-3. EEPROM Map of the PC-AO-2DC and DAQCard-AO-2DC

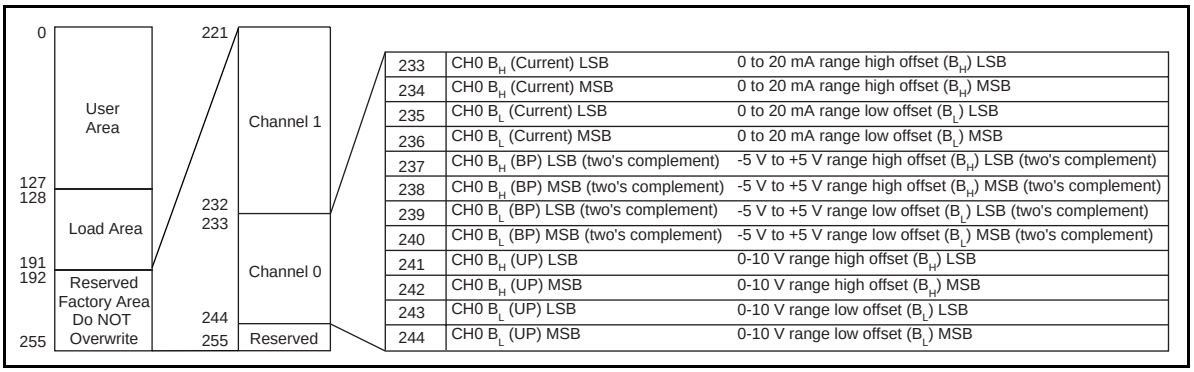
You can calibrate your AO-2DC with new calibration constants and still use NI-DAQ for your application needs. Use the following procedure to do this.

1. You must unprotect the upper quadrant of your Calibration EEPROM. You can do this by writing to the Write Status Register (WRSR). Refer to the X25020 data sheet in Appendix B for additional information.

2. Perform calibration and store the constants in the factory area.

   Warning: ***You will lose all the factory calibration constants if you store the constants in the factory area. National Instruments is not responsible for reprogramming your EEPROM if you disturb the factor calibration area of the EEPROM.***

Figure E-4 shows the memory map for the factory area.



233	CH0 B_H (Current) LSB	0 to 20 mA range high offset (B_H) LSB
234	CH0 B_H (Current) MSB	0 to 20 mA range high offset (B_H) MSB
235	CH0 B_L (Current) LSB	0 to 20 mA range low offset (B_L) LSB
236	CH0 B_L (Current) MSB	0 to 20 mA range low offset (B_L) MSB
237	CH0 B_H (BP) LSB (two's complement)	-5 V to +5 V range high offset (B_H) LSB (two's complement)
238	CH0 B_H (BP) MSB (two's complement)	-5 V to +5 V range high offset (B_H) MSB (two's complement)
239	CH0 B_L (BP) LSB (two's complement)	-5 V to +5 V range low offset (B_L) LSB (two's complement)
240	CH0 B_L (BP) MSB (two's complement)	-5 V to +5 V range low offset (B_L) MSB (two's complement)
241	CH0 B_H (UP) LSB	0-10 V range high offset (B_H) LSB
242	CH0 B_H (UP) MSB	0-10 V range high offset (B_H) MSB
243	CH0 B_L (UP) LSB	0-10 V range low offset (B_L) LSB
244	CH0 B_L (UP) MSB	0-10 V range low offset (B_L) MSB

Figure E-4. Factory Area of the EEPROM Map

You can now use NI-DAQ with your new calibration constants.

Appendix F
Power-Management Modes

This appendix describes the power-management modes of the DAQCard-AO-2DC.

- Normal Mode—This is the normal operating mode of the DAQCard-AO-2DC in which all the circuits are fully functional. This mode draws about 89 mA from the 5 V supply (about 445 mW).

- Power-down Mode—In this mode, the digital circuitry is nonfunctional. The analog output circuits are powered down by setting the PWRDOWN bit in the PCMCIA Card Configuration and Status Register. The analog supplies are reduced to zero; negligible power is supplied to the analog circuits. This mode draws about 26 mA from the 5 V supply (about 130 mW).

  If you are using a PC, you can set the PWRDOWN bit by using the `DAQPOWER` utility that is shipped with NI-DAQ. Use `DAQPOWER-D` to power down and `DAQPOWER-U` to power up the DAQCard-AO-2DC. This utility is also available in Windows and is installed whenever you install NI-DAQ.

Table F-1 shows the effects of different power-management modes on the DAQCard-AO-2DC circuits.

Table F-1. DAQCard-AO-2DC Power-Management Modes

	Normal Mode	**Power-Down Mode**
Analog Output	Functional. Defaults to unipolar (0 to 10 V). Output of each DAC remains close to 0 V until the first update is performed on that DAC. Short circuit protected to 80 mA. DC impedance = 0.5 Ω.	Nonfunctional. Draws negligible power. Output of each DAC is ideally 0 V, but may get some negligible value. Short circuit protected to 80 mA. Assume impedance = 0.5 Ω.
Calibration Circuitry	Functional. Software calibration.	Nonfunctional.
Digital I/O	Functional. Defaults to mode 0 input for all ports. Protected from -0.5 to 5.5 V.	Nonfunctional.

Appendix G
PCMCIA Questions and Answers

This appendix contains a list of common questions and answers relating to PCMCIA card operation. The questions are grouped according to the type of information requested. You may find this information useful if you are having difficulty with the PCMCIA system software configuration.

Configuration

1. Do I need to use my PCMCIA configuration utility to configure the National Instruments PCMCIA cards?

No. Use the configuration utilities included with the NI-DAQ driver software to properly configure your card. If you are using Windows 95, it will automatically configure your card.

2. What should I do if my computer does not have Card and Socket Services version 2.0 or later?

Contact the manufacturer of your computer or of your PCMCIA adapter and request the latest Card and Socket PCMCIA driver. Our NI-DAQ software will work with any Card and Socket Service driver that is compliant to version 2.0 or later.

Operation

1. My PCMCIA card works when inserted before power-on time, but it does not work when hot inserted. What is wrong?

You may have an interrupt conflict. If you have a utility such as `MSD.EXE`, run it to determine the allocated interrupts, then refer to question 5 in the *Resources* section. `MSD.EXE` is usually shipped with Microsoft Windows.

2. My computer locks up when I use a PCMCIA card. What should I do?

This usually happens because Card Services allocated an unusable interrupt level to the PCMCIA card. For example, on some computers, interrupt level 11 is not routed to PCMCIA cards. If Card Services is not aware of this, it may assign interrupt 11 to a PCMCIA card even though the interrupt is not usable. When a call uses the interrupt, the interrupt never occurs, and the computer locks up waiting for a response. For information about how to locate an interrupt that is free to be used, refer to question 4 in the *Resources* section.

3. Is there a way I can conserve power on my PCMCIA card when it is not in use?

Yes. If you are using NI-DAQ for PC compatibles version 4.8.0 or later, a DOS utility called DAQPOWER.EXE will switch all National Instruments PCMCIA cards between normal mode and power-down mode. Power-up and power-down icons are also installed for Windows users to access either of these two power-management modes.

Resources

1. How do I determine if I have a memory conflict?

If no PCMCIA cards are working at all, it is probably because a memory window is not usable. Card Services uses a 4 KB memory window for its own internal use. If the memory cannot be used, then Card Services cannot read the Card Information Structure (CIS) from the card's EPROM, which means it cannot identify cards.

There are two different methods you can use when Card Services has a problem reading the CIS. First, you can determine which memory window Card Services is using, and then exclude that window from use by Card Services and/or the memory manager. Second, you can attempt to determine all of the memory that Card Services can possibly use and then exclude all but that memory from use by Card Services.

2. How do I determine all of the memory that Card Services can use?

One way to find out which memory addresses Card Services can use is to run a utility such as `MSD.EXE` that scans the system and tells you how the system memory is being used. For example, if you run such a memory utility and it tells you that physical addresses C0000 to C9FFF are being used for ROM access, then you know that C8000–D3FFF is an invalid range for Card Services and should be changed to CA000–D3FFF.

3. How can I find usable I/O addresses?

Finding usable I/O addresses is done by trial and error. Of the three resources used—memory, I/O, interrupts—I/O conflicts will be low. You can use the DAQ configuration utility to diagnose I/O space conflicts. When you have configured the utility for a particular I/O space, save the configuration. If there is a conflict, the configuration utility will report an error describing the conflict.

4. How do I find usable interrupt levels?

Some utilities, such as `MSD.EXE`, will scan the system and display information about what is using hardware interrupts. If you have such a utility, you can run it to determine what interrupts Card Services can use. Card Services needs an interrupt for itself as well as one interrupt for each PCMCIA socket in the system. For example, in a system with two PCMCIA sockets, at least three interrupts should be allocated for use by Card Services.

Keep in mind that utilities such as `MSD.EXE` will sometimes report that an interrupt is in use when it really is not. For example, if a PC has one serial port, COM1, and one parallel port, LPT1, you know that IRQs 4 and 7 are probably in use. In general, IRQ5 is used for LPT2, but if the computer does not have two parallel ports, IRQ5 should be usable. IRQ3 is used for COM2, but if the computer has only has one serial port, IRQ3 should be usable.

5. I run a memory utility, and it appears there is no memory available for Card Services. What should I do?

You should remove your memory manager by commenting it out of the `CONFIG.SYS` file. Next, you can rerun the memory utility. Memory managers often consume an enormous amount of memory, and you will need to determine what memory is really usable by Card Services. When you have determined what memory is available for Card Services, reinstall your memory manager and make the necessary changes to provide Card Services with the memory needed. We suggest that you use the minimum amount of memory for Card Services, namely 4 to 12 KB, which frees more memory for the memory manager.

Resource Conflicts

1. How do I resolve conflicts between my memory manager and Card Services?

Card Services can usually use memory space that is not being used for real RAM on the system. Even when this is the case, you should still exclude the memory addresses used by Card Services from use by any memory manager that may be installed.

Appendix H
Customer Communication

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve technical problems you might have as well as a form you can use to comment on the product documentation. Filling out a copy of the *Technical Support Form* before contacting National Instruments helps us help you better and faster.

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Company _____

Address _____

_____

Fax (___)_____ Phone (___)_____

Computer brand _____ Model _____ Processor _____

Operating system _____

Speed _____MHz RAM _____MB Display adapter _____

Mouse _____yes _____no Other adapters installed _____

Hard disk capacity _____MB Brand _____

Instruments used _____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is _____

_____

_____

_____

List any error messages _____

_____

_____

_____

The following steps will reproduce the problem _____

_____

_____

PC-AO-2DC/DAQCard-AO-2DC Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

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- Base I/O Address of PC-AO-2DC or DAQCard-AO-2DC (Factory Setting–in Hex) _____
- Analog Output Channel 0 Configuration (Factory Setting - Unipolar) _____
- Analog Output Channel 1 Configuration (Factory Setting - Unipolar) _____
- NI-DAQ, LabVIEW, or LabWindows/CVI Version _____
- Software Version _____

Other Products

- Microprocessor _____
- Clock Frequency _____
- Computer Make and Model _____
- Type of Video Board Installed _____
- Operating System and Version _____
- Programming Language _____
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Edition Date: **April 1996**

Part Number: **320919B-01**

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Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{12}

°	degrees
Ω	ohms
/	per
%	percent
±	plus or minus
+5 V	+5 V signal
2SDAC0	two's complement DAC0 bit
2SDAC1	two's complement DAC0 bit
A	amperes
AC	alternating current
A/D	analog-to-digital
ADC	A/D converter
AGND	analog ground signal
AO	analog output
API	application programming interface
AWG	American Wire Gauge
BIOS	basic input/output system
BP	bipolar
C	Celsius
CW	control word bit
D	data bit
D/A	digital-to-analog
DAC	D/A converter
DAC0H	DAC0 high-byte register
DAC0L	DAC0 low-byte register
DAC0OUT	voltage output signal
DAC0UNI/B1*	DAC0 unipolar/bipolar bit
DAC1H	DAC1 high-byte register
DAC1L	DAC1 low-byte register
DAC1UNI/B1*	DAC1 unipolar/bipolar bit
DAQ	data acquisition
DC	direct current

DGND	digital ground signal
DIO	digital I/O
DLL	dynamic link library
DMA	direct memory access
DNL	differential nonlinearity
EEPROMCS	EEPROM chip select bit
EISA	Extended Industry Standard Architecture
GND	ground signal
hex	hexadecimal
Hz	hertz
IDE	Integrated Development Environment
in.	inch
INL	integral nonlinearity
I/O	input/output
I_{OH}	current, output high
I_{OL}	current, output low
IOUT	current output signal
ISA	Industry Standard Architecture
LED	light-emitting diode
LSB	least significant bit
MB	megabytes of memory
MSB	most significant bit
NC	not connected (signal)
OUT	output signal
PA	port A
PB	port B
PCMCIA	Personal Computer Memory Card International Association
PROMOUT	EEPROM out bit
PPI	Programmable Peripheral Interface
PPM	parts per million
R_{EXT}	external resistance
rms	root mean square
S	samples
s	seconds
SCLK	serial clock bit
SCXI	Signal Conditioning eXtensions for Instrumentation
SDATA	serial data bit
SDK	Software Development Kit
SHIELD	shield signal
TPCX	Turbo Pascal Compiler
TPU	Turbo Pascal Unit
TSR	terminate-and-stay resident
TTL	transistor-transistor logic
UP	unipolar
V	volts
VCC	positive supply voltage from the PCMCIA bus (usually +5V)
VDC	volts, direct current
VDMAD	Virtual DMA Driver
V_{EXT}	external volts

V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage
WRTPRT	write protect bit

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