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DAQ

NI PCI-1200 User Manual

Multifunctional I/O Device for PCI Bus Computers

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About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments PCI-1200 data acquisition (DAQ) device and contains information concerning its operation and programming.

The NI PCI-1200 is a low-cost multifunction analog, digital, and timing device. The NI PCI-1200 is a member of the National Instruments PCI Series of expansion devices for PCI bus computers. These devices are designed for high-performance data acquisition and control for applications in laboratory testing, production testing, and industrial process monitoring and control.

Conventions Used in This Manual

The following conventions appear in this manual

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DBIO<3..0>.

 — This icon denotes a note, which alerts you to important information.

 — This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on a product, see the *Safety Information* section of Chapter 1, *Introduction*, for precautions to take.

bold — Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

italic — Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.

Macintosh — Macintosh refers to all Macintosh computers with PCI bus, unless otherwise noted.

`monospace` — Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories,

programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

NI-DAQ — NI-DAQ is used in this manual to refer to the NI-DAQ software for PC or Macintosh computers, unless otherwise noted.

SCXI — SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ devices.

National Instruments Documentation

The *PCI-1200 User Manual* is one piece of the documentation set for your DAQ system. You could have any of several types of manuals, depending on the hardware and software in your system. Use the manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- *SCXI Chassis Manual*—If you are using SCXI, read this manual for maintenance information on the chassis and installation instructions.
- SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to the computer. Use these manuals for hardware installation and configuration instructions, specification information about the DAQ hardware, and application hints.
- Software documentation—Examples of software documentation you may have are the LabVIEW or LabWindows/CVI documentation sets and the NI-DAQ documentation. After you set up the hardware system, use either the application software (LabVIEW or LabWindows/CVI) or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure the hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation

guides and accessory user manuals. They explain how to physically connect the relevant pieces of the system. Consult these guides when making connections.

Related Documentation

The following documents contain information that you may find helpful:

- NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, located at `ni.com/zone`
- *PCI Local Bus Specification*, *Revision 2.2*, available at `pcisig.com`
- The technical reference manual for the computer

1 Introduction

This chapter describes the NI PCI-1200, lists what you need to get started, software programming choices, and optional equipment, and explains how to build custom cables and unpack the NI PCI-1200.

About the NI PCI-1200

Thank you for purchasing the NI PCI-1200, a low-cost, high-performance multifunction analog, digital, and timing device for PCI bus computers. The NI PCI-1200 has eight analog input (AI) channels that you can configure as eight single-ended or four differential inputs, a 12-bit successive-approximation A/D converter (ADC), two 12-bit D/A converters (DACs) with voltage outputs, 24 lines of TTL-compatible digital I/O (DIO), and three 16-bit counter/timers for timing I/O (TIO).

Detailed NI PCI-1200 specifications are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your NI PCI-1200, you need the following items:

- ❑ A computer
- ❑ NI PCI-1200 device
- ❑ *NI PCI-1200 User Manual*
- ❑ One of the following software packages and documentation:
  - LabVIEW for Macintosh or Windows
  - Measurement Studio for Windows
  - NI-DAQ for Macintosh or Windows

Software Programming Choices

When programming National Instruments DAQ hardware, you can use an NI application development environment (ADE) or other ADEs. In either case, you use NI-DAQ.

NI-DAQ

NI-DAQ, which ships with the NI PCI-1200, has an extensive library of functions that you can call from the ADE. These functions allow you to use all the features of the NI PCI-1200.

NI-DAQ carries out many of the complex interactions, such as programming interrupts, between the computer and the DAQ hardware. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to the code. Whether you are using LabVIEW, Measurement Studio, or other ADEs, your application uses NI-DAQ, as illustrated in Figure 1-1.

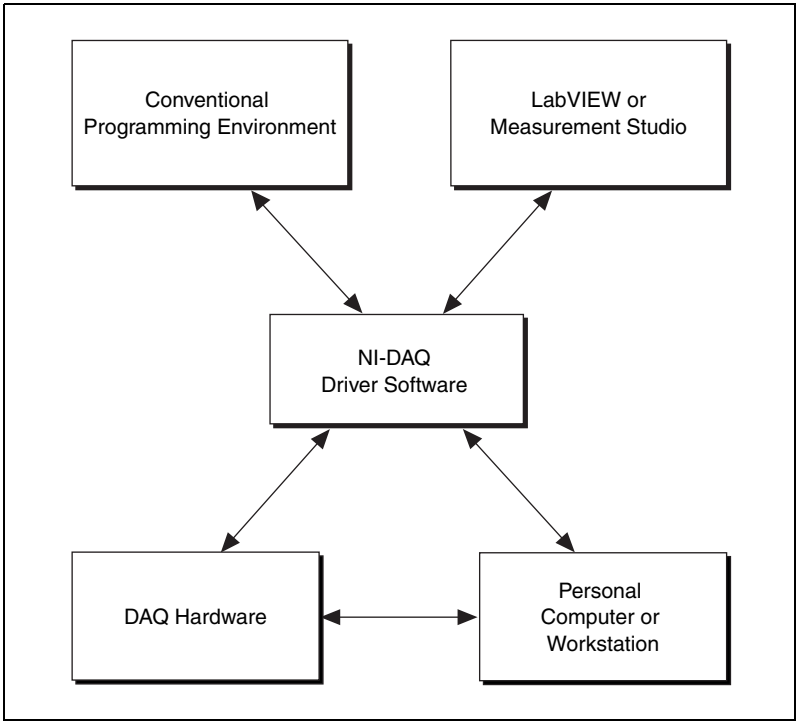


Figure 1-1. The Relationship Between the Programming Environment, NI-DAQ, and the Hardware

To download a free copy of the most recent version of NI-DAQ, click **Download Software** at `ni.com`.

National Instruments ADE Software

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

Measurement Studio, which includes LabWindows/CVI, tools for Visual C++, and tools for Visual Basic, is a development suite that allows you to use ANSI C, Visual C++, and Visual Basic to design the test and measurement software. For C developers, Measurement Studio includes LabWindows/CVI, a fully integrated ANSI C application development environment that features interactive graphics and the LabWindows/CVI Data Acquisition and Easy I/O libraries. For Visual Basic developers, Measurement Studio features a set of ActiveX controls for using National Instruments DAQ hardware. These ActiveX controls provide a high-level programming interface for building virtual instruments. For Visual C++ developers, Measurement Studio offers a set of Visual C++ classes and tools to integrate those classes into Visual C++ applications. The libraries, ActiveX controls, and classes are available with Measurement Studio and NI-DAQ.

Using LabVIEW or Measurement Studio greatly reduces the development time for your data acquisition and control application.

Optional Equipment

NI offers a variety of products to use with the NI PCI-1200 device, including cables, connector blocks, and other accessories, as follows:

- Shielded cables and cable assemblies
- Connector blocks, RTSI bus cables, 50-shielded and 68-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels. To use the NI PCI-1200 with SCXI you need the SCXI-1341 adapter.
- Low-channel-count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and resistance

temperature detectors (RTDs), simultaneous sample and hold, and relays

For more information about optional equipment available from NI, refer to `ni.com/catalog`.

Custom Cabling

NI offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the AI signals, shielded twisted-pair wires for each AI pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- You should route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

The mating connector for the NI PCI-1200 is a 50-position, polarized, ribbon socket connector with strain relief. NI uses a polarized (keyed) connector to prevent inadvertent upside-down connection to the NI PCI-1200.

Unpacking

The NI PCI-1200 is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge (ESD) can damage several components on the device. To avoid such damage in handling the device, take the following precautions:

Caution *Never* touch the exposed pins of connectors.

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the device from the package.

Remove the device from the package and inspect the device for loose components or any other sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into your computer.

Store the NI PCI-1200 in the antistatic envelope when not in use.

Safety Information

The following section contains important safety information that you *must* follow during installation and use of the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to NI for repair.

If the product is rated for use with hazardous voltages (>30 V_{rms}, 42.4 V_{pk}, or 60 V_{dc}), you may need to connect a safety earth-ground wire according to the installation instructions. Refer to Appendix A, *Specifications*, for maximum voltage ratings.

Do *not* substitute parts or modify the product. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. Operate the product only at or below the pollution degree stated in Appendix A, *Specifications*. Pollution is foreign matter in a solid, liquid, or gaseous state that can produce a reduction of dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution degree 1 means no pollution or only dry, non conductive pollution occurs. The pollution has no influence.
- Pollution degree 2 means that only non conductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution degree 3 means that conductive pollution occurs, or dry, non conductive pollution occurs, which becomes conductive due to condensation.

Clean the product with a soft nonmetallic brush. The product *must* be completely dry and free from contaminants before returning it to service.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Remove power from signal lines before connection to or disconnection from the product.

Operate this product only at or below the installation category stated in Appendix A, *Specifications*.

The following is a description of installation categories:

- Installation Category I is for measurements performed on circuits not directly connected to MAINS[1]. This category is a signal level such as voltages on a printed wire device (PWB) on the secondary of an isolation transformer.

  Examples of Installation Category I are measurements on circuits not derived from MAINS and specially protected (internal) MAINS-derived circuits.

- Installation Category II is for measurements performed on circuits directly connected to the low-voltage installation. This category refers to local-level distribution such as that provided by a standard wall outlet.

  Examples of Installation Category II are measurements on household appliances, portable tools, and similar equipment.

- Installation Category III is for measurements performed in the building installation. This category is a distribution level referring to hardwired equipment that does not rely on standard building insulation.

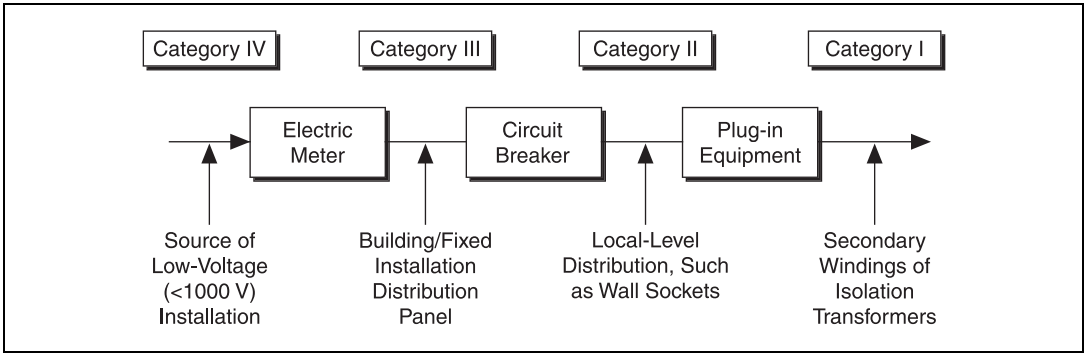
  Examples of Installation Category III include measurements on distribution circuits and circuit breakers. Other examples of Installation Category III are wiring including cables, bus-bars, junction boxes, switches, socket outlets in the building/fixed installation, and equipment for industrial use, such as stationary motors with a permanent connection to the building/fixed installation.

- Installation Category IV is for measurements performed at the source of the low-voltage (<1,000 V) installation.

  Examples of Installation Category IV are electric meters, and measurements on primary overcurrent protection devices and ripple-control units.

[1] MAINS is defined as the electricity supply system to which the equipment concerned is designed to be connected either for powering the equipment or for measurement purposes.

Below is a diagram of a sample installation.



2

Installing and Configuring the NI PCI-1200

This chapter describes how to install and configure the NI PCI-1200.

Installing the Software

If you are using NI-DAQ or NI application software, refer to the installation instructions in your software documentation to install and configure your software.

Complete the following steps to install the software before installing the NI PCI-1200.

1. Install the application development environment (ADE), such as LabVIEW or Measurement Studio, according to the instructions on the CD and the release notes.
2. Install NI-DAQ according to the instructions on the CD and the *DAQ Quick Start Guide* included with the NI PCI-1200.

Note It is important to install NI-DAQ before installing the NI PCI-1200 to ensure that the NI PCI-1200 is properly detected.

Installing the Hardware

The following are general installation instructions. Consult the computer or chassis user manual or technical reference manual for specific instructions and warnings about new devices.

1. Power off and unplug your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.

5. Insert the NI PCI-1200 in an unused PCI system slot. The fit may be tight, but do *not* force the device into place.
6. Screw the NI PCI-1200 mounting bracket to the back panel rail of the computer or use the slot side tabs, if available, to secure the NI PCI-1200 in place.
7. Replace the top cover on the computer. Visually verify the installation. Make sure the device is not touching other devices or components and is fully inserted into the slot.
8. Plug in and power on the computer.

The NI PCI-1200 device is installed.

Configuring the Device

The NI PCI-1200 is completely software configurable. The NI PCI-1200 is fully compliant with the *PCI Local Bus Specification*, *Revision 2.2*. Therefore, all device resources are automatically allocated by the system. For the NI PCI-1200, this allocation includes the base memory address and interrupt level. You do not need to perform any configuration steps after the system powers up.

Analog I/O Configuration

Upon power-up or after a software reset, the NI PCI-1200 is set to the following configuration:

- Referenced single-ended input mode
- ±5 V AI range (bipolar)
- ±5 V analog output (AO) range (bipolar)

Table 2-1 lists all the available analog I/O configurations for the NI PCI-1200 and shows the configuration in reset condition.

Table 2-1. Analog I/O Settings

Parameter	Configuration
Analog Output CH0 Polarity	Bipolar—±5 V (reset condition) Unipolar—0 to 10 V
Analog Output CH1 Polarity	Bipolar—±5 V (reset condition) Unipolar—0 to 10 V

Table 2-1. Analog I/O Settings (Continued)

Parameter	Configuration
Analog Input Polarity	Bipolar—±5 V (reset condition) Unipolar—0 to 10 V
Analog Input Mode	Referenced single-ended (RSE) (reset condition) Nonreferenced single-ended (NRSE) Differential (DIFF)

Both the AI and AO circuitries are software configurable. Refer to the software documentation for more information on changing these settings.

Analog Output Polarity

The NI PCI-1200 has two channels of AO voltage at the I/O connector. You can configure each AO output channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to 10 V at the analog output. A bipolar configuration has a range of –5 to +5 V at the analog output. In addition, you can select the coding scheme for each DAC as either two's complement or straight binary.

If you select a bipolar range for a DAC, the two's complement coding is recommended. In this mode, data values written to the AO channel range from F800 hex (–2,048 decimal) to 7FF hex (2,047 decimal). If you select a unipolar range for a DAC, the straight binary coding is recommended. In this mode, data values written to the AO channel range from 0 to FFF hex (4,095 decimal).

Analog Input Polarity

You can select the analog input on the NI PCI-1200 for either a unipolar range (0 to 10 V) or a bipolar range (–5 to +5 V). In addition, you can select the coding scheme for analog input as either two's complement or straight binary. If you select a bipolar range, the two's complement coding is recommended. In this mode, –5 V input corresponds to F800 hex (–2,048 decimal) and +5 V corresponds to 7FF hex (2,047 decimal). If you select a unipolar mode, the straight binary coding is recommended. In this mode, 0 V input corresponds to 0 hex, and +10 V corresponds to FFF hex (4,095 decimal).

Analog Input Mode

The NI PCI-1200 has three input modes—referenced single-ended (RSE) input mode, non-referenced single-ended (NRSE) input mode, and differential (DIFF) input mode. The single-ended input configurations use eight channels. The DIFF input configuration uses four channels. Table 2-2 describes these configurations.

Table 2-2. Analog Input Modes for the NI PCI-1200

Analog Input Modes	Description
RSE	RSE mode provides eight single-ended inputs with the negative input of the instrumentation amplifier referenced to analog ground (reset condition).
NRSE	NRSE mode provides eight single-ended inputs with the negative input of the instrumentation amplifier tied to AISENSE/AIGND and not connected to ground.
DIFF	DIFF mode provides four differential inputs with the positive input of the instrumentation amplifier tied to channels 0, 2, 4, or 6 and the negative input tied to channels 1, 3, 5, or 7, respectively, thus choosing channel pairs (0, 1), (2, 3), (4, 5), or (6, 7).

While reading the following sections, you may find it helpful to refer to the *Analog Input Signal Connections* section of Chapter 3, *Signal Connections*, which contains diagrams showing the signal paths for the three configurations.

RSE Input Mode (Eight Channels, Reset Condition)

RSE input means that all input signals are referenced to a common ground point that is also tied to the NI PCI-1200 AI ground. The differential amplifier negative input is tied to analog ground. RSE mode is useful for measuring floating signal sources. With this input configuration, the NI PCI-1200 can monitor eight AI channels.

Considerations for using RSE mode are discussed in Chapter 3, *Signal Connections*. Notice that in this mode, the signal return path is analog ground at the connector through the AISENSE/AIGND pin.

NRSE Input Mode (Eight Channels)

NRSE input means that all input signals are referenced to the same common-mode voltage, which floats with respect to the NI PCI-1200 analog ground. This common-mode voltage is subsequently subtracted by the input instrumentation amplifier. NRSE mode is useful for measuring ground-referenced signal sources.

Considerations for using NRSE mode are discussed in Chapter 3, *Signal Connections*. Notice that in this mode, the signal return path is through the negative terminal of the amplifier at the connector through the AISENSE/AIGND pin.

DIFF Input Mode (Four Channels)

DIFF input means that each input signal has its own reference, and the difference between each signal and its reference is measured. The signal and its reference are each assigned an input channel. With this input configuration, the NI PCI-1200 can monitor four differential AI signals.

Considerations for using DIFF mode are discussed in Chapter 3, *Signal Connections*. Notice that the signal return path is through the negative terminal of the amplifier and through channel 1, 3, 5, or 7, depending on which channel pair you select.

3

Signal Connections

This chapter describes how to make input and output signal connections to the NI PCI-1200 through the device I/O connector and details the I/O timing specifications.

The I/O connector for the NI PCI-1200 has 50 pins that you can connect to 50-pin accessories.

I/O Connector

Figure 3-1 shows the pin assignments for the NI PCI-1200 I/O connector.

Caution You should not externally drive DIO lines while the computer is powered off; doing so can damage the computer. NI is *not* liable for any damage resulting from signal connections that exceed these maximum ratings. Connections, including connecting power signals to ground and vice versa, that exceed any of the maximum ratings of input or output signals on the NI PCI-1200 may damage the NI PCI-1200 and the computer.

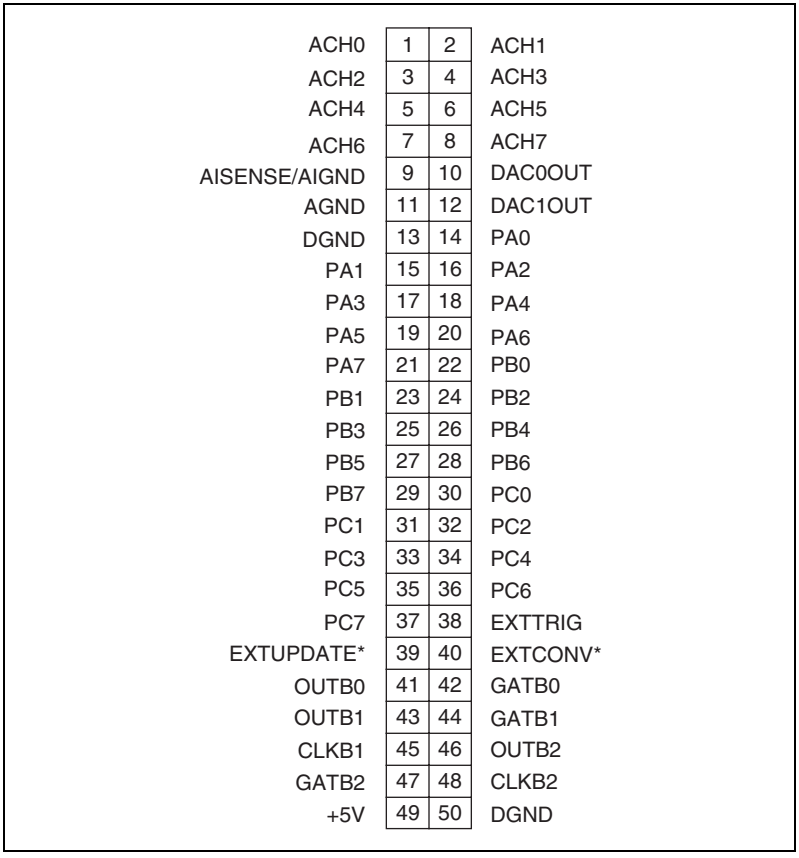


Figure 3-1. NI PCI-1200 I/O Connector Pin Assignments

Signal Connection Descriptions

The following table describes the connector pins on the NI PCI-1200 I/O connector by pin number and gives the signal name and description of each signal connector pin.

Table 3-1. Signal Descriptions for NI PCI-1200 I/O Connector Pins

Pin	Signal Name	Direction	Reference	Description
1–8	ACH<7..0>	AI	AGND	Analog Channel 7 through 0—AI channels 0 through 7.
9	AISENSE/AIGND	I/O	AGND	Analog Input Sense/Analog Input Ground—Connected to AGND in RSE mode, AI sense in NRSE mode.

Table 3-1. Signal Descriptions for NI PCI-1200 I/O Connector Pins (Continued)

Pin	Signal Name	Direction	Reference	Description
10	DAC0OUT	AO	AGND	Digital-to-Analog Converter 0 Output—Voltage output signal for AO channel 0.
11	AGND	N/A	N/A	Analog Ground—AO ground reference for AO voltages. Bias current return point for differential measurements.
12	DAC1OUT	AO	AGND	Digital-to-Analog Converter 1 Output—Voltage output signal for AO channel 1.
13, 50	DGND	N/A	N/A	Digital Ground—Voltage ground reference for the digital signals and the +5 V supply.
14–21	PA<7..0>	DIO	DGND	Port A 7 through 0—Bidirectional data lines for port A. PA7 is the most significant bit (MSB), and PA0 is the least significant bit (LSB).
22–29	PB<7..0>	DIO	DGND	Port B 7 through 0—Bidirectional data lines for port B. PB7 is the MSB, and PB0 is the LSB.
30–37	PC<7..0>	DIO	DGND	Port C 7 through 0—Bidirectional data lines for port C. PC7 is the MSB, and PC0 is the LSB.
38	EXTTRIG	DI	DGND	External Trigger—External control signal to trigger a DAQ operation.
39	EXTUPDATE*	DI	DGND	External Update—External control signal to update DAC outputs.
40	EXTCONV*	DIO	DGND	External Convert—External control signal to time A/D conversions (DI) and drive SCANCLK when you use SCXI (DO).
41	OUTB0	DO	DGND	Output B0—Digital output signal of counter B0.
42	GATB0	DI	DGND	Gate B0—External control signal for gating counter B0.

Table 3-1. Signal Descriptions for NI PCI-1200 I/O Connector Pins (Continued)

Pin	Signal Name	Direction	Reference	Description
43	OUTB1	DIO	DGND	Output B1—Digital output signal of counter B1 (DO). External control signal for timing a scan interval (DI).
44	GATB1	DI	DGND	Gate B1—External control signal for gating counter B1.
45	CLKB1	DI	DGND	Clock B1—External control clock signal for counter B1.
46	OUTB2	DO	DGND	Counter B2—Digital output signal of counter B2.
47	GATB2	DI	DGND	Gate B2—External control signal for gating counter B2.
48	CLKB2	DI	DGND	Clock B2—External control clock signal for counter B2.
49	+5V	DO	DGND	+5 Volts—This pin is fused for up to 1 A of +4.65 to +5.25 V.

* Indicates that the signal is active low.

DI = Digital Input DO = Digital Output N/A = Not Applicable

The connector pins are grouped into AI signal pins, AO signal pins, DIO signal pins, TIO signal pins, and power connections. The following sections describe the signal connection guidelines for each of these groups.

Analog Input Signal Connections

Pins 1 through 8 are AI signal pins for the 12-bit ADC. Pin 9, AISENSE/AIGND, is an analog common signal. You can use this pin for a general analog power ground tie to the NI PCI-1200 in RSE mode or as a return path in NRSE mode. Pin 11, AGND, is the bias current return point for differential measurements. Pins 1 through 8 are tied to the eight single-ended AI channels of the input multiplexer through 4.7 kΩ series resistors. Pins 2, 4, 6, and 8 and also tied to an input multiplexer for DIFF mode.

The signal ranges for inputs ACH<7..0> at all possible gains are shown in Tables 3-2 and 3-3. Exceeding the input signal range will not damage the input circuitry as long as the maximum powered-on input voltage rating

of ±35 V or powered off voltage rating of ±25 V is not exceeded. The NI PCI-1200 is guaranteed to withstand inputs up to the maximum input voltage rating.

Caution Exceeding the input signal range distorts input signals. Exceeding the maximum input voltage rating may damage the NI PCI-1200 device and the computer. NI is *not* liable for any damage resulting from such signal connections.

Table 3-2. Bipolar Analog Input Signal Range Versus Gain

Gain Setting	Input Signal Range
1	–5.0 to 4.99756 V
2	–2.5 to 2.49878 V
5	–1.0 to 0.99951 V
10	–500 to 499.756 mV
20	–250 to 249.877 mV
50	–100 to 99.951 mV
100	–50 to 49.975 mV

Table 3-3. Unipolar Analog Input Signal Range Versus Gain

Gain Setting	Input Signal Range
1	0 to 9.99756 V
2	0 to 4.99878 V
5	0 to 1.99951 V
10	0 to 999.756 mV
20	0 to 499.877 mV
50	0 to 199.951 mV
20	0 to 99.975 mV

How you connect AI signals to the NI PCI-1200 depends on how you configure the NI PCI-1200 AI circuitry and the type of input signal source. With different NI PCI-1200 configurations, you can use the NI PCI-1200

instrumentation amplifier in different ways. Figure 3-2 shows a diagram of the NI PCI-1200 instrumentation amplifier.

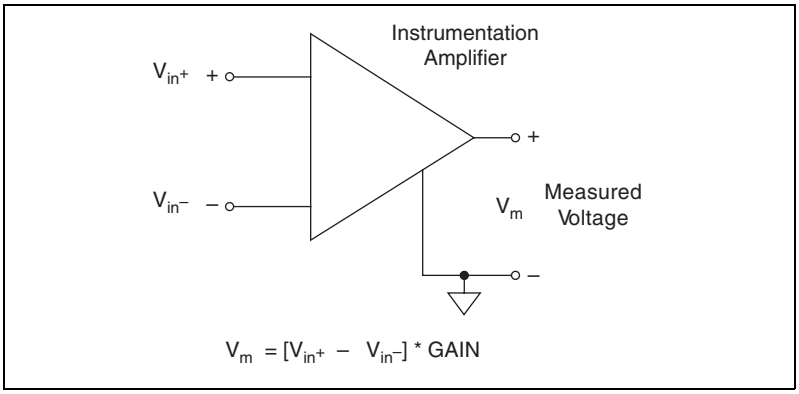


Figure 3-2. NI PCI-1200 Instrumentation Amplifier

The NI PCI-1200 instrumentation amplifier applies gain, common-mode voltage rejection, and high-input impedance to the AI signals connected to the NI PCI-1200. Signals are routed to the positive and negative inputs of the instrumentation amplifier through input multiplexers on the device. The instrumentation amplifier converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the NI PCI-1200 ground. The NI PCI-1200 ADC measures this output voltage when it performs A/D conversions.

All signals must be referenced to ground, either at the source device or at the NI PCI-1200. If you have a floating source, you must use a ground-referenced input connection at the NI PCI-1200. If you have a grounded source, use a nonreferenced input connection at the NI PCI-1200.

Types of Signal Sources

When configuring the input mode of the NI PCI-1200 and making signal connections, first determine whether the signal source is floating or ground referenced. These two signal types are described in the following sections.

Floating Signal Sources

A floating signal source is not connected in any way to the building ground system but has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers.

Tie the ground reference of a floating signal to the NI PCI-1200 AI ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies or appears to float. An instrument or device that supplies an isolated output falls into the floating signal source category.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the NI PCI-1200, assuming that the computer is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are improperly connected. The connection instructions that follow for grounded signal sources eliminate this ground potential difference from the measured signal.

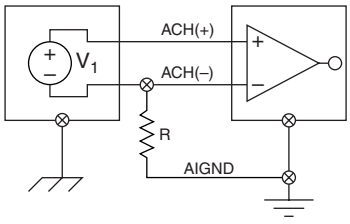
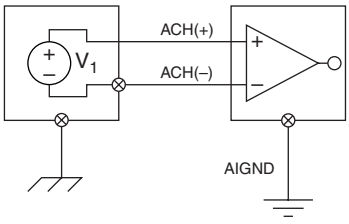
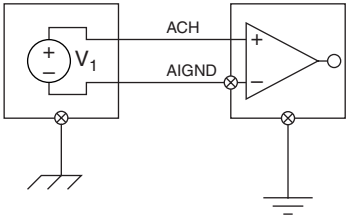
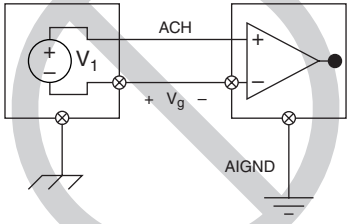
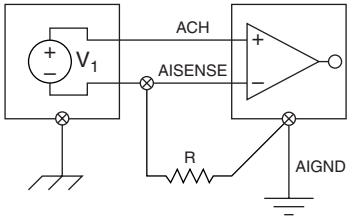
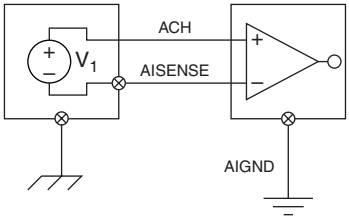


Note If you power both the NI PCI-1200 and the computer with a floating power source (such as a battery), the system may float with respect to earth ground. In this case, treat all of the signal sources as floating sources.

Input Configurations

You can configure the NI PCI-1200 for RSE, NRSE, or DIFF input mode. The following sections discuss the use of single-ended and differential measurements, and considerations for measuring both floating and ground-referenced signal sources. Table 3-4 summarizes the recommended input configurations for both types of signal sources.

Table 3-4. Summary of Analog Input Connections

Input	Signal Source Type	
	Floating Signal Source (Not Connected to Building Ground)	**Grounded Signal Source**
	Examples • Ungrounded Thermocouples • Signal Conditioning with Isolated Outputs • Battery Devices	Examples • Plug-in Instruments with Nonisolated Outputs
Differential (DIFF)	 See text for information on bias resistors.	
Single-Ended — Ground Referenced (RSE)		NOT RECOMMENDED  Ground-loop losses, V_g, are added to measured signal.
Single-Ended — Nonreferenced (NRSE)	 See text for information on bias resistors.	

Differential Connection Considerations (DIFF Configuration)

Differential connections are those in which each NI PCI-1200 AI signal has its own reference signal or signal return path. These connections are available when you configure the NI PCI-1200 in the DIFF mode. Each input signal is tied to the positive input of the instrumentation amplifier, and its reference signal, or return, is tied to the negative input of the instrumentation amplifier.

When configuring the NI PCI-1200 for DIFF input, each signal uses two of the multiplexer inputs—one for the signal and one for its reference signal. Therefore, only four AI channels are available when using DIFF mode. Use DIFF input mode when any of the following conditions is present:

- Input signals are low level (less than 1 V).
- Leads connecting the signals to the NI PCI-1200 are greater than 10 ft.
- Any of the input signals require a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce noise pickup and increase common-mode signal and noise rejection. With these connections, input signals can float within the common-mode limits of the input instrumentation amplifier.

Differential Connections for Grounded Signal Sources

Figure 3-3 shows how to connect a ground-referenced signal source to a NI PCI-1200 configured for DIFF input mode. Configuration instructions are in the *Analog I/O Configuration* section of Chapter 2, *Installing and Configuring the NI PCI-1200*.

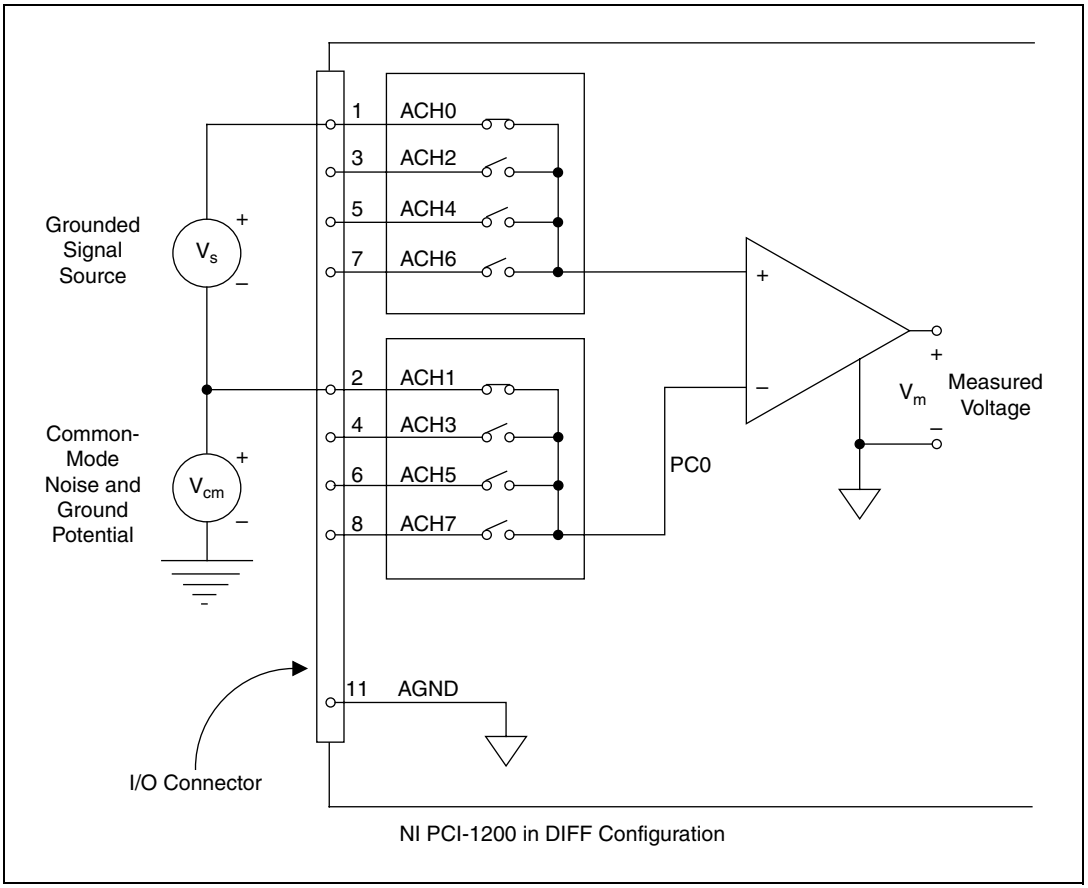


Figure 3-3. Differential Input Connections for Grounded Signal Sources

With this connection type, the instrumentation amplifier rejects both the common-mode noise in the signal and the ground-potential difference between the signal source and the NI PCI-1200 ground (shown as V_{cm} in Figure 3-3).

Differential Connections for Floating Signal Sources

Figure 3-4 shows how to connect a floating signal source to a NI PCI-1200 configured for DIFF input mode. Configuration instructions are in the *Analog I/O Configuration* section of Chapter 2, *Installing and Configuring the NI PCI-1200*.

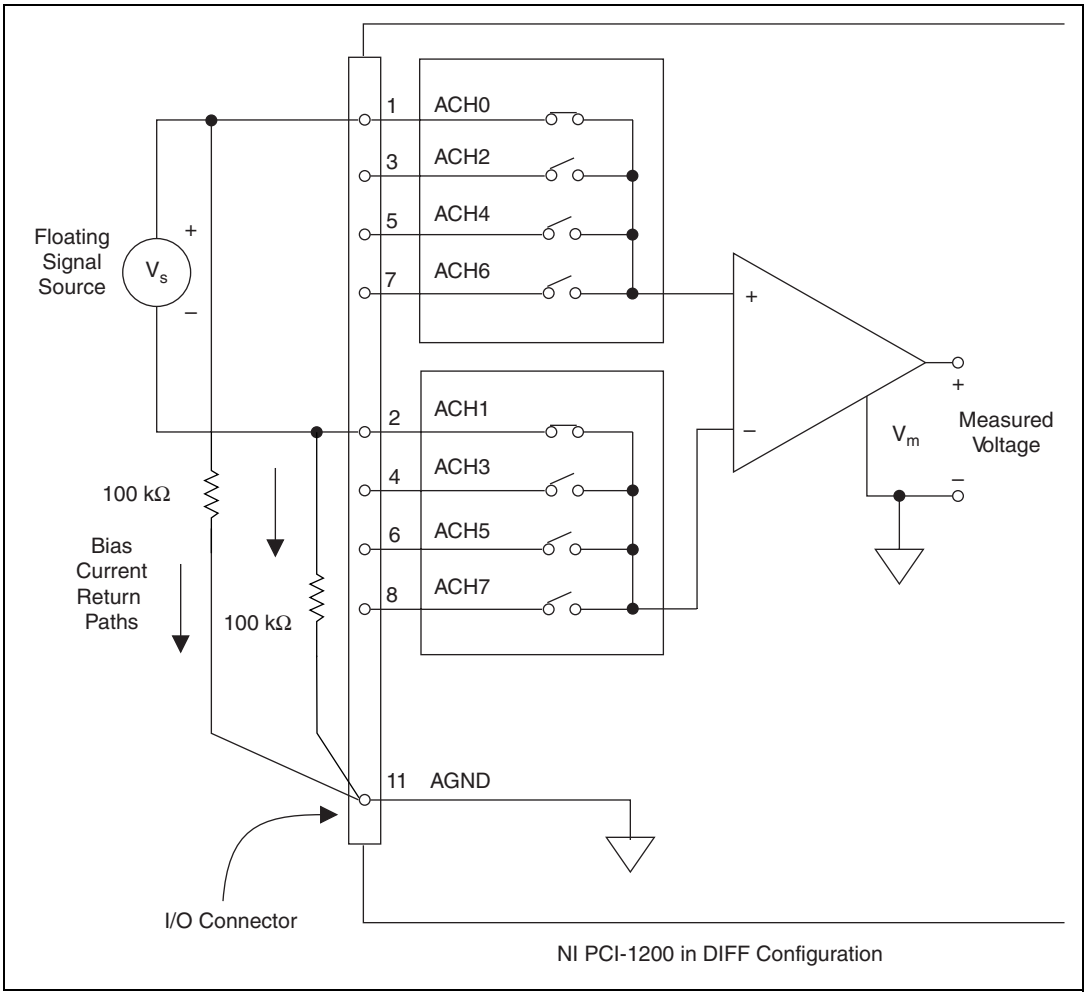


Figure 3-4. Differential Input Connections for Floating Sources

The 100 kΩ resistors shown in Figure 3-4 create a return path to ground for the bias currents of the instrumentation amplifier. If there is no return path, the instrumentation amplifier bias currents charge stray capacitances, resulting in uncontrollable drift and possible saturation in the amplifier. Typically, values from 10 to 100 kΩ are used.

A resistor from each input to ground, as shown in Figure 3-4, provides bias current return paths for an AC-coupled input signal.

If the input signal is DC-coupled, you need only the resistor that connects the negative signal input to ground. This connection does not lower the input impedance of the AI channel.

Single-Ended Connection Considerations

Single-ended connections are those in which all NI PCI-1200 AI signals are referenced to one common ground. The input signals are tied to the positive input of the instrumentation amplifier, and the common ground point is tied to the negative input of the instrumentation amplifier.

When the NI PCI-1200 is configured for a single-ended input mode (NRSE or RSE), eight AI channels are available. Use single-ended input connections when the following conditions are met by all input signals:

- Input signals are high level (greater than 1 V).
- Leads connecting the signals to the NI PCI-1200 are less than 10 ft.
- All input signals share a common reference signal (at the source).

If any of the preceding criteria is not met, use the DIFF input configuration.

You can software configure the NI PCI-1200 for two types of single-ended connections, RSE configuration and NRSE configuration. Use the RSE configuration for floating signal sources; in this case, the NI PCI-1200 provides the reference ground point for the external signal. Use the NRSE configuration for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the NI PCI-1200 should not supply one.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 3-5 shows how to connect a floating signal source to an NI PCI-1200 configured for RSE mode. Configure the NI PCI-1200 AI circuitry for RSE input to make these types of connections. Configuration instructions are in the *Analog I/O Configuration* section of Chapter 2, *Installing and Configuring the NI PCI-1200*.

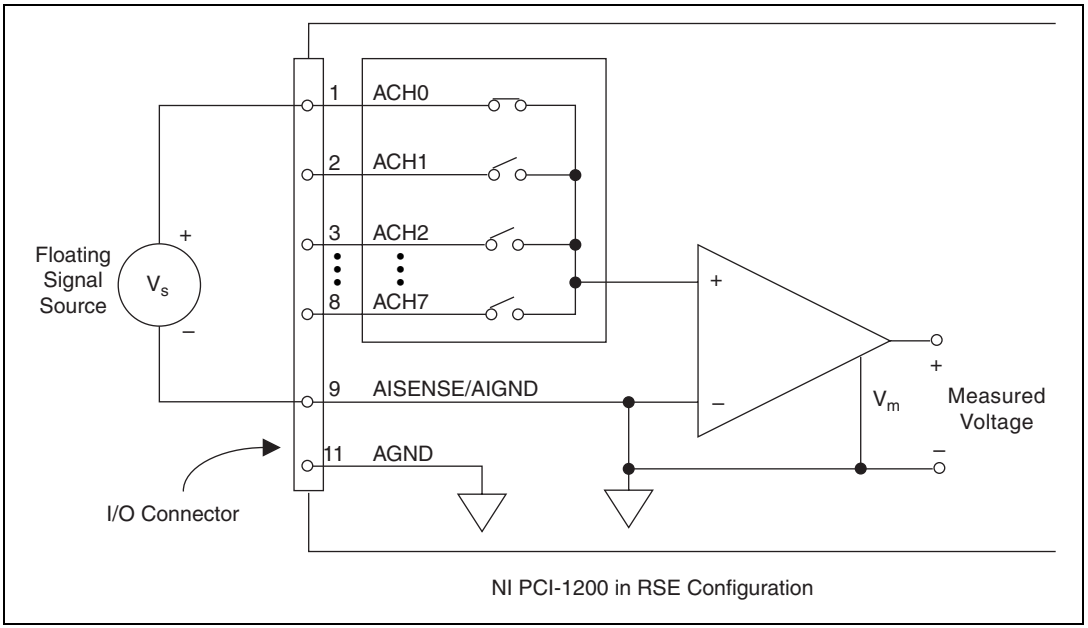


Figure 3-5. Single-Ended Input Connections for Floating Signal Sources

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

If you measure a grounded signal source with a single-ended configuration, configure the NI PCI-1200 in the NRSE input configuration. The signal is connected to the positive input of the NI PCI-1200 instrumentation amplifier and the signal local ground reference is connected to the negative input of the NI PCI-1200 instrumentation amplifier. Therefore, connect the ground point of the signal to the AISENSE pin. Any potential difference between the NI PCI-1200 ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the instrumentation amplifier and is therefore rejected by the amplifier. On the other hand, if the input circuitry of the NI PCI-1200 is referenced to ground,

such as in the RSE configuration, this difference in ground potentials appears as an error in the measured voltage.

Figure 3-6 shows how to connect a grounded signal source to an NI PCI-1200 configured in NRSE input mode. Configuration instructions are included in the *Analog I/O Configuration* section of Chapter 2, *Installing and Configuring the NI PCI-1200*.

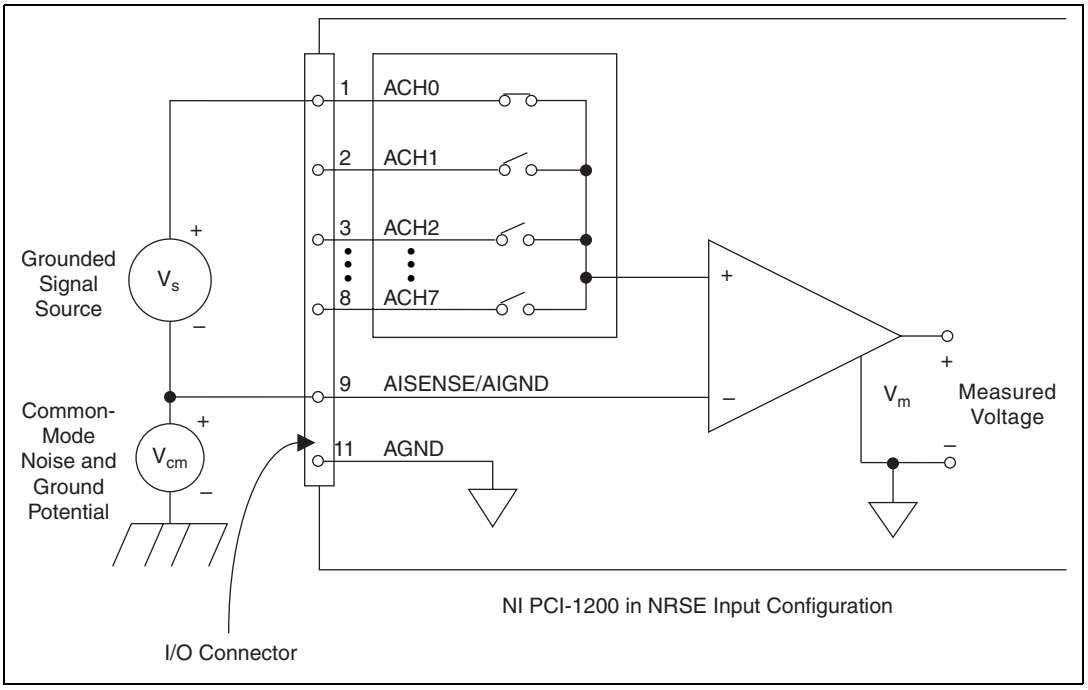


Figure 3-6. Single-Ended Input Connections for Grounded Signal Sources

Common-Mode Signal Rejection Considerations

Figures 3-4 and 3-6 show connections for signal sources that are already referenced to some ground point with respect to the NI PCI-1200. In these cases, the instrumentation amplifier can reject any voltage caused by ground-potential differences between the signal source and the NI PCI-1200. In addition, with differential input connections, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the NI PCI-1200.

The common-mode input range of the NI PCI-1200 instrumentation amplifier is the magnitude of the greatest common-mode signal that can be rejected.

The common-mode input range for the NI PCI-1200 depends on the size of the differential input signal, $V_{diff} = (V_{in}+) - (V_{in}-)$, and the gain setting of the instrumentation amplifier. In unipolar mode, the differential input range is 0 to 10 V. In bipolar mode, the differential input range is –5 to +5 V. Inputs should remain within a range of –5 to 10 V in both bipolar and unipolar modes.

Analog Output Signal Connections

Pins 10 through 12 on the I/O connector are AO signal pins.

Pins 10 and 12 are the DAC0OUT and DAC1OUT signal pins. DAC0OUT is the voltage output signal for AO channel 0. DAC1OUT is the voltage output signal for AO channel 1.

Pin 11, AGND, is the ground-reference point for the AO and AI channels.

The following output ranges are available:

- Bipolar output: ±5 V[1]
- Unipolar output: 0 to 10 V[1]

[1] Maximum load current: ±2 mA for 12-bit linearity

Figure 3-7 shows how to make AO signal connections.

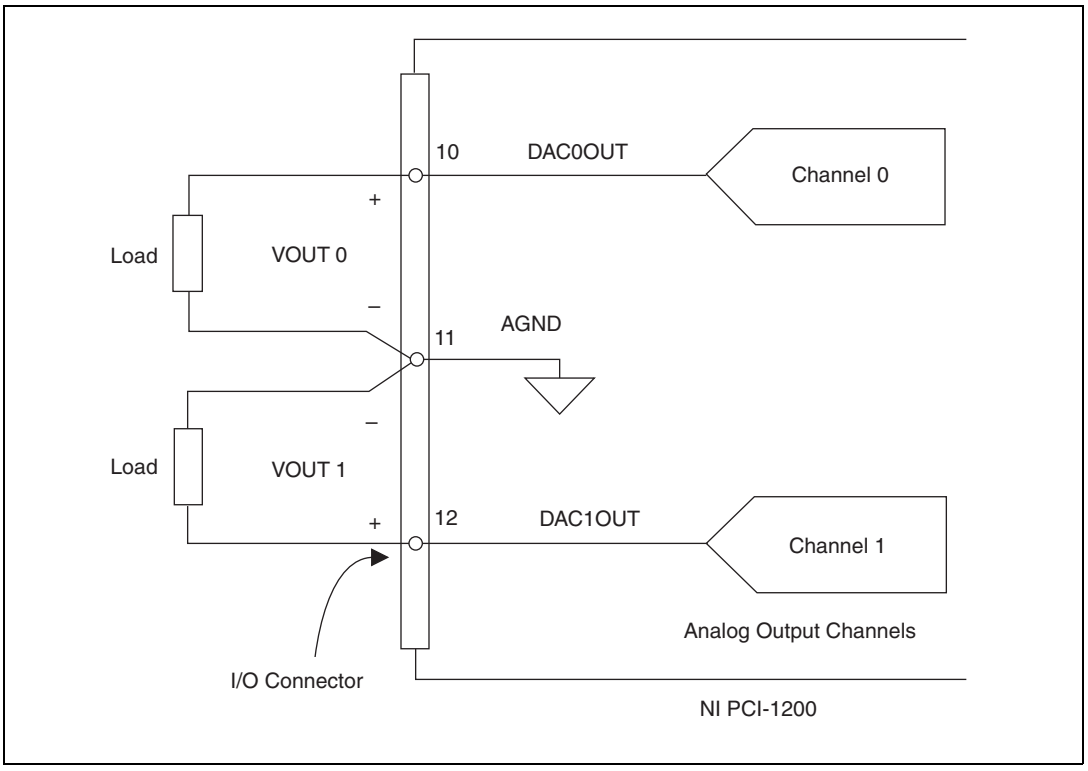


Figure 3-7. Analog Output Signal Connections

Digital I/O Signal Connections

Pins 13 through 37 of the I/O connector are DIO signal pins. DIO on the NI PCI-1200 uses the 82C55A integrated circuit. The 82C55A is a general-purpose peripheral interface containing 24 programmable I/O pins. These pins represent the three 8-bit ports (PA, PB, and PC) of the 82C55A.

Pins 14 through 21 are connected to the digital lines PA<7..0> for DIO port A. Pins 22 through 29 are connected to the digital lines PB<7..0> for DIO port B. Pins 30 through 37 are connected to the digital lines PC<7..0> for DIO port C. Pin 13, DGND, is the digital ground pin for all three DIO ports. Refer to Appendix A, *Specifications*, for signal voltage and current specifications.

The following specifications and ratings apply to the DIO lines. All voltages are with respect to DGND.

Logical Inputs and Outputs

- Absolute max voltage rating –0.5 to +5.5 V
- DIO lines:
  - Input logic low voltage –0.3 V min 0.8 V max
  - Input logic high voltage 2.2 V min 5.3 V max
  - Output logic low voltage (at output current = 2.5 mA) — 0.4 V max
  - Output logic high voltage (at output current = –2.5 mA) 3.7 V min —
  - Input leakage current ($0 < V_{in} < 5$ V) –1 µA min 1 µA max

Figure 3-8 illustrates signal connections for three typical DIO applications.

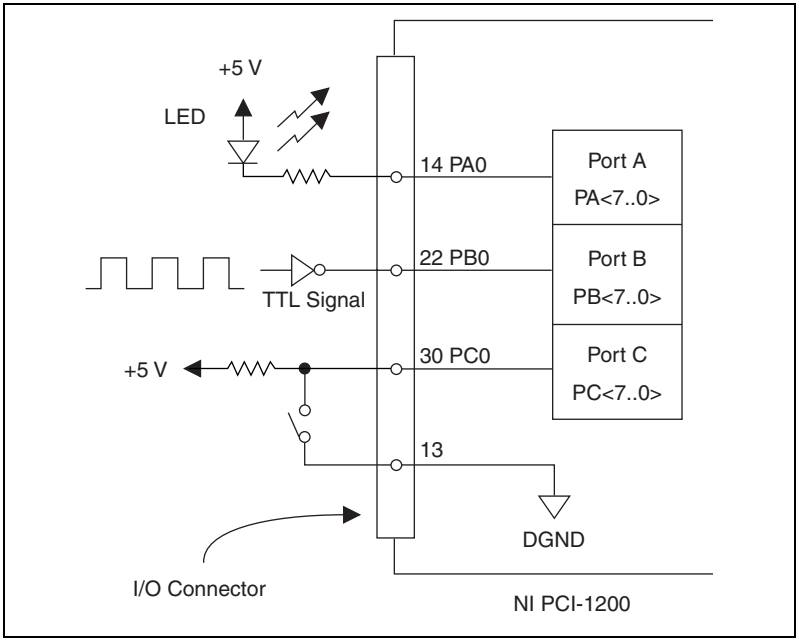


Figure 3-8. Digital I/O Connections

In Figure 3-8, port A is configured for digital output, and ports B and C are configured for digital input. Digital input applications include receiving

TTL signals and sensing external device states, such as the state of the switch in Figure 3-8. Digital output applications include sending TTL signals and driving external devices, such as the LED in Figure 3-8.

Port C Pin Connections

The signals assigned to port C depend on the mode in which the 82C55A is programmed. In mode 0, port C is considered to be two 4-bit I/O ports. In modes 1 and 2, port C is used for status and handshaking signals with two or three I/O bits mixed in. Table 3-5 summarizes the signal assignments of port C for each programmable mode.

Table 3-5. Port C Signal Assignments

Programmable Mode	Group A					Group B		
	PC7	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O

* Indicates that the signal is active low.

Power Connections

Pin 49 of the I/O connector supplies +5 V from the computer power supply through a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. Pin 49 is referenced to DGND, and you can use the +5 V to power external digital circuitry.

- Power rating: 1 A at +4.65 to +5.25 V

Caution Do not directly connect this +5 V power pin to analog or digital ground or to any other voltage source on the NI PCI-1200 or any other device. Doing so can damage the NI PCI-1200 or the computer. NI is *not* liable for any damage due to incorrect power connections.

DAQ and General Purpose Timing Signal Connections

Pins 38 through 48 of the I/O connector are connections for TIO signals. The NI PCI-1200 timing I/O uses two 82C53 counter/timer integrated circuits. One circuit, designated 82C53(A), is used exclusively for DAQ timing, and the other, 82C53(B), is available for general use. Use pins 38

through 40 and pin 43 to carry external signals for DAQ timing. These signals are explained in the *DAQ Timing Connections* section. Pins 41 through 48 carry general purpose timing signals from 82C53(B). These signals are explained in the *General Purpose Timing Signal Connections* section.

DAQ Timing Connections

Each 82C53 counter/timer circuit contains three counters. Counter 0 on the 82C53(A) counter/timer, referred to as A0, is a sample-interval counter in timed A/D conversions. Counter 1 on the 82C53(A) counter/timer, referred to as A1, is a sample counter in controlled A/D conversions. Therefore, counter A1 stops data acquisition after a predefined number of samples. These counters are unavailable for general use.

Instead of counter A0, you can use EXTCONV* to externally time conversions. Figure 3-9 shows the timing requirements for the EXTCONV* input. An A/D conversion is initiated by a falling edge on the EXTCONV*.

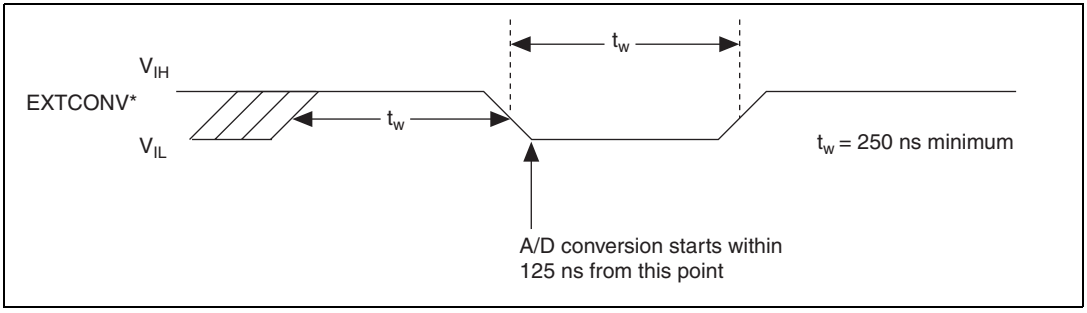


Figure 3-9. EXTCONV* Signal Timing

The external control signal EXTTRIG can either start a DAQ sequence or terminate an ongoing DAQ sequence depending on the mode—posttrigger (POSTTRIG) or pretrigger (PRETRIG). These modes are software-selectable.

In the POSTTRIG mode, EXTTRIG serves as an external trigger that initiates a DAQ sequence. When you use counter A0 to time sample intervals, a rising edge on EXTTRIG starts counter A0 and the DAQ sequence. When you use EXTCONV* to time sample intervals, data acquisition is enabled on a rising edge of EXTTRIG followed by a rising edge on EXTCONV*. The first conversion occurs on the next falling edge of EXTCONV*. Further transitions on the EXTTRIG line have no effect until a new DAQ sequence is established.

Figure 3-10 shows a possible controlled DAQ sequence using EXTCONV* and EXTTRIG. The rising edge of EXTCONV* that enables external conversions must occur a minimum of 50 ns after the rising edge of EXTTRIG. The first conversion occurs on the next falling edge of EXTCONV*.

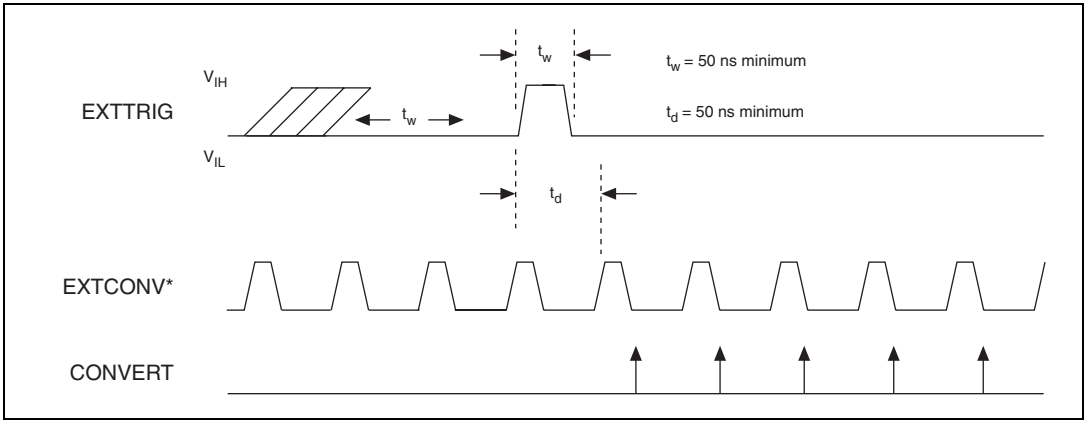


Figure 3-10. Posttrigger DAQ Timing

In the PRETRIG mode, EXTTRIG serves as a pretrigger signal. Data is acquired both before and after the EXTTRIG signal occurs. A/D conversions are software enabled, which initiates the DAQ operation. However, the sample counter is not started until the EXTTRIG input senses a rising edge. Conversions remain enabled until the sample counter counts to zero. You can acquire up to 65,535 samples after the stop trigger. The number of samples acquired before the trigger is limited only by the size of the memory buffer available for data acquisition.

Figure 3-11 shows a pretrigger DAQ timing sequence using EXTTRIG and EXTCONV*. The DAQ operation has been initiated through software.

Note The sample counter has been programmed to allow five conversions after the rising edge on the EXTTRIG signal. Additional transitions on the EXTTRIG line have no effect until you initiate a new DAQ sequence.

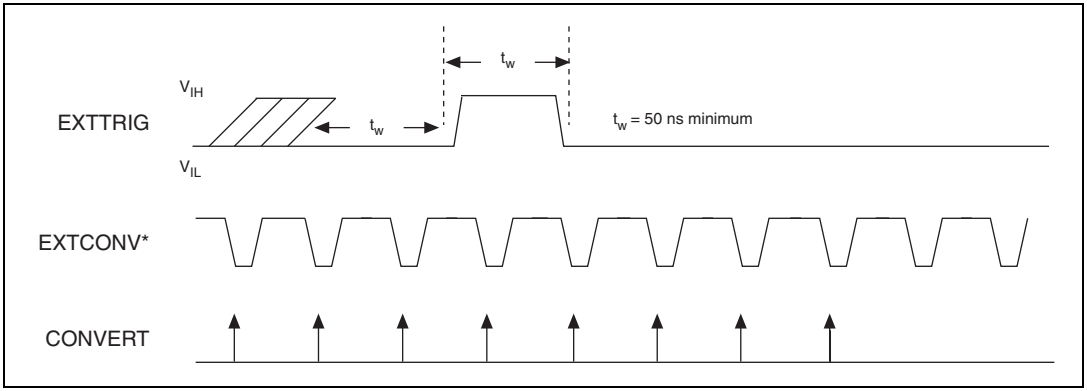


Figure 3-11. Pretrigger DAQ Timing

For interval scanning data acquisition, counter B1 determines the scan interval. Instead of using counter B1, you can externally time the scan interval through OUTB1. If you externally time the sample interval, you should also externally time the scan interval.

Figure 3-12 shows an example of an interval-scanning DAQ operation. The scan interval and the sample interval are being timed externally through OUTB1 and EXTCONV*. Channels 1 and 0 of the input multiplexers are scanned once during each scan interval. The first rising edge of EXTCONV* must occur a minimum of 50 ns after the rising edge on OUTB1. The first rising edge of EXTCONV* after the rising edge of OUTB1 enables an internal GATE signal that allows conversions to occur. The first conversion then occurs on the following falling edge of EXTCONV*. The GATE signal disables conversions for the rest of the scan interval after the desired channels have been scanned. Refer to the *Interval Scanning Acquisition Mode* section of Chapter 4, *Theory of Operation*, for more information on interval scanning.

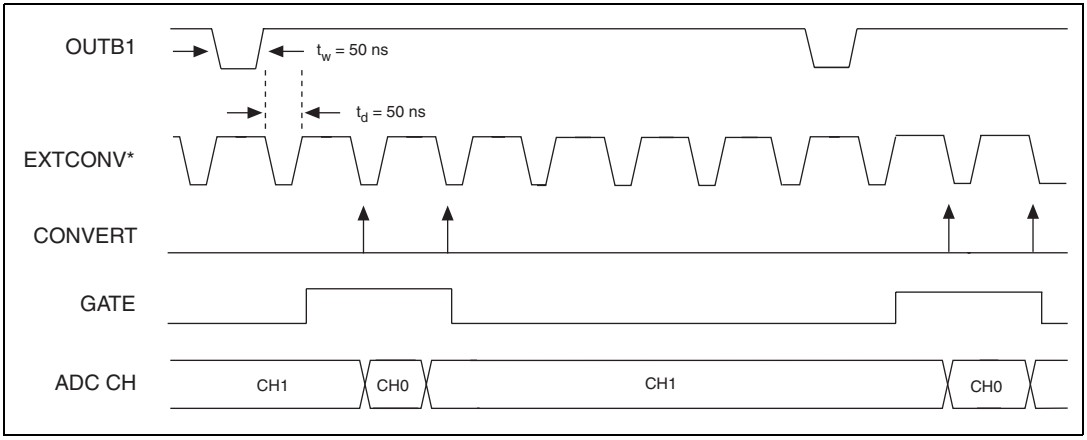


Figure 3-12. Interval-Scanning Signal Timing

Use the final external control signal, EXTUPDATE*, to externally control updating the output voltage of the 12-bit DACs and/or to generate an externally timed interrupt. There are two update modes, immediate update and delayed update. In immediate update mode, the analog output is updated as soon as a value is written to the DAC. If you select the delayed update mode, a value is written to the DAC; however, the corresponding DAC voltage is not updated until a low level on the EXTUPDATE* signal is sensed. Furthermore, if you enable interrupt generation, an interrupt is generated whenever a rising edge is detected on the EXTUPDATE* bit. Therefore, you can perform externally timed, interrupt-driven waveform generation on the NI PCI-1200. The EXTUPDATE* line is susceptible to noise caused by switching lines and could generate false interrupts. You should make the width of the EXTUPDATE* pulse as short as possible, but greater than 50 ns.

Figure 3-13 illustrates a waveform generation timing sequence using the EXTUPDATE* signal and the delayed-update mode. The DACs are updated by a high level on the DAC OUTPUT UPDATE signal, which in this case is triggered by a low level on the EXTUPDATE* line. CNTINT is the signal that interrupts the computer. This interrupt is generated on the rising edge of EXTUPDATE*. DACWRT is the signal that writes a new value to the DAC.

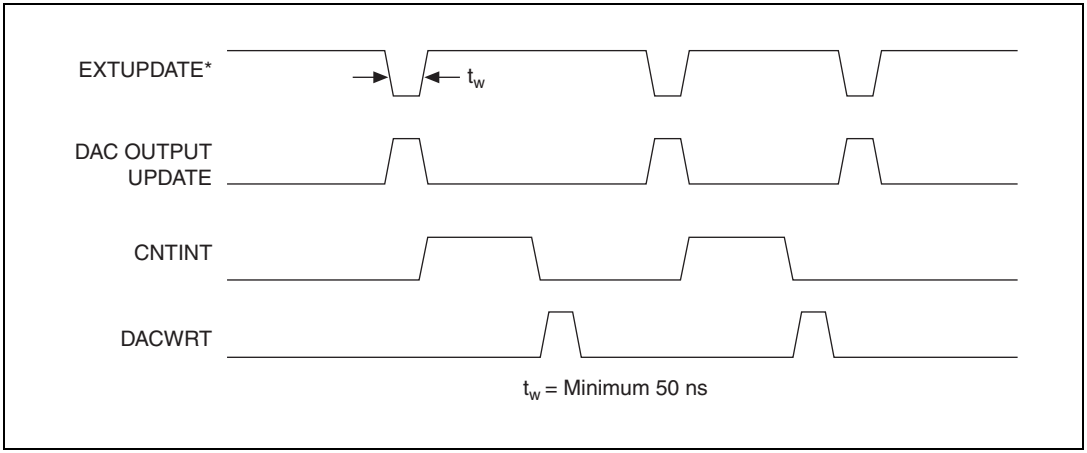


Figure 3-13. EXTUPDATE* Signal Timing for Updating DAC Output

The absolute max voltage input rating for the EXTCONV*, EXTTRIG, OUTB1, and EXTUPDATE* signals is –0.5 to 5.5 V with respect to DGND.

For more information concerning the various modes of data acquisition and analog output, refer to Chapter 4, *Theory of Operation*, or to the NI-DAQ documentation.

General Purpose Timing Signal Connections

The general purpose timing signals include the GATE, CLK, and OUT signals for the three 82C53(B) counters. The 82C53 counter/timers can be used for general-purpose applications such as pulse and square wave generation, event counting, and pulse-width, time-lapse, and frequency measurement. For these applications, the CLK and GATE signals at the I/O connector control the counters. The single exception is counter B0, which has an internal 2 MHz clock.

To perform pulse and square wave generation, program a counter to generate a timing signal at its OUT output pin. To perform event counting, program a counter to count rising or falling edges applied to any of the 82C53 CLK inputs, then read the counter value to determine the number of edges that have occurred. You can enable or disable the counting operation by controlling the gate input. Figure 3-14 shows connections for a typical event-counting operation in which a switch is used to gate the counter on and off.

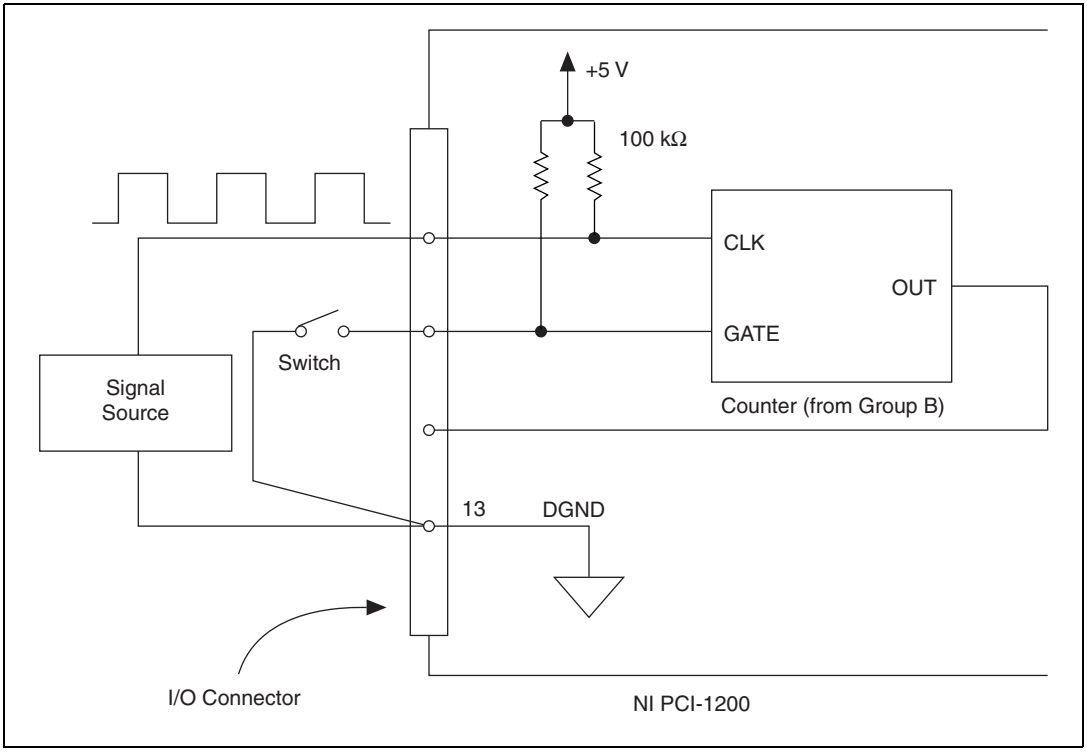


Figure 3-14. Event-Counting Application with External Switch Gating

Pulse-width measurement is performed by level gating. The pulse you want to measure is applied to the counter GATE input. The counter is loaded with the known count and is programmed to count down while the signal at the GATE input is high. The pulse width equals the counter difference (loaded value minus read value) multiplied by the CLK period.

Perform time-lapse measurement by programming a counter to be edge gated. An edge is applied to the counter GATE input to start the counter. Program the counter to start counting after receiving a low-to-high edge. The time lapse since receiving the edge equals the counter value difference (loaded value minus read value) multiplied by the CLK period.

To perform frequency measurement, program a counter to be level gated and count the number of falling edges in a signal applied to a CLK input. The gate signal applied to the counter GATE input is of known duration. In this case, program the counter to count falling edges at the CLK input while the gate is applied. The frequency of the input signal then equals the count value divided by the gate period. Figure 3-15 shows the connections for a

frequency measurement application. You can also use a second counter to generate the gate signal in this application. If you use a second counter, you must externally invert the signal.

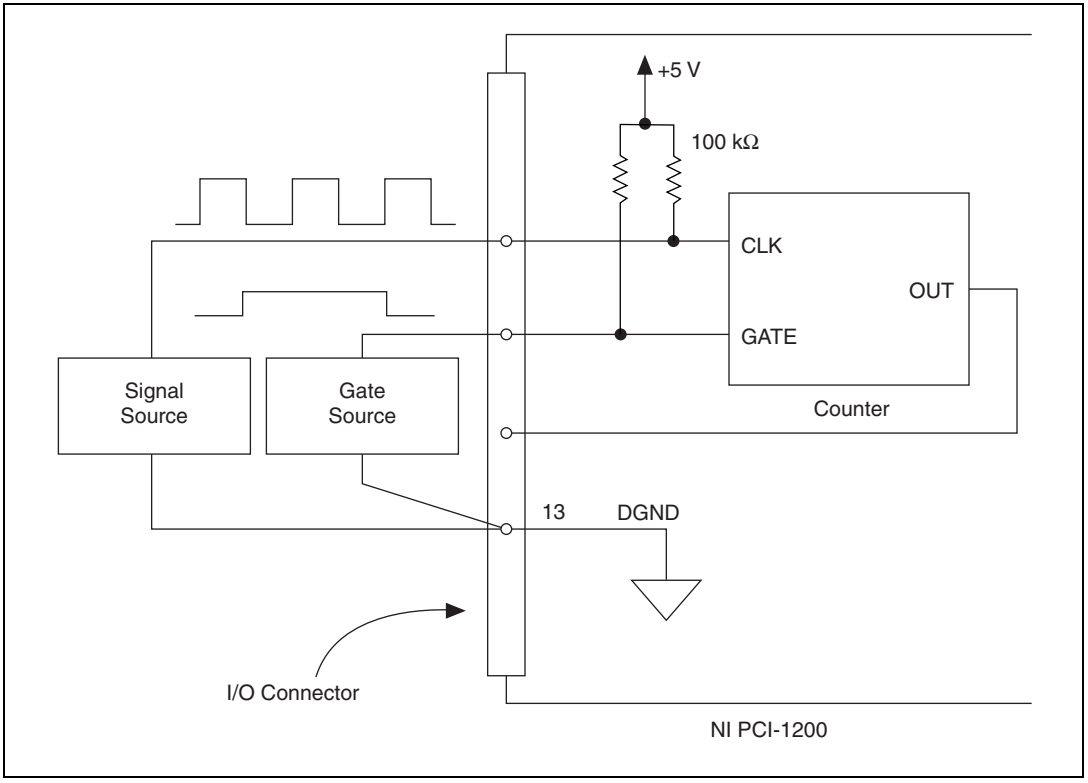


Figure 3-15. Frequency Measurement Application

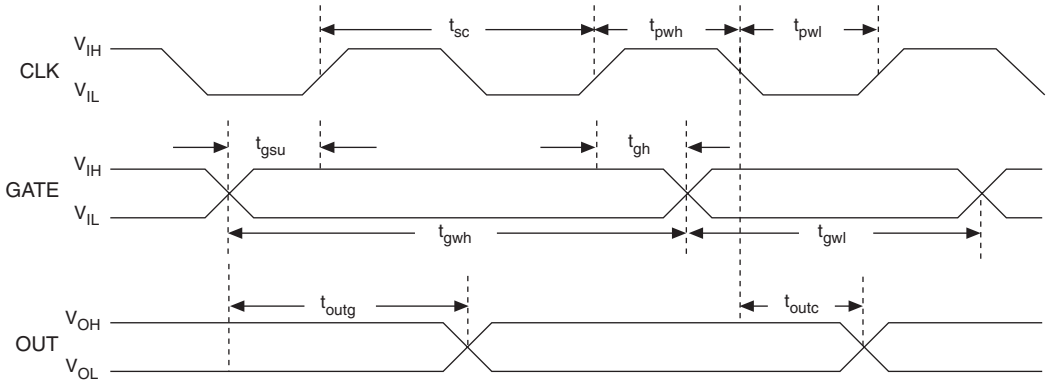
The GATE, CLK, and OUT signals for counters B1 and B2 are available at the I/O connector. The GATE and CLK pins are internally pulled up to +5 V through a 100 kΩ resistor. Refer to Appendix A, *Specifications*, for signal voltage and current specifications.

The following specifications and ratings apply to the 82C53 I/O signals:

- Absolute max voltage input rating –0.5 to +5.5 V, with respect to DGND
- 82C53 digital input specifications (referenced to DGND):
  - V_{ih} input logic high voltage 2.2 V min 5.3 V max
  - V_{il} input logic low voltage –0.3 V min 0.8 V max
  - Input load current –10 µA min +10 µA max

- 82C53 digital output specifications (referenced to DGND):
  - V_{oh} output logic high voltage 3.7 V min —
  - V_{ol} output logic low voltage — 0.45 V max
  - I_{oh} output source current, at V_{oh} — –0.92 mA max
  - I_{ol} output sink current, at V_{ol} — 2.1 mA max

Figure 3-16 shows the timing requirements for the GATE and CLK input signals and the timing specifications for the 82C53 OUT output signals.



t_{sc}	clock period	380 ns minimum
t_{pwh}	clock high level	230 ns minimum
t_{pwl}	clock low level	150 ns minimum
t_{gsu}	gate setup time	100 ns minimum
t_{gh}	gate hold time	50 ns minimum
t_{gwh}	gate high level	150 ns minimum
t_{gwl}	gate low level	100 ns minimum
t_{outc}	output delay from clock ↓	300 ns maximum
t_{outg}	output delay from gate ↓	400 ns maximum

Figure 3-16. General Purpose Timing Signals

The GATE and OUT signals in Figure 3-16 are referenced to the rising edge of the CLK signal.

Timing Specifications

Use the handshaking lines STB* and IBF to synchronize input transfers. Use the handshaking lines OBF* and ACK* to synchronize output transfers.

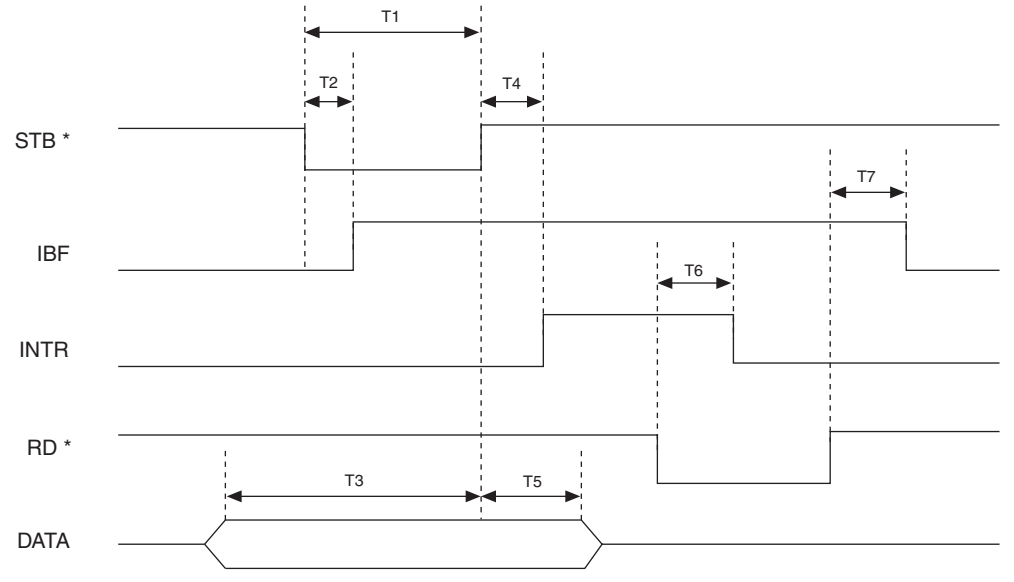
The following signals are used in the mode timing diagrams.

Table 3-6. Signal Names Used in Timing Diagrams

Name	Type	Description
STB*	Input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. IBF is primarily an input acknowledge signal.
ACK*	Input	Acknowledge Input—A low signal on this handshaking line indicates that the data written from the specified port has been accepted. ACK* is primarily a response from the external device that it has received the data from the NI PCI-1200.
OBF*	Output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written from the specified port.
INTR	Output	Interrupt Request—This signal becomes high when the 82C55A is requesting service during a data transfer. Set the appropriate interrupt enable signals to generate this signal.
RD*	Internal	Read Signal—This signal is the read signal generated from the PCI interface circuitry.
WRT*	Internal	Write Signal—This signal is the write signal generated from the PCI interface circuitry.
DATA	Bidirectional	Data Lines at the Specified Port—This signal indicates when the data on the data lines at a specified port is or should be available.

Mode 1 Input Timing

The timing specifications for an input transfer in mode 1 are as follows.



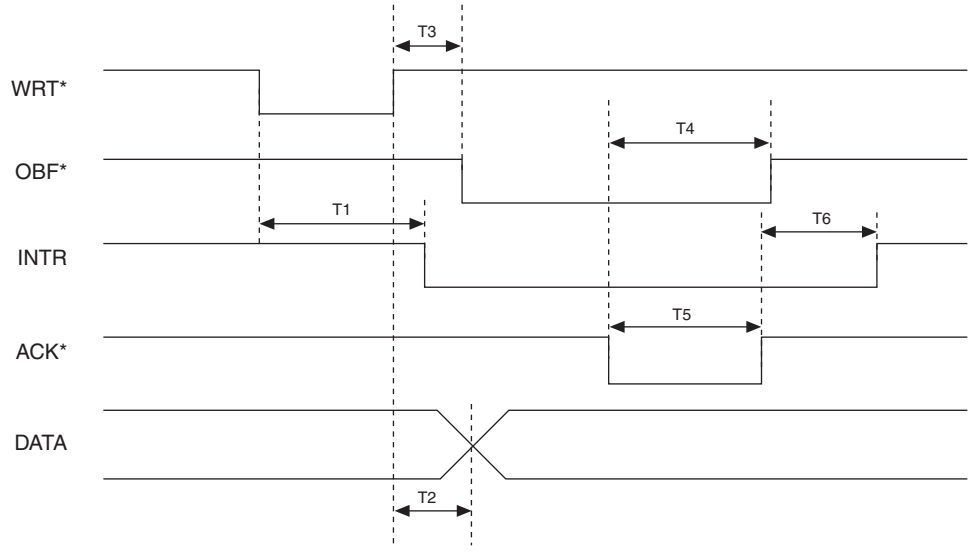
Name	Description	Minimum	Maximum
T1	STB* pulse width	500	—
T2	STB* = 0 to IBF = 1	—	300
T3	Data before STB* = 1	0	—
T4	STB* = 1 to INTR = 1	—	300
T5	Data after STB* = 1	180	—
T6	RD* = 0 to INTR = 0	—	400
T7	RD* = 1 to IBF = 0	—	300

All timing values are in nanoseconds.

Figure 3-17. Mode 1 Timing Specifications for Input Transfers

Mode 1 Output Timing

The timing specifications for an output transfer in mode 1 are as follows.



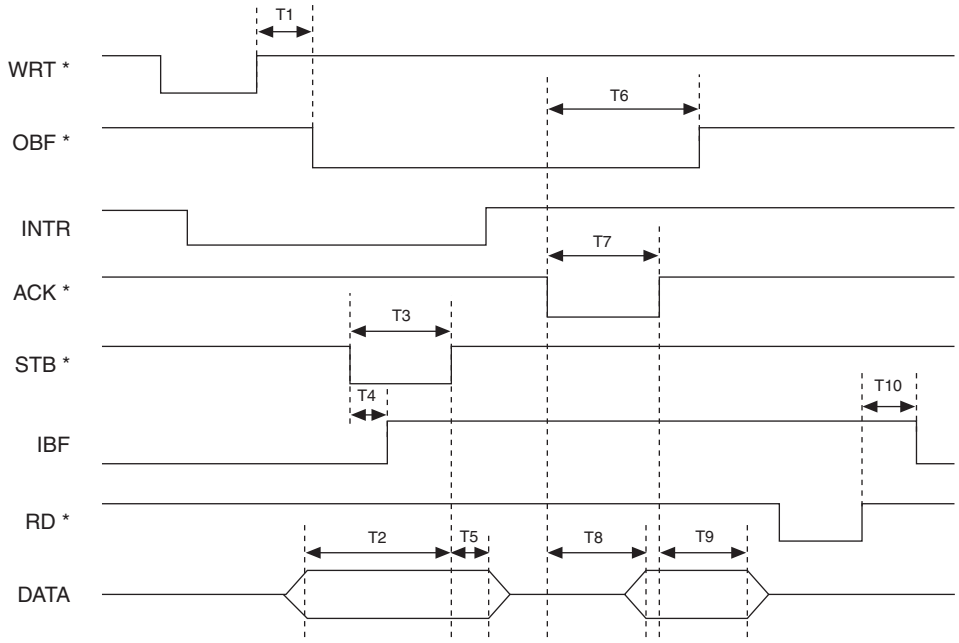
Name	Description	Minimum	Maximum
T1	WRT* = 0 to INTR = 0	—	450
T2	WRT* = 1 to output	—	350
T3	WRT* = 1 to OBF* = 0	—	650
T4	ACK* = 0 to OBF* = 1	—	350
T5	ACK* pulse width	300	—
T6	ACK* = 1 to INTR = 1	—	350

All timing values are in nanoseconds.

Figure 3-18. Mode 1 Timing Specifications for Output Transfers

Mode 2 Bidirectional Timing

The timing specifications for bidirectional transfers in mode 2 are as follows.



Name	Description	Minimum	Maximum
T1	WRT* = 1 to OBF* = 0	—	650
T2	Data before STB* = 1	0	—
T3	STB* pulse width	500	—
T4	STB* = 0 to IBF = 1	—	300
T5	Data after STB* = 1	180	—
T6	ACK* = 0 to OBF* = 1	—	350
T7	ACK* pulse width	300	—
T8	ACK* = 0 to output	—	300
T9	ACK* = 1 to output float	20	250
T10	RD* = 1 to IBF = 0	—	300

All timing values are in nanoseconds.

Figure 3-19. Mode 2 Timing Specifications for Bidirectional Transfers

4

Theory of Operation

This chapter explains the operation of each functional unit of the NI PCI-1200.

Functional Overview

The block diagram in Figure 4-1 shows a functional overview of the device.

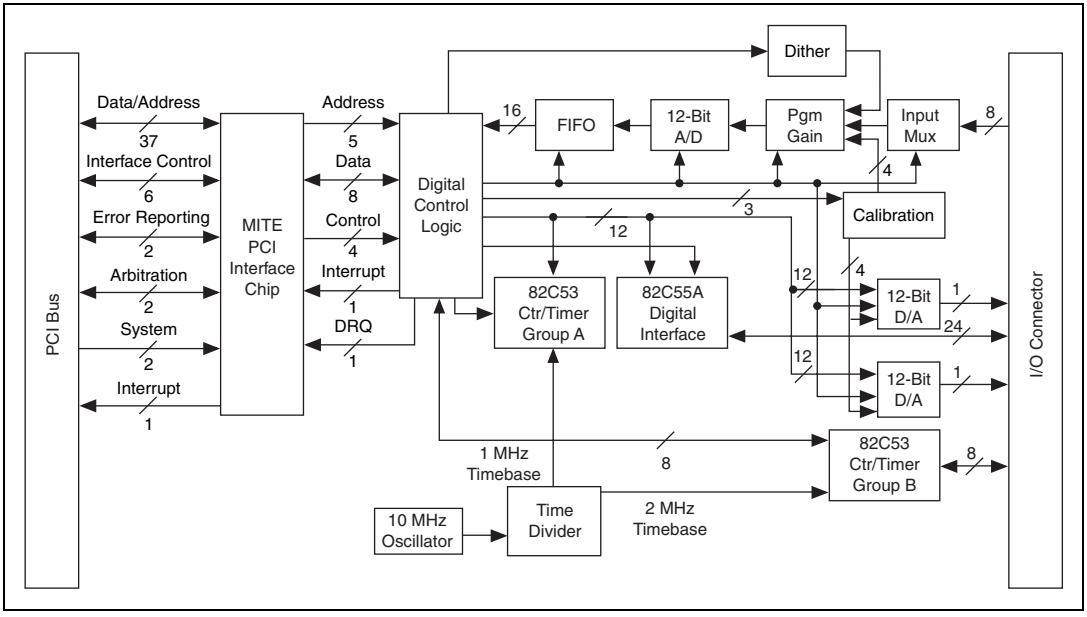


Figure 4-1. NI PCI-1200 Block Diagram

The major components of the NI PCI-1200 are as follows:

- MITE PCI interface circuitry
- TIO circuitry
- AI circuitry
- AO circuitry

- DIO circuitry
- Calibration circuitry

The internal data and control buses interconnect the components. The rest of this chapter explains the theory of operation of each NI PCI-1200 components. Calibration circuitry is discussed in Chapter 5, *Calibration*.

PCI Interface Circuitry

The NI PCI-1200 interface circuitry consists of the MITE PCI interface chip and a digital control logic chip. The MITE PCI interface chip provides a mechanism for the NI PCI-1200 to communicate with the PCI bus. It is an Application Specific Integrated Circuit (ASIC) designed by NI specifically for data acquisition. The digital control logic chip connects the MITE PCI interface chip with the rest of the device. The NI PCI-1200 is fully compliant with *PCI Local Bus Specification, Revision 2.2*. Therefore, the base memory address and interrupt level for the device are stored inside the MITE PCI interface chip at power on. You do not need to set any switches or jumpers. The PCI bus is capable of 8-bit, 16-bit, or 32-bit transfers, but the NI PCI-1200 uses only 8-bit transfers.

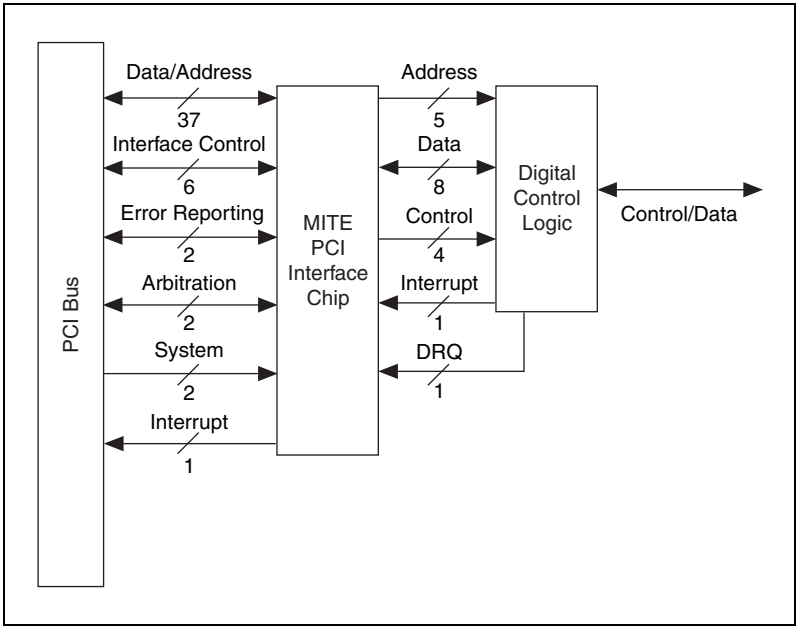


Figure 4-2. PCI Interface Circuitry

The NI PCI-1200 generates an interrupt in the following five cases (each of these interrupts is individually enabled and cleared):

- When a single A/D conversion can be read from the A/D FIFO memory
- When the A/D FIFO is half-full
- When a DAQ operation completes, including when either an OVERFLOW or an OVERRUN error occurs
- When the DIO circuitry generates an interrupt
- When a rising edge signal is detected on the DAC update signal

Timing

The NI PCI-1200 uses two 82C53 counter/timer integrated circuits for internal DAQ and DAC timing and for general purpose I/O timing functions. Figure 4-3 shows a block diagram of both groups of timing circuitry (counter groups A and B).

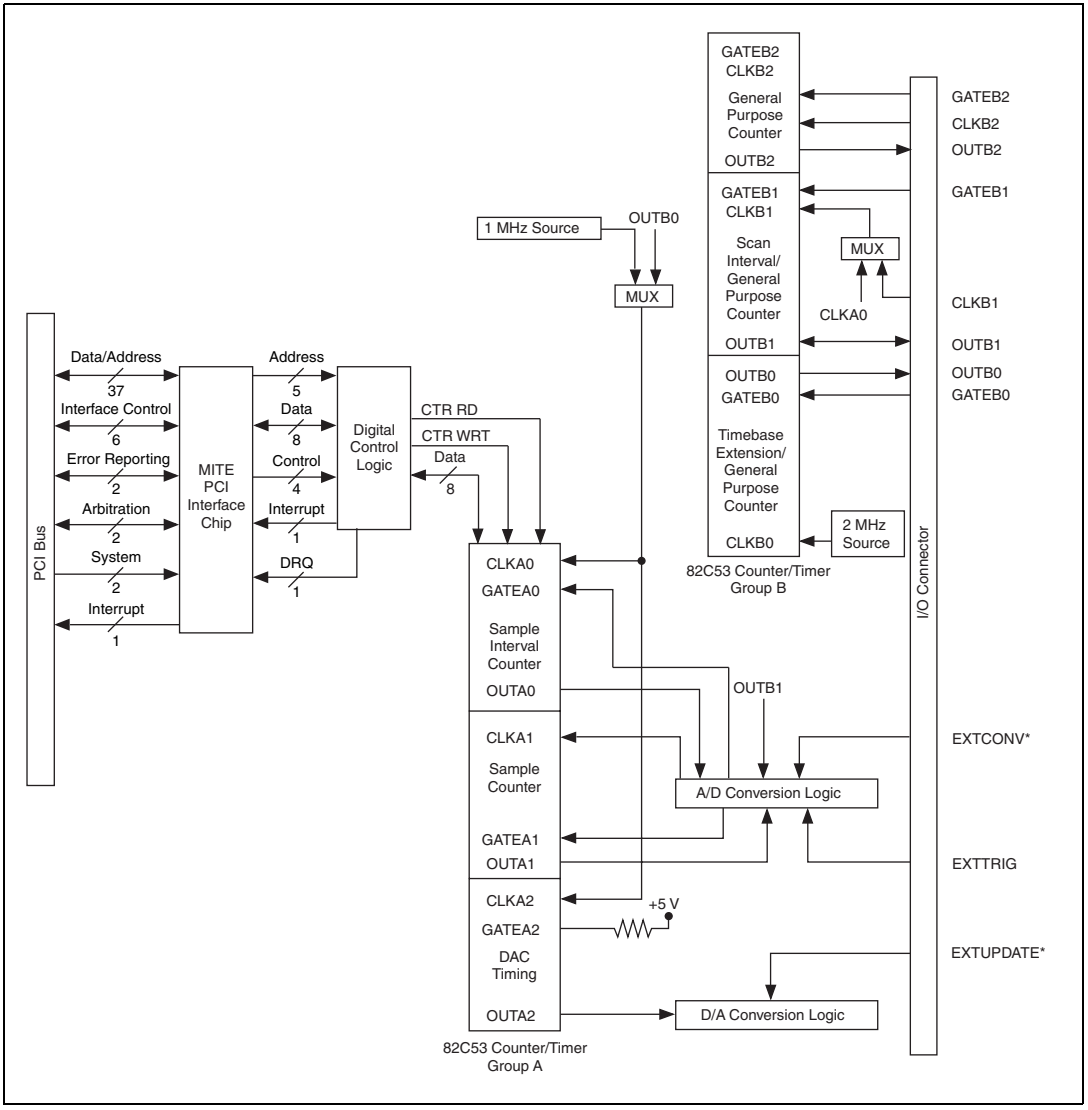


Figure 4-3. Timing Circuitry

Each 82C53 contains three independent 16-bit counter/timers and one 8-bit mode register. Each counter has a CLK input pin, a GATE input pin, and an OUT output pin. You can program all six counter/timers to operate in several timing modes.

The first group of counter/timers, group A, includes A0, A1, and A2. You can use these three counters for internal DAQ and DAC timing, or you can use the three external timing signals, EXTCONV*, EXTTRIG, and EXTUPDATE*, for DAQ and DAC timing.

The second group of counter/timers, group B, includes B0, B1, and B2. You can use counters B0 and B1 for internal DAQ and DAC timing, or you can use the external timing signal CLKB1 for AI timing. If you are not using counters B0 and B1 for internal timing, you can use these counters as general purpose counter/timers. Counter B2 is reserved for external use as a general purpose counter/timer.

For a more detailed description of counter group A and counters B0 and B1, refer to the *Analog Input* and *Analog Output* sections.

Analog Input

The NI PCI-1200 has eight channels of analog input with software-programmable gain and 12-bit A/D conversion. The NI PCI-1200 also contains DAQ timing circuitry for automatic timing of multiple A/D conversions and includes advanced options such as external triggering, gating, and clocking. Figure 4-4 shows a block diagram of the AI circuitry.

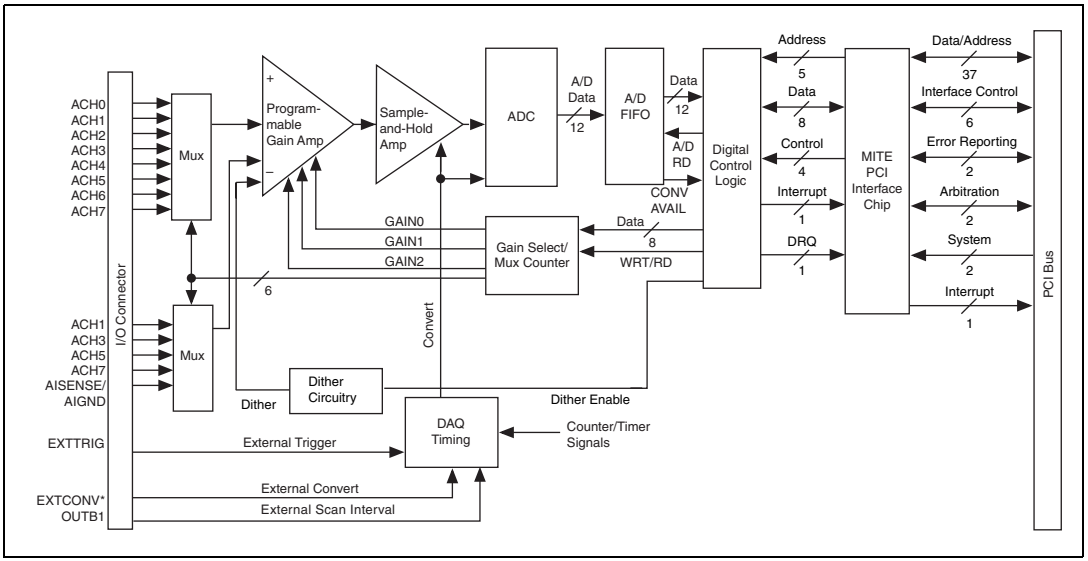


Figure 4-4. Analog Input Circuitry

Analog Input Circuitry

The AI circuitry consists of two AI input multiplexers, multiplexer (mux) counter/gain select circuitry, a software-programmable gain amplifier, a 12-bit ADC, and a 16-bit sign-extended FIFO memory.

One of the input multiplexers has eight AI channels (channels 0 through 7). The other multiplexer is connected to channels 1, 3, 5, and 7 for differential mode. The input multiplexers provide input overvoltage protection of ±35 V powered on and ±25 V powered off.

The mux counters control the input multiplexers. The NI PCI-1200 can perform either single-channel data acquisition or multichannel scanned data acquisition. These two modes are software-selectable. For single-channel data acquisition, select the channel and gain before initiating data acquisition. These gain and multiplexer settings remain constant during the entire DAQ process. For multichannel scanned data acquisition, select the highest numbered channel and gain before initiating data acquisition. Then the mux counter decrements from the highest numbered channel to channel 0 and repeats the process. Thus, you can scan from two to eight channels. Notice that you use the same gain setting for all channels in the scan sequence.

The programmable gain amplifier applies gain to the input signal, allowing an input analog signal to be amplified before being sampled and converted, thus increasing measurement resolution and accuracy. The instrumentation amplifier gain is software-selectable. The NI PCI-1200 provides gains of 1, 2, 5, 10, 20, 50, and 100.

The dither circuitry, when enabled, adds approximately 0.5 LSBrms of white Gaussian noise to the signal to be converted to the ADC. This addition is useful for applications involving averaging, to increase the resolution of the NI PCI-1200 to more than 12 bits, as in calibration. In such applications, which are often lower frequency in nature, noise modulation is decreased and differential linearity is improved by the addition of the dither. For high-speed 12-bit applications not involving averaging, you should disable dither because it only adds noise.

When taking DC measurements, such as when calibrating the device, enable dither and average about 1,000 points to take a single reading. This process removes the effects of 12-bit quantization and reduces measurement noise, resulting in improved resolution. Dither, or additive white noise, has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of input.

The NI PCI-1200 uses a 12-bit successive-approximation ADC. The 12-bit resolution of the counter allows it to resolve its input range into 4,095 different steps. The ADC has input ranges of ±5 V and 0 to 10 V.

When an A/D conversion is complete, the ADC clocks the result into the A/D FIFO. The A/D FIFO is 16 bits wide and 4,096 words deep. This FIFO serves as a buffer to the ADC. The A/D FIFO can collect up to 4,096 A/D conversion values before any information is lost, thus allowing software some time to catch up with the hardware. If you store more than 4,096 values in the A/D FIFO before reading from it, an error condition called *A/D FIFO overflow* occurs, and you lose A/D conversion information.

The ADC output can be interpreted as either straight binary or two's complement, depending on which coding scheme you select. Straight binary is the recommended coding scheme for unipolar input mode. With this scheme, the ADC data is interpreted as a 12-bit straight binary number with a range of 0 to +4,095. Two's complement is the recommended coding scheme for bipolar input mode. With this scheme, the ADC data is interpreted as a 12-bit two's complement number with a range of –2,048 to +2,047. The ADC output is then sign-extended to 16 bits, causing either a leading 0 or a leading F (hex) to be added, depending on the coding and the sign. Thus, data values read from the FIFO are 16-bits wide.

DAQ Operations

This manual uses the phrase *data acquisition operation* (abbreviated as *DAQ operation*) to refer to a sequence of timed A/D conversions. The NI PCI-1200 performs DAQ operations in one of three modes: controlled acquisition mode, free-run acquisition mode, and interval scanning acquisition mode. The NI PCI-1200 performs both single-channel and multichannel scanned data acquisition.

The DAQ timing circuitry consists of various clocks and timing signals that control the DAQ operation. DAQ timing consists of signals that initiate a DAQ operation, time the individual A/D conversions, gate the DAQ operation, and generate scanning clocks. The DAQ operation can be timed either by the timing circuitry or by externally generated signals. These two timing modes are software configurable.

DAQ operations are initiated either externally through EXTTRIG or through software control. The DAQ operation is terminated either internally by counter A1 of the 82C53 (A) counter/timer circuitry, which counts the total number of samples taken during a controlled operation, or through software control in a free-run operation.

Controlled Acquisition Mode

The NI PCI-1200 uses two counters, counter A0 and counter A1, to execute DAQ operations in controlled acquisition mode. Counter A0 counts sample intervals, while counter A1 counts samples. In a controlled acquisition mode DAQ operation, the device performs a specified number of conversions, and then the hardware shuts off the conversions. Counter A0 generates the conversion pulses, and counter A1 gates off counter A0 after the programmed count has expired. The number of conversions in a single controlled acquisition mode DAQ operation is limited to a 16-bit count (65,535 conversions).

Freerun Acquisition Mode

The NI PCI-1200 uses one counter, counter A0, to execute DAQ operations in freerun acquisition mode. Counter A0 continuously generates the conversion pulses as long as GATEA0 is held at a high logic level. The software keeps track of the number of conversions that have occurred and turns off counter A0 either after the required number of conversions has been obtained or after some other user-defined criteria have been met. The number of conversions in a single free-run acquisition mode DAQ operation is unlimited.

Interval Scanning Acquisition Mode

The NI PCI-1200 uses two counters for interval scanning data acquisition. Counter B1 is used to time the scan interval. Counter A0 times the sample interval. In interval scanning AI operations, scan sequences are executed at regular, specified intervals. The amount of time that elapses between consecutive scans within the sequence is the *sample interval*. The amount of time that elapses between consecutive scan sequences is the *scan interval*. LabVIEW, LabWindows/CVI, other application software, and NI-DAQ support only multichannel interval scanning.

Because interval scanning allows you to specify how frequently scan sequences are executed, it is useful for applications in which you need to sample data at regular but relatively infrequent intervals. For example, to sample channel 1, wait 12 µs, then sample channel 0; and if you want to repeat this process every 65 ms, then you should define the operation as follows:

- Start channel: ch1 (which gives a scan sequence of “ch1, ch0”)
- Sample interval: 12 µs
- Scan interval: 65 ms

The first channel will not be sampled until one sample interval from the scan interval pulse. Since the A/D conversion time is 10 µs, the sample interval must be at least this value to ensure proper operation.

Single-Channel Data Acquisition

The NI PCI-1200 executes a single-channel AI operation by performing an A/D conversion on a specified AI channel every sample interval. The sample interval is the amount of time that elapses between successive A/D conversions. The sample interval is controlled either externally by EXTCONV* or internally by counter A0 of the timing circuitry.

To specify a single-channel AI operation, select an AI channel and a gain setting for that channel.

Multichannel Scanned Data Acquisition

The NI PCI-1200 executes a multichannel DAQ operation by repeatedly scanning a sequence of AI channels (the same gain is applied to each channel in the sequence). The channels are scanned in decreasing consecutive order; the highest-numbered channel is the start channel, and channel 0 is the last channel in the sequence.

During each scan sequence, the NI PCI-1200 scans the start channel (the highest-numbered channel) first, then the next highest-numbered channel, and so on until it scans channel 0. The NI PCI-1200 repeats these scan sequences until the DAQ operation is terminated.

For example, if channel 3 is specified as the start channel, then the scan sequence is as follows:

ch3, ch2, ch1, ch0, ch3, ch2, ch1, ch0, ch3, ch2, …

To specify the scan sequence for a multichannel scanned AI operation, select the start channel for the scan sequence.

DAQ Rates

Maximum DAQ rates (number of samples per second) are determined by the conversion period of the ADC plus the sample-and-hold acquisition time. During multichannel scanning, the DAQ rates are further limited by the settling time of the input multiplexers and programmable gain amplifier. After the input multiplexers are switched, the amplifier must be allowed to settle to the new input signal value to within 12-bit accuracy before you perform an A/D conversion, or 12-bit accuracy will not be achieved. The settling time is a function of the gain selected.

Table 4-1 shows the recommended settling time for each gain setting during multichannel scanning. Table 4-2 shows the maximum recommended DAQ rates for both single-channel and multichannel data acquisition. For single-channel scanning, this rate is limited only by the ADC conversion period plus the sample-and-hold acquisition time, specified at 10 µs. For multichannel data acquisition, observing the DAQ rates in Table 4-2 ensures 12-bit resolution. The hardware is capable of multiple scanning at higher rates than those listed in Table 4-2, but 12-bit resolution is not guaranteed.

Table 4-1. Analog Input Settling Time Versus Gain

Gain	Settling Time (Accuracy ±0.024% [±1 LSB])
1	10 µs typ, 14 µs max
2–10	13 µs typ, 16 µs max
20	15 µs typ, 19 µs max
50	27 µs typ, 34 µs max
100	60 µs typ, 80 µs max

Table 4-2. NI PCI-1200 Maximum Recommended DAQ Rates

Acquisition Mode	Gain	Rate
Single-channel	1, 2, 5, 10, 20, 50, 100	100 kS/s
Multichannel	1 2, 5, 10 20 50 100	100 kS/s 77 kS/s 66.6 kS/s 37 kS/s 16.6 kS/s

The recommended DAQ rates in Table 4-2 assume that voltage levels on all the channels included in the scan sequence are within range for the given gain and are driven by low-impedance sources.

Analog Output

The NI PCI-1200 has two channels of 12-bit D/A output. Each AO channel can provide unipolar or bipolar output. The NI PCI-1200 also contains timing circuitry for waveform generation timed either externally or internally. Figure 4-5 shows the AO circuitry.

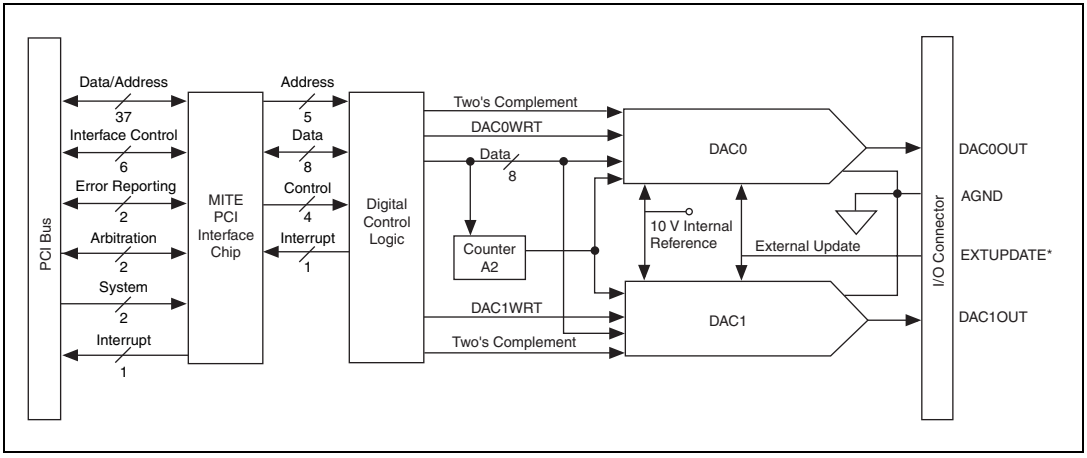


Figure 4-5. Analog Output Circuitry

Analog Output Circuitry

Each AO channel contains a 12-bit DAC. The DAC in each AO channel generates a voltage proportional to the 10 V internal reference multiplied by the 12-bit digital code loaded into the DAC. The voltage output from the two DACs is available at the DAC0OUT and DAC1OUT pins.

You can program each DAC channel for a unipolar voltage output or a bipolar voltage output range. A unipolar output gives an output voltage range of 0.0000 to +9.9976 V. A bipolar output gives an output voltage range of –5.0000 to +4.9976 V. For unipolar output, 0.0000 V output corresponds to a digital code word of 0. For bipolar output, –5.0000 V output corresponds to a digital code word of F800 hex. One LSB is the voltage increment corresponding to an LSB change in the digital code word. For both outputs:

$$1LSB = \frac{10V}{4,095}$$

DAC Timing

There are two modes in which you can update the DAC voltages. In *immediate update mode*, the DAC output voltage is updated as soon as you write to the corresponding DAC. In *delayed update mode*, the DAC output voltage does not change until a low level is detected either from counter A2 of the timing circuitry or EXTUPDATE*. This mode is useful for waveform generation. These two modes are software-selectable.

Digital I/O

The DIO circuitry has an 82C55A integrated circuit. The 82C55A is a general purpose programmable peripheral interface containing 24 programmable I/O pins. These pins represent the three 8-bit I/O ports (A, B, and C) of the 82C55A, as well as PA<0..7>, PB<0..7>, and PC<0..7> on the NI PCI-1200 I/O connector. Figure 4-6 shows the DIO circuitry.

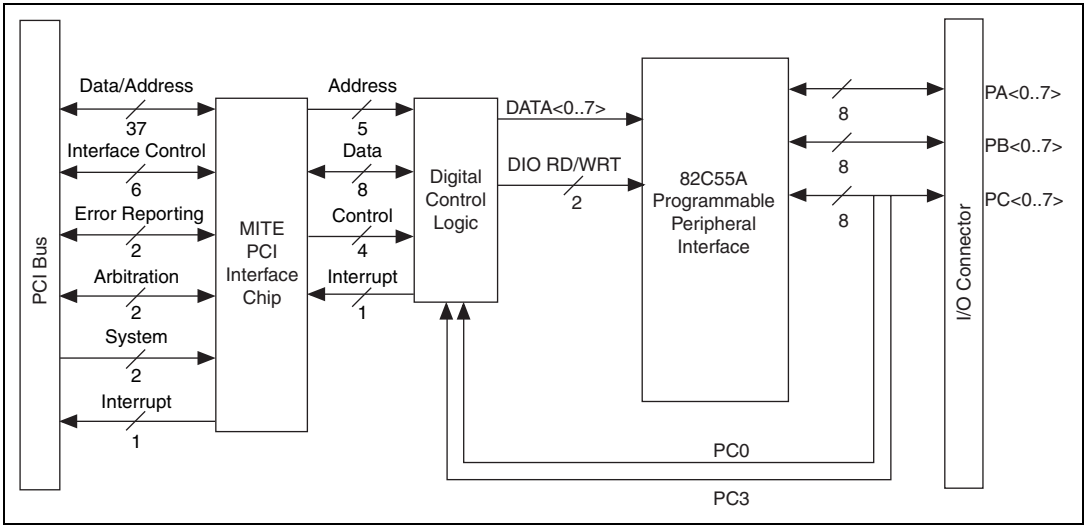


Figure 4-6. Digital I/O Circuitry

All three ports on the 82C55A are TTL-compatible. When enabled, the digital output ports are capable of sinking 2.5 mA of current and sourcing 2.5 mA of current on each DIO line. When the ports are not enabled, the DIO lines act as high-impedance inputs.

5

Calibration

This chapter discusses the calibration procedures for the NI PCI-1200 analog I/O circuitry. However, the NI PCI-1200 is factory calibrated, and NI can recalibrate the device if needed. To maintain the 12-bit accuracy of the NI PCI-1200 AI and AO circuitry, recalibrate at six-month intervals.

There are four ways to perform calibrations.

- If you have LabVIEW, use the 1200 Calibrate VI. This VI is located in the **Calibration and Configuration** palette.
- If you have LabWindows/CVI, use the `Calibrate_1200` function.
- If you do not have LabVIEW or LabWindows/CVI, use the NI-DAQ `Calibrate_1200` function.
- Use your own register-level writes to the calibration DACs and the EEPROM. (Use this method only if NI-DAQ does not support your operating system.)

To calibrate using register-level writes, you need to use the *NI PCI-1200 Register-Level Programmer Manual.*

The NI PCI-1200 is software calibrated. The calibration process involves reading offset and gain errors from the AI and AO data areas and writing values to the appropriate calibration DACs to null the errors. There are four calibration DACs associated with the AI circuitry and four calibration DACs associated with the AO circuitry. After the calibration process is complete, each calibration DAC is at a known value. Because these values are lost when the device is powered down, they are also stored in the onboard EEPROM for future reference.

The factory information occupies one half of the EEPROM and is write-protected. The lower half of the EEPROM contains four user areas for calibration data.

When the NI PCI-1200 is powered on, or the conditions under which it is operating change, you must load the calibration DACs with the appropriate calibration constants.

If you use the NI PCI-1200 with NI-DAQ, LabVIEW, LabWindows/CVI, or other application software, the factory calibration constants are automatically loaded into the calibration DAC the first time a function pertaining to the NI PCI-1200 is called, and again each time you change the configuration (which includes gain). You can, instead, choose to load the calibration DACs with calibration constants from the user areas in the EEPROM or you can recalibrate the NI PCI-1200 and load these constants directly into the calibration DACs. Calibration software is included with the NI PCI-1200 as part of the NI-DAQ software.

Calibration at Higher Gains

The NI PCI-1200 has a maximum gain error of 0.8%. This means that if the device is calibrated at a gain of 1 and if the gain is switched to 100, a maximum error of 32 LSB may result in the reading. Therefore, when you recalibrate the NI PCI-1200, you should perform gain calibration at all other gains (2, 5, 10, 20, 50, and 100), and store the corresponding values in the user-gain calibration data area of the EEPROM, thus ensuring a maximum error of 0.02% at all gains. The NI PCI-1200 is factory-calibrated at all gains, and NI-DAQ automatically loads the correct values into the calibration DACs whenever you switch gains.

Calibration Equipment Requirements

The equipment you use to calibrate the NI PCI-1200 should have a ±0.001% rated accuracy, which is 10 times as accurate as the NI PCI-1200. However, calibration equipment with only four times the accuracy as the NI PCI-1200 and a ±0.003% rated accuracy is acceptable. The inaccuracy of the calibration equipment results only in gain error; offset error is unaffected.

Calibrate the NI PCI-1200 to a measurement accuracy of ±0.5 LSBs, which is within ±0.012% of its input range.

For AI calibration, use a precision DC voltage source, such as a calibrator, with the following specifications:

- Voltage 0 to 10 V
- Accuracy ±0.001% standard
  ±0.003% acceptable

Using the Calibration Function

The `Calibrate_1200` function and the 1200 Calibrate VI can either load the calibration DACs with the factory constants or the user-defined constants stored in the EEPROM, or you can perform your own calibration and directly load these constants into the calibration DACs. To use the `Calibrate_1200` function or the 1200 Calibrate VI for AI calibration, ground an AI channel at the I/O connector for offset calibration and apply an accurate voltage reference to another input channel for gain calibration. You should first configure the ADC for RSE mode, then for the correct polarity at which you want to perform data acquisition.

To use the `Calibrate_1200` function or the 1200 Calibrate VI for AO calibration, the DAC0 and DAC1 outputs must be wrapped back and applied to two other AI channels. You should first configure the AI circuitry for RSE and for bipolar polarity, then configure the AO circuitry for the polarity at which you want to perform output waveform generation.

Refer to your software documentation for more details on the `Calibrate_1200` function and the 1200 Calibrate VI.

A

Specifications

This appendix lists the NI PCI-1200 specifications. These specifications are typical at 25 °C unless otherwise stated.

Analog Input

Input Characteristics

Number of channels ..... 8 single-ended,
8 pseudodifferential, or
4 differential, software-selectable

Type of ADC..... Successive-approximation

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate..... 100 kS/s

Input signal ranges

Device Gain (Software Selectable)	Device Ranges (Software Selectable)	
	±5 V	**0 to 10 V**
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1 V	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

Input coupling ..... DC

Max working voltage
(signal + common mode) ..... In differential or NRSE mode, the negative input/AISENSE should remain within ±5 V (bipolar) or –5 to 2 V (unipolar) of AGND except for the DAQCard-1200, where the values are ±6 V (bipolar) and –6 to 2 V (unipolar). The positive input should remain within –5 V to +10 V of AGND. For the DaQCard-1200 in RSE mode, the input signal referenced to AGND should remain within ±5 V (bipolar) or 0 to 10 V (unipolar).

Overvoltage protection ..... ±35 V powered on, ±25 V powered off

Inputs protected ..... ACH<0..7>

FIFO buffer size ..... 4,096 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA mode ..... Scatter-gather

Dither ..... Available

Transfer Characteristics

Relative accuracy ..... ±0.5 LSB typ dithered, ±1.5 LSB max undithered

DNL ..... ±1 LSB max

No missing codes ..... 12 bits, guaranteed

Offset error

Pregain error after calibration ..... 10 µV max

Pregain error before calibration ..... ±20 mV max

Postgain error after calibration ..... 1 mV max

Postgain error before calibration ..... ±200 mV max

Gain error (relative to calibration reference)

After calibration ..... 0.02% of reading max

Before calibration ..... ±2% of reading max

Amplifier Characteristics

Input impedance

Normal powered on ..... 100 GΩ in parallel with 50 pF

Powered off ..... 4.7 kΩ min

Overload ..... 4.7 kΩ min

Input bias current ..... ±100 pA

Input offset current ..... ±100 pA

CMRR ..... 70 dB, DC to 60 Hz

Dynamic Characteristics

Bandwidth

Small signal (–3 dB)

Gain	Bandwidth
1-10	250 kHz
20	150 kHz
50	60 kHz
100	30 kHz

Settling time for full-scale step

Gain	Settling Time (Accuracy ±0.024% (±1 LSB))
1	10 µs typ, 14 µs max
2–10	13 µs typ, 16 µs max
20	15 µs typ, 19 µs max
50	27 µs typ, 34 µs max
100	60 µs typ, 80 µs max

System noise (including quantization error)

Gain	Dither off	Dither on
1–50	0.3 LSB_{rms}	0.5 LSB_{rms}
100	0.5 LSB_{rms}	0.7 LSB_{rms}

Stability

Recommended warm-up time.....15 min.

Offset temperature coefficient

Pregain.....±15 µV/°C

Postgain .....±100 µV/°C

Gain temperature coefficient .....±40 ppm/°C

Explanation of Analog Input Specifications

Relative accuracy is a measure of the linearity of an ADC. However, relative accuracy is a tighter specification than a *nonlinearity* specification. Relative accuracy indicates the maximum deviation from a straight line for the analog-input-to-digital-output transfer curve. If an ADC has been calibrated perfectly, this straight line is the ideal transfer function, and the relative accuracy specification indicates the worst deviation from the ideal that the ADC permits.

A relative accuracy specification of ±1 LSB is roughly equivalent to, but not the same as, a ±0.5 LSB nonlinearity or integral nonlinearity specification because relative accuracy encompasses both nonlinearity and variable quantization uncertainty, a quantity often mistakenly assumed to be exactly ±0.5 LSB. Although quantization uncertainty is ideally ±0.5 LSB, it can be different for each possible digital code and is actually the analog width of each code. Thus, it is more specific to use relative accuracy as a measure of linearity than it is to use what is normally called nonlinearity, because relative accuracy ensures that the *sum* of quantization uncertainty and A/D conversion error does not exceed a given amount.

Integral nonlinearity (INL) in an ADC is an often ill-defined specification that should indicate the overall A/D transfer linearity of a converter. The manufacturer of the ADC chip NI uses on the NI PCI-1200 specifies its integral nonlinearity by stating that the analog center of any code does not deviate from a straight line by more than ±1 LSB. This specification is misleading because, although a particularly wide code center may be found within ±1 LSB of the ideal, one of its edges may be well beyond ±1.5 LSB;

thus, the ADC would have a relative accuracy of that amount. NI tests its devices to ensure that they meet all three linearity specifications defined in this appendix.

Differential nonlinearity (DNL) is a measure of deviation of code widths from the theoretical value of 1 LSB. The width of a given code is the size of the range of analog values that can be input to produce that code, ideally 1 LSB. A specification of ±1 LSB differential nonlinearity ensures that no code has a width of 0 LSBs (that is, no missing codes) and that no code width exceeds 2 LSBs.

System noise is the amount of noise seen by the ADC when there is no signal present at the input of the device. The amount of noise that is reported directly (without any analysis) by the ADC is not necessarily the amount of real noise present in the system, unless the noise is considerably greater than 0.5 LSB rms. Noise that is less than this magnitude produces varying amounts of flicker, and the amount of flicker seen is a function of how near the real mean of the noise is to a code transition. If the mean is near or at a transition between codes, the ADC flickers evenly between the two codes, and the noise is very near 0.5 LSB. If the mean is near the center of a code and the noise is relatively small, very little or no flicker is seen, and the noise is reported by the ADC as nearly 0 LSB. From the relationship between the mean of the noise and the measured rms magnitude of the noise, the character of the noise can be determined. NI has determined that the character of the noise in the NI PCI-1200 is fairly Gaussian, so the noise specifications given are the amounts of pure Gaussian noise required to produce our readings.

Explanation of Dither

The *dither circuitry*, when enabled, adds approximately 0.5 LSB rms of white Gaussian noise to the signal to be converted to the ADC. This addition is useful for applications, such as calibration, that involves averaging to increase the resolution of the NI PCI-1200 to more than 12 bits. In such applications, which are often lower frequency in nature, noise modulation is decreased and differential linearity is improved by the addition of dither. For high-speed 12-bit applications not involving averaging, dither should be disabled because it only adds noise.

When taking DC measurements, such as when calibrating the device, enable dither and average about 1,000 points to take a single reading. This process removes the effects of 12-bit quantization and reduces measurement noise, resulting in improved resolution. Dither, or additive white noise, has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of input.

Explanation of DAQ Rates

Maximum DAQ rates (number of S/s) are determined by the conversion period of the ADC plus the sample-and-hold acquisition time, which is specified at 10 µs. During multichannel scanning, the DAQ rates are further limited by the settling time of the input multiplexers and programmable gain amplifier. After the input multiplexers are switched, the amplifier must be allowed to settle to the new input signal value to within 12-bit accuracy. The settling time is a function of the gain selected.

Analog Output

Output Characteristics

Number of channels.....2 voltage

Resolution.....12 bits, 1 in 4,096

Typical update rate .....20 S/s–1 kS/s, system dependent

Type of DAC .....Double buffered

Data transfers.....Interrupts, programmed I/O

Transfer Characteristics

Relative accuracy (INL) .....±0.25 LSB typ, ±0.50 LSB max

DNL .....±0.25 LSB typ, ±0.75 LSB max

Monotonicity .....12 bits, guaranteed

Offset error

- After calibration.....±0.2 mV max
- Before calibration .....±50 mV max

Gain error (relative to internal reference)

- After calibration.....±0.01% of reading max
- Before calibration .....±1% of reading max

Voltage Output

Ranges .....0 to 10 V, ±5 V, software selectable

Output coupling .....DC

Output impedance ..... 0.2 Ω typ

Current drive ..... ±2 mA

Protection ..... Short circuit to ground

Power-on state..... 0 V

Dynamic Characteristics

Settling time to full-scale range (FSR)..... 5 µs

Stability

Offset temperature coefficient ..... ±50 µV/°C

Gain temperature coefficient..... ±30 ppm/°C

Explanation of Analog Output Specifications

Relative accuracy in a D/A system is the same as nonlinearity because no uncertainty is added due to code width. Unlike an ADC, every digital code in a D/A system represents a specific analog value rather than a range of values. The relative accuracy of the system is therefore limited to the worst-case deviation from the ideal correspondence (a straight line), except noise. If a D/A system has been perfectly calibrated, the relative accuracy specification reflects its worst-case absolute error.

DNL in a D/A system is a measure of deviation of code width from 1 LSB. In this case, code width is the difference between the analog values produced by consecutive digital codes. A specification of ±1 LSB differential nonlinearity ensures that the code width is always greater than 0 LSBs (guaranteeing monotonicity) and is always less than 2 LSBs.

Digital I/O

Number of channels ..... 24 I/O (three 8-bit ports; uses 82C55A PPI)

Compatibility ..... TTL

Digital logic levels

Level	Min	Max
Input low voltage	–0.3 V	0.8 V
Input high voltage	2.2 V	5.3 V
Output low voltage (I_{OUT} = 2.5 mA)	—	0.4 V
Output high voltage (I_{OUT} = –40 µA) (I_{OUT} = –2.5 mA)	 4.2 V 3.7 V	 — —

Power-on state .....All ports mode 0 input

Protection.....–0.5 to 5.5 V powered on,
±0.5 V powered off

Data transfers.....Interrupts, programmed I/O

Timing I/O

Number of channels.....3 counter/timers

Protection.....–0.5 to 5.5 V powered on,
±0.5 V powered off

Resolution

Counter/timers .....16 bits

Compatibility .....TTL

Base clock available .....2 MHz

Base clock accuracy.....±50 ppm max

Max source frequency.....8 MHz

Min source pulse duration .....125 ns

Min gate pulse duration .....50 ns

Digital logic levels

Level	Min	Max
Input low voltage	–0.3 V	0.8 V
Input high voltage	2.2 V	5.3 V
Output low voltage (I_{OUT} = 2.1 mA)	—	0.45 V
Output high voltage (I_{OUT} = -0.92 mA)	3.7 V	—

Protection ..... –0.5 to 5.5 V powered on,
±0.5 V powered off

Data transfer ..... Interrupts, programmed I/O

Digital Trigger

Compatibility ..... TTL

Response ..... Rising edge

Pulse width ..... 50 ns min

Bus Interface

Type ..... Slave

Power Requirement

Power consumption ..... 425 mA at +5 VDC (±5%)

Power available at I/O connector ..... +4.65 to +5.25 V fused at 1 A

Physical

Dimensions ..... 17.45 by 10.56 cm
(6.87 by 4.16 in.)

I/O connector ..... 50-pin male

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth .....42 V, Installation Category II

Channel-to-channel.....42 V, Installation Category II

Environmental

Operating temperature .....0 to 50 °C

Storage temperature.....–55 to 150 °C

Humidity.....5 to 90% RH, noncondensing

Maximum altitude.....2,000 meters

Pollution degree (indoor use only) 2

Safety

The NI PCI-1200 meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3101-1:1993, UL 3111-1:1994, UL 3121:1998
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions .....EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity .....Evaluated to EN 61326:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by the product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

B

Technical Support and Professional Services

Visit the following sections of the National Instruments Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources include the following:
  - **Self-Help Resources**—For immediate answers and solutions, visit our extensive library of technical support resources available in English, Japanese, and Spanish at ni.com/support. These resources are available for most products at no cost to registered users and include software drivers and updates, a KnowledgeBase, product manuals, step-by-step troubleshooting wizards, hardware schematics and conformity documentation, example code, tutorials and application notes, instrument drivers, discussion forums, a measurement glossary, and so on.
  - **Assisted Support Options**—Contact NI engineers and other measurement and automation professionals by visiting ni.com/ask. Our online system helps you define your question and connects you to the experts by phone, discussion forum, or email.
- **Training**—Visit ni.com/custed for self-paced tutorials, videos, and interactive CDs. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, NI Alliance Program members can help. To learn more, call your local NI office or visit ni.com/alliance.

If you searched ni.com and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Prefix	Meanings	Value
p-	pico	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Numbers/Symbols

°	degrees
>	greater than
≥	greater than or equal to
<	less than
–	negative of, or minus
≠	not equal to
Ω	ohms
%	percent
±	plus or minus
+	positive of, or plus
+5V	+5 volts signal

A

A	amperes
A/D	analog-to-digital
AC	alternating current
ACH <0..7>	analog channel 0 through 7 signals
ACK*	acknowledge input signal
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
AGND	analog ground signal
AI	analog input
AISENSE/AIGND	analog input sense/analog input ground signal
ANSI	American National Standards Institute
AO	analog output
AWG	American Wire Gauge

C

C	Celsius
CALDAC	calibration digital-to-analog converter
CH	channel
CLKB1, CLKB2	counter B1, B2 clock signals
cm	centimeters
CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
CNTINT	counter interrupt signal

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC OUTPUT UPDATE	DAC output update signal
DAC0OUT, DAC1OUT	digital-to-analog converter 0, 1 output signals
DACWRT	DAC write signal
DAQ	data acquisition—a system that uses the computer to collect, receive, and generate electrical signals
DATA	data lines at the specified port signal
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB=20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DI	digital input
DIFF	differential
DIO	digital input/output
DMA	direct memory access
DNL	differential nonlinearity
DO	digital output

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
EXTCONV*	external convert signal
EXTTRIG	external trigger signal
EXTUPDATE*	external update signal

F

F	farad
FIFO	first in first out memory buffer
FSR	full-scale range
ft	feet

G

GATB <0..2>	counter B0, B1, B2 gate signals
GATE	gate signal

H

hex	hexadecimal
Hz	hertz

I

I/O	input/output
IBF	input buffer full signal
in.	inches

INL	integral nonlinearity—a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry
INTR	interrupt request signal

L

LED	light-emitting diode
LSB	least significant bit

M

m	meters
max	maximum
MB	megabytes of memory
min	minimum
min.	minutes
MIO	multifunction I/O
MSB	most significant bit
mux	multiplexer—a switching device with multiple inputs that connects one of its inputs to its output

N

NRSE	nonreferenced single-ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground

O

OBF*	output buffer full signal
OUTB0, OUTB1	counter B0, B1 output signals
OVERFLOW	overflow error
OVERRUN	overrun error

P

PA, PB, PC <0..7>	port A, B, or C 0 through 7 signals
PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
port	digital port, consisting of four or eight lines of digital input and/or output
postriggering	technique used on a DAQ device to acquire a programmed number of samples after trigger conditions are met.
POSTTRIG	posttrigger mode
PPI	programmable peripheral interface
ppm	parts per million
PRETRIG	pretrigger mode
pretriggering	technique used on a DAQ device to keep a continuous buffer filled with data, so that when the trigger conditions are met, the sample includes the data leading up to the trigger condition

R

RD*	read signal
R_{EXT}	external resistance
rms	root mean square

RSE	referenced single-ended mode—all measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system

S

s	seconds
S	samples
scan	one or more analog or digital input samples. Typically, the number of input samples in a scan is equal to the number of channels in the input group. For example, one pulse from the scan clock produces one scan which acquires one new sample from every analog input channel in the group.
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ devices in the noisy PC environment
signal conditioning	manipulation of signals to prepare them for digitizing
STB	strobe input signal

T

t_d	minimum period
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gwh}	gate high level
t_{gwl}	gate low level
t_m	minimum pulse width
t_{outc}	output delay from gate
t_{outg}	output delay from clock
t_{pwh}	clock high level

t_{pwl}	clock low level
TTL	transistor-transistor logic
typ	typical

V

V	volts
V_{cm}	common-mode noise
VDC	volts direct current
V_{diff}	differential input voltage
V_{EXT}	external voltage
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program.
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	positive/negative input voltage
V_m	measured voltage
Vrms	volts, root-mean-square
V_s	signal source

W

W	watts
WRT*	write signal

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