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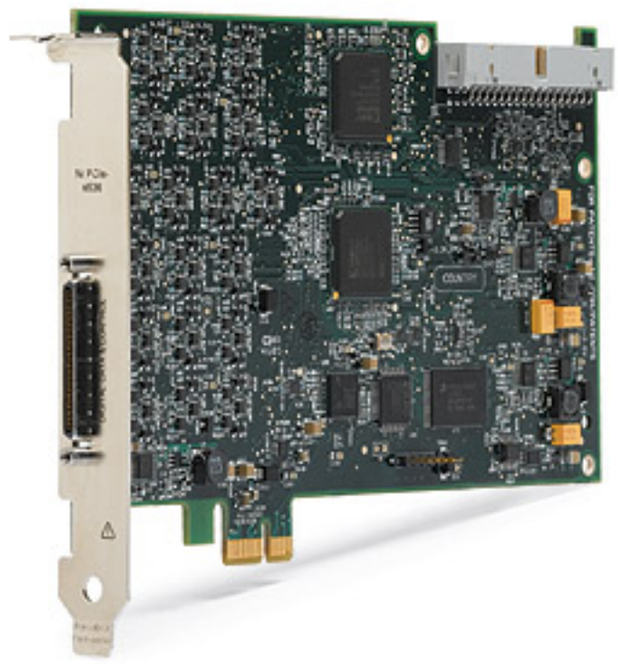
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Requirements and Compatibility | Detailed Specifications
For user manuals and dimensional drawings, visit the product page resources tab on ni.com.

Last Revised: 2010-04-08 11:04:00.0

NI PCIe/PXIe 6535, 6536, 6537





- 10 MHz maximum clock rate
- 40 MB/s maximum throughput
- 32 channels with per-channel directional control
- Selectable voltage levels of 2.5 and 3.3 V (5 V compatible)
- Synchronous and asynchronous timing modes
- Software compatible with NI 6533 and NI 6534 NI-DAQmx applications

Overview

NI 6535, NI 6536, and NI 6537 digital I/O devices are high-speed 32-bit interfaces built on PCI Express bus technology. These cost-effective devices provide an ideal way to interface with a variety of digital applications requiring a high number of channels for digital I/O including high-speed functional digital tests, handshaking, chip testing, pattern generation, memory testing, and logic vector capture. This family features maximum clock rates of 10, 25, or 50 MHz; selectable voltage levels compatible with 2.5, 3.3, and 5 V TTL logic; and individually configured pins for input or output. With both synchronous and asynchronous timing modes, handshaking, and a software API designed around the NI-DAQmx driver , NI 6535/36/37 devices have the flexibility to meet the requirements of semiconductor, consumer electronics, and communications applications.

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Requirements and Compatibility

OS Information

- Windows XP
- Windows XP x64

Driver Information

- NI-DAQmx

Software Compatibility

- ANSI C/C++
- LabVIEW
- LabVIEW Base Development System
- Measurement Studio
- Measurement Studio .NET Support
- Visual Studio
- Visual Studio .NET

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Application and Technology

Digital Interfacing

- Use NI 6535/36/37 devices to interface digital systems and devices directly with PC-based applications
- Control, communicate with, or send data to a digital device or system
- Analyze and record digital data
- Perform bidirectional communications with handshaking

Timing Modes

- Pattern I/O or sample clock (synchronous) – transfer patterns using an internal or external clock signal
- Burst handshaking (synchronous) – handshake an NI 6535, NI 6536, or NI 6537 device and the peripheral device during synchronous transfer to maximize the transfer rate
- Handshaking I/O (asynchronous) – transfer patterns when both the NI 6535, NI 6536, or NI 6537 device and the peripheral device are ready
- On-demand (unstrobed or static I/O) – acquire or generate data through software-timed commands

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• Change detection – acquire data whenever a change occurs on one or more digital lines

High Signal Quality
NI 6535/36/37 devices feature an improved architecture, offering not only higher clock rates up to 50 MHz at low cost but also superior signal integrity and impedance matching.

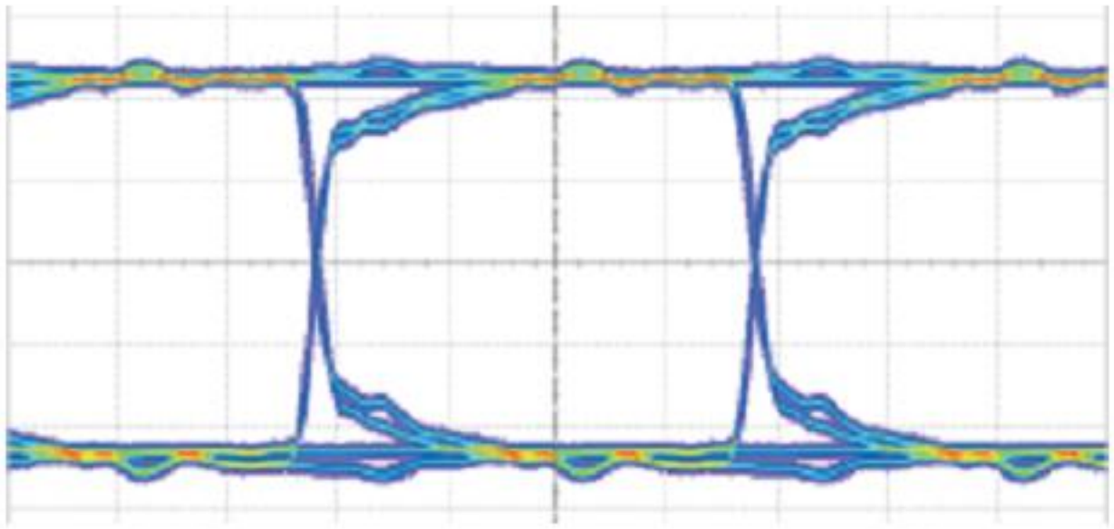


Figure 1. Eye Diagram of PXIe-6537 at 50 MHz

Improved Architecture Compatible with NI 6533
and NI 6534 Applications
These devices are ideal replacements for future-proofing applications currently using NI 6533/34 devices.
• NI 6535/36/37 devices are software-compatible with existing NI 6533/34 NI-DAQmx applications
• You can interface to existing NI 6533/34 fixtures and terminal blocks with the NI 653x cable adapter
• NI 6535/36/37 devices are compatible with most NI 6533/34 timing modes – pattern I/O, handshaking, change detection, and burst



Figure 2. You can use NI 6535/36/37 devices with an NI 653x cable adapter to connect to existing NI 6533/34 applications.

• In comparison to legacy digital I/O boards, NI 6535/36/37 devices have improved signal quality. In Figure 3, the top eye diagram is from an NI PXIe-6535 generating at 10 MHz. The bottom diagram shows an NI PXI-6534 generating a 10 MHz signal using signal termination recommended by NI.

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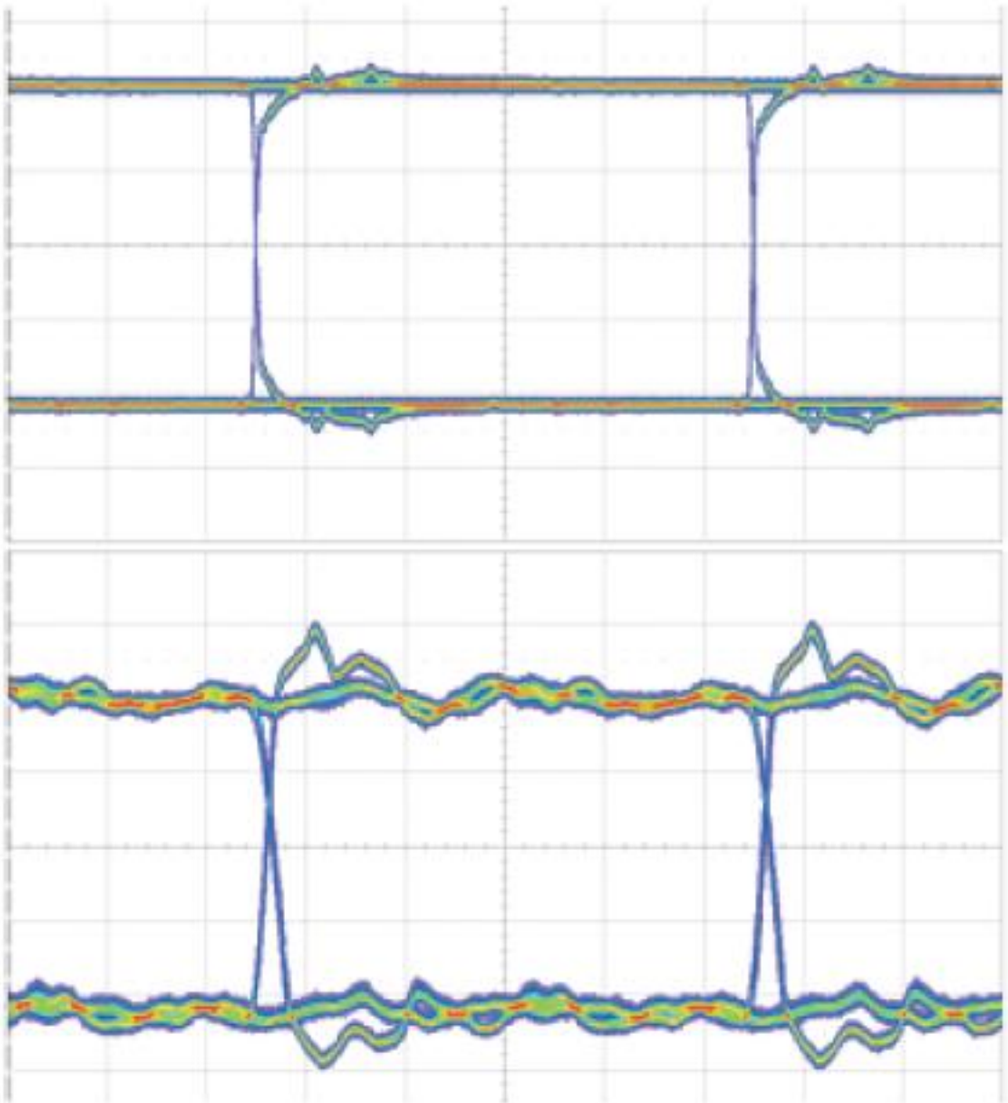


Figure 3. Eye Diagram Comparison of the NI 6535 (top) with the NI 6534 (bottom) Using Recommended Signal Termination

Connectivity Options

To meet connectivity requirements for high-speed digital applications, you can use NI 6535/36/37 devices with a variety of accessories.

- A CB-2162 connector block
- A 50 ½ shielded flying lead cable
- A VHDCI high-density connector

High-Speed Data Streaming

- Generate and acquire larger digital waveforms with PCI Express high-speed devices, using the ideal, low-cost NI 6535/36/37 devices
  Stream continuously at up to 200 MB/s of data
- Stream data from the host computer's memory or high-end storage solution such as NI RAID arrays and controllers
- Use for applications requiring high speeds and fast streaming capabilities such as LCD testing, wireless protocols, ADC/DAC interfacing, or digital pattern capture
- Visit ni.com/streaming for more information

Multidevice Synchronization

These products use the PXI trigger bus or RTSI bus to send and receive clock and trigger signals to and from other NI 6535/36/37 devices in your system. With these capabilities, you can create synchronized systems with large numbers of digital I/O lines.

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Calibration

NI measurement hardware is calibrated to ensure measurement accuracy and verify that the device meets its published specifications. NI offers a number of calibration services to help maintain the ongoing accuracy of your measurement hardware. These services allow you to be completely confident in your measurements, and help you maintain compliance to standards like ISO 9001, ANSI/NCSL Z540-1 and ISO/IEC 17025. To learn more about NI calibration services or to locate a qualified service center near you, contact your local sales office or visit ni.com/calibration.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

- **Classroom training in cities worldwide** - the most comprehensive hands-on training taught by engineers.
- **On-site training at your facility** - an excellent option to train multiple employees at the same time.
- **Online instructor-led training** - lower-cost, remote training if classroom or on-site courses are not possible.
- **Course kits** - lowest-cost, self-paced training that you can use as reference guides.
- **Training memberships** and training credits - to buy now and schedule training later.

Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

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Our Professional Services Team is comprised of NI applications engineers, NI Consulting Services, and a worldwide National Instruments Alliance Partner program of more than 600 independent consultants and integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

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Detailed Specifications

This document provides the specifications for the NI PXIe/PCIe-6535/6536/6537 (NI 6535/6536/6537).

Typical values are representative of an average unit operating at room temperature. Specifications are subject to change without notice. For the most recent NI 6535/6536/6537 specifications, visit ni.com/manuals .

Channel Specifications

Specification	Value	
Number of data channels	32	
Direction control of data channels	Per channel	
Number of Programmable Function Interface (PFI) channels	6	
Direction control of PFI channels	Per channel	
Number of RTSI/PXI trigger channels	**PXI Express**	**PCI Express**
	10 (PXI_TRIG<0..7>, PXIe_DSTARB, PXIe_DSTARC)	8 (RTSI <0..7>)
Direction control of RTSI/PXI trigger channels	RTSI <0..7>/PXI_TRIG<0..7>: Bidirectional; per channel PXIe_DSTARB: Unidirectional input (PXI Express only) PXIe_DSTARC: Unidirectional output (PXI Express only)	
Number of Sample clock terminals	3 bidirectional clock terminals (PFI 4, PFI 5, RTSI 7) 1 exported clock terminal (PXIe_DSTARC) (PXI Express only) 2 clock source terminals (PXIe_DSTARA, PXI_STAR) (PXI Express only)	

Generation Channels (Data and PFI <0..5> Channels)

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Specification	Value			
Generation voltage families	2.5 V, 3.3 V (5 V TTL compatible)			
Generation signal type	Single-ended			
Generation voltage levels	**Low Voltage Levels**		**High Voltage Levels**	
	Typical	**Maximum**	**Minimum**	**Typical**
2.5 V	0.0 V	0.1 V	2.4 V	2.5 V
3.3 V	0.0 V	0.1 V	3.2 V	3.3 V
5.0 V	0.0 V	0.1 V	3.2 V	3.3 V
Output impedance	50 Ω, nominal			
Maximum DC drive strength	±16 mA at 2.5 V ±32 mA at 3.3 V			
Data channel driver enable/disable control	Per channel			
Channel power-up state	Software programmable (Tristate, 0, or 1 at 2.5 V or 3.3 V)			
Output protection	The device can indefinitely sustain a short to any voltage between 0 V and 5 V.			

Acquisition Channels (Data and PFI <0..5> Channels)

Specification	Value		Comments
Acquisition voltage families	2.5 V, 3.3 V (5 V TTL compatible)		—
Acquisition voltage levels	**Low Voltage Thresholds**	**High Voltage Thresholds**	—
	Maximum	**Minimum**	
2.5 V	0.75 V	1.75 V	
3.3 V	1.00 V	2.30 V	
5.0 V	1.00 V	2.30 V	
Input impedance	High-impedance (50 kΩ to ground)		—
Input protection	–1 V to +6 V		Diode clamps in the design may provide additional protection outside this range.

Timing Specifications

Sample Clock

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<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>Sample clock sources</td><td colspan="2">1. On Board Clock (Sample Clock Timebase with divider)
2. PFI <4..5>
3. PXI_TRIG 7 (PXI backplane—PXI Express only) RTSI 7 (RTSI bus—PCI Express only)
4. PXI_STAR (PXI backplane—PXI Express only)
5. PXIe_DSTARA (PXI backplane—PXI Express only)</td><td rowspan="2">Refer to the Clocking diagram in the NI 6535/6536/6537 Help for an illustration of the various clock and timebase sources.</td></tr>
<tr><td>Sample clock timebase sources</td><td colspan="2">1. 200 MHz Timebase (internal oscillator)
2. PFI <0..5>
3. PXI_TRIG<0..6> (PXI backplane—PXI Express only) RTSI <0..7> (RTSI bus—PCI Express only)
4. PXIe_DSTARB (PXI backplane—PXI Express only)</td></tr>
<tr><td>On Board Clock frequency range</td><td colspan="2">NI 6535: 48 Hz to 10 MHz Configurable to 200 MHz/N; 20 ≤ N ≤ 4,194,307
NI 6536: 48 Hz to 25 MHz Configurable to 200 MHz/N; 8 ≤ N ≤ 4,194,307
NI 6537: 48 Hz to 50 MHz Configurable to 200 MHz/N; 4 ≤ N ≤ 4,194,307</td><td>—</td></tr>
<tr><td rowspan="2">Imported Sample clock frequency range</td><td>PFI <4..5>
PXIe_DSTARA (PXIe Only)</td><td>PXI_TRIG 7 (PXIe Only)
RTSI 7 (PCIe Only)</td><td rowspan="2">—</td></tr>
<tr><td>NI 6535: 0 Hz to 10 MHz
NI 6536: 0 Hz to 25 MHz
NI 6537: 0 Hz to 50 MHz</td><td>NI 6535: 0 Hz to 10 MHz
NI 6536/6537: 0 Hz to 25 MHz</td></tr>
<tr><td rowspan="2">Minimum detectable Sample clock pulse width</td><td>PFI <4..5>
PXIe_DSTARA (PXIe Only)</td><td>PXI_TRIG 7 (PXIe Only)
RTSI 7 (PCIe Only)</td><td rowspan="2">Positive and negative pulse width at voltage thresholds.</td></tr>
<tr><td>8 ns</td><td>15 ns</td></tr>
<tr><td rowspan="2">Imported timebase clock frequency range</td><td>PFI <0..5>
PXIe_DSTARB (PXIe Only)</td><td>PXI_TRIG 7 (PXIe Only)
RTSI 7 (PCIe Only)</td><td rowspan="2">—</td></tr>
<tr><td>NI 6535: 0 Hz to 10 MHz
NI 6536: 0 Hz to 25 MHz
NI 6537: 0 Hz to 50 MHz</td><td>NI 6535: 0 Hz to 10 MHz
NI 6536/6537: 0 Hz to 25 MHz</td></tr>
<tr><td rowspan="2">Minimum detectable imported timebase clock pulse width</td><td>PFI <4..5>
PXIe_DSTARB (PXIe Only)</td><td>PXI_TRIG 7 (PXIe Only)
RTSI 7 (PCIe Only)</td><td rowspan="2">Positive and negative pulse width at voltage thresholds.</td></tr>
<tr><td>6.5 ns</td><td>15 ns</td></tr>
<tr><td rowspan="2">Exported Sample clock destinations</td><td>Generation</td><td>Acquisition</td><td rowspan="2">—</td></tr>
<tr><td>1. PFI 4
2. RTSI 7 (PCI Express only) PXI_TRIG7 (PXI Express only)
3. PXIe_DSTARC (PXI Express only)</td><td>PFI 5</td></tr>
</table>

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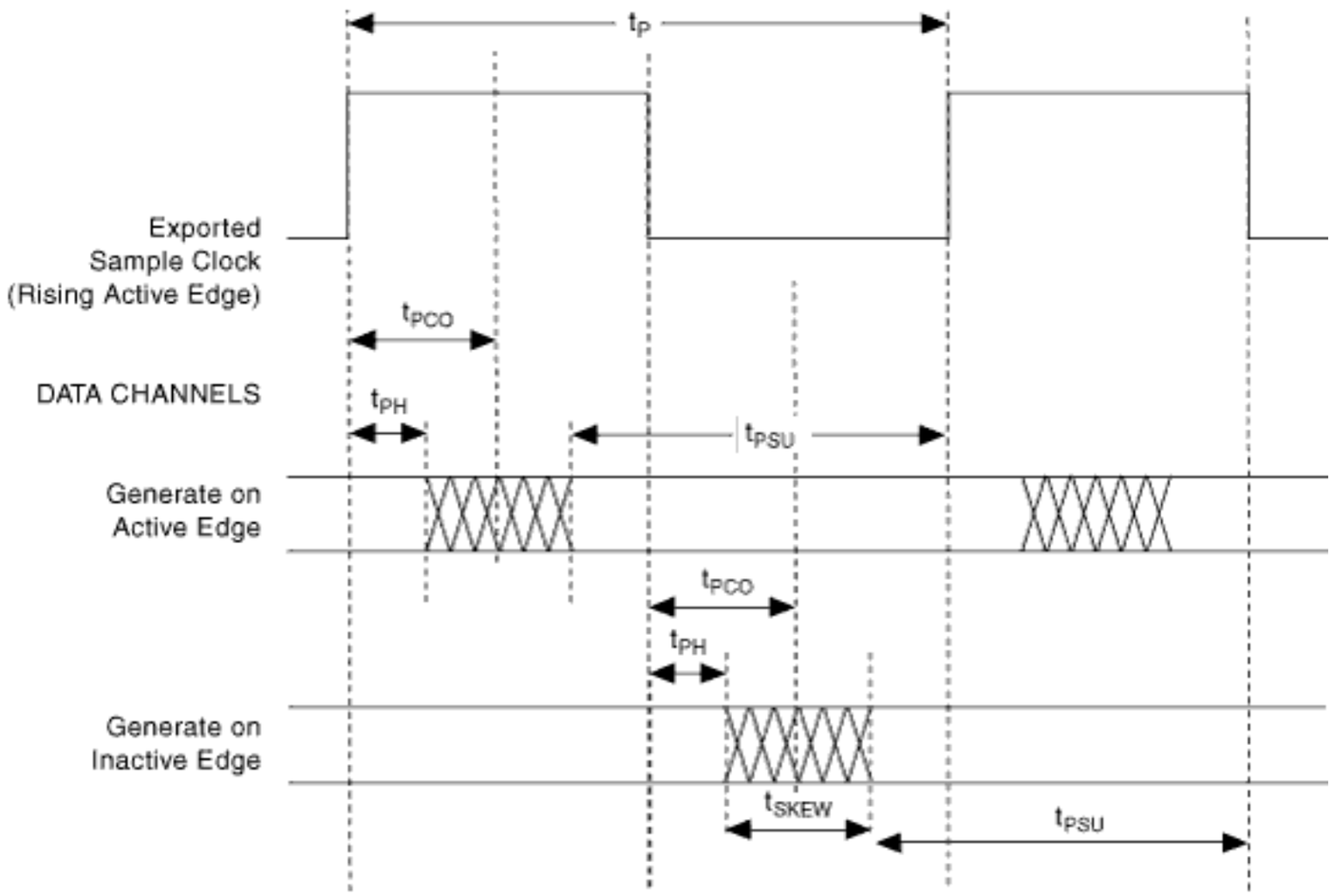
Exported Sample clock duty cycle	Internal Sample clock or divided-down timebase: 33% to 67% Imported Sample clock: Limited by input duty cycle	Typical.

Pattern Generation Timing (Data and PFI 5 Channels)

Specification	Value		Comments
Maximum data channel toggle rate	NI 6535: 5.0 MHz NI 6536: 12.5 MHz NI 6537: 25.0 MHz		—
Data position modes	**Data Channels**	**PFI Channels**	Relative to Sample clock; Active edge may be rising or falling.
	Active edge, Inactive edge	Active edge	
Exported Sample Clock Offset (t_{PCO})	3.1 ns		Typical.
Minimum provided hold time with respect to PFI 4 (t_{PH})	**PXI Express**	**PCI Express**	t_P is the Sample clock interval; values assume the sample is generated and acquired on the same clock edge; includes maximum channel-to- channel skew; valid for all data and events.
	750 ps	1.1 ns	
Minimum provided setup time with respect to PFI 4 (t_{PSU})	Sample clock interval (t_P) – 5.35 ns	Sample clock interval (t_P) – 5 ns	

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Provided Setup and Hold Times



$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{PH} = Minimum Provided Hold Time

t_{PSU} = Minimum Provided Setup Time

t_{PCO} = Time from Rising Clock Edge to Data Transition (Provided Clock to Out Time)

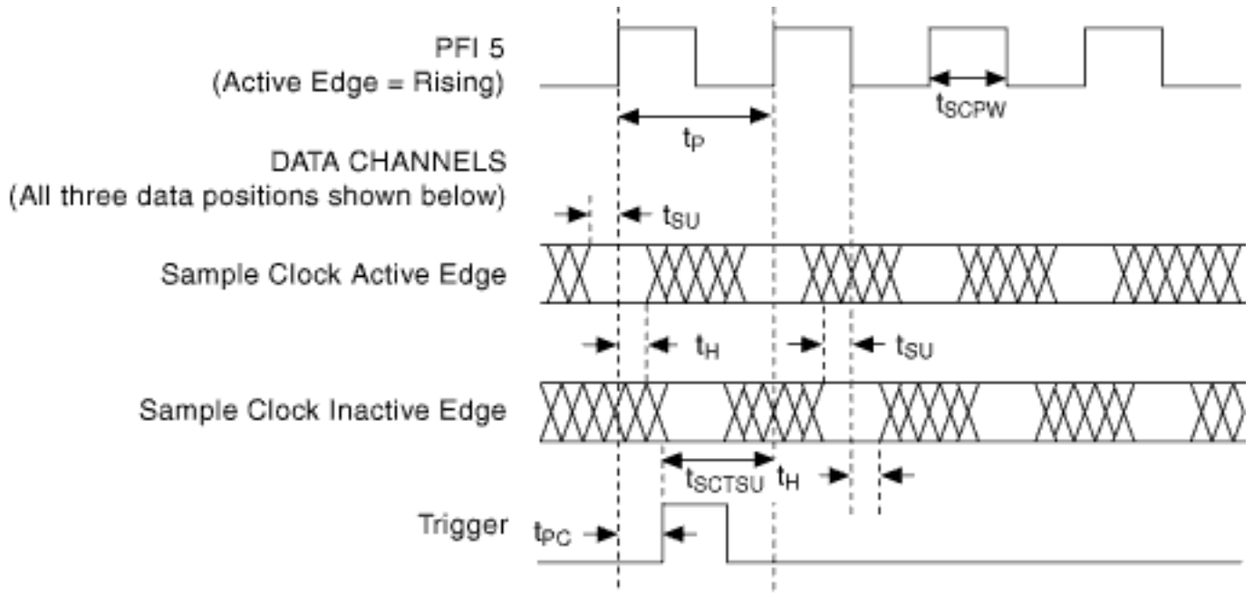
t_{SKEW} = Maximum Channel-to-Channel Skew and Clock Uncertainty

Pattern Acquisition Timing (Data and PFI 5 Channels)

Specification	Value		Comments
Setup time with respect to PFI 5 (t_{SU})	**PXI Express / PCI Express Rev C* or later**	**PCI Express Rev B***	Maximum required; includes maximum data channel-to- channel skew; valid for data and all triggers except the Start trigger when using the Sample Clock sample timing type. * Refer to assembly number sticker for revision information.
	2.8 ns	2.0 ns	
Hold time with respect to PFI 5 (t_H)	**PXI Express / PCI Express Rev C* or later**	**PCI Express Rev B***	
	1.5 ns	2.0 ns	
Setup time of triggers with respect to PFI 5 (t_{SCTSU})	15 ns		Maximum required; Sample Clock sample timing type only.
Trigger delay from PFI 5 to trigger edge (t_{PC})	2 ns		

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Acquisition Timing Diagram Using PFI 5 as the Sample Clock



t_{SU} = Setup Time with Respect to PFI 5

t_H = Hold Time with Respect to PFI 5

$t_P = \frac{1}{f}$ = Sample Clock Period

t_{SCPW} = Minimum Detectable Sample Clock Pulse Width

t_{PC} = Trigger Delay from PFI 5 to Trigger Edge*

t_{SCTSU} = Setup Time of Trigger with Respect to PFI 5*

*Sample Clock Sample Timing Type only.

Handshaking

Specification	Value	Comments
Asynchronous handshaking modes	Handshake (8255) sample timing type	8255 emulation equivalent.
Synchronous handshaking modes	1. Burst sample timing type 2. Pipelined Sample Clock sample timing type	—
Control line polarity	1. Active high 2. Active low	—
Programmable delay resolution for Handshake sample timing type	20 ns	—

Change Detection

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Specification	Value	Comments
Change detection resolution	Sample clock period	—
Sources	P0.<0..7>, P1.<0..7>, P2.<0..7>, P3.<0..7>	Per data channel selectable.
Valid sample position	1. Active edge 2. Inactive edge	Per data channel selectable.
Valid changes	1. Don’t care 2. Rising edge 3. Falling edge 4. Rising or falling edge	Per data channel selectable.

Waveform Specifications

Memory

Specification	Value	Comments
Onboard memory size	2,048 samples (S)	First-in first-out based.
Transfer type	1. DMA 2. Programmed I/O (On Demand sample timing type only)	—
Generation waveform quantum	Waveform size must be an integer multiple of 1 S.	—
Acquisition minimum buffer size	2 S	—

Triggers

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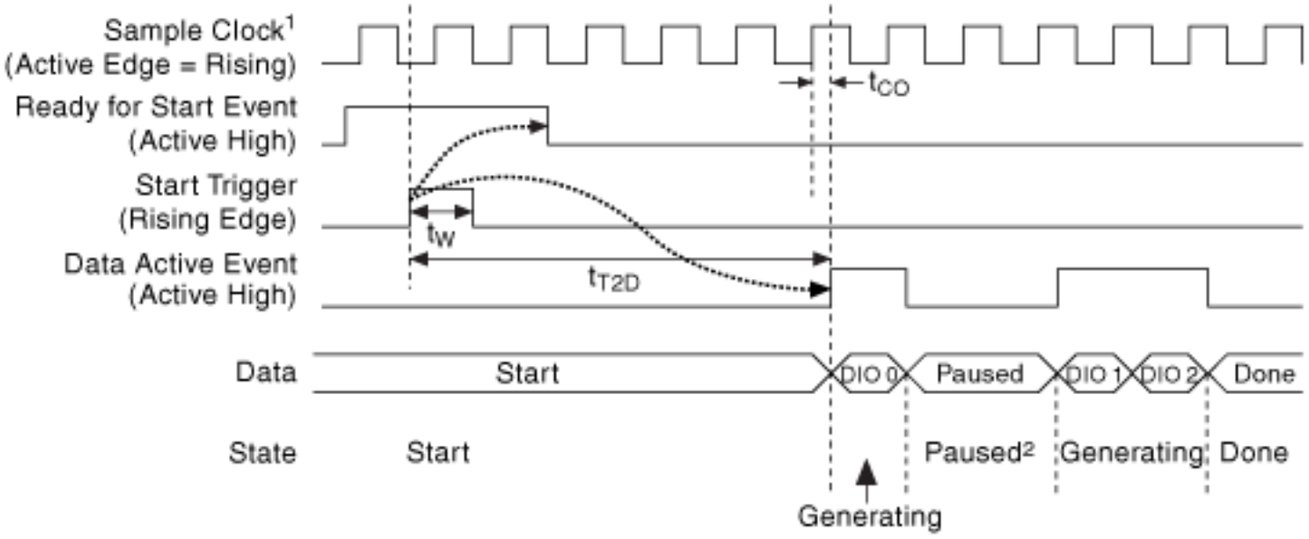
<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td rowspan="5">Supported triggers (by sample timing type)</td><td>Sample Timing Type</td><td>Acquisition</td><td>Generation</td><td rowspan="5">Generation operations do not support pattern match triggers.</td></tr>
<tr><td>Sample Clock</td><td>Start, Reference</td><td>Start</td></tr>
<tr><td>Pipelined Sample Clock</td><td>Pause, Start, Reference</td><td>Pause, Start</td></tr>
<tr><td>Burst Handshake</td><td>Pause (not including the pattern match type trigger)</td><td>Pause</td></tr>
<tr><td>Handshake</td><td>Handshake</td><td>Handshake</td></tr>
<tr><td>Change Detection</td><td>Start</td><td>N/A</td></tr>
<tr><td>Sources</td><td colspan="3">1. PFI <0..5> (DDC connector)
2. PXI_TRIG<0..6> (PXI backplane—PXI Express only) RTSI <0..7> (RTSI bus—PCI Express only)
3. PXIe_DSTARB (PXI backplane—PXI Express only)
4. Pattern match (Acquisition sessions only)
5. Disabled (Do not wait for a trigger)</td><td>—</td></tr>
<tr><td>Trigger detection</td><td colspan="3">1. Start Trigger (Edge detection: rising or falling; Pattern match: match or does not match)
2. Pause Trigger (Level detection: high or low; Pattern match: match or does not match)
3. Reference Trigger (Edge detection: rising or falling; Pattern match: match or does not match)
4. Handshaking Trigger (Interlocked: high or low)</td><td>—</td></tr>
<tr><td>Destinations</td><td colspan="3">1. PFI <0..5> (DDC Connector)
2. PXI_TRIG<0..7> (PXI backplane—PXI Express only) RTSI <0..7> (RTSI bus—PCI Express only)
3. PXIe_DSTARC (PXI backplane—PXI Express only)</td><td>—</td></tr>
<tr><td rowspan="3">Delay from Pause trigger to Paused state (t_{P2S})</td><td colspan="2">Generation</td><td>Acquisition</td><td rowspan="3">Use the Data Active event during generation operations to determine on a sample-by-sample basis when the NI device has entered the Paused state. Pause trigger only supported by Pipelined Sample Clock sample timing type.</td></tr>
<tr><td>Minimum</td><td>Maximum</td><td rowspan="2"></td></tr>
<tr><td>6 sample clock cycles + 6.7 ns</td><td>PCI Express: 7 sample clock cycles + 15.4 ns
PXI Express: 7 sample clock cycles + 17 ns</td><td>Synchronous to the data</td></tr>
<tr><td rowspan="3">Delay from trigger to digital data output (t_{T2D})</td><td colspan="2">Generation</td><td>Acquisition</td><td rowspan="3">Guaranteed by design.</td></tr>
<tr><td>Minimum</td><td>Maximum</td><td rowspan="2"></td></tr>
<tr><td>65 ns</td><td>1 sample clock cycle + 130 ns</td><td>N/A</td></tr>
<tr><td rowspan="2">Minimum detectable trigger pulse width (t_W)</td><td colspan="2">Sample Clock Sample Timing Type Triggers and Pipelined Sample Timing Type Generation Start Trigger</td><td>Burst and Pipelined Sample Timing Type Generation Pause Trigger</td><td rowspan="2">Maximum required pulse width to guarantee sampling by an asynchronous clock; synchronous triggers have same setup and hold requirements as data.</td></tr>
<tr><td colspan="2">10 ns</td><td>Sample clock period + 4 ns</td></tr>
<tr><td>Maximum required setup and hold of Sample Clock sample timing type triggers with respect to PFI 5</td><td colspan="3">Refer to the
Pattern Acquisition Timing (Data and PFI 5 Channels)
section of this document.</td><td>—</td></tr>
<tr><td>Maximum required delay from data to Handshake trigger (t_{DT})</td><td colspan="3">5 ns</td><td>Maximum required time between data valid and the Handshake trigger; Handshake sample timing type only.</td></tr>
</table>

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Maximum required delay from Handshake trigger to data (t_{TD})	50 ns	Maximum required time between the Handshake Trigger and data invalid; Handshake sample timing type only.

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Pipelined Generation Timing Diagram



[1] Must be free-running.

[2] Generation pauses if the DAQmx Underflow property/attribute is set to Pause Until Data Available or Pause Trigger Received.

t_W = Minimum detectable trigger pulse width.

t_{CO} = Exported Sample clock offset.

t_{T2D} = Delay from trigger to digital data out.

Pipelined Generation Handshaking Timing Diagram

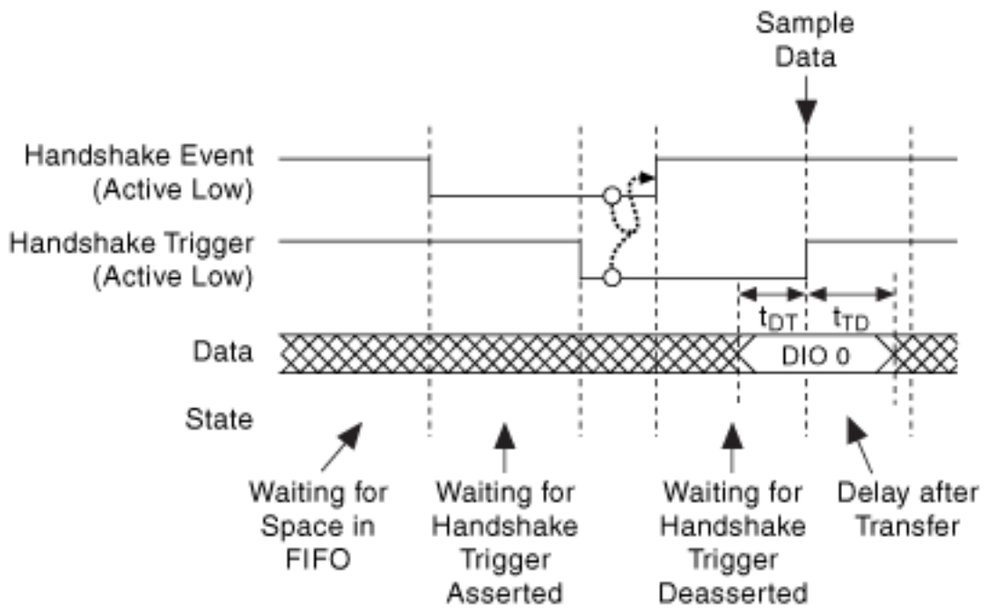
[1] Must be free-running.

t_{P2S} = Pause trigger to Paused state.

t_{CO} = Exported Sample clock offset.

Handshake (8255) Acquisition Timing Diagram

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t_{DT} = Maximum required delay from data valid to trigger.
t_{TD} = Maximum required delay from trigger to data invalid.

Events

Specification	Value		
Supported events (by sample timing type)	**Sample Timing Type**	**Acquisition**	**Generation**
	Sample Clock	Ready for Start	Ready for Start, Data Active
	Pipelined Sample Clock	Ready for Transfer, Ready for Start	Ready for Start, Data Active
	Burst Handshake	Ready for Transfer	Ready for Transfer
	Handshake	Handshake	Handshake
	Change Detection	Change Detection, Ready for Start	N/A
Destinations	1. PFI <0..5> (DDC Connector) 2. PXI_TRIG<0..7> (PXI backplane—PXI Express only) RTSI <0..7> (RTSI bus—PCI Express only) 3. PXIe_DSTARC (PXI backplane—PXI Express only)		
Pulse width for the exported Change Detection event	**Frequency ≤ 10 MHz**	**Frequency > 10 MHz***	
	50 ns	15 ns	
Delay from Change Detect to event	**Minimum**	**Maximum**	
	90 ns	**PCIe:** 1 Sample clock cycle + 100 ns **PXIe:** 1 Sample clock cycle + 105 ns	

Nonvolatile Storage

Specification	Value	Comments
Description	16 Mbit storage for firmware and power up states	—
Write Cycles	75,000 minimum	—

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Power

Specification	Value		Comments
	Typical	**Maximum**	All data channels loaded by 5 kΩ.
+3.3 VDC	700 mA	750 mA	
+12 VDC	250 mA	300 mA	
Total power	5.1 W	6.1 W	

Physical Specifications

Specification	Value		Comments
Dimensions	**PXI Express**	**PCI Express**	—
	21.4 cm × 2.0 cm × 13.1 cm (8.42 in. × 0.79 in.× 5.14 in.)	18.1 cm × 2.2 cm × 12.6 cm (7.13 in. × 0.85 in. × 4.93 in.)	
Weight	144.58 g (5.1 oz)	107.7 g (3.8 oz)	—

Software

Specification	Value		Comments
Driver software	**NI 6535**	**NI 6536/6537**	—
	NI-DAQmx driver software version 8.8 or later	NI-DAQmx driver software version 8.5 or later	
Application software	NI-DAQmx provides programming interfaces for the following application development environments: • National Instruments LabVIEW 7.1.1, 8.2.1, 8.5.1, and 8.6 (LabVIEW 8.6 requires NI-DAQmx 8.8 or later) • National Instruments LabWindows™/CVI™ 7.*x* or later • Microsoft Visual Studio 6.0 or later for ANSI C • Microsoft Visual Studio 2003 for C++		—
Test Panel	National Instruments Measurement and Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 6535/6536/6537. MAX is included on the NI-DAQmx instrument driver CD.		—

Environment

Note The NI 6535/6536/6537 is intended for indoor use only.

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Specification	Value		Comments
Operating temperature	**PXI Express**	**PCI Express**	—
	0 °C to +55 °C	0 °C to +45 °C	
Storage temperature	–20 °C to +70 °C		—
Operating relative humidity	10% to 90% relative humidity, noncondensing (Meets IEC 60068-2-56)		—
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC 60068-2-56)		—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL PRF-28800F.)		PXIe only
Storage shock	50 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL PRF-28800F.)		PXIe only
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC 60068-2-64.)		PXIe only
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets IEC 60068-2-64. Test profile exceeds requirements of MIL PRF-28800F, Class B.)		PXIe only
Altitude	0 m to 2,000 m above sea level (at 25 °C ambient temperature)		—
Pollution Degree	II		—

Safety, Electromagnetic Compatibility, and CE Compliance

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Specification	Value	Comments
Safety	This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 61010-1, CSA 61010-1	—
Note For UL and other safety certifications, refer to the product label or the Online Product Certification section.		
Electromagnetic Compatibility	This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use: • EN 61326 (IEC 61326): Class A emissions; Basic immunity • EN 55011 (CISPR 11): Group 1, Class A emissions • AS/NZS CISPR 11: Group 1, Class A emissions • FCC 47 CFR Part 15B: Class A emissions • ICES-001: Class A emissions Note For the standards applied to access the EMC of this product, refer to the Online Product Certification section. Note For EMC compliance, device *must* be operated with shielded cabling. In addition, filler panels must be installed.	With use of SHC68-C68- D2 or SHC68-C68- D4 shielded cable.
This product meets the essential requirements of applicable European Directives as follows:		
CE Compliance	• 2006/95/EC; Low-Voltage Directive (safety) • 2004/108/EC; Electromagnetic Compatibility Directive (EMC)	—
Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification , search by model number or product line, and click the appropriate link in the Certification column.		
Environmental Management	NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers. For additional environmental information, refer to the NI and the Environment web page at ni.com/environment . This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.	—
Waste Electrical and Electronic Equipment (WEEE)	**EU Customers:** At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee .	

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