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DAQ

Static DIO Register-Level Programmer Manual for NI 6509, 651*x*, 6520, 6521, and 6528 Devices

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About This Manual

This manual contains the following information you need to perform register-level programming for your NI 6509, 651*x*, 6520, 6521, and 6528 digital I/O (DIO) devices:

- Address and function of each NI 6509/651*x*/6520/6521/6528 device register for reading data, writing data, and implementing any standard function of the industrial DIO feature set (watchdog timer, digital filtering, change detection, and programmable power-up states) on the digital lines
- Examples that show the programming steps necessary to execute an operation

Use the change detection feature *only* if you are familiar with writing, installing, and uninstalling interrupt service routines. This manual does not cover writing, installing, and uninstalling interrupt service routines.

If you are programming using NI-DAQ driver software or application development software such as LabVIEW, Measurement Studio for Visual Studio .NET, or LabWindows™/CVI™, you do not need to read this manual.

Note While it is possible to program your DAQ device at the register level, National Instruments strongly recommends using NI-DAQ driver software and application development software such as LabVIEW, Measurement Studio for Visual Studio .NET, or LabWindows/CVI to program your NI 6509/651*x*/6520/6521/6528 device for improved productivity. NI-DAQ software provides easier programming with the same flexibility as register-level programming.

NI-DAQ driver software will not work for your programming needs in some cases, however. For example, if you are programming your DAQ device in an OS that is unsupported in NI-DAQ, NI-DAQmx Base software could be used as an alternative. If your OS is also unsupported in NI-DAQmx Base, you would then need to program your device using the *Static DIO Register-Level Programmer Manual for NI 6509, 651x, 6520, 6521, and 6528 Devices*.

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How To Use the Manual Set

The *Static DIO Register-Level Programmer Manual for NI 6509, 651x, 6520, 6521, and 6528 Devices* is one piece of the documentation set for your data acquisition system. You could have any of several types of manuals, depending on the hardware and software in your system. Use the manuals you have as follows:

- *Digital I/O Help*—This help file describes how to use the National Instruments 6509, 651*x*, 6520, 6521, and 6528 data acquisition (DAQ) devices with NI-DAQ 7.0 or later. This help file also contains specifications for each device. Programming options other than register-level programming are also described here.
- Accessory installation guides or manuals—If you are using accessory products, consult these guides when you are making your connections. The terminal block and cable assembly installation guides or accessory board user manuals explain how to physically connect the relevant pieces of your system.
- *DAQ Getting Started Guide*

Conventions

The following conventions are used in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIG+0.<3..0>.

♦ — The ♦ symbol indicates that the following text applies only to a specific product, a specific operating system, or a specific software version.

 — This icon denotes a tip, which alerts you to advisory information.

 — This icon denotes a note, which alerts you to important information.

 — This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

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italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Text in this font denotes sections of code, programming examples, and syntax examples. This font is also used for the proper names of programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

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1

Getting to Know Your NI 6509/651*x*/6520/6521/6528 Device

The NI 6509 is a 96-bit, high-drive digital input/output (DIO) device for PCI, PXI, and CompactPCI chassis. The NI 6509 features 96 TTL/CMOS-compatible digital I/O lines, 24 mA high-drive output, and the industrial DIO feature set. For more information on the industrial DIO feature set, refer to the *About This Manual* section.

The NI 651*x* devices are 30 V bank isolated data acquisition (DAQ) devices for PCI, PXI, or CompactPCI chassis. The NI 651*x* devices feature either 64 or 32 channels of various channel count input/output signaling for sourcing (NI 6510/6512/6514/6516/6518) or sinking (NI 6511/6513/6515/6517/6519) current. The NI 651*x* devices also provide the industrial DIO feature set. For more information on the industrial DIO feature set, refer to the *About This Manual* section. Refer to Table 1-1 for more information on port directions for the NI 651*x* devices.

The NI 6520/6521 devices contain five Form A single-pole single-throw (SPST) non-latching relay outputs, three Form C single-pole double-throw (SPDT) non-latching relay outputs, and eight channel-to-channel isolated industrial inputs. The NI 6520/6521 devices provide 16 channels of digital I/O (eight optically isolated digital input channels and eight non-latching relay output channels), and the industrial DIO feature set. For more information on the industrial DIO feature set, refer to the *About This Manual* section.

The NI 6528 device provides 24 isolated input channels, 24 isolated output channels, real-time system integration (RTSI) capabilities, and the industrial DIO feature set. For more information on the industrial DIO feature set, refer to the *About This Manual* section. The NI 6528 is ideal for 60 V isolation and switching in both industrial and laboratory environments.

For more information regarding the functions, installation, connections, and safe use of the NI 6509/651*x*/6520/6521/6528 devices, refer to the *Digital IO Help*.

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Caution Using your NI 6509/651*x*/6520/6521/6528 device in a way inconsistent with the directions in the *Digital IO Help* can lead to equipment damage or injury. National Instruments is *not* liable for damage or injuries resulting from incorrect use.

Using Your NI 6509/651*x*/6520/6521/6528

- PCI interface
- General operation registers

PCI Interface

The NI 6509/651*x*/6520/6521/6528 use the PCI MITE Application-Specific Integrated Circuit (ASIC) to communicate with the PCI or PXI bus. National Instruments designed this ASIC specifically for data acquisition. Before register-level programming the NI 6509/651*x*/6520/6521/6528 device, you must initialize the PCI interface as described in Chapter 3, *Programming*.

General Operation Registers

Initialize the PCI interface before using the general operation registers. Read the ID Register, one of the general operation registers, to verify the PCI interface is initialized properly. For more information on the ID Register, refer to the *ID Register* section in Chapter 2, *Register Map and Descriptions*.

The general operation registers include the IO Port Data registers and corresponding IO Select registers for reading and writing data. There are also registers for controlling digital filtering, change detection, the watchdog timer, RTSI output, and PXI synchronization. With the final set of registers, you can read and reset the status of your device.

The general operation registers are organized into two groups—recurring and non-recurring registers. Each port has a sequence of recurring registers for Data, IO Select, and other port-specific features. This same set of registers is repeated for each port but incremented 0x10 times the port number above the base address. The non-recurring registers affect the entire board and have set addresses.

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Table 1-1. NI 6509/651*x*/6520/6521/6528 Product Port Directions

Model	Port Direction											
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10 (xA)**	**11 (xB)**
PCI-6509	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
PXI-6509	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
PCI-6510	I	I	I	I	—	—	—	—	—	—	—	—
PCI-6511	I	I	I	I	I	I	I	I	—	—	—	—
PXI-6511	I	I	I	I	I	I	I	I	—	—	—	—
PCI-6512	O	O	O	O	O	O	O	O	—	—	—	—
PXI-6512	O	O	O	O	O	O	O	O	—	—	—	—
PCI-6513	O	O	O	O	O	O	O	O	—	—	—	—
PXI-6513	O	O	O	O	O	O	O	O	—	—	—	—
PCI-6514	I	I	I	I	O	O	O	O	—	—	—	—
PXI-6514	I	I	I	I	O	O	O	O	—	—	—	—
PCI-6515	I	I	I	I	O	O	O	O	—	—	—	—
PXI-6515	I	I	I	I	O	O	O	O	—	—	—	—
PCI-6516	O	O	O	O	—	—	—	—	—	—	—	—
PCI-6517	O	O	O	O	—	—	—	—	—	—	—	—
PCI-6518	I	I	O	O	—	—	—	—	—	—	—	—
PCI-6519	I	I	O	O	—	—	—	—	—	—	—	—
PCI-6520	I	O	—	—	—	—	—	—	—	—	—	—
PCI-6521	I	O	—	—	—	—	—	—	—	—	—	—
PXI-6521	I	O	—	—	—	—	—	—	—	—	—	—
PCI-6528	I	I	I	O	O	O	—	—	—	—	—	—
PXI-6528	I	I	I	O	O	O	—	—	—	—	—	—

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2

Register Map and Descriptions

Table 2-2 shows the register map for the NI 6509, 651*x*, 6520, 6521, and 6528 devices. The table gives the register name, the register address offset from the device base address (Base Address Register 1), the size of the register in bits, and the type of register (read-only, write-only, or read and write).

Registers are grouped in the table by function. A bit-by-bit description of each register follows the table.

The following sections show the register map for the NI 6509/651*x*/6520/6521/6528 devices with the registers sorted by function.

All NI 6509/651*x*/6520/6521/6528 devices have the same addresses for common registers.

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Table 2-1. NI 6509/651*x*/6520/6521/6528 Register Address Map—Recurring Port Registers

Register Name	Short Name	Offset (Hex)	Type	Size
IO Port Data	IOPort(*N*)Data	0x40 + 0x*N*0	Read-write	8-bit
IO Select	IOSelect(*N*)	0x41 + 0x*N*0	Read-write	8-bit
Rising Edge Sensitivity Configuration	RiseEdgeEnable(*N*)	0x42 + 0x*N*0	Read-write	8-bit
Falling Edge Sensitivity Configuration	FallEdgeEnable(*N*)	0x43 + 0x*N*0	Read-write	8-bit
Filter Enable	FilterEnable(*N*)	0x44 + 0x*N*0	Read-write	8-bit
Watchdog Timer High Impedance	WatchdogHighImp(*N*)	0x46 + 0x*N*0	Read-write	8-bit
Watchdog Timer Enable	WatchdogEnable(*N*)	0x47 + 0x*N*0	Read-write	8-bit
Watchdog Timer High or Low	WatchdogHighLow(*N*)	0x48 + 0x*N*0	Read-write	8-bit
RTSI Enable	RTSI_En(*N*)	0x49 + 0x*N*0	Read-write	8-bit

Note: *N* is the port number in hexidecimal. Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 times the port number in hex.

Examples:
1. Offset of Port 6 Data Register (IOPort6Data) = 0x40 + 0x60 = 0xA0
2. Offset of Port 11 Filter Enable Register (FilterEn11) = 0x44 + 0xB0 = 0xF4

Table 2-2. NI 6509/651*x*/6520/6521/6528 Register Address Map—Non-recurring Registers

Register Name	Offset (Hex)	Type	Size
ID Register	0x00	Read	8-bit
Clear Register	0x01	Write strobe	8-bit
Change Status Register	0x02	Read	8-bit
Master Interrupt Control Register	0x03	Read-write	8-bit
Revision Register	0x04	Read	32-bit
Filter Interval 32-bit Register	0x08	Read-write	32-bit
Automatic Clock Selection Register	0x14	Bit 0: Write Bit 1: Read	8-bit

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Table 2-3. NI 6509/651*x*/6520/6521/6528 Register Address Map—Watchdog Timer Registers

Register Name	Offset (Hex)	Type	Size
Watchdog Timer Software Timeout Enable	0x15	Read-write	8-bit
Watchdog Timer Expire Status	0x17	Read	8-bit
Watchdog Timer Timeout Interval	0x18	Read-write	32-bit

Table 2-4. NI 6509/651*x*/6520/6521/6528 Register Address Map—RTSI Configuration Registers

Register Name	Offset (Hex)	Type	Size
RTSI Input Route	0x0C	Read-write	16-bit
RTSI Pulse when Edge Detected	0x0E	Read-write	16-bit
RTSI Pulse when Watchdog Timer Expires	0x10	Read-write	16-bit
RTSI Trigger for Watchdog Timer	0x12	Read-write	16-bit
RTSI Edge Detection Configuration Register	0x16	Read-write	8-bit

The following pages provide a description of each register. The register bit map shows a diagram of the register with the most significant bit (MSB), bit 7, on the left and the least significant bit (LSB), bit 0, on the right. Each bit is represented by a rectangle with the bit name inside. The size of the register indicates how many bits you should read or write at a time. Reading a different size—for example, reading a 32-bit register with four 8-bit reads—may create invalid data.

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IO Port Data

IOPort(*N*)Data

This register is used to read digital data from or write data to port *N*, where *N* is the port number in hexidecimal.

Note Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 time the port number in hex.

Address Offsets: 0x40 + 0x(*N*)0

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D(7)	D(6)	D(5)	D(4)	D(3)	D(2)	D(1)	D(0)

Bit	Name	Description
7–0	D(<7..0>)	Read or write digital data at this address.

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IO Select Registers

IOSelect(*N*)

This register configures bidirectional port *N* as input or output, where *N* is the port number in hexidecimal.

Note Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 time the port number in hex.

Address Offset: 0x41 + 0x(*N*)0

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	I(1) / O(0)

Bit	Name	Description
7–1	Reserved	Write only zeros to these bits.
0	I(1) / O(0)	Write a 0 for input or a 1 for output.

Note It is not necessary to set this register if your device only supports fixed direction ports.

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Rising Edge Sensitivity Configuration Registers

RiseEdgeEnable(*N*)

This register enables monitoring of input lines of port *N* for rising edges, where *N* is the port number in hexidecimal.

Note Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 time the port number in hex.

Address Offset: 0x42 + 0x(*N*)0

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
REE(7)	REE(6)	REE(5)	REE(4)	REE(3)	REE(2)	REE(1)	REE(0)

Bit	Name	Description
7–0	REE(<7..0>)	Write a 1 to a bit to enable monitoring for the corresponding line.

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Falling Edge Sensitivity Configuration Registers

FallEdgeEnable(*N*)

This register enables monitoring of input lines of port *N* for falling edges, where *N* is the port number in hexidecimal.

Note Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 time the port number in hex.

Address Offset: 0x43 + 0x(*N*)0

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
FEE(7)	FEE(6)	FEE(5)	FEE(4)	FEE(3)	FEE(2)	FEE(1)	FEE(0)

Bit	Name	Description
7–0	FEE(<7..0>)	Write a 1 to a bit to enable monitoring for the corresponding line.

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Filter Enable Registers

FilterEnable(*N*)

This register enables filtering of input lines of port *N*, where *N* is the port number in hexidecimal. In FilterEnable(*N*) registers, all lines of all ports share the same interval.

Note Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 time the port number in hex.

Address Offset: 0x44 + 0x(*N*)0

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
FLE(7)	FLE(6)	FLE(5)	FLE(4)	FLE(3)	FLE(2)	FLE(1)	FLE(0)

Bit	Name	Description
7–0	FLE(<7..0>)	Write a 1 to a bit to enable filtering for the corresponding line.

For more information on digital filtering registers, refer to the *Filter Interval 32-Bit Register* section.

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Watchdog Timers High-Impedance Registers

WatchdogHighImp(*N*)

This register configures port *N* to go to high impedance when the watchdog timer (WDT) expires, where *N* is the port number in hexidecimal. WatchdogHighImp(*N*) is only valid for bidirectional ports.

Note Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 time the port number in hex.

Address Offset: 0x46 + 0x(*N*)0

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WDTHImp

Bit	Name	Description
7–1	Reserved	Write only zeros to this bit.
0	WDTHImp	Write a 1 to this register to make the port go to high impedance when the watchdog timer expires. Write a 0 to this register to make the port output high/low values on a per line basis. The watchdog timer must be enabled for either option to activate.

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Watchdog Timer Enable Registers

WatchdogEnable(*N*)

This register enables port *N* to go to configured expiration states when the watchdog timer (WDT) expires, where *N* is the port number in hexidecimal. WatchdogEnable(*N*) is only valid for fixed output or bidirectional ports.

Note Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 time the port number in hex.

Address Offset: 0x47 + 0x(*N*)0

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WDT_En

Bit	Name	Description
7–1	Reserved	Write only zeros to these bits.
0	WDT_En	Write a 1 to this register to allow the port to go into a user programmable safe state when the watchdog timer expires.

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Watchdog Timer High or Low Registers

WatchdogHighLow(*N*)

This register configures expiration states for port *N* to go to when the watchdog timer expires, where *N* is the port number in hexidecimal. WatchdogHighLow(*N*) is only valid for fixed output and bidirectional ports.

Note Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 time the port number in hex.

Address Offset: 0x48 + 0x(*N*)0

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
wdtHL(7)	wdtHL(6)	wdtHL(5)	wdtHL(4)	wdtHL(3)	wdtHL(2)	wdtHL(1)	wdtHL(0)

Bit	Name	Description
7–0	wdtHL(<7..0>)	WatchdogHighImp(*N*) must be 0 to enable this option. Write a 1 to output high on line i. Write a 0 to output low on line i.

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RTSI Enable Registers

RTSI_En(*N*)

This register enables RTSI for port *N*, where *N* is the port number in hexidecimal.

Note Ports can range from 0 to 11 (0x0 to 0xB), depending on your device. For each port, you must add an additional offset equal to 0x10 time the port number in hex.

Address Offset: 0x49 + 0x(*N*)0

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
RTSI_En(7)	RTSI_En(6)	RTSI_En(5)	RTSI_En(4)	RTSI_En(3)	RTSI_En(2)	RTSI_En(1)	RTSI_En(0)

Bit	Name	Description
7–0	RTSI_En(<7..0>)	Write a 1 to any bit to enable RTSI routing to the corresponding port bit. RTSI can only be enabled on two ports. The second port can only have one bit, the least significant bit (LSB) or bit 0, of the port enabled.

RTSI_En(*N*) is only available on the NI 6528.

- For PCI—Only valid for the first output-enabled port.
- For PXI—Only valid for the first output-enabled port and the first line of the second output-enabled port. The single line in the second port corresponds to the PXI Star Trigger line.

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Non-recurring Registers

ID Register

Contains identifying code for the board. Use this register to confirm that you are successfully reading from your device.

Address Offset: 0x00

Type: Read

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
ID(7)	ID(6)	ID(5)	ID(4)	ID(3)	ID(2)	ID(1)	ID(0)

Bit	Name	Description
7–0	ID(<7..0>)	Contains the ID of your device in hexidecimal. Usually corresponds to the last two digits of the model name of your device.

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Clear Register

Write to individual bit of this register to clear certain functionality in the board.

Address Offset: 0x01

Type: Write strobe

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	ClrWDT+	RstWDT	ClrWDTExp	ClrEdge	ClrOvrFlow	Reserved	Reserved

Bit	Name	Description
7	Reserved	Write only zeros to this bit.
6	ClearInterruptWDT	Set this bit to 1 to clear an interrupt caused by the expiration of the watchdog timer (WDT).
5	RstWDT	Set this bit to 1 periodically (less than the minimum watchdog timer expiration interval) to indicate that the application is running as expected.
4	ClrWDTExp	Set this bit to 1 to clear the effect of a watchdog timer expiration.
3	ClrEdge	Set this bit to 1 to clear the Edge Status bit in the Change Status Register and clear all edge detectors.
2	ClrOvrFlow	Clear Overflow—Set this bit to 1, along with the Clear Edge Detectors bit, to clear the overflow status bit in the Change Status Register.
1–0	Reserved	Write only zeros to these bits.

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Change Status Register

The Change Status Register gives the status of change detection.

Address Offset: 0x02

Type: Read

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	WDT Int status	Falling Edge Status	Rising Edge Status	MasterInterrupt Status	OverFlow	Edge Status

Bit	Name	Description
7–6	Reserved	Disregard these bits.
5	WDT Int Status	A 1 indicates that there has been a watchdog timer expiration that could cause an interrupt (if watchdog timer expiration interrupts are enabled).
4	Falling Edge Status	A 1 indicates that there has been a falling edge that could cause an interrupt (if falling edge interrupts are enabled).
3	Rising Edge Status	A 1 indicates that there has been a rising edge that could cause an interrupt (if rising edge interrupts are enabled).
2	MasterInterrupt Status	Indicates that the device is asserting an interrupt.
1	OverFlow	Indicates that at least one more edge has been detected since an interrupt is asserted.
0	Edge Status	Indicates an edge has been detected. If the EdgeInt bit is set in the Master Interrupt Control Register, Edge Status set indicates an interrupt is currently being asserted.

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Master Interrupt Control Register

The Master Interrupt Control Register enables change detection interrupts.

Address Offset: 0x03

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	WDT Expiration IntEnable	Falling Edge IntEnable	Rising Edge IntEnable	Master Interrupt Enable	OverFlow Enable	Edge Interrupt Enable

Bit	Name	Description
7–6	Reserved	Write only zeros to these bits.
5	WDT Exp IntEnable	Enable interrupt on watchdog timer expiration.
4	Falling Edge IntEnable	Enable interrupt on falling edge detection.
3	Rising Edge IntEnable	Enable interrupt on rising edge detection.
2	Master Interrupt Enable	This bit must be 1 for any interrupt to occur.
1	OverFlow Enable	Enable overflow interrupt.
0	Edge Interrupt Enable	Enable edge detection interrupt.

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Revision Register

This 32-bit register contains the revision of your device.

Address Offset: 0x04

Type: Read

Size: 32-bit

Bit Map:

31	30	29	28	27	26	25	24
Rev(31)	Rev(30)	Rev(29)	Rev(28)	Rev(27)	Rev(26)	Rev(25)	Rev(24)

23	22	21	20	19	18	17	16
Rev(23)	Rev(22)	Rev(21)	Rev(20)	Rev(19)	Rev(18)	Rev(17)	Rev(16)

15	14	13	12	11	10	9	8
Rev(15)	Rev(14)	Rev(13)	Rev(12)	Rev(11)	Rev(10)	Rev(9)	Rev(8)

7	6	5	4	3	2	1	0
Rev(7)	Rev(6)	Rev(5)	Rev(4)	Rev(3)	Rev(2)	Rev(1)	Rev(0)

Bit	Name	Description
31–0	Rev(<31..0>)	Contains the revision of your device.

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Filter Interval 32-Bit Register

The filter interval register controls the filter interval for distinguishing between valid input pulses and glitches. There are twenty bits in the filter interval register.

Address Offset: 0x08

Type: Read-write

Size: 32-bit

Bit Map:

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

23	22	21	20	19	18	17	16
Reserved	Reserved	Reserved	Reserved	FI(19)	FI(18)	FI(17)	FI(16)

15	14	13	12	11	10	9	8
FI(15)	FI(14)	FI(13)	FI(12)	FI(11)	FI(10)	FI(9)	FI(8)

7	6	5	4	3	2	1	0
FI(7)	FI(6)	FI(5)	FI(4)	FI(3)	FI(2)	FI(1)	FI(0)

Bit	Name	Description
31–20	Reserved	Write only zeros to these bits.
19–0	FI(<19..0>)	Filter interval, bits 19 and down to 0 in increments of 200 ns.

For more information on digital filtering registers, refer to the *Filter Enable Registers* section.

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Automatic Clock Selection Register (PXI-6528 Only)

This register enables/disables automatic clock selection (selecting between the PXI 10 MHz backplane clock and the 10 MHz onboard oscillator), and gives which clock is currently being used.

Address Offset: 0x14

Type: Bit 0: Write-only

Bit 1: Read-only

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SClkStat	AutoClkDis

Bit	Name	Description
7–2	Reserved	Write only zeros to these bits.
1	SystemClockStatus	Bit 1 indicates which clock is currently being used as the system clock (SClk). A 0 indicates the PXI 10 MHz backplane clock is being used. A 1 indicates the 10 MHz onboard oscillator is being used.
0	AutomaticClockDisable	Bit 0 has a default value of 0, which means automatic clock selection is enabled. Write a 1 to bit 0 to disable automatic clock selection and force use of the onboard oscillator.

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Watchdog Timer Software Timeout Enable

This register enables the device to go to specified expiration states when the watchdog timer expires.

Address Offset: 0x15

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WDTSwToEn

Bit	Name	Description
7–1	Reserved	Write only zeros to these bits.
0	WDTSwToEn	Set this bit to ensure the device goes to a specified expiration state when the watchdog timer expires.

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Watchdog Timer Expire Status

This register indicates whether or not the device is currently in the expiration state.

Address Offset: 0x17

Type: Read

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WDTExpStat

Bit	Name	Description
7–1	Reserved	Disregard these bits.
0	WDTExpStat	A 0 indicates the device is operating normally. A 1 indicates the device has gone to the expiration state.

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Watchdog Timer Timeout Interval

This register specifies the amount of time to wait before going to the expiration state. It is expressed in terms of 100 ns.

Address Offset: 0x18

Type: Read-write

Size: 32-bit

Bit Map:

31	30	29	28	27	26	25	24
WDT_TI(31)	WDT_TI(30)	WDT_TI(29)	WDT_TI(28)	WDT_TI(27)	WDT_TI(26)	WDT_TI(25)	WDT_TI(24)

23	22	21	20	19	18	17	16
WDT_TI(23)	WDT_TI(22)	WDT_TI(21)	WDT_TI(20)	WDT_TI(19)	WDT_TI(18)	WDT_TI(17)	WDT_TI(16)

15	14	13	12	11	10	9	8
WDT_TI(15)	WDT_TI(14)	WDT_TI(13)	WDT_TI(12)	WDT_TI(11)	WDT_TI(10)	WDT_TI(9)	WDT_TI(8)

7	6	5	4	3	2	1	0
WDT_TI(7)	WDT_TI(6)	WDT_TI(5)	WDT_TI(4)	WDT_TI(3)	WDT_TI(2)	WDT_TI(1)	WDT_TI(0)

Bit	Name	Description
31–0	WDT_TI(<31..0>)	Set these bits to specify the amount of time, in increments of 100 ns, the device waits before going to the expiration state.

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RTSI Configuration Registers

RTSI Input Route

This register configures which RTSI lines are driven by inputs from the RTSI-enabled input port.

Address Offset: 0x0C

Type: Read-write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RTSI IR(8)

7	6	5	4	3	2	1	0
RTSI IR(7)	RTSI IR(6)	RTSI IR(5)	RTSI IR(4)	RTSI IR(3)	RTSI IR(2)	RTSI IR(1)	RTSI IR(0)

Bit	Name	Description
15–9	Reserved	Write only zeros to these bits.
8–0	RTSI IR(<8..0>)	If a bit is 1 in this register, it should not be 1 in any other RTSI register. Write a 1 to a bit to make that RTSI line drive the value of the corresponding pin of the RTSI-enabled input port. RTSI IR(8) corresponds to the PXI Star Trigger line on PXI devices.

- For PCI—The RTSI-enabled port is the first input-enabled port.
- For PXI—The RTSI-enabled ports are the first two input-enabled ports.

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RTSI Pulse when Edge Detected

This register configures which RTSI lines to pulse for 200 ns when there is an edge detected on any of the lines configured for monitoring.

Address Offset: 0x0E

Type: Read-write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RTSI PED(8)

7	6	5	4	3	2	1	0
RTSI PED(7)	RTSI PED(6)	RTSI PED(5)	RTSI PED(4)	RTSI PED(3)	RTSI PED(2)	RTSI PED(1)	RTSI PED(0)

Bit	Name	Description
15–9	Reserved	Write only zeros to these bits.
8–0	RTSI PED(<8..0>)	If a bit is 1 in this register, it should not be 1 in any other RTSI register. Write a 1 to a bit to make that RTSI line drive the value of the corresponding pin of the RTSI-enabled input port. RTSI PED(8) corresponds to the PXI Star Trigger line on PXI devices.

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RTSI Pulse when Watchdog Timer Expires

This register configures which RTSI lines to pulse for 200 ns when the watchdog timer expires.

Address Offset: 0x10

Type: Read-write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RTSI PWE(8)

7	6	5	4	3	2	1	0
RTSI PWE(7)	RTSI PWE(6)	RTSI PWE(5)	RTSI PWE(4)	RTSI PWE(3)	RTSI PWE(2)	RTSI PWE(1)	RTSI PWE(0)

Bit	Name	Description
15–9	Reserved	Write only zeros to these bits.
8–0	RTSI PWE(<8..0>)	If a bit is 1 in this register, it should not be 1 in any other RTSI register. Write a 1 to a bit to make that RTSI line pulse for 200 ns when the watchdog timer expires. RTSI PWE(8) corresponds to the PXI Star Trigger line on PXI devices.

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RTSI Trigger for Watchdog Timer

Enables RTSI line to act as a hardware trigger for the watchdog timer.

Address Offset: 0x12

Type: Read-write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RTSI Trig(8)

7	6	5	4	3	2	1	0
RTSI Trig(7)	RTSI Trig(6)	RTSI Trig(5)	RTSI Trig(4)	RTSI Trig(3)	RTSI Trig(2)	RTSI Trig(1)	RTSI Trig(0)

Bit	Name	Description
15–9	Reserved	Write only zeros to these bits.
8–0	RTSI Trig(<8..0>)	RTSI enable does not have to be 1 for the port to allow the watchdog timer to expire. Write a 1 to this register to allow the watchdog timer to expire on a rising/falling RTSI line. RTSI Trig(8) corresponds to the PXI Star Trigger line on PXI devices.

For more information on RTSI industrial DIO feature registers, refer to the *RTSI Edge Detection Configuration Register* section.

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RTSI Edge Detection Configuration Register

The RTSI Edge Detection Configuration register sets RTSI edge detection to synchronous or asynchronous mode and selects sensitivity to rising edges, falling edges, or both.

When using synchronous edge detection, the RTSI signals are sampled every 100 ns. Therefore, for an edge to be detected, the RTSI line must remain in its new value for at least 100 ns.

When using the asynchronous edge detectors, pulses as short as 10 ns can trigger the edge detection, in compliance with PXI specifications. At power up, asynchronous edge detection is selected by default.

Address Offset: 0x16

Type: Read-write

Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	RESens	FESens	SyncED

Bit	Name	Description
7–3	Reserved	Write only zeros to these bits.
2	Rising Edge Sensitivity	Write a 1 to enable monitoring of rising edges on RTSI.
1	Falling Edge Sensitivity	Write a 1 to enable monitoring of falling edges on RTSI.
0	Synchronous Edge Detect	Write a 1 to this bit to use synchronous RTSI edge detection.

For more information on RTSI industrial DIO feature registers, refer to the *RTSI Trigger for Watchdog Timer* section.

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3

Programming

This chapter contains basic programming information for your NI 6509/651*x*/6520/6521/6528 devices. Programming your NI 6509/651*x*/6520/6521/6528 device involves writing to and reading from registers on the device. Registers are listed in Chapter 2, *Register Map and Descriptions*.

Programming Examples

Most of the register-level functionality is explained through a separate set of examples in the NI Measurement Hardware Driver Development Kit (DDK). These examples show how to program the device register and isolate you from register addressing and MITE initialization. The NI Measurement Hardware DDK works on a variety of operating systems, including Linux and Mac OS X. It also includes an OS generic bus interface you can use to support additional operating systems. To download the NI Measurement Hardware DDK and NI 6509/651*x*/6520/6521/6528 examples, go to `ni.com/info` and enter `mhddk`.

Using Interrupts and Other Advanced Functionality

The NI Measurement Hardware DDK does not directly support interrupts. As a result, it does not provide programming examples for change detection, the watchdog timer, and other advanced functionality. If you wish to program these features at the register level, you must install your own interrupt service routines. Refer to the register descriptions in Chapter 2, *Register Map and Descriptions*, for information on the relevant registers for these features.

Programming Your Device without the NI Measurement Hardware DDK

If you chose not to use the NI Measurement Hardware DDK, you will need to detect your device and initialize the PCI bus and MITE interface.

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Initializing the PCI Bus

The PCI Bus is a high performance, 32-bit bus with multiplexed address and data lines. This system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers.

The PCI Bus moves data for the NI 6509/651*x*/6520/6521/6528 devices. Configure the bus-related resources before you execute a register-level program. To do this, you need to assign a base address and optionally assign an interrupt channel to your NI 6509/651*x*/6520/6521/6528 device as shown here and in the following section.

For proper operation, configure the PCI MITE ASIC as described in this section. The references made to PCI BIOS[1] calls are left for you to implement.

First, write an algorithm that finds and stores configuration information about the device. You can do this by using PCI BIOS calls to search PCI configuration space for the National Instruments vendor ID (0x1093) and one of the device IDs listed in Table 3-1.

Table 3-1. Static DIO Devices and IDs

Device	ID	Description
PCI-6509	0x7085	96 Channel, 5 V, TTL/CMOS Digital I/O
PCI-6510	0x7124	32 Input, 30 V, Bank-Isolated Digital Input
PCI-6511	0x70C3	64 Input, 30 V, Bank-Isolated Digital Input
PCI-6512	0x70CC	64 Source Output, 30 V, Bank-Isolated Digital Output
PCI-6513	0x70C8	64 Sink Output, 30 V, Bank-Isolated Digital Output
PCI-6514	0x7088	32 Input, 32 Source Output, 30 V, Bank-Isolated Digital I/O
PCI-6515	0x7087	32 Input, 32 Sink Output, 30 V, Bank-Isolated Digital I/O
PCI-6516	0x7125	32 Source Output, 30 V, Bank-Isolated Digital Output
PCI-6517	0x7126	32 Sink Output, 30 V, Bank-Isolated Digital Output
PCI-6518	0x7127	16 Input, 16 Source Output, 30 V, Bank-Isolated Digital I/O
PCI-6519	0x7128	16 Input, 16 Sink Output, 30 V, Bank-Isolated Digital I/O
PCI-6520	0x71C5	8 Input, 8 Source Output, 60 V, Ch-Ch Isolated Digital I/O
PCI-6521	0x718B	8 Input, 8 Sink Output, 60 V, Ch-Ch Isolated Digital I/O

[1] You can obtain more information on PCI BIOS calls from the PCI SIG online at `www.pcisig.com`.

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Table 3-1. Static DIO Devices and IDs (Continued)

Device	ID	Description
PCI-6528	0x70A9	24 Input, 24 Output, 60 V, Ch-Ch Isolated Digital I/O
PXI-6509	0x1710	96 Channel, 5 V, TTL/CMOS Digital I/O
PXI-6511	0x70D3	64 Sink/Source Input, 30 V, Bank-Isolated Digital Input
PXI-6512	0x70D2	64 Source Output, 30 V, Bank-Isolated Digital Output
PXI-6513	0x70D1	64 Sink Output, 30 V, Bank-Isolated Digital Output
PXI-6514	0x70CD	32 Source/Sink Input, 32 Source Output, 30 V, Bank-Isolated Digital I/O
PXI-6515	0x70C9	32 Input, 32 Sink Output, 30 V, Bank-Isolated Digital I/O
PXI-6521	0x718C	8 Output, 8 Input, 60 V, Ch-Ch Isolated Digital I/O
PXI-6528	0x7086	24 Input, 24 Output, 60 V, Ch-Ch Isolated Digital I/O

If a device is found, the algorithm can store the configuration information of the device into a data structure. Base Address Register 0 (BAR0) points to the base address of the PCI MITE, while Base Address Register 1 (BAR1) points to the base address of the device registers. The size of BAR0 is 4 KB, and the size of BAR1 is 8 KB.

Both addresses are most likely mapped above 1 MB in the memory map. This means that in order to communicate with the device you must know how to perform memory cycles to extended memory.

Tip To make communication with the device simpler, re-map the device below 1 MB in the memory map using PCI BIOS read and write calls.

Example

This pseudocode example re-maps the device below 1 MB. If you choose not to re-map the device, you can skip the first CWrite instruction, but you still need to perform the next and last instructions to initialize the device. All values in this example are 32 bits.

Use the following pseudocode to re-map the PCI MITE to memory address 0xD0000 and the device to memory address 0xD1000:

```
CWrite(0x10,0x000D0000)      //Write the address to which you want to re-map the
                             PCI MITE to PCI configuration space offset 0x10
                             (BAR0).

Write(0xD0340,0x0000AEAE)    //Write the value 0x0000AEAE to offset 0x340 from the
                             new PCI MITE address.
```


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CWrite(0x14,0x000D1000)	//Write the address to which you want to re-map the device (other than the PCI MITE) to PCI configuration space offset 0x14 (BAR1).
	//Create the window data value by masking the new device address:window data value = ((0xFFFFFF00 AND new device address) OR (0x00000080)).
	//If you are not re-mapping the device, then the new device address is the value in BAR1.
Write(0xD00C0,0x000D1080)	//Write the window data value to offset 0xC0 from the new PCI MITE address. If you are not re-mapping the device, then the new PCI MITE address is the value in BAR0.

The base address is now 0xD1000. Make sure the re-mapped PCI MITE and the NI 6509/651*x*/6520/6521/6528 memory ranges are not used by another device or system resource. You can exclude this memory from use with a memory manager.

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A

Technical Support Resources

Visit the following sections of the National Instruments Web site at `ni.com` for technical support and professional services:

- **Support**—Online technical support resources at `ni.com/support` include the following:
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Glossary

Symbol	Prefix	Value
n	nano	10^{-9}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}

Symbols

+	Positive of, or plus
–	Negative of, or minus

A

ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions for a specific application

C

CompactPCI	refers to the core specification defined by the PCI Industrial Computer Manufacturer's Group (PICMG)

D

DAQ	data acquisition—a system that uses the personal computer to collect, measure, and generate electrical signals
DIO	digital input/output

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I

isolation	signal conditioning to break ground loops and reject high common-mode voltages to protect equipment and users and to ensure accurate measurements

L

LSB	least significant bit

M

MSB	most significant bit

O

optical isolation	the technique of using an optocoupler to transfer data without electrical continuity, to eliminate high-potential differences and transients
optocoupler	a device that transfers electrical signals by utilizing light waves to provide coupling with electrical isolation between input and output

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA
port	a digital port, consisting of eight lines of digital input and/or output
PXI	PCI eXtensions for Instrumentation—an open specification that builds on the CompactPCI specification by adding instrumentation-specific features

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