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PXI

PXI™-8320 User Manual

December 1997 Edition
Part Number 321717A-01

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

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About This Manual

The *PXI-8320 User Manual* describes the functional, physical, and electrical aspects of the PXI-8320 and contains information concerning its operation and programming.

Organization of This Manual

The *PXI-8320 User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the PXI-8320, lists the contents of your PXI-8320 kit, lists optional equipment and software, and introduces the concepts of MXI-2.
- Chapter 2, *Functional Overview*, contains functional descriptions of each major logic block on the PXI-8320.
- Chapter 3, *PXI-8320 Configuration and Installation*, contains the instructions to configure and install the PXI-8320 module.
- Appendix A, *Specifications*, lists various module specifications of the PXI-8320, such as physical dimensions and power requirements.
- Appendix B, *MXI-2 Connector*, describes the MXI-2 connector on the PXI-8320 module.
- Appendix C, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products and manuals.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, and symbols.
- The *Index* contains an alphabetical list of key terms and topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual:



This icon to the left of bold italicized text denotes a note, which alerts you to important information.



This icon to the left of bold italicized text denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

	This icon to the left of bold italicized text denotes a warning, which advises you of precautions to take to avoid being electrically shocked.
bold italic	Bold italic text denotes a note, caution, or warning.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
`monospace`	Text in this font denotes text or characters that you should literally enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and for statements and comments taken from programs.

Related Documentation

The following documents contain information that you may find helpful as you read this manual:

- ANSI/IEEE Standard 1014-1987, *IEEE Standard for a Versatile Backplane Bus: VMEbus*
- ANSI/IEEE Standard 1155-1993, *IEEE VMEbus Extensions for Instrumentation: VXIbus*
- ANSI/VITA 1-1994, *VME64*
- *Multisystem Extension Interface Bus Specification*, Version 2.0 (available from National Instruments Corporation)
- VXI-6, *VXIbus Mainframe Extender Specification*, Rev. 1.0, VXIbus Consortium

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix C, *Customer Communication*, at the end of this manual.

1

Introduction

This chapter describes the PXI-8320, lists the contents of your PXI-8320 kit, lists optional equipment and software, and introduces the concepts of MXI-2.

PXI-8320 Overview

The PXI-8320 is a 32-bit 3U style CompactPCI compatible plug-in circuit board that plugs into one of the peripheral slots of your PXI or CompactPCI chassis. It links your PXI/CompactPCI-based computer directly to the MXIbus and vice versa. Because the PXI-8320 uses the same communication register set that other VXIbus message-based devices use, other MXIbus devices view the PXI-8320 as a VXIbus device. The PXI-8320 can also function as the MXIbus System Controller and can terminate the MXIbus signals directly on the PXI-8320. In addition, you can install up to 16 MB of onboard DRAM on the PXI-8320 that the board can either share with the MXIbus and VXI/VMEbus or use as a dedicated data buffer.

The PXI-8320 achieves high-performance block transfer rates by integrating the MITE custom ASIC, a sophisticated dual-channel DMA controller with standard interfaces for VXI, VME, MXI, and PCI. By using MITE DMA to transfer data and commands to and from devices, the MITE frees up a computer's microprocessor to perform other tasks such as data analysis and presentation. In addition to DMA, the MITE incorporates both the new Synchronous MXI protocol and VME64 MBLT (8-byte block transfers in which both the address bus and data bus are used to transfer data) directly into the ASIC to perform the fastest transfer operation to instruments.

The PXI-8320 has the following features:

- Interfaces the PXI/CompactPCI bus to the MXIbus (32-bit Multisystem eXtension Interface bus)
- Supports D64, block, and synchronous MXI cycles for high-performance data transfer

- Directly controls MXIbus interrupt levels, utility signals, TTL triggers, and CLK10
- Allows for optional or user-installable onboard DRAM up to 16 MB, which can be shared with the MXIbus
- Conforms to CompactPCI Specification Revision 2.0/PXI Specification
- Conforms to *Multisystem Extension Interface Bus Specification*, Version 2.0
- Supports MXIbus termination

MXI-2 Description

MXI-2 is the second generation of the National Instruments MXIbus product line. The MXIbus is a general-purpose, 32-bit, multimaster system bus on a cable. MXI-2 expands the number of signals on a standard MXI cable by including VXI triggers, all VXI interrupts, CLK10, and all of the utility bus signals (SYSFAIL*, SYSRESET*, and ACFAIL*).

Because MXI-2 incorporates all of these new signals into a single connector, you can extend the triggers, interrupts, and utility signals not only to other mainframes but also to the local CPU in all MXI-2 products using a single cable. Thus, with the MXI-2, CPU interface boards such as the PXI-8320 perform as though they were plugged directly into the VXI/VME backplane.

In addition, MXI-2 surpasses the data throughput of previous-generation MXIbus products by defining new high-performance protocols. MXI-2 is a superset of MXI. All accesses initiated by MXIbus devices work with MXI-2 devices. However, MXI-2 defines synchronous MXI block data transfers that surpass previous block data throughput benchmarks. The new synchronous MXI block protocol increases MXI-2 throughput to a maximum of 33 MB/s between two MXI-2 devices. All National Instruments MXI-2 boards can initiate and respond to synchronous MXI block cycles.

☞ **Note** ***In the remainder of this manual, the term* MXIbus *refers to* MXI-2.**

What You Need to Get Started

- ❑ PXI or CompactPCI chassis
- ❑ PXI-8320 interface board
- ❑ MXI-2 cable

Optional Equipment

- Type M1 MXI-2 Cables
  Straight-point connector to straight-point connector:
  - 1, 2, 4, 8, or 20 m
- Type M2 MXI-2 Cables
  Straight-point connector to right-angle daisy-chain connector:
  - 1, 2, 4, 8, or 20 m
- Type M3 MXI-2 Cables
  Right-angle point connector to right-angle daisy-chain connector:
  - 1, 2, 4, 8, or 20 m
- Type M4 MXI-2 Cables
  Straight-point connector to reverse right-angle daisy-chain connector:
  - 1, 2, 4, 8, or 20 m
- Type MB-1 MXI-2 Cables
  Standard right-angle point connector to wall-mount bulkhead exit connector:
  - 1, 2, 4, or 8 m
- Type MB-2 MXI-2 Cables
  Straight bulkhead exit connector to straight bulkhead entry connector:
  - 1, 2, 4, or 8 m
- Type MB-3 MXI-2 Cables
  Wall-mount bulkhead entry connector to straight right-angle daisy-chain connector:
  - 1, 2, 4, or 8 m
- Type MB-4 MXI-2 Cables
  Standard right-angle point connector to straight bulkhead entry connector:
  - 1, 2, 4, or 8 m

- Type MB-5 MXI-2 Cables
  Standard right-angle daisy-chain connector to straight bulkhead exit connector:
  - 1, 2, 4, or 8 m
- Type MB-6 MXI-2 Cables
  Reverse right-angle daisy-chain connector to wall-mount bulkhead exit connector:
  - 1, 2, 4, or 8 m
- Onboard DRAM
  - 4 or 16 MB

Optional Software

You can order the National Instruments NI-VXI bus interface software for the PXI-8320. The NI-VXI software includes a Resource Manager, graphical and text-based versions of an interactive VXI resource editor program, a comprehensive library of software routines for VXI/VME programming, and graphical and text-based versions of an interactive control program for VXI/VME. You can use this software to seamlessly program multiple-mainframe configurations and have software compatibility across a variety of VXI/VME controller platforms.

In addition to NI-VXI, you can order the National Instruments LabVIEW and LabWindows/CVI application programs and instrument drivers to ease your programming task. These standardized programs match the modular virtual instrument capability of VXI and can reduce your VXI/VMEbus software development time. These programs are fully VXI*plug&play* compliant and feature extensive libraries of VXI instrument drivers written to take full advantage of direct VXI control.

LabVIEW is a complete programming environment that departs from the sequential nature of traditional programming languages and features a graphical programming environment.

LabWindows/CVI is an interactive C development environment for building test and measurement and instrument control systems. It includes interactive code-generation tools and a graphical editor for building custom user interfaces.

LabVIEW and LabWindows/CVI include all the tools needed for instrument control, data acquisition, analysis, and presentation. When you order the LabVIEW VXI Development System for Windows or the

LabWindows/CVI VXI Development System for Windows, you also get more than 500 complete instrument drivers, which are modular, source-code programs that handle the communication with your instrument to speed your application development.

2

Functional Overview

This chapter contains functional descriptions of each major logic block on the PXI-8320.

PXI-8320 Functional Description

In the simplest terms, you can think of the PXI-8320 as a bus translator that converts PCI bus signals into appropriate MXIbus signals. From the perspective of the MXIbus, the PXI-8320 implements a MXIbus interface to communicate with other MXIbus devices. From the perspective of the PCI bus, the PXI-8320 is an interface to the outside world.

Figure 2-1 is a functional block diagram of the PXI-8320. Following the diagram is a description of each logic block shown.

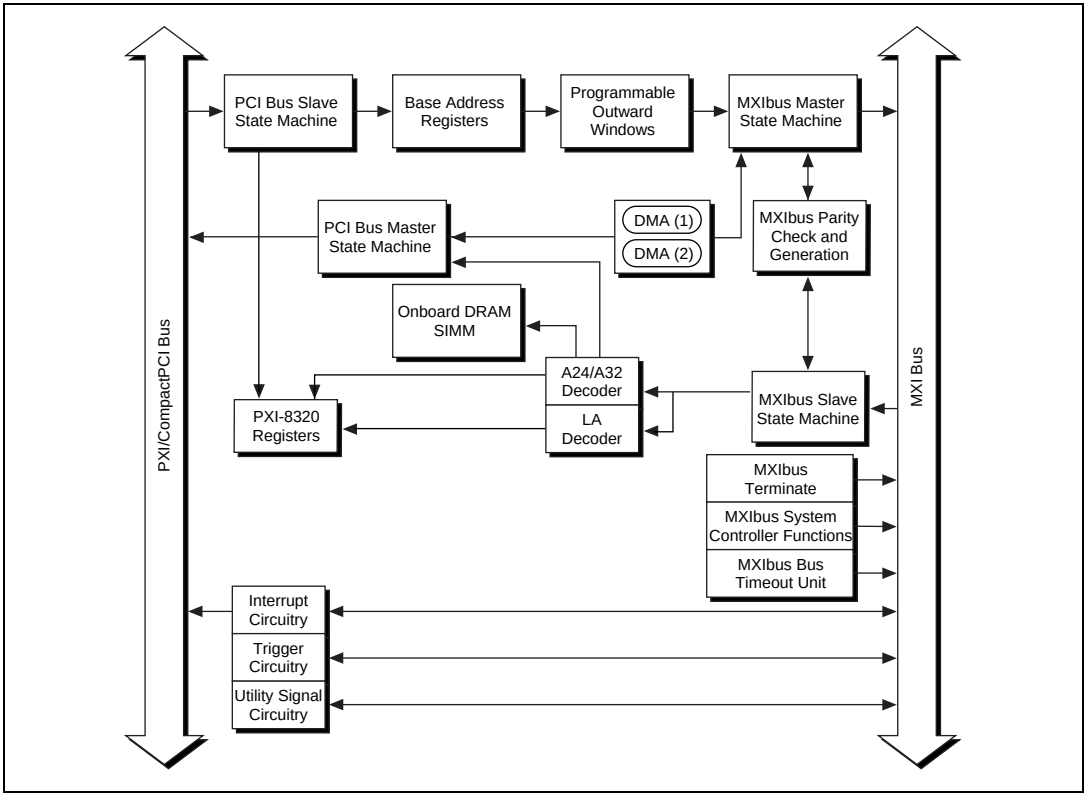


Figure 2-1. PXI-8320 Block Diagram

- **PCI Bus Slave State Machine**

  This state machine monitors the output of the window decoders and responds to PCI bus cycles intended for the PXI-8320. The cycles may map to the PXI-8320 registers, the onboard DRAM, or the MXIbus. The PXI-8320 is a medium-speed PCI decoder that accepts both configuration and memory cycles. The interface logic ensures that the PXI-8320 meets the loading, driving, and timing requirements of the PCI specification.

- **Base Address Registers**

  The PXI-8320 uses PCI registers BAR0 to BAR3 to decode PCI memory space. The final destination of PCI cycles that match the base address registers is determined by the programmable outward windows.

- **Programmable Outward Windows** — The PXI-8320 has multiple programmable outward windows. These windows direct the PCI slave state machine to route incoming cycles to local registers, onboard DRAM, or the MXIbus.

- **MXIbus Master State Machine** — This state machine generates MXIbus master data transfer cycles when directed to do so by the PCI bus slave state machine, thus allowing PCI bus cycles to map to the MXIbus. The PXI-8320 can generate D64, D32, D16, and D08(EO) single, block, and RMW cycles on MXIbus in A32 and A24 space (performing the D64 transfers by doing successive D32 transfers). The PXI-8320 can also generate data transfers in A16 space, with the exception of D64 and block transfers. The MXIbus master state machine also checks MXIbus parity on read data received and stores an error status when a parity error is detected. The transceivers ensure that the PXI-8320 meets the loading, driving, and timing requirements of the MXIbus specification for the AD[31–0], AM[4–0], and CONVERT* signals.

- **PCI Bus Master State Machine** — This state machine generates PCI bus master data transfer cycles when directed to do so by the MXIbus slave state machine or one of the DMA controllers on the PXI-8320. The PXI-8320 can generate 8-, 16-, and 32-bit memory read and write cycles (both single and multiple). The PXI-8320 does not generate unaligned PCI bus data transfers. The interface logic ensures that the PXI-8320 meets the loading, driving, and timing requirements of the PCI specification.

- **DMA Controllers** — The PXI-8320 has two independent onboard DMA controllers. The DMA controllers can transfer data at maximum speeds between any combination of the PCI bus, onboard DRAM, or MXIbus.

- **MXIbus Parity Check and Generation** — The MXIbus parity check/generation circuitry checks for even parity anytime the PXI-8320 is receiving the AD[31–0] signals. If parity is not even, the circuitry signals the appropriate MXIbus state machine. The MXIbus master state machine is signaled for a parity error during the data phase of a MXIbus master read cycle, while the MXIbus slave state machine is signaled for a parity error during the address phase of any MXIbus slave cycle and the data phase of a MXIbus slave write cycle. Even parity is also generated and sent to the MXIbus with master address and write data as well as slave read data.
- **Onboard DRAM SODIMM** — This logic block represents the DRAM SODIMM socket on the PXI-8320. If DRAM is installed, it is accessible in the PXI-8320 A24/A32 memory space.
- **PXI-8320 Registers** — This logic block represents all registers on the PXI-8320. Both the PCI bus and MXIbus can access the registers. All registers are available from the PCI bus, while a subset is accessible in the PXI-8320 MXIbus A16 configuration area.
- **A24/A32 Decoder** — This address decoder monitors the MXIbus for access to the PXI-8320 A24/A32 memory space. All resources located on the PXI-8320 are accessible in this region. The decoded region can be routed to the PCI bus or onboard DRAM SODIMM.
- **Logical Address Decoder** — This address decoder monitors the MXIbus for A16 accesses to the PXI-8320 MXIbus configuration space registers based on the VXIbus logical address of the PXI-8320. A subset of the PXI-8320 registers is accessible in this region.

- **MXIbus Slave State Machine**

  This state machine monitors the output of the address decoders and responds to MXIbus cycles intended for the PXI-8320. Cycles that map to the Logical Address decoder access the PXI-8320 registers, while cycles that map to the A24/A32 decoder access either the PXI-8320 registers or the onboard DRAM SODIMM. The PXI-8320 can accept D32, D16, and D08(EO) single and RMW MXIbus cycles in A32, A24, and A16 space. The PXI-8320 can also accept synchronous and block MXIbus cycles in A32 and A24 space. The MXIbus slave state machine checks for MXIbus parity errors. If it detects a parity error during the address phase of a cycle, the PXI-8320 ignores the cycle. If it detects a parity error during the data phase of a write cycle, the MXIbus slave state machine responds with a BERR* on the MXIbus. The transceivers ensure that the PXI-8320 meets the loading, driving, and timing requirements of the MXIbus specification for the AD[31–0], AM[4–0], and CONVERT* signals.

- **MXIbus Terminate**

  The PXI-8320 has onboard MXIbus termination to terminate the MXIbus signals if it is at either end of the cable. If the PXI-8320 is a middle device on the MXIbus, disable the termination.

- **MXIbus System Controller Functions**

  The PXI-8320 can act as the MXIbus system controller. When acting as the system controller, the PXI-8320 provides the MXIbus arbiter, priority-selection daisy-chain driver, and bus timeout unit. The PXI-8320 automatically detects from the MXIbus cable whether it is the system controller.

- **MXIbus Bus Timeout Unit**

  The PXI-8320 has a MXIbus bus timeout unit, which terminates (with BERR*) any MXIbus cycle in which DTACK* or BERR* are not asserted in a prescribed amount of time after DS* is asserted. The duration of the timeout is programmably selectable in the range of 30 µs to 500 ms.

- **Interrupt, Trigger, and Utility Signal Circuitry**

  This circuitry handles mapping of the interrupt, trigger, and utility signals to the MXIbus. The utility signals include SYSRESET*, SYSFAIL*, and ACFAIL*. This circuitry also generates interrupts from other conditions on the PXI-8320 and allows generation of the trigger or utility signals. The transceivers ensure that the PXI-8320 meets the loading, driving, and timing requirements of the MXIbus specification for the IRQ[7:1], ±TRIG[7:0], SYSRESET*, SYSFAIL*, and ACFAIL* signals.

3

PXI-8320 Configuration and Installation

This chapter contains the instructions to configure and install the PXI-8320 module.

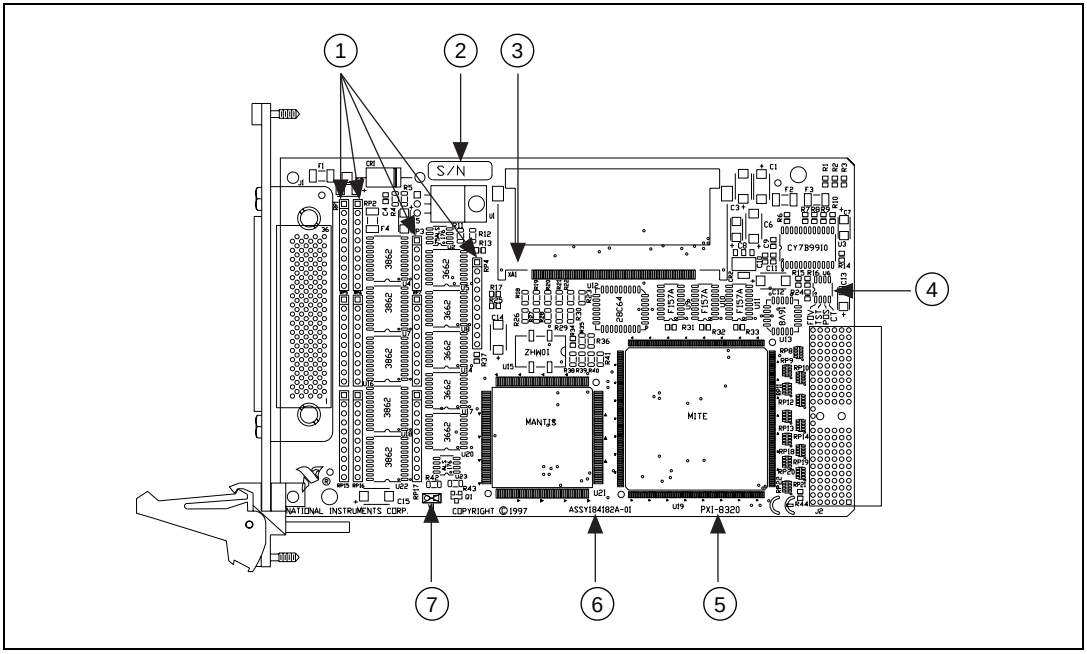
Warning ***Electrostatic discharge can damage several components on your PXI-8320 module. To avoid such damage in handling the module, touch the antistatic plastic package to a metal part of your chassis before removing the PXI-8320 from the package.***

Configure the PXI-8320

This section describes how to configure the following options on the PXI-8320:

- Configuration EEPROM
- Onboard DRAM
- 8320 termination

Figure 3-1 shows the PXI-8320. The drawing shows the location and factory-default settings on the module.



1	Termination Circuitry	3	DRAM	5	Product Name	7	W1
2	Serial Number	4	U6	6	Assembly Number		

Figure 3-1. PXI-8320 Parts Locator Diagram

Configuration EEPROM

The PXI-8320 has an onboard EEPROM, which stores default register values that are loaded at power-on. The EEPROM is divided into two halves—a factory-configuration half and a user-configuration half, so you can modify the user-configurable half while the factory-configured half stores a back-up of the default user settings. The factory configuration is a minimal configuration that can boot your PXI-8320 regardless of the changes made to the user configuration.

Use switch 1 (FOV) of the four-position switch at location U6 to control the operation of the EEPROM. Switch 1 determines whether the PXI-8320 boots from the factory-configured half or the user-configurable half. In its default setting, the PXI-8320 boots from the user-configurable half. This switch is useful for restoring the user-configured half of the EEPROM to the factory configuration values in the event that it becomes corrupted in

such a way that the PXI-8320 boots to an unusable state. See *Fixing an Invalid EEPROM Configuration* later in this chapter for more details on using switch 1.

The TST switch (switch 2 of U6) lets you change the default factory configuration settings by permitting writes to the factory settings section of the EEPROM. This switch serves as a safety measure and should not be needed under normal circumstances. When this switch is off (its default setting) the factory configuration of the EEPROM is protected so any writes to the factory area will be ignored. The factory area is protected regardless of the setting of switch 1 of U6.

Figure 3-2 shows the default configuration settings for EEPROM operation.

Caution ***Do not alter the settings of switches 3 and 4 of U6. Leave these switches as shown in Figure 3-2 unless specifically directed by National Instruments.***

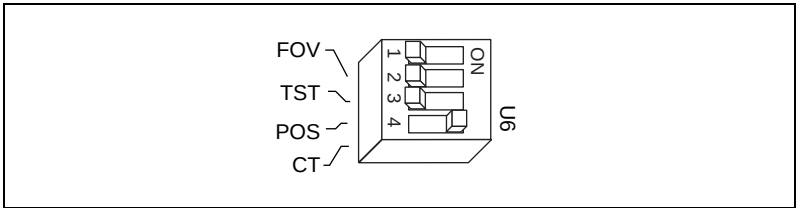


Figure 3-2. EEPROM Operation

Onboard DRAM

The PXI-8320 can accommodate one DRAM SODIMM. Table 3-1 lists the SODIMMs you can use. The PXI-8320 can hold up to 16 MB of onboard memory. The PXI-8320 supports DRAM speeds of 80 ns or faster.

Table 3-1. PXI-8320 DRAM Configurations

SODIMM	Total DRAM	National Instruments Option?
—	0	—
1M × 32	4 MB	YES
4M × 32	16 MB	YES

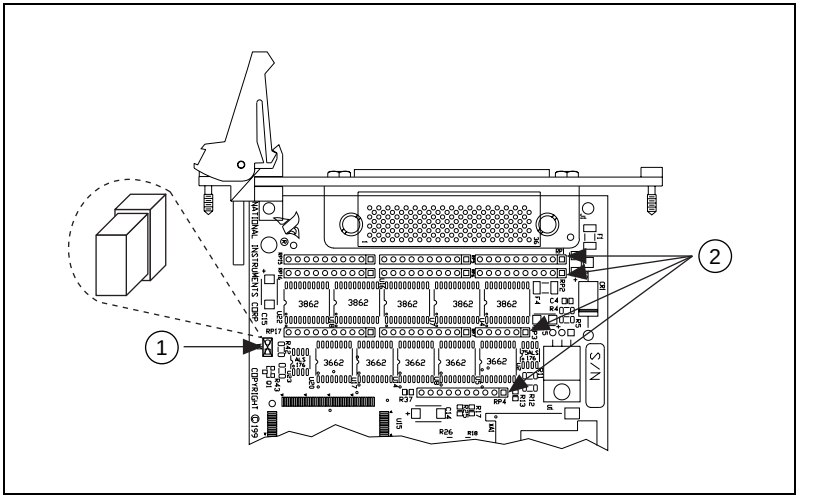
MXIbus Termination Option

The MXIbus requires that the first and last devices in the daisy-chain have a termination network. The PXI-8320 has the ability to terminate the MXIbus signals on the interface board using terminating resistor networks in single inline packages (SIPs). You should terminate only the first and last devices in the MXIbus daisy-chain.

The onboard termination option lets you install or remove terminating resistor networks from their sockets on the PXI-8320 board. The board is shipped from the factory with these terminating resistor networks installed. If your PXI-8320 is to be the first or last device in the MXIbus daisy-chain, leave these internal resistor terminators in place. Also leave the jumper on the pins at W1 in place when the PXI-8320 is an end device.

If you do *not* make the PXI-8320 an end device on the MXIbus daisy-chain, remove the jumper from the pins at W1 as well as *all* of the internal terminating resistor networks from their sockets. Store them in a safe place in case you later decide to change the MXIbus system configuration. When reinstalling the resistor networks, ensure that they are plugged firmly into their respective sockets.

Figure 3-3 shows the location of the terminating resistors and the W1 jumper. The figure shows the resistors and the jumper installed for use as an end device.



1	W1	2	Termination Circuitry

Figure 3-3. Terminating Resistors and Jumper W1

Install the PXI-8320

This section contains general installation instructions for the PXI-8320. Consult your computer user manual or technical reference manual for specific instructions and warnings.

1. Plug in your PXI or CompactPCI chassis before installing the PXI-8320. The power cord grounds the chassis and protects it from electrical damage while you install the module.

Warning ***To protect both yourself and the computer from electrical hazards, leave the chassis off until you finish installing the PXI-8320 module.***

2. Select any available PXI or CompactPCI peripheral slot.
3. Locate the metal bracket that covers the slot of the chassis that you have selected. Remove and save the bracket-retaining screw and the bracket cover.
4. Touch the metal part of the case to discharge any static electricity that might be on your clothes or body.
5. Line up the PXI-8320 with the card guides on the slot of the PXI/CompactPCI peripheral slot. Press down on the PXI-8320 until it seats in the chassis.
6. Screw in bracket-retaining screws to secure the PXI-8320 to the chassis.
7. Check the installation.

Fixing an Invalid EEPROM Configuration

`VXIedit` is the software configuration utility in the NI-VXI software. You can use this utility to edit the configuration of the PXI-8320. Some of these settings are stored in files that are read by the NI-VXI software, while other settings are stored directly in the PXI-8320 EEPROM. Certain EEPROM configurations can cause your PXI/CompactPCI computer to lock up while in its boot process. Generally, only the size and location of the memory windows can cause problems with the PXI-8320 locking up your system. For example, many PCI-based computers will not boot if a board in the system requests more memory space than the computer can allocate. If you encounter this situation, reduce the size of the PXI-8320 user window.

If this situation occurs after you change the configuration on the PXI-8320, follow these steps to reconfigure the PXI-8320.

1. Turn off your chassis.

Warning ***To protect both yourself and the chassis from electrical hazards, leave the chassis off while changing the settings on the PXI-8320 module.***

2. Remove the PXI-8320 from your PXI/CompactPCI chassis.
3. Change switch 1 (FOV) on U6 to the ON position as shown in Figure 3-4 to restore the factory configuration.

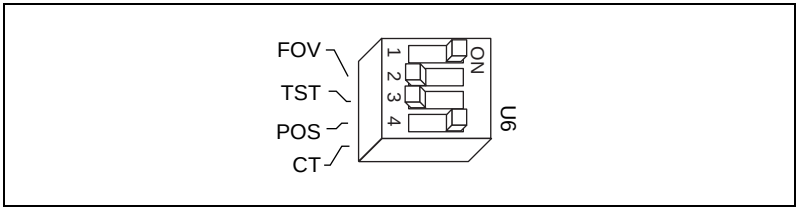


Figure 3-4. Restoring the Factory Configuration

Note ***If you have to remove the PXI-8320 module to access switch 1, follow the installation instructions given in the previous section to re-install the PXI-8320 module.***

4. Replace the PXI-8320.
5. Turn on the chassis. The computer should boot this time because it is using the factory-default configuration to initialize the PXI-8320 module.
6. Use the T&M Explorer utility in NI-VXI to re-adjust the configuration of your PXI-8320. For information on the software, including optional settings, use T&M Explorer and its online help. Use the Windows **Start** menu to open the NI-VXI program group and select **T&M Explorer**. To access the T&M Explorer online help, open the **Help** menu and select **Help Topics**.
7. After saving the configuration, exit Windows and turn off the chassis.
8. Remove the PXI-8320.
9. Change switch 1 (FOV) on U6 to the OFF position.
10. Replace the PXI-8320.
11. Turn on the chassis. If the computer does not boot with this configuration, you will have to repeat these steps, modifying your configuration until a final configuration is reached.

A

Specifications

This appendix lists various module specifications of the PXI-8320, such as physical dimensions and power requirements.

MXIbus Capability Descriptions

- Master-mode A32, A24, and A16 addressing
- Master-mode block transfers and synchronous block transfers
- Slave-mode A32, A24, and A16 addressing
- Slave-mode block transfers and synchronous block transfers
- Master-mode D32, D16, and D08 data sizes
- Slave-mode D32, D16, and D08 data sizes
- Optional MXIbus System Controller
- Can be a fair MXIbus requester
- Can lock the MXIbus for indivisible transfers
- Can terminate the MXIbus
- MXIbus master retry support
- MXIbus slave retry support
- Interrupt handler for levels 7 to 1
- Interrupt requester for levels 7 to 1
- MXIbus D32, D16, D08(O) interrupt handler
- MXIbus D32, D16, D08(O) interrupter
- Release on Acknowledge or Register Access interrupter
- MXIbus bus timer (programmable limit)
- Automatic MXIbus System Controller detection

PCI Functionality

Characteristic	Specification
PCI Initiator (Master) Capability	Supported
PCI Target (Slave) Capability	Supported
Data Path	32 bits
Card Voltage/Type	5 V only; 32-bit 3U-size card
Parity Generation/Checking, Error Reporting	Supported
Target Decode Speed	Medium (1 clock)
Target Fast-Back-to-Back Capability	Supported
Resource Locking	Supported as a master and slave
PCI Interrupts	Interrupts passed on INTA# signal
Base Address Registers	BAR 0 dedicated to local registers BAR 1-3 size configurable from 256 B to 4 GB
Expansion ROM	8 KB
PCI Master Performance (Ideal Maximum)	132 MB/s (16 Dwords max.)
PCI Slave Performance (Ideal Maximum)	33 MB/s (to local registers)

Requirements

Characteristic	Specification
Memory Space	32 KB minimum, programmable

Environmental

Characteristic	Specification
Temperature	0° to 55° C operating; –40° to 85° C storage
Relative Humidity	0% to 95% noncondensing, operating; 0% to 95% noncondensing, storage
EMI	FCC Class A Verified

Physical

Characteristic	Specification
Board Dimensions	160 by 100 mm (6.3 by 3.94 in.)
Connectors	Single fully implemented MXI-2 connector
Slot Requirements	Single CompactPCI/PXI Peripheral Slot
MTBF	Contact factory
Weight	0.18 kg (0.41 lb) typical (no DRAM installed)

Electrical

Source	Typical	Direct Current (Max)
+5 VDC	2.2 A	3.5 A

Performance

MXI Transfer Rate	
Peak	33 MB/s
Sustained	23 MB/s

B

MXI-2 Connector

This appendix describes the MXI-2 connector on the PXI-8320 module.

The MXI-2 connector is a 144-pin female connector manufactured by Meritec (Meritec part number 182800A-01). The mating cable assembly is National Instruments part number 182801A-*xxx*, where *xxx* is the length in meters.

Figure B-1 shows the MXI-2 connector on the PXI-8320. The drawing shows the pinout assignments for each pin, which are described in Table B-1.

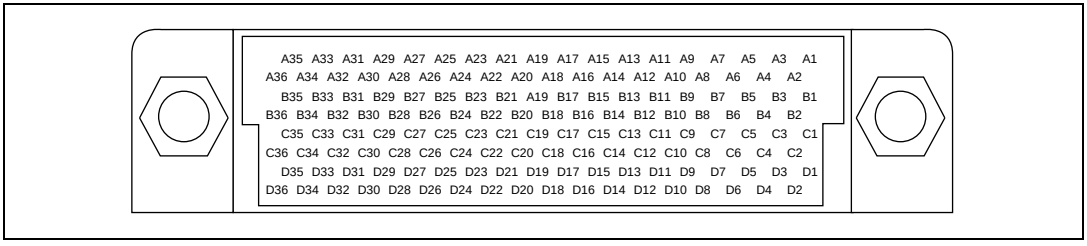


Figure B-1. MXI-2 Connector

Table B-1 lists the signal assignments for the MXI-2 connector.

Table B-1. MXI-2 Connector Signal Assignments

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	AD(31)*	B1	AD(14)*	C1	AM(4)*	D1	BUSY*
A2	GND	B2	GND	C2	GND	D2	GND
A3	AD(30)*	B3	AD(13)*	C3	AM(3)*	D3	IRQ(1)*
A4	GND	B4	GND	C4	GND	D4	GND
A5	AD(29)*	B5	AD(12)*	C5	AM(2)*	D5	IRQ(2)*
A6	GND	B6	GND	C6	GND	D6	GND
A7	AD(28)*	B7	AD(11)*	C7	AM(1)*	D7	IRQ(3)*

Table B-1. MXI-2 Connector Signal Assignments (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A8	GND	B8	GND	C8	GND	D8	GND
A9	AD(27)*	B9	AD(10)*	C9	AM(0)*	D9	IRQ(4)*
A10	GND	B10	GND	C10	GND	D10	GND
A11	AD(26)*	B11	AD(9)*	C11	WR*	D11	IRQ(5)*
A12	GND	B12	GND	C12	GND	D12	GND
A13	AD(25)*	B13	AD(8)*	C13	SIZE*	D13	IRQ(6)*
A14	GND	B14	GND	C14	GND	D14	GND
A15	AD(24)*	B15	AD(7)*	C15	DISBTO*	D15	IRQ(7)*
A16	GND	B16	GND	C16	GND	D16	GND
A17	AD(23)*	B17	AD(6)*	C17	ACFAIL*	D17	TRG(0)+
A18	GND	B18	GND	C18	GND	D18	TRG(0)–
A19	AD(22)*	B19	AD(5)*	C19	SYSRESET*	D19	TRG(1)+
A20	GND	B20	GND	C20	GND	D20	TRG(1)–
A21	AD(21)*	B21	AD(4)*	C21	SYSFAIL*	D21	TRG(2)+
A22	GND	B22	GND	C22	GND	D22	TRG(2)–
A23	AD(20)*	B23	AD(3)*	C23	BERR*	D23	TRG(3)+
A24	GND	B24	GND	C24	GND	D24	TRG(3)–
A25	AD(19)*	B25	AD(2)*	C25	DTACK*	D25	TRG(4)+
A26	GND	B26	GND	C26	GND	D26	TRG(4)–
A27	AD(18)*	B27	AD(1)*	C27	DS*	D27	TRG(5)+
A28	GND	B28	GND	C28	GND	D28	TRG(5)–
A29	AD(17)*	B28	AD(0)*	C29	AS*	D29	TRG(6)+
A30	GND	B30	GND	C30	GND	D30	TRG(6)–
A31	AD(16)*	B31	CONVERT*	C31	BREQ*	D31	TRG(7)+
A32	GND	B32	GND	C32	GND	D32	TRG(7)–

Table B-1. MXI-2 Connector Signal Assignments (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A33	AD(15)*	B33	PAR*	C33	GIN*	D33	CLK10+
A34	GND	B34	GND	C34	GND	D34	CLK10–
A35	5 V	B35	TERMPOWER	C35	GOUT*	D35	MXISC*
A36	5 V	B36	TERMPOWER	C36	GND	D36	ENDDEV

Table B-2 lists additional characteristics of the MXIbus signals.

Table B-2. MXIbus Signal Characteristics

Signal Category	Voltage Range	Max Current	Frequency Range
Each single-ended signal	0 to 3.4 V	60 mA	DC to 10 MHz
Each differential signal (D17–D34)	0 to 5 V	80 mA	DC to 10 MHz
Each 5 V (A35, A36)	5 V	1.75 A fused	DC
Each TERMPOWER (B35, B36)	3.4 V	1.75 A fused	DC

Note ***The characteristic impedance of all the MXIbus signals is 120 Ω.***

C

Customer Communication

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve your technical problems and a form you can use to comment on the product documentation. When you contact us, we need the information on the Technical Support Form and the configuration form, if your manual contains one, about your system configuration to answer your questions as quickly as possible.

National Instruments has technical assistance through electronic, fax, and telephone systems to quickly provide the information you need. Our electronic services include a bulletin board service, an FTP site, a fax-on-demand system, and e-mail support. If you have a hardware or software problem, first try the electronic support systems. If the information available on these systems does not answer your questions, we offer fax and telephone support through our technical support centers, which are staffed by applications engineers.

Electronic Services

Bulletin Board Support

National Instruments has BBS and FTP sites dedicated for 24-hour support with a collection of files and documents to answer most common customer questions. From these sites, you can also download the latest instrument drivers, updates, and example programs. For recorded instructions on how to use the bulletin board and FTP services and for BBS automated information, call 512 795 6990. You can access these services at:

United States: 512 794 5422
Up to 14,400 baud, 8 data bits, 1 stop bit, no parity

United Kingdom: 01635 551422
Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

France: 01 48 65 15 59
Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

FTP Support

To access our FTP site, log on to our Internet host, `ftp.natinst.com`, as `anonymous` and use your Internet address, such as `joesmith@anywhere.com`, as your password. The support files and documents are located in the `/support` directories.

Fax-on-Demand Support

Fax-on-Demand is a 24-hour information retrieval system containing a library of documents on a wide range of technical information. You can access Fax-on-Demand from a touch-tone telephone at 512 418 1111.

E-Mail Support (Currently USA Only)

You can submit technical support questions to the applications engineering team through e-mail at the Internet address listed below. Remember to include your name, address, and phone number so we can contact you with solutions and suggestions.

`support@natinst.com`

Telephone and Fax Support

National Instruments has branch offices all over the world. Use the list below to find the technical support number for your country. If there is no National Instruments office in your country, contact the source from which you purchased your software to obtain support.

Country	Telephone	Fax
Australia	03 9879 5166	03 9879 6277
Austria	0662 45 79 90 0	0662 45 79 90 19
Belgium	02 757 00 20	02 757 03 11
Brazil	011 288 3336	011 288 8528
Canada (Ontario)	905 785 0085	905 785 0086
Canada (Quebec)	514 694 8521	514 694 4399
Denmark	45 76 26 00	45 76 26 02
Finland	09 725 725 11	09 725 725 55
France	01 48 14 24 24	01 48 14 24 14
Germany	089 741 31 30	089 714 60 35
Hong Kong	2645 3186	2686 8505
Israel	03 6120092	03 6120095
Italy	02 413091	02 41309215
Japan	03 5472 2970	03 5472 2977
Korea	02 596 7456	02 596 7455
Mexico	5 520 2635	5 520 3282
Netherlands	0348 433466	0348 430673
Norway	32 84 84 00	32 84 86 00
Singapore	2265886	2265887
Spain	91 640 0085	91 640 0533
Sweden	08 730 49 70	08 730 43 70
Switzerland	056 200 51 51	056 200 51 55
Taiwan	02 377 1200	02 737 4644
United Kingdom	01635 523545	01635 523154
United States	512 795 8248	512 794 5678

Technical Support Form

Photocopy this form and update it each time you make changes to your software or hardware, and use the completed copy of this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name _____

Company _____

Address _____

_____

Fax (___) _____Phone (___) _____

Computer brand_____ Model _____ Processor_____

Operating system (include version number) _____

Clock speed _____MHz RAM _____MB Display adapter _____

Mouse ___yes ___no Other adapters installed_____

Hard disk capacity _____MB Brand_____

Instruments used _____

_____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is: _____

_____

_____

_____

_____

List any error messages: _____

_____

_____

The following steps reproduce the problem: _____

_____

_____

_____

_____

Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

National Instruments Products

PXI-8320 module part number _____

Serial number _____

Revision number _____

MXIbus terminators and W1 jumper installed or removed _____

EEPROM operation (U6 switches 1 and 2) _____

DRAM SIMMs installed _____

National Instruments software _____

Other Products

Computer make and model _____

Mainframe make and model _____

Microprocessor _____

Clock frequency or speed _____

Type of video board installed _____

Operating system version _____

Operating system mode _____

Other MXIbus devices in system _____

_____

Other VXIbus devices in system _____

_____

Base I/O address of other boards _____

DMA channels of other boards _____

Interrupt level of other boards _____

VXIbus/MXIbus Resource Manager (make, model, version, software version) _____

_____

Documentation Comment Form

National Instruments encourages you to comment on the documentation supplied with our products. This information helps us provide quality products to meet your needs.

Title: *PXI™-8320 User Manual*

Edition Date: December 1997

Part Number: 321717A-01

Please comment on the completeness, clarity, and organization of the manual.

_____

_____

_____

_____

_____

_____

_____

If you find errors in the manual, please record the page numbers and describe the errors.

_____

_____

_____

_____

_____

_____

_____

Thank you for your help.

Name _____

Title _____

Company _____

Address _____

_____

E-Mail Address _____

Phone (___) _____ Fax (___) _____

Mail to: Technical Publications
National Instruments Corporation
6504 Bridge Point Parkway
Austin, Texas 78730-5039

Fax to: Technical Publications
National Instruments Corporation
512 794 5678

Glossary

Prefix	Meanings	Value
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Symbols

°	degrees
Ω	ohms
%	percent

A

A	amperes
A16 space	VXIbus address space equivalent to the VME 64 KB short address space. In VXI, the upper 16 KB of A16 space is allocated for use by VXI devices configuration registers. This 16 KB region is referred to as VXI configuration space.
A24 space	VXIbus address space equivalent to the VME 16 MB *standard* address space.
A32 space	VXIbus address space equivalent to the VME 4 GB *extended* address space.
ACFAIL	A VMEbus backplane signal that is asserted when a power failure has occurred (either AC line source or power supply malfunction), or if it is necessary to disable the power supply (such as for a high temperature condition).

address	Character code that identifies a specific location (or series of locations) in memory.
address modifier	One of six signals in the VMEbus specification used by VMEbus masters to indicate the address space in which a data transfer is to take place.
address space	A set of 2^n memory locations differentiated from other such sets in VXI/VMEbus systems by six addressing lines known as address modifiers. *n* is the number of address lines required to uniquely specify a byte location in a given space. Valid numbers for *n* are 16, 24, and 32. In VME/VXI, because there are six address modifiers, there are 64 possible address spaces.
address window	A portion of address space that can be accessed from the application program.
ANSI	American National Standards Institute
arbitration	A process in which a potential bus master gains control over a particular bus.
asynchronous	Not synchronized; not controlled by time signals.

B

B	bytes
backplane	An assembly, typically a printed circuit board, with 96-pin connectors and signal paths that bus the connector pins. A C-size VXIbus system will have two sets of bused connectors called J1 and J2. A D-size VXIbus system will have three sets of bused connectors called J1, J2, and J3.
BERR*	Bus error signal
binary	A numbering system with a base of 2.
BIOS	Basic Input/Output System. BIOS functions are the fundamental level of any PC or compatible computer. BIOS functions embody the basic operations needed for successful use of the computer's hardware resources.

block-mode transfer	An uninterrupted transfer of data elements in which the master sources only the first address at the beginning of the cycle. The slave is then responsible for incrementing the address on subsequent transfers so that the next element is transferred to or from the proper storage location. In VME, the data transfer may have no more than 256 elements; MXI does not have this restriction.
BTO unit	Bus Timeout Unit; a functional module that times the duration of each data transfer and terminates the cycle if the duration is excessive. Without the termination capability of this module, a bus master attempt to access a nonexistent slave could result in an indefinitely long wait for a slave response.
bus master	A device that is capable of requesting the Data Transfer Bus (DTB) for the purpose of accessing a slave device.

C

C	Celsius
CLK10	A 10 MHz, ±100 ppm, individually buffered (to each module slot) differential ECL system clock that is sourced from Slot 0 of a VXIbus mainframe and distributed to Slots 1 through 12 on P2. It is distributed to each slot as a single-source, single-destination signal with a matched delay of under 8 ns.
CMOS	Complementary Metal Oxide Semiconductor; a process used in making chips.
Commander	A message-based device which is also a bus master and can control one or more Servants.
CompactPCI	
configuration registers	A set of registers through which the system can identify a module device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus specification requires that all VXIbus devices have a set of such registers.

D

daisy-chain	A method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus.
Data Transfer Bus	DTB; one of four buses on the VMEbus backplane. The DTB is used by a bus master to transfer binary data between itself and a slave device.
DIP	Dual Inline Package
DMA	Direct Memory Access; a method by which data is transferred between devices and internal memory without intervention of the central processing unit.
DRAM	Dynamic RAM
driver window	A region of PCI address space that is decoded by the PXI-8320 for use by the NI-VXI software.
DTACK*	Data Acknowledge signal
DTB	*See* Data Transfer Bus.
dynamic configuration	A method of automatically assigning logical addresses to VXIbus devices at system startup or other configuration times.
dynamically configured device	A device that has its logical address assigned by the Resource Manager. A VXI device initially responds at Logical Address 255 when its MODID line is asserted. A MXIbus device responds at Logical Address 255 during a priority select cycle. The Resource Manager subsequently assigns it a new logical address, which the device responds to until powered down.

E

ECL	Emitter-Coupled Logic
EEPROM	Electronically Erasable Programmable Read Only Memory
embedded controller	An intelligent CPU (controller) interface plugged directly into the VXI backplane, giving it direct access to the VXIbus. It must have all of its required VXI interface capabilities built in.
EMC	Electromechanical Compliance

EMI	Electromagnetic Interference
expansion ROM	An onboard EEPROM that may contain device-specific initialization and system boot functionality.
external controller	In this configuration, a plug-in interface board in a computer is connected to the VXI mainframe via one or more VXIbus extended controllers. The computer then exerts overall control over VXIbus system operations.

F

fair requester	A MXIbus master that will not arbitrate for the MXIbus after releasing it until it detects the bus request signal inactive. This ensures that all requesting devices will be granted use of the bus.

H

hex	Hexadecimal; the numbering system with base 16, using the digits 0 to 9 and letters A to F.
Hz	hertz; cycles per second.

I

IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
in.	inches
interrupt	A means for a device to request service from another device.
interrupt handler	A VMEbus functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identify information.
interrupt level	The relative priority at which a device can interrupt.
I/O	input/output; the techniques, media, and devices used to achieve communication between machines and users.
IRQ*	Interrupt signal

K

KB	Kilobytes of memory

L

LED	Light Emitting Diode
logical address	An 8-bit number that uniquely identifies each VXIbus device in a system. It defines the A16 register address of a device, and indicates Commander and Servant relationships.

M

m	meters
master	A functional part of a MXI/VME/VXIbus device that initiates data transfers on the backplane. A transfer can be either a read or a write.
master-mode operation	A device is in master mode if it is performing a bus cycle which it initiated.
MB	Megabytes of memory
MBLT	Eight-byte block transfers in which both the Address bus and the Data bus are used to transfer data.
message-based device	An intelligent device that implements the defined VXIbus registers and communication protocols. These devices are able to use Word Serial Protocol to communicate with one another through communication registers.
MITE	A National Instruments custom ASIC, a sophisticated dual-channel DMA controller that incorporates the Synchronous MXI and VME64 protocols to achieve high-performance block transfer rates.
MODID	Module Identification lines
MTBF	Mean Time Between Failure
MXI-2	The second generation of the National Instruments MXIbus product line. MXI-2 expands the number of signals on a standard MXIbus cable by including VXI triggers, all VXI interrupts, CLK10, SYSFAIL*, SYSRESET*, and ACFAIL*.

MXIbus	Multisystem eXtension Interface Bus; a high-performance communication link that interconnects devices using round, flexible cables.
MXIbus System Controller	A functional module that has arbiter, daisy-chain driver, and MXIbus cycle timeout responsibility. Always the first device in the MXIbus daisy-chain.

N

NI-VXI	The National Instruments bus interface software for VME/VXIbus systems.
Non-Slot 0 device	A device configured for installation in any slot in a VXIbus mainframe other than Slot 0. Installing such a device into Slot 0 can damage the device, the VXIbus backplane, or both.

O

Onboard RAM	The optional RAM installed into the SIMM slots of the PXI-8320 board.

P

PCI	Peripheral Component Interconnect. The PCI bus is a high-performance 32-bit or 64-bit bus with multiplexed address and data lines.
propagation	The transmission of signal through a computer system.
PXI	PCI Extensions for Instrumentation.

R

register-based device	A Servant-only device that supports VXIbus configuration registers. Register-based devices are typically controlled by message-based devices via device-dependent register reads and writes.
RESMAN	The name of the National Instruments Resource Manager in NI-VXI bus interface software. *See* Resource Manager.

Resource Manager	A message-based Commander located at Logical Address 0, which provides configuration management services such as address map configuration, Commander and Servant mappings, and self-test and diagnostic management.
retry	An acknowledge by a destination that signifies that the cycle did not complete and should be repeated.

S

s	seconds
Servant	A device controlled by a Commander; there are message-based and register-based Servants.
Shared Memory Protocol	A communication protocol that uses a block of memory that is accessible to both a client and a server. The memory block operates as a message buffer for communications.
slave	A functional part of a MXI/VME/VXIbus device that detects data transfer cycles initiated by a VMEbus master and responds to the transfers when the address specifies one of the device's registers.
slave-mode operation	A device is in slave mode it if is responding to a bus cycle.
Slot 0 device	A device configured for installation in Slot 0 of a VXIbus mainframe. This device is unique in the VXIbus system in that it performs the VMEbus System Controller functions, including clock sourcing and arbitration for data transfers across the backplane. Installing such a device into any other slot can damage the device, the VXIbus backplane, or both.
SODIMM	Small Outline Dual Inline Memory Module
statically configured device	A device whose logical address cannot be set through software; that is, it is not dynamically configurable.
SYSFAIL	A VMEbus signal that is used by a device to indicate an internal failure. A failed device asserts this line. In VXI, a device that fails also clears its PASSed bit in its Status register.
SYSRESET	A VMEbus signal that is used by a device to indicate a system reset or power-up condition.

System RAM	RAM installed on your personal computer and used by the operating system, as contrasted with onboard RAM, which is installed on the PXI-8320.

T

trigger	Either TTL or ECL lines used for intermodule communication.
TTL	Transistor-Transistor Logic

U

user window	A region of PCI address space reserved by the PXI-8320 for use via the NI-VXI low-level function calls. `MapVXIAddress()` uses this address space to allocate regions for use by the `VXIpeek()` and `VXIpoke()` macros.

V

V	volts
VDC	volts direct current
VIC or VICtext	VXI Interactive Control Program, a part of the NI-VXI bus interface software package. Used to program VXI devices, and develop and debug VXI application programs.
VME	Versa Module Eurocard or IEEE 1014
VMEbus System Controller	A device configured for installation in Slot 0 of a VXIbus mainframe or Slot 1 of a VMEbus chassis. This device is unique in the VMEbus system in that it performs the VMEbus System Controller functions, including clock sourcing and arbitration for data transfers across the backplane. Installing such a device into any other slot can damage the device, the VMEbus/VXIbus backplane, or both.
VXIbus	VMEbus Extensions for Instrumentation

VXIedit or VXItedit	VXI Resource Editor program, a part of the NI-VXI bus interface software package. Used to configure the system, edit the manufacturer name and ID numbers, edit the model names of VXI and non-VXI devices in the system, as well as the system interrupt configuration information, and display the system configuration information generated by the Resource Manager.
VXIinit	A program in the NI-VXI bus interface software package that initializes the board interrupts, shared RAM, VXI register configurations, and bus configurations.

W

Word Serial Protocol	The simplest required communication protocol supported by message-based devices in a VXIbus system. It utilizes the A16 communication registers to transfer data using a simple polling handshake method.
write posting	A mechanism that signifies that a device will immediately give a successful acknowledge to a write transfer and place the transfer in a local buffer. The device can then independently complete the write cycle to the destination.

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