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DAQ

NI 660*x* User Manual

NI 6601, NI 6602, and NI 6608 Devices

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This product is intended for use in industrial locations. However, harmful interference may occur in some installations, when the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.



Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.



Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 3 meters (10 feet).

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About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments NI 6601, NI 6602, and NI 6608 devices, and contains information about device operation and programming. Unless otherwise noted, text applies to all NI 660*x* devices. The PCI and PXI implementations are the same in functionality; their primary difference is the bus interface.

Related Documentation

The following documents contain information that you may find helpful as you read this manual:

- *Read Me First: Safety and Electromagnetic Compatibility*—Lists precautions to take to avoid possible injury, data loss, or a system crash.
- *NI 660x Specifications*—Contains all specifications for devices listed in this manual.
- *DAQ Getting Started* guides—Explains installation of the NI-DAQ driver software and the DAQ device, and how to confirm that the device is operating properly.
- *NI 6601/6602 Calibration Procedure*—Contains instructions for calibrating the NI 6601 and NI 6602.
- *NI 6608 Timing I/O Device Calibration Procedure*—Contains instructions for calibrating the NI 6608.
- *NI 660X Register-Level Programmer Manual*—Describes the programmable features and information necessary for the programming of devices in this manual.
- *NI-DAQmx Help*—Contains API overviews, general information about measurement concepts, key NI-DAQmx concepts, and common applications that are applicable to all programming environments. NI-DAQmx is the software you use to communicate with and control your DAQ device. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.
- *Measurement & Automation Explorer Help*—Contains information about configuring and testing supported NI devices using Measurement & Automation Explorer (MAX) for NI-DAQmx. For more information, in Measurement& Automation Explorer (MAX), select **Help»Help Topics»NI-DAQmx»MAX Help for NI-DAQmx**.

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- *DAQ Assistant Help*—Contains information about creating and configuring channels, tasks, and scales using the DAQ Assistant. For more information, in Measurement& Automation Explorer (MAX), select **Help»Help Topics»NI-DAQmx»DAQ Assistant**.
- *PXI Hardware Specifications Revision 2.1*—Introduces the PXI architecture and describes the electrical, mechanical, and software requirements for PXI. Available at `http://www.pxisa.org`.
- *PICMG Specification 2.0 3.0*—Details the CompactPCI Base specification. Available at `http://www.picmg.org`.



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1 Introduction

This chapter describes the NI 660*x* devices, lists what you need to get started, and describes optional equipment. If you have not already installed the TIO device, refer to the *DAQ Getting Started* documents.

The NI 660*x* devices are timing and digital I/O devices for use with the PCI bus in PC-compatible computers, PXI chassis, or CompactPCI chassis. The NI 6601 offers four 32-bit counter channels and up to 32 lines of individually configurable, TTL/CMOS-compatible digital I/O. The NI 6602 offers this capability and four additional 32-bit counter channels. The NI 6608 is a functional superset of the NI 6602 device with a high-stability clock called an oven-controlled crystal oscillator (OCXO).

The counter/timer channels have many measurement and generation modes, such as event counting, time measurement, frequency measurement, encoder position measurement, pulse generation, and square-wave generation.

The NI 660*x* devices contain the National Instruments MITE PCI interface. The MITE offers bus-master operation, PCI burst transfers, and high-speed DMA controller(s) for continuous, scatter-gather DMA without requiring DMA resources from your computer. Refer to the *Using PXI with CompactPCI* section for more information about your NI PXI-660*x* device.

Device specifications are available in the *NI 660x Specifications* document.

Using PXI with CompactPCI

Using PXI-compatible products with CompactPCI products is an important feature provided by *PXI Hardware Specification Revision 2.1*. If you use a PXI-compatible plug-in module in a CompactPCI chassis, you cannot use PXI-specific functions, but you can still use the basic plug-in device functions. For example, the RTSI bus on a PXI TIO Series device is available in a PXI chassis, but not in a CompactPCI chassis.

The specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the bus. Compatible operation is not guaranteed between devices with different sub-buses nor between devices with

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sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. The PXI TIO Series device works in any CompactPCI chassis adhering to the *PICMG 2.0 R3.0* core specification.

PXI-specific features are implemented on the J2 connector of the bus. The PXI device is compatible with any chassis with a sub-bus that does not drive the lines used by that device. Even if the sub-bus is capable of driving these lines, the PXI device is still compatible as long as those pins on the sub-bus are disabled by default and never enabled.

Caution Damage can result if these lines are driven by the sub-bus. NI is *not* liable for any damage resulting from improper signal connections.

Installation

Before installing your DAQ device, you must install the software you plan to use with the device.

1. **Installing application software**—Refer to the installation instructions that accompany your software.
2. **Installing the NI-DAQmx**—The *DAQ Getting Started* documents contain step-by-step instructions for installing software and hardware, configuring channels and tasks, and getting started developing an application.
3. **Installing the hardware**—The *DAQ Getting Started* documents contain non-software-specific information about how to install PCI, PXI, PCMCIA, and USB/IEEE 1394 devices, as well as accessories and cables.

Accessories and Cables

Table 1-1 lists the accessories and cables available for use with NI 660*x* devices.

Caution This NI product must be operated with shielded cables and accessories to ensure compliance with the Electromagnetic Compatibility (EMC) requirements defined in the Specifications section of this document. Do not use unshielded cables or accessories unless they are installed in a shielded enclosure with properly designed and shielded input/output ports and connected to the NI product using a shielded cable. If unshielded cables or accessories are not properly installed and shielded, the EMC specifications for the product are no longer guaranteed.

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Table 1-1. Accessories and Cables

Accessory	Description
SH68-68-D1	Shielded 68-conductor cable
R6868 cable	68-conductor flat ribbon cable
BNC-2121	BNC connector block with built-in test features
CA-1000	Configurable connector accessory
SCB-68A	Shielded screw connector block
TB-2715	Front-mount terminal block for NI PXI 660*x*
TBX-68	DIN-rail connector block
CB-68LP	Low-cost screw connector block
CB-68LPR	Low-cost screw connector block

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2

Device Overview

This chapter provides information about the functionality of NI 660*x* devices.

Digital I/O

The NI 660*x* devices have a 32-bit DIO port on PFI <0..31>. Digital I/O consists of asynchronous reads and writes to the digital port upon software command. You can individually configure each line for digital input or output. For output, you can individually configure PFI <8..31> for either counter-associated output or digital output. You must specify whether you are using the PFI line for counter I/O or digital I/O only if that line is being used as an output. For input, both counter I/O and digital I/O can share the lines on PFI <0..31>.

For more information about the signals that can be driven onto PFI lines, refer to the *I/O Connector Pinout* section of this document.

For information about how to implement specific digital I/O functions, refer to the application software documentation.

Prescaling

Prescaling allows the counter to count a signal that is faster than the maximum timebase of the counter. The counters on the NI 660*x* devices offer 8X and 2X prescaling on each counter (prescaling can be disabled). Each prescaler consists of a small, simple counter that counts to eight (or two) and rolls over. This counter is specifically designed for this application and can count signals that are faster than the general purpose counters. The Ctr*n*Source signal on the general purpose counter will be the divided signal from the simple counter.

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Figure 2-1 shows an example of prescaling.

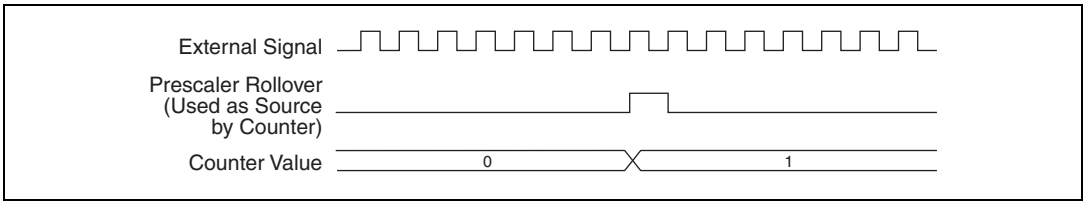


Figure 2-1. Prescaling Example

Prescaling is intended for use with two counter period and frequency measurements where the measurement is made on a continuous, repetitive signal. The prescaling counter cannot be read, so you cannot determine how many edges have occurred since the previous roll-over. You can also use prescaling for counting edges if it is acceptable to have an error of up to seven when using 8X prescaling or one when using 2X prescaling.

Pad Synchronization

The NI 660*x* devices allow synchronization of their PFI lines and RTSI lines at the I/O pads. This is called *pad synchronization* in this document, and *digital synchronization* in the NI-DAQmx API. You cannot use digital filtering while enabling this feature.

Pad synchronization is useful when several counters are measuring or operating off the same external signal. For example, suppose counters 0 and 1 are configured for triggered pulse generation and each counter uses the same external trigger (this external signal is connected to PFI 38 on the I/O connector and both counters have PFI 38 selected as their GATE). After the trigger signal propagates through the I/O pad of the ASIC, the time for the signal to reach the GATE of each counter within the ASIC may differ by a few nanoseconds.

This signal is sampled at the counters' GATEs using the selected SOURCE. Because of different propagation times for the paths to the two GATEs, it is possible for the counters to detect the trigger on different edges on SOURCE. Thus, one counter could see the trigger one SOURCE period after the other. If you want to allow the counters to see the changes in the signal at the same instance, you should use pad synchronization. During pad synchronization, the signal is offset by one clock cycle.

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This feature is useful in applications with two or more counters that are armed by an external start trigger, or that use the same PFI line as a counter control signal. Pad synchronization is only useful if the counters involved are using one of the internal timebases. A counter is using maximum timebase as its source if the synchronous counting mode is enabled for that counter.

Figures 2-2 and 2-3 illustrate how pad synchronization can be useful. These figures assume a 0.5 and a 0.75 SOURCE cycle delay between the PFI 38 input pin, and CTR 0 GATE and CTR 1 GATE, respectively. Figure 2-2 shows counter 0 at the gate edge on PFI 38 one source period before counter 1. Figure 2-3 shows both counters at the gate edge on PFI 38 at the same time.

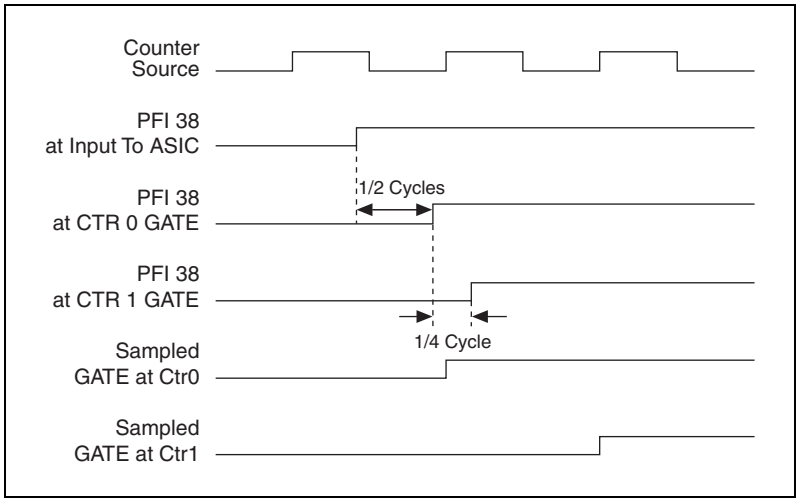


Figure 2-2. Counter 0 at Gate Edge on PFI 38 One Source Period before Counter 1

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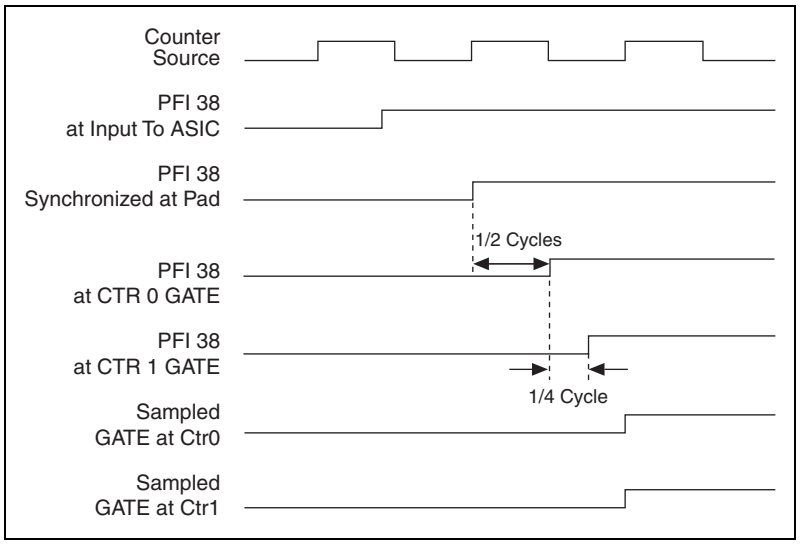


Figure 2-3. Counters 0 and 1 at Gate Edge on PFI 38 at the Same Time

Duplicate Count Prevention

Duplicate count prevention (or synchronous counting mode) ensures that a counter returns correct data in applications that are a slow or non-periodic external source. Duplicate count prevention applies only to buffered counter applications such as measuring frequency or period.

For such buffered applications, the counter should store the number of times an external source pulses between rising edges on the Gate signal.

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Example Application That Works Correctly (No Duplicate Counting)

Figure 2-4 shows an external buffered signal as the period measurement Source.

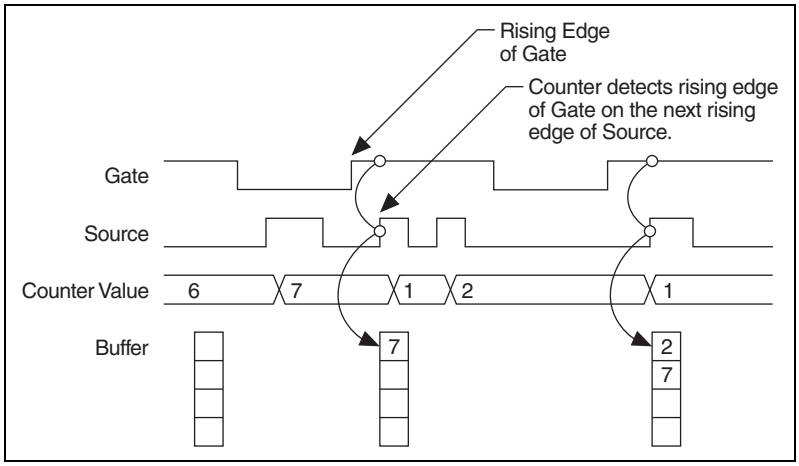


Figure 2-4. Example Application That Works Correctly

On the first rising edge of the Gate, the current count of 7 is stored. On the next rising edge of the Gate, the counter stores a 2 because two Source pulses occurred after the previous rising edge of Gate.

The counter synchronizes or samples the Gate signal with the Source signal. So the counter does not detect a rising edge in the Gate until the next Source pulse. In this example, the counter stores the values in the buffer on the first rising Source edge after the rising edge of Gate.

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Example Application That Works Incorrectly (Duplicate Counting)

In Figure 2-5, after the first rising edge of Gate, no Source pulses occur. So the counter does not write the correct data to the buffer.

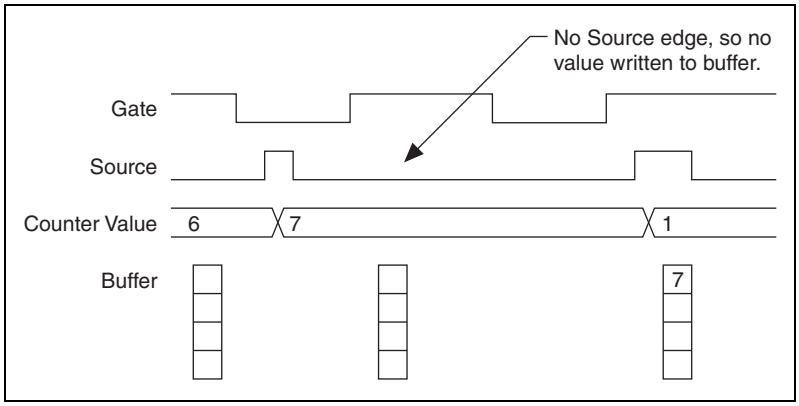


Figure 2-5. Example Application That Works Incorrectly

Example Application That Prevents Duplicate Counting

With duplicate count prevention enabled, the counter synchronizes both the Source and Gate signals to the maximum onboard timebase. By synchronizing to the timebase, the counter detects edges on the Gate even if the Source does not pulse. This enables the correct current count to be stored in the buffer even if no Source edges occur between Gate signals. Figure 2-6 shows an example application that prevents duplicate counting.

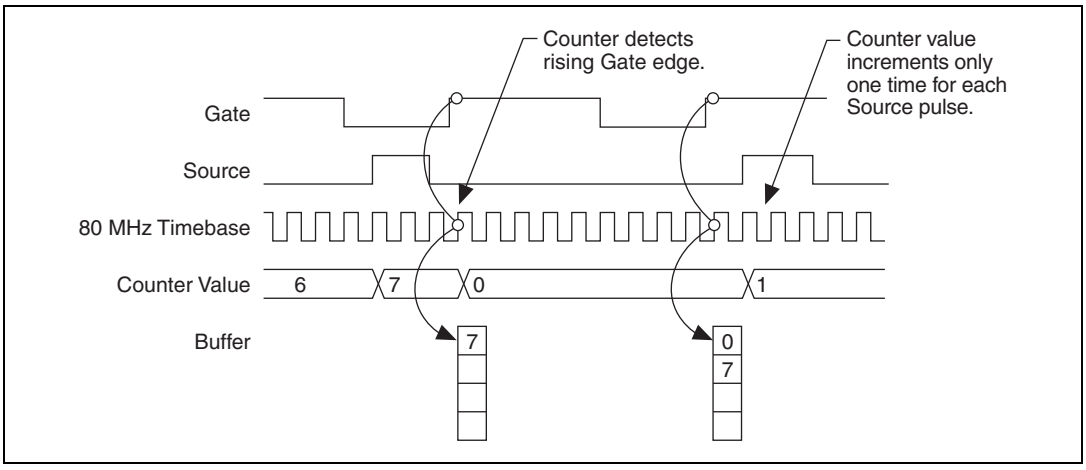


Figure 2-6. Example Application That Prevents Duplicate Counting

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Even if the Source pulses are long, the counter increments only once for each source pulse.

Normally, the counter and Counter *n* Internal Output signals change synchronously to the Source signal. With duplicate count prevention, the counter value and Counter *n* Internal Output signals change synchronously to the maximum onboard timebase.

Notice that duplicate count prevention should only be used if the frequency of the Source signal is one-fourth of the maximum onboard timebase.

Enabling Duplicate Count Prevention in NI-DAQmx

You can enable duplicate count prevention in NI-DAQmx by setting the **Enable Duplicate Count Prevention** attribute/property. For specific information on finding the **Enable Duplicate Count Prevention** attribute/property, refer to the help file for the API you are using. Refer to the *NI-DAQmx Help* for more information.

When to Use Duplicate Count Prevention

Use duplicate count prevention for buffered measurements that use an external Ctr*n*Source signal and the frequency of the signal is less than or equal to one-fourth of the maximum onboard timebase. Use this mode if you are using a low frequency or you expect zero Ctr*n*Source edges between successive edges of the Ctr*n*Gate signal.

You should use duplicate count prevention if the following conditions are true:

- You are making a buffered counter input measurement.
- You are using an external signal (such as PFI *x*) as the counter Source.
- The frequency of the external source is one-fourth of the maximum onboard timebase.
- You can have the counter value and output to change synchronously with the maximum onboard timebase.

In all other cases, you should *not* enable duplicate count prevention.

When Not to Use Duplicate Count Prevention

Use duplicate counter prevention only for buffered measurements with an external Ctr*n*Source signal. Do not use it when the Ctr*n*Source signal is greater than one-fourth of the maximum timebase.

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Transfer Rates

The maximum sustainable transfer rate a TIO device can achieve for a buffered acquisition depends on the following factors:

- Amount of available bus bandwidth
- Processor speed and operating system
- Application software

To reduce the amount of bus activity, limit the number of devices generating bus cycles. Because direct-memory access (DMA) transfers are faster than interrupt-driven transfers, NI-DAQmx uses DMA by default for buffered acquisitions.

Note The maximum sustainable transfer rate is always lower than the peak transfer rate.

Table 2-1 lists the maximum transfer rates for TIO devices.

Table 2-1. Maximum Transfer Rates

Operation	DMA		Interrupt	
	Buffer Size (Samples)	Rate (kS/s)	Buffer Size (Samples)	Rate (kS/s)
Finite	100	5,000	100	77
	1,000	2,150	1,000	77
	10,000	1,600	10,000	77
	100,000	1,350	100,000	77
Continuous	100	44	100	7
	1,000	202	1,000	46
	10,000	212	10,000	75
	100,000	245	100,000	76
	default	212	default	75

Note Transfer rates may vary depending on your computer hardware, operating system and system activity. This benchmark data was determined on an AMD Athlon XP 1800 computer with 128 MB of PC-2100 DDR RAM running Windows XP and LabVIEW using

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one counter of the TIO device. For continuous measurements, the transfer rate is the maximum sustained rate for 30 seconds on one counter.

High Precision Clock (NI 6608)

The accuracy of your time measurement and pulse generation is determined by the timing accuracy of your counter clock. The NI 6608 device has an oven-controlled crystal oscillator (OCXO) that provides a highly stable 10 MHz clock that you can use as a GATE or SOURCE of a counter. You can also use the OCXO as the PXI backplane clock. Modules phase locked to the PXI backplane clock will acquire the same clock stability as the NI 6608. For more information, refer to Info Codes at `ni.com/info` and search using keywords `rdpxib`, `ex9kw2`, and `ex8jnu`.

Using the OCXO as the SOURCE Counter

Using the OCXO as the timebase source of the counter, you can route the 10 MHz clock to Ctr*n*Source.

Using the OCXO as the 10 MHz PXI Backplane Clock

Your PXI chassis has a built-in 10 MHz backplane clock that is independently routed to each peripheral slot. An independent buffer on the chassis drives the clock signal to each peripheral slot with a skew of less than 1 ns between slots. You can use this common reference clock signal to synchronize multiple modules in a measurement or control system.

Use the OCXO 10 MHz clock to drive the PXI backplane clock so the modules in the other slots can take advantage of the stable timebase.

Note On NI PXI-660*x* devices, the maximum timebase is phase locked to the PXI backplane clock.

To use the OCXO 10 MHz clock as the PXI backplane clock, plug the NI PXI-6608 device into Slot 2, or the slot immediately to the right of the controller of the PXI chassis.

By default, NI-DAQ software drives the 10 MHz clock from the OCXO onto the PXI CLK10 in pin so that the OCXO is used as the PXI backplane clock. When the PXI chassis senses a clock on the PXI CLK10 in pin in Slot 2, the chassis disables its internal clock, then uses the OCXO clock instead, illustrated in Figure 2-7.

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Note The PXI CLK10 in pin is used as the PXI Star pin in other slots. The PXI Star pin is not used for the PXI backplane clock.

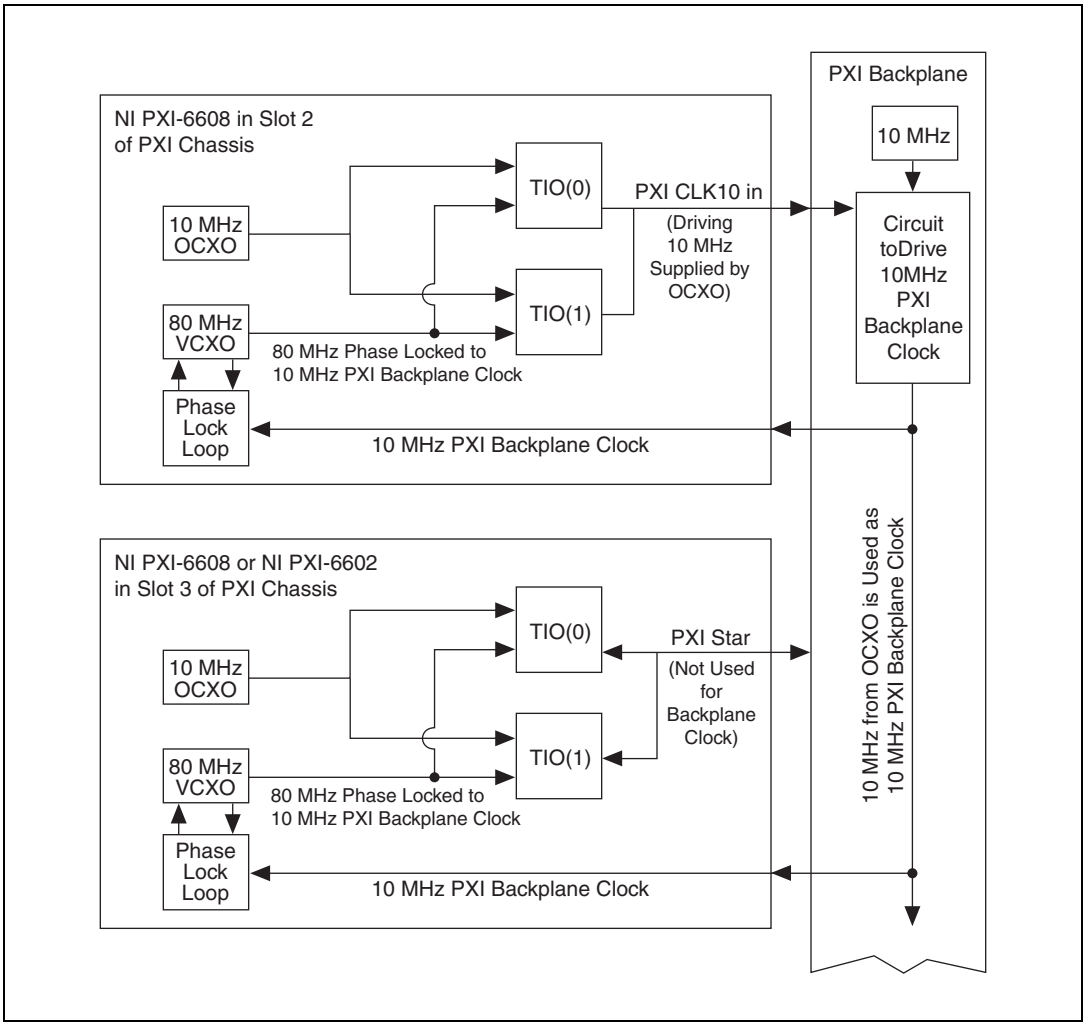


Figure 2-7. OCXO as the 10 MHz PXI Backplane Clock

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Measuring OCXO Stable Frequency Deviation

When you power the NI 6608 device, the OCXO requires adequate warm-up time to reach stable frequency. Five minutes is adequate warm-up time for a power-off duration of less than one hour, with maximum deviation within 20 ppb, or parts per billion, while four hours of operation is adequate for a power-off duration of up to 90 days.

Note For best performance, minimize power-off periods for the OCXO.

The OCXO is calibrated to within 0.1 Hz of 10.000000 MHz prior to shipment. Table 2-2 shows additional change in stable frequency that occurs over time. A change in stable frequency of approximately 45 ppb occurs after the first year of normal use.

Table 2-2. Change in Stable Frequency over Time

Days of Operation	Additional Change in Stable Frequency (ppb)
0-10	11.25
11-60	11.25
61-200	11.25
201-365	11.25
366-375	5.63
376-425	5.63
426-565	5.63
566-730	5.63
731-740	2.82
741-790	2.82

For example, if the OCXO has a perfect stable frequency of 10 MHz after warm-up, after the first 10 days of operation, the stable frequency drifts 11.25 ppb. During the next 50 days of operation, this frequency will drift an additional 11.25 ppb, thus making the total drift caused by aging to be 22.5 ppb. After 365 days, drift will be 45 ppb. If you calibrate the OCXO after 365 days of operation to restore the stable frequency to a perfect 10 MHz, the drift during the first 10 days following calibration (days 366-375) will now be 5.63 ppb—the stable frequency in this case will

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be 10 MHz ± 5.63 ppb after 375 days of operation. Calibration does not affect the drift in frequency; it only changes the stable frequency.

Calibration

When you are ready to calibrate your device to correct for drift in frequency, refer to the *NI 6601/6602 Calibration Procedure* or the *NI 6608 Timing I/O Device Calibration Procedure*. You can calibrate these devices in Traditional NI-DAQ (Legacy) only.

Register-Level Programming Information



Caution NI is *not* liable for any damage or injury that results from register-level programming the TIO Series devices.

For information about programming the NI 660*x* devices at the register level, refer to the *NI 660X Register-Level Programmer Manual*.

The National Instruments Measurement Hardware Driver Development Kit (MHDDK) provides development tools and a register-level programming interface for NI data acquisition hardware. The MHDDK provides access to the full register map of each device and offers examples for completing common measurement and control functions. The MHDDK works with TIO Series digital I/O and counter/timer I/O devices. Refer to `ni.com` for more information.

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3

Signal Connections

This chapter describes how to make input and output signal connections to NI 660*x* devices by way of the device I/O connector and the RTSI connector.

Programmable Function Interfaces (PFIs)

The 40 PFI pins are connected to the signal routing multiplexer for each timing signal, and software can select a PFI as the external source for a given timing signal. Any PFI pin can be used as an input by any timing signal and multiple timing signals can simultaneously use the same PFI pin. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You also can individually enable each PFI pin to output a specific internal timing signal.

You can individually enable many of the PFI pins to output a specific internal timing signal. For example, if you need the Counter 0 Source signal as an output on the I/O connector, software can turn on the output driver for the PFI 39/CTR 0 SRC pin.

Caution Do not drive a PFI signal externally when it is configured as an output.

When using the PFI pin as an input, you can individually configure each PFI for edge or level detection and for polarity selection. You can use the polarity selection for any of the timing signals, but the edge or level detection depends upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that signal.

Digital Filtering

Use the digital filter option available on the NI 660*x* PFI lines to eliminate glitches on input data. The filter operates off a filter clock and a fast internal sampling clock. The filter circuit samples the signal on the PFI line on each rising edge of the sampling clock. However, a change in the signal is propagated only if the signal maintains its new state for at least two

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consecutive rising edges of the filter clock. The frequency of the filter clock timebase determines whether a transition in the signal may propagate or not. The function of the internal sampling clock is to increase the sampling rate and prevent aliasing. Figure 3-1 demonstrates the function of this filter.

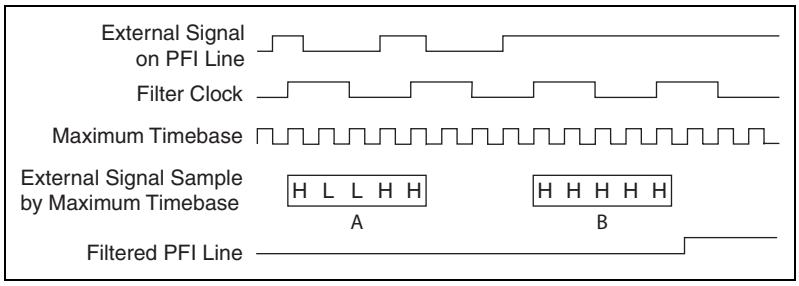


Figure 3-1. Digital Filtering

In period A, the filter blocks the glitches because the external signal does not remain steadily high from one rising edge of the filter clock to the next. In period B, the filter passes the transition because the external signal remains steadily high. Depending on when the transition occurs, the filter may require up to two filter clocks—one full filter interval—to pass a transition. The figure shows a rising (0 to 1) transition. The same filtering applies to falling (1 to 0) transitions.

Note The effect of filtering is that the signal transition is shifted by a minimum of one filter clock and a maximum of two filter clocks.

The filter is sensitive to the duration for which a digital signal transitions from one state to another. If a square wave is applied to the filter, its propagation will depend on its frequency and duty cycle.

There are four filter settings available in the TIO devices: 5 µs, 1 µs, 500 ns, and 100 ns. The 5 µs filter will pass all pulse widths (high and low) that are 5 µs or longer. It will block all pulse widths that are 2.5 µs (one-half of 5 µs) or shorter. Pulse widths between 2.5 µs and 5 µs may or may not pass, depending on the phase of the pulse with respect to the filter clock timebase. The same relationship extends to all other filter clocks.

In addition to these hard-wired filter clocks, you can use any PFI, RTSI, or internal signal as the source for the filter clock timebase. Use signals with a duty cycle as close to 50 percent as possible.

If the period of the filter clock timebase is $t_{fltrclk}$, this filter guarantees to pass pulse widths that are $2*t_{fltrclk}$ or longer and to block pulse widths that

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are $t_{fltrclk}$ or shorter. A pulse with a width between these two ranges may or may not pass, depending on the phase of the pulse with respect to the filter clock timebase.

Table 3-1 summarizes the properties of the different filter settings.

Table 3-1. Filter Settings

Filter Setting	Pulse Width Passed	Pulse Width Blocked
5 µs	5 µs	2.5 µs
1 µs	1 µs	500 ns
500 ns	500 ns	250 ns
100 ns	100 ns	50 ns
Programmable setting with period of clock = $t_{fltrclk}$	$2*t_{fltrclk}$	$t_{fltrclk}$

You individually configure the filter setting for each PFI line. The filters are useful to maintain signal integrity. They can prevent measurement errors caused by noise, crosstalk, or transmission line effects.

Note The digital filters on the NI 660*x* devices are not enabled by default.

For more information about using the digital filters on your device, refer to the *NI-DAQmx Help*.

Power-On State

The PFI lines are weakly pulled down within the NI-TIO ASIC, and the RTSI lines are weakly pulled high. Connections for pulling up the PFI lines or for stronger pull-down connections must be made external to the NI 660*x*. These connections affect the drive strength of NI 660*x* devices when the lines pulled up or down are used as outputs.

I/O Connector Pinout

Figure 3-2 shows the pinout of the NI 6601. Figure 3-3 shows the pinout of the NI 6602/6608. The descriptions beside each pin are in the following format: Signal Name / DIO Context / Counter Context (Default).

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Note The NI 6601 uses counters <0..3> only.

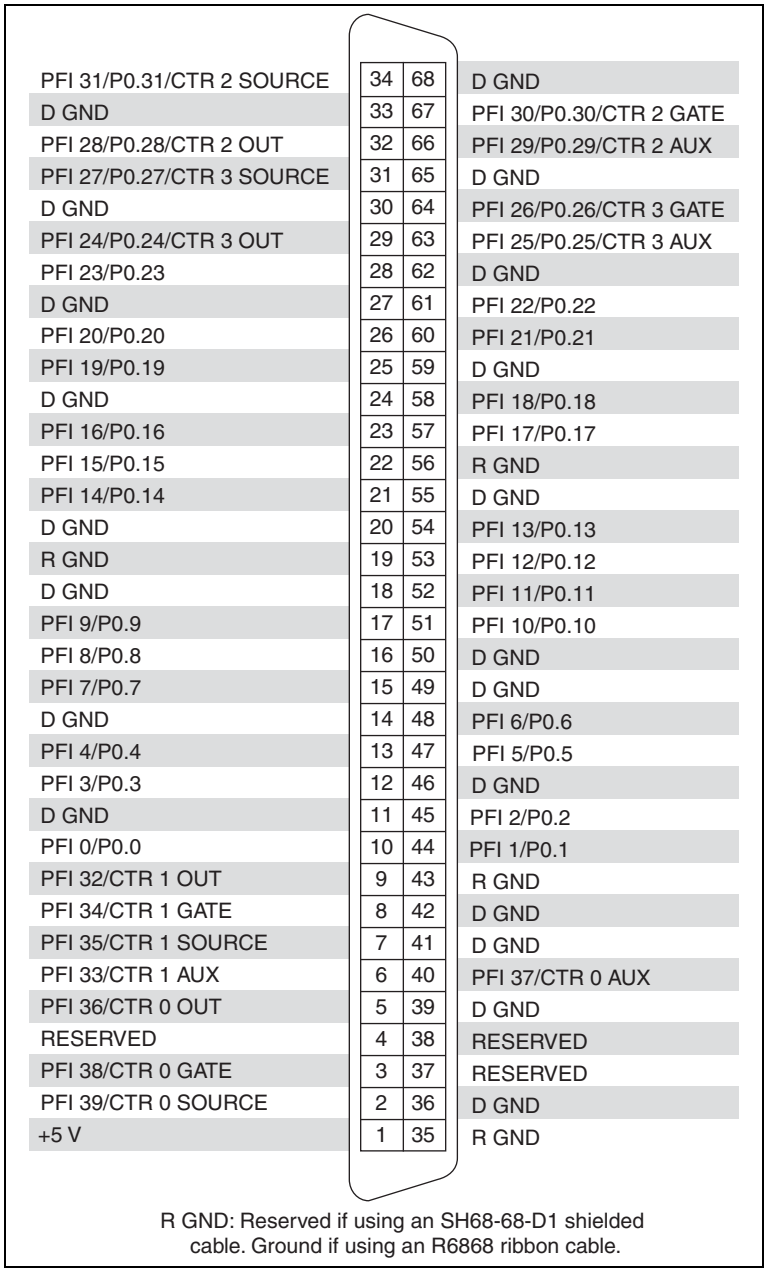


Figure 3-2. NI 6601 Pinout

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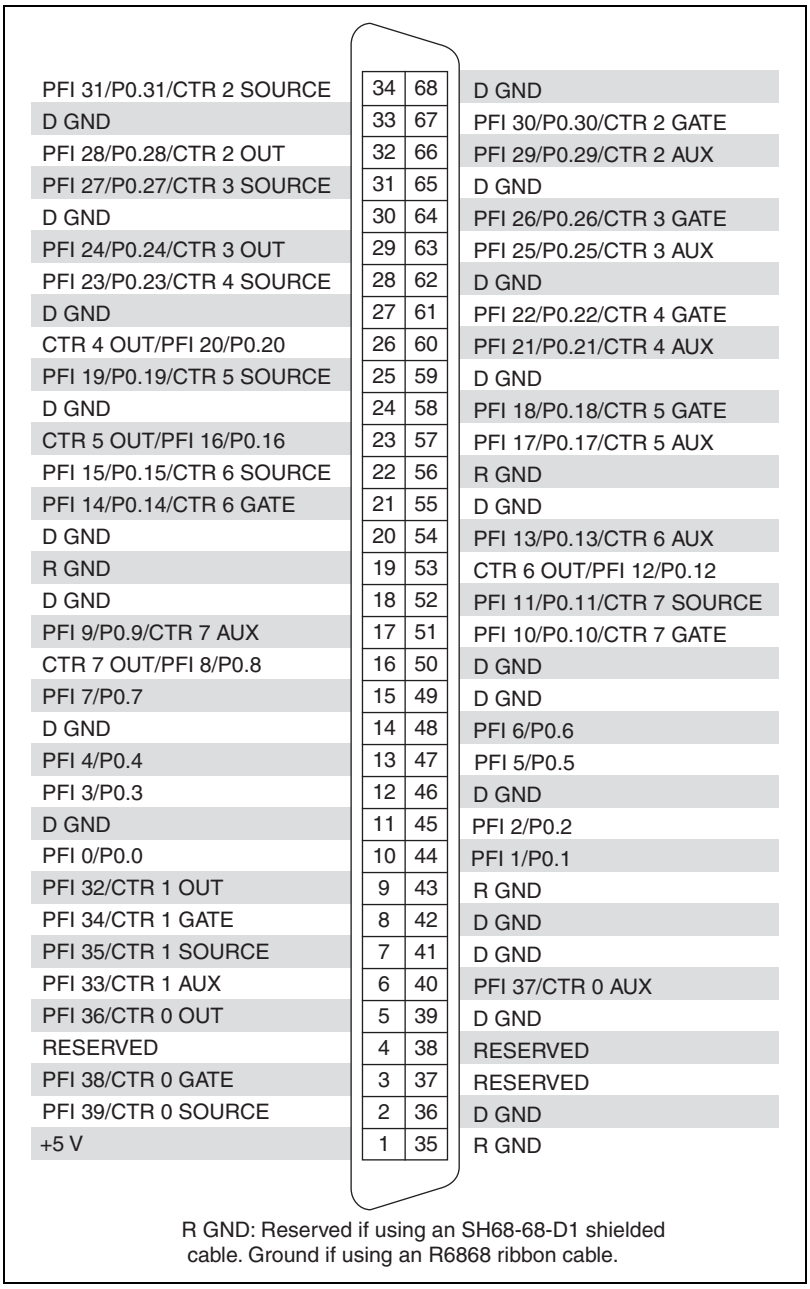


Figure 3-3. NI 6602/6608 Pinout

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Motion Encoder Context Pin Assignments

Table 3-2 lists the motion encoder context pin assignments for the I/O connector on NI 660*x* devices.

Table 3-2. NI 660*x* Motion Encoder Context Pin Assignments

Pin Number	Motion Encoder Context
2	channel A(0)
3	index/z(0)
6	channel B(1)
7	channel A(1)
8	index/z(1)
17	channel B(7)
21	index/z(6)
22	channel A(6)
25	channel A(5)
28	channel A(4)
31	channel A(3)
34	channel A(2)
40	channel B(0)
51	index/z(7)
52	channel A(7)
54	channel B(6)
57	channel B(5)
58	index/z(5)
60	channel B(4)
61	index/7(4)
63	channel B(3)
64	index/z(3)
66	channel B(2)
67	index/z(2)

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Outputs

PFI <0..7> are used for DIO only. PFI <32..39> are used for counters and motion encoders only. You can use PFI <8..31> as either of the three choices. When used as an output, you can individually configure each PFI line as a DIO line or a counter line (you need not distinguish between counter/encoder or DIO applications when you use a PFI line as an input).

Furthermore, the PFI lines associated with gates and sources can be used as outputs associated with the counter. When used as such, these PFI lines drive the selected GATE or SOURCE associated with these lines. For example, if PFI 39 is configured as an output, it will drive the selected SOURCE of counter 0.

Table 3-3 summarizes what you can drive onto the different PFI lines when they are used as outputs.

Table 3-3. PFI Lines Used as Outputs

PFI Line	Possible Signals
PFI 0	P0.0
PFI 1	P0.1
PFI 2	P0.2
PFI 3	P0.3
PFI 4	P0.4
PFI 5	P0.5
PFI 6	P0.6
PFI 7	P0.7
PFI 8	P0.8 or CTR 7 OUT[1]
PFI 9	P0.9
PFI 10	P0.10 or CTR 7 GATE[1]
PFI 11	P0.11 or CTR 7 SOURCE[1]
PFI 12	P0.12 or CTR 6 OUT[1]
PFI 13	P0.13
PFI 14	P0.14 or CTR 6 GATE[1]

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Table 3-3. PFI Lines Used as Outputs (Continued)

PFI Line	Possible Signals
PFI 15	P0.15 or CTR 6 SOURCE[1]
PFI 16	P0.16 or CTR 5 OUT
PFI 17	P0.17
PFI 18	P0.18 or CTR 5 GATE[1]
PFI 19	P0.19 or CTR 5 SOURCE[1]
PFI 20	P0.20 or CTR 4 OUT[1]
PFI 21	P0.21
PFI 22	P0.22 or CTR 4 GATE[1]
PFI 23	P0.23 or CTR 4 SOURCE[1]
PFI 24	P0.24 or CTR 3 OUT
PFI 25	P0.25
PFI 26	P0.26 or CTR 3 GATE
PFI 27	P0.27 or CTR 3 SOURCE
PFI 28	P0.28 or CTR 2 OUT
PFI 29	P0.29
PFI 30	P0.30 or CTR 2 GATE
PFI 31	P0.31 or CTR 2 SOURCE
PFI 32	CTR 1 OUT
PFI 33	Input only
PFI 34	CTR 1 GATE
PFI 35	CTR 1 SOURCE
PFI 36	CTR 0 OUT
PFI 37	Input only
PFI 38	CTR 0 GATE
PFI 39	CTR 0 SOURCE

[1] Counters 4 through 7 are not available in NI 6601 devices.

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Note For all NI 660*x* devices, output frequency on any of the pins should not exceed 40 MHz. The maximum frequency you can drive at the I/O connector is affected by the capacitive load your cable presents. You can achieve 40 MHz output with a National Instruments 1 m SH68-68-D1 shielded cable (capacitive load = 80 pF). At larger loads, your maximum output frequency may be lower.

Counters

The counters on TIO devices are a superset of the DAQ system timing controller (DAQ-STC) general-purpose counters developed by National Instruments. These counters are backward compatible with the DAQ-STC in functionality and software programming. The same software API and functions are used to program the DAQ-STC general-purpose counters and the counters on TIO devices.

The counters on TIO devices have two internal timebases: 100 kHz and 20 MHz. The counters on the NI 6602 and NI 6608 also have an 80 MHz timebase. Each counter has a gate, auxiliary, and source input. Each of these inputs can be an internal or external signal that connects to the I/O connector. Each counter also has an output signal.

Counter *n* Source Signal

You can select any PFI as well as many other internal signals as the Counter *n* Source (Ctr*n*Source) signal. The Ctr*n*Source signal is configured in edge-detection mode on either the rising or falling edge. The selected edge of the Ctr*n*Source signal increments and decrements the counter value depending on the application the counter is performing.

You can export the Ctr*n*Source signal to the I/O connector's default PFI input for each Ctr*n*Source. For example, you can export the Ctr0Source signal to the PFI 39/CTR 0 SRC pin, even if another PFI is inputting the Ctr0Source signal. This output is set to high-impedance at startup.

For most applications, unless you select an external source, the 80MHzTimebase signal (if available), 20MHzTimebase signal, or 100kHzTimebase signal generates the Ctr*n*Source signal.

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Figure 3-4 shows the timing requirements for the Ctr*n*Source signal.

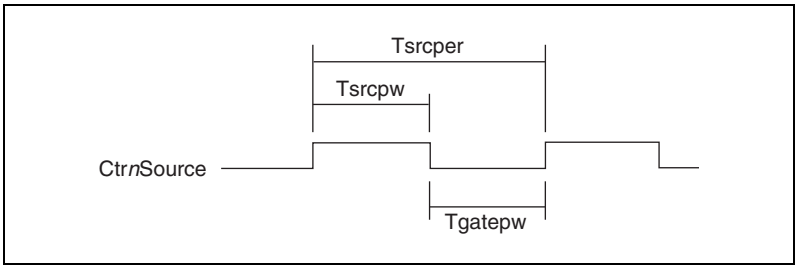


Figure 3-4. Timing Requirements for Ctr*n*Source Signal

Figure 3-4 shows the minimum pulse width and period that you must use for the Ctr*n*Source signal. This signal must satisfy both minimum criteria. If the high phase of the Ctr*n*Source signal is Tsrcpw ns, the low phase must be Tsrcper - Tsrcpw.

Table 3-4. Minimum Pulse Width and Period for Ctr*n*Source Internal Signals

Parameter	Minimum		Minimum with RTSI Connector	Description
	NI 6601	NI 6602		
Tsrcpw (without prescaling)	5 ns	5 ns	5 ns	Ctr*n*Source minimum pulse width (without prescaling)
Tsrcpw (with prescaling)	3.5 ns	3.5 ns	3.5 ns	Ctr*n*Source minimum pulse width (with prescaling)
Tsrcper (without prescaling)	50 ns	12.5 ns	50 ns	Ctr*n*Source minimum period (without prescaling)
Tsrcper (with prescaling)	16.67 ns	8 ns	16.67 ns	Ctr*n*Source minimum period (with prescaling)

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Counter Source to Counter Out Delay

Figure 3-5 shows the Ctr*n*Source to Ctr*n*InternalOutput delay.

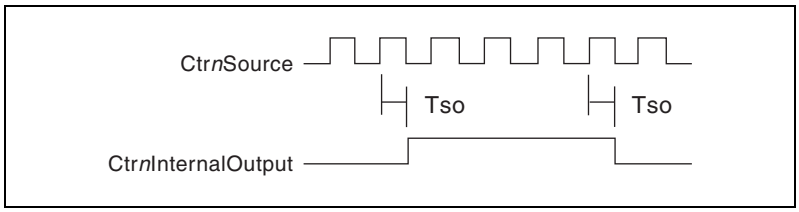


Figure 3-5. CtrnSource to CtrnInternalOutput Delay

Figure 3-5 shows the delay between the active edge of the Ctr*n*Source signal and the active edge of the Ctr*n*InternalOutput signal. In the figure, the Ctr*n*Source and Ctr*n*InternalOutput signals are active high. If you use the pulse output mode for the Ctr*n*InternalOutput signal, you will see the TC pulse one Ctr*n*Source period before the Ctr*n*InternalOutput toggles under the toggle output mode.

The output delay listed in Table 3-5 is for internal signals. The corresponding delay values at a connector block are larger due to cable delays.

Table 3-5. Output Delay for Internal Signals

Parameter	Typical	Maximum	Description
Tso	16 ns	26 ns	Ctr*n*Source to Ctr*n*InternalOutput delay

Note When using duplicate count prevention mode, the minimum period of signal used as the source of the counter must be greater than or equal to four times the period of the maximum timebase. For more information, refer to the *Duplicate Count Prevention* section of this document.

Counter *n* Gate Signal

You can select any PFI or RTSI, as well as many other internal signals like the Counter *n* Gate (Ctr*n*Gate) signal. The Ctr*n*Gate signal is configured in edge-detection or level-detection mode depending on the application performed by the counter. The gate signal can perform many different operations including starting and stopping the counter, generating interrupts, and saving the counter contents.

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You can export the Ctr*n*Gate signal to the I/O connector's default PFI input for each Ctr*n*Gate. For example, you can export the gate signal connected to counter 0 to the PFI 38/CTR 0 GATE pin, even if another PFI is inputting the Ctr0Gate signal. This output is set to high-impedance at startup.

Figure 3-6 shows the timing requirements for the Ctr*n*Gate signal.

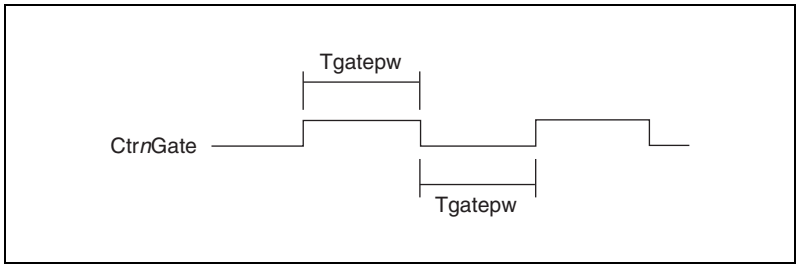


Figure 3-6. Timing Requirements for CtrnGate Signal

Table 3-6 shows the minimum pulse width required for the internal signals.

Table 3-6. Minimum Pulse Width for Ctr*n*Gate Internal Signals

Parameter	Minimum	Minimum with RTSI Connector	Description
Tgatepw	5 ns	5 ns	Ctr*n*Gate minimum pulse width

Note For buffered measurements, the minimum period required for the Ctr*n*Gate signal is determined by how fast the system can transfer data from your device to computer memory.

Counter *n* Auxiliary Signal

You can select any PFI or RTSI, as well as many other internal signals as the Counter *n* Auxiliary (Ctr*n*Aux) signal. Much like this Ctr*n*Gate signal, the Ctr*n*Aux signal is configured in edge-detection or level-detection mode depending on the application performed by the counter. The aux signal can perform many different operations including starting and stopping the counter, generating interrupts, and saving the counter contents. You can also use this signal to control the counting direction in edge-counting applications.

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Figure 3-7 shows the timing requirements for the Ctr*n*Aux signal.

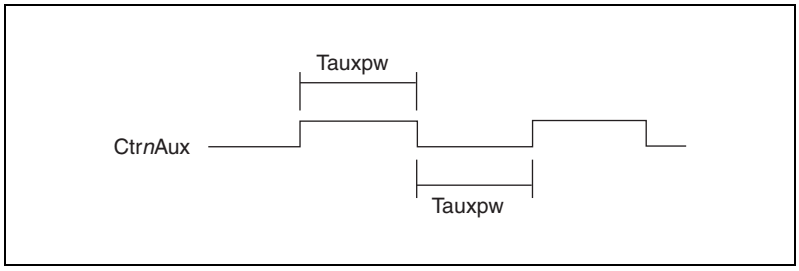


Figure 3-7. Timing Requirements for the CtrnAux Signal

Table 3-7. Minimum Pulse Width for Ctr*n*Aux Internal Signals

Parameter	Minimum	Minimum with RTSI Connector	Description
Tauxpw	5 ns	5 ns	Ctr*n*Aux minimum pulse width

Counter *n* Internal Output Signal

The Counter *n* Internal Output (Ctr*n*InternalOutput) signal is available only as an output on the CTR *n* OUT pin, where *n* is the number of your counter. For example, the Ctr0InternalOutput signal is available as an output on the PFI 36/CTR 0 OUT pin. You can also route the Ctr*n*InternalOutput signal to other locations on the board, such as RTSI.

The Ctr*n*InternalOutput signal reflects the terminal counter (TC) of counter *n*. The counter generates a terminal count when its count value rolls over. The two software-selectable output options are pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to high-impedance at startup.

Hardware Arm Start Triggers

You can arm each counter using a software command or by using the Arm Start Trigger. The Arm Start Trigger may be an internal or an external signal. By using the Arm Start Trigger, you can start more than one counter simultaneously by configuring each counter to use the same Arm Start Trigger signal.

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Counter Pairs

Each counter on the TIO is paired with another counter. This pairing allows some counter signals to connect to signals on the other counter. The counters are paired as ctr0 with ctr1, ctr2 with ctr 3, ctr 4 with ctr5, and ctr6 with ctr7.

Ctr0InternalOutput, which you can connect to Ctr1Gate, is an example of two signals that you can connect between the ctr0/ctr1 pair. Conversely, to connect Ctr0InternalOutput to Ctr2Gate, you must use other circuitry on the TIO device (such as RTSI Triggers).

Note The NI 6601 uses counters <0..3> only.

Counter Applications

You can use the TIO device in the following counter-based applications:

- Counting Edges
- Frequency Measurement
- Period Measurement
- Position Measurement with Linear and Angular Encoders
- Pulse Width Measurement
- Semi-Period Measurement
- Two-Edge Separation Measurement
- Pulse Generation

You can perform these measurements through programmed I/O, interrupt, or DMA data transfer mechanisms. The measurements can be finite or continuous in duration. Some of the applications also use start triggers, pause triggers, and hardware arm triggers.

Note For more information about programming counter applications and triggers in software, refer to the *NI-DAQmx Help*, and/or use the examples that are available with NI-DAQmx.

Real-Time System Integration Bus

TIO devices use the National Instruments Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. In a PCI system, the RTSI bus consists of the RTSI bus interface and a ribbon cable. The bus can route timing and

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trigger signals between several functions on as many as five DAQ devices in the computer. In a PXI system, the RTSI bus consists of the RTSI bus interface and the PXI trigger signals on the PXI backplane. This bus can route timing and trigger signals between several functions on as many as seven DAQ devices in the system. For a RTSI connector pinout, go to `ni.com/info` and enter `rtsipin`.

RTSI Triggers

TIO devices require a frequency timebase for its operation. This frequency timebase must come from the onboard crystal oscillator and is required even if the device is receiving a MasterTimebase signal from the RTSI trigger bus. Any TIO device can drive its 20MHzTimebase signal onto the RTSI Trigger 7 pin. Although some TIO devices have a 80MHzTimebase (such as the NI 6602), the RTSI bus cannot carry the 80MHzTimebase signal for bandwidth reasons. By default, TIO devices do not drive the RTSI Trigger 7 bus clock line.

Figure 3-8 shows the RTSI signal connection scheme for PCI TIO devices.

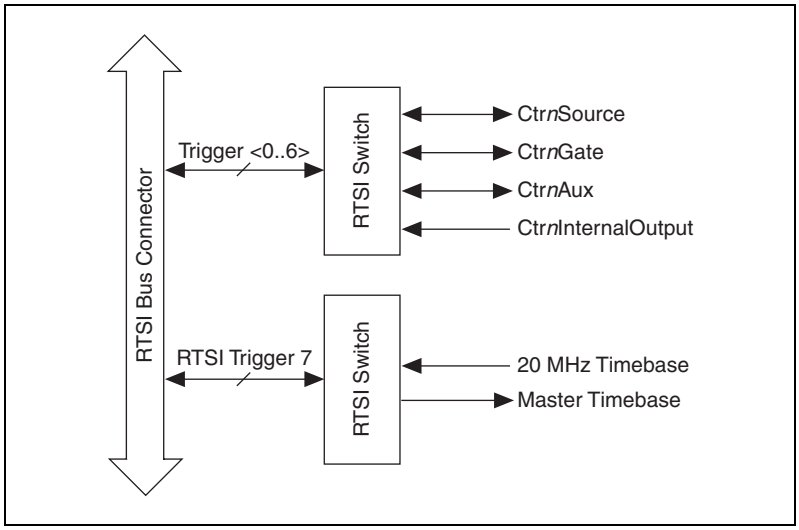


Figure 3-8. RTSI Signal Connection Scheme for PCI

PXI TIO devices use PXI trigger line 7 as their RTSI clock line. The maximum timebase provided by the PXI TIO device is phase locked to the 10 MHz PXI backplane clock. By using other PXI modules that phase lock their board clocks to the 10 MHz PXI backplane clock, you can better synchronize operation in a multi-module PXI system. The phase locking is

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enabled by default and can be disabled by way of software. If the module is used in a compact PCI chassis that does not have the 10 MHz PXI backplane clock, the phase locking is automatically disabled. Additionally, PXI trigger line 6 corresponds to PXI star trigger on PXI TIO devices.

Figure 3-9 shows the RTSI signal connection scheme for PXI TIO devices.

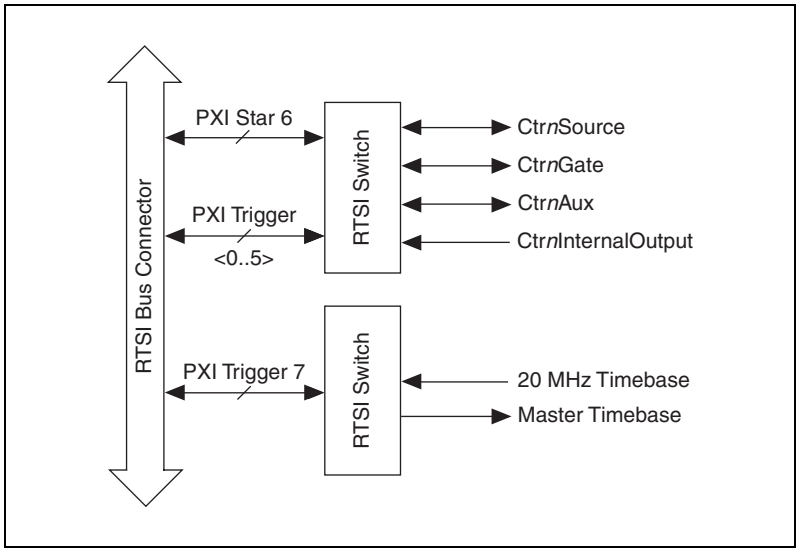


Figure 3-9. RTSI Signal Connection for PXI

+5 V Power Source

The +5 V pin on the I/O connector supplies power from the computer power supply through a self-resetting fuse. The fuse resets automatically within a few seconds after removal of an overcurrent condition. The power pin is referenced to the D GND pins and can supply power to external digital circuitry. The power rating for this +5V pin on NI 660*x* devices is +4.45 to +5.25 VDC at 1A.

Caution Do not connect the +5 V power pin directly to D GND, R GND, or any pin configured for output on NI 660*x* devices, or any voltage source or output pin on another device. Doing so can damage the device and the computer. National Instruments is not liable for damages resulting from such a connection.

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I/O Signals

Field Wiring Considerations

To prevent incorrect results caused by environmental noise and crosstalk, make sure the NI 660*x* and the peripheral device share a common ground reference. Connect one or more NI 660*x* device D GND lines to the ground reference of your peripheral device.

You can also use the digital filters available on each PFI line to reduce errors that these problems might cause.

Noise

For noise immunity, take the following precautions:

- When routing signals to the TIO device, keep cabling away from noise sources.
- Separate the TIO device signal lines from high-current or high-voltage lines. High-current or high-voltage lines that run in parallel paths at a close distance can induce currents in or voltages on the TIO device signal lines. To reduce the coupling between lines, separate parallel lines by a reasonable distance or run the lines at right angles to one another.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic and electric fields caused by monitors, electric motors, welding equipment, breakers, transformers, or other devices by running them through special metal conduits.
- Use appropriate digital filtering to remove noise.

Crosstalk

Crosstalk mainly occurs when the capacitance between lines in a cable induces a smaller transition on another line. Figure 3-10 shows an example of crosstalk.

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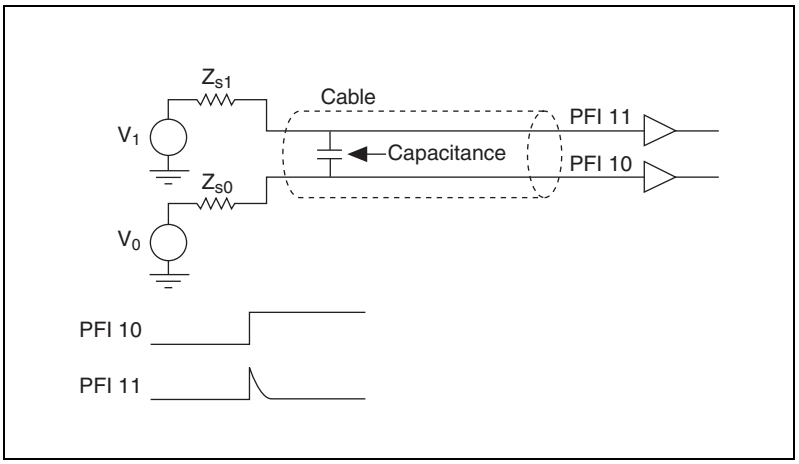


Figure 3-10. Crosstalk Example

In Figure 3-10, PFI 10 and PFI 11 are configured as inputs. V_0 drives PFI 10 and V_1 drives PFI 11. When PFI 10 (the offending line) transitions from one state to another, it induces a small transition in PFI 11 (the victim line). The magnitude of the transition (or crosstalk) induced in PFI 11 is proportional to the following:

- The speed of the transition on the offending line (PFI 10 in the previous example)
- The length of the cable and the proximity of the victim to the offending line
- The source impedance of the victim line (V_1 in the previous example) and the level of the offending line (V_0)

Crosstalk is most likely to cause measurement errors when the victim line is at a low voltage. If this crosstalk is 0.5 V or greater, you may get errors in measurement.

You should not experience crosstalk if the source impedance of the voltage source driving the victim line is less than 100 Ω. If this source impedance is larger than 100 Ω and you see crosstalk problems, you should use NI-TIO filters or a voltage follower with a low output impedance to drive the victim line.

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Inductive Effects

For high-speed signals, inductive effects can degrade signal integrity and cause ringing. To minimize inductive effects, you must minimize ground loops and allow a return path for currents. Twist your signal with a ground wire when you connect it to the 68-pin connector block you are using. Connect the signal wire to the PFI pin you are using and connect the ground wire to the adjacent D GND line with which the PFI line is twisted.

Figure 3-11 shows an example of wiring that minimizes inductive effects.

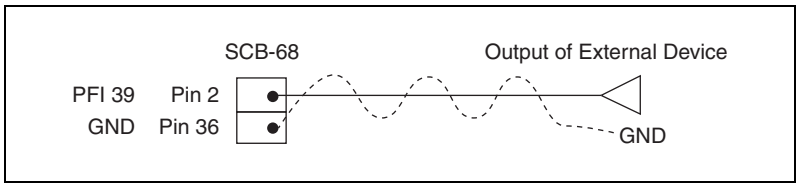


Figure 3-11. Example of Wiring That Minimizes Inductive Effects

The SH68-68-D1 cable is designed to help minimize inductive effects. Each signal line is twisted with a ground wire connected to a nearby pin. Each ground wire is shared by two signal lines.

Table 3-8 lists the signals and the D GND pin number on the 68-pin connector block.

Table 3-8. Signals and D GND Pin Number on 68-Pin Connector Block

PFI Number	Pin Number for D GND
PFI 0	11
PFI 1	
PFI 2	46
PFI 3	
PFI 4	14
PFI 5	
PFI 6	49
PFI 7	
PFI 8	50
PFI 9	

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Table 3-8. Signals and D GND Pin Number on 68-Pin Connector Block (Continued)

PFI Number	Pin Number for D GND
PFI 10	18
PFI 11	
PFI 12	20
PFI 13	
PFI 14	55
PFI 15	
PFI 16	24
PFI 17	
PFI 18	59
PFI 19	
PFI 20	27
PFI 21	
PFI 22	62
PFI 23	
PFI 24	30
PFI 25	
PFI 26	65
PFI 27	
PFI 28	33
PFI 29	
PFI 30	68
PFI 31	
PFI 32	42
PFI 33	39
PFI 34	42
PFI 35	41

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Table 3-8. Signals and D GND Pin Number on 68-Pin Connector Block (Continued)

PFI Number	Pin Number for D GND
PFI 36	39
PFI 37	41
PFI 38	36
PFI 39	

Transmission Line Effects

Transmission line effects can degrade the signal and cause measurement errors. Use twisted-pair wires to connect external signals to the device to improve impedance matching and signal integrity. NI 660*x* devices provide onboard series termination to reduce signal reflections when it drives an output.

For reflection problems that occur when the device drives the signal, use parallel AC termination at the destination. When using a National Instruments SH68-68-D1 cable, the recommended values for R_P and C_P are 68 Ω and 150 pF, respectively.

For reflection problems that occur when NI 660*x* devices receives the signal, use series termination at the device driving the signal. The sum of R_S and the output impedance of the source is approximately 80 Ω. Typically, this condition results in a value of approximately 50 Ω for R_S. To use serial termination when the source impedance is larger than 80 Ω, use a voltage follower with low output impedance, and connect R_S at the output of the voltage follower.

Note Before using a voltage follower or series termination, use digital filtering to eliminate measurement errors.

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Figure 3-12 shows an example of parallel and series termination.

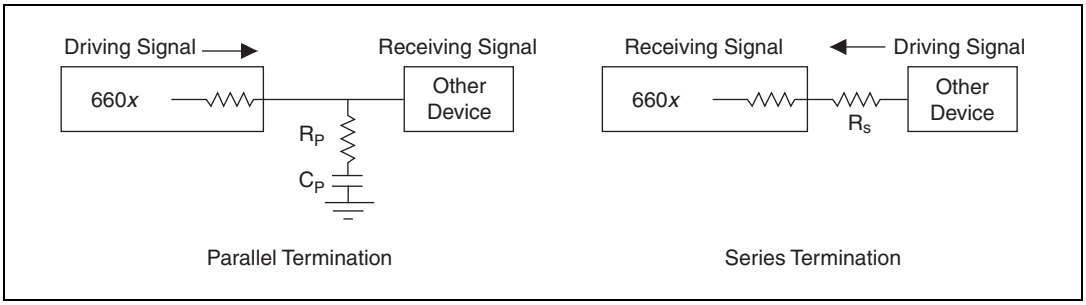


Figure 3-12. Parallel and Series Termination Example

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A

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