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PXI

NI PXI-6653 User Manual

Timing and Synchronization Module for PXI

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Worldwide Technical Support and Product Information

ni.com

National Instruments Corporate Headquarters

11500 North Mopac Expressway Austin, Texas 78759-3504 USA Tel: 512 683 0100

Worldwide Offices

Australia 61 2 9672 8846, Austria 43 0 662 45 79 90 0, Belgium 32 0 2 757 00 20, Brazil 55 11 3262 3599,
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Depending on where it is operated, this Class A product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.) Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products.

All Class A products display a simple warning statement of one paragraph in length regarding interference and undesired operation. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

Consult the FCC Web site at `www.fcc.gov` for more information.

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This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Mark Declaration of Conformity*, may cause interference to radio and television reception. Classification requirements are the same for the Federal Communications Commission (FCC) and the Canadian Department of Communications (DOC).

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

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Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

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To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* The CE Mark Declaration of Conformity contains important supplementary information and instructions for the user or installer.

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About This Manual

Thank you for purchasing the National Instruments PXI-6653 (NI 6653) Timing and Synchronization Module. The NI 6653 enables you to pass PXI timing and trigger signals between two or more PXI chassis. The NI 6653 can generate and route clock signals between devices in multiple chassis, providing a method to synchronize multiple devices in a multichassis PXI system.

This manual describes the electrical and mechanical aspects of the NI 6653 and contains information concerning its operation and programming.

Conventions

The following conventions appear in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIO<3..0>.

» — The **»** symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

 This icon denotes a tip, which alerts you to advisory information.

 This icon denotes a note, which alerts you to important information.

 This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the product, see the *Safety Information* for precautions to take.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.

CompactPCI — The CompactPCI bus is a Eurocard configuration of the PCI bus for industrial applications.

italic — Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.

`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.
NI 6653	This phrase refers to the NI 6653 module for the PXI bus.
PCI	The PCI bus is a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA.
PXI	The PXI bus is a rugged, open system for modular instrumentation based on CompactPCI, with special mechanical, electrical, and software features. The PXIbus standard was originally developed by National Instruments in 1997, and is now managed by the PXIbus Systems Alliance.

National Instruments Documentation

The *NI PXI-6653 User Manual* is one piece of the documentation set for your measurement system. You could have any of several other documents describing your hardware and software. Use the documentation you have as follows:

- Measurement hardware documentation—This documentation contains detailed information about the measurement hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and configuration instructions, specifications about the measurement hardware, and application hints.
- Software documentation—Please refer the `readme.htm` file on the *NI PXI-6653 Driver and Examples* CD, which ships with the device.

You can download NI documentation from `ni.com/manuals`.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *PICMG 2.0 R3.0, CompactPCI Core Specification*, available from PICMG, available from `www.picmg.org`
- *PXI Specification*, Revision 2.0, available from `www.pxisa.org`
- *NI-VISA User Manual*, available from `ni.com/manuals`
- *VISA Help*, available from `ni.com/manuals`
- *Getting Started with Multi-Chassis Synchronization Using the NI PXI-6653 and NI PXI-4472*, available from `ni.com/manuals`

1 Introduction

The NI 6653 timing and triggering module enables you to pass PXI timing signals between two or more PXI chassis. The NI 6653 generates and routes clock signals between devices in multiple chassis, providing a method for synchronizing multiple devices in a PXI system.

What You Need to Get Started

To set up and use the NI 6653, you need the following items:

- ❑ NI PXI-6653 Timing and Triggering Module
- ❑ *NI PXI-6653 User Manual*
- ❑ NI-VISA
- ❑ *NI PXI-6653 Driver and Examples* CD
- ❑ One of the following software packages and documentation:
  - LabVIEW
  - LabWindows™/CVI™
  - Microsoft Visual C++ (MSVC)
- ❑ PXI chassis
- ❑ PXI embedded controller or a desktop computer connected to the PXI chassis using MXI-3 hardware

If you are using the NI 6653 in a system to synchronize NI PXI-4472 modules, you can refer to *Getting Started with Multichassis Synchronization Using the NI PXI-6653 and the NI PXI-4472*, which you can download from `ni.com/manuals`.

Unpacking

The NI 6653 is shipped in an antistatic package to prevent electrostatic damage to the module. Electrostatic discharge (ESD) can damage several components on the module.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the module, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the module from the package.

Remove the module from the package and inspect the module for loose components or any sign of damage. Notify NI if the module appears damaged in any way. Do *not* install a damaged module into the computer.

Store the NI 6653 in the antistatic envelope when not in use.

Software Programming Choices

When programming the NI 6653, you can use NI application development environment (ADE) software such as LabVIEW or LabWindows/CVI, or you can use other ADEs such as Visual C/C++.

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive user interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

Safety Information

The following section contains important safety information that you *must* follow when installing and using the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do *not* substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. If you must operate the product in such an environment, it must be in a suitably rated enclosure.

If you need to clean the product, use a soft, nonmetallic brush. The product *must* be completely dry and free from contaminants before you return it to service.

Operate the product only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Do not install wiring while the product is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping modules. Remove power from signal lines before connecting them to or disconnecting them from the product.

Operate the product at or below the *installation category*[1] marked on the hardware label. Measurement circuits are subjected to *working voltages*[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Installation categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of installation categories:

- Installation Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.
- Installation Category II is for measurements performed on circuits directly connected to the electrical distribution system. This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 V for U.S. or 230 V for Europe). Examples of Installation Category II are measurements performed on household appliances, portable tools, and similar products.
- Installation Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired equipment such as equipment in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus-bars, junction boxes, switches, socket-outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- Installation Category IV is for measurements performed at the primary electrical supply installation (<1,000 V). Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

[1] Installation categories, also referred to as *measurement categories*, are defined in electrical safety standard IEC 61010-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers equipment. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

2

Installing and Configuring

This chapter describes how to install the NI 6653 hardware and software and how to configure the device.

Installing the Software

Please refer to the `readme.htm` file that accompanies the *NI PXI-6653 Driver and Examples* CD for directions on software installation.

Note Be sure to install the driver software *before* installing the NI 6653 hardware.

Installing the Hardware

The following are general installation instructions. Consult the chassis user manual or technical reference manual for specific instructions and warnings about installing new modules.

1. Power off and unplug the chassis.
2. Choose an available PXI slot in the PXI chassis.

Note The NI 6653 is usually installed in Slot 2.

3. Remove the filler panel for the PXI slot you chose in step 2.
4. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.
5. Insert the NI 6653 into the PXI slot. Use the injector/ejector handle to fully insert the module into the chassis.
6. Screw the front panel of the device to the front panel mounting rail of the chassis.
7. Visually verify the installation. Make sure the module is not touching other modules or components and is fully inserted into the slot.
8. Plug in and power on the chassis.

The NI 6653 is now installed.

Configuring the Module

The NI 6653 is completely software configurable. The system software automatically allocates all module resources, including base memory address and interrupt level.

The two LEDs on the front panel provide information about module status. The *NI 6653 Front Panel* section of Chapter 3, *Hardware Overview*, describes the LEDs in greater detail. Refer to Figure 3-2, *NI 6653 Front Panel*, for the parts locator diagram for the NI 6653.

3

Hardware Overview

This chapter presents an overview of the hardware functions of the NI 6653. Figure 3-1 provides a functional overview of the NI 6653 hardware.

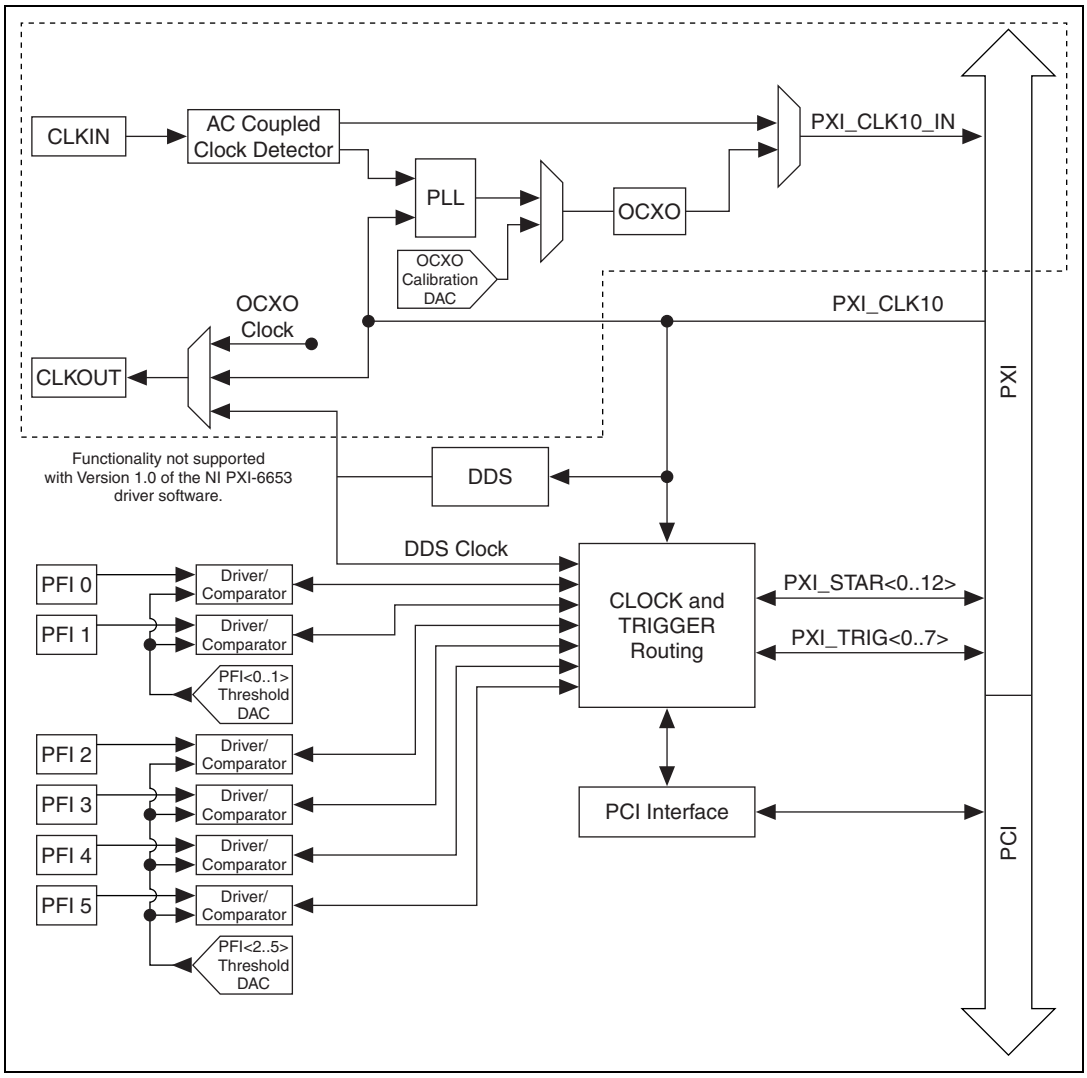
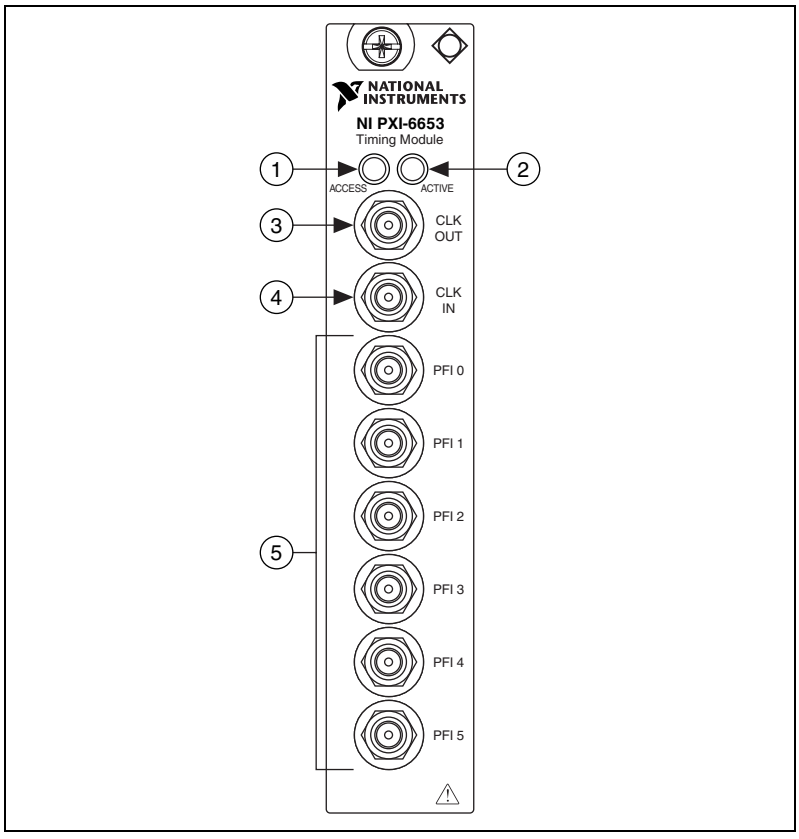


Figure 3-1. Functional Overview of the NI 6653

NI 6653 Front Panel

Figure 3-2 shows the connectors and LEDs on the front panel of the NI 6653.



1	Access LED	4	CLKIN Connector
2	Active LED	5	PFI <0..5> Connectors
3	CLKOUT Connector		

Figure 3-2. NI 6653 Front Panel

Access LED

The Access LED indicates the communication status of the NI 6653. Refer to Figure 3-2 for the location of the Access LED.

Table 3-1 summarizes what the Access LED colors represent.

Table 3-1. Access LED Color Indication

Color	Status
Off	Module is not yet functional.
Green	Driver has initialized the module.
Amber	Module is being accessed. The Access LED flashes amber for 50 ms when the module is accessed.

Active LED

The Active LED can indicate an error or phase-locked loop (PLL) activity. You can change the Active LED to amber[1], unless an error overrides the selection. Refer to Figure 3-2 for the location of the Active LED.

Tip Changing the Active LED color to amber is helpful when you want to identify devices in a multichassis situation or when you want an indication that your application has reached a predetermined section of the code.

[1] This feature is not supported in version 1.0 of the NI 6653 Driver Software.

Table 3-2 illustrates the meaning of each Active LED color.

Table 3-2. Active LED Color Quick Reference Table

Color	PXI_CLK10 Stopped	PLL Error[1]	User Setting[1]	PLL Active[1]
Red	Yes	Yes	—	—
Amber	—	—	Yes	—
Green	—	—	—	Yes
Off	—	—	—	—

[1] This feature is not supported in version 1.0 of the NI 6653 Driver Software

Note A red Active LED can indicate that either PXI_CLK10 has stopped *or* that there is a PLL error.

Connectors

This section describes the connectors on the front panel of the NI 6653.

- **CLKIN**[1]—Clock Input. This connector supplies the module with a clock that can be programmatically routed to the onboard PLL for use as a reference or routed directly to the PXI backplane (PXI_CLK10_IN) for distribution to the other modules in the chassis.
- **CLKOUT**[1] —Clock Output. This connector is used to source a clock that can programmatically be routed from the oven-controlled crystal oscillator (OCXO), Direct Digital Synthesis (DDS), or backplane clock (PXI_CLK10).
- **PFI <0..5>**—Programmable Function Interface <0..5>. These connectors can be used for either input or output. Additionally, **PFI 0** can be used as a clock input for internally synchronizing other signals. Refer to the *Synchronous Routing* section for more information about this functionality**.** You can program the behavior of these PFI connections individually.

Refer to Figure 3-2 for a diagram showing the locations of these connections on the NI 6653 front panel.

[1] This feature is not supported in version 1.0 of the NI 6653 Driver Software.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI PXI-6653 can damage the module and the computer. NI is *not* liable for any damage resulting from such signal connections.

Hardware Features

The NI 6653 performs two broad functions:

- Generating clock and trigger signals
- Routing internally or externally generated signals from one location to another

Table 3-3 outlines the function and direction of the signals that are discussed in detail in the remainder of this chapter.

Table 3-3. Signal Descriptions

Signal Name	Direction	Description
PXI_CLK10_IN[1]	In	This is an internal signal that can replace the native 10 MHz oscillator on the PXI backplane. PXI_CLK10_IN may originate from the onboard OCXO or from an external source.
PXI_CLK10	Out	This signal is the PXI 10 MHz backplane clock. By default, this signal is the output of the native 10 MHz oscillator in the chassis. An NI 6653 in Slot 2 can replace this signal with PXI_CLK10_IN.
OCXO Clock[1]	Out	This is the output of the 10 MHz OCXO. The OCXO is an extremely stable and accurate frequency source.
CLKIN[1]	In	CLKIN is a signal connected to the SMB input pin of the same name. CLKIN can serve as PXI_CLK10_IN or be used as a phase lock reference for the OCXO.
CLKOUT[1]	Out	CLKOUT is the signal on the SMB output pin of the same name. Either the OCXO clock or PXI_CLK10 may be routed to this location.

Table 3-3. Signal Descriptions (Continued)

Signal Name	Direction	Description
DDS Clock	Out	This is the output of the NI 6653 DDS. The DDS frequency can be programmed with fine granularity from 1 Hz to 80 MHz. The DDS chip automatically phase-locks to PXI_CLK10.
PXI_STAR<0..12>	In/Out	The PXI star trigger bus connects Slot 2 to Slot<3..15> in a star configuration. The electrical paths of each star line are closely matched to minimize intermodule skew. An NI 6653 in Slot 2 can route signals to Slots 3–15 using the star trigger bus.
PFI <0..5>	In/Out	The Programmable Function Interface pins on the NI 6653 route timing and triggering signals between multiple PXI chassis. A wide variety of input and output signals can be routed to or from the PFI lines.
PXI_TRIG<0..7>	In/Out	The PXI trigger bus consists of eight digital lines shared among all slots in the PXI chassis. The NI 6653 can route a wide variety of signals to and from these lines. **Note:** PXI_TRIG<0..5> are also known as RTSI <0..5> in some hardware devices and APIs. However, PXI_TRIG<6..7> are *not* identical to RTSI<6..7>.

[1] This feature is not supported in version 1.0 of the NI 6653 Driver Software.

The remainder of this chapter describes how these signals are used, acquired, and generated by the NI 6653 hardware, and explains how you can route the signals between various locations to synchronize multiple measurement devices and PXI chassis.

Clock Generation

The NI 6653 can generate two types of clock signals. The first clock is generated using the onboard DDS chip, and the second is generated with a precise 10 MHz oscillator. The following sections describe the two types of clock generation and explain the considerations for choosing either type.

Direct Digital Synthesis (DDS)

DDS is a method of generating a clock with programmable frequency. DDS consists of a *frequency tuning word*, an accumulator, a sine-lookup table, a D/A converter (DAC), and a comparator.

The frequency tuning word is a number that specifies the desired frequency. Each master clock cycle, the frequency tuning word is added to the accumulator, which rolls over when it gets to its maximum value. The accumulator value is used to get a point in the sine-lookup table, which is converted to an analog voltage by the DAC. For example, if the sine table is 128 points long, and the frequency tuning word is one, the accumulator takes 128 clock cycles to output one sine wave. If you change the frequency tuning word to 3, the accumulator steps through the sine table three times as fast, and outputs a sine wave in 128/3, or 42.6, clock cycles.

The output of the DAC is run through an analog filter to smooth the sine wave. The filtered output is then run through a comparator, which changes the output to a square wave with the specified frequency.

You can specify the programmable DDS frequency on the NI 6653 with a precision of better than 1 µHz within the range 1 Hz–80 MHz. The accuracy of the frequency depends on the PXI_CLK10 reference clock, so a precise 10 MHz source improves the accuracy of the DDS output. You can replace the 10 MHz clock with the OCXO for more accurate DDS timing.[1]

Tip For better jitter performance in low-frequency applications (below 5 MHz), you should run the DDS at a higher frequency and digitally divide it down rather than run the DDS at a low frequency. Refer to Figures 3-3 and 3-4 for schematic information on the DDS clock dividers.

PXI_CLK10 and OCXO[1]

The NI 6653 features a precision 10 MHz OCXO. The frequency accuracy of this clock is several orders of magnitude greater than the frequency accuracy of the native 10 MHz PXI backplane clock (PXI_CLK10).

The main source of error in most frequency reference oscillators is temperature variation. The OCXO houses the oscillator circuit inside of a sealed oven. A resistive heater and automatic feedback circuit maintain a precisely controlled operating temperature for the oscillator. This temperature-control scheme minimizes frequency error.

[1] This feature is not supported in version 1.0 of the NI 6653 Driver Software.

An NI 6653 module located in Slot 2 of a PXI chassis can replace the native PXI 10 MHz backplane frequency reference clock (PXI_CLK10) with the more stable and accurate output of the OCXO. All other PXI modules in the chassis that reference the 10 MHz backplane clock benefit from this more accurate frequency reference. Furthermore, the DDS chip on the NI 6653 references its output to the backplane clock and also takes advantage of the superior OCXO accuracy. The OCXO does not automatically replace the native 10 MHz clock; this feature must be explicitly enabled in software[1]. The OCXO output can also be routed out to the **CLKOUT** connector[1].

In addition to replacing the native backplane clock directly, the OCXO can phase lock to an external frequency source. This operation is discussed in detail in the *Using the PXI_CLK10 PLL* section.

Routing Signals

The NI 6653 has versatile trigger routing capabilities. It can route signals to and from the front panel, the PXI star triggers, and the PXI/RTSI triggers.

The NI 6653 also can route a 10 MHz clock from **CLKIN** to the PXI 10 MHz reference clock, or it can lock the OCXO to an external reference clock and send that to the PXI 10 MHz reference clock. The NI 6653 can route either the OCXO or the PXI 10 MHz reference clock to **CLKOUT**[1].

Figures 3-3 and 3-4 summarize the routing features of the NI 6653. The remainder of this chapter details the capabilities and constraints of the routing architecture.

[1] This feature is not supported in version 1.0 of the NI 6653 Driver Software.

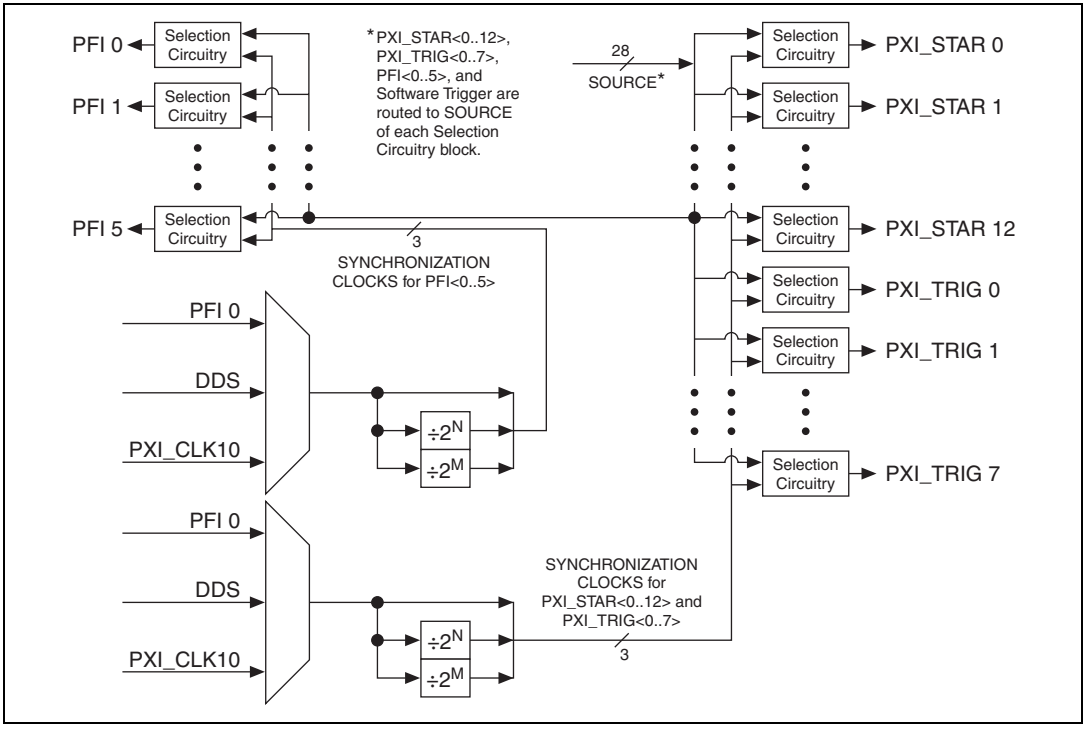


Figure 3-3. High-Level Schematic of NI 6653 Signal Routing Architecture

Figure 3-4 provides a more detailed view of the *Selection Circuitry* referenced in Figure 3-3.

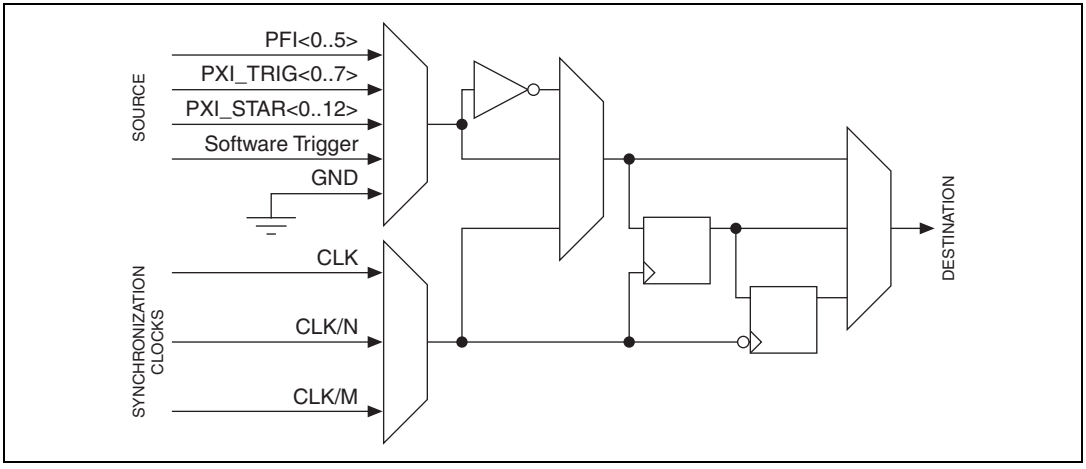


Figure 3-4. Signal Selection Circuitry Diagram

Determining Sources and Destinations

All signal routing operations can be characterized by a *source* (input) and a *destination*. In addition, synchronous routing operations must also define a third signal known as the *synchronization clock*. Refer to the *Choosing the Type of Routing* section for more information on synchronous versus asynchronous routing.

Table 3-4 summarizes the sources and destinations of the NI 6653. The destinations are listed in the horizontal heading row, and the sources are listed in the column at the far left. A ✓ in a cell indicates that the source and destination combination defined by that cell is a valid routing combination.

Table 3-4. Sources and Destinations for NI 6653 Signal Routing Operations

			Destinations					
			Front Panel		Backplane			Onboard
Sources	Front Panel	CLKIN	CLKOUT	PFI <0..5>	PXI_ CLK10_IN	PXI_Star Trigger <0..12>	RTSI/ PXI TRIG <0..7>	OCXO Reference PLL
		CLKIN			✓			✓
		PFI <0..5>		✓		✓	✓	
	Backplane	PXI_ CLK10	✓	✓		✓	✓	✓
		PXI_STAR <0..12>		✓		✓	✓	
		RTSI/PXI TRIG <0..7>		✓		✓	✓	
	Onboard	OCXO	✓		✓			
		DDS	✓	✓		✓	✓	
		Global Software Trigger		✓		✓	✓	

Using Front Panel PFIs As Inputs

The front-panel PFIs can receive external signals from 0 to +5 V. They can be terminated programmatically with 50 Ω resistances to match the cable impedance and minimize reflections.

Note Terminating the signals with a 50 Ω resistance is recommended when the source is another NI 6653 or any other source with a 50 Ω output.

The voltage thresholds for the front-panel PFI inputs are programmable. The input signal is generated by comparing the input voltage on the PFI connectors to the voltage output of software-programmable DACs. The threshold for PFI <0..1> can be set to one value, and the threshold for PFI <2..5> can be set to a second value. This capability is useful if you are importing signals from multiple sources with different voltage swings. The front panel PFI inputs can be routed to any PXI star triggers, PXI/RTSI triggers, or other front panel PFI outputs.

Using Front Panel PFIs As Outputs

The front panel PFI outputs are +3.3 V drivers with 50 Ω output impedance. The outputs can drive 50 Ω loads, such as a 50 Ω coaxial cable with a 50 Ω receiver. This cable configuration is the recommended setup to minimize reflections. With this configuration, the receiver sees a single +1.6 V step, a +3.3 V step split across the 50 Ω resistors at the source and the destination.

You also can drive a 50 Ω cable with a high-impedance load. The destination sees a single step to +3.3 V, but the source sees a reflection. This cable configuration is acceptable for low-frequency signals or short cables. You can select the signal source from the front panel triggers (PFI <0..5>), the PXI star triggers, the PXI/RTSI triggers, or the synchronization clock (PXI_CLK10 or the DDS clock). The synchronization clock concept is explained in more detail in the *Choosing the Type of Routing* section.

You can independently select the output signal source for each PFI line from one of the following sources:

- Another PFI <0..5>
- PXI/RTSI triggers <0..7> (PXI_TRIG<0..7>)
- PXI_STAR<0..12>
- Global software trigger
- Front panel synchronization clock

The front panel synchronization clock may be any of the following signals

- DDS clock
- PXI_CLK10
- **PFI 0** Input
- Any of the above signals divided by the first frequency divider (2^n, up to 512)
- Any of the above signals divided by the second frequency divider (2^m, up to 512)

Refer to the *Choosing the Type of Routing* section for more information on the synchronization clock.

Note The front panel synchronization clock is the same for all routing operations in which PFI <0..5> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI/RTSI Triggers

The PXI/RTSI triggers go to all the slots in the chassis. All modules receive the same PXI/RTSI triggers, so PXI/RTSI trigger 0 is the same for Slot 2 as it is for Slot 3, and so on. This feature makes the PXI/RTSI triggers convenient in situations where you want, for instance, to start an acquisition on several devices at the same time because all modules will receive the same trigger.

The frequency on the PXI/RTSI triggers should not exceed 20 MHz to preserve signal integrity. The signals do not reach each slot at precisely the same time. A difference of several nanoseconds between slots can occur in an eight-slot chassis. However, this delay is not a problem for many applications. You can route signals to the PXI/RTSI triggers from PFI <0..5>, from the PXI star triggers, or from other PXI/RTSI triggers. You also can route PXI_CLK10 or the DDS clock to a PXI/RTSI trigger line (PXI_TRIG<0..7>) using the synchronization clock.

You can independently select the output signal source for each PXI/RTSI trigger line from one of the following sources:

- PFI <0..5>
- Another PXI/RTSI trigger <0..7> (PXI_TRIG<0..7>)
- PXI_STAR <0..12>
- Global software trigger
- Backplane synchronization clock

The backplane synchronization clock may be any of the following signals:

- DDS clock
- PXI_CLK10
- **PFI 0** Input
- Any of the above signals divided by the first frequency divider (2^n, up to 512)
- Any of the above signals divided by the second frequency divider (2^m, up to 512)

Refer to the *Choosing the Type of Routing* section for more information about the synchronization clock.

Note The backplane synchronization clock is the same for all routing operations in which PXI/RTSI <0..5> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI Star Triggers

There are up to 13 PXI star triggers per chassis. Each trigger line is a dedicated connection between Slot 2 and one other slot. The *PXI Specification, Revision 2.0*, requires that the propagation delay along each star trigger lines be matched to within 1 ns. A typical upper limit for the skew in most PXI chassis is 500 ps. The low skew of the PXI star trigger bus is useful for applications that require triggers to arrive at several modules nearly simultaneously.

The star trigger lines are bidirectional, so signals can be sent to Slot 2 from a module in another slot or from Slot 2 to the other module.

You can independently select the output signal source for each PXI star trigger line from one of the following sources:

- PFI <0..5>
- PXI/RTSI triggers <0..7> (PXI_TRIG<0..7>)
- Another PXI star trigger line (PXI_STAR <0..12>)
- Global software trigger
- Backplane synchronization clock

Refer to the *Using the PXI/RTSI Triggers* section for more information on the backplane synchronization clock.

Choosing the Type of Routing

The NI 6653 routes signals in one of two ways: asynchronously or synchronously. The following sections describe the two routing types and the considerations for choosing each type.

Asynchronous Routing

Asynchronous routing is the most straightforward method of routing signals. Any asynchronous route can be defined in terms of two signal locations: A source and a destination. A digital pulse or train comes in on the source and is propagated to the destination. When the source signal goes from low to high, this rising edge is transferred to the destination after a propagation delay through the module. Figure 3-5 illustrates an asynchronous routing operation.

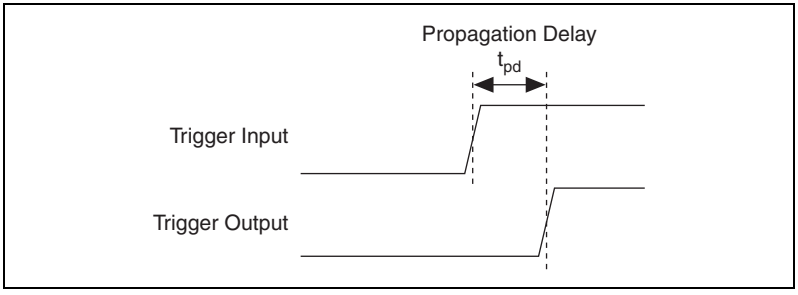


Figure 3-5. Asynchronous Routing Operation

Some delay is always associated with an asynchronous route, and this delay varies among NI 6653 modules, depending on variations in temperature and chassis voltage. Typical delay times in the NI 6653 for asynchronous routes between various sources and destinations are given in Appendix A, *Specifications*.

Asynchronous routing works well if the total system delays are not too long for the application. Propagation delay could be caused by the following reasons:

- Output delay on the source
- Propagation delay of the signal across the backplane(s) and cable(s)
- Propagation delay of the signal through the NI 6653
- Time for the receiver to recognize the signal

Both the source and the destination of an asynchronous routing operation on the NI 6653 can be any of the following lines:

- Any front panel PFI pin (PFI <0..5)
- Any PXI star trigger line (PXI_STAR<0..12>)
- Any PXI/RTSI trigger line (PXI_TRIG<0..7>)

Synchronous Routing

A synchronous routing operation is defined in terms of three signal locations: A source, a destination, and *synchronization clock*. A digital signal comes in on the source and is propagated to the destination after the edge has been realigned with the synchronization clock.

Unlike asynchronous routing, the output of a synchronous routing operation does not directly follow the input after a propagation delay. Instead, the output waits for the next rising edge of the clock before it follows the input. Thus, the output is said to be "synchronous" with this clock.

Figure 3-6 shows a timing diagram that illustrates synchronous routing.

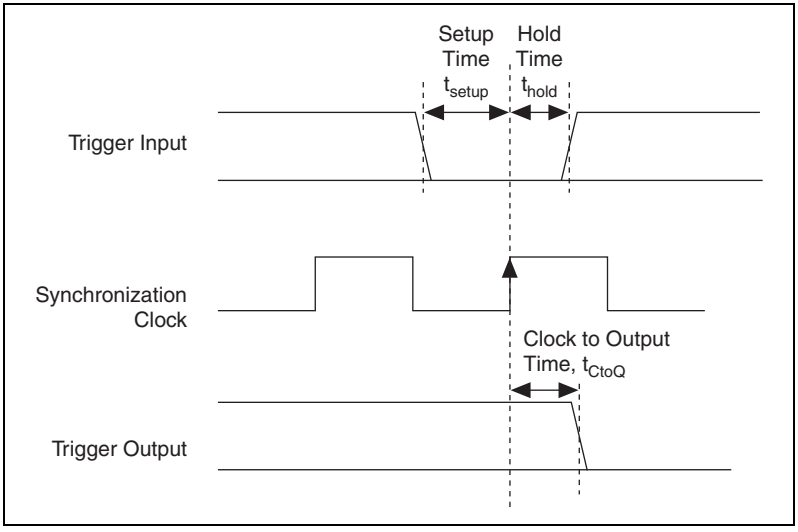


Figure 3-6. Synchronous Routing Operation

Synchronous routing can send triggers to several places in the same clock cycle or send the trigger to those same places after a deterministic skew of a known number of clock cycles. If a signal arrives at two chassis within the same clock cycle, each NI 6653 realigns the signal with the

synchronization clock and distributes it to the modules in each chassis at the same time. Synchronous routing can thus remove uncertainty about when triggers are received. If the delays through the system are such that an asynchronous trigger might arrive near the edge of the receiver clock, the receiver might see the signal in the first clock cycle, or it might see it in the second clock cycle. However, by synchronizing the signal, you can eliminate the ambiguity, and the signal will always be seen in the second clock cycle.

One useful feature of synchronous routing is that the signal can be propagated on either the rising or falling edge of the synchronization clock. In addition, the polarity of the destination signal can be inverted, which is useful when handling active-low digital signals.

Possible sources for synchronous routing include the following sources:

- Any front panel PFI pin
- Any PXI star trigger line (PXI_STAR<0..12>)
- Any PXI/RTSI trigger line (PXI_TRIG<0..7>)
- Global software trigger
- The synchronization clock itself

Note The possible destinations for a synchronous route are identical to those for an asynchronous route. The destinations include any front panel PFI pin, any PXI star trigger line, or any PXI/RTSI trigger line.

The synchronization clock for a synchronous route can be any of the following signals:

- 10 MHz PXI backplane clock signal
- DDS clock on the NI 6653
- Front panel **PFI 0** input
- One of two “divided copies” of any of the above three signals. The NI 6653 includes two clock-divider circuits that can divide the synchronization clock signals by any power of 2 up to 512.

Refer to the Figures 3-3 and 3-4 for an illustration of how the NI 6653 performs synchronous routing operations.

Generating a Single Pulse (Global SoftwareTrigger)

The global software trigger is a single pulse with programmable delay that is fired on a software command. This signal is always routed synchronously with a clock. Therefore, asynchronous routing is not supported when the signal source is the global software trigger.

The software trigger can be delayed by up to 15 clock cycles on a per route basis. This feature is useful if a single pulse must be sent to several destinations with significantly different propagation delays. By delaying the pulse on the routes with shorter paths, you can compensate for the propagation delay. An example of such a situation would be when a trigger pulse must arrive nearly simultaneously at the local backplane and the backplane of another chassis separated by 50 meters of coaxial cable.

Using the PXI_CLK10 PLL[1]

A module in Slot 2 of a PXI chassis can replace the PXI_CLK10 reference clock. The NI 6653 offers three options for this replacement. This section describes each of those options.

- The first option is to directly replace PXI_CLK10 with the OCXO output. This oscillator is a more stable and accurate reference than the native backplane clock.
- The second option is to route a 10 MHz clock directly from the front panel to PXI_CLK10_IN, which is the pin on the backplane that will replace PXI_CLK10. There is a delay through the module, as well as a distribution delay on the backplane. These delays tend to be similar for chassis of the same model, so routing the same clock to a pair of chassis usually matches PXI_CLK10 to within a few nanoseconds.
- The third option is to employ the NI 6653 PLL circuitry for the OCXO. As in option 1, the output of the OCXO replaces the native 10 MHz signal. However, this scheme also requires an input signal on **CLKIN**. This signal must be a stable clock, and its frequency must be a multiple of 1 MHz (5 MHz or 13 MHz, for example). The PLL feedback circuit generates a voltage proportional to the phase difference between the reference input on PXI_CLK10 and the output of the OCXO itself. This PLL voltage output then tunes the output frequency of the OCXO. As long as the incoming signal is a stable 1 MHz frequency multiple, the PLL circuit quickly locks the OCXO to the reference, eliminating all phase drift between the two signals.

[1] The PXI_CLK10 PLL is not supported with version 1.0 of the NI 6653 Driver Software.

Using the PLL provides several advantages over the other two options for replacing the PXI backplane clock:

- CLKIN is not required to be 10 MHz. If you have a stable reference that is a multiple of 1 MHz, such as 13 or 5 MHz, you can frequency-lock the chassis to it.
- If CLKIN stops or becomes disconnected, PXI_CLK10 is still present in the chassis.
- If CLKIN is 10 MHz, the NI 6653 can compensate for distribution delays in the backplane. The feedback in the PLL comes from PXI_CLK10. This PLL makes it possible for the NI 6653 to align clock edges at CLKIN with the edges of PXI_CLK10 that the modules receive. If you split an external (accurate) 10 MHz reference and route it to two chassis, they can both lock to it. The result is a tighter synchronization of PXI_CLK10 on the chassis.

4

Calibration

This chapter discusses the calibration of the NI 6653.

Calibration consists of verifying the measurement accuracy of a device and correcting for any measurement error. The NI 6653 is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the corrections that were needed to meet specifications—are stored in the onboard nonvolatile memory (EEPROM). The driver software uses these stored values.

Factory Calibration

The factory calibration of the NI 6653 involves calculating and storing four calibration constants. These values control the accuracy of four features of the device, which are discussed in the following sections.

OCXO Frequency

The OCXO frequency can be varied over a small range. The output frequency of the OCXO is adjusted using this constant to meet the specification listed in Appendix A, *Specifications*.

PXI_CLK10 Phase

When using the PLL to lock PXI_CLK10 to an external reference clock, the phase between the clocks can be adjusted. The time between rising edges of PXI_CLK10 and the input clock is minimized using this constant.

DDS Start Trigger Phase

In order to start the DDS reliably, the DDS start trigger must arrive within a certain window of time. The phase of the DDS start trigger is controlled by this constant to meet the setup and hold-time requirements of the DDS.

DDS Initial Phase

The phase of the DDS output is adjusted using this constant so that the DDS outputs from multiple NI 6653 modules are aligned.

User Calibration

User calibration of the NI 6653 is currently not supported.

Refer to `ni.com/calibration` for additional information on NI calibration services.

A

Specifications

All specifications are typical at 25 °C unless otherwise noted.

CLKIN Characteristics

CLKIN fundamental frequency range[1] ..... 1 MHz to 100 MHz, sine or square wave

Input impedance ..... 50 Ω ±5%

Input coupling ..... AC

Voltage range ..... 400 mV_{p-p} to 5 V_{p-p}

Absolute maximum input voltage[2] ..... 6 V_{p-p}, max

CLKIN to PXI_CLK10_IN delay

- Uncompensated ..... 11 ns to 11.7 ns
- PLL compensated ..... ±1 ns, max

CLKIN frequency accuracy

- For PLL and OCXO ..... ±1.5 ppm

Jitter added to CLKIN

- Without PLL ..... 15 ps_{rms}
- With PLL ..... 2.5 ps_{rms}

Duty cycle distortion of CLKIN without PLL ..... +1%

Duty cycle of PLL ..... 45 to 55%

---

[1] CLKIN fundamental frequency can be any multiple of 1 MHz within the range specified when the PLL is engaged and PXI_CLK10 is locking to it. The frequency must be 10 MHz when replacing PXI_CLK10 without the PLL.

[2] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specification is not implied.

CLKOUT Characteristics

Output frequency

From PXI_CLK10 ..... 10 MHz

From OCXO ..... 10 MHz

From DDS ..... 1 MHz[1] to 80 MHz

Duty cycle ..... 40 to 60%

Output impedance ..... 50 Ω ±5%

Output coupling ..... AC

Amplitude, software configurable to two voltage levels (low and high drive)

Open Load	Sine Wave (10 MHz only)	Square Wave
Low Drive	3.6–5.1 V_{p-p}	4.1–5.4 V_{p-p}
High Drive	5.4–7.6 V_{p-p}	7.1–9.2 V_{p-p}

50 Ω Load	Sine Wave (10 MHz only)	Square Wave
Low Drive	1.8–2.6 V_{p-p}	2.0–2.7 V_{p-p}
High Drive	2.6–3.8 V_{p-p}	3.5–4.6 V_{p-p}

Square wave rise/fall time (10 to 90%)

Low drive ..... 4 ns min, 6 ns max

High drive ..... 4.5 ns min, 7 ns max

Maximum recommended 50 Ω loads[2] .... 8, low or high drive, square or sine

[1] The lower limit is load dependent because of the AC coupling. This limit is less than 1 MHz for high-impedance loads.

[2] With an external 50 Ω splitter. This value does not include cable attenuation or splitter insertion loss.

PFI<0..5>

Input Characteristics

Frequency range ..... DC to 100 MHz

Input impedance ..... 50 Ω ±5% or 1 kΩ ±5%, software-selectable

Input coupling ..... DC

Voltage level ..... 0 to 5 V

Absolute maximum input voltage[1]

- System powered off ..... ±7 V, max
- System powered on ..... –7 to +5.5 V max

Input threshold

- Voltage level ..... 0.3 to 4.3 V, software-selectable
- Voltage resolution ..... 20 mV (8 bits)
- Error ..... ±40 mV

Hysteresis ..... 10 mV

Asynchronous delay, t_{pd}

- PFI <0..5> to PXI_TRIG<0..7> output ..... 16 to 23 ns
- PFI <0..5> to PXI_STAR<0..12> output ..... 11 to 12.5 ns

Synchronized trigger input setup time, t_{setup}[2] ..... 8 ns

Synchronized trigger input hold time, t_{hold}[2] ..... 8 ns

[1] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specifications is not implied.

[2] Relative to PXI_CLK10.

Output Characteristics

Frequency range .....DC to 100 MHz

Output impedance.....50 Ω ±5%

Output coupling .....DC

Voltage level.....1.6 V into 50 Ω;
3.3 V into open circuit

Absolute maximum input voltage[1]

System powered off.....±7 V, max

System powered on.....–7 V to +5.5 V, max

Synchronized trigger clock
to out time, t_{CtoQ}[2] .....10 ns

Output-to-output skew, synchronous.....500 ps

PXI_STAR Trigger Characteristics

PXI_STAR<0..12> to
PXI_STAR<0..12> output skew
at NI 6653 backplane connector .....400 ps[3]

Asynchronous delays, t_{pd}

PXI_STAR<0..12> to
PFI <0..5> output.....7.5 to 13 ns

PXI_STAR<0..12> to
PXI_TRIG<0..7> output.....13 to 19 ns

PXI Trigger Characteristics

Asynchronous delay, t_{pd}

PXI_TRIG<0..7> to
PFI <0..5> output.....11 to 16 ns

---

[1] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specifications is not implied.

[2] Relative to PXI_CLK10.

[3] This specification applies to all synchronous routes to the PXI_Star lines, as well as asynchronous routes from the PFI inputs to the PXI_Star lines.

OCXO Characteristics

Frequency ..... 10 MHz

Warm-up time (to within 20 ppb of operating frequency (one-hour reading), power-off duration <1 hour) ..... 3 minutes

Initial accuracy ..... ±3.2 ppb

Long-term stability[1] ..... ±50 ppb/year

Temperature stability (0 to 55 °C)[2] ..... ±5 ppb, referenced to 25 °C

DDS Characteristics

Frequency range ..... 1 Hz to 80 MHz

Frequency resolution ..... 711 nHz

Frequency accuracy ..... Equivalent to PXI_CLK10 accuracy[3]

Physical

Chassis requirement ..... One 3U CompactPCI or PXI slot (PXI Slot 2 for full functionality)

Front panel connectors ..... SMB male, 50 Ω

Front panel indicators ..... Two tricolor LEDs (green, red, and amber)

Recommended maximum cable length ..... 100 meters

[1] Includes stability of OCXO and supporting circuitry.

[2] Includes temperature stability of OCXO and supporting circuitry.

[3] The DDS frequency inherits the relative frequency of PXI_CLK10. For example, if you route the OCXO to PXI_CLK10, the DDS output inherits the same relative frequency accuracy as the OCXO output.

Power Requirements

+5 V .....900 mA, max

+3.3 V .....1.5 A, max

+12 V .....100 mA, max

–12 V .....100 mA, max

Environmental

Operating temperature .....0 to 55 °C

Storage temperature .....–25 to +85 °C

Humidity .....10 to 95% RH, noncondensing

Maximum altitude.....2,000 meters

Pollution Degree (indoor use only) 2

Safety

The NI PXI-6653 meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 3111-1
- CAN/CSA C22.2 No. 1010.1

Note For UL and other safety certifications, refer to the product label or to `ni.com`.

Electromagnetic Compatibility

Emissions.....EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Immunity .....EN 61326-1:1997 + A1:1998, Table 1

EMC/EMI .....CE, C-Tick, and FCC Part 15 (Class A) Compliant

Note For EMC compliance, you *must* operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE Marking, as follows:

Low-Voltage Directive (safety) 73/23/EEC

Electromagnetic Compatibility
Directive (EMC) 89/336/EEC

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

B

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  - **Assisted Support Options**—Contact NI engineers and other measurement and automation professionals by visiting ni.com/ask. Our online system helps you define your question and connects you to the experts by phone, discussion forum, or email.
- **Training**—Visit ni.com/custed for self-paced tutorials, videos, and interactive CDs. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, NI Alliance Program members can help. To learn more, call your local NI office or visit ni.com/alliance.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electronic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/hardref.nsf.

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Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
μ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}

Symbols

%	percent
±	plus or minus
+	positive of, or plus
–	negative of, or minus
/	per
°	degree
Ω	ohm

A

accumulator	a part where numbers are totaled or stored
ADE	application development environment
asynchronous	a property of an event that occurs at an arbitrary time, without synchronization to a reference clock

B

backplane	an assembly, typically a printed circuit board (PCB), with 96-pin connectors and signal paths that bus the connector pins. PXI systems have two connectors, called the J1 and J2 connectors.
backplane synchronization clock	the clock signal that is used to synchronize the RTSI/PXI triggers or PXI_STAR triggers on an NI 6653
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. An examples of a PC bus is the PCI bus.

C

C	Celsius
CLKIN	CLKIN is a signal connected to the SMB input pin of the same name. CLKIN can serve as PXI_CLK10_IN or be used as a phase lock reference for the OCXO.
CLKOUT	CLKOUT is the signal on the SMB output pin of the same name. Either the OCXO clock or PXI_CLK10 may be routed to CLKOUT.
clock	hardware component that controls timing for reading from or writing to groups
CompactPCI	a Eurocard configuration of the PCI bus for industrial applications

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device that converts a digital number into a corresponding analog voltage or current
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer

DC	direct current
DDS	Direct Digital Synthesis—a method of creating a clock with a programmable frequency

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
ESD	electrostatic discharge

F

frequency	the basic unit of rate, measured in events or oscillations per second using a frequency counter or spectrum analyzer. Frequency is the reciprocal of the period of a signal.
frequency tuning word	a number that specifies the frequency
front panel	the physical front panel of an instrument or other hardware

H

Hz	hertz—the number of scans read or updates written per second

I

in.	inch or inches

J

jitter	the rapid variation of a clock or sampling frequency from an ideal constant frequency

L

LabVIEW	a graphical programming language
LED	Light-Emitting Diode—a semiconductor light source

M

master	the requesting or controlling device in a master/slave configuration.
Measurement & Automation Explorer (MAX)	a controlled centralized configuration environment that allows you to configure all of your National Instruments DAQ, GPIB, IMAQ, IVI, Motion, VISA, and VXI devices

N

NI-DAQ	National Instruments driver software for DAQ hardware

O

oscillator	a device that generates a fixed frequency signal. An oscillator most often generates signals by using oscillating crystals, but may also use tuned networks, lasers, or atomic clock sources. The most important specifications on oscillators are frequency accuracy, frequency stability, and phase noise.
OCXO	oven-controlled crystal oscillator
output impedance	the measured resistance and capacitance between the output terminals of a circuit

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PFI	Programmable Function Interface

PLL	phase-locked loop
precision	the measure of the stability of an instrument and its capability to give the same measurement over and over again for the same input signal
propagation delay	the amount of time required for a signal to pass through a circuit
PXI	a rugged, open system for modular instrumentation based on CompactPCI, with special mechanical, electrical, and software features. The PXIbus standard was originally developed by National Instruments in 1997, and is now managed by the PXIbus Systems Alliance.
PXI star	a special set of trigger lines in the PXI backplane for high-accuracy device synchronization with minimal latencies on each PXI slot

R

RTSI bus	Real-Time System Integration bus—the NI timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise synchronization of functions

S

s	seconds
skew	the actual time difference between two events that would ideally occur simultaneously. Inter-channel skew is an example of the time differences introduced by different characteristics of multiple channels. Skew can occur between channels on one module, or between channels on separate modules (intermodule skew).
slave	a computer or peripheral device controlled by another computer
slot	the place in the computer or chassis in which a card or module can be installed
Slot 2	the second slot in a PXI system which can house a master timing unit
SMB	Sub Miniature Type B—a small coaxial signal connector that features a snap coupling for fast connection
synchronous	a property of an event that is synchronized to a reference clock

T

t_{CtoQ}	clock to output time
t_{hold}	hold time
t_{pd}	propagation delay time
TRIG	trigger signal
trigger	a digital signal that starts or times a hardware event (e.g. starting a data acquisition operation)
t_{setup}	setup time

V

V	volts
VI	virtual instrument

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