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PXIe-6556 Device Specifications

2024-08-26

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PXIe-6556 Specifications

This document provides the specifications for the PXIe-6556.



Hot Surface If the PXIe-6556 has been in use, it may exceed safe handling temperatures and cause burns. Allow the PXIe-6556 to cool before removing it from the chassis.



Note All values were obtained using a 1 m cable (SHC68-C68-D4 recommended). Performance specifications are not guaranteed when using longer cables.

Definitions and Conditions

Specifications are valid for the range 0 °C to 45 °C unless otherwise noted.

Accuracy specifications are valid within ±5 °C of self-calibration unless otherwise noted.

Maximum and ***minimum*** specifications are warranted not to exceed these values within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Typical specifications are unwarranted values that are representative of a majority (3σ) of units within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Characteristic specifications are unwarranted values that are representative of an average unit operating at room temperature.

Nominal specifications are unwarranted values that are relevant to the use of the product and convey the expected performance of the product.

All specifications are Typical unless otherwise noted.

Channels

Data	
Number of channels	24, per-pin parametric measurement unit (PPMU)–enabled
Direction control	Per channel



Note All data channels have pattern memory.

Programmable Function Interface (PFI)	
Number of channels	
PPMU-enabled: 4	PFI 1 PFI 2 PFI 4/DDC CLK OUT PFI 5/STROBE
General: 10	PFI 0 PFI 3 PFI <24..31>
Direction control	Per channel
Clock terminals	

Input	4
Output	2
Number of remote sense channels	28

Note All PPMU-enabled channels have remote sense capability.

Related reference:

- CLK IN
- CLK OUT

Digital Generation Channels

Note These features are controlled independently per channel.

Channels	DIO <0..23> PFI 1 PFI 2 PFI 4 PFI 5
Generation signal type	Single-ended, ground-referenced
Programmable generation voltage levels	Drive voltage high level (V_{OH})

	Drive voltage low level (V_{OL}) Drive tristate (V_{TT})
Generation voltage	
Ranges	Software-selectable: -2 V to 6 V (default) or -1 V to 7 V
Resolution	122 µV
DC generation voltage accuracy[1]	
Within ±5 °C of self-calibration	±11 mV
Within ±15 °C of self-calibration	±16 mV
Generation voltage swing[2]	400 mV to 8.0 V
Output impedance	50 Ω, nominal
Maximum allowed DC drive strength per channel	±35 mA, nominal

Caution Do not exceed the maximum power limit of the device.

Data channel tristate control	Software-selectable, hardware-timed: per channel, per cycle
Channel power-on state	Drivers disabled, high impedance

Output protection	
Range	-3 V to 8.5 V
Duration	Indefinite if maximum allowed DC drive strength of ±35 mA per channel is observed

Digital Acquisition Channels

Note These features are controlled independently per channel.

Channels	DIO <0..23> PFI 1 PFI 2 PFI 4 PFI 5
Acquisition signal type	Single-ended, ground-referenced
Programmable acquisition voltages	Compare voltage high threshold (V_{IH}) Compare voltage low threshold (V_{IL}) Termination voltage (V_{TT})
Acquisition voltage threshold range	-2 V to 7 V
Acquisition and termination voltage resolution	122 µV

Termination voltage ranges	-2 V to 6 V (default) -1 V to 7 V	
DC acquisition voltage accuracy[3]		
Within ±5 °C of self-calibration		V_{IL} = ±25 mV V_{IH} = ±25 mV V_{TT} = ±11 mV
Within ±15 °C of self-calibration		V_{IL} = ±28 mV V_{IH} = ±28 mV V_{TT} = ±16 mV
Minimum detectable voltage swing	50 mV	
Input impedance	Software-selectable: High-impedance or 50 Ω terminated into V_{TT}	
High impedance leakage	<5 nA, characteristic	
Input protection		
Range	-3 V to 8.5 V	
Duration	Indefinite if maximum allowed DC drive strength of ±35 mA per channel is observed	

Active Load Channels

Note These features are controlled independently per channel.

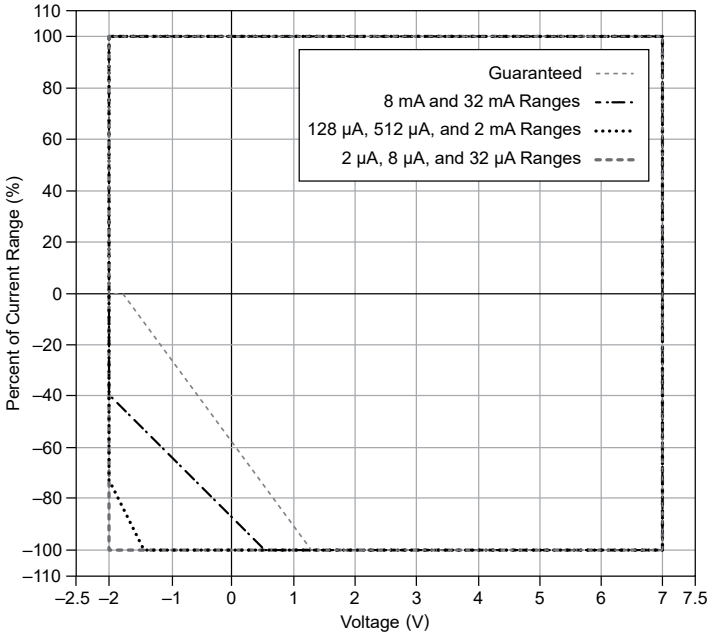
Channels	Data <0..23> PFI 1 PFI 2 PFI 4 PFI 5
Programmable levels	Commutating voltage (V_{TT}) Current source (I_{SOURCE}) Current sink (I_{SINK})
Load[4]	
Range	1.5 mA to 24 mA
Resolution	488 nA
Accuracy, ±15 °C of self-calibration	±1 mA

PPMU Channels

Note These features are controlled independently per channel.

Channels	DIO <0..23> PFI 1 PFI 2 PFI 4 PFI 5
PPMU signal type[5]	Single-ended, ground-referenced
Programmable levels[6]	Force voltage (F_V) Force current (F_I) Voltage clamp high (V_{CHI}) Voltage clamp low (V_{CLO})

Figure 1. Characteristic Quadrant Behavior by Current Range



Force voltage	
Ranges	-2 V to 6 V (default) -1 V to 7 V
Resolution	122 µV
Accuracy[7]	
Within ±5 °C of self-calibration	±11 mV
Within ±15 °C of self-calibration	±16 mV

Table 1. Force Voltage Settling Time

Current Range	Settling Time[8]
2 µA	150 µs
8 µA	75 µs
32 µA	40 µs
128 µA	
512 µA	
2 mA	45 µs
8 mA	55 µs
32 mA	60 µs

Table 2. Load Capacitance

Current Range	Load Capacitance[9]
2 µA	1 nF
8 µA	

Current Range	Load Capacitance[9]
32 µA	
128 µA	
512 µA	4.7 nF
2 mA	10 nF
8 mA	47 nF
32 mA	100 nF

Characteristic Step Response

Figure 2. Characteristic Step Response into a Capacitive Load in the 2 µA Range

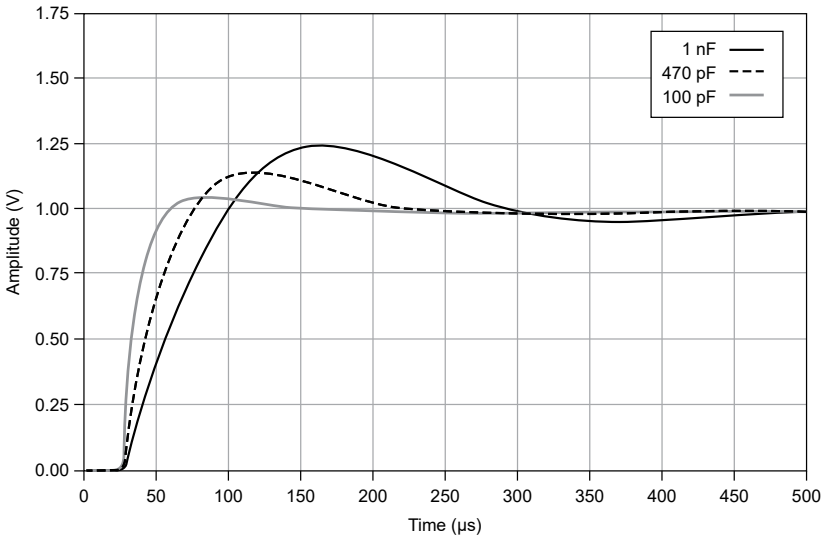


Figure 3. Characteristic Step Response into a Capacitive Load in the 512 µA Range

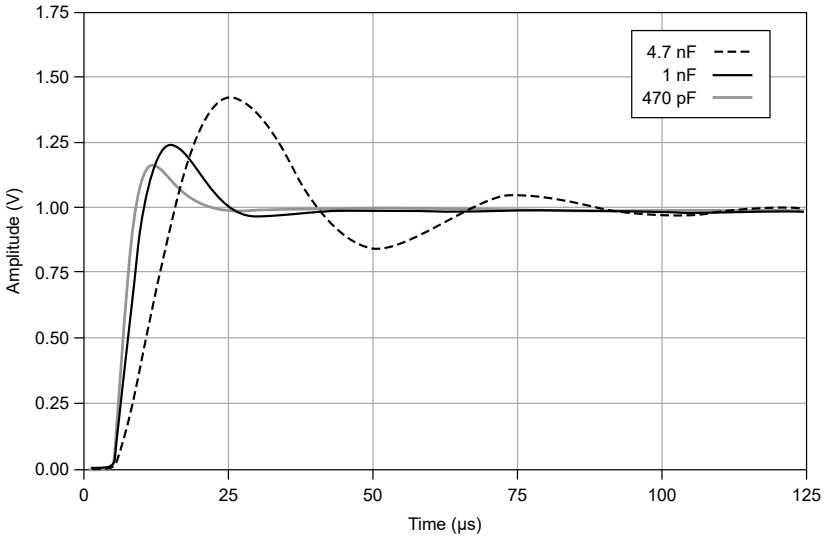


Figure 4. Characteristic Step Response into a Capacitive Load in the 32 mA Range

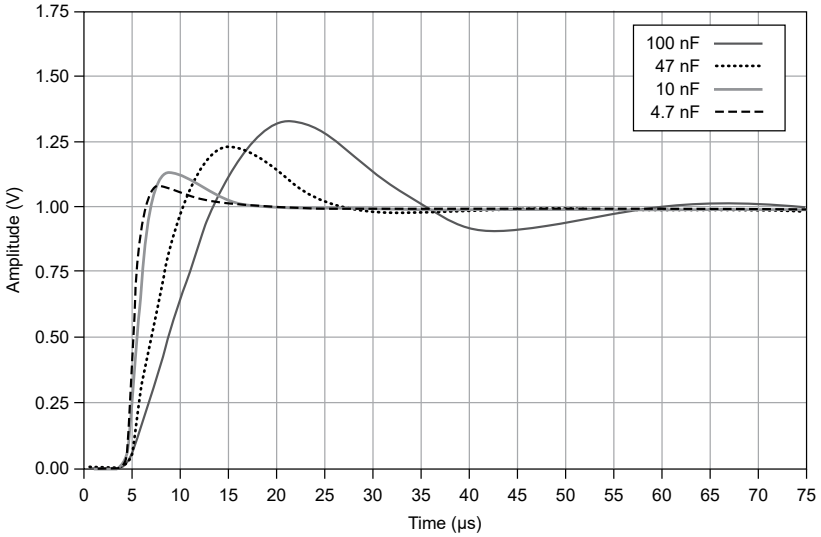


Table 3. Force Current Resolution, Nominal

Current Range	Resolution
±2 µA	60 pA
±8 µA	240 pA
±32 µA	980 pA
±128 µA	3.9 nA
±512 µA	15.6 nA
±2 mA	60 nA
±8 mA	240 nA
±32 mA	980 nA

Force current accuracy	
Within ±5 °C of self-calibration	1% of range, maximum
Within ±15 °C of self-calibration	1.3% of range, maximum
Force current voltage clamps, maximum	
Current range[10]	

V_{CLO}	-2 V to 6 V, maximum
V_{CHI}	-1 V to 7 V, maximum

Resolution	122 µV, maximum
Accuracy within ±15 °C of self-calibration	±100 mV, maximum

Note Voltage clamps begin to conduct within 700 mV of the programmable voltage level.

Aperture time	
Range	4 µs to 65 ms
Resolution	4 µs

Measure voltage[11]	
Range	-2 V to 7 V
Resolution	228 µV
Accuracy within ±15 °C of self-calibration	±3 mV

Figure 5. Typical Voltage Measurement Noise for Given Aperture Times

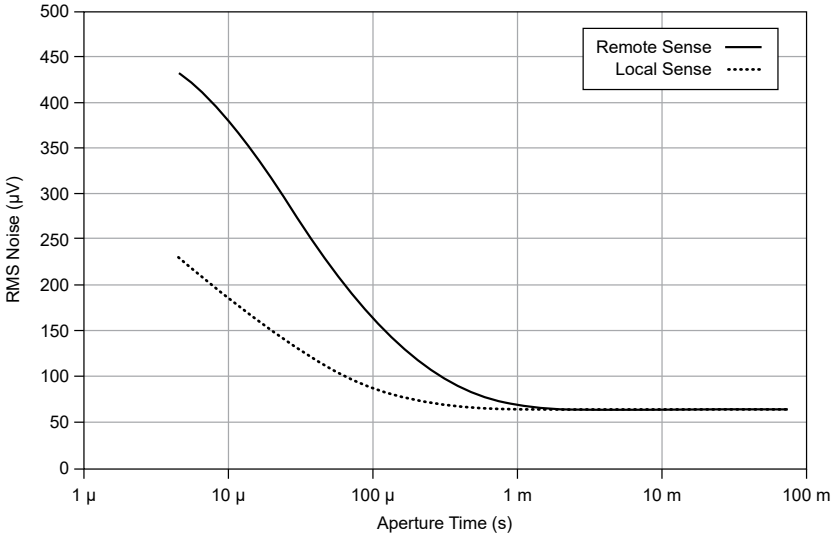
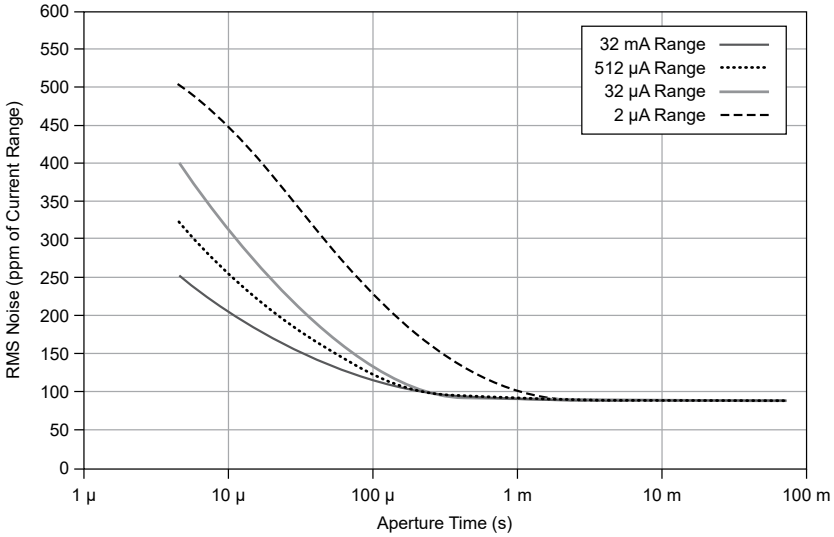


Table 4. Measure Current Resolution, Nominal

Current Range	Resolution
±2 µA	460 pA
±8 µA	1.8 nA
±32 µA	7.3 nA
±128 µA	30 nA
±512 µA	120 nA
±2 mA	460 nA
±8 mA	1.8 µA
±32 mA	7.3 µA

Measure current accuracy[12]	
Within ±5 °C of self-calibration	1% of range
Within ±15 °C of self-calibration	1.3% of range

Figure 6. Typical Current Measurement Noise for Given Aperture Times



Note I_{RMS} Noise is represented by the following equation: I_{rms} Noise = (rms Noise × Current Range)/10^6. For example, 100 ppm on a 32 mA range yields a noise of 3.2 μA_{rms}, which is calculated as 3.2 μA_{rms} = (100 ppm × 32 mA)/10^6.

I/O switch resistance	5.5 Ω, nominal
Remote feedback impedance	100 kΩ, nominal
Output protection	
Range	-3 V to 8.5 V
Duration	Indefinite if maximum allowed DC drive strength of ±35 mA per channel is observed

General PFI Channels

Channels	PFI 0

	PFI 3 PFI <24..31>
Circuit type	
PFI 0 and PFI 3	High-speed I/O circuits
PFI <24..31>	5 V compatible I/O circuits
Generation voltage level	
Low voltage levels, characteristic	0 V, nominal
High voltage levels, characteristic	3.3 V, nominal
Drive strength	
PFI 0 and PFI 3	±33 mA
PFI <24..31>	±85 mA
Output impedance	50 Ω, nominal
Output protection	
Range	0 V to 5 V
Duration	Indefinite
Acquisition voltage level	

Low thresholds	0.8 V, nominal
High thresholds	2 V, nominal
Input protection	
PFI 0 and PFI 3	-1 V to 5 V, maximum
PFI <24..31>	-1 V to 6.5 V, maximum

EXTERNAL FORCE and EXTERNAL SENSE Channels

Note These specifications are valid for the EXTERNAL FORCE and EXTERNAL SENSE channels on the AUX I/O connector and on the REMOTE SENSE connector. The AUX I/O connector is available only on PXIe-6556 devices.

EXTERNAL FORCE	
Direction	Input
Analog bandwidth	3 MHz, characteristic with a single channel connected
Maximum current	±32 mA
Range	-2 V to 7 V
EXTERNAL SENSE	
Direction	Output

Analog bandwidth	30 kHz, characteristic with a single channel connected
Range	-2 V to 7 V
Input protection	
Range	-3 V to 8.5 V
Duration	Indefinite if maximum allowed DC drive strength of ±35 mA per channel is observed

CAL Channels

These specifications are valid for the CAL channel on the AUX I/O connector and on the REMOTE SENSE connector. The AUX I/O connector is available only on PXIe-6556 devices.

Direction	Output[13]
Voltage level	5 V, nominal
Drive strength	1 mA [14]

Timing

Sample Clock

Sources	1. On Board clock (internal)

	2. CLK IN (SMA jack connector) 3. PXIe_DStarA (PXI Express backplane) 4. STROBE (acquisition only; Digital Data & Control [DDC] connector)
On Board clock frequency[15]	
Resolution	<0.1 Hz
Accuracy[16]	±150 ppm, nominal
Frequency ranges	
On Board clock	800 Hz to 200 MHz
CLK IN	20 kHz to 200 MHz
PXIe_DStarA	800 Hz to 200 MHz
STROBE	800 Hz to 200 MHz
Relative delay adjustment	
Range	±5 ns
Resolution	3.125 ps

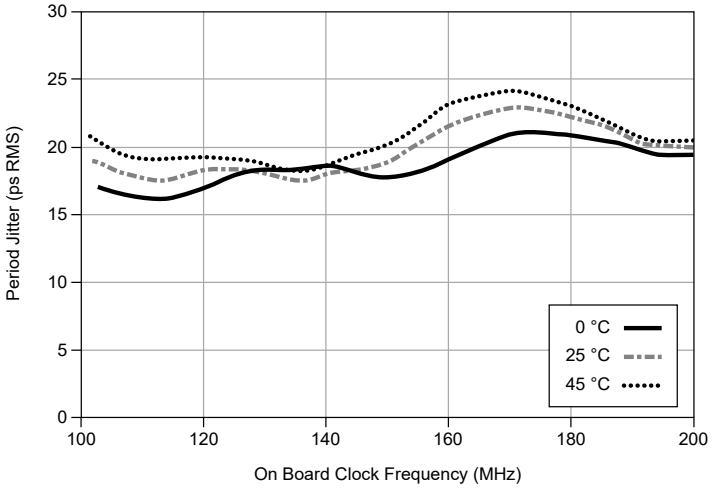
Tip To align multiple devices, apply a delay or phase adjustment to the On Board clock.

Exported Sample clock destinations	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMA jack connector)

Note Internal Sample clocks with sources other than STROBE can be exported.

Exported Sample clock	
Offset range (t_{CO})	Software-programmable: 0 ns to 2.4 ns
Offset resolution (t_{CO})	Software-programmable: 13 ps
Offset accuracy (t_{CO})	Software-programmable: ±200 ps
Duty cycle (DDC CLK OUT)[17]	42%, minimum 55%, maximum
Period jitter	24 ps_{rms}, characteristic (using On Board clock)

Figure 7. Characteristic Period Jitter (RMS) versus Frequency



Related reference:

- CLK IN
- PXIe_DStarA
- PFI 5 as STROBE

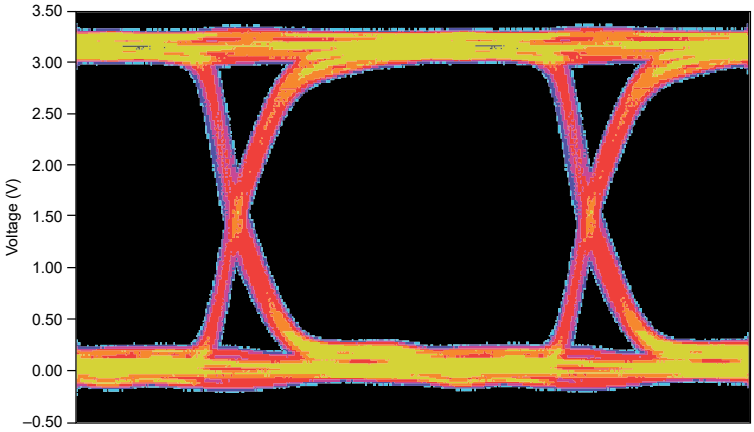
Generation Timing

Channels	Data DDC CLK OUT PFI <0..3>
Maximum data rate per channel	200 Mbps
Maximum data channel toggle rate[18]	
3.3 V swing	100 MHz
5 V swing	50 MHz

The following figure shows an eye diagram of a 200 Mbps pseudorandom bit sequence

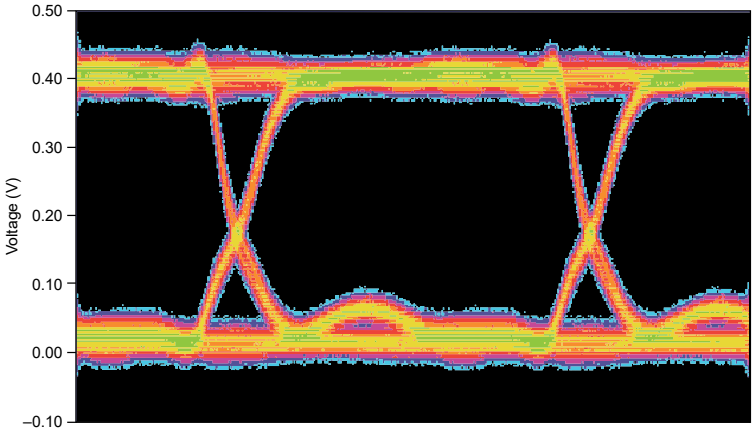
(PRBS) waveform at 3.3 V. This waveform was captured on a characteristic DIO channel at room temperature into high-impedance.

Figure 8. Characteristic Eye Diagram at 3.3 V



The following figure shows an eye diagram of a 200 Mbps PRBS waveform at 0.4 V. This waveform was captured on a characteristic DIO channel at room temperature into high-impedance.

Figure 9. Characteristic Eye Diagram at 0.4 V



Data channel-to-channel skew	600 ps, maximum 300 ps, characteristic

Note There will be additional skew from crosstalk, acquisition threshold, and other transmission line effects in your system. You may see up to 150 ps

of additional skew from differences between channels in the average rate of pattern transitions.

Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge
Generation data	
Frequency	
On Board clock	All supported frequencies
External clock	Frequencies ≥20 MHz
Delay range	-1 to 2 Sample clock cycles, expressed as a fraction of the Sample clock period
Deskew range	-2 to 3 Sample clock cycles, expressed as a time in seconds
Delay and deskew resolution	30 ps, nominal

Note The sum of data delay and data deskew may not exceed -2 to 3 Sample clock cycles.

Generation Provided Setup and Hold Times

Provided setup and hold times assume the data position is set to Sample clock rising edge and the noninverted Sample clock is exported to the DDC connector with t_{CO}

programmed using exported Sample clock offset.

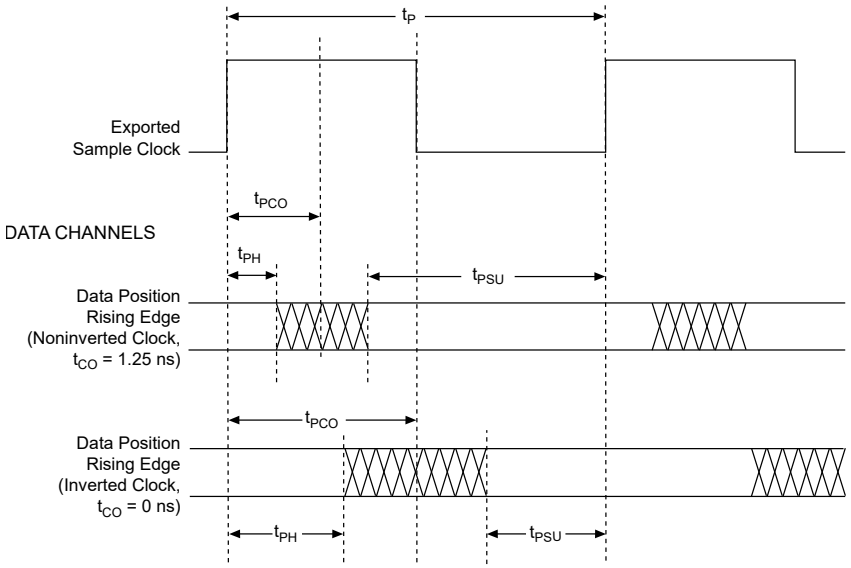
Provided setup time (t_{PSU})	t_p - t_{CO} - 850 ps, characteristic
Provided hold time (t_{PH})	t_{CO} - 700 ps, characteristic

Note Exported Sample clock Offset (t_{CO}) is software programmable.

Compare the setup and hold times from the datasheet of your device under test (DUT) to the provided setup and hold time values above. The provided setup and hold times must be greater than the setup and hold times required for the DUT. If you require more setup time, configure your exported Sample clock mode to Inverted and/or delay your clock or data relative to the Sample clock.

The following figure illustrates the relationship between the exported Sample clock mode and the provided setup and hold times.

Figure 10. Generation Provided Setup and Hold Times Timing Diagram



$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{PH} = Provided Hold Time

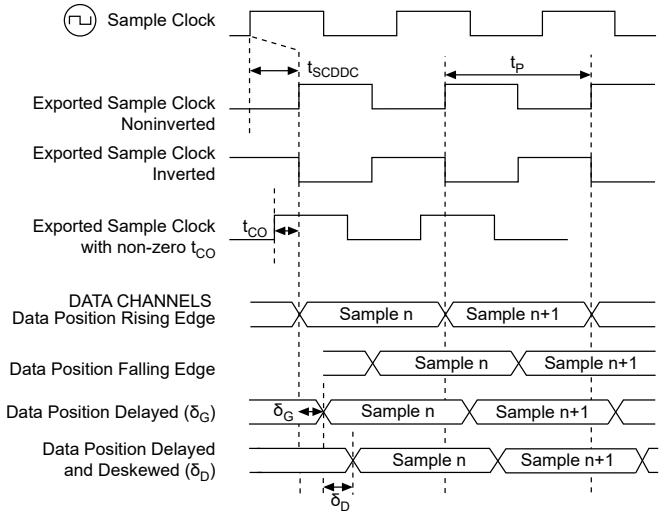
t_{PSU} = Provided Setup Time

t_{PCO} = Time from Rising Clock Edge to Data Transition (Provided Clock to Out Time)

t_{CO} = Exported Sample Clock Offset

Note Provided setup and hold times account for maximum channel-to-channel skew and jitter.

Figure 11. Generation Timing Diagram



t_{SCDDC} : Time Delay from Sample Clock (Internal) to DDC Connector

$-1 \le \delta_G \le 2$: Pattern Generation Channel Data Delay (Fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{CO} = Exported Sample Clock Offset

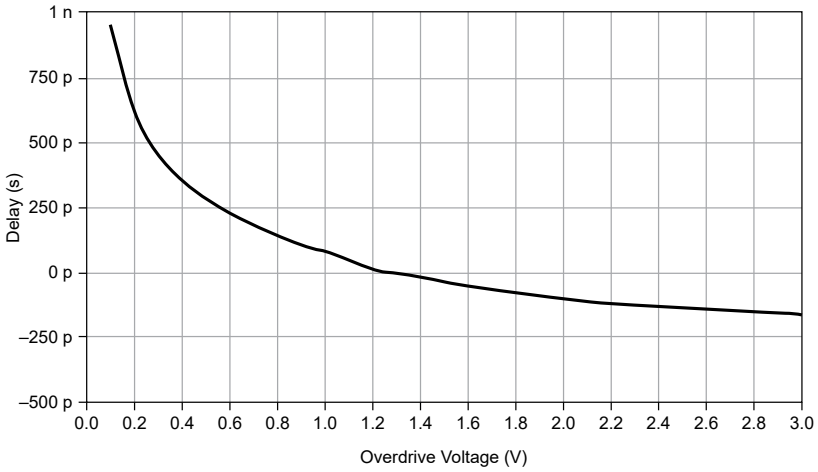
δ_D = Pattern Generation Channel Deskew (Time)

Acquisition Timing

Channels	Data STROBE PFI <0..3>
Maximum data rate per channel	200 Mbps
Channel-to-channel skew	600 ps, maximum 300 ps, characteristic

Note There will be additional skew from crosstalk, acquisition threshold, overdrive, dispersion, and transmission line effects. You may see up to 175 ps of additional skew from differences between channels in the average rate of pattern transitions.

Figure 12. Typical Overdrive Dispersion Adjustment



Note Timing calibration executes with 1.25 V of overdrive.

Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge
Acquisition data	
Delay and deskew frequency	
On Board clock	All supported frequencies
External clock	Frequencies ≥20 MHz
Delay range	-1 to 2 Sample clock cycles, expressed as a fraction of the Sample clock period
Deskew range	-2 to 3 Sample clock cycles, expressed as a time in seconds
Delay and deskew resolution	30 ps

Note The sum of data delay and data deskew may not exceed -2 to 3 Sample clock cycles.

Setup and Hold Times to STROBE

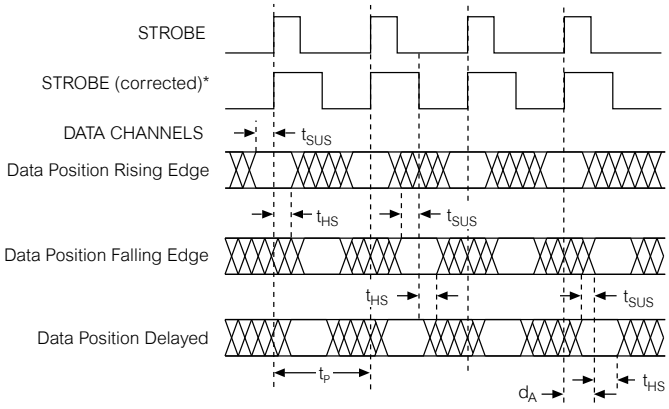
Setup time to STROBE (t_{SUS})	
f <20 MHz	2.2 ns

f ≥20 MHz	1.86 ns
Hold time to STROBE (t_{HS})	
f <20 MHz	3.47 ns
f ≥20 MHz	1.49 ns

Note Setup and hold times include maximum data channel-to-channel skew but do not include system crosstalk. 1.65 V overdrive on all channels. Overall performance may vary with system crosstalk performance. Values are specified within ±15 °C of self-calibration.

The following diagram illustrates the relationship between the exported Sample clock mode and the setup and hold times to STROBE.

Figure 13. Acquisition Timing Diagram Using STROBE as the Sample Clock



t_{SUS} = Setup Time to STROBE

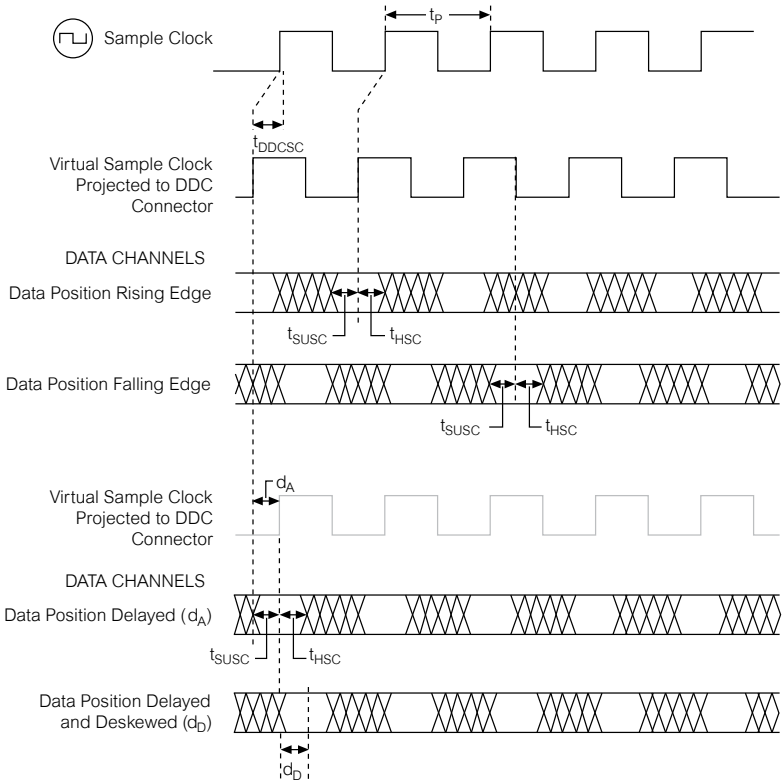
t_{HS} = Hold Time from STROBE

$-1 \le d_A \le 2$: Acquisition Data Delay (fraction of $\frac{1}{f}$)

$t_P = \frac{1}{f}$ = Sample Clock Period

*Note: When using an external Sample clock greater than 20 MHz, the duty cycle is corrected to 50%.

Figure 14. Acquisition Timing Diagram with Sample Clock Sources Other than STROBE



t_{DDCSC} : Time Delay from DDC Connector or to Internal Sample Clock

$-1 \le \delta_A \le 2$: Pattern Acquisition Channel Data Delay (Fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Setup Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

δ_D = Pattern Acquisition Channel Deskew (Time)

CLK IN

Connector	SMA jack
Direction	Input
Destinations	1. Reference clock (for the phase-locked loop [PLL]) 2. Sample clock
Input	

Coupling	AC
Protection	±10 VDC, nominal
Impedance	Software-selectable: 50 Ω (default) or 1 kΩ, nominal
Minimum detectable pulse width	2 ns
Clock requirements	Free-running (continuous) clock
Clock square wave ranges[19]	
Voltage	300 mV_{pk-pk} to 5.5 V_{pk-pk}, nominal
Frequency	20 kHz to 200 MHz, nominal
Duty cycle	40% to 60%, nominal
Clock sine wave ranges	
0 dBm	
Voltage	630 mV_{pk-pk} to 5.5 V_{pk-pk}
Frequency	10 MHz to 200 MHz
6 dBm	
Voltage	1.265 V_{pk-pk} to 5.5 V_{pk-pk}

Frequency	5 MHz to 200 MHz
12 dBm	
Voltage	2.53 V_{pk-pk} to 5.5 V_{pk-pk}
Frequency	2.5 MHz to 200 MHz

PFI 5 as STROBE

Connector	DDC
Direction	Input
Destination	Sample clock (acquisition only)
Frequency range	800 Hz to 200 MHz
Duty cycle range[20]	
f <20 MHz	25% to 75%
f ≥20 MHz	40% to 60%

Note STROBE duty cycle is corrected to 50% at f ≥20 MHz.

Minimum detectable pulse width[20]	2 ns
Clock requirements	Free-running (continuous) clock

Related reference:

- Digital Acquisition Channels

PXIe_DStarA

Connector	PXI Express backplane
Direction	Input
Destinations	1. Reference clock (for the PLL) 2. Sample clock
Frequency range	800 Hz to 200 MHz
Duty cycle range	40% to 60%
Clock requirements	Free-running (continuous) clock

CLK OUT

Connector	SMA jack

Direction	Output
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)
Generation voltage level[21]	
Low voltage levels, characteristic	0 V, nominal
High voltage levels, characteristic	3.3 V, nominal
Drive strength	±33 mA
Output impedance	50 Ω, nominal
Output protection	
Range	0 V and 5 V
Duration	Indefinite

PFI 4 as DDC CLK OUT

Connector	DDC
Direction	Output

Source	Sample clock (generation only)

Note STROBE and acquisition Sample clock cannot be routed to DDC CLK OUT.

Related reference:

- Digital Generation Channels

Reference Clock (PLL)

Sources[22]	1. PXI_CLK100 (PXI Express backplane) 2. CLK IN (SMA jack connector) 3. PXIe_DStarA (PXI Express backplane) 4. None (internal oscillator locked to an internal reference)
Frequency	
Range	5 MHz to 100 MHz (integer multiples of 1 MHz)
Accuracy	<5,000 ppm (required accuracy of the external Reference clock source)
Lock time	≤25 ms, not including software latency
Duty cycle range	40% to 60%
Destination	CLK OUT (SMA jack connector)

Waveform

Memory and Scripting

Memory architecture	The PXIe-6556 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples available for waveform storage are flexible and user defined.
Onboard memory size[23]	
8 Mbit/channel	
Acquisition	8 Mbit/channel (32 MBytes total)
Generation	8 Mbit/channel (32 MBytes total)
64 Mbit/channel	
Acquisition	64 Mbit/channel (256 MBytes total)
Generation	64 Mbit/channel (256 MBytes total)
Generation	
Single-waveform mode	Generates a single waveform once, n times, or continuously
Scripted mode[24]	Generates a simple or complex sequence of waveforms
Finite repeat count	1 to 16,777,216
Waveform quantum	

Data width = 4	1 sample
Data width = 2	2 samples
Waveform block size (in physical memory)[25]	
Data width = 4	32 samples
Data width = 2	64 samples

Table 5. Generation Minimum Waveform Size, Samples (S)[26]

Configuration	Sample Rate	
	200 MHz	**100 MHz**
Single waveform	1 S	1 S
Continuous waveform	128 S	64 S
Stepped sequence	128 S	64 S
Burst sequence	1,056 S	512 S

Acquisition	
Minimum record size[27]	1 sample
Record quantum	1 sample
Total records[28]	2,147,483,647

Total pre-Reference trigger samples	0 up to full record
Total post-Reference trigger samples	0 up to full record
Hardware compare	
Error FIFO depth	4,094
Number of unique enable states	255
Maximum speed	200 MHz

Triggers

Trigger Types	Sessions	Edge Detection	Level Detection
1. Start	Acquisition and generation	Rising or falling	—
2. Pause	Acquisition and generation	—	High or low
3. Script <0..3>	Generation	Rising or falling	High or low
4. Reference	Acquisition	Rising or falling	—
5. Advance	Acquisition	Rising or falling	—
6. Stop	Generation	Rising or falling	—

Sources	1. PFI 0 (SMA jack connector) 2. PFI <1..3> (DDC connector) 3. PFI <24..31> (DDC connector)

	4. PXI_TRIG <0..7> (PXI Express backplane) 5. Pattern match (acquisition sessions only) 6. Software (user function call) 7. Disabled (do not wait for a trigger)
Destinations	1. PFI 0 (SMA jack connector) 2. PFI <1..3> (DDC connector) 3. PFI <24..31> (DDC connector) 4. PXI_TRIG <0..6> (PXI Express backplane)
Minimum required trigger pulse width[29]	15 ns

Note Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported.

Trigger rearm time[30]	
Start to Reference trigger	150 S
Start to Advance trigger	220 S
Advance to Advance trigger	220 S
Reference to Reference trigger	220 S
Delay from Pause trigger to Pause state and Stop trigger to Done state	

Generation sessions	55 Sample clock periods + 300 ns, maximum
Acquisition sessions	Synchronous with the data

Note Use the Data Active event during generation to determine on a sample by sample basis when the device enters the Pause or Done states.

Delay from Start trigger or Script triggers to digital data output	6 Sample clock periods + 600 ns, maximum

Events

Event Types	Sessions
1. Marker <0..2>	Generation
2. Data Active	Generation
3. Ready for Start	Acquisition and generation
4. Ready for Advance	Acquisition
5. End of Record	Acquisition

Destinations[31]	1. PFI 0 (SMA jack connector) 2. PFI <1..3> (DDC connector) 3. PFI <24..31> (DDC connector) 4. PXI_TRIG <0..6> (PXI Express backplane)
Marker time resolution (placement)	Markers can be placed at any sample

Calibration

Warm-up time	30 minutes from driver loaded
External calibration interval	1 year

Software

Driver Software

Driver support for this device was first available in NI-HSDIO 1.8.1.

NI-HSDIO is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-6556. NI-HSDIO provides application programming interfaces for many development environments.

Application Software

NI-HSDIO provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

NI Measurement Automation Explorer

NI Measurement Automation Explorer (MAX) provides interactive configuration and test tools for the PXIe-6556. MAX is included on the NI-HSDIO media.

Power

Usage Profile[32]	Current Draw, by Voltage		Total Power
	3.3 V	12 V	
3.3 V swing at 200 Mbps	4.1 A	4.5 A	67.5 W
5.0 V swing at 100 Mbps	4.0 A	4.3 A	64.8 W
8.0 V swing at 50 Mbps	3.8 A	4.3 A	64.1 W
3.3 V swing at 100 Mbps with active load set to 24 mA	4.5 A	4.7 A	71.5 W
Device maximums[33]	5.7 A	5.2 A	76 W

Physical

Dimensions	Dual 3U CompactPCI Express slot, PXI Express compatible 21.6 cm × 2.0 cm × 13.0 cm
Weight	793 g (28 oz)

I/O Panel Connectors

Signal	Connector Type	Description
CLK IN	SMA jack	External Sample clock, external Reference clock
PFI 0		Events, triggers
CLK OUT		External Sample clock,

Signal	Connector Type	Description
		exported Reference clock
AUX I/O	Combicon	External force, external sense, and analog calibration
REMOTE SENSE	68-pin VHDCI	PPMU remote sensing channels, external force, external sense, analog calibration
Digital Data & Control (DDC)		Digital data channels, PPMU channels, exported Sample clock, STROBE, events, triggers

Environment

Note To ensure that the PXIe-6556 cools effectively, follow the guidelines in the ***Maintain Forced Air Cooling Note to Users*** included with the PXIe-6556 or available at ni.com/manuals. The PXIe-6556 is intended for indoor use only.

Operating temperature	0 °C to 45 °C in all NI PXI Express and hybrid NI PXI Express chassis (meets IEC 60068-2-2)
Operating relative humidity	10 to 90% relative humidity, noncondensing (meets IEC 60068-2-56)
Storage temperature	-20 °C to 70 °C (meets IEC 60068-2-2)
Storage relative humidity	5 to 95% relative humidity, noncondensing (meets IEC 60068-2-56)

Operating shock	30 g, half-sine, 11 ms pulse (meets IEC 60068-2-27; test profile developed in accordance with MIL-PRF-28800F)
Operating vibration	5 Hz to 500 Hz, 0.3 g_{rms} (meets IEC 60068-2-64)
Storage shock	50 g, half-sine, 11 ms pulse (meets IEC 60068-2-27; test profile developed in accordance with MIL-PRF-28800F)
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (meets IEC 60068-2-64; test profile exceeds requirements of MIL-PRF-28800F, Class B)
Altitude	0 to 2,000 m above sea level (at 25 °C ambient temperature)
Pollution degree	2

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Notice Refer to the ***Read Me First: Safety and Electromagnetic Compatibility*** document for important safety and electromagnetic compatibility information. To obtain a copy of this document online, visit ni.com/manuals and search for the document title.

Notice To ensure the specified EMC performance, operate this product only with shielded cables and accessories. Do not use unshielded cables or accessories unless they are installed in a shielded enclosure with properly designed and shielded input/output ports and connected to the product

using a shielded cable. If unshielded cables or accessories are not properly installed and shielded, the EMC specifications for the product are no longer guaranteed.

Notice To ensure the specified EMC performance, the length of all I/O cables must be no longer than 3 m (10 ft).

Notice To ensure the specified EMC performance, you must install PXI EMC Filler Panels, National Instruments part number 778700-01, in all open chassis slots.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

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