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SCXI-1140
User Manual

An Eight-Channel Simultaneously Sampling Differential Amplifier Module for Signal Conditioning

September 1994 Edition

Part Number 320410B-01

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About This Manual

This manual describes the electrical and mechanical aspects of the SCXI-1140 and contains information concerning its operation and programming. The SCXI-1140 is a member of the National Instruments Signal Conditioning eXtensions for Instrumentation (SCXI) Series modules for National Instruments data acquisition plug-in boards. This module is designed for low-cost signal conditioning of a wide variety of high-level and low-level DC and AC voltage sources.

This manual also describes the installation, basic programming considerations, and theory of operation for the SCXI-1140.

Organization of This Manual

The *SCXI-1140 User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the SCXI-1140; lists the contents of your SCXI-1140 kit; describes the optional software, optional equipment, and custom cables; and explains how to unpack the SCXI-1140 kit.
- Chapter 2, *Configuration and Installation*, describes the SCXI-1140 jumper configurations, DIP switch settings, installation of the SCXI-1140 into the SCXI chassis, signal connections to the SCXI-1140, and cable wiring.
- Chapter 3, *Theory of Operation*, contains a functional overview of the SCXI-1140 module and explains the operation of each functional unit making up the SCXI-1140.
- Chapter 4, *Register Descriptions*, describes in detail the SCXI-1140 Configuration Register, the Module ID Register, and the Slot 0 registers.
- Chapter 5, *Programming*, contains a functional programming description of the SCXI-1140 and Slot 0.
- Chapter 6, *Calibration Procedures*, discusses the calibration procedures for the SCXI-1140 module.
- Appendix A, *Specifications*, lists the specifications for the SCXI-1140.
- Appendix B, *Rear Signal Connector*, describes the pinout and signal names for the SCXI-1140 50-pin rear signal connector, including a description of each connection.
- Appendix C, *SCXIbus Connector*, describes the pinout and signal names for the SCXI-1140 96-pin SCXIbus connector, including a description of each signal.
- Appendix D, *SCXI-1140 Front Connector*, describes the pinout and signal names for the SCXI-1140 front connector, including a description of each connection.
- Appendix E, *SCXI-1140 Cabling*, describes the usage and installation of the hardware accessories that you can use with the SCXI-1140.

- Appendix F, *Revision A and B Photograph and Parts Locator Diagram*, contains a photograph of the Revision A and B SCXI-1140 signal conditioning module and the SCXI-1140 parts locator diagram.
- Appendix G, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* contains an alphabetical list of key terms and topics used in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual:

DIO board	DIO board refers to the National Instruments AT-DIO-32F, MC-DIO-24, MC-DIO-32F, NB-DIO-24, NB-DIO-96, NB-DIO-32F, PC-DIO 24, and PC-DIO-96 digital I/O data acquisition boards unless otherwise noted.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
Lab board	Lab board refers to the National Instruments Lab-LC, Lab-NB, Lab-PC, and Lab-PC+ boards unless otherwise noted.
MC	MC refers to the Micro Channel series computers.
MIO board	MIO board refers to the National Instruments AT-MIO-16, AT-MIO-16D, AT-MIO-16F-5, AT-MIO-16X, AT-MIO-64F-5, MC-MIO-16, NB-MIO-16, and NB-MIO-16X multichannel I/O data acquisition boards unless otherwise noted.
`monospace`	Lowercase text in this font denotes text or characters that are to be literally input from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, variables, filenames, and extensions, and for statements and comments taken from program code.
NB	NB refers to the NuBus series computers.
PC	PC refers to the IBM PC/XT/AT and compatible computers.
SCXIbus	SCXIbus refers to the backplane in the chassis. A signal on the backplane is referred to as the SCXIbus <signal name> line (or signal). The SCXIbus descriptor may be omitted when the meaning is clear. Descriptions of all SCXIbus signals are given in Appendix C, *SCXIbus Connector*.
Slot 0	Slot 0 refers to the power supply and control circuitry in the SCXI chassis.

Abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms are listed in the *Glossary*.

Related Documentation

The following documents contain information that you may find helpful as you read this manual:

- *AT-MIO-16 User Manual* (part number 320476-01)
- *AT-MIO-16D User Manual* (part number 320489-01)
- *AT-MIO-16F-5 User Manual* (part number 320266-01)
- *AT-MIO-16X User Manual* (part number 320488-01)
- *AT-MIO-64F-5 User Manual* (part number 320487-01)
- *Lab-LC User Manual* (part number 320380-01)
- *Lab-NB User Manual* (part number 320174-01)
- *Lab-PC User Manual* (part number 320205-01)
- *Lab-PC+ User Manual* (part number 320502-01)
- *MC-MIO-16 User Manual*, Revisions A to C (part number 320130-01)
- *MC-MIO-16 User Manual*, Revision D (part number 320560-01)
- *NB-MIO-16 User Manual* (part number 320295-01)
- *NB-MIO-16X User Manual* (part number 320157-01)
- *PC-LPM-16 User Manual* (part number 320287-01)
- *SCXI-1000/1001 User Manual* (part number 320423-01)

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix G, *Customer Communication*, at the end of this manual.

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Chapter 1
Introduction

This chapter describes the SCXI-1140; lists the contents of your SCXI-1140 kit; describes the optional software, optional equipment, and custom cables; and explains how to unpack the SCXI-1140 kit.

The SCXI-1140 is a class I module that operates as an eight-channel simultaneously sampling differential-input gain block. The SCXI-1140 is an SCXIbus module for signal conditioning of high-level and low-level AC and DC signal sources. The SCXI-1140 operates with full functionality with the National Instruments MIO-16 boards. You can use the Lab-NB, the Lab-PC, the Lab-PC+, the Lab-LC, and the PC-LPM-16 boards with the SCXI-1140, but they cannot scan the module; these boards can only perform single-channel reads. You can control the SCXI-1140 with either the data acquisition board or the SCXIbus Slot 0 controller. Each SCXI-1140 module can multiplex its channels into a single data acquisition board channel, although separate outputs are available as well. You can multiplex several SCXI-1140s into a single channel, thus greatly increasing the number of analog input signals that can be digitized.

An additional shielded terminal block has screw terminals for easy signal attachment to the SCXI-1140. In addition to the analog input signal terminals, there is a terminal for a digital input signal that you can use to place the module into Hold mode and thus initiate a data acquisition sequence.

You can use the SCXI-1140 in a wide range of applications ranging from thermocouple and low-level DC measurement to phase measurement. With the SCXI-1140, the SCXI chassis can serve as a fast-scanning signal conditioner for laboratory testing, production testing, and industrial process monitoring.

A 50-pin male ribbon connector at the rear of the module connects the module to the MIO-16 boards. The Lab boards and the PC-LPM-16 require special adapters. At the front, a 96-pin DIN C connector connects the analog inputs to an optional terminal block. A mating DIN C connector and shell are also available.

What Your Kit Should Contain

The contents of the SCXI-1140 kit (part number 776572-40) are listed as follows.

Kit Component	Part Number
SCXI-1140 Module *SCXI-1140 User Manual*	181705-01 320410-01

If your kit is missing any of the components, contact National Instruments.

Optional Software

This manual contains complete instructions for directly programming the SCXI-1140. You can order separate software packages for controlling the SCXI-1140 from National Instruments.

When you combine the PC, AT, and MC data acquisition boards with the SCXI-1140, you can use LabVIEW for Windows or LabWindows for DOS. LabVIEW and LabWindows are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows enhances Microsoft C and QuickBASIC. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

Your National Instruments data acquisition board is shipped with the NI-DAQ software. NI-DAQ has a library of functions that can be called from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer, SCXI, RTSI, and self-calibration. NI-DAQ maintains a consistent software interface among its different versions so you can switch between platforms with minimal modifications to your code.

You can also use the SCXI-1140, together with the PC, AT, and MC data acquisition boards, with NI-DAQ software for DOS/Windows/LabWindows. NI-DAQ software for DOS/Windows/LabWindows comes with language interfaces for Professional BASIC, Turbo Pascal, Turbo C, Turbo C++, Borland C++, and Microsoft C for DOS; and Visual Basic, Turbo Pascal, Microsoft C with SDK, and Borland C++ for Windows. NI-DAQ software for DOS/Windows/LabWindows is on high-density 5.25 in. and 3.5 in. diskettes.

You can use the SCXI-1140, together with the NB Series data acquisition boards, with LabVIEW for Macintosh, a software system that features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments boards, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software for Macintosh.

You can also use the SCXI-1140, combined with the NB Series data acquisition boards, with NI-DAQ software for Macintosh. NI-DAQ software for Macintosh, which is shipped with all National Instruments Macintosh data acquisition boards, comes with language interfaces for MPW C, THINK C, Pascal, and Microsoft QuickBASIC. Any language that uses Device Manager Toolbox calls can access NI-DAQ software for Macintosh.

Optional Equipment

Equipment	Part Number
NB6 cable	
0.5 m	181305-01
1.0 m	181305-10
SCXI-1301 sample-and-hold terminal block	776573-01
SCXI-1310 96-pin connector and shell	776573-10
SCXI-1340 cable assembly	776574-40
SCXI-1341 Lab-NB/Lab-PC/Lab-PC+ cable assembly	776574-41
SCXI-1342 PC-LPM-16 cable assembly	776574-42
SCXI-1343 rear screw terminal adapter	776574-43
SCXI-1344 Lab-LC cable assembly	776574-44
SCXI-1346 shielded multichassis cable adapter	776574-46
SCXI-1347 SCXI shielded cable assembly	
with 1 m cable	776574-471
with 2 m cable	776574-472
with 5 m cable	776574-475
with 10 m cable	776574-470
SCXI-1349 SCXI shielded cable assembly	
with 1 m cable	776574-491
with 2 m cable	776574-492
with 5 m cable	776574-495
with 10 m cable	776574-490
SCXI-1350 multichassis adapter	776575-50
Standard ribbon cable	
0.5 m	180524-05
1.0 m	180524-10

Refer to the *Signal Connections* section in Chapter 2 and Appendix E, *SCXI-1140 Cabling*, for additional information on cabling, connectors, and adapters.

Custom Cables

The SCXI-1140 rear signal connector is a 50-pin male ribbon-cable header. The manufacturer part number of the header National Instruments uses is as follows:

- AMP Inc. (part number 1-103310-0)

The mating connector for the SCXI-1140 rear signal connector is a 50-position polarized ribbon-socket connector with strain relief. National Instruments uses a polarized or keyed connector to prevent inadvertent upside-down connection to the SCXI-1140. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

Part numbers of standard 50-conductor 28 AWG stranded ribbon cables that work with these connectors are as follows:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

The SCXI-1140 front connector is a 96-pin DIN C male connector. Recommended manufacturer part numbers for this connector are as follows:

- Harting Electronik Inc. (part number 09-03-396-6921)
- Panduit Corporation (part number 100-096-033)

The mating connector for the SCXI-1140 front connector is a 96-pin DIN C female connector. The recommended manufacturer part number for this mating connector is as follows:

- AMP Inc. (part number 535020-1; right-angle pins)
- Panduit Corporation (part number 100-096-434; straight-solder eyelet pins)

Unpacking

Your SCXI-1140 module is shipped in an antistatic package to prevent electrostatic damage to the module. Several components on the board can be damaged by electrostatic discharge. To avoid such damage in handling the module, take the following precautions:

- Touch the package to a metal part of your SCXI chassis before removing the module from the package.
- Remove the module from the package and inspect it for loose components or any other sign of damage. Notify National Instruments if the module appears damaged in any way. *Do not* install a damaged module into your SCXI chassis.

Chapter 2
Configuration and Installation

This chapter describes the SCXI-1140 jumper configurations, DIP switch settings, installation of the SCXI-1140 into the SCXI chassis, signal connections to the SCXI-1140, and cable wiring.

Module Configuration

The SCXI-1140 includes 14 jumpers and eight DIP switches that are shown in the parts locator diagram in Figure 2-1.

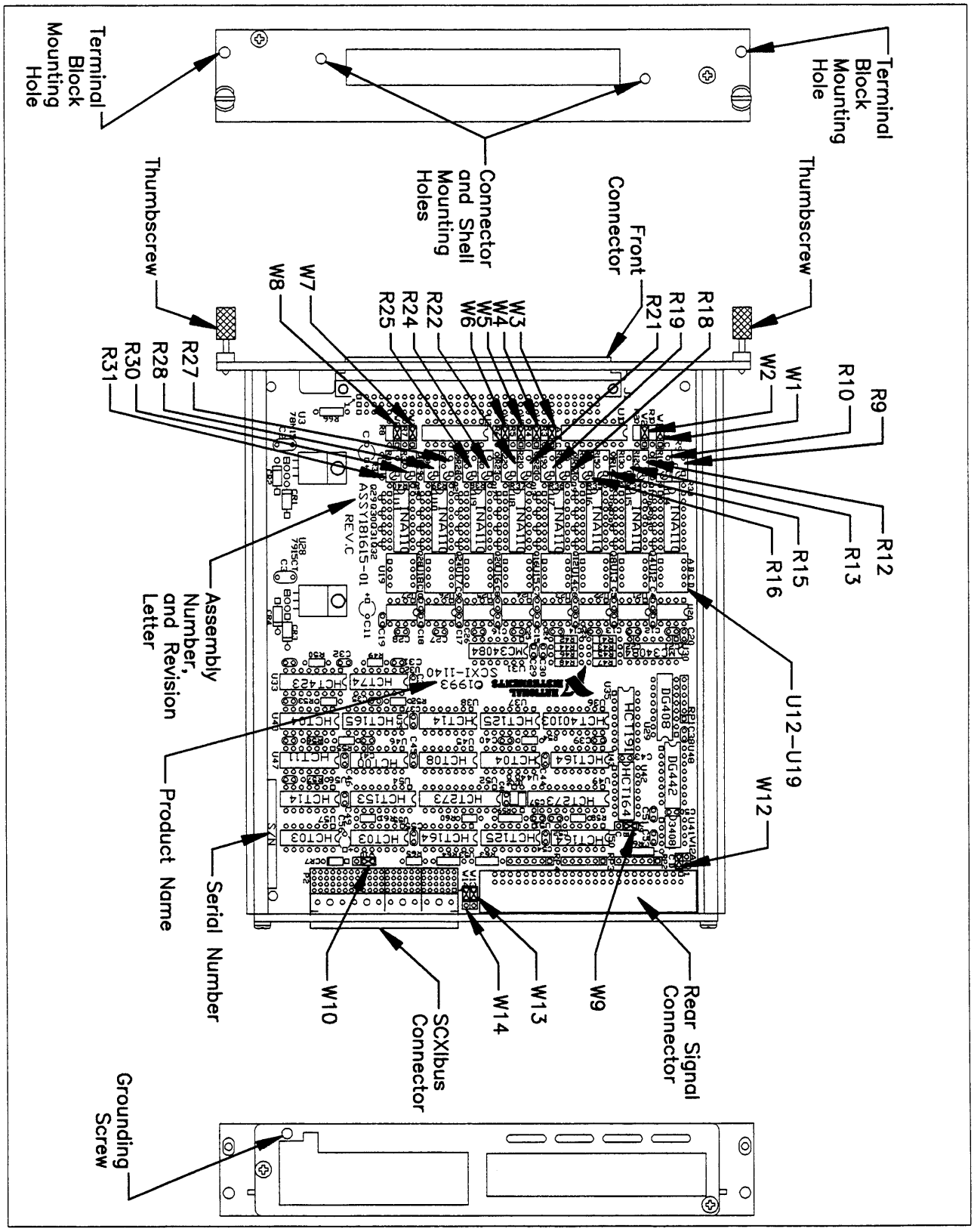


Figure 2-1. SCXI-1140 Parts Locator Diagram

The jumpers are used as follows:

- Fixed jumpers
  - Jumper W10 is reserved and you should not reconfigure it.
  - On Revision A and B modules, jumper W11 carries the SLOT0SEL* signal from the rear signal connector, after buffering, to the SCXIbus INTR* line. Leave jumper W11 in the factory-set position (position A-B). On Revision C or later modules, jumper W11 does not exist.
  - On Revision A and B modules, jumper W13 is unused and you should not connect it.
- User-configurable jumpers
  - Jumpers W1 through W8 ground the negative inputs of each input through 100 kΩ resistors for floating sources and transducers.
  - Jumper W9 allows the module to connect to a single-ended data acquisition board instead of a full differential board.
  - Jumper W12 determines the connections between the SCXIbus guard, chassis ground, and the data acquisition board analog ground.
  - Jumper W14 carries the SCXIbus MISO line, after buffering, to the SERDATOUT signal on the rear signal connector.
  - On Revision C and later modules, jumper W13 connects a pullup resistor to the SERDATOUT signal on the rear signal connector.

The module also includes eight four-position DIP switches that you use to set the gains of the eight channels. The DIP switches are shown in the parts locator diagram, Figure 2-1, as U12 through U19.

Further configuration of the module is software controlled and is discussed in Chapter 5, *Programming*.

Digital Signal Connections

The SCXI-1140 has three jumpers dedicated for communication between the data acquisition board and the SCXIbus. These jumpers are W11, W13, and W14.

Jumper W11

On Revision A and B modules, position A-B connects SLOT0SEL* to the SCXIbus INTR* line, after buffering. This is the factory-default setting and you should not change it. In this setting, the data acquisition board controls the SCXIbus INTR* line. See the *Timing Requirements and Communication Protocol* section later in this chapter, and Chapter 5, *Programming*, for information on using the INTR* line. See Appendix E, *SCXI-1140 Cabling*, for pin equivalences of the SCXI-1140 rear signal connector and the data acquisition board I/O connector.

Position B-C is reserved and you should not use it.

On Revision C or later modules, jumper W11 does not exist. SLOT0SEL* is always buffered to the INTR* line.

Jumper W14

Position A-B connects the SCXIbus MISO line, after buffering, to the SERDATOUT pin of the rear signal connector. When jumper W14 is in Position A-B and jumper W13 is properly set, the data acquisition board can read the Module ID Register of the SCXI-1140. See the *Timing Requirements and Communication Protocol* section later in this chapter, and Chapter 5, *Programming*, for information on reading the Module ID Register. See Appendix E, *SCXI-1140 Cabling*, for the SCXI-1140 rear signal connector and the data acquisition board I/O connector pin equivalences.

Position B-C disconnects SERDATOUT from the SCXIbus MISO line.

Jumper W13

On Revision A and B modules, jumper W13 should not be connected. On Revision C or later modules, position A-B connects a 2.2kΩ pullup resistor to the SERDATOUT line. Position B-C does not connect the pullup resistor to the SERDATOUT line.

Using Jumpers W13 and W14

If the SCXI-1140 is not cabled to a data acquisition board, the positions of these jumpers do not matter, so leave them in their factory default positions (both in position A-B).

If the SCXI-1140 is cabled to a data acquisition board, and the SCXI chassis that the SCXI-1140 is in, is the only SCXI chassis cabled to that data acquisition board, leave the jumpers in their factory default positions (both in position A-B).

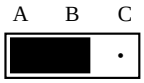
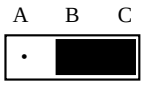
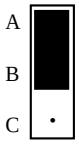
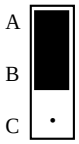
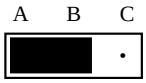
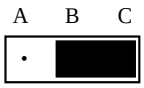
If the SCXI-1140 is cabled to a data acquisition board, and there are multiple SCXI chassis cabled to that data acquisition board with shielded cables (you are using SCXI-1346 shielded cable multi-chassis adapters), leave the jumpers in their factory default positions (both in position A-B).

If the SCXI-1140 is cabled to a data acquisition board, and there are multiple SCXI chassis cabled to that data acquisition board with ribbon cables (you are using SCXI-1350 multi-chassis adapters), leave jumper W14 in its factory default position (position A-B). On all but one of the SCXI-1140s that are cabled to the data acquisition board, move jumper W13 to position B-C. It does not matter which of the SCXI-1140 modules that are cabled to the data acquisition board has jumper W13 set to position A-B. If you have different types of modules cabled to the data acquisition board, those different modules will have jumpers similar to W14 and W13 of the SCXI-1140. Set those jumpers on the different modules using the same method described here for the SCXI-1140.

On Revision A and B SCXI-1140s, jumper W13 is not used. You set jumper W14 as explained in the cases above, except in the case of a multiple chassis ribbon cable system. In a multichassis ribbon cable system with Revision A and B SCXI-1140s cabled to the data acquisition board, you can access the MISO line in only one chassis. Pick one of the chassis and set jumper W14 to position A-B on the SCXI-1140 in that chassis that is cabled to the data acquisition board. On the SCXI-1140s that are in the other chassis and cabled to the data acquisition board, set jumper W14 to position B-C. Notice that you will only be able to access digital information from the chassis that has the SCXI-1140 with jumper W14 set to position A-B.

On Revision C and later modules, the SERDATOUT line is driven by an open-collector driver, which is a driver that actively drives low or goes to a high-impedance state, relying on a pullup resistor to make the signal line go high. When using a single chassis, leave W13 and W14 in position A-B (factory default) on the SCXI-1140 that is connected to the data acquisition board. In this configuration, jumper W13 connects the necessary pullup resistor to the SERDATOUT line, and the module drives MISO to SERDATOUT. When using multiple chassis, leave jumper W14 in position A-B on all of the SCXI-1140s that are cabled to the data acquisition board. You should set jumper W13 in position A-B on only one (it does not matter which one) of the SCXI-1140s that are cabled to the data acquisition board. Set jumper W13 in position B-C on all of the other SCXI-1140 modules that are cabled to the data acquisition board. If too many pullup resistors are attached to the SERDATOUT line, the drivers cannot drive the line low. See Table 2-1 for a description and configuration of the jumper settings.

Table 2-1. Digital Jumper Settings

Jumper	Description	Configuration
W14	Factory-default setting; connects MISO to SERDATOUT	
W14	Parking position	
W10	Factory-default setting	
W11	Factory-default setting (revisions A and B modules only)	
W13	Factory-default setting; connects pullup to SERDATOUT (revision C and later)	
W13	Parking position (not connected on revisions A or B modules)	

Analog Configuration

The SCXI-1140 has 10 analog configuration jumpers–W1 through W9, and W12–and eight gain-setting, four-position DIP switches–U12 through U19.

Input Mode Selection

Jumpers W1 through W8

Position A-B leaves the negative input of the instrumentation amplifier connected only to the front connector. This is the factory-default setting.

Position B-C connects the negative input of the instrumentation amplifier to the module analog ground through a 100 kΩ resistor. This setting is useful for keeping floating (non-ground referenced) sources from saturating the instrumentation amplifier. Table 2-2 shows the input mode jumper and channel selections.

Table 2-2. Input Mode Selection Jumpers

Channel	Use Jumper
0	W1
1	W2
2	W3
3	W4
4	W5
5	W6
6	W7
7	W8

Output Selection

Jumper W9

Position A-B leaves pin 19 (AIGND/NC) of the rear signal connector unconnected and is the factory-default setting.

Position B-C connects the module analog ground to pin 19 (AIGND/NC) of the rear signal connector. Use this position for MIO boards operating in NRSE mode.

Grounding and Shielding

Jumper W12

Position A-B connects the module analog ground to the analog bus guard.

Position A-C connects the module analog ground to pins 1 and 2 (AIGND/GUARD) of the rear signal connector. Use this position for all boards operating in RSE mode, and for the Lab-PC+ operating in NRSE mode.

Position B-D connects the data acquisition board analog ground to the analog bus guard.

Position C-D leaves the grounds disconnected and is the factory-default setting.

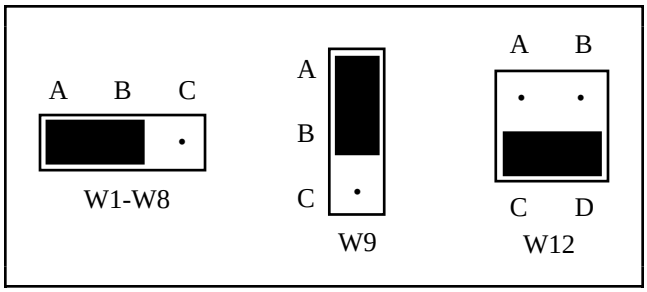


Figure 2-2. Analog Jumpers (Factory Setting)

Gain Selection

You can use each DIP switch to set the gain of its channel as shown in Table 2-3.

Table 2-3. Gain Switches for Each Channel

Channel	Use DIP Switch
0	U12
1	U13
2	U14
3	U15
4	U16
5	U17
6	U18
7	U19

Leaving all four switches in the open (number side up) position selects a gain of one, as shown in Figure 2-3. This setting is the factory default.

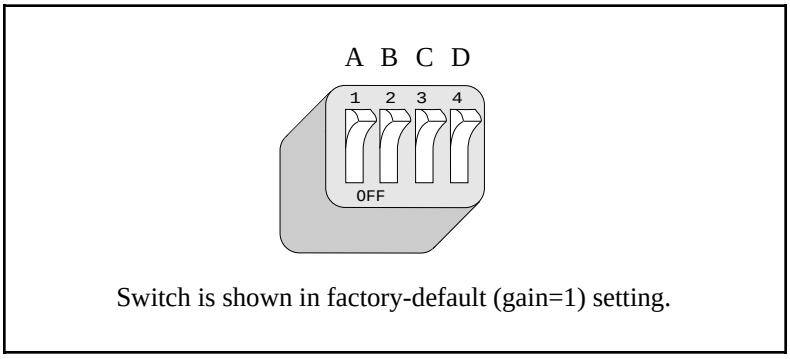


Figure 2-3. Gain Switches for Each Channel

Closing switch A selects a gain of 500.

Closing switch B selects a gain of 200.

Closing switch C selects a gain of 100.

Closing switch D selects a gain of 10.

You can select other gains by closing more than one switch, as shown in Table 2-4.

Table 2-4. Switch Settings for Gain Selection

Desired Gain	Close Switches
1	None
10	D
100	C
200	B
300	B and C
500	A
600	A and C
700	A and B
800	A, B, and C

Hardware Installation

You can install the SCXI-1140 in any available SCXI chassis. After you have made any necessary changes and have verified and recorded the jumper and DIP switch settings (a form is included for this purpose in Appendix G, *Customer Communication*), you are ready to install the SCXI-1140. The following are general installation instructions, but consult the user manual of your SCXI chassis for specific instructions and warnings.

1. Turn off the computer that contains the data acquisition board.

2. Turn off the SCXI chassis. Do not insert the SCXI-1140 into a chassis that is turned on.

3. Insert the SCXI-1140 into the board guides. Gently guide the module into the back of the slot until the connectors make good contact. If a cable assembly has already been installed in the rear of the chassis, the module and cable assembly must be firmly engaged; however, *do not force* the module into place.

4. Screw the front mounting panel of the SCXI-1140 to the top and bottom threaded strips of your SCXI chassis.

5. If you are going to connect this module to an MIO-16 data acquisition board, attach the connector at the metal end of the SCXI-1340 cable assembly to the rear signal connector on the SCXI-1140 module. Screw the rear panel to the rear threaded strip. Attach the loose end of the cable to the MIO-16 board.

   Notes: If you already have another module in your chassis that is cabled to your data acquisition board, you generally do not need to connect additional cabling to the SCXI-1140. Typically, only one module in a chassis is cabled to a board. If your chassis has different types of modules, cable the data acquisition board to one of the SCXI-1140 modules.

   For installation procedures with other SCXI accessories and data acquisition boards, consult Appendix E, *SCXI-1140 Cabling.*

6. Check the installation.

7. Turn on the SCXI chassis.

8. Turn on the computer.

The SCXI-1140 module is installed and ready for operation.

Signal Connections

This section describes the input and output signal connections to the SCXI-1140 module via the SCXI-1140 front and rear signal connectors, and includes specifications and connection instructions for the SCXI-1140 connector signals.

Warning: Connections that exceed any of the maximum ratings of input or output signals on the SCXI-1140 can result in damage to the SCXI-1140 module, to the SCXIbus, to any connected data acquisition board, and to the computer in which the data acquisition board is installed. Maximum input ratings for each signal are given in this chapter under the discussion of that signal. National Instruments is *not* liable for any damages resulting from such signal connections.

The Front Connector

Figure 2-4 shows the pin assignments for the SCXI-1140 front connector.

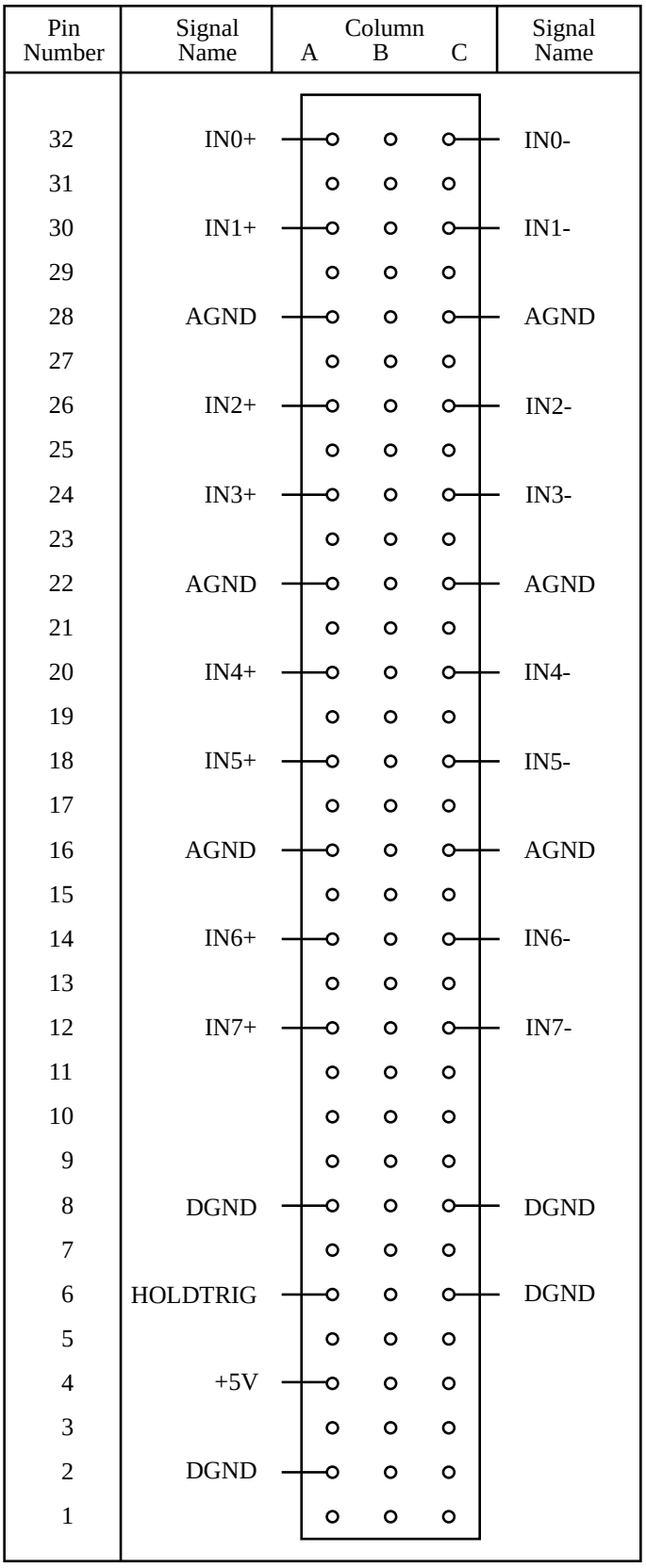


Figure 2-4. SCXI-1140 Front Connector Pin Assignment

Front Connector Signal Connection Descriptions

Pin	Signal Name	Description
A32, A30, A26, A24, A20, A18, A14, A12	IN0+ through IN7+	Positive Input Channels – Connect to the noninverting inputs of the instrumentation amplifier of each channel.
C32, C30, C26, C24, C20, C18, C14, C12	IN0- through IN7-	Negative Input Channels – Connect to the inverting inputs of the instrumentation amplifier of each channel.
A28, A22, A16, C28, C22, C16	AGND	Analog Ground – Connect to the module analog ground.
A6	HOLDTRIG	HOLDTRIG – Can be programmed to input or output the Hold Trigger signal for the module. The Hold Trigger signal can place the module into Hold mode. This signal is also brought out to the rear signal connector.
A2, C6, A8, C8	DGND	Digital Ground – Connect to the module digital ground.
A4	+5V	Digital Five Volts – This signal is for test purposes only and should not be loaded by more than 25 mA. Only on Rev C and later modules.

Analog Input Channels

All eight channels have fully differential inputs, so the signals you are measuring should be ground referenced. If they are not, you should move jumpers W1 through W8 of the nonreferenced channels to position B-C to create a DC path for the input bias currents. If you do not do this, the bias currents of the instrumentation amplifiers of the nonreferenced channels produce stray capacitances, resulting in uncontrollable drift and possible saturation.

Figure 2-5 illustrates how to connect a ground-referenced signal.

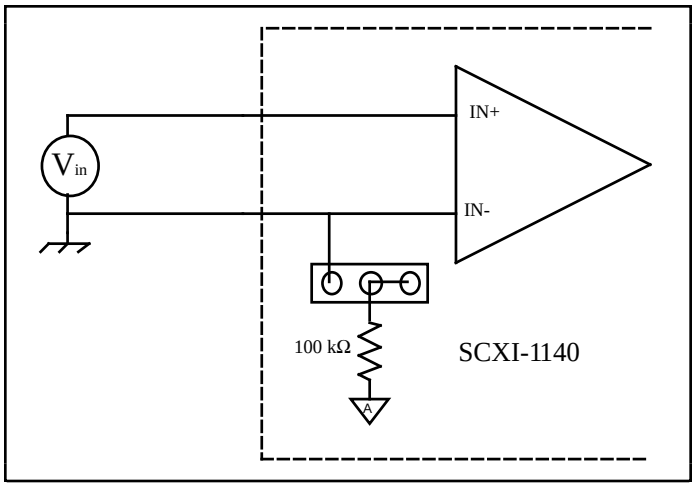


Figure 2-5. Ground-Referenced Signal Connection

Figure 2-6 illustrates how to connect a floating signal.

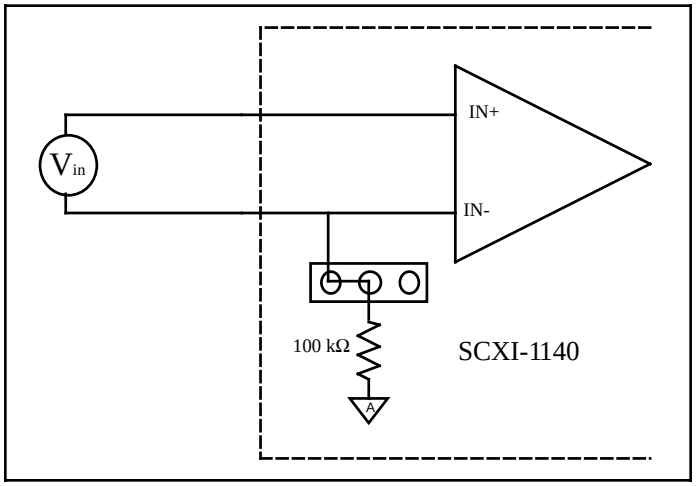


Figure 2-6. Floating Signal Connection

For AC-coupled signals, set jumpers W1 through W8 to position B-C with an external resistor from the positive input channel connected to its negative ground. Doing this creates the DC path for the positive input bias current. Typical resistor values range from 100 kΩ to 10 MΩ. This solution, although necessary in this case, lowers the input impedance of the channel and introduces an additional offset voltage proportional to the product of the input bias current and the resistor value used. The inputs of the SCXI-1140 have a typical bias current of about ±100 pA. When you use a 1 MΩ resistor, the result is ±100 µV of offset, which is insignificant in most applications. However, if you use larger valued bias resistors, significant input offset may result. Lower valued bias resistors will increase loading of the source, possibly resulting in gain error.

Figures 2-7 through 2-9 illustrate how to connect AC-coupled signals.

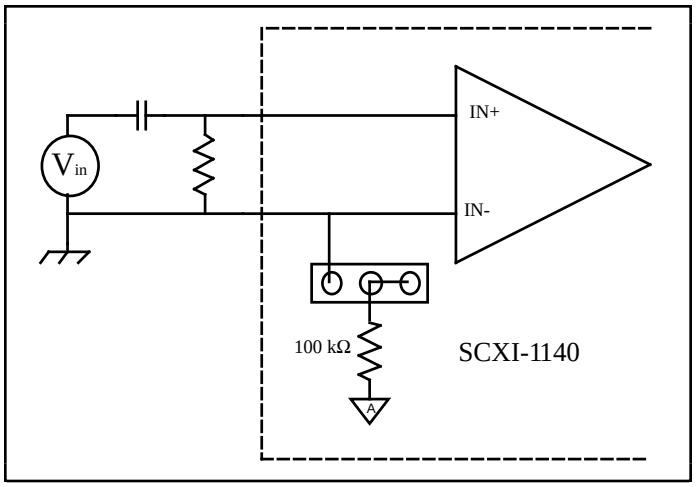


Figure 2-7. Ground-Referenced AC-Coupled Signal Connection

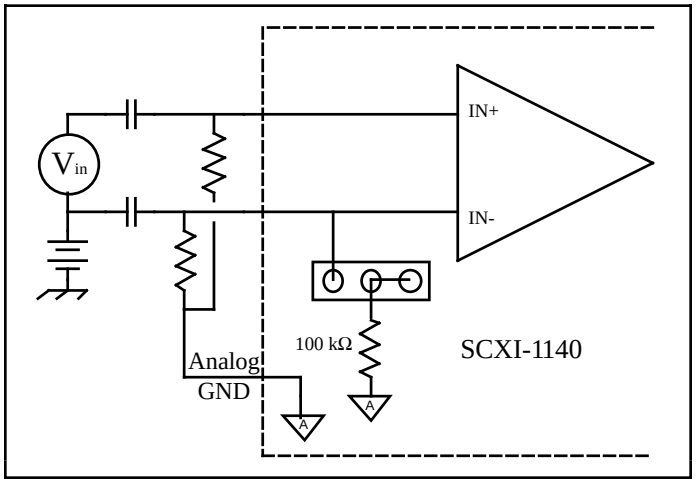


Figure 2-8. Ground-Offset AC-Coupled Signal Connection

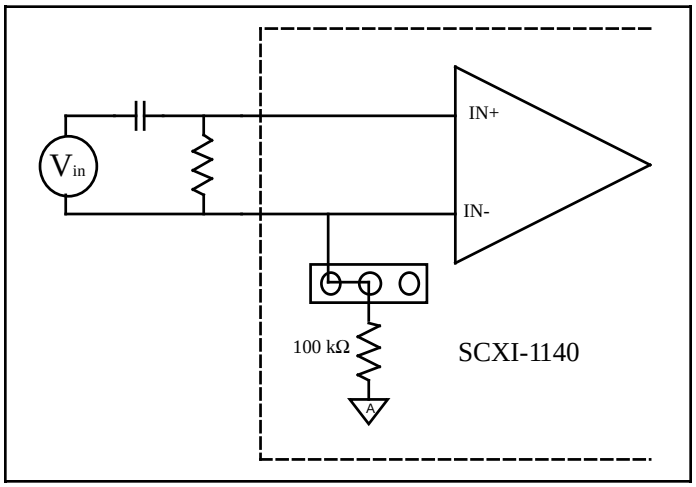


Figure 2-9. Floating AC-Coupled Signal Connection

The SCXI-1140 instrumentation amplifiers can reject any voltage within their common-mode input range caused by ground potential differences between the signal source and the module. In addition, the amplifiers can reject common-mode noise pickup in the leads connecting the signal sources to the SCXI-1140 module. However, you should be careful to minimize noise pickup. The common-mode rejection of the instrumentation amplifiers decreases significantly at high frequencies. The amplifiers do not reject normal-mode noise.

The common-mode input range of the SCXI-1140 instrumentation amplifiers is defined as the magnitude of the greatest common-mode signal that can be rejected. Thus the common-mode input range for the SCXI-1140 depends on the gain and size of the differential input signal ($V_{diff} = V^{+}_{in} - V^{-}_{in}$).

The exact formula for the permissible common-mode input range is as follows:

$$V_{cm\text{-}allowed} = \pm (12\ V - G\ |V_{diff}| / 2)$$

Thus, with a differential voltage of 10 V and a gain of G = 1, the maximum possible common-mode voltage would be ±7 V. The same range would apply for a differential input of 100 mV and a gain of 100. The range increases to ±12 V for zero differential input voltage. The actual common-mode voltage available at the input is measured with respect to the SCXI-1140 ground, and can be calculated by the following formula:

$$V_{cm\text{-}actual} = (V^{+}_{in} + V^{-}_{in})/2$$

where V^{+}_{in} is the signal at the positive input (IN0+ through IN7+), and V^{-}_{in} is the signal at the corresponding negative input (IN0- through IN7-). Both V^{+}_{in} and V^{-}_{in} are measured with respect to the SCXI-1140 chassis ground.

Warning: Exceeding the differential and common-mode input ranges results in distorted input signals. Exceeding the maximum input voltage rating can result in damage to the SCXI-1140 module, the SCXIbus, and the data acquisition board. National Instruments is *not* liable for any damages resulting from such signal connections.

Digital Input

The HOLDTRIG pin on the front signal connector is identical in function to the HOLDTRIG pin on the rear signal connector. The two are wired together internally through about 200 Ω of protection resistance. For this reason, you should be careful to ensure that the signal is not simultaneously driven from both connectors. For further information on this signal, see the *Digital I/O Signal Connections* and *Timing Requirements and Communication Protocol* sections for the rear signal connector later in this chapter. The signal should be in the 0 to 5 V range, with switching occurring around 1.5 V.

Although HOLDTRIG is a digital signal, it is still susceptible to noise, particularly at its transitions. If you configure the SCXI-1140 to be level sensitive, noise at the HOLDTRIG signal transitions is not particularly important. In Edge-Sensitive mode, however, noise can cause the module to enter Hold mode on the wrong edge. Two possible transition noise sources are interference and reflection. You can minimize interference by properly shielding the incoming trigger signal. You can minimize reflection by ensuring that the trigger signal source is impedance matched to the cable used to transmit the signal. You can frequently accomplish impedance matching by inserting a small resistor (about 50 Ω) in series with the signal source.

However, the best way to ensure that the HOLDTRIG signal is not corrupted by noise is to minimize the distance that the signal must travel.

Terminal Block and Connector and Shell

There are two types of connectors to connect the signals to the SCXI-1140 inputs. The first is a 96-pin DIN C female connector and its shell. The second is a terminal block with screw terminals for easy connection.

These kits are listed in the *Optional Equipment* section in Chapter 1, *Introduction*.

Connector and Shell

The SCXI-1310 front connector and shell are available in a kit. The connector has eyelet ends for easy hook-and-soldering of wires. With this kit, you can build your own cable to connect to the SCXI-1140 inputs. After you build the cable, the shell covers and protects the connector.

Follow the steps included in your connector and shell kit to assemble the shell. After you have built the shell, mount the connector and shell to your SCXI module in the following steps:

1. Turn off your computer or disconnect it from your SCXI chassis.
2. Turn off your SCXI chassis.
3. Slide the module of interest out of the SCXI chassis.
4. Refer to Figure 2-10, *Assembling and Mounting the Connector and Shell*.
5. Remove the module cover.
6. Place one jack screw as indicated in Figure 2-10.
7. While holding the screw in place, insert the lock washer and then the nut. Notice that you might need long-nose pliers to insert the washer and nut.
8. Tighten the nut by firmly holding it and rotating the jack screw.
9. Repeat steps 6 through 8 for the second jack screw.
10. Place the module cover back in place and tighten the grounding screw.
11. Slide the module back in place.
12. Connect the connector and shell to your module connector and hold the connector and shell in place by tightening both mounting screws.

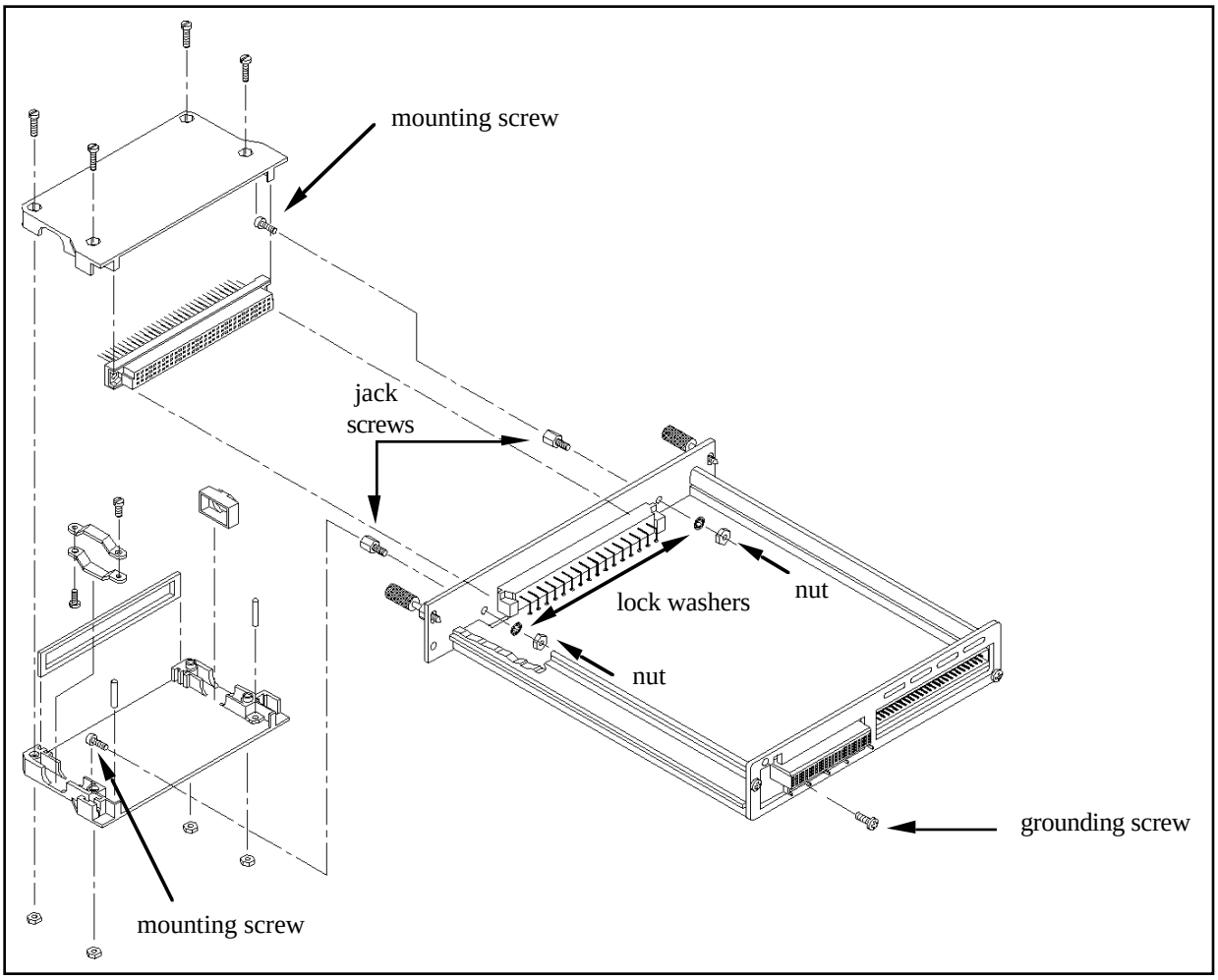


Figure 2-10. Assembling and Mounting the Connector and Shell

Terminal Block

The terminal block consists of a shielded board with supports to connect to the SCXI-1140 front signal connector. There are twenty screw terminals for easy connection. Eight pairs of screw terminals are dedicated for signal connection to the eight differential inputs of the SCXI-1140, two screw terminals connect to AGND, and one pair of screw terminals connects to the HOLDTRIG digital signal and DGND.

Cable Connection

To connect wire pairs to the terminal block, use the following procedure:

1. Remove the rear grounding screw on the edge of the rear panel of the terminal block.
2. Snap out the top cover of the shield by placing a screwdriver in the groove at the bottom of the terminal block.
3. Slide the wires, one at a time, through the front panel strain relief.

4. Connect the wires to the screw terminals.
5. Tighten the strain relief.
6. Snap the top cover back in place.
7. Reinsert the rear grounding screw.
8. Connect the terminal block to the SCXI-1140 front connector, and tighten the top and bottom screws on the back of the terminal block to hold it securely in place.

The Rear Signal Connector

Note: If you will be using the SCXI-1140 with a National Instruments data acquisition board and cable assembly, you *do not* need to read the remainder of this chapter. If you will also be using the SCXI-1180 feedthrough panel, the SCXI-1343 rear screw terminal adapter, or the SCXI-1351 one-slot cable extender with the SCXI-1140, you should read this section.

Figure 2-11 shows the pin assignments for the SCXI-1140 rear signal connector.

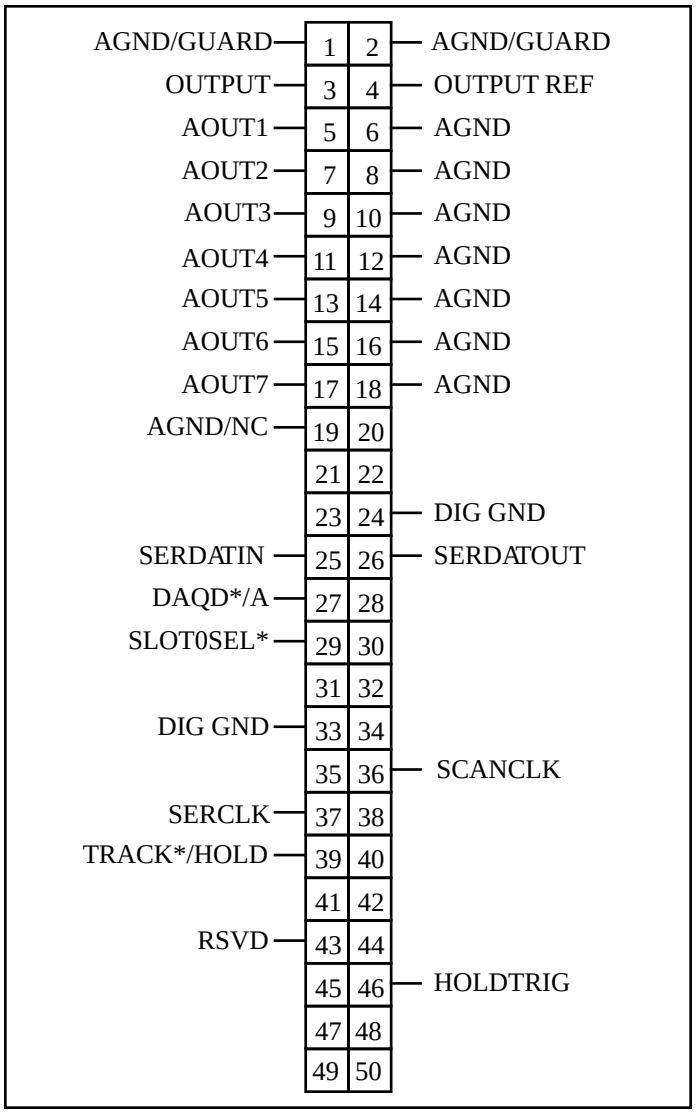


Figure 2-11. SCXI-1140 Rear Signal Connector Pin Assignment

Rear Signal Connector Pin Descriptions

Pin	Signal Name	Description
1-2	AGND/GUARD	Analog Ground/Guard – Connected to the module analog ground when jumper W12 is in position A-C, or to the SCXIbus analog bus guard when the jumper is in position A-B. Otherwise leave unconnected. These pins connect to the analog ground of the MIO data acquisition boards.
3	OUTPUT	Output – Main module analog output. In Scan mode, the outputs of all eight channels appear here in sequence. Outputs from other modules can also appear here through the analog bus. In Nonscanning mode, OUTPUT is the output of Channel 0.
4	OUTPUT REF	Output Reference – Connects to the module analog ground unless an output from another module is selected through the analog bus, in which case the pins connect to the analog ground for the selected module.
5, 7, 9, 11, 13, 15, 17	AOUT1 through AOUT7	Analog Outputs – Outputs of channels 1 through 7, independent of whether or not scanning is enabled.
6, 8, 10, 12, 14, 16, 18	AGND	Analog Ground – Connect to the module analog ground. They are used as the reference points for AOUT1 through AOUT7.
19	AGND/NC	Analog Ground/No Connect – Connect to the module analog ground when jumper W9 is in position B-C. When the jumper is in position A-B, this pin is unconnected.
24, 33	DIG GND	Digital Ground – Supply the reference for data acquisition digital signals and are tied to the module digital ground.
25	SERDATIN	Serial Data In – Taps into the SCXIbus MOSI line to send serial input data to a module or Slot 0.
26	SERDATOUT	Serial Data Out – Taps into the SCXIbus MISO line to accept serial output data from a module if jumper W14 is in position A-B. Otherwise, it is unconnected.

Pin	Signal Name	Description (continued)
27	DAQD*/A	Data Acquisition Board Data/Address Line – Taps into the SCXIbus D*/A line to indicate to the module whether the incoming serial stream is data or address information.
43	RSVD	Reserved.
29	SLOT0SEL*	Slot 0 Select – Taps into the SCXIbus INTR* line to indicate whether the information on MOSI is being sent to a module or Slot 0.
36	SCANCLK	Scan Clock – Indicates to the SCXI-1140 that a sample has been taken by the data acquisition board and causes the SCXI-1140 to change channels.
37	SERCLK	Serial Clock – Taps into the SCXIbus SPICLK line to clock the data on the MOSI and MISO lines.
39	TRACK*/HOLD	Track/Hold – Can be programmed to reflect the state of the module–low in Track mode or high in Hold mode. TRACK*/HOLD can also be programmed to a high-impedance output.
46	HOLDTRIG	HOLDTRIG – You can program HOLDTRIG to input or output the Hold Trigger signal for the module. You can use the Hold Trigger signal to place the module into Hold mode. This signal is also brought out to the front connector.

All other pins are not connected. See the *Timing Requirements and Communication Protocol* section later in this chapter for more detailed information on timing.

The signals on the rear signal connector can be classified as analog output signals, digital I/O signals, or timing I/O signals. The following section contains signal connection guidelines for each of these groups.

Analog Output Signal Connections

Pins 3 through 19 of the rear signal connector are analog output signal pins. Pin 3 is the main output, and pin 4 is its reference signal. All eight channels are multiplexed onto this output under hardware control in Scan mode. In Nonscanning mode, the output simply becomes the output of one selected channel. Channel 0 is the power up and reset default. When scanning multiple modules, you can also connect this output to the SCXIbus analog bus and the analog bus will drive this output. Pins 5, 7, 9, 11, 13, 15, and 17 are direct outputs from channels 1 through 7, respectively. Thus, if you program pin 3 to monitor the Channel 0 output, all eight channels are available simultaneously at the connector. Pins 6, 8, 10, 12, 14, 16, and 18 are the reference signals for outputs 1 through 7. If possible, you should use differential connections to measure

the outputs. If your data acquisition board uses single-ended inputs, connect the ground (or the negative input, for NRSE mode) of the data acquisition board to pin 19 and set jumper W9 to position B-C so that pin 19 connects to the module analog ground.

Warning: The SCXI-1140 analog outputs are not overvoltage protected, although they are short circuit protected. Applying external voltage to these outputs may result in damage to the SCXI-1140. National Instruments is *not* liable for any damages resulting from such signal connections.

Digital I/O Signal Connections

Pins 24 through 27, 29, 33, 36 through 39, 43, and 46 constitute the digital I/O lines of the rear signal connector. These pins belong to one of three categories–digital input signals, digital output signals, and timing signals. Pins 24 and 33 are the digital ground reference for all the data acquisition board digital signals and are tied to the module digital ground.

The digital input signals are pins 25, 27, 29, and 37. The data acquisition board uses these pins to configure the SCXI module when the module is under data acquisition control. Each digital line emulates the SCXIbus communication signals as follows:

- Pin 25 is SERDATIN and is equivalent to the SCXIbus MOSI serial data input line.
- Pin 27 is DAQD*/A and is equivalent to the SCXIbus D*/A line. Pin 27 indicates to the module whether the incoming serial stream on SERDATIN is data (DAQD*/A = 0) or address (DAQD*/A = 1) information.
- Pin 29 is SLOT0SEL* and is equivalent to the SCXIbus INTR* line. Pin 29 indicates whether the data on the SERDATIN line is being sent to Slot 0 (SLOT0SEL* = 0) or to a module (SLOT0SEL* = 1). Jumper W11 must be in position A-B.
- Pin 37 is SERCLK and is equivalent to the SCXIbus SPICLK line and is used to clock the serial data on the SERDATIN line into the module registers.

The digital output signal is pin 26.

- Pin 26 is SERDATOUT and is equivalent to SCXIbus MISO when jumper W14 is in position A-B.

The digital I/O signals of the SCXI-1140 match the digital I/O lines of the MIO-16. When you use the SCXI-1140 with an SCXI-1341 or an SCXI-1342 cable assembly, the SCXI-1140 signals match the digital lines of the Lab boards and the PC-LPM-16 board, respectively. Table 2-5 lists the equivalences. For more information, consult Appendix E, *SCXI-1140 Cabling.*

Table 2-5. SCXIbus to SCXI-1140 Rear Signal Connector to Data Acquisition Board Pin Equivalences

SCXIbus Line	SCXI-1140 Rear Signal Connector	MIO-16	Lab-NB Lab-PC Lab-PC+ Lab-LC	PC-LPM-16
MOSI	SERDATIN	ADIO0	PB4	DOUT4
D*/A	DAQD*/A	ADIO1	PB5	DOUT5
INTR*	SLOT0SEL*	ADIO2	PB6	DOUT6
SPICLK	SERCLK	EXTSTROBE*	PB7	DOUT7
MISO	SERDATOUT	BDIO0	PC1	DIN6

The digital timing signals are pins 36, 39, 43, and 46:

- Pin 36 is SCANCLK, and you use it as a clock for the SCXI-1140 multiplexer counter. The data acquisition board should pulse this signal at the end of each conversion if the module is in Scan mode.
- Pin 39 is TRACK*/HOLD, which you can use to gate or trigger conversions on the data acquisition board. Enable pin 39 through the Module Configuration Register. See Chapter 5, *Programming*, for more information.
- Pin 43 is a reserved digital input.
- Pin 46 is HOLDTRIG, which you can use to place the module into Hold mode. See Chapter 3, *Theory of Operation*, and Chapter 5, *Programming*, for more information.

The following specifications and ratings apply to the digital I/O and timing lines.

Absolute maximum voltage
Input rating -0.5 to 5.5 V with respect to DIG GND

Digital input specifications (referenced to DIG GND):

V_{IH} input logic high voltage 2 V minimum
V_{IL} input logic low voltage 0.8 V maximum

I_I input current leakage ±1 µA maximum

Digital output specifications (referenced to DIG GND)

V_{OH} output logic high voltage 3.7 minimum at 4 mA
V_{OL} output logic low voltage 0.4 maximum at 4 mA

Timing Requirements and Communication Protocol

Timing Signals

The data acquisition timing signals are SCANCLK, TRACK*/HOLD, and HOLDTRIG.

Use SCANCLK to increment the output multiplexer on its rising edge. Figure 2-12 illustrates the timing requirements on the SCANCLK signal. These requirements ensure that SCANCLK is properly transmitted over TRIG0.

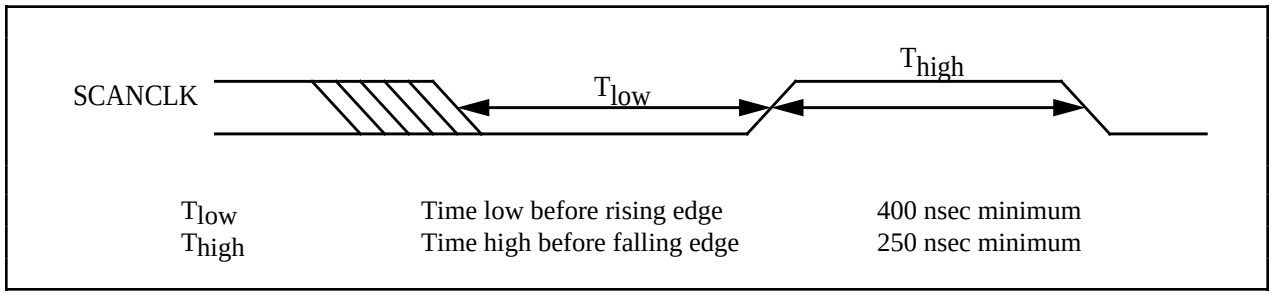


Figure 2-12. SCANCLK Timing Requirements

For settling time specifications, refer to Appendix A, *Specifications.*

Use HOLDTRIG to put the module into Hold mode. Figure 2-13 shows the timing requirements on the HOLDTRIG signal. These requirements ensure that HOLDTRIG is properly transmitted over TRIG1.

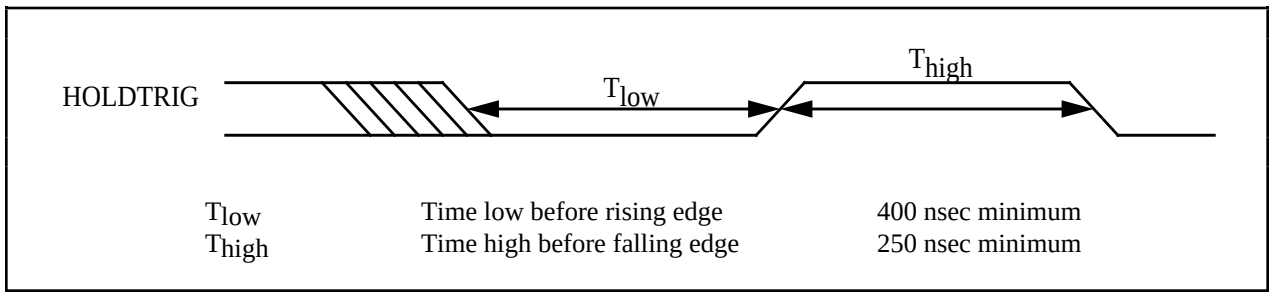
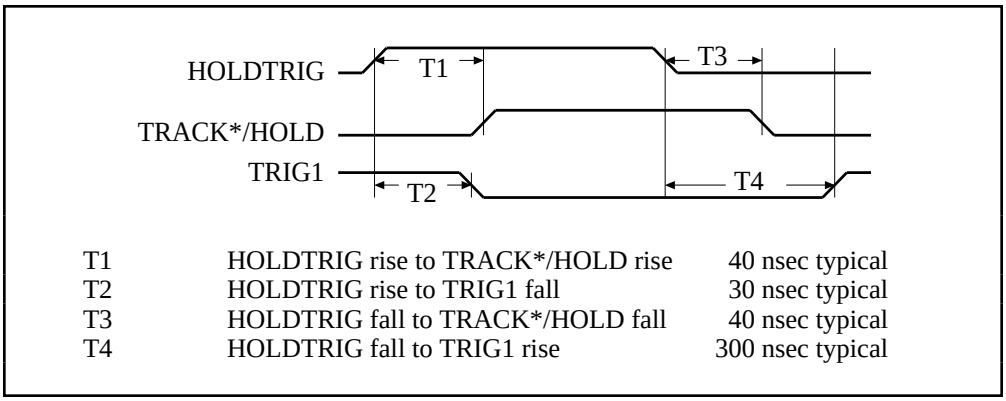


Figure 2-13. HOLDTRIG Timing Requirements

Notice that these are only requirements on the pulse widths of HOLDTRIG, and do not imply that the SCXI-1140 will operate properly in Level-Sensitive mode with a 1 MHz HOLDTRIG signal. See Appendix A, *Specifications*, for the settling time requirements of the SCXI-1140 module. The following diagrams show the timing delays of TRIG1, TRACK*/HOLD, HOLDTRIG, SCANCLK, and TRIG0.

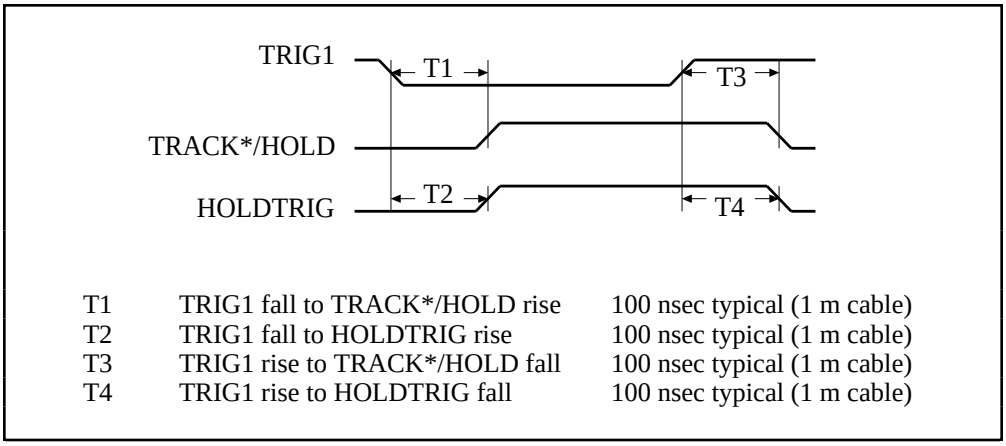
In Level-Sensitive mode, when HOLDTRIG is the source of the Hold Trigger, the TRACK*/HOLD signal follows HOLDTRIG and TRIG1 inverts HOLDTRIG, as shown in Figure 2-14.



T1	HOLDTRIG rise to TRACK*/HOLD rise	40 nsec typical
T2	HOLDTRIG rise to TRIG1 fall	30 nsec typical
T3	HOLDTRIG fall to TRACK*/HOLD fall	40 nsec typical
T4	HOLDTRIG fall to TRIG1 rise	300 nsec typical

Figure 2-14. Level-Sensitive Mode, HOLDTRIG Source

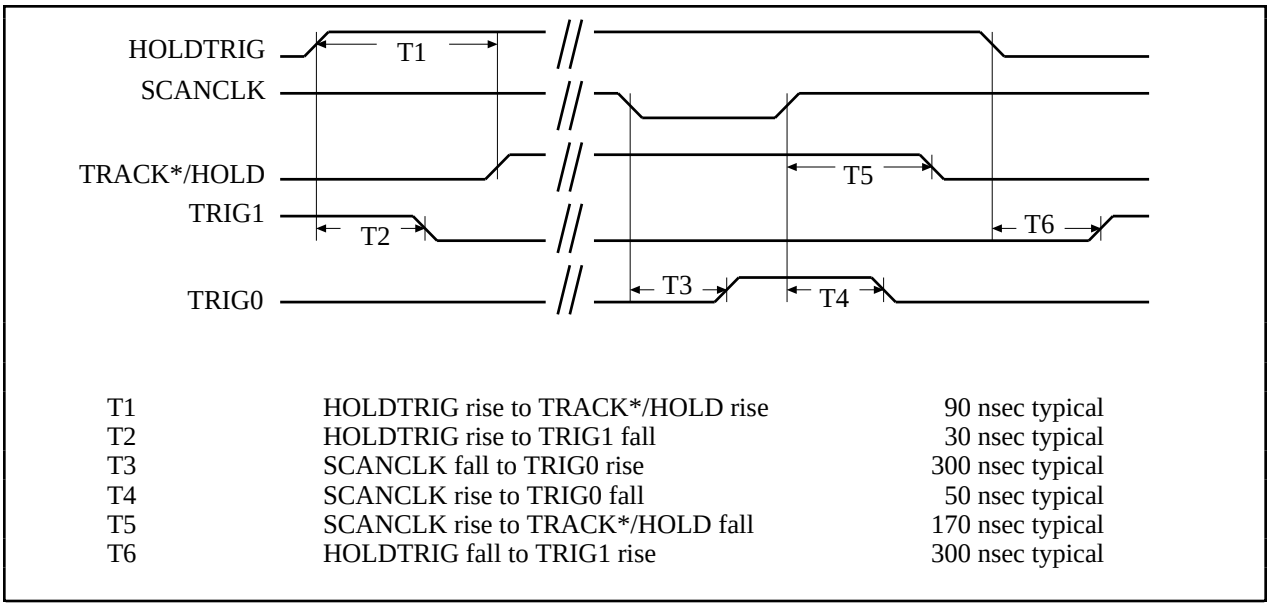
In Level-Sensitive mode, when TRIG1 is the source of the Hold Trigger, both the TRACK*/HOLD pin and the HOLDTRIG pin give the inverse of TRIG1, as shown in Figure 2-15.



T1	TRIG1 fall to TRACK*/HOLD rise	100 nsec typical (1 m cable)
T2	TRIG1 fall to HOLDTRIG rise	100 nsec typical (1 m cable)
T3	TRIG1 rise to TRACK*/HOLD fall	100 nsec typical (1 m cable)
T4	TRIG1 rise to HOLDTRIG fall	100 nsec typical (1 m cable)

Figure 2-15. Level-Sensitive Mode, TRIG1 Source

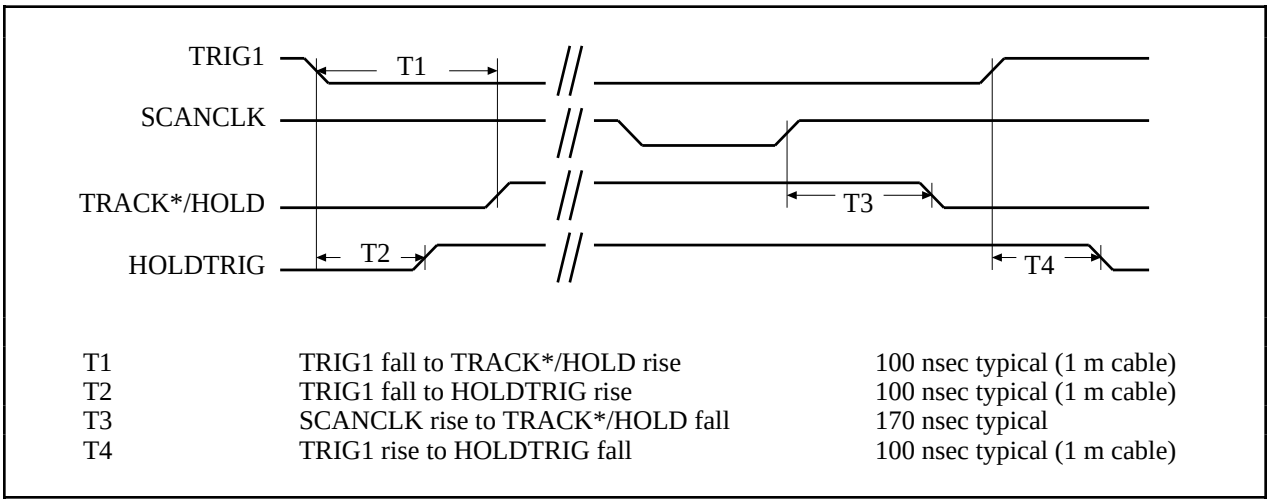
In Edge-Triggered mode, when HOLDTRIG is the source of the Hold Trigger, the rising edge of HOLDTRIG puts the module into Hold mode. After enough samples have been taken, a SCANCLK will cause SCANCON to change, which eventually puts the module back into Track mode, as shown in Figure 2-16.



T1	HOLDTRIG rise to TRACK*/HOLD rise	90 nsec typical
T2	HOLDTRIG rise to TRIG1 fall	30 nsec typical
T3	SCANCLK fall to TRIG0 rise	300 nsec typical
T4	SCANCLK rise to TRIG0 fall	50 nsec typical
T5	SCANCLK rise to TRACK*/HOLD fall	170 nsec typical
T6	HOLDTRIG fall to TRIG1 rise	300 nsec typical

Figure 2-16. Edge-Triggered Mode, HOLDTRIG Source

In Edge-Triggered mode, when TRIG1 is the source of the Hold Trigger, the falling edge of TRIG1 puts the module into Hold mode. After enough samples have been taken, a SCANCLK causes SCANCON to change, which eventually puts the module back into Track mode, as shown in Figure 2-17.



T1	TRIG1 fall to TRACK*/HOLD rise	100 nsec typical (1 m cable)
T2	TRIG1 fall to HOLDTRIG rise	100 nsec typical (1 m cable)
T3	SCANCLK rise to TRACK*/HOLD fall	170 nsec typical
T4	TRIG1 rise to HOLDTRIG fall	100 nsec typical (1 m cable)

Figure 2-17. Edge-Triggered Mode, TRIG1 Source

Communication Signals

This section describes the methods for communicating on the Serial Peripheral Interface (SPI) bus and their timing requirements. The communication signals are SERDATIN, DAQD*/A, SLOT0SEL*, SERDATOUT, and SERCLK. Furthermore, Slot 0 produces SS* according to data acquisition board programming; therefore, its timing relationships with the communication signals are also discussed. For information on the Slot-Select Register in Slot 0, consult Chapter 5, *Programming*.

The data acquisition board determines to which slot it will talk by writing a slot-select number to Slot 0. In the case of an SCXI-1001 chassis, this write also determines to which chassis the data acquisition board will talk. You also write a slot-select number to program the Slot 0 hardscan circuitry. See Chapter 5, *Programming*, for information on programming the Slot 0 hardscan circuitry.

Use the following procedure for selecting a slot in a particular chassis. Figure 2-18 illustrates the timing of this procedure with the example of selecting Slot 11 in Chassis 9. Notice that the factory-default chassis address for the SCXI-1001 is address 0. For information on changing the address of your chassis, consult the *SCXI-1000/1001 User Manual.* An SCXI-1000 chassis responds to any chassis number.

To write the 16-bit slot-select number to Slot 0, follow these steps:

1. Initial conditions:

   SERDATIN = don't care.
   DAQD*/A = don't care.
   SLOT0SEL* = 1.
   SERCLK = 1.

2. Clear SLOT0SEL* to 0 to deassert all SS* lines to all modules in all chassis.

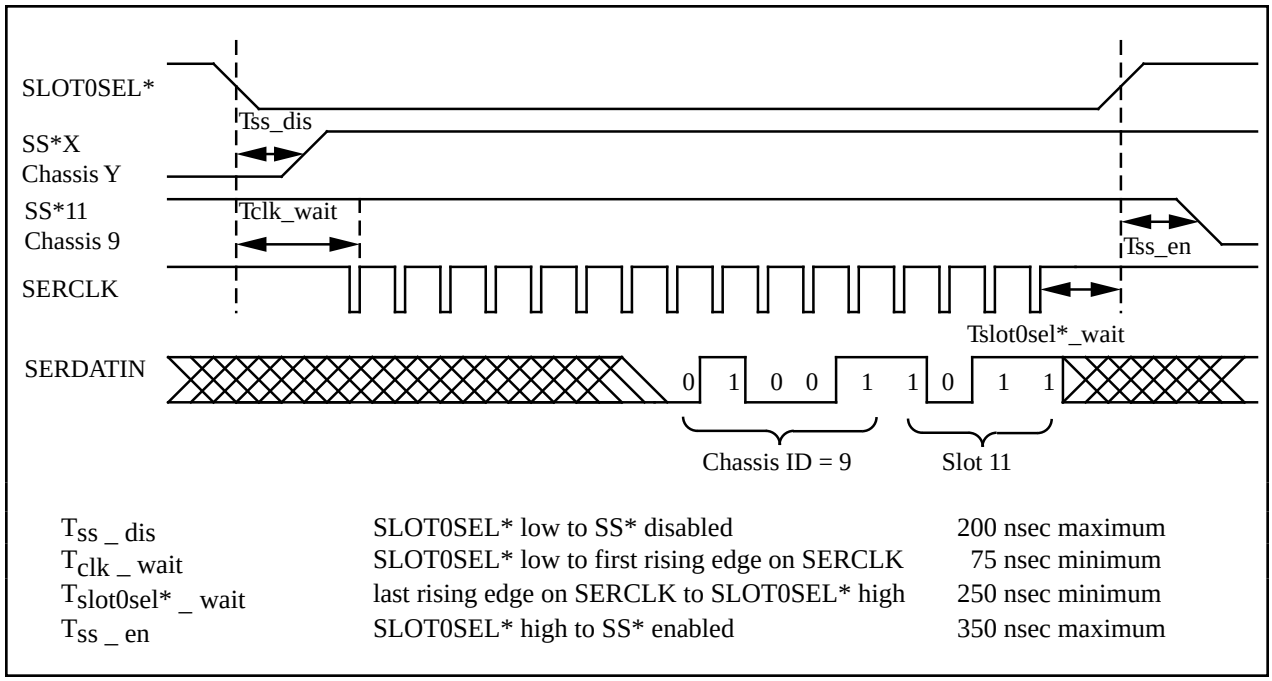
3. For each bit, starting with the most significant bit, set the bits as follows:

   a. SERDATIN = bit to be sent. These bits are the data that is being written to the Slot-Select Register.

   b. SERCLK = 0

   c. SERCLK = 1. This rising edge clocks the data. If you are using an MIO-16 board, a write to the EXTSTROBE Register will cause EXTSTROBE* to pulse low, thus accomplishing steps b and c.

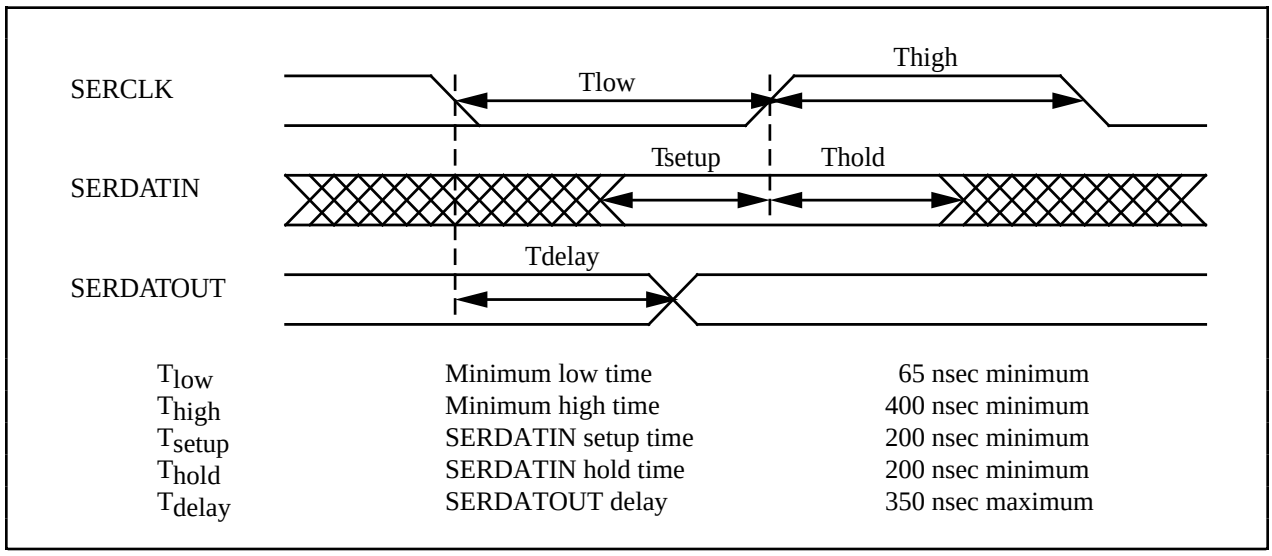
4. Set SLOT0SEL* to 1 to assert the SS* line of the module whose slot number was written to Slot 0. If you are using multiple chassis, only the appropriate slot in the chassis whose address corresponds to the written chassis number will be selected. When no communication is taking place between the data acquisition board and any modules, it is recommended that you write zero to the Slot-Select Register to ensure that no accidental writes occur.



T_{ss_dis}	SLOT0SEL* low to SS* disabled	200 nsec maximum
T_{clk_wait}	SLOT0SEL* low to first rising edge on SERCLK	75 nsec minimum
$T_{slot0sel*_wait}$	last rising edge on SERCLK to SLOT0SEL* high	250 nsec minimum
T_{ss_en}	SLOT0SEL* high to SS* enabled	350 nsec maximum

Figure 2-18. Slot-Select Timing Diagram

Figure 2-19 shows the timing requirements on the SERCLK and SERDATIN signals. These requirements must be observed for all communications. T_{delay} is a SCXI-1140 specification.



T_{low}	Minimum low time	65 nsec minimum
T_{high}	Minimum high time	400 nsec minimum
T_{setup}	SERDATIN setup time	200 nsec minimum
T_{hold}	SERDATIN hold time	200 nsec minimum
T_{delay}	SERDATOUT delay	350 nsec maximum

Figure 2-19. Serial Data Timing Diagram

After the Slot-Select line to an SCXI-1140 has been asserted, you can write to its Configuration Register and read its Module ID Register by using the protocols of the following. After the 32 bits of data are read from the Module ID Register, further data will be zeros until reinitialization occurs. Deassert Slot-Select to reinitialize the contents of the Module ID Register.

To write to the Configuration Register, follow these steps:

1. Initial conditions:

   SS* asserted low.
   SERDATIN = don't care.
   DAQD*/A = 0 (indicates data will be written to the Configuration Register).
   SLOT0SEL* = 1.
   SERCLK = 1 (and has not changed since SS* went low).

2. For each bit, starting with the MSB, perform the following action:

   a. Set SERDATIN = bit to be sent. These bits are the data that is being written to the Configuration Register.

   b. Clear SERCLK = 0

   c. Set SERCLK = 1. This rising edge clocks the data. If you are using an MIO-16, a write to the EXTSTROBE Register causes EXTSTROBE* to pulse low, thus accomplishing steps b and c.

3. Pull SLOT0SEL* low to deassert the SS* line and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.

4. If another slot will not be selected, it is recommended that you write zero to the Slot 0 Slot-Select Register.

Figure 2-20 illustrates a write to the SCXI-1140 Configuration Register of the binary pattern:

```
00000001 01010000 00010001 10100111
```

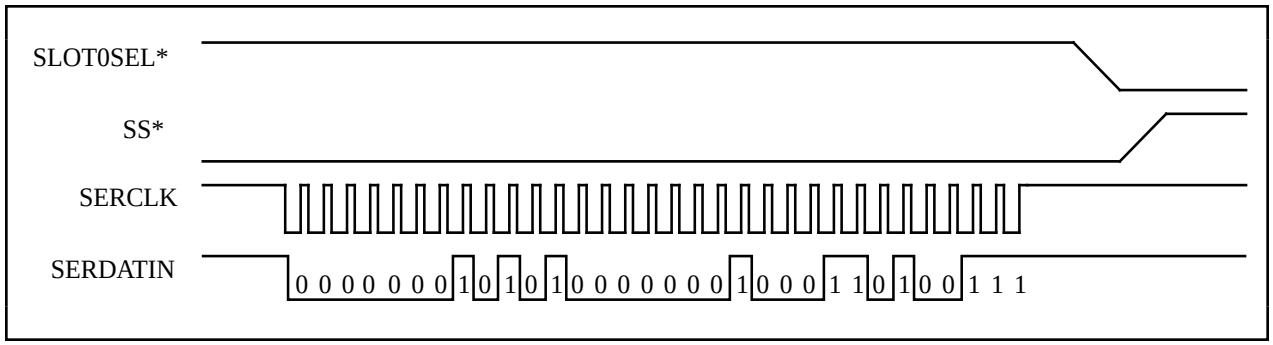


Figure 2-20. Configuration Register Write Timing Diagram

To read from the Module ID Register, follow these steps:

1. Initial conditions:

   SS* asserted low.
   SERDATIN = don't care.
   DAQD*/A = 1. Make sure DAQD*/A does not go low or erroneous data will be written to the Configuration Register.
   SLOT0SEL* = 1.
   SERCLK = 1 (and has not changed since SS* went low).

2. For each bit to be read:

   a. Clear SERCLK = 0

   b. Set SERCLK = 1. Clock the data. If you are using an MIO-16 board, a write to the EXTSTROBE Register will cause EXTSTROBE* to pulse low, thus accomplishing steps b and c.

   c. Read the level of the SERDATOUT line.

3. Pull SLOT0SEL* low to deassert the SS* line and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.

4. If you are not selecting another slot, write zero to the Slot 0 Slot-Select Register.

Figure 2-21 illustrates a read of the SCXI-1140 Module ID Register.

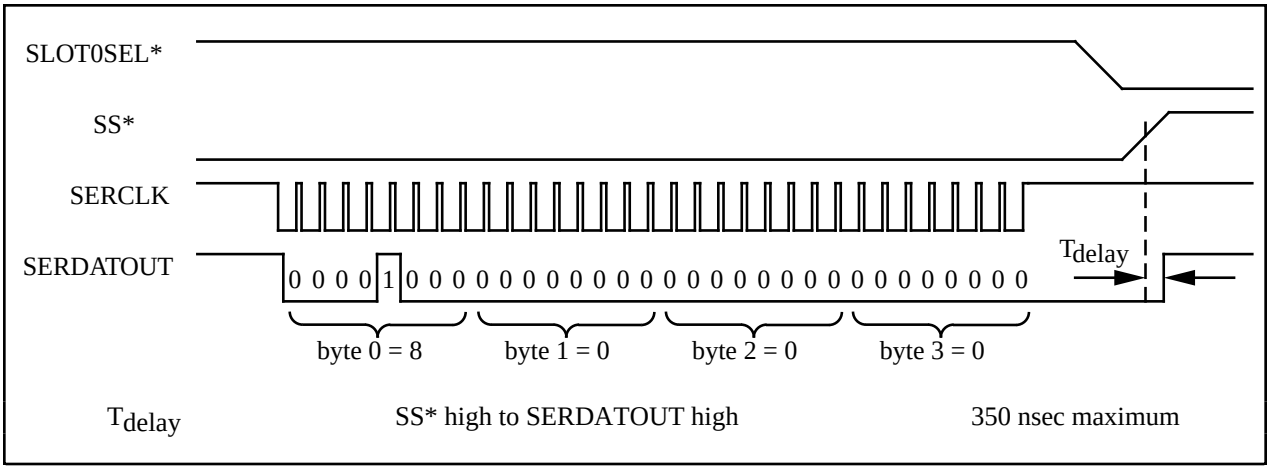


Figure 2-21. SCXI-1140 Module ID Register Timing Diagram

For further details on programming these signals, refer to Chapter 5, *Programming*.

Chapter 3
Theory of Operation

This chapter contains a functional overview of the SCXI-1140 module and explains the operation of each functional unit making up the SCXI-1140.

Functional Overview

The SCXI-1140 consists of eight channels, each one comprising an instrumentation amplifier with DIP switch-programmable gains of 1, 10, 100, 200, 300, 500, 600, 700, or 800, and a track-and-hold amplifier. The analog inputs are overvoltage protected. All eight channels are placed in Hold mode simultaneously. Internal counters are used for automatic scanning. You can operate multiple SCXI-1140 boards under SCXIbus control or directly from a data acquisition board. The outputs of all eight channels are available at the output connector. You can also multiplex the outputs onto a single channel. You can use SCXI-1140 switches to connect other SCXI-1140 outputs to the same channel over the analog bus.

The block diagram in Figure 3-1 illustrates the key functional components of the SCXI-1140. The major components of the SCXI-1140 are the digital interface, the timing control circuitry, the track-and-hold circuitry, and the analog circuitry.

The theory of operation of each of these components is explained in the remainder of this chapter.

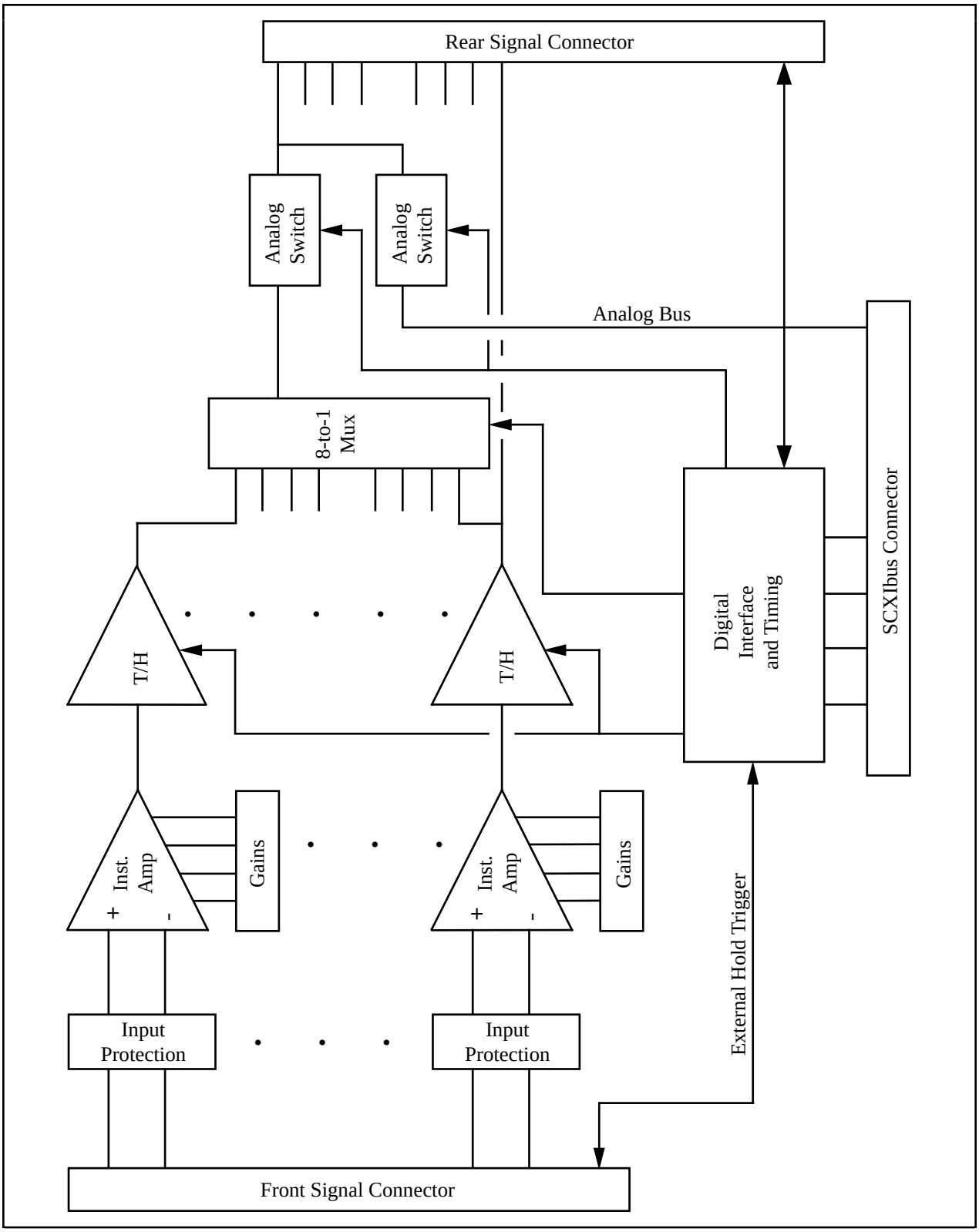


Figure 3-1. SCXI-1140 Block Diagram

Digital Interface

The block diagram in Figure 3-2 illustrates the digital interface circuitry of the SCXI-1140.

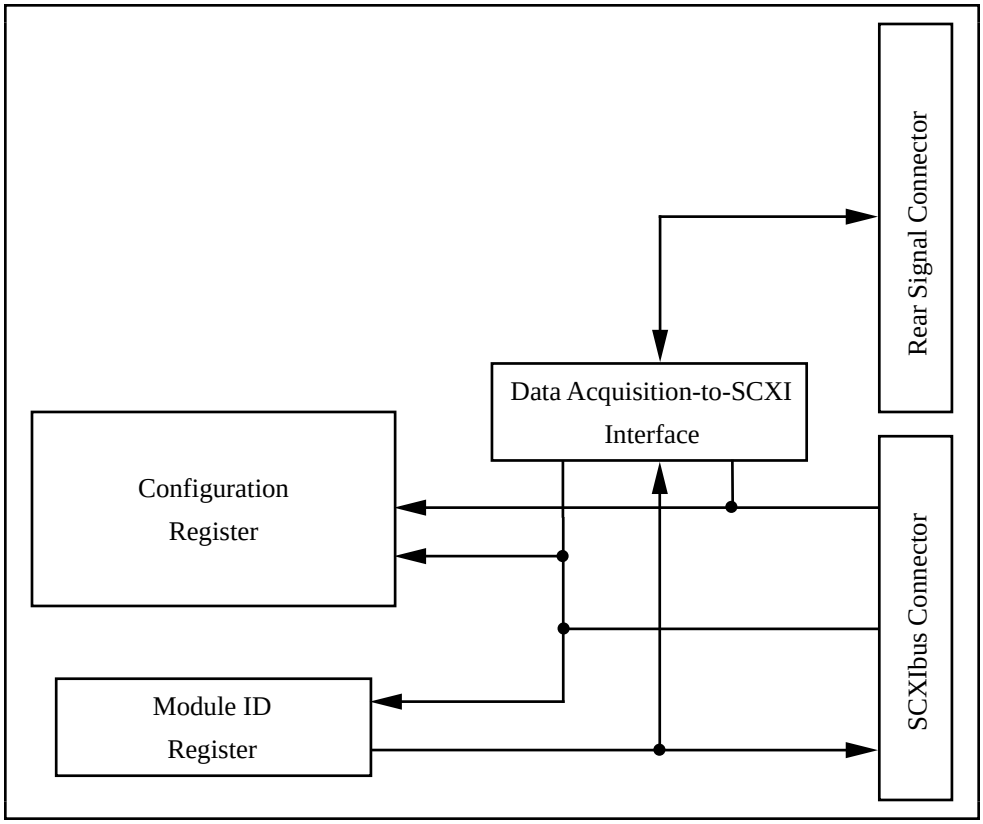


Figure 3-2. SCXI-1140 Digital Interface Circuitry Block Diagram

The digital interface circuitry is divided into five main sections–the SCXIbus connector, the rear signal connector, the data acquisition-to-SCXI interface, the Configuration Register, and the Module ID Register.

SCXIbus Connector

The SCXI-1140 connects to the SCXIbus via a triple 4x6 metral receptacle. Figure 3-3 shows the pin assignment for the SCXI-1140 SCXIbus connector.

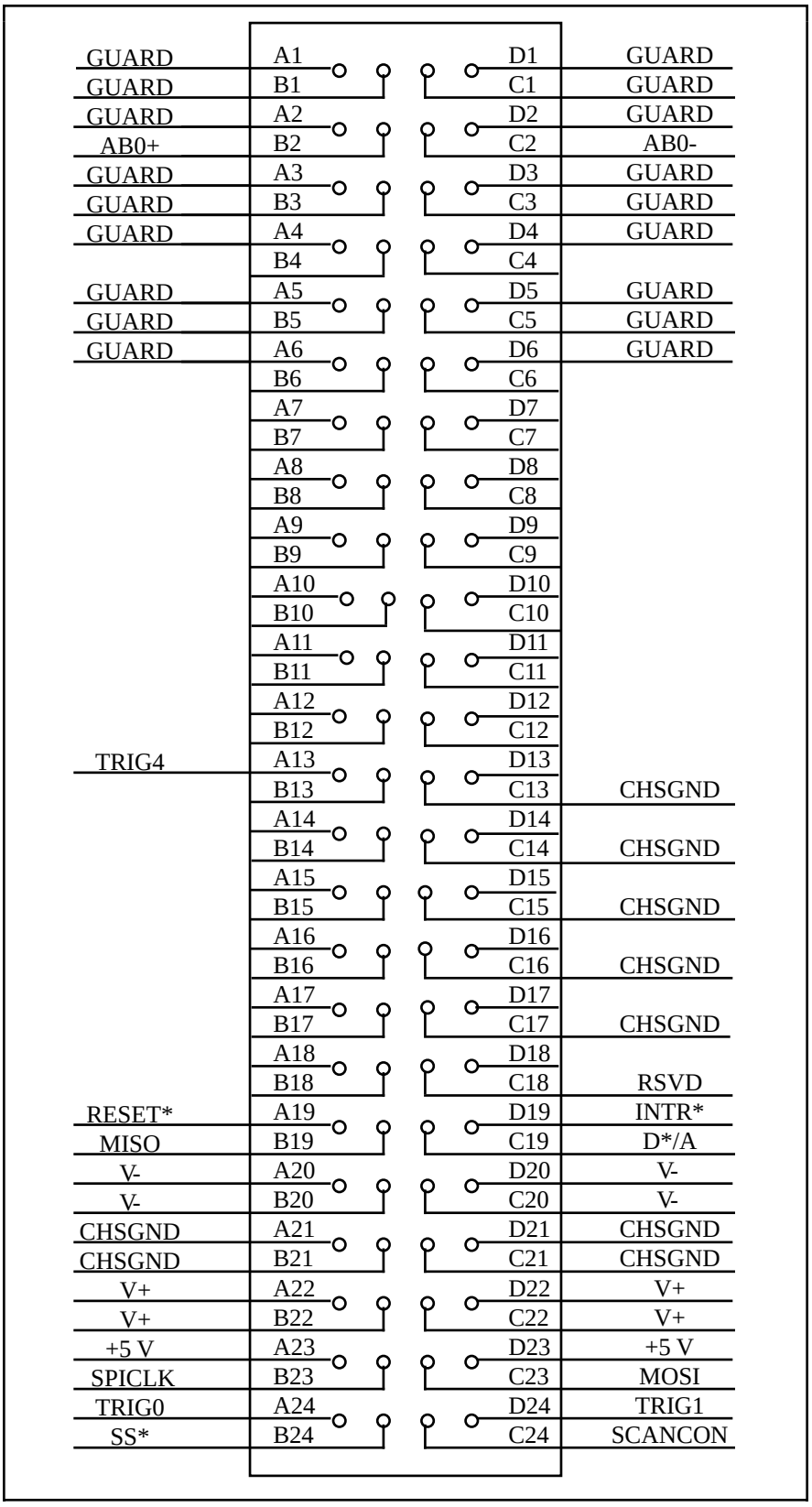


Figure 3-3. SCXI-1140 SCXIbus Connector Pin Assignment

SCXIbus Connector Signal Descriptions

Pin	Signal Name	Description
B2	AB0+	Analog Bus 0+ – Positive analog bus 0 line. Used to multiplex several modules to one analog signal.
C2	AB0-	Analog Bus 0- – Negative analog bus 0 line. Used to multiplex several modules to one analog signal.
A1, B1, C1, D1, A2, B2, C2, D2, A3, B3, C3, D3, A5, B5, C5, D5, A4, D4, A6, D6	GUARD	Guard – Shields, guards the analog bus lines from noise.
C13-C17, A21, B21, C21, D21	CHSGND	Chassis Ground – Digital and analog ground reference.
A13	TRIG4	TRIG4 – Reserved. Open collector.
C18	RSVD	Reserved.
A19	RESET*	Reset – When pulled low, reinitializes the module to its power-up state. Totem pole. Input.
B19	MISO	Master-In Slave-Out – Transmits data from the module to the SCXIbus. Open collector. I/O.
C19	D*/A	Data/Address – Indicates to the module whether address information or data information is being sent to the module on MOSI. Open collector. I/O.
D19	INTR*	Interrupt – (active low) Causes data that is on MOSI to be written to the Slot-Select Register in Slot 0. Open collector. Output.
A20, B20, C20, D20	V-	Negative Analog Supply – -18.5 to -25 V.
A22, B22, C22, D22	V+	Positive Analog Supply – +18.5 to +25 V.
A23, D23	+5 V	+5 VDC Source – Digital power supply.
B23	SPICLK	Serial Peripheral Interface (SPI) Clock – Clocks the serial data on the MOSI and MISO lines. Open collector. I/O.
C23	MOSI	Master-Out Slave-In – Transmits data from the SCXIbus to the module. Open collector. I/O.

Pin	Signal Name	Description (continued)
TRIG0	A24	TRIG0 – General-purpose trigger line used by the SCXI-1140 to send SCANCLK to other modules or receive SCANCLK from other modules. Open collector. I/O.
B24	SS*	Slot Select – When low, enables module communications over the SCXIbus. Totem pole. Input.
C24	SCANCON	Scanning Control – Combination output enable and reload signal for scanning operations. Each module in a chassis receives a separate SCANCON. Totem pole. Input.
D24	TRIG1	TRIG1 – Can be used to synchronize several SCXI-1140s in the same chassis by forcing them to go into Hold mode at the same time. Open collector. I/O.

MOSI, MISO, SPICLK, and SS* form a synchronous communication link that conforms with SPI, using an idle-high clock and second-edge data latching. D*/A, INTR*, and RESET* are additional control signals.

When you are using the module in an SCXI-1000 or SCXI-1001 chassis, the data acquisition board, via the module rear signal connector, must tap into the open collector backplane signal lines as a master to write to the module. Table 3-1 shows the signal connections from the rear signal connector to the backplane.

Table 3-1. SCXIbus Equivalents for the Rear Signal Connector

Rear Signal Connector Signal	SCXIbus Equivalent
SERDATIN	MOSI
DAQD*/A	D*/A
SLOT0SEL*	INTR* Jumper W11 must be set to position A-B
SERCLK	SPICLK
SERDATOUT	MISO Jumper W14 must be set to position A-B

In order for the data acquisition board to talk to a slot, the board must first assert the SS* for that slot. You do this by asserting INTR* low, writing a 16-bit number over MOSI, corresponding to the desired slot (and chassis if an SCXI-1001 chassis is being used), and then releasing INTR* high. At this point, SS* of the desired slot is asserted low and the data acquisition board can communicate with the module in that slot according to the SPI protocol.

Digital Control Circuitry

The digital control section consists of the Configuration Register and the Module ID Register.

The Configuration Register is a 32-bit serial-in, parallel-out shift register. Data is received on the MOSI line from either Slot 0 or the data acquisition board when SS* is enabled and D*/A indicates data transfer (D*/A low). Use the Configuration Register for channel selection and for configuring the SCXI-1140 for scanning and control options. Complete descriptions of the register bits are given in Chapter 5, *Programming*. Writes to the Configuration Register consist of the following steps:

1. SS* goes low, enabling communication with the board.
2. D*/A goes low, indicating that the information sent on the MOSI line is data.
3. The serial data is available on MOSI; SPICLK clocks it into the register.
4. SS* goes high and D*/A goes high, indicating an end of communication. This action latches the Configuration Register bits.

When you reset the SCXIbus, all bits in the Configuration Register are cleared.

The Module ID Register connects to MISO on the SCXIbus. The Module ID Register is an eight-bit parallel-in, serial-out shift register and an SPI communication adapter. The contents of the Module ID Register are written onto MISO during the first four bytes of transfer after SS* has been asserted low. Zeros are written to MISO thereafter until SS* is released and reasserted. The SCXI-1140 module ID is hex 00000008.

Timing Control Circuitry

Figure 3-4 illustrates the timing control circuitry, which consists of the multiplexer addressing circuitry and the track-and-hold control circuitry.

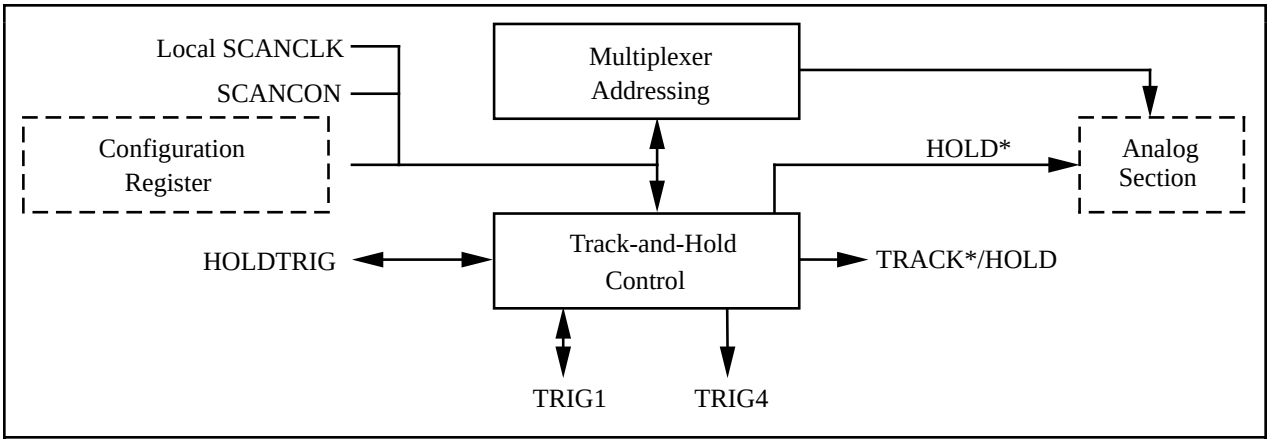


Figure 3-4. SCXI-1140 Timing Control Circuitry Block Diagram

Multiplexer Addressing

The two output modes for the SCXI-1140 are Parallel mode and Multiplexed mode. In Parallel mode, set the output multiplexer to Channel 0 to disable scanning. Thus, all eight outputs become available simultaneously on the rear signal connector. In Multiplexed mode, only one output is used. All eight channel outputs are multiplexed into the one board output that is under hardware control.

The SCXI-1140 powers up in Parallel mode. To place the module in Parallel mode, you must clear the SCAN, FOUTEN*, and AB0EN bits in the Configuration Register. You also must set CHAN<2..0> in the Configuration Register to 000. Clearing the SCAN bits prevents the channel multiplexer from scanning; clearing the FOUTEN* bit enables the multiplexer output; clearing the AB0EN bit ensures that the multiplexer output is disconnected from the SCXIbus; and setting CHAN<2..0> to 000 sets the multiplexer reload channel to 0. Because writing to the Configuration Register automatically loads the multiplexer with CHAN<2..0>, Channel 0 will appear at the multiplexed output. The other seven outputs are always directly available at the rear signal connector.

Multiplexed mode facilitates multimodule operation and uses fewer data acquisition board channels. This mode, however, requires more care with regard to programming and timing.

The local SCANCLK signal increments the output multiplexer, provided you have set the SCAN bit in the Configuration Register. There is no local SCANCLK if SCANCLKEN* is set, so you should clear SCANCLKEN*. This is the power-up condition. The local SCANCLK will be either SCANCLK from the rear signal connector or TRIG0 from the SCXIbus connector, depending on the state of the CLKSELECT bit in the Configuration Register. TRIG0 may be driven with the local SCANCLK if SCANCLKEN* is coming from the rear signal connector and if the CLKOUTEN bit in the Configuration Register is set. Using TRIG0, several modules in one chassis can access SCANCLK from only one rear signal connector.

You can reload the output multiplexer by one of the following events:

- At power up or board reset
- Assertion of the SCXIbus SS* signal; that is, any access to the module
- A high level on SCANCON on the SCXIbus connector, if you set the SCANCONEN bit in the Configuration Register. The output multiplexer will be reloaded to the channel specified by CHAN<2..0> in the Configuration Register.

The module output is enabled if either the FOUTEN* bit in the Configuration Register is cleared or SCANCON on the SCXIbus connector is low. Each module in a chassis receives a separate SCANCON, each of which is under the control of Slot 0. Set the AB0EN bit in the Configuration Registers of all the modules involved to perform multimodule scanning. This configuration connects all of the multiplexed module outputs in parallel through the SCXIbus backplane. Slot 0 then asserts the SCANCON of each module independently to select one module at a time during scanning.

For more information on multiplexer addressing, see the *Scanning Modes* section later in this chapter, and Chapter 5, *Programming.*

Track-and-Hold Control Circuitry

Figure 3-5 illustrates the SCXI-1140 track-and-hold control circuitry. Each block is described in the following paragraphs.

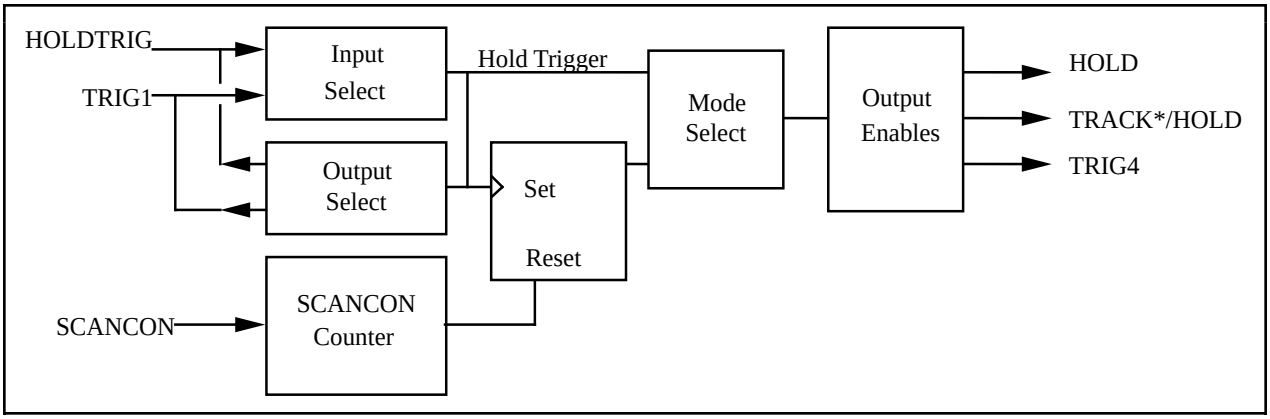


Figure 3-5. SCXI-1140 Track-and-Hold Control

The two primary modes of operation of the track-and-hold control circuitry are Edge-Triggered mode and Level-Sensitive mode. In Edge-Triggered mode, the module is placed into Hold mode on the rising edge of the Hold Trigger signal. The module is placed back into Track mode when the SCANCON counter has counted down to zero. In Level-Sensitive mode, the Hold Trigger signal becomes the HOLD signal for the module; when the selected Hold Trigger signal is high, the module is in Hold mode, and when it is low, the module is in Track mode. Level-Sensitive mode is the power up and reset condition.

The source of the Hold Trigger signal is software selectable, and can either be the HOLDTRIG signal from the front or rear signal connector, or the inverse of TRIG1 from the SCXIbus connector. The Hold Trigger signal can be sent out by the HOLDTRIG pins of the signal connectors, or onto TRIG1 in inverted form. The HOLDTRIG and TRIG1 I/O select circuitry powers up and resets so that HOLDTRIG is selected as an input and no other signal is selected as an output. Hardware prevents both signals from being selected as inputs and either signal being both input and output.

TRACK*/HOLD, which connects to the rear signal connector, and TRIG4, which connects to the SCXIbus connector, power up and reset in the disabled state. You can enable TRACK*/HOLD and TRIG4 as a replica of the HOLD signal, which directly controls the track-and-hold circuits in the analog section.

The SCANCON counter, whose activity is relevant only in Edge-Triggered mode, counts the number of SCANCON pulses. All modules being scanned enter Hold mode on the rising edge of their Hold Trigger signals, all of which should be the same. After the designated number of SCANCON pulses for a module, the module goes back into Track mode. For most applications, the count value of the SCANCON counter should be one.

Analog Circuitry

The SCXIbus provides analog power (±18.5 VDC minimum), which the SCXI-1140 regulates to ±15 VDC, a chassis ground (CHSGND), and an analog bus (AB0±) with a guard. AB0± buses the SCXI-1140 output to other modules via the SCXIbus. The guard guards the analog bus and you can connect it via jumper W12 to the chassis ground, to the data acquisition board input ground (AIGND), or leave floating (for example, if you make the connection on another board). Figure 3-6 illustrates the analog circuitry.

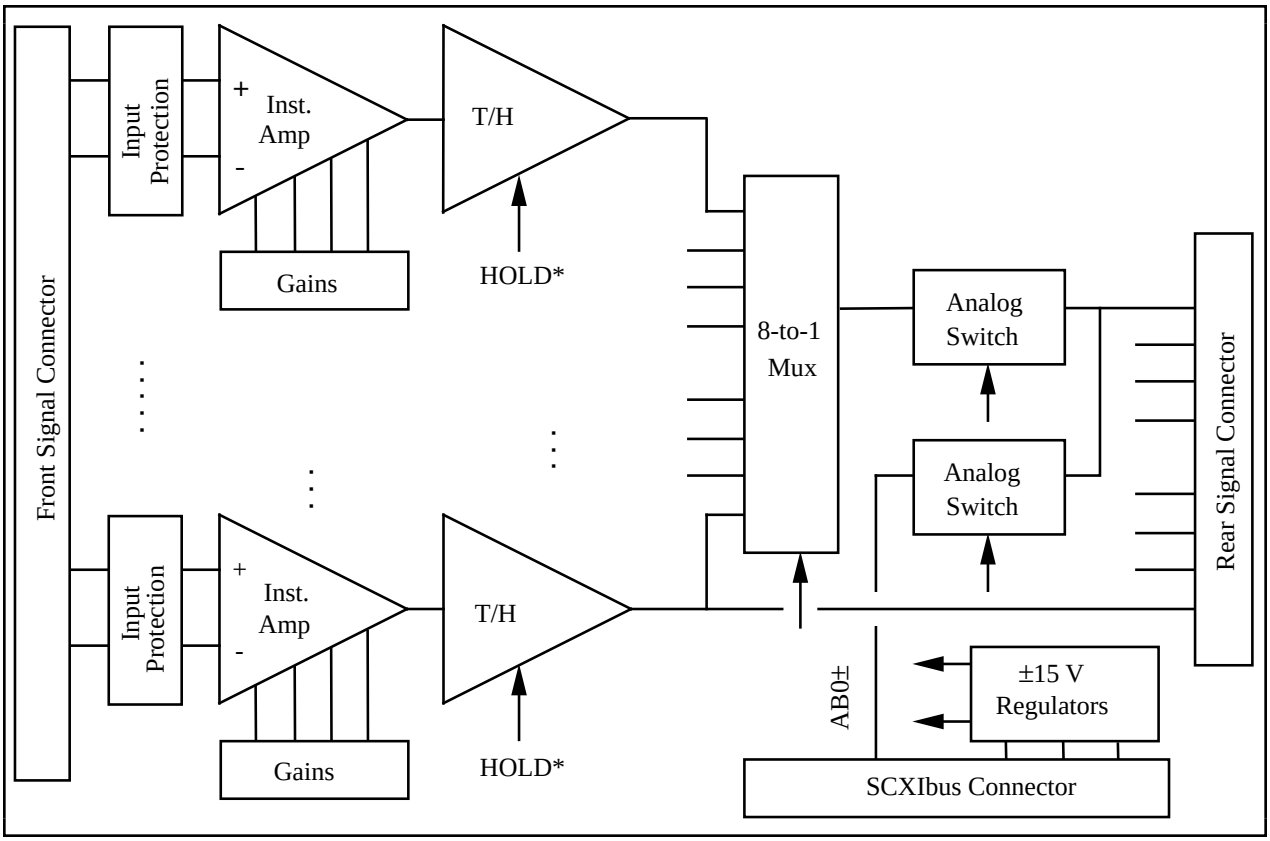


Figure 3-6. SCXI-1140 Analog Circuitry

The analog input circuitry consists of eight channels with DIP switch-programmable instrumentation amplifiers followed by buffered track-and-hold amplifiers, an eight-to-one multiplexer, and output switches. In addition, you can include the voltage-regulation circuitry and input protection in the analog section. Each block is described in the following paragraphs.

The first block an incoming analog signal encounters is the input protection. The input protection consists of a 1 kΩ resistor in series with each input line followed by low-leakage diodes to the supply rails (±15 V). Each input terminal is protected against input voltages up to ±15 V powered off and ±30 V powered on.

Next in the signal path are the instrumentation amplifiers, which fulfill two purposes on the SCXI-1140 module. First, the instrumentation amplifiers convert differential input signals into single-ended signals referred to the SCXI-1140 ground for input common-mode signal rejection. With this conversion, you can extract the analog input signals from common-mode noise voltages before the data acquisition board samples and converts the signals. Second, the instrumentation amplifiers amplify input signals, resulting in an increase in measurement resolution and accuracy. Furthermore, the amplifiers exhibit low bias currents and good bandwidth, even at high gains. You can select gains for each channel independently with separate DIP switches. Gains are 1, 10, 100, 200, and 500, although gains of 300, 600, 700, and 800 are available with reduced accuracy. See Appendix A, *Specifications,* for details on the performance of the instrumentation amplifiers.

The track-and-hold amplifiers operate as simple buffers when in Track mode, but freeze their outputs when placed into Hold mode. Because all of the track-and-hold amplifiers in each SCXI-1140 module enter Hold mode at the same time, they implement simultaneous sampling of all channels. Simultaneous sampling is useful for preserving phase relationships between channels. Track-and-hold amplifiers are subject to various imperfections, which are listed in Appendix A, *Specifications*. The track-and-hold amplifiers on the SCXI-1140 exhibit a droop rate of about 10 mV/sec, which means that the output of the track-and-hold amplifier changes about 10 mV for every second that the amplifier is in Hold mode. If the data acquisition board you use has a throughput of 50 kHz, a 10 V input range, and 12-bit resolution, theoretically you could scan up to 5,000 channels with only half an LSB of error introduced by the track-and-hold amplifiers. The present practical limit on channel count using an MIO-16 board is determined by the following calculation:

8 channels/module x 12 modules/chassis x 8 chassis/data acquisition board =
768 channels/data acquisition board

The output of every channel is connected to a multiplexer whose output connects, through switches and a buffer, to the rear signal connector. The multiplexer control is described in the *Multiplexer Addressing* section earlier in this chapter. The analog switches connect the multiplexed module output to and from the SCXIbus analog bus. Use these switches when multiplexing the outputs of several modules. In this case, all the module AB0 switches are closed while the output multiplexers of all of the modules except the one being read are disabled. Refer to Chapter 5, *Programming*, for more information on how to program and configure multiple modules. When you set the multiplexer to Channel 0 and disable the analog bus, the outputs of all eight channels are simultaneously available on the rear signal connector. This configuration is useful in stand-alone applications in which programming is difficult or impossible. The module is useful even without programming in those cases because the module powers up and resets to the parallel-output configuration. The SCXI-1140 outputs are short-circuit protected but are not overvoltage protected.

The SCXIbus provides power to each module in the ±18.5 to ±25 V range. The SCXI-1140 regulates the power to ±15 V. The outputs of the regulators are clamped so that the overvoltage protection circuitry works properly without interfering with the voltages on the bus.

Scanning Modes

The SCXI-1140 module has four basic types of scanning modes–single-module parallel scanning, single-module multiplexed scanning, multiple-module multiplexed scanning, and multiple-chassis scanning, which is possible only with the SCXI-1001 chassis. Only with the MIO-16 data acquisition boards can you scan the SCXI-1140. For additional information,

consult either Chapter 2, *Configuration and Installation*, Chapter 5, *Programming*, your data acquisition board user manual, or your SCXI chassis user manual. If you need more information, contact National Instruments.

During scanning, a module sends the SCANCLK signal to Slot 0 over the SCXIbus TRIG0 line, and Slot 0 sends the SCANCON signal to the modules. In Multiplexed mode, this timing signal reloads the output multiplexer and determines when the SCXI-1140 output is enabled. In Multiplexed or Parallel mode, when the Hold Trigger signal is in Edge-Triggered mode, the SCANCON signal is also counted on the module to determine when to go back into Track mode. Slot 0 contains a module scan list first-in first-out (FIFO) memory chip. The memory chip is similar to the Channel and Gain FIFO on an MIO-16 board, except that instead of having a channel number and gain setting for each entry, the scan list contains a slot number and a sample count for each entry. The list in Slot 0 determines which module is being accessed and for how many samples. Make sure that the lists on the data acquisition board and Slot 0 are compatible so that the samples are acquired as you intend. See your *SCXI-1000/1001 User Manual* for more information.

In either Parallel or Multiplexed scanning mode, you need a source for the HOLDTRIG source. Typically, the data acquisition board supplies the signal when you use Interval-Scanning mode. See Chapter 5, *Programming*, for more information on Interval-Scanning mode. The HOLDTRIG signal can also be supplied at the front connector of the SCXI-1140 and sent out the HOLDTRIG pin of the rear signal connector to the data acquisition board to trigger each scan interval. Notice that if you use SCXI-1140s in conjunction with other modules, the module that is cabled to the data acquisition board must be an SCXI-1140 or must have the ability to route the HOLDTRIG signal to and from the SCXIbus TRIG1 line from or to the HOLDTRIG rear signal connector pin.

Single-Module Parallel Scanning

Single-Module Parallel Scanning is the simplest scanning mode. Cable the SCXI-1140 directly to the data acquisition board as shown in Figure 3-7; each analog signal has its own channel. Either the data acquisition board or the front connector can supply the HOLDTRIG signal. If you configure the Hold Trigger in Edge-Triggered mode, the module must send SCANCLK over TRIG0 to Slot 0 and count the pulses of the SCANCON signal to determine when to go back into Track mode.

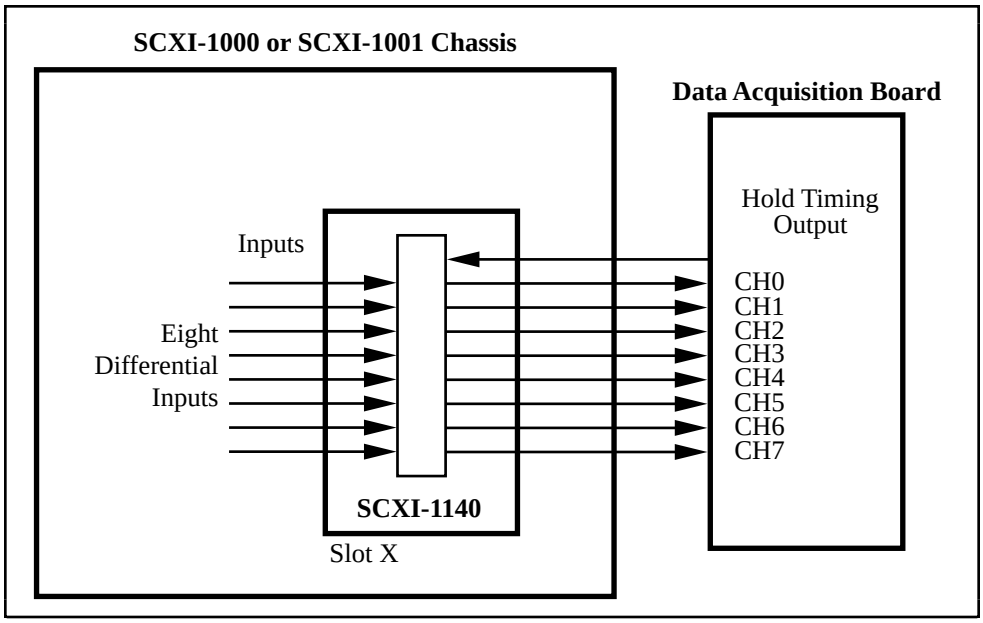


Figure 3-7. Single-Module Parallel Scanning

Single-Module Multiplexed Scanning

Single-Module Multiplexed Scanning (Direct)

Direct Single-Module Multiplexed Scanning is the simplest multiplexed scanning mode. Cable the SCXI-1140 directly to the data acquisition board as shown in Figure 3-8. The module sends SCANCLK onto TRIG0 and Slot 0 sends SCANCON back to the module. SCANCON will be low at all times during the scan except during changes from one Slot 0 scan list entry to the next, when SCANCON pulses high to make the output multiplexer reload its starting channel. Although you are only using a single module, you can put many entries in the Slot 0 FIFO with different counts, so that some channels are read more often than others. You cannot change the start channel in the module Configuration Register during a scan. Either the data acquisition board or the front connector can supply the HOLDTRIG signal.

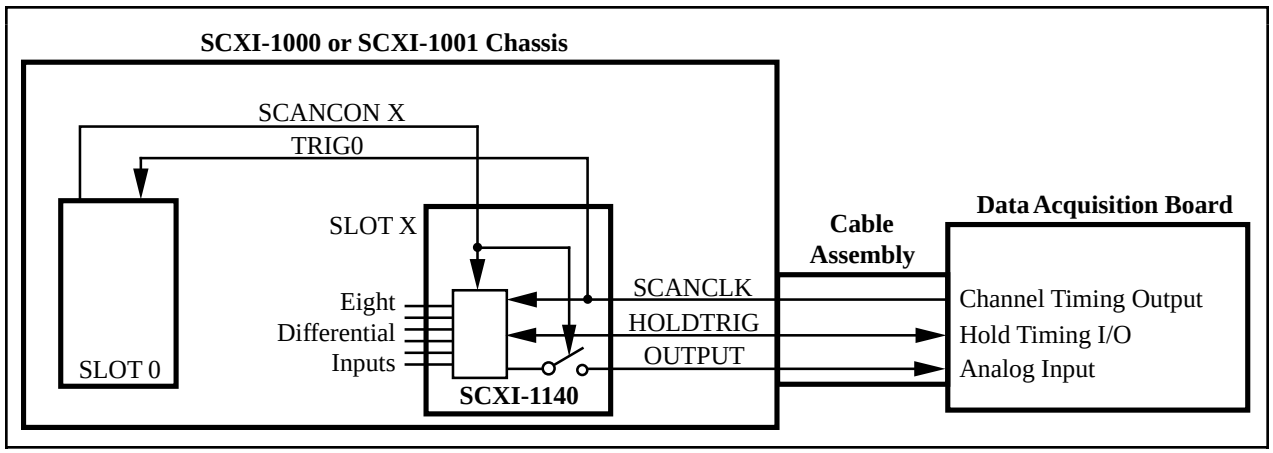


Figure 3-8. Single-Module Multiplexed Scanning (Direct)

Single-Module Multiplexed Scanning (Indirect)

In this mode, you do not cable the SCXI-1140 directly to the data acquisition board. Instead, you cable another module to the data acquisition board, and the analog output of the SCXI-1140 is sent over Analog Bus 0, through the intermediate module, and then to the data acquisition board. The output multiplexer clock is received from TRIG0, having been sent there by the intermediate module, as shown in Figure 3-9. Either the data acquisition board or the front connector can supply the HOLDTRIG signal. The HOLDTRIG signal is bused on TRIG1 of the SCXIbus. Slot 0 operation is the same as in the direct connection case.

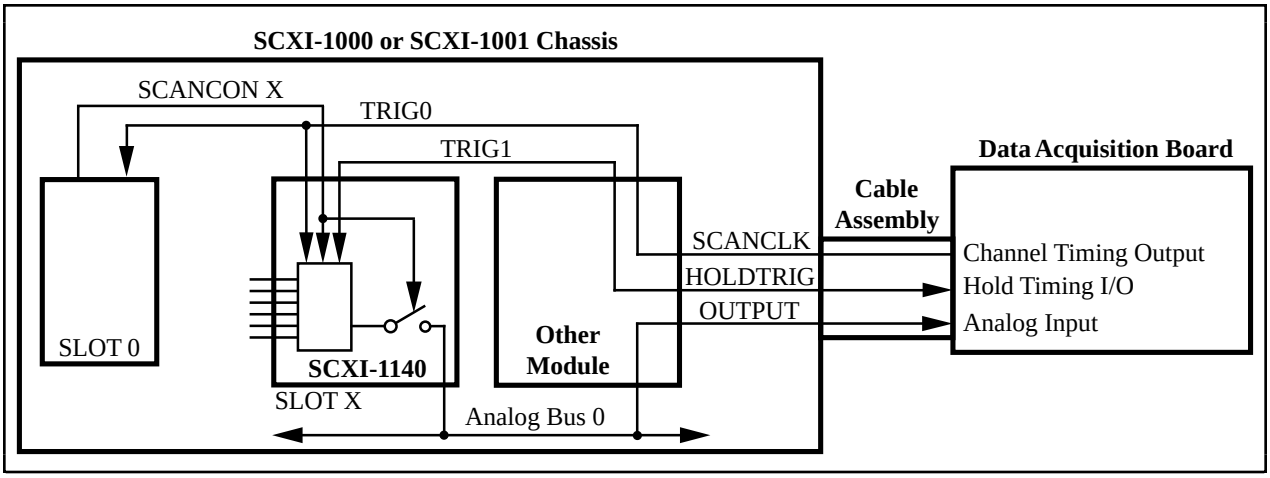


Figure 3-9. Single-Module Multiplexed Scanning (Indirect)

Multiple-Module Multiplexed Scanning

In this mode, all of the modules tie into Analog Bus 0, and SCANCON enables the output of their amplifiers. The module that is directly cabled to the data acquisition board sends SCANCLK onto TRIG0 for the other modules and Slot 0, as shown in Figure 3-10. Either the data acquisition board or the front connector of one of the modules can supply the HOLDTRIG signal. The HOLDTRIG signal is bused on TRIG1 of the SCXIbus. Program the scan list in Slot 0 of one of the modules with the sequence of modules and the number of samples per entry.

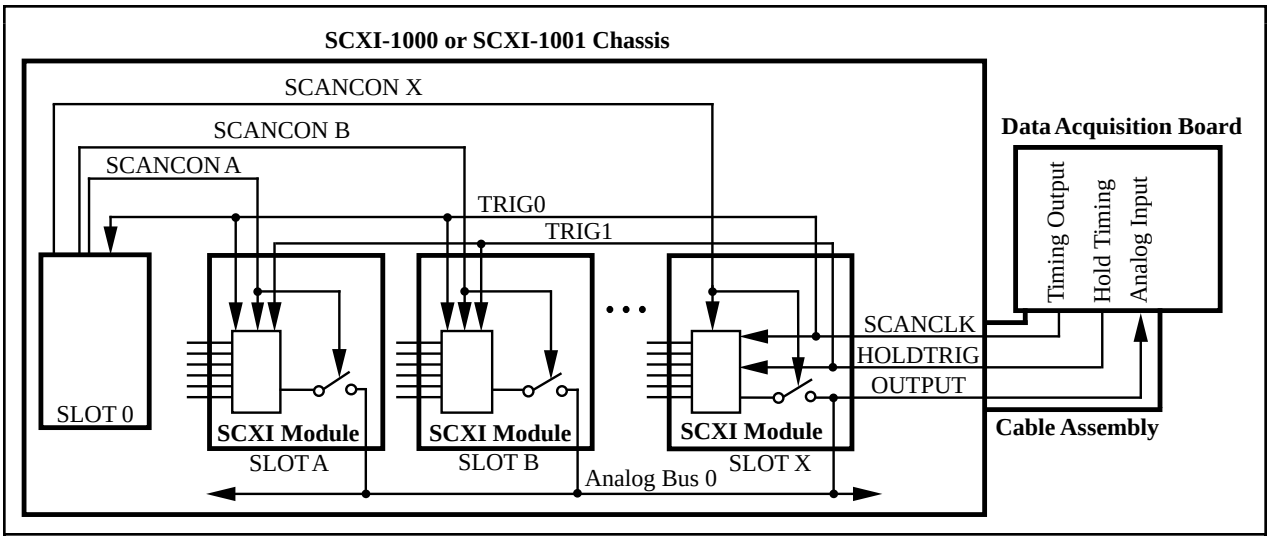


Figure 3-10. Multiple-Module Multiplexed Scanning

Multiple-Chassis Scanning

In Multiple-Chassis Scanning mode, you attach each chassis to a daisy chain of cable assemblies and multichassis adapter boards, as shown in Figure 3-11. Program each chassis separately; each occupies a dedicated channel of the data acquisition board. Either the data acquisition board or the front connector of one of the modules can supply the HOLDTRIG signal. The HOLDTRIG signal is sent to all chassis over the HOLDTRIG line of the cable assemblies, and is bused on TRIG1 within each chassis. Within each chassis, scanning operations act as if the other chassis are not being used, with one exception. To keep the chassis synchronized, you must program the Slot 0 scan list in each chassis with dummy entries of Slot 13 to fill the samples when the data acquisition board will be sampling another chassis or data acquisition board channel. You can only perform multiple-chassis scanning with the SCXI-1001 chassis and MIO-16 data acquisition boards. See Chapter 5, *Programming*, for more information on multiple-chassis scanning. See Appendix E, *SCXI-1140 Cabling*, for more information on the necessary cable accessories for multichassis scanning.

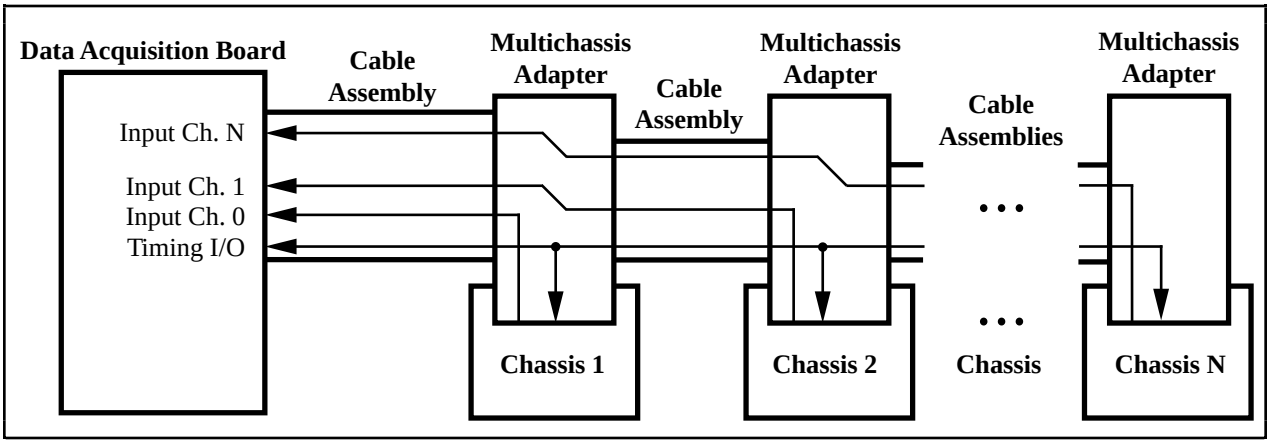


Figure 3-11. Multiple-Chassis Scanning

Chapter 4
Register Descriptions

This chapter describes in detail the SCXI-1140 Configuration Register, the Module ID Register, and the Slot 0 registers.

Note: If you plan to use a programming software package such as NI-DAQ for DOS/Windows, NI-DAQ for Macintosh, LabWindows, or LabVIEW with your SCXI-1140 module, you do not need to read this chapter.

Register Description

Register Description Format

This register description chapter discusses the SCXI-1140 registers and the Slot 0 registers. A detailed bit description of each register is given. The individual register description gives the type, word size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the MSB shown on the left (bit 31 for a 32-bit register, bit 15 for a 16-bit register, and bit 7 for an 8-bit register) and the LSB shown on the right (bit 0). A rectangle is used to represent each bit. Each bit is labeled with a name inside its rectangle. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic). The Module ID register has a unique format and is described in the *Module ID Register* section.

In many of the registers, several bits are labeled with an X, indicating don't care bits. When you write to a register, you may set or clear these bits without effect.

SCXI-1140 Registers

The SCXI-1140 has two registers. The Module ID register is a four-byte read-only register that contains the Module ID number of the SCXI-1140. The Configuration Register is a 32-bit write-only register that controls the functions and characteristics of the SCXI-1140.

Module ID Register

The Module ID Register contains the four-byte module ID code for the SCXI-1140. This code number is read as the first four bytes on the MISO line whenever the module is accessed. The bytes appear least significant byte first. Within each byte, data is sent out MSB first. Additional data transfers result in all zeros being sent on the MISO line. The Module ID Register is reinitialized to its original value each time the SCXI-1140 is deselected by the SS* signal on the backplane. The SCXI-1140 Module ID is eight.

Type: Read-only

Word Size: Four-byte

Bit Map:

Byte 0

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0

Byte 1

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Byte 2

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Byte 3

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Configuration Register

The Configuration Register contains 32 bits that control the functions of the SCXI-1140. When SS* is asserted (low) and D*/A indicates data (low), the register shifts in the data present on the MOSI line, bit 31 first, and then latches the data when the SCXI-1140 is deselected by the SS* signal on the backplane. The Configuration Register initializes to all zeros when you first turn on or reset the SCXI chassis.

Type: Write-only

Word Size: 32-bit

Bit Map:

31	30	29	28	27	26	25	24
SCCT7	SCCT6	SCCT5	SCCT4	SCCT3	SCCT2	SCCT1	SCCT0
23	22	21	20	19	18	17	16
X	CHAN2	CHAN1	CHAN0	X	X	X	X
15	14	13	12	11	10	9	8
X	RSVD	TRACK*/ HOLDEN	LEVEL*/ EDGE	HTRIGINEN*	HTRIGOUTEN	TRIG1INEN	TRIG1OUTEN
7	6	5	4	3	2	1	0
CLKOUTEN	CLKSELECT	SCANEN	RSVD	SCANCLKEN*	SCANCONEN	AB0EN	FOUTEN*

Bit	Name	Description
31-24	SCCT<7..0>	Scan Control Count – Indicates how many SCANCON pulses (1 to 256) the module should count before returning to Track mode. Zero corresponds to 256. Scan Control Count is significant only when the module is in Edge-Triggered mode.
23, 19-15	X	Don't care bits – Unused.
22-20	CHAN<2..0>	Channel Select – Determine the channel number (zero to seven) that is loaded into the output multiplexer to determine the analog channel to be read during a single read, or the starting channel on the module for a scanned data acquisition. CHAN2 is the MSB.
14, 4	RSVD	Reserved – Should always be written to zero.
13	TRACK*/HOLDEN	Track/Hold Enable – Specifies whether the module HOLD signal is driven onto the TRACK*/HOLD line on the rear signal connector. If you set this bit, the TRACK*/HOLD line is driven. If you clear this bit, the TRACK*/HOLD line is not driven.

Bit	Name	Description (continued)
12	LEVEL*/EDGE	Level-Sensitive/Edge-Triggered Mode Control – If you clear this bit to zero, the module is level sensitive and will be in Hold mode when the selected Hold Trigger signal is high and in Track mode when the selected Hold Trigger signal is low. If you set the bit to one, the module becomes edge sensitive and enters Hold mode on the rising edge of the selected Hold Trigger signal and enters Track mode after the number of SCANCON pulses determined by SCCNT<7..0>.
11	HTRIGINEN*	HOLDTRIG Input Enable – Determines whether HOLDTRIG is selected as the Hold Trigger signal. When you clear this bit to zero, HOLDTRIG is the Hold Trigger signal. When this bit is set to one, HOLDTRIG is not the Hold Trigger signal.
10	HTRIGOUTEN	HOLDTRIG Output Enable – Determines whether the Hold Trigger signal is driven onto the HOLDTRIG pins. When you clear this bit to zero, the Hold Trigger signal is not driven onto the HOLDTRIG pins. When you set this bit to one, the Hold Trigger signal is driven onto the HOLDTRIG pins, unless HOLDTRIG is also selected as an input by HTRIGINEN*.
9	TRIG1INEN	TRIG1 Input Enable – Determines whether the inverse of SCXIbus TRIG1 signal is selected as the Hold Trigger signal. When you clear this bit to zero, TRIG1 is not selected as the Hold Trigger. When you set this bit to one, the inverse of TRIG1 is selected as the Hold Trigger signal. If HOLDTRIG is also selected as the Hold Trigger, HOLDTRIG becomes the Hold Trigger signal.
8	TRIG1OUTEN	TRIG1 Output Enable – Determines whether the inverse of the Hold Trigger signal is driven onto TRIG1. When you clear this bit to zero, the Hold Trigger signal is not driven onto TRIG1. When you set this bit to one, the inverse of the Hold Trigger signal is driven onto TRIG1, unless TRIG1 has been selected as the Hold Trigger signal by TRIG1INEN.
7	CLKOUTEN	Scanclock Output Enable – Determines whether the rear signal connector SCANCLK signal is sent out, in inverted form, to the TRIG0 signal. If CLKOUTEN is set to one, SCANCLK* is transmitted on TRIG0. If CLKOUTEN is cleared to zero, SCANCLK* is not transmitted on TRIG0.

Bit	Name	Description (continued)
6	CLKSELECT	Scanclock Select – Determines whether the SCXI-1140 uses SCANCLK or the inverted form of TRIG0 to clock the output multiplexer to scan through the analog channels. If CLKSELECT is cleared to zero, SCANCLK clocks the output multiplexer. If CLKSELECT is set to one, TRIG0* is used as the source to clock the output multiplexer.
5	SCANEN	Scan Enable – Determines whether the output multiplexer will be clocked by the local SCANCLK. If this bit is cleared to zero, the output multiplexer is not clocked. If this bit is set to one, the output multiplexer is clocked by the local SCANCLK.
3	SCANCLKEN*	Scan Clock Enable – Determines whether the output multiplexer increments on each clock signal (the clock source is determined by CLKSELECT) or keeps its loaded value. If SCANCLKEN* is cleared to zero, the output multiplexer is clocked during scans. If SCANCLKEN* is set to one, the output multiplexer is not clocked.
2	SCANCONEN	Scan Control Enable – When set to one, enables the SCANCON signal.
1	AB0EN	Analog Bus 0 Enable – Determines whether Analog Bus 0 on the SCXIbus drives OUTPUT on the rear signal connector. If AB0EN is cleared to zero, Analog Bus 0 does not drive OUTPUT. If AB0EN is set to one, Analog Bus 0 + drives OUTPUT through a buffer and Analog Bus 0 - is connected to OUTPUT REF.
0	FOUTEN*	Forced Output Enable – When cleared to zero, causes the OUTPUT pin on the rear signal connector to be driven by the selected channel through the output buffer, and the OUTPUTREF pin to be tied to local analog ground. If FOUTEN* is set to one, the selected channel on the module does not drive the output buffer unless SCANCON is active (low) and the SCANCONEN* bit is cleared. If the module is driving the output buffer, it also drives Analog Bus 0 if AB0EN is set. If nothing is driving the output buffer, the SCXI-1140 output saturates.

Slot 0 Register Descriptions

Slot 0 has three registers–the Slot-Select Register, the FIFO Register, and the Hardscan Control Register. The Slot-Select Register is a 16-bit write-only register that determines with which slot the data acquisition board speaks when SLOT0SEL* is released high. In the case of the SCXI-1001 chassis, the Slot-Select Register also determines in which chassis the desired slot is. The FIFO Register is a 16-bit write-only register for storing the Slot 0 scan list that determines the chassis scan sequence. The Hardscan Control Register (HSCR) is an 8-bit write-only register for setting up the timing circuitry in Slot 0. Use the SLOT0SEL* line to write to the Slot-Select Register. Write to the HSCR and the FIFO Register as if they were registers located on modules in slots 13 and 14. It is recommended that you maintain software copies of the Slot-Select Register, HSCRs, and all the Slot 0 scan lists that correspond to the writes to FIFO Registers.

If you are using multiple chassis, it is important to understand the architectural differences of the Slot-Select Register as compared to the HSCR and the FIFO Register. Although each chassis has its own physical Slot-Select Register, all are written to at the same time. The jumper settings in Slot 0 of a chassis determine with which chassis number Slot 0 is identified. From the software perspective, there is only one Slot-Select Register in a system composed of multiple chassis. The HSCR and FIFO Register, on the other hand, are unique to each chassis and must be programmed separately.

Slot-Select Register

The Slot-Select Register contains 16 bits that determine which module in which chassis is enabled for communication when the SLOT0SEL* line is high. An SCXI-1000 chassis selects the appropriate module in its chassis, regardless of the chassis number written. The Slot-Select Register shifts in the data present on the MOSI line, bit 16 first, when SLOT0SEL* is low.

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	CHS4

7	6	5	4	3	2	1	0
CHS3	CHS2	CHS1	CHS0	SL3	SL2	SL1	SL0

Bit	Name	Description
15-9	X	Don't care bits – Unused.
8-4	CHS<4..0>	Chassis Bit 4 through 0 – Determine which chassis is selected. On the SCXI-1000 chassis, these are don't care bits.
3-0	SL<3..0>	Slot Bit 3 through 0 – Determine which slot in the selected chassis is selected.

Hardscan Control Register (HSCR)

The HSCR contains eight bits that control the setup and operation of the hardscan timing circuitry of Slot 0. To write to the HSCR, follow the procedure given in the *Register Writes* section using 13 as the slot number, and writing eight bits to the HSCR. The register shifts in the data present on the MOSI line, bit 7 first, when Slot 13 is selected by the Slot-Select Register.

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
RSVD	FRT	RD	ONCE	HSRS*	LOAD*	SCANCONEN	CLKEN

Bit	Name	Description
7	RSVD	Reserved – Should always be written to zero.
6	FRT	Forced Retransmit – When cleared to zero, reinitializes the scan list in the FIFO to the first entry, thus allowing the scan list to be reprogrammed in two steps instead of having to rewrite the entire list. When this bit is set to one, it has no effect.
5	RD	Read – When cleared to zero, prevents the FIFO from being read. When set to one, the FIFO is read except at the end of a scan list entry during scanning, when reading is briefly disabled to advance to the next entry.
4	ONCE	Once – When set to one, this bit shuts down the hardscan circuitry at the end of the scan list during a data acquisition. When cleared to zero, the circuitry wraps around and continues seamlessly with the first scan list entry after the entry is finished.
3	HSRS*	Hardscan Reset – When cleared to zero, this bit resets the FIFO and all the hardware scanning circuitry to the power up state. When set to one, this bit has no effect.
2	LOAD*	Load – When cleared to zero, forces a loading of the Slot 0 sample counter with the output of the FIFO. When set to one, this bit has no effect.
1	SCANCONEN	Scan Control Enable – When set to one, this bit enables the SCANCON lines. When cleared to zero, all SCANCON lines are disabled (high).
0	CLKEN	Clock Enable – When set to one, this bit enables TRIG0 as a hardscan circuitry clock . When cleared to zero, TRIG0 is disabled.

FIFO Register

The FIFO Register adds entries to the Slot 0 FIFO. The FIFO contains the Slot 0 scan list. Each entry contains a slot number to be accessed, and a count number to determine the number of samples to be taken from that slot. To write to the FIFO Register, follow the procedure given in the *Register Writes* section, using 14 as the slot number, and writing 16 bits to the FIFO Register. The register shifts in the data present on the MOSI line, bit 15 first, when Slot 14 is selected by the Slot-Select Register. The Slot 0 scan list is created by consecutive writes to the FIFO Register. Each write creates a new entry at the end of the scan list. The maximum number of entries is 256. To clear the FIFO of all entries, clear the HSRS* bit in the HSCR.

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	MOD3	MOD2	MOD1

7	6	5	4	3	2	1	0
MOD0	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

Bit	**Name**	**Description**
15-11	X	Don't care bits – Unused.
10-7	MOD<3..0>	Module Number – The value of these bits plus one determines the number of the slot to be accessed for this scan entry. For example, to access Slot 6, MOD<3..0> would be 0101.
6-0	CNT<6..0>	Count – The value of these bits plus one determines how many samples are taken before the next scan list entry becomes active. A value of zero corresponds to one sample and a value of 127 corresponds to 128 samples.

Chapter 5
Programming

This chapter contains a functional programming description of the SCXI-1140 and Slot 0.

Note: If you plan to use a programming software package such as NI-DAQ, LabWindows, or LabVIEW with your SCXI-1140 module, you do not need to read this chapter.

Programming Considerations

This section contains programming instructions for operating the circuitry on the SCXI-1140. Programming the SCXI-1140 involves writing to the Configuration Register. Programming Slot 0 involves writing to the HSCR and FIFO registers. Programming the data acquisition boards involves writes to their registers. See your data acquisition board user manual for more information. The programming instructions list the sequence of steps to take. The instructions are language independent; that is, they instruct you to write a value to a given register without presenting the actual code.

Notation

The instructions in this chapter use the following symbols to represent bits:

`0` binary zero
`1` binary one
`X` don't care, either zero or one may be written.
`C` one of three bits used to specify the channel to be loaded into the output multiplexer. This value will either be the channel to be read for single reads, or a starting channel for scanned measurements.
`H` Hold Trigger routing control bits. Instructions for these bits are explained in each section.
`U` User-option bit. Typically, clear these bits to zero, but see the register bit descriptions for more information.
`S` SCCT bits. Usually all zeros for measurements and `00000001` for scans.

The 32-bit patterns are presented MSB first, left to right.

Register Writes

This section describes how to write to the Configuration Register, HSCR, and FIFO Register, including the procedure for writing to the Slot-Select Register to select the appropriate slot. For timing specifics, refer to the *Communication Timing Requirements* section in Chapter 2, *Configuration and Installation.* The rear signal connector pin equivalences to National Instruments data acquisition boards are given in Table 4-1. See also Appendix E, *SCXI-1140 Cabling*. The Configuration Register, the FIFO Register, the and HSCR are write-only registers.

The different bits in these registers often control independent pieces of circuitry. Sometimes you may want to set or clear a specific bit or bits without affecting the remaining bits. However, a write to one of these registers affects all bits simultaneously. You cannot read the registers to determine which bits have been set or cleared in the past; therefore, you should maintain a software copy of these registers. You can then read the software copy to determine the register status. To change the state of a single bit without disturbing the remaining bits, set or clear the bit in the software copy and write the software copy to the register.

Table 5-1. SCXI-1140 Rear Signal Connector Pin Equivalences

SCXIbus Line	SCXI-1140 Rear Signal Connector	MIO-16	Lab Boards	PC-LPM-16
MOSI	SERDATIN	ADIO0	PB4	DOUT4
D*/A	DAQD*/A	ADIO1	PB5	DOUT5
INTR*	SLOT0SEL*	ADIO2	PB6	DOUT6
SPICLK	SERCLK	EXTSTROBE*	PB7	DOUT7
MISO	SERDATOUT	BDIO0	PC1	DIN6

Register Selection and Write Procedure

Select the slot of the module to be written to (or Slot 13 or 14). Initial conditions:

SERDATIN = X
DAQD*/A = X
SLOT0SEL* = 1
SERCLK = 1

2. Clear SLOT0SEL* to 0. This deasserts all SS* lines to all modules in all chassis.

3. For each bit, starting with the MSB (bit 15), do the following:

   a. Set SERDATIN = bit to be sent. These bits are the data being written to the Slot-Select Register.

   b. Clear SERCLK to 0.

   c. Set SERCLK to 1. This rising edge clocks the data. If you are using an MIO-16 board, writing to the EXTSTROBE* register pulses EXTSTROBE* low and then high, accomplishing steps 3b and 3c.

4. Set SLOT0SEL* to 1, which asserts the SS* line of the module whose slot number was written to Slot 0. If you are using multiple chassis, only the appropriate slot in the chassis whose address corresponds to the written chassis number is selected. When no communication is taking place between the data acquisition board and any modules, write zero to the Slot-Select Register to ensure that no accidental writes occur.

5. If you are writing to a Configuration Register, clear DAQD*/A to zero; this indicates data will be written to the Configuration Register. If you are writing to the HSCR or FIFO Register, leave DAQD*/A high.

6. For each bit to be written to the Configuration Register:

    a. Establish the desired SERDATIN level corresponding to this bit.

    b. Clear SERCLK to 0.

    c. Set SERCLK to 1 (clock the data). If you are using an MIO-16 board, writing to the EXTSTROBE* register pulses EXTSTROBE* low and then high, accomplishing steps 6b and 6c.

7. Pull SLOT0SEL* low to deassert the SS* line, latch the data into the Configuration Register, and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.

8. If you are not selecting another slot, write zero to the Slot 0 Slot-Select Register. If you are selecting another slot, repeat the procedure starting at step 3.

For a timing illustration of a Configuration Register write, see Figure 2-20, *Configuration Register Write Timing Diagram*, which shows the proper write to configure an SCXI-1140 that is directly cabled to an AT-MIO-16 board for multiple-module multiplexed scanning with a start channel of five and a scan control count of one.

Initialization

The SCXI-1140 powers up with its Configuration Register cleared to all zeros. This state is also forced by an active low signal on the RESET* pin of the SCXIbus connector. In the reset state, Channel 0 is connected to OUTPUT on the rear signal connector. The module is disconnected from Analog Bus 0. The Hold Trigger is in Level-Sensitive mode and uses the HOLDTRIG pins on the front or rear signal connector as its source. The TRACK*/HOLD pin is high-impedance and the Hold Trigger signal is not sent on TRIG1.

Track-and-Hold Modes

The SCXI-1140 analog channels have two modes–Track mode, in which the outputs at the rear signal connector follow the inputs at the front connector; and Hold mode, in which the outputs freeze at the voltage that was present at the inputs when the Hold Trigger occurred. Because the SCXI-1140 is factory calibrated in Hold mode, you must ensure that the module is in Hold mode when readings are taken. Because the outputs of the SCXI-1140 droop when the module is in Hold mode, it is best to acquire the outputs quickly.

Level-Sensitive Hold Trigger

In this mode, the SCXI-1140 is in Track mode when the Hold Trigger is low, and is in Hold mode when the Hold Trigger is high. Level-Sensitive Hold Trigger mode is the default power-up state and requires minimum software.

Edge-Sensitive Hold Trigger

In this mode, the SCXI-1140 goes into Hold mode on the rising edge of the Hold Trigger signal. The SCXI-1140 goes back into Track mode after it receives the number of rising edges on SCANCON that is specified in the SCCT bits in the Configuration Register. The module also goes back into Track mode if SS* or RESET* is pulled low. Push the RESET button on the Slot 0 front panel to reset the chassis.

Single-Channel Measurements

This section describes how you program the SCXI-1140, either alone or in conjunction with other modules, to make single-channel or nonscanned measurements. It also describes how you program the various data acquisition boards to put the module into Track or Hold mode.

Putting the SCXI-1140 into Track or Hold Mode

Using an MIO Board

Consult the *Programming* chapter of your data acquisition board user manual and Chapter 4, *Register Map and Descriptions*, of the *AT-MIO-16D, AT-MIO-16X* , or *AT-MIO-64F-5 User Manuals* for register locations and initialization procedures. Make sure you have initialized the board.

The initialization routine described in your board user manual puts the OUT2 pin into the high-impedance state. If you change the function of OUT2 to be driven by the MIO board and then want to change back to the high-impedance state so you can drive the HOLDTRIG pin on the front connector of the SCXI-1140 without suffering driver contention, perform the following steps:

1. Write FF02 to the Am9513 Command Register to select Counter 2 Mode Register.

2. Write 0004 to the Am9513 Data Register to select High-Impedance mode.

To control Track and Hold modes from the MIO board, establish OUT2 (HOLDTRIG) low before programming your module:

1. Write FFE2 to the Am9513 Command Register to clear TC Toggle Output of Counter 2.

2. Write FF02 to the Am9513 Command Register to select Counter 2 Mode Register.

3. Write 0002 to the Am9513 Data Register to select TC Toggle mode.

HOLDTRIG should now be low. Check it on the HOLDTRIG pin of the front signal connector. Now program your modules for single measurements. Notice that you can use either Level-Sensitive or Edge-Triggered mode for the Hold Trigger signal.

Put the module or modules into Hold mode:

- Write FFEA to the Am9513 Command Register to Set TC Toggle Output of Counter 2.

From now on, alternate between the Set TC Toggle Output and the Clear TC Toggle Output commands to go between Hold and Track modes. If you are using edge-sensitive triggering, you

must assert SS* to the module or hit the reset switch to put the module back into Track mode before you create another rising edge on OUT2.

Before trying to set Track or Hold modes, make sure you have followed the steps in the *Initializing the MIO Board* section in your board user manual. You will need to decide whether to operate the SCXI-1140 in Edge-Triggered mode or Level-Sensitive mode.

Using a Lab-NB, Lab-PC, Lab-PC+, or Lab-LC Board

Consult the *Programming* chapter in your Lab-PC, Lab-PC+, Lab-NB, or Lab-LC user manual for register locations and initialization procedures.

Before programming your module, establish OUTB1 (HOLDTRIG) low:

- Write 70 (hex) to the Counter Mode Register to put Counter 1 into mode 0, output low.

HOLDTRIG should now be low. Check it on the HOLDTRIG pin of the front signal connector. Now program your modules for single measurements. Notice that you can use either Level-Sensitive or Edge-Triggered mode for the Hold Trigger signal.

Put the module or modules into Hold mode:

- Write 78 (hex) to the Counter Mode Register to put Counter 1 into mode 4, output high.

Alternate between the two lines to go between Track mode and Hold mode. If you are using edge-sensitive triggering, you must assert SS* to the module or hit the reset switch to put it back into Track mode before you create another rising edge on OUTB1.

You cannot program the OUTB1 pin to a high-impedance state. If you want to control Track mode and Hold mode at the front signal connector, set jumper W1 on the SCXI-1341 adapter board to position B to prevent a driver-contention problem.

Using a PC-LPM-16 Board

Consult the *Programming* chapter in your *PC-LPM-16 User Manual* for register locations and initialization procedures.

Before programming your module, establish OUT2 (HOLDTRIG) low:

- Write B0 (hex) to the Counter Mode Register to put Counter 2 into mode 0, output low.

HOLDTRIG should now be low. Check it on the HOLDTRIG pin of the front signal connector. Now program your modules for single measurements. Notice that you can use either Level-Sensitive or Edge-Triggered mode for the Hold Trigger signal.

Put the module(s) into Hold mode:

- Write B8 (hex) to the Counter Mode Register to put Counter 2 into mode 4, output high.

Alternate between the two lines to go between Track mode and Hold mode. If you are using edge-sensitive triggering, you must assert SS* to the module or hit the reset switch to put it back into Track mode before you create another rising edge on OUT2.

You cannot program the OUT2 pin to a high-impedance state. If you want to control Track mode and Hold mode at the front signal connector, set jumper W1 on the SCXI-1342 adapter board to position B to prevent a driver-contention problem.

Direct Measurements

Parallel Output

To perform a direct measurement, you must cable the SCXI-1140 rear signal connector to a data acquisition board, and connect each output to a different data acquisition board channel. See Chapter 2, *Configuration and Installation*, for more information. For information on how to make the voltage measurement with your data acquisition board, consult your data acquisition board user manual. Remember to account for the gains of both the SCXI-1140 and the data acquisition board when calculating the actual voltage present at the input of the SCXI-1140.

To measure one of the eight differential input channels to the SCXI-1140, perform the following steps:

1. Write the binary pattern `XXXXXXXX X000XXXX X0UU0000 00000000` to the SCXI-1140 Configuration Register. Notice that this pattern can be the RESET state.
2. Put the SCXI-1140 into Hold mode.
3. Measure the voltage with the data acquisition board.
4. If desired, make other measurements quickly before the SCXI-1140 output voltage droops too much.
5. Return the SCXI-1140 to Track mode.

Multiplexed Output

To perform a direct measurement, you must have the SCXI-1140 rear signal connector cabled to a data acquisition board. Connect the Output signal to the data acquisition board analog input. See Chapter 2, *Configuration and Installation*, for more information. For information on how to make the voltage measurement with your data acquisition board, consult your data acquisition board user manual. Remember to account for the gains of both the SCXI-1140 and the data acquisition board when you calculate the actual voltage present at the input of the SCXI-1140.

To measure one of the eight differential input channels to the SCXI-1140, perform the following steps:

1. Write the binary pattern `XXXXXXXX XCCCXXXX X0UU0000 00000000` to the SCXI-1140 Configuration Register.
2. Put the SCXI-1140 into Hold mode.
3. Measure the voltage with the data acquisition board.
4. If desired, make other measurements quickly before the SCXI-1140 output voltage droops too much.
5. Return the SCXI-1140 to Track mode.

Indirect Measurements

Measurements from Other Modules

To perform measurements from other modules, you must cable the SCXI-1140 rear signal connector to a data acquisition board. Indirect measurements pass one analog signal over Analog Bus 0 and therefore are considered multiplexed measurements. See Chapter 2, *Configuration and Installation,* for more information.

To make a measurement from another module, perform the following steps:

1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1140, clearing the AB0EN bit in the Configuration Register ensures that its output is not driving AB0.

2. Write the binary pattern `XXXXXXXX XXXXXXXX X0UUDDDD 00000011` to the SCXI-1140 Configuration Register. This step causes AB0+ to drive the OUTPUT pin through a buffer, AB0- to directly drive the OUTPUTREF pin, and prevents the SCXI-1140 from driving the analog bus. Program the four bits marked `DDDD` as follows:

   - If the other module needs the Hold Trigger signal, and it comes from the data acquisition board or will be connected to the HOLDTRIG pin on the front connector of the SCXI-1140, the bits become `0001`. This setting makes the SCXI-1140 receive the Hold Trigger signal from the HOLDTRIG pin (front or rear), and sends an inverted Hold Trigger signal on the SCXIbus TRIG1 line.

   - If the other module receives the Hold Trigger signal at its front or rear signal connector, and it is not necessary to send the Hold Trigger signal to the data acquisition board, the bits become `0000`.

   - If the other module receives the Hold Trigger signal at its own front or rear signal connector, and it is necessary to send the Hold Trigger signal to the data acquisition board, the bits become `1110`. This setting makes the SCXI-1140 send the Hold Trigger signal that it receives from the TRIG1 SCXIbus line.

   - If the other module does not need a Hold Trigger signal, these are don't care bits (`XXXX`).

3. Program the other module to drive Analog Bus 0 with the signal to be measured, and program the appropriate Hold Trigger routing, if necessary.

4. If necessary, put the other module into Hold mode.

5. Measure the voltage with the data acquisition board.

Measurements from the SCXI-1140 via Another Module

To perform measurements via another module, you must cable the rear signal connector of the other module to a data acquisition board and the module must be capable of transferring Analog Bus 0 to the data acquisition board. The other module must also have the ability to route the Hold Trigger signal, unless it will be connected to the front of the SCXI-1140 and is not needed by the data acquisition board. See Chapter 2, *Configuration and Installation*, for more information.

To measure one of the eight differential input channels to the SCXI-1140, perform the following actions:

1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1140, clearing AB0EN in the Configuration Register ensures that its output is not driving AB0.

2. Program the other module to connect Analog Bus 0 to the data acquisition board, but not to drive the connection. You must also program the module to appropriately handle the routing of the Hold Trigger signal.

3. Write the binary pattern `XXXXXXXX XCCCXXXX X0UUDDDD 00000010` to the SCXI-1140 Configuration Register. Program the four bits marked `DDDD` as follows:

   - If the Hold Trigger signal comes from the other module via TRIG1, the bits become `0010`.

   - If the Hold Trigger signal comes to the SCXI-1140 at its own front or rear signal connector and it is not necessary to send the Hold Trigger signal to the data acquisition board that is connected to the other module, the bits become `0000`.

   - If the Hold Trigger signal comes to the SCXI-1140 at its own front or rear signal connector and it is necessary to send the Hold Trigger signal to the data acquisition board that is connected to the other module, the bits become `0001`.

4. Put the SCXI-1140 into Hold mode.

5. Measure the voltage with the data acquisition board.

Scanning Measurements

Programming for scanned data acquisition involves programming your data acquisition board, the modules, and Slot 0. In general, the steps to be taken are as follows:

1. Perform all data acquisition board programming up to the point of enabling the data acquisition.

2. Perform all module programming.

3. Program the Slot 0 hardscan circuitry.

4. Enable the data acquisition, trigger it either through software or hardware, and service the data acquisition.

Only MIO boards can do channel scanning. Lab-NB, Lab-PC, Lab-PC+, Lab-LC, and PC-LPM-16 boards cannot scan channels.

1. Data Acquisition Board Setup Programming

Your data acquisition board user manual contains the programming steps for your data acquisition board. Follow the instructions in the following sections:

- *AT-MIO-16 User Manual*
  - *Multiple A/D Conversions with Interval Channel Scanning (Pseudosimultaneous)*
- *AT-MIO-16 D User Manual*
  - *Multiple A/D Conversions with Continuous Channel Scanning (Round Robin)*
  - *Multiple A/D Conversions with Interval Channel Scanning (Pseudosimultaneous)*
- *AT-MIO-16F-5 User Manual*
  - *Posttrigger Data Acquisition with Interval Channel Scanning*
- *AT-MIO-16X User Manual*
  - *Interval Channel Scanning Data Acquisition*
- *AT-MIO-64F-5 User Manual*
  - *Continuous Channel Scanning Data Acquisition*
  - *Interval Channel Scanning Data Acquisition*
- *MC-MIO-16 User Manual*
  - *Multiple A/D Conversions with Interval Channel Scanning (Pseudosimultaneous)*
- *NB-MIO-16X User Manual*
  - *Multiple A/D Conversions with Interval Channel Scanning (Pseudosimultaneous)*
- *NB-MIO-16 User Manual*
  - *Programming Multiple A/D Conversions with Channel Scanning*. Follow the instructions in this section with the following changes:

    1. Perform step *1. Set up the analog channel and gain selection sequence*. Add the following instructions.

       Program the Scan-Interval Counter.

       Counter 2 of the Am9513A Counter/Timer is programmed to create a square wave in which the high time of the square wave corresponds to the total time needed to take all samples in one scan interval, and the sum of the high time and the low time is the time of the scan interval. The timebase for the Scan-Interval Counter must be the same as the timebase used for the sample-interval counter. The SCXI-1140 operates in Level-Sensitive mode when used with the NB-MIO-16.

The formulas you should use are as follows:

Sample interval = timebase * number of counts entered into Counter 3
High time = sample interval * number of samples per scan interval
High number = high time / timebase
Scan interval time = desired time interval between the start of each scan
Low time = scan interval time - high time
Low number = low time / timebase

a. Write FFB2 (hex) to the Am9513A Command Register to disarm Counter 2.

b. Write FF02 (hex) to the Am9513A Command Register to select Counter 2 Mode Register.

c. Write the mode value to the Am9513 Data Register to store the Counter 2 mode value. Use one of the following hex mode values:

4B62–Selects 1 MHz clock.
4C62–Selects 100 kHz clock.
4D62–Selects 10 kHz clock.
4E62–Selects 1 kHz clock.
4F62–Selects 100 Hz clock.
4562–Selects signal at SOURCE5 input as it clocks the rising edge of the signal, 6 MHz maximum.

d. Write FF0A (hex) to the Am9513A Command Register to select Counter 2 Load Register.

e. Write the low number to the Am9513 Data Register to store the Counter 2 Load value. This number must be between 2 and 65,535.

f. Write FF12 (hex) to the Am9513A Command Register to select Counter 2 Hold Register.

g. Write the high number to the Am9513 Data Register to store the Counter 2 Hold value. This number must be between 2 and 65,535.

h. Write FF42 (hex) to the Am9513A Command Register to load Counter 2 .

i. Write FFE2 (hex) to the Am9513A Command Register to clear the Counter 2 output low.

j. Write FF22 (hex) to the Am9513A Command Register to arm Counter 2.

2. Program the Sample-Interval Counter (substitute this section for the one in Chapter 4 of the *NB-MIO-16 User Manual*.)

a. Write FF03 (hex) to the Am9513A Command Register to select Counter 3 Mode Register.

b. Write the mode value to the Am9513 Data Register to store the Counter 3 mode value. Use one of the following hex mode values:

4B25–Selects the 1 MHz clock.
4C25–Selects the 100 kHz clock.
4D25–Selects the 10 kHz clock.
4E25–Selects the 1 kHz clock.
4F25–Selects the 100 Hz clock.
4525–Selects signal at SOURCE5 input as it clocks the rising edge of the signal, 6 MHz maximum.

Be sure to use the same clock source as the Scan-Interval Counter.

c. Write FF0B (hex) to the Am9513A Command Register to select Counter 3 Load Register.

d. Write the desired sample interval minus one to the Am9513A Data Register to store the Counter 3 load value. The sample interval must be between 2 and 1 0000 (hex) (65,536 decimal).

e. Write FF64 (hex) to the Am9513A Command Register to load and arm Counter 3.

f. Write the desired sample interval to the Am9513A Data Register to store the Counter 3 load value.

- If the sample interval is between 2 and FFFF (hex) (65,535 decimal), write the sample interval to the Am9513A Data Register.

- If the sample interval is 1 0000 (hex) (65,536 decimal), write 0 to the Am9513A Data Register.

3. Perform step *3. Program the Sample Counter* as given in Chapter 4 of the *NB-MIO-16 User Manual*.

Follow the instructions in these sections through the part called *Clear the A/D Circuitry and Reset the Mux Counter*. In the *AT-MIO-16X User Manual*, follow the instructions through the section called *Program the Scan-Interval Counter*. Do not continue to the part labeled *Enable the Scanning Data Acquisition Operation*. Do this after you have programmed the modules and Slot 0.

Note: It is important that you follow the instructions in the interval channel-scanning sections, not the single-channel sections. Although you may be using only one MIO channel, the channel-scanning programming ensures that the MIO board outputs SCANCLK and HOLDTRIG, which the SCXI-1140 and Slot 0 need.

When you program the MIO board for interval scanning, you can also program Counter 2 for high-impedance output, provide your own HOLDTRIG signal, and supply the MIO board with the OUT2 signal. However, you should allow sufficient time between OUT2/HOLDTRIG pulses for the MIO board to acquire all the data in the scan interval. To program Counter 2 for high impedance instead of for operating as a scan-interval counter, substitute the following steps in place of the previously described *Program the Scan-Interval Counter* section. You cannot do this programming with an NB-MIO-16 board.

1. Write FF02 to the Am9513 Command Register to select Counter 2 Mode Register.

2. Write 0004 to the Am9513 Data Register to select High-Impedance mode.

Counter 1 and SCANDIV

All MIO boards can operate their data acquisition board scan lists in two ways. They can acquire one sample per data acquisition board scan list entry; or they can acquire *N* samples per data acquisition board scan list entry, where *N* is a number from 2 to 65,535 that is programmed in Counter 1. This second method of operation can be quite useful, especially when the data acquisition board scan list length is limited to 16 entries. (The AT-MIO-16F-5, AT-MIO-16X, and AT-MIO-64F-5 boards can have up to 512 entries.) Because many SCXI-1140s in one chassis can be multiplexed to one MIO channel, often the simplest way to program the MIO board is to use only one data acquisition board scan list entry, and make *N* the total number of samples to be taken on all modules in one scan. Check your MIO board user manual for limitations of the data acquisition board scan list format.

To program the MIO board to take *N* samples per data acquisition board scan list entry, perform the following additional programming steps at the end of the *Enable the Scanning Data Acquisition Operation* section in the appropriate data acquisition board user manual:

1. Write FF01 to the Am9513 Command Register to select Counter 1 Mode Register.
2. Write 0325 (hex) to the Am9513 Data Register to store Counter 1 Mode Value for most MIO boards. Write 1325 (hex) to the Am9513 Data Register to store Counter 1 Mode Value for the AT-MIO-16F-5, AT-MIO-64F-5, and AT-MIO-16X boards.
3. Write FF09 to the Am9513 Command Register to select Counter 1 Load Register.
4. Write the number of samples to be taken per scan list entry (2 to 65,535) to the Am9513 Data Register to load Counter 1.
5. Write FF41 to the Am9513 Command Register to load Counter 1.
6. Write FFF1 to the Am9513 Command Register to step Counter 1.
7. Write FF21 to the Am9513 Command Register to arm Counter 1.
8. Set the SCANDIV bit in Command Register 1.

2. Module Programming

This section describes the programming steps for various scanning possibilities.

Single-Module Parallel Scanning

To perform single-module parallel scanning, you must cable the SCXI-1140 rear signal connector to a data acquisition board with each output connected to a different data acquisition board channel. See Chapter 2, *Configuration and Installation*, for more information.

To program the SCXI-1140 for single-module parallel scanning, write the binary pattern `XXXXXXXX X000XXXX X0UU0000 00000000` to the SCXI-1140 Configuration Register. Notice that this can be the RESET state.

Program the bits marked UU to 10 when you use an NB-MIO-16 board, and 01 when you use any other MIO-16 board. If you are using your own data acquisition scheme, program these bits appropriately.

Single-Module Multiplexed Scanning (Direct)

To perform simple channel scanning, cable the SCXI-1140 to a data acquisition board. See Chapter 2, *Configuration and Installation*, for more information.

To program the module for scanned channel measurements, write the binary pattern SSSSSSSS XCCCXXXX X0UU0000 00100101 to the SCXI-1140 Configuration Register.

Program the bits marked UU to 10 when you use an NB-MIO-16 board, and 01 when you use any other MIO-16 board. If you are using your own data acquisition scheme, program these bits appropriately.

Program the bits marked SSSSSSSS to 00000001 unless you want to acquire the same data from the SCXI-1140 several times.

Single-Module Multiplexed Scanning (Indirect)

Channel Scanning from Other Modules. To scan measurements from other modules, you must cable the SCXI-1140 to a data acquisition board. See Chapter 2, *Configuration and Installation*, for more information. The module programming steps are as follows:

1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1140, clearing the AB0EN bit in the Configuration Register ensures that its output is not driving AB0.

2. Write the binary pattern XXXXXXXX XXXXXXXX X0UUDDDD 10000011 to the SCXI-1140 Configuration Register. This step causes AB0+ to drive the OUTPUT pin through a buffer, AB0- to drive the OUTPUTREF pin directly, and prevents the SCXI-1140 from driving the analog bus. This step also sends SCANCLK* onto TRIG0.

   Program the bits marked UU to 10 when you use an NB-MIO-16 board, and to 01 when you use any other MIO-16 board. Program the four bits marked DDDD as follows:

   - If the other module needs the Hold Trigger signal, and it will come from the data acquisition board or will be connected to the HOLDTRIG pin on the SCXI-1140 front connector, the bits become 0001. The SCXI-1140 then receives the Hold Trigger signal from the HOLDTRIG pin (front or rear), and sends the inverted Hold Trigger signal on the SCXIbus TRIG1 line.

   - If the other module receives the Hold Trigger signal at its front or rear signal connector and it is not necessary to send the Hold Trigger signal to the board, the bits become 0000.

   - If the other module receives the Hold Trigger signal at its front or rear signal connector and it is necessary to send the Hold Trigger signal to the data acquisition board, the bits

become `1110`. This causes the SCXI-1140 to send the Hold Trigger signal that it receives from the TRIG1 SCXIbus line to the board.

- If the other module does not need a Hold Trigger signal, these are don't care bits (`XXXX`).

3. Program the other module to be scanned to drive Analog Bus 0 with its output. Also program the appropriate Hold Trigger routing, if necessary.

Channel Scanning from the SCXI-1140 via Another Module. To scan the SCXI-1140 via another module, you must cable the other module to a data acquisition board and the module must be capable of transferring Analog Bus 0 to the board. The other module must also be capable of sending a SCANCLK* compatible signal on TRIG0 and a HOLDTRIG*-compatible signal on TRIG1. See Chapter 2, *Configuration and Installation*, for more information.

The module programming steps are as follows:

1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1140, clearing the AB0EN bit in the Configuration Register ensures that its output is not driving AB0.

2. Program the other module to connect Analog Bus 0 to the data acquisition board but not drive Analog Bus 0. Program the other module to send a SCANCLK*-compatible signal onto TRIG0. Also program the module to appropriately handle the routing of the Hold Trigger signal.

3. Write the binary pattern `SSSSSSSS XCCCXXXX X0UUDDDD 01100111` to the SCXI-1140 Configuration Register.

   Program the bits marked `SSSSSSSS` to `00000001` unless you want to acquire the same data from the SCXI-1140 several times. `CCC` is the starting channel number.

   Program the bits marked `UU` to `10` when you use an NB-MIO-16 board, and `01` when you use any other MIO-16 board. If you are using your own data acquisition scheme, program these bits appropriately.

   Program the four bits marked `DDDD` as follows:

   - If the Hold Trigger signal comes from the other module via TRIG1, the bits become `1010`.

   - If the Hold Trigger signal comes to the SCXI-1140 front or rear signal connector and it is not necessary to send the Hold Trigger signal to the board that is connected to the other module, the bits become `0000`.

   - If the Hold Trigger signal comes to the SCXI-1140 front or rear signal connector and it is necessary to send the Hold Trigger signal the board that is connected to the other module, the bits become `0001`.

Multiple-Module Multiplexed Scanning

To scan multiple modules, you must cable one module to a data acquisition board and the module must be capable of transferring Analog Bus 0 to the data acquisition board. This module must also be capable of sending a SCANCLK*-compatible signal on TRIG0. If any of the modules being scanned need a Hold Trigger signal, then this module must also be able to send a HOLDTRIG*-compatible signal on TRIG1. See Chapter 2, *Configuration and Installation*, for more information. The module programming steps are as follows:

1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1140, clearing the AB0EN bit in the Configuration Register ensures that its output is not driving AB0.

2. Program the module that has the connection to the data acquisition board to connect Analog Bus 0 to the board but not drive the Analog Bus 0 unless it is receiving an active low signal on SCANCON. Program the module to send a SCANCLK*-compatible signal onto TRIG0. If necessary, program the module to send a HOLDTRIG*-compatible signal onto TRIG1. If this module is an SCXI-1140, write the binary pattern `SSSSSSSS XCCCXXXX X0UUDDDD 10100111` to its Configuration Register.

   The bits marked `SSSSSSSS` should be programmed to `00000001` unless you want to acquire the same data from the SCXI-1140 several times.

   Program the bits marked `UU` to `10` when you use an NB-MIO-16 board, and to `01` when you use any other MIO-16 board. If you are using your own data acquisition scheme, program these bits appropriately.

   Program the four bits marked `DDDD` as follows:

   - If the Hold Trigger signal comes from the data acquisition board or will be connected to the HOLDTRIG pin on the SCXI-1140 front connector, and any of the other modules need the Hold Trigger signal, program the four bits as `0001`. This makes the SCXI-1140 receive the Hold Trigger signal from the HOLDTRIG pin (front or rear) and send the inverted Hold Trigger signal on the SCXIbus TRIG1 line.

   - If the Hold Trigger signal comes from the data acquisition board or will be connected to the HOLDTRIG pin on the SCXI-1140 front connector and no other module needs the Hold Trigger signal, program the four bits as `0000`.

   - If another module receives the Hold Trigger signal at its front or rear signal connector and it is not necessary to send the Hold Trigger signal to the data acquisition board or the SCXI-1140, program the four bits as `0000`.

   - If another module receives the Hold Trigger signal at its front or rear signal connector and it is necessary to send the Hold Trigger signal to the data acquisition board, program the four bits as `1110`.

   - If another module receives the Hold Trigger signal at its front or rear signal connector and it is not necessary to send the Hold Trigger signal to the data acquisition board, but the SCXI-1140 needs the signal, program the four bits as `1010`.

If you are not going to scan this module, or if you are only using it as an interface, write a zero to bit 2 (SCANCONEN) in the Configuration Register. The start channel bits become don't care bits.

3. Program the other modules to be used in the scan to connect their outputs to Analog Bus 0, but not to drive Analog Bus 0 unless receiving an active low signal on SCANCON. Also program the modules to use TRIG0 as their clock source. For SCXI-1140 modules, write the binary pattern `SSSSSSSS XCCCXXXX X0UUDDDD 10100111` to their Configuration Registers.

   Program the bits marked `SSSSSSSS` to `00000001` unless you want to acquire the same data from the SCXI-1140 several times.

   Program the bits marked `UU` to `10` when you use an NB-MIO-16 board and `01` when you use any other MIO-16 board. If you are using your own data acquisition scheme, program these bits appropriately.

   Program the four bits marked `DDD` as follows:

   - If the Hold Trigger signal comes from another module via TRIG1, program the four bits as `0010`.
   - If the Hold Trigger signal comes to the SCXI-1140 at its front or rear signal connector and it is not necessary to send the Hold Trigger signal to the data acquisition board or to another module, program the four bits as `0000`.
   - If the Hold Trigger signal comes to the SCXI-1140 at its front (or rear) connector and it is necessary to send the Hold Trigger to the data acquisition board or to another module, program the four bits as `0001`.

Multiple-Chassis Scanning

To scan modules on multiple chassis, you must use the SCXI-1001 chassis. The cable from the data acquisition board must bus the digital lines to one module on each chassis. Additionally, the cable must provide each chassis with its own analog channel. The data acquisition board must be able to take several readings at a time on a given channel before accessing a new channel. See the *Counter 1 and SCANDIV* subsection of the *Data Acquisition Board Setup Programming* section earlier in this chapter. You can use the MIO-16 boards with the SCXI-1350 multichassis adapter for multichassis scanning.

For each chassis, program the modules according to the appropriate mode of operation, disregarding the fact that other chassis will be involved, except for the routing of the Hold Trigger.

For example, you want to scan thirteen modules. Twelve modules are in one chassis, and the thirteenth is in the second chassis and is to be scanned through a fourteenth module that is cabled to the data acquisition board but is not involved in the scan. Program the twelve modules in the first chassis according to the steps in the *Multiple-Module Scanning* section shown previously in this chapter, and program the thirteenth and fourteenth modules according to *Channel Scanning from the SCXI-1140 via Another Module*.

The SCXI-1350 multichassis adapters connect the HOLDTRIG pins of all modules that have a connection to the cable assembly. Thus, you can bring the Hold Trigger signal into the front connector of one module, bus it on TRIG1 to another module, send it out the HOLDTRIG on the rear signal connector of that module to the data acquisition board and the other chassis, bring it into a module on another chassis, and send it onto the TRIG1 of that chassis, where another module finally uses it. Such a complicated scheme can introduce a timing skew of up to 250 nsec between modules. If you use the data acquisition board as the Hold Trigger source, the maximum skew is not as significant. If you must externally supply the Hold Trigger, it is best to supply it to the module in any chassis that has a direct connection to the data acquisition board. Because the HOLDTRIG pins on the front and rear signal connectors are the same, you will drive all chassis simultaneously, except for cable length and capacitance delays, thus eliminating several delay elements. If the additional skew caused by one backplane routing is too significant for your needs and you have a strong enough driver, you can cable the HOLDTRIG pin on all the modules together. Recall that the delay in a typical wire is about 1.5 nsec/ft.

3. Programming the Slot 0 Hardscan Circuitry

The following section describes how to program the Slot 0 circuitry for scanning operations. For a more detailed description of the Slot 0 scanning circuitry, consult the *SCXI-1000/1001 User Manual*. Descriptions of the Slot 0 registers are given earlier in the section *Slot 0 Register Descriptions*.

To program the hardscan circuitry, perform the following steps:

1. Write binary `0000 0000` to the HSCR.
2. Write binary `0000 1000` to the HSCR.
3. Write the Slot 0 scan list to the FIFO.
4. Write binary `0010 1100` to the HSCR.
5. Write binary `101S 1100` to the HSCR.
6. Write binary `101S 1110` to the HSCR.
7. Write binary `101S 1111` to the HSCR.

To program the hardscan circuitry to use the current scan list, perform the following steps:

1. Write binary `0000 1000` to the HSCR.
2. Write binary `0100 1000` to the HSCR.
3. Write binary `0000 1000` to the HSCR.
4. Write binary `0010 1100` to the HSCR.
5. Write binary `101S 1100` to the HSCR.
6. Write binary `101S 1110` to the HSCR.

7. Write binary `101S 1111` to the HSCR where `S` = 0 if you want the scanning to repeat when the end of the list is reached, or `S` = 1 if you want the circuitry to shut down after a single scan.

When writing multiple entries to the same register, for example, repetitive writes to the HSCR or several FIFO entries, it is important that SS*13 or SS*14 go inactive (high) between each entry. To accomplish this, select another slot, or toggle the SLOT0SEL* line to temporarily deassert the appropriate SS* line.

If consecutive scan list entries access an SCXI-1140, the SCXI-1140 reloads the output multiplexer with the starting channel after each entry. Thus, two entries for one module with counts of four yields different behavior than one entry with a count of eight.

For multiple-chassis scanning, program each Slot 0 to have dummy entries to fill the sample counts when the data acquisition board is accessing other chassis. Use Slot 13 as the dummy entry slot.

See *Example 3* at the end of this chapter.

4. Acquisition Enable, Triggering, and Servicing

At this point, you should now continue from where you left off in the *Data Acquisition Board Setup Programming* section of this chapter. Perform the following steps given in your data acquisition board user manual:

1. Enable the scanning data acquisition operation.

2. Apply a trigger.

3. Service the data acquisition operation.

Scanning Examples

The following examples may aid your understanding of module and Slot 0 programming. Referring to the bit descriptions for the Configuration Register and the FIFO Register at the beginning of this chapter is helpful.

Example 1

You want to scan channels 3 through 7 on an SCXI-1140 that is in Slot 1 of an SCXI-1000 chassis and is directly cabled to an AT-MIO-16 data acquisition board.

Programming steps:

1. Program your data acquisition board as described in the *Data Acquisition Board Setup Programming* section of this chapter.

2. Following the procedure given in the *Register Writes* section, write `00000001 00110000 00010000 00100101` to the Configuration Register of the SCXI-1140 in Slot 1.

3. Follow the steps outlined in the section, *3. Programming the Slot 0 Hardscan Circuitry*, earlier in this chapter, in which step 3, *Write the Slot 0 scan list to the FIFO*, consists of the following task:

   Write `00000000 00000100` to the FIFO Register. This corresponds to Slot 1 for five samples.

4. Follow the procedure given in the *Acquisition Enable, Triggering, and Servicing* section earlier in this chapter.

Example 2a

An SCXI-1000 chassis has SCXI-1140s in slots 1, 2, 3, and 4. The SCXI-1140 in Slot 4 is cabled to an MIO-16 board. You want to scan channels 2 through 5 on the SCXI-1140 in Slot 1, channels 0 through 6 on the SCXI-1140 in Slot 4, and channels 7 through 3 on the SCXI-1140 in Slot 3.

Programming steps:

1. Program your data acquisition board as described in the *Data Acquisition Board Setup Programming* section of this chapter.

2. Following the procedure given in the *Register Writes* section, write `00000000 00000000 00000000 00000000` to the Configuration Register of the SCXI-1140 in Slot 2. This step resets the module, including the clearing of the AB0EN bit (bit 0). Notice that a complete reset of this module is not necessary, but is used for simplicity.

3. Following the procedure given in the *Register Writes* section, write `00000001 00000000 00010001 10100111` to the Configuration Register of the SCXI-1140 in Slot 4.

4. Following the procedure given in the *Register Writes* section, write `00000001 00100000 00011010 01100111` to the Configuration Register of the SCXI-1140 in Slot 1.

5. Following the procedure given in the *Register Writes* section, write `00000001 01110000 00011010 01100111` to the Configuration Register of the SCXI-1140 in Slot 3. Notice that, after Channel 7, the SCXI-1140 wraps around to Channel 0.

6. Follow the steps given in the section, *3. Programming the Slot 0 Hardscan Circuitry*, earlier in this chapter, in which the step *Write the Slot 0 scan list to the FIFO* consists of the following steps:

   a. Write `00000000 00000011` to the FIFO Register. This corresponds to Slot 1 for four samples.

   b. Write `00000001 10000110` to the FIFO Register. This corresponds to Slot 4 for seven samples.

   c. Write `00000001 00000100` to the FIFO Register. This corresponds to Slot 3 for five samples.

   Make sure to toggle SLOT0SEL* or reselect the FIFO Register from scratch between steps a, b, and c.

7. Follow the procedure given in the *Acquisition Enable, Triggering, and Servicing* section earlier in this chapter.

Example 2b

This example is similar to *Example 2a*, with the exception that the Hold Trigger signal is supplied at the front signal connector of module 2 and must be sent to the MIO-16 board. Notice that you cannot do this with an NB-MIO-16 board.

The Configuration Register writes given in the programming steps 2 through 5 in example 2a become (changes are underlined):

2. `00000000 00000000 0000000`<u>`1`</u> `00000000` to Slot 2.

3. `00000001 00000000 0001`<u>`1110`</u> `10100111` to Slot 4.

4. `00000001 00100000 00011010 01100111` to Slot 1 (no change).

5. `00000001 01110000 00011010 01100111` to Slot 3 (no change).

Example 3

You want to scan six channels on an SCXI-1140 in Slot 4 of Chassis 1, then seven channels of an SCXI-1140 in Slot 11 of Chassis 2, three channels of an SCXI-1140 in Slot 3 of Chassis 3, and five channels of an SCXI-1140 in Slot 8 of Chassis 3.

Assuming you have correctly cabled and programmed the modules, the Slot 0 scan lists should be as follows:

Chassis 1			**Chassis 2**			**Chassis 3**		
Entry	Slot Number	Count	Entry	Slot Number	Count	Entry	Slot Number	Count
1 2	4 13	6 15	1 2 3	13 11 13	6 7 8	1 2 3	13 3 8	13 3 5

Other solutions are possible.

The step labeled *Write the Slot 0 scan list to the FIFO* in the section *3. Programming the Slot 0 Hardscan Circuitry*, earlier in this chapter, consists of the following steps:

1. Select Slot 14 in Chassis 1.

2. Write `XXXXX001 10000101` over MOSI.

3. Toggle SLOT0SEL*.

4. Write `XXXXX110 00001110` over MOSI.

5. Select Slot 14 in Chassis 2.
6. Write `XXXXX110 00000101` over MOSI.
7. Toggle SLOT0SEL*.
8. Write `XXXXX101 00000110` over MOSI.
9. Toggle SLOT0SEL*.
10. Write `XXXXX110 00000111` over MOSI.
11. Select Slot 14 in Chassis 3.
12. Write `XXXXX110 00001100` over MOSI.
13. Toggle SLOT0SEL*.
14. Write `XXXXX001 00000010` over MOSI.
15. Toggle SLOT0SEL*.
16. Write `XXXXX011 10000100` over MOSI.
17. Select Slot 0 in Chassis 0.

Chapter 6
Calibration Procedures

This chapter discusses the calibration procedures for the SCXI-1140 module. Although hardware calibration is discussed in greater detail than software calibration, software calibration is the preferred choice for the following reasons :

- The calibration adjustments on the SCXI-1140 are inaccessible under most normal operating circumstances.
- With software calibration, the module is calibrated in the exact environment in which it will be operating. Software calibration compensates for system-introduced, in addition to module-introduced, errors. You can perform software calibration fairly frequently, which helps reduce drift effects.

Because module-introduced errors are minimal with the SCXI-1140, the use of software rather than hardware calibration does not significantly reduce dynamic range. The main penalty is reduction of throughput due to the increased processing time. Notice that in many applications, the SCXI-1140 factory-hardware calibration is sufficient to meet accuracy requirements, and no further calibration, either hardware or software, is needed.

Software Calibration

Software calibration is very simple in concept. Depending on your accuracy requirements, you may want to perform only offset adjustment; offset and gain adjustments; or offset, gain, and linearity adjustments. These are discussed in the following sections.

Offset Adjustment

Offset adjustment requires that you apply an input signal of zero to the channel to be calibrated. *Zero input* can mean shorting the module inputs to zero, or it can mean applying zero excitation to the transducer being used. In the former case, you can remove only module and data acquisition board offset; in the latter case, transducer offset is removed as well. In either case, measurements are taken with the zero input signal. Average these measurements to reduce uncertainty. This average represents the offset. Next, subtract the offset from all subsequent measurements. Notice that offset changes with gain; thus, during calibration the channel should be set to the gain at which the subsequent measurements will be taken.

Gain Adjustment

Gain adjustment requires you to apply two different input signals, rather than one as for offset adjustment. One of the two points is typically zero, because zero is easy to generate with a high degree of accuracy. The other should be near full scale, either a DC-voltage from a precision calibrator or a voltage generated by application of a known excitation to the transducer being used. Of course, you should generate both signals–zero and full-scale–from the same source.

Take measurements on both signals, and compute separate averages. Then combine the averages with the known input signals to generate linear correction factors for all subsequent measurements. Specifically, if input X yields measurement x, and input Y yields measurement y, then you should process measurement z as shown in the following equation to yield the corrected measurement Z:

$$Z = X + (Y-X)(z-x)/(y-x)$$

Linearity Adjustment

The SCXI-1140 seldom needs linearity adjustment because its linearity is quite good, especially at low gains, and error is often dominated by the nonlinearity of the data acquisition board you use. If necessary, the method described previously for correcting gain and offset error may be extended to include linearity by taking more points along the transfer function and processing subsequently acquired data according to a polynomial fit of the calibration points. Alternatively, and preferably for data acquisition boards with no more than 12 bits of resolution, you can determine the nonlinearity of the system on a code-by-code basis, and you can subtract the error of each code from any measurement that returns that value. This method has the advantage of correcting differential as well as integral linearity errors. However, this method may be time-consuming. If time permits, you may use it with even higher resolution data acquisition boards. Describing methods of measuring system nonlinearity is outside the scope of this manual. If linearity correction becomes necessary, you can contact National Instruments for assistance.

Hardware Calibration

There are two potentiometers (pots) to adjust for each channel. These are set at the factory and should not need to be readjusted for most applications. The pots adjust input offset voltage and output offset voltage for each of the eight channels. Gain and linearity are not adjustable. For detailed specifications of offset, gain, and linearity error, see Appendix A, *Specifications*.

Input offset is any error voltage that appears to be added to the input signal; that is, its effect is multiplied by the gain of the instrumentation amplifier. Output offset is any error voltage that appears to be added to the output signal; that is, its effect is independent of the gain of the instrumentation amplifier. At a fixed gain these errors are indistinguishable; thus, it is necessary to switch between gains to properly calibrate the SCXI-1140.

Your accuracy needs determine how carefully the offsets need to be calibrated. A typical requirement might be for total offset referred to output to be less than half of an LSB of the data acquisition board being used. For example, a 12-bit, 20 V system has a resolution of $20\ V/2^{12} = 4.88\ mV$. Calibration to under 2 mV would thus be sufficient for most applications. The SCXI-1140 is factory calibrated to have total offset referred to output of less than 2 mV at low gains.

Table 6-1 shows which pots to adjust for each type of offset for each channel and which DIP switch selects the gain for each channel. Refer to the parts locator diagram in Chapter 2, *Configuration and Installation*, to determine the location of each component.

Table 6-1. Calibration Component Identification

Channel	Output Offset Adjust	Input Offset Adjust	Gain DIP Switch
0	R9	R10	U12
1	R12	R13	U13
2	R15	R16	U14
3	R18	R19	U15
4	R21	R22	U16
5	R24	R25	U17
6	R27	R28	U18
7	R30	R31	U19

A complicating factor in the calibration of the module is that the output offset is not the same in Track mode as in Hold mode. This difference is because of a phenomenon known as *hold step*, in which a small amount of charge is transferred to the track-and-hold amplifier hold capacitor during the transition from Track mode to Hold mode. This charge transfer slightly changes the voltage at the output of the track-and-hold amplifier. The magnitude of the *hold step* on the SCXI-1140 is approximately 5 mV, enough to make it necessary to calibrate output offset in Hold mode rather than Track mode. You may calibrate input offset without switching the module to Hold mode.

Another complication is the fact that channels 1 through 7 use different signal paths depending on whether the module is in Parallel-Output mode or Multiplexed-Output mode. Thus, the output offset voltage will be slightly different for the two modes. The module is factory calibrated in Multiplexed mode. Channel 0 uses the same signal path in both modes, so its output offset is independent of the output mode.

To calibrate the SCXI-1140 module, the following steps are required:

1. Connect the module with the top cover removed, so that the pots and DIP switches are readily accessible.
2. Short each input of the module to ground.
3. Program the module and data acquisition board to take data in the desired output mode, Multiplexed or Parallel.
4. Set the data acquisition board to a high gain and measure its offset by shorting its input. You must subtract this measured offset from all subsequent module measurements to ensure accuracy.
5. Measure the output of the first channel with its gain set to one and adjust its output offset pot until the output is close to zero.
6. Measure the output of the same channel with its gain set to 500 and adjust its input offset pot until the output is close to zero.
7. Repeat steps 5 and 6 until the offset at both gains is as close to zero as desired.
8. Repeat steps 5 through 7 for all other channels you want to calibrate.
9. Reinstall the module enclosure.

Steps 1 through 9 of the calibration procedure are elaborated on as follows:

1. Position the module so that the chassis has several empty slots in the right side of the module. Alternatively, contact National Instruments concerning availability of an SCXIbus extender board.

2. At low gains, more alternatives exist to serve as a short circuit, but at a gain of 500, 1 mV referred to the output is only 2 μV referred to the input. Thermoelectric effects make it difficult to keep a short circuit from generating such voltages. The best solution is to use short lengths of heavy copper wire, and to keep the short away from heat sources.

3. As mentioned previously, channels 1 through 7 have slightly different output offsets in Parallel mode and Multiplexed mode. Thus, for proper calibration you must decide which mode you plan to use in normal operation. The module is factory calibrated for use in Multiplexed mode. Be careful not to leave the module in Track mode during data acquisition. The SCXI-1140 should switch between Track mode and Hold mode, with the data acquisition board sampling occurring while the module is in Hold mode.

4. For the offset of the data acquisition board not to affect the calibration, you must subtract the offset from all module offset measurements. Thus, you must first measure the offset to an accuracy better than that to which the module is to be calibrated. Furthermore, setting the data acquisition board to a high gain (100, for example) makes it possible to resolve offset changes that would be indiscernible at lower gains. Because the data acquisition board offset will not be independent of gain, you should set the gain first, and then measure the offset. To measure the offset, disconnect the module from the data acquisition board, short circuit the board inputs to ground, and take some data. The measured value is the offset. For a reliable value, use software to average a few hundred readings. After you have measured and recorded the offset, remove the short circuits and reconnect the module.

5. Set the gain of the first module channel you want to calibrate to one. At this gain, most of the module offset is due to output offset. The input offset adjustment has minimal effect. Set the data acquisition board to read the channel. Acquire the data, averaging as in step 4. Adjust the output offset pot until the difference between the measured offset and the data acquisition board offset is close to zero. There is no need to adjust it perfectly because the input offset adjustment in the next step might make a slight change in the measured gain-of-one offset.

6. Switch the gain of the same channel to 500. At this gain, the input offset adjustment has the dominant effect. Acquire the data and average as before. Adjust the input offset pot until the difference between the measured offset and the data acquisition board offset is close to zero. Again, it is not necessary to adjust the input offset perfectly because there will be a slight interdependence between the two offsets.

7. Repeat step 5, adjusting the offset as carefully as desired. Then repeat step 6, adjusting the offset as carefully as desired. Switch back to a gain of one to ensure that the low-gain offset is still calibrated. If necessary, repeat steps 5 and 6 until the offset is calibrated at both gains.

8. Repeat steps 5 through 7 for the additional channels you want to calibrate. There is no calibration interdependence among the channels.

9. Remove the SCXI-1140 module from the SCXI chassis, replace the top cover, and insert the module back into the chassis.

Appendix A
Specifications

This appendix lists the specifications for the SCXI-1140. These are typical at 25° C unless otherwise stated. The operating temperature range is 0° to 50° C.

DC

Maximum output voltage	±10 V
Input offset voltage	±100 µV maximum
Temperature drift	±10 µV/°C maximum
Output offset voltage	±2 mV maximum
Temperature drift	±150 µV/°C maximum
Input bias current	±100 pA typical ±10 nA maximum
Input offset current	±10 pA
Common-mode range	±12 V with zero differential input voltage ±7 V at full-scale output
Input impedance	100 GΩ in parallel with 20 pF

Gains (DIP switch-selectable)	**Max. Gain Error**	**Max. Gain Tempco**	**Max. Nonlinearity**
1	±0.05%	±25 ppm/°C	±0.01%
10	±0.1%	±25 ppm/°C	±0.01%
100	±0.2%	±45 ppm/°C	±0.02%
200	±0.4%	±60 ppm/°C	±0.02%
300	-0.3%, ±0.6%	±80 ppm/°C	±0.03%
500	±1.0%	±100 ppm/°C	±0.04%
600	-0.2%, ±1.5%	±120 ppm/°C	±0.05%
700	-0.1%, ±2.0%	±150 ppm/°C	±0.06%
800	-0.3%, ±3.0%	±200 ppm/°C	±0.07%

Common-mode rejection ratio	
Gain = 1	70 dB minimum 90 dB typical
Gain = 10	87 dB minimum 104 dB typical
Gain ≥ 100	100 dB minimum 110 dB typical
Input protection	±30 V on each terminal, powered on ±15 V on each terminal, powered off

AC

Output noise spectral density 75 nV/$\sqrt{\text{Hz}}$

Input noise spectral density 12 nV/$\sqrt{\text{Hz}}$

Channel output slew rate 15 V/µsec

		Full-Scale Settling Time			
Gains	**-3 dB Bandwidth**	**0.01%**	**0.003%**	**0.0015%**	**0.00076%**
1	2 MHz	7 µsec	8 µsec	10 µsec	15 µsec
10	800 kHz	7 µsec	7 µsec	11 µsec	20 µsec
100	500 kHz	7 µsec	7 µsec	11 µsec	20 µsec
200	300 kHz	7 µsec	8 µsec	11 µsec	20 µsec
300	180 kHz	10 µsec	12 µsec	12 µsec	20 µsec
500	120 kHz	15 µsec	16 µsec	20 µsec	25 µsec
600	100 kHz	20 µsec	20 µsec	20 µsec	25 µsec
700	80 kHz	25 µsec	25 µsec	30 µsec	30 µsec
800	70 kHz	25 µsec	30 µsec	30 µsec	35 µsec

Output multiplexer settling time 1.5 µsec to 0.01%
5 µsec to 0.00076%

Sampling

	0.012%	**0.003%**	**0.0015%**	**0.00076%**
Acquisition time	7 µsec	10 µsec	50 µsec	1 msec
Hold mode settling time	1 µsec	1 µsec	1 µsec	2 µsec

Hold step -5 mV

Droop rate ±10 mV/sec

Effective aperture delay time ±50 nsec

Interchannel skew ±50 nsec

Intermodule skew ±100 nsec

Power

V+ supply current 85 mA

V- supply current 85 mA

+5 V supply current 10 mA

Total power dissipation 4 W

Physical

Dimensions	1.2 by 6.8 by 8.0 in.
I/O connectors	
Input	96-pin DIN C front connector
Output	50-pin male ribbon cable rear connector

Operating Environment

Temperature	0° to 50° C
Relative humidity	5% to 90% noncondensing

Storage Environment

Temperature	-55° to 150° C
Relative humidity	5% to 90% noncondensing

Appendix B
Rear Signal Connector

This appendix describes the pinout and signal names for the SCXI-1140 50-pin rear signal connector, including a description of each connection.

Figure B-1 shows the pin assignments for the SCXI-1140 rear signal connector.

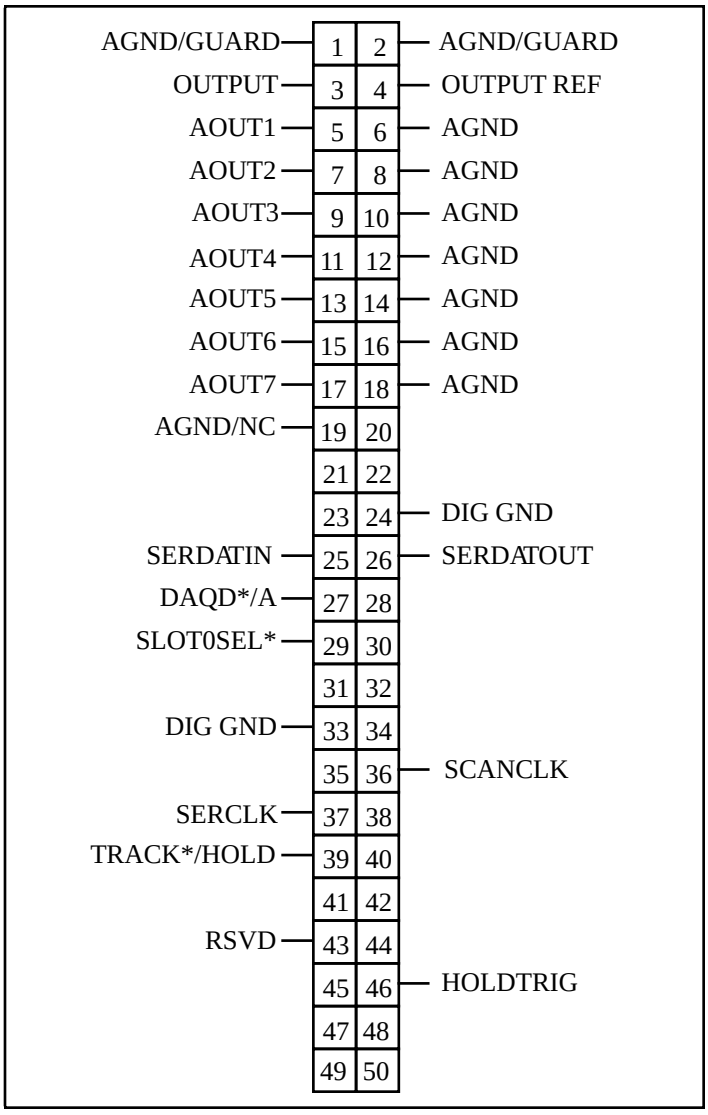


Figure B-1. SCXI-1140 Rear Signal Connector Pin Assignment

Rear Signal Connector Pin Descriptions

Pin	Signal Name	Description
1-2	AGND/GUARD	Analog Ground/Guard – Connected to the module analog ground when jumper W12 is in position A-C, or to the SCXIbus analog bus guard when the jumper is in position A-B. Otherwise leave unconnected. These pins connect to the analog ground of the MIO data acquisition boards.
3	OUTPUT	Output – Main module analog output. In Scan mode, the outputs of all eight channels appear here in sequence. Outputs from other modules can also appear here through the analog bus. In Nonscanning mode, OUTPUT is the output of Channel 0.
4	OUTPUT REF	Output Reference – Connects to the module analog ground unless an output from another module is selected through the analog bus, in which case the pins connect to the analog ground for the selected module.
5, 7, 9, 11, 13, 15, 17	AOUT1 through AOUT7	Analog Outputs – Outputs of channels 1 through 7, independent of whether or not scanning is enabled.
6, 8, 10, 12, 14, 16, 18	AGND	Analog Ground – Connect to the module analog ground. They are used as the reference points for AOUT1 through AOUT7.
19	AGND/NC	Analog Ground/No Connect – Connected to the module analog ground when jumper W9 is in position B-C. When the jumper is in position A-B, this pin is unconnected.
24, 33	DIG GND	Digital Ground – Supply the reference for data acquisition digital signals and are tied to the module digital ground.
25	SERDATIN	Serial Data In – Taps into the SCXIbus MOSI line to send serial input data to a module or Slot 0.
26	SERDATOUT	Serial Data Out – Taps into the SCXIbus MISO line to accept serial output data from a module if jumper W14 is in position A-B. Otherwise, it is unconnected.

Pin	Signal Name	Description (continued)
27	DAQD*/A	Data Acquisition Board Data/Address Line – Taps into the SCXIbus D*/A line to indicate to the module whether the incoming serial stream is data or address information.
43	RSVD	Reserved.
29	SLOT0SEL*	Slot 0 Select – Taps into the SCXIbus INTR* line to indicate whether the information on MOSI is being sent to a module or Slot 0.
36	SCANCLK	Scan Clock – Indicates to the SCXI-1140 that a sample has been taken by the data acquisition board and causes the SCXI-1140 to change channels.
37	SERCLK	Serial Clock – Tps into the SCXIbus SPICLK line to clock the data on the MOSI and MISO lines.
39	TRACK*/HOLD	Track/Hold – Can be programmed to reflect the state of the module–low in Track mode or high in Hold mode. It can also be programmed to a high-impedance output.
46	HOLDTRIG	HOLDTRIG – You can program HOLDTRIG to input or output the Hold Trigger signal for the module. You can use the Hold Trigger signal to place the module into Hold mode. This signal is also brought out to the front connector.

All other pins are not connected.

Appendix C
SCXIbus Connector

This appendix describes the pinout and signal names for the SCXI-1140 96-pin SCXIbus connector, including a description of each signal.

The connector is a triple 4x6 metral receptacle. Figure C-1 shows the pin assignment for the SCXIbus connector.

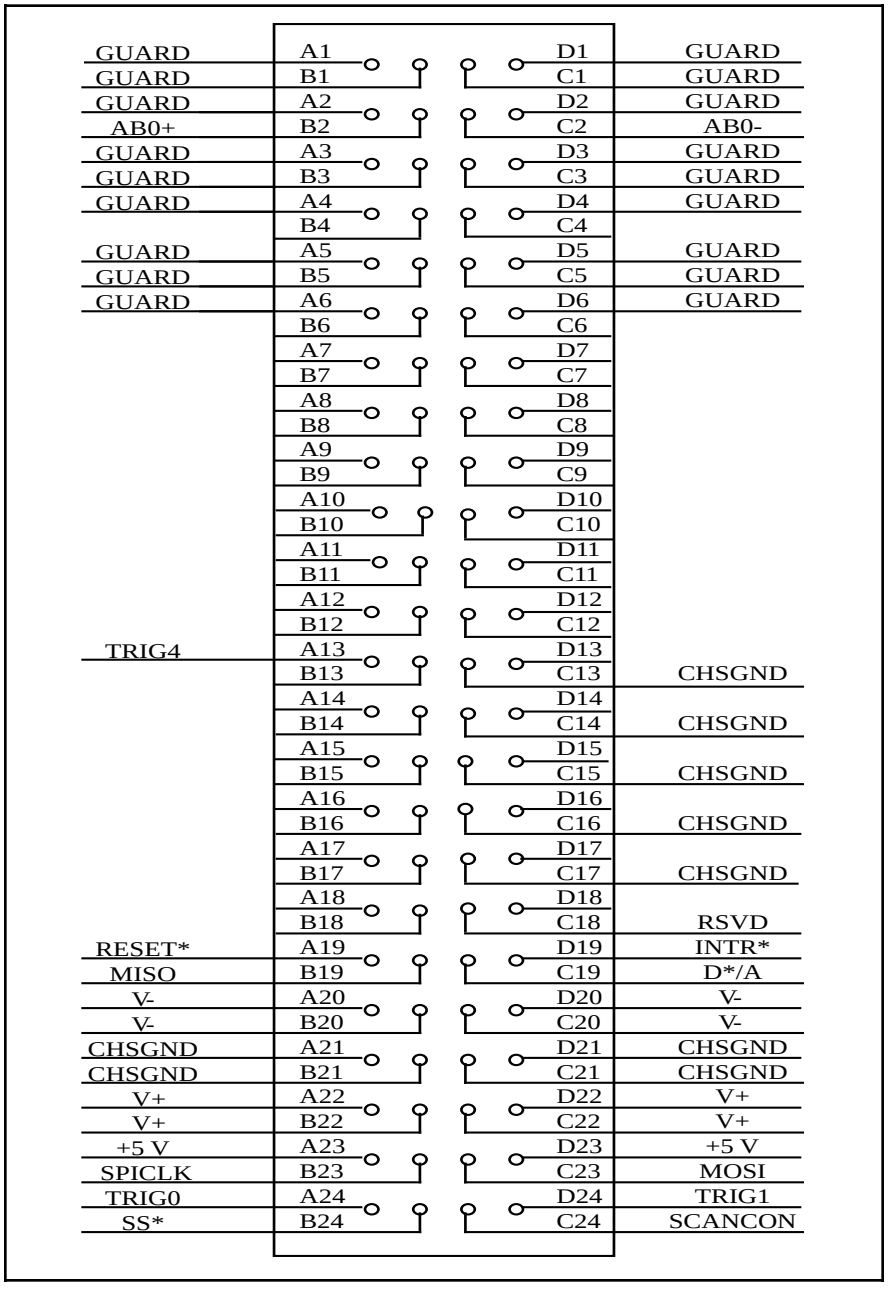


Figure C-1. SCXI-1140 SCXIbus Connector

SCXIbus Connector Signal Descriptions

Pin	Signal Name	Description
B2	AB0+	Analog Bus 0+ – Positive analog bus 0 line. Used to multiplex several modules to one analog signal.
C2	AB0-	Analog Bus 0- – Negative analog bus 0 line. Used to multiplex several modules to one analog signal.
A1, B1, C1, D1, A2, B2, C2, D2, A3, B3, C3, D3, A5, B5, C5, D5, A4, D4, A6, D6	GUARD	Guard – Shields, guards the analog bus lines from noise.
C13-C17, A21, B21, C21, D21	CHSGND	Chassis Ground – Digital and analog ground reference.
A13	TRIG4	TRIG4 – Reserved. Open collector.
C18	RSVD	Reserved.
A19	RESET*	Reset – When pulled low, reinitializes the module to its power-up state. Totem pole. Input.
B19	MISO	Master-In Slave-Out – Transmits data from the module to the SCXIbus. Open collector. I/O.
C19	D*/A	Data/Address – Indicates to the module whether address information or data information is being sent to the module on MOSI. Open collector. I/O.
D19	INTR*	Interrupt – (active low) Causes data that is on MOSI to be written to the Slot-Select Register in Slot 0. Open collector. Output.
A20, B20, C20, D20	V-	Negative Analog Supply – -18.5 to -25 V.
A22, B22, C22, D22	V+	Positive Analog Supply – +18.5 to +25 V.
A23, D23	+5 V	+5 VDC Source – Digital power supply.
B23	SPICLK	Serial Peripheral Interface (SPI) Clock – Clocks the serial data on the MOSI and MISO lines. Open collector. I/O.
C23	MOSI	Master-Out Slave-In – Transmits data from the SCXIbus to the module. Open collector. I/O.

Pin	Signal Name	Description (continued)
TRIG0	A24	TRIG0 – General-purpose trigger line used by the SCXI-1140 to send SCANCLK to other modules or receive SCANCLK from other modules. Open collector. I/O.
B24	SS*	Slot Select – When low, enables module communications over the SCXIbus. Totem pole. Input.
C24	SCANCON	Scanning Control – Combination output enable and reload signal for scanning operations. Each module in a chassis receives a separate SCANCON. Totem pole. Input.
D24	TRIG1	TRIG1 – Can be used to synchronize several SCXI-1140s in the same chassis by forcing them to go into Hold mode at the same time. Open collector. I/O.

All other pins are not connected.

Further information is given in Chapter 3, *Theory of Operation*.

Appendix D
SCXI-1140 Front Connector

This appendix describes the pinout and signal names for the SCXI-1140 front connector, including a description of each connection.

Figure D-1 shows the pin assignments for the SCXI-1140 front connector.

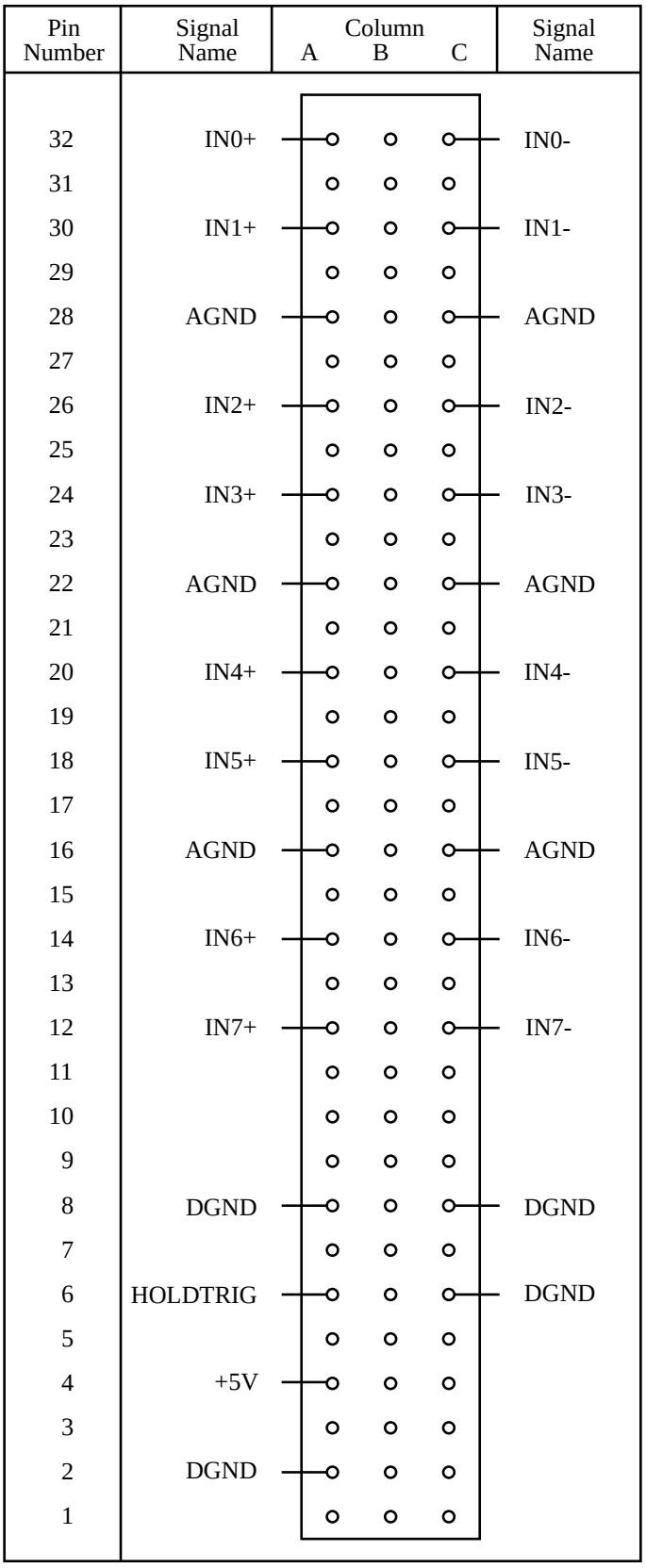


Figure D-1. SCXI-1140 Front Connector Pin Assignment

Front Connector Signal Connection Descriptions

Pin	Signal Name	Description
A32, A30, A26, A24, A20, A18, A14, A12	IN0+ to IN7+	Positive Input Channels – Connect to the noninverting inputs of the instrumentation amplifier of each channel.
C32, C30, C26, C24, C20, C18, C14, C12	IN0- to IN7-	Negative Input Channels – Connect to the inverting inputs of the instrumentation amplifier of each channel.
A28, A22, A16, C28, C22, C16	AGND	Analog Ground – Connect to the module analog ground.
A6	HOLDTRIG	HOLDTRIG – Can be programmed to input or output the Hold Trigger signal for the module. The Hold Trigger signal can place the module into Hold mode. This signal is also brought out to the rear signal connector.
A2, C6, A8, C8	DGND	Digital Ground – Connect to the module digital ground.
A4	+5V	Digital Five Volts – For test purposes only; should not be loaded by more than 25 mA. Only on Rev C and later modules.

Detailed signal specifications are included in Chapter 2, *Configuration and Installation*.

Appendix E
SCXI-1140 Cabling

This appendix describes how to use and install the hardware accessories for the SCXI-1140:

- SCXI-1340 cable assembly
- SCXI-1341 Lab-NB, Lab-PC, or Lab-PC+ cable assembly
- SCXI-1342 PC-LPM-16 cable assembly
- SCXI-1344 Lab-LC cable assembly
- SCXI-1180 feedthrough panel
- SCXI-1302 50-pin terminal block
- SCXI-1351 one-slot cable extender
- SCXI-1350 multichassis adapter
- SCXI-1343 rear screw terminal adapter

SCXI-1340 Cable Assembly

The SCXI-1340 cable assembly connects an MIO-16 board to an SCXI-1140 module. The SCXI-1340 consists of a mounting bracket at one end and a 50-conductor ribbon cable that has a female 50-pin connector at the other end. The female connector connects to the I/O connector of the MIO-16 board. Attached to the mounting bracket is the 50-pin female mounting bracket connector that connects to the rear signal connector of the module. A male breakout connector is near the mounting bracket on the ribbon cable. You can use this male breakout connector to extend the signals of the MIO-16 board to an SCXI-1180 feedthrough panel or an SCXI-1181 breadboard module. All 50 pins from the MIO-16 board go straight to the rear signal connector. You can use a standard 50-pin ribbon cable in lieu of the SCXI-1340 cable assembly, but the SCXI-1340 has the following advantages over the ribbon cable:

- The SCXI-1340 provides strain relief so the cable cannot be accidentally disconnected.
- The SCXI-1340 includes a mounting bracket that mounts to the chassis so that you can remove and reinsert the module without explicitly removing the cable from the back of the chassis. The bracket is especially useful when the SCXI chassis is rack mounted, making rear access difficult.
- The SCXI-1340 has an extra male breakout connector that you can use with the SCXI-1180 feedthrough panel or with additional modules or breadboards that need a direct connection to the MIO-16 board.
- The SCXI-1340 rear panel gives the module and chassis both mechanical and electrical shielding.

Table E-1 lists the pin equivalences of the MIO-16 board and the SCXI-1140.

Table E-1. SCXI-1140 and MIO-16 Board Pinout Equivalences

Pin	SCXI-1140 Rear Signal Connector	MIO-16 Equivalent
1-2	AGND/GUARD	AIGND
3	OUTPUT	ACH0
4	OUTPUT REF	ACH8
5	AOUT1	ACH1
6	OUTPUT REF	ACH9
7	AOUT2	ACH2
8	OUTPUT REF	ACH10
9	AOUT3	ACH3
10	OUTPUT REF	ACH11
11	AOUT4	ACH4
12	OUTPUT REF	ACH12
13	AOUT5	ACH5
14	OUTPUT REF	ACH13
15	AOUT6	ACH6
16	OUTPUT REF	ACH14
17	AOUT7	ACH7
18	OUTPUT REF	ACH15
19	AGND/NC	AISENSE
24, 33	DIG GND	DIG GND
25	SERDATIN	ADIO0
26	SERDATOUT	BDIO0
27	DAQD*/A	ADIO1
29	SLOT0SEL*	ADIO2
36	SCANCLK	SCANCLK
37	SERCLK	EXTSTROBE*
39	TRACK/HOLD	EXTGATE
43	RSVD	OUT1
46	HOLDTRIG	OUT2

No other pins are connected on the SCXI-1140.

SCXI-1340 Installation

Follow these steps to install the SCXI-1340:

1. Make sure that the computer and the SCXI chassis are turned off.
2. Install the SCXI module in the chassis.
3. Plug the mounting bracket connector onto the module rear signal connector as shown in Figure E-1. An alignment tab on the bracket enters the upper board guide of the chassis.

4. Screw the mounting bracket to the threaded strips in the rear of the chassis.

5. Connect the loose end of the cable assembly to the MIO-16 board rear signal connector.

Check the installation.

After step 1, the order of these steps is not critical; however, it is easier to locate the correct position for the mounting bracket with a module installed in the chassis. If you attach a cable to the breakout connector, installation is easiest if you attach the second cable before installing the SCXI-1340.

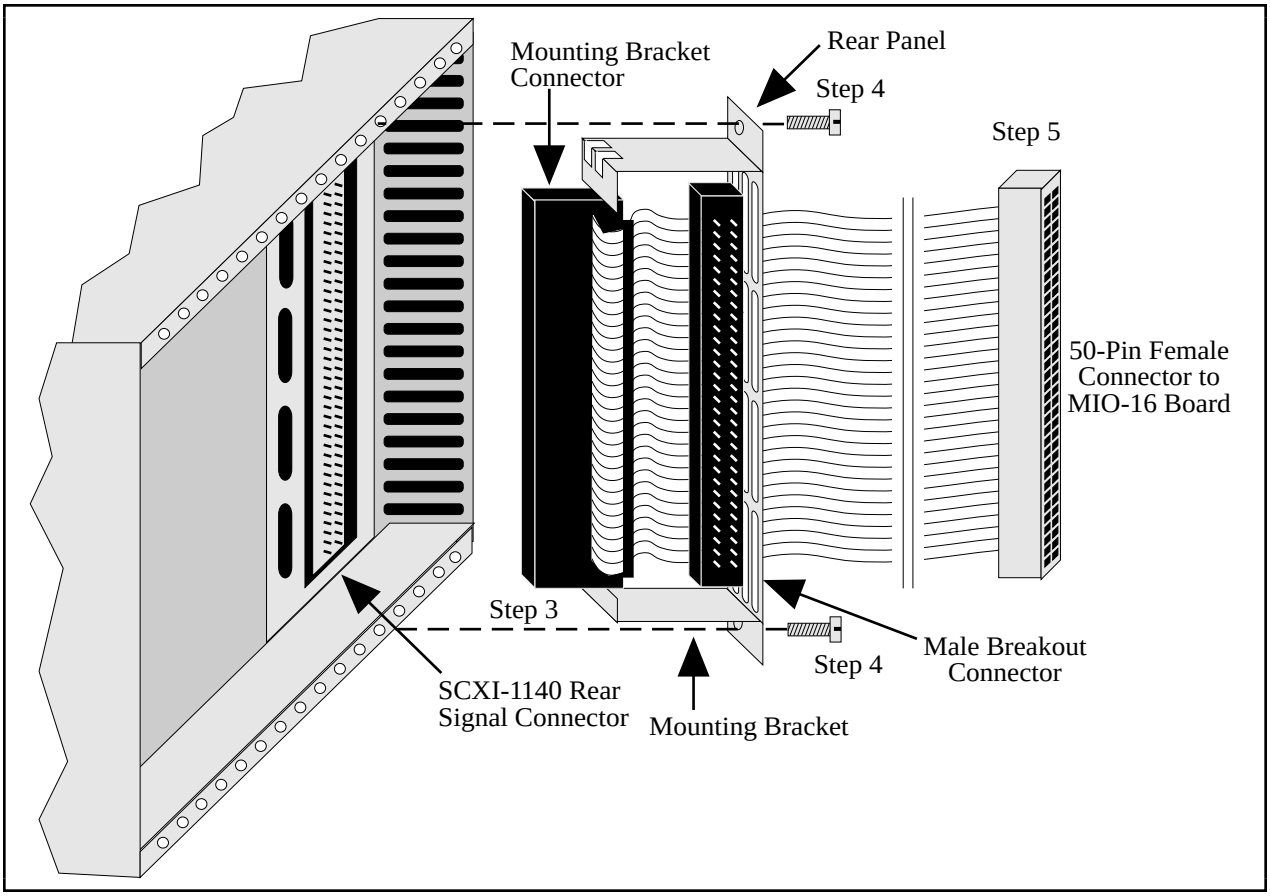


Figure E-1. SCXI-1340 Installation

SCXI-1341 Lab-NB, Lab-PC, or Lab-PC+ and SCXI-1344 Lab-LC Cable Assembly

The SCXI-1341 Lab-NB, Lab-PC, or Lab-PC+ cable assembly connects a Lab-NB, Lab-PC, or Lab-PC+ board to an SCXI-1140 module. The SCXI-1344 Lab-LC cable assembly connects a Lab-LC board to an SCXI-1140 module. The SCXI-1341 and SCXI-1344 cable assemblies consist of two pieces – an adapter board and a 50-conductor ribbon cable that connects the Lab board to the adapter board rear connector. The adapter board converts the signals from the Lab board I/O connectors to a format compatible with the SCXI-1140 rear signal connector pinout at

the front connector of the SCXI-1341 or SCXI-1344. The adapter board also has an additional male breakout connector that provides the unmodified Lab board signals for use with an SCXI-1180 feedthrough panel or SCXI-1181 breadboard module. The adapter board allows the Lab boards full access to the digital control lines but does not allow the Lab boards to scan channels, only to take single measurements. Table E-2 lists the SCXI-1341 and SCXI-1344 pin translations .

Table E-2. SCXI-1341 Pin Translations

Lab Board Pin	Lab Board Signal	SCXI-1140 Pin	SCXI-1140 Signal
1	ACH0	3	OUTPUT
2	ACH1	5	OUT1
3	ACH2	7	OUT2
4	ACH3	9	OUT3
5	ACH4	11	OUT4
6	ACH5	13	OUT5
7	ACH6	15	OUT6
8	ACH7	17	OUT7
9	AIGND	1-2	AGND/GUARD
10	DAC0OUT	20	No Connect
11	AOGND	23	No Connect
12	DAC1OUT	21	No Connect
13, 50	DGND	24, 33	DIG GND
26	PB4	25	SERDATIN
27	PB5	27	DAQD*/A
28	PB6	29	SLOT0SEL*
29	PB7	37	SERCLK
31	PB1	26	SERDATOUT
32	PB2	28	No Connect
40	EXTCONV*	36	SCANCLK
43	OUTB1	46	HOLDTRIG
49	+5 V	34-35	No Connect

All other pins of the Lab board pinout are not sent to the SCXI-1140 rear signal connector.

Jumper W1 on the adapter board is used to connect or disconnect the HOLDTRIG pin on the SCXI-1140 rear signal connector to the OUTB1 pin of the Lab board. If you want to source the HOLDTRIG signal from the data acquisition board, place the jumper in position A, the factory-default setting. If you want to source the HOLDTRIG signal externally, place the jumper in position B as shown in Figure E-2.

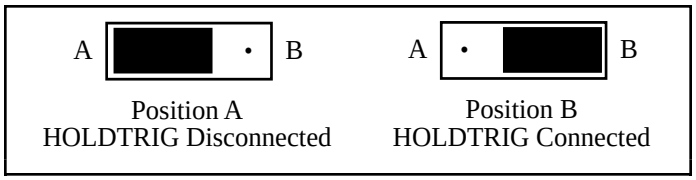


Figure E-2. Jumper W1

SCXI-1341 and SCXI-1344 Installation

Follow these steps to install the SCXI-1341 or SCXI-1344:

1. Make sure that the computer and the SCXI chassis are turned off.
2. Configure jumper W1.
3. Install the SCXI module in the chassis.
4. Connect one end of the ribbon cable to the adapter board rear connector. This is the 50-pin connector of the SCXI-1344 cable.
5. Plug the adapter board front connector to the module rear signal connector. A corner of the adapter board will enter the upper board guide of the chassis.
6. Screw the rear panel to the threaded strips in the rear of the chassis.
7. For an SCXI-1341, connect the loose end of the ribbon cable to the Lab board I/O connector. For an SCXI-1344, connect the two 26-pin connectors to the Lab-LC according to the instructions given in the *Installation* section of Chapter 2, *Configuration and Installation*, of the *Lab-LC User Manual*.

Check the installation.

SCXI-1342 PC-LPM-16 Cable Assembly

The SCXI-1342 PC-LPM-16 cable assembly connects a PC-LPM-16 board to a SCXI-1140 module. The cable assembly consists of two pieces – an adapter board and a 50-conductor ribbon cable that connects the PC-LPM-16 board to the adapter board. The adapter board converts the signals from the PC-LPM-16 I/O connector to a format compatible with the SCXI-1140 rear signal connector pinout. The adapter board also has an additional male breakout connector that provides the unmodified signals of the PC-LPM-16 for use with an SCXI-1180 feedthrough panel or SCXI-1181 breadboard module. The adapter board gives the PC-LPM-16 full access to the digital control lines but does not allow the PC-LPM-16 to scan channels, only to take single measurements. Table E-3 lists the SCXI-1342 pin translations.

Table E-3. SCXI-1342 Pin Translations

PC-LPM-16 Pin	PC-LPM-16 Signal	Rear Signal Connector Pin	SCXI-1140 Use
1-2	AIGND	1-2	AGND/GUARD
3	ACH0	3	OUTPUT
4	ACH8	4	OUTPUT REF
5	ACH1	5	OUT1
6	ACH9	6	OUTPUT REF
7	ACH3	7	OUT2
8	ACH10	8	OUTPUT REF
9	ACH4	9	OUT3
10	ACH11	10	OUTPUT REF
11	ACH5	11	OUT4
12	ACH12	12	OUTPUT REF
13	ACH6	13	OUT5
14	ACH13	14	OUTPUT REF
15	ACH7	15	OUT6
16	ACH14	16	OUTPUT REF
17	ACH8	17	OUT7
18	ACH15	18	OUTPUT REF
19, 50	DGND	24, 33	DIG GND
28	DIN6	26	SERDATOUT
29	DIN7	28	No Connect
34	DOUT4	25	SERDATIN
35	DOUT5	27	DAQD*/A
36	DOUT6	29	SLOT0SEL*
37	DOUT7	37	SERCLK
46	OUT2	46	OUT2
49	+5 V	34-35	No Connect

All other pins of the PC-LPM-16 pinout are not sent to the SCXI-1140 rear signal connector.

Use jumper W1 on the adapter board to connect or disconnect the HOLDTRIG pin on the SCXI-1140 rear signal connector to or from the OUT2 pin of the PC-LPM-16. If you want to source the HOLDTRIG signal from the data acquisition board, place the jumper in position A, which is the factory default. If you want to source the HOLDTRIG signal externally, place the jumper in position B, as shown in Figure E-2.

SCXI-1342 Installation

Follow these steps to install the SCXI-1342:

1. Make sure that the computer and the SCXI chassis are turned off.
2. Install the SCXI module to which the SCXI-1342 will connect.
3. Configure jumper W1.
4. Connect the one end of the ribbon cable to the adapter board rear connector.

5. Plug the adapter board front connector onto the module rear signal connector. A corner of the adapter board will enter the upper board guide of the chassis.

6. Screw the rear panel to the threaded strips in the rear of the chassis.

7. Connect the loose end of the ribbon cable to the PC-LPM-16 I/O connector.

Check the installation.

SCXI-1180 Feedthrough Panel

The SCXI-1180 feedthrough panel has front panel access to the signals of any data acquisition board that uses a 50-pin I/O connector. The SCXI-1180 consists of a front panel with a 50-pin male front panel connector that occupies one slot in the SCXI chassis, and a ribbon cable with a female rear connector and a male breakout connector. The rear connector attaches to the male breakout connector of an SCXI-1340, SCXI-1341, SCXI-1342, or SCXI-1351 in the adjacent slot. The breakout connector further extends the cabling scheme. The front panel connector has the feedthrough connection. You can attach an SCXI-1302 terminal block to the front panel connector for simple screw terminal connections. A rear filler panel that shields and protects the interior of the SCXI chassis is also included.

SCXI-1180 Installation

The SCXI-1180 should be installed to the right of a slot that has an SCXI-1340, SCXI-1341, or SCXI-1342 cable assembly or an SCXI-1351 slot extender in its rear connector space.

Follow these steps to install the SCXI-1180:

1. Make sure that the computer and the SCXI chassis are turned off.

2. Remove the front filler panel of the slot where you want to insert the SCXI-1180.

3. Thread the rear connector through the front of the chassis to the rear of the chassis. Attach the rear connector to the breakout connector of the adjacent cable assembly or slot extender, as shown in Figure E-3.

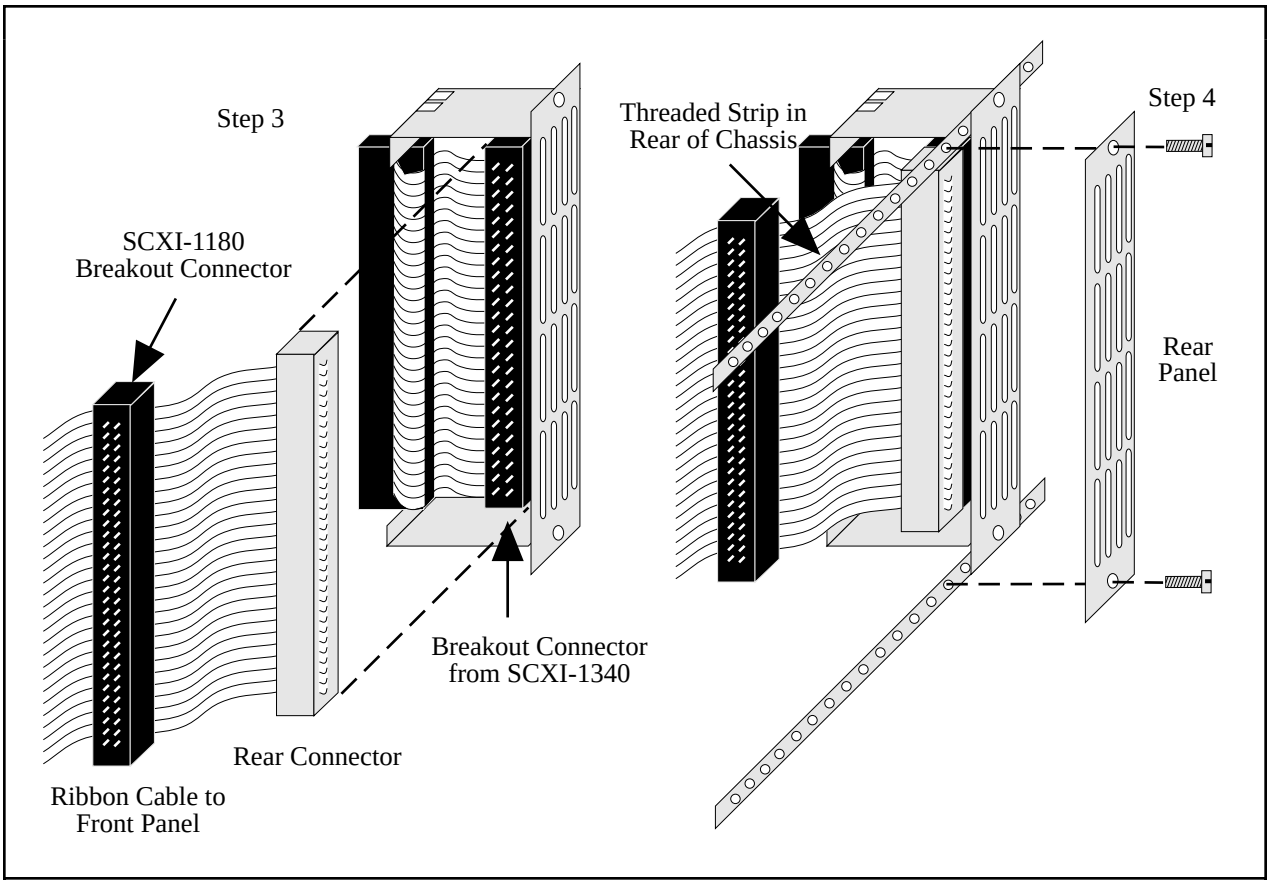


Figure E-3. SCXI-1180 Rear Connections

4. Screw in the rear panel to the threaded strip in the rear of the chassis.
5. Screw the front panel into the front threaded strip, as shown in Figure E-4.

Check the installation.

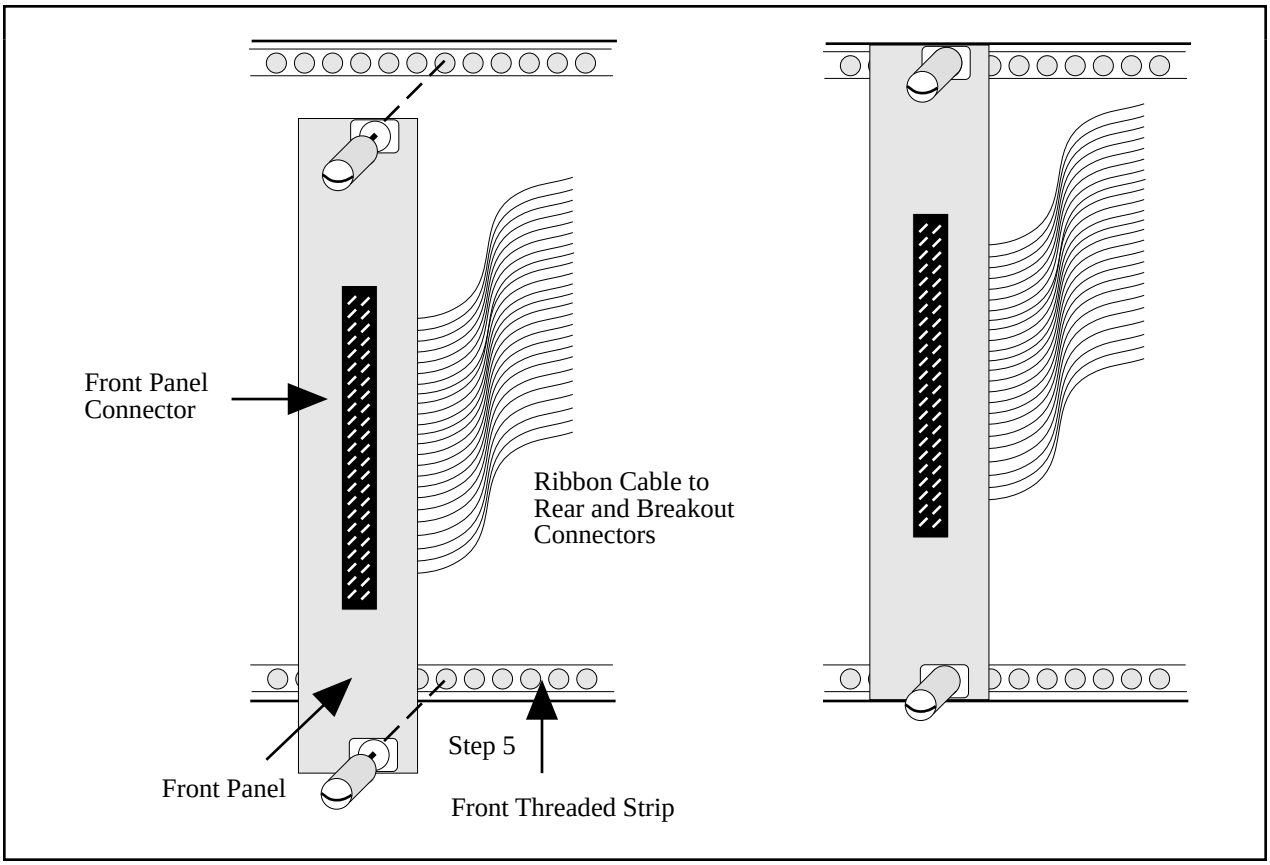


Figure E-4. SCXI-1180 Front Panel Installation

SCXI-1302 50-Pin Terminal Block

The SCXI-1302 terminal block has screw terminal connections for the 50-pin connector on the SCXI-1180 feedthrough panel.

SCXI-1302 Wiring Procedure

To wire the SCXI-1302 terminal block, you must remove the cover, connect all the wiring, and replace the cover, using the following procedure:

1. Unscrew the rear grounding screw on the back of the terminal block, as shown in Figure E-5.
2. With a flathead screwdriver, carefully pry the cover off the terminal block.
3. Insert each wire through the terminal block strain relief.

4. Connect the wires to the screw terminals.
5. Tighten the large strain relief screws to secure the wires.
6. Snap the cover back in place.
7. Reinsert the rear grounding screw. The terminal block is now ready to be connected to the front panel connector.

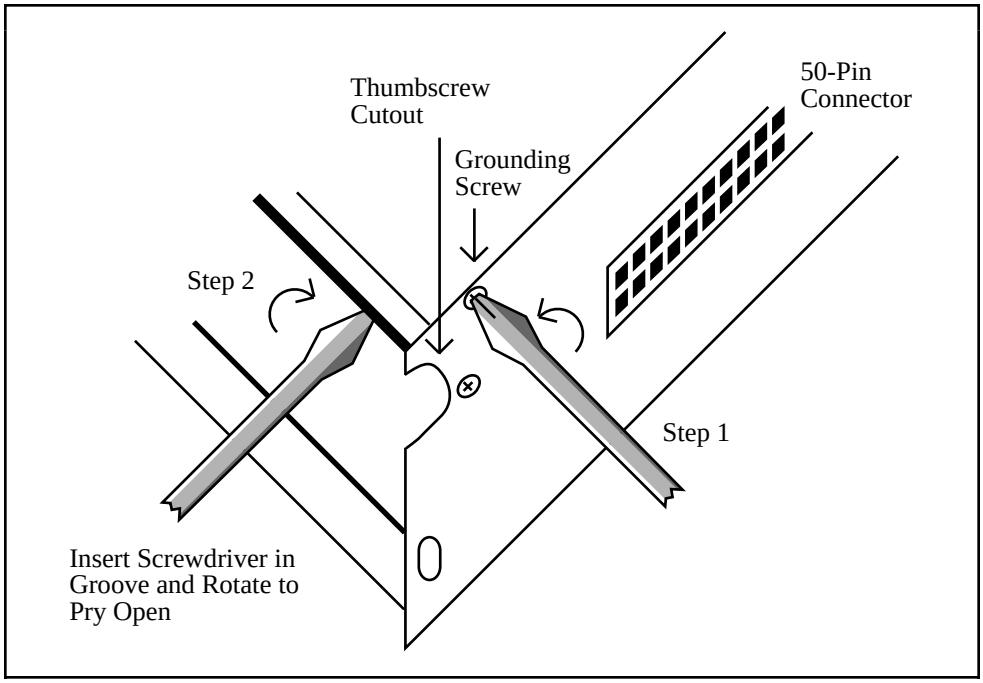


Figure E-5. Cover Removal

SCXI-1302 Installation

Follow these steps to install the SCXI-1302:

1. Install an SCXI-1180 feedthrough panel as described in the *SCXI-1180 Installation* section.
2. Wire the terminal block as described in the previous section, *SCXI-1302 Wiring Procedure*.
3. Connect the SCXI-1302 terminal block to the front panel connector on the SCXI-1180 feedthrough panel. Be careful to fit the thumbscrews into the thumbscrew cutouts.
4. Tighten the top and bottom captive screws on the back of the terminal block into the screw holes in the front panel to hold the SCXI-1302 securely in place.

Check the installation.

SCXI-1351 One-Slot Cable Extender

The SCXI-1351 cable extender is a miniature SCXI-1340 cable assembly. Instead of connecting to an MIO board 1 m away, the SCXI-1351 female rear connector connects to a male breakout connector that must be in the rear connector space of the slot to the left. The SCXI-1351 has a female mounting bracket connector that mates with the rear signal connector of a module, and also provides a male breakout connector on the ribbon cable to support a feedthrough panel or more cable extenders.

SCXI-1351 Installation

Follow these steps to install the SCXI-1351:

1. Make sure that the computer and the SCXI chassis are turned off.
2. Install the SCXI module in the chassis.
3. Connect the rear connector of the cable extender to the breakout connector in the adjacent slot. This attachment is similar to Step 3 in the *SCXI-1180 Installation* section, as shown in Figure E-2.
4. Plug the mounting bracket connector to the module rear signal connector. An alignment tab on the bracket will enter the upper board guide of the chassis.
5. Screw the mounting bracket to the threaded strips in the rear of the chassis.

Check the installation.

Multiple-Chassis Connections for the SCXI-1140

The SCXI-1140 can operate in a multiple-chassis system when you add the SCXI-1350 multichassis adapter. You use the SCXI-1350 multichassis adapter to connect an additional SCXI-1001 chassis to the MIO-16. Using several SCXI-1350s, you can connect up to eight chassis to a single MIO board. You will also need a ribbon cable for each chassis-to-chassis connection, and a ribbon cable for the connection from the MIO board to the first chassis.

Note: When connecting multiple chassis, you should use a 0.5 m length ribbon cable to minimize cable length and maintain signal integrity. It is all right to use a 1.0 m cable from the MIO board to the first chassis.

SCXI-1350 Multichassis Adapter

The adapter board has a male rear connector, a female front connector, and a male chassis extender connector. The rear connector attaches to a ribbon cable from the MIO board or a preceding chassis. The front connector connects with the module rear signal connector. The chassis extender connector connects to a ribbon cable that goes to the subsequent chassis. The adapter takes Channel 0 from the front connector and sends it to Channel 0 of the rear connector, and also takes channels 0 through 6 on the chassis extender connector and maps them to channels 1 through 7, respectively, on the rear connector.

SCXI-1350 Installation

Follow these steps to install the SCXI-1350:

1. Make sure that the computer and all of the SCXI chassis are turned off.
2. Insert all of the modules in all of the chassis.
3. Connect one end of a ribbon cable to the MIO board.
4. Connect the other end of the ribbon cable to the rear connector of the first SCXI-1350.
5. Connect another ribbon cable or cable assembly to the chassis extender connector.
6. Plug the adapter board front connector to the module rear signal connector. A corner of the adapter board enters the upper board guide of the chassis.
7. Screw the rear panel to the threaded strips in the rear of the chassis.
8. Connect the cable assembly to the desired module in the second chassis, or if more than two chassis are being used, connect the loose end of the ribbon cable to the rear connector of the second SCXI-1350, and install the adapter board.
9. Continue until all of the chassis are connected. For *N* chassis, you will need *N* ribbon cables and *N* multichassis adapters.

SCXI-1343 Rear Screw Terminal Adapter

You use the SCXI-1343 universal adapter to adapt custom wiring to the SCXI-1140. The SCXI-1343 has screw terminals for the analog output connections, and solder pads for the rest of the signals. A strain relief is on the outside of the rear panel.

Table E-4. SCXI-1343 Pin Connections

Rear Signal Connector Pin	SCXI-1140 Use	Connection Type
1	AGND/GUARD	Solder pad
2	AGND/GUARD	Screw terminal
3	OUTPUT	Screw terminal
4	OUTREF	Screw terminal
5	OUT1	Screw terminal
6	OUTREF	Screw terminal
7	OUT2	Screw terminal
8	OUTREF	Screw terminal
9	OUT3	Screw terminal
10	OUTREF	Screw terminal
11	OUT4	Screw terminal
12	OUTREF	Screw terminal
13	OUT5	Screw terminal

(continues)

Table E-4. SCXI-1343 Pin Connections (Continued)

Rear Signal Connector Pin	SCXI-1140 Use	Connection Type
14	OUTREF	Screw terminal
15	OUT6	Screw terminal
16	OUTREF	Screw terminal
17	OUT7	Screw terminal
18	OUTREF	Screw terminal
19	AGND/NC	Screw terminal
20	No Connect	Solder pad
21	No Connect	Solder pad
22	No Connect	Solder pad
23	No Connect	Solder pad
24, 33	DIG GND	Solder pad
25	SERDATIN	Solder pad
26	SERDATOUT	Solder pad
27	DAQD*/A	Solder pad
28	No Connect	Solder pad
29	SLOT0SEL*	Solder pad
30	No Connect	Solder pad
31	No Connect	Solder pad
32	No Connect	Solder pad
33	No Connect	Solder pad
34-35	No Connect	Solder pad
36	SCANCLK	Solder pad
37	SERCLK	Solder pad
38	No Connect	Solder pad
39	TRACK*/HOLD	Solder pad
40	No Connect	Solder pad
41	No Connect	Solder pad
42	No Connect	Solder pad
43	RSVD	Solder pad
44	No Connect	Solder pad
45	No Connect	Solder pad
46	HOLDTRIG	Solder pad
47	No Connect	Solder pad
48	No Connect	Solder pad
49	No Connect	Solder pad
50	No Connect	Solder pad

SCXI-1343 Installation

1. Insert each wire through the adapter strain relief.
2. Make all solder connections first.
3. Connect the other wires to the screw terminals.
4. Tighten the strain relief screws to secure the wires.
5. Plug the adapter board front connector to the module rear signal connector. A corner of the adapter board enters the upper board guide of the chassis.
6. Screw the rear panel to the threaded strips in the rear of the chassis.

Appendix F
Revision A and B Photograph and Parts Locator Diagram

This appendix contains a photograph of the Revision A and B SCXI-1140 signal conditioning module and the SCXI-1140 parts locator diagram.

Figure F-1 shows the SCXI-1140 module. Figures F-2 shows the parts locator diagram of the Revision A and B SCXI-1140.

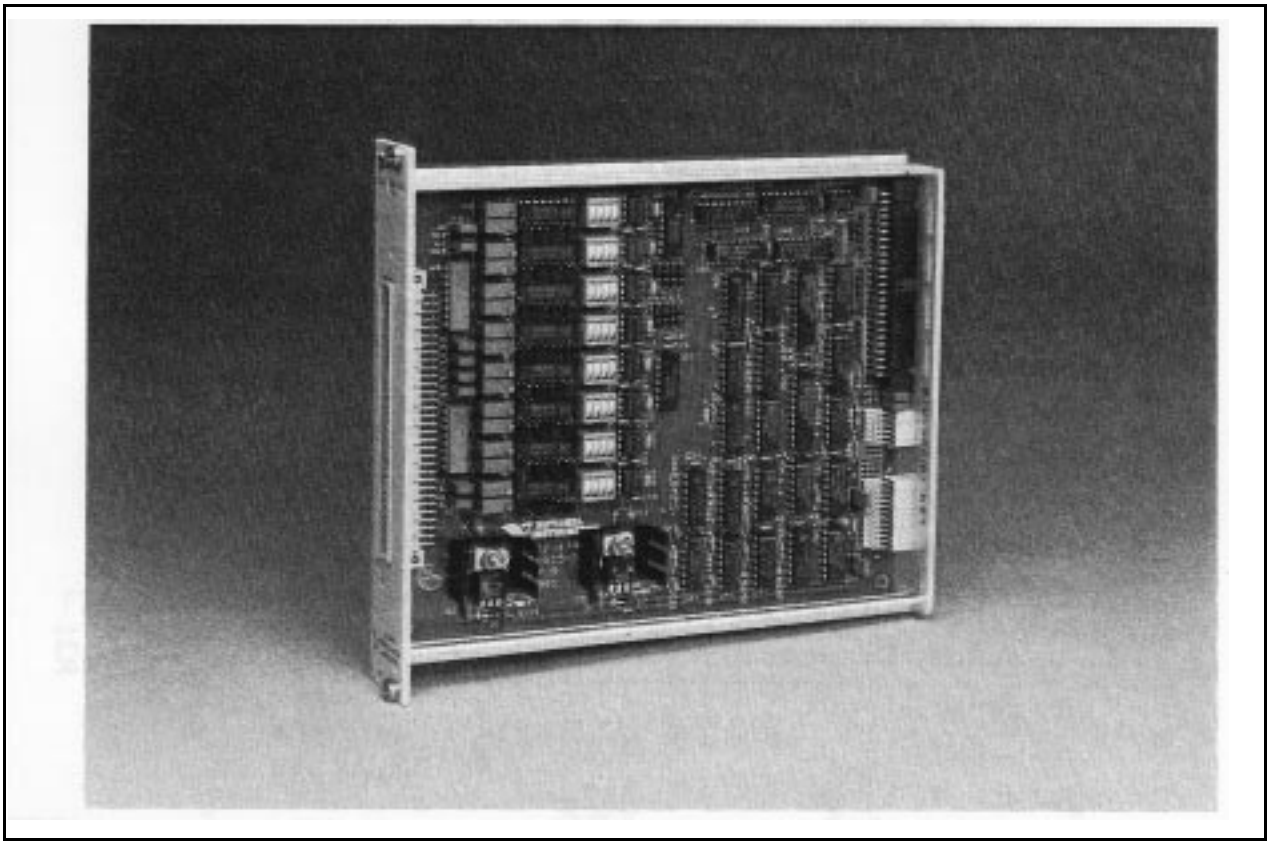


Figure F-1. Revision A and B SCXI-1140 Signal Conditioning Module

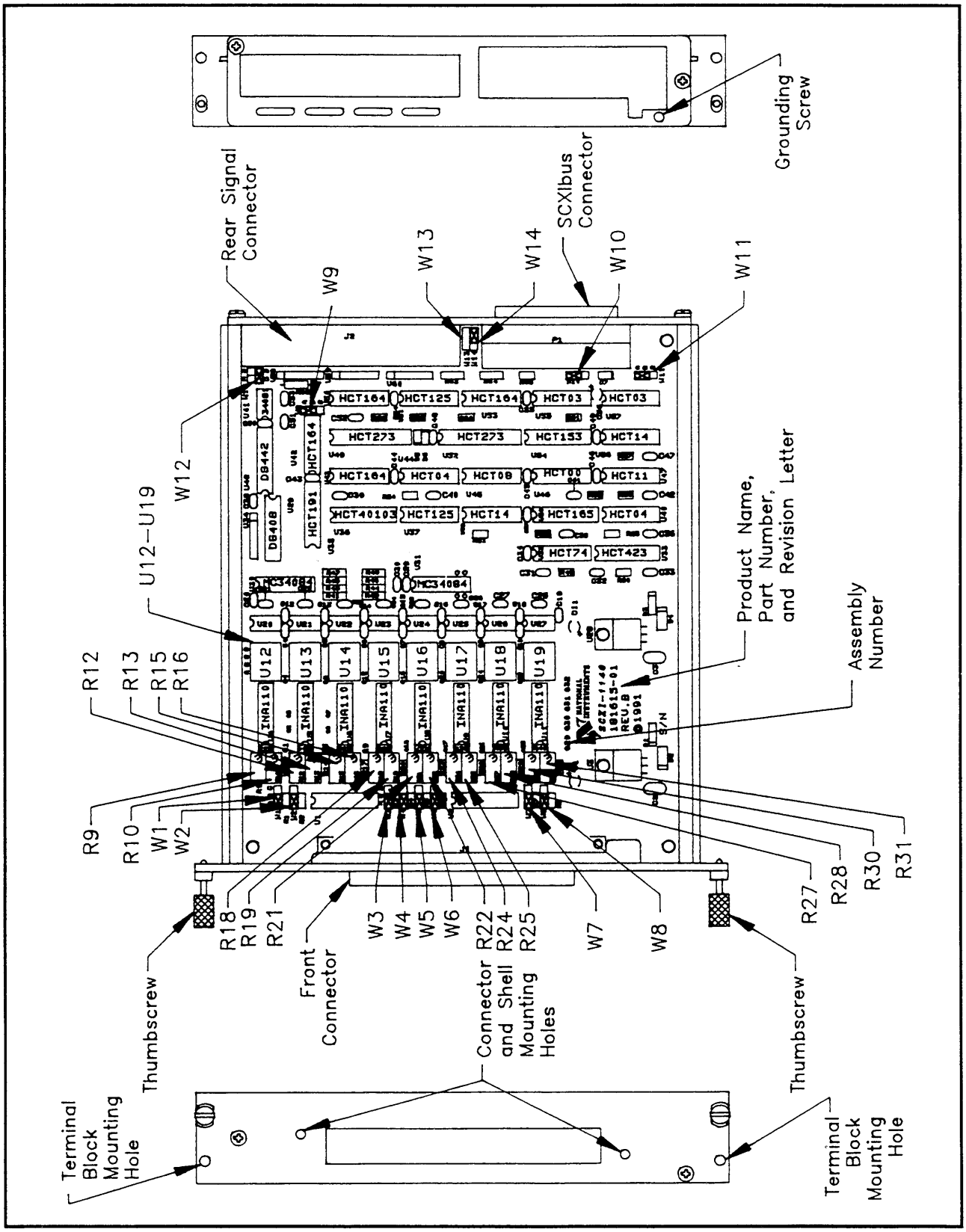


Figure F-2. Revision A and B SCXI-1140 Parts Locator Diagram

Appendix G
Customer Communication

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve technical problems you might have as well as a form you can use to comment on the product documentation. Filling out a copy of the *Technical Support Form* before contacting National Instruments helps us help you better and faster.

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If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name _____

Company _____

Address _____

_____

Fax (___)_____ Phone (___)_____

Computer brand _____ Model _____ Processor _____

Operating system _____

Speed _____ MHz RAM _____ MB Display adapter _____

Mouse _____ yes _____ no Other adapters installed _____

Hard disk capacity _____ M Brand _____

Instruments used _____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is _____

_____

_____

_____

_____

List any error messages _____

_____

_____

_____

_____

The following steps will reproduce the problem _____

_____

_____

_____

SCXI-1140 Hardware Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

- SCXI-1140 Revision Letter _____
- Chassis Slot _____
- Module Grounding _____
  (Factory Setting: W12,
  parking position, A-C)
- Output Grounding _____
  (Factory Setting: W9,
  parking position, A-B)
- Input Grounding (Factory Setting: A-B)

Channel	0	1	2	3	4	5	6	7
Jumper	W1	W2	W3	W4	W5	W6	W7	W8
Setting								

- Channel Gain (Factory Setting: ABCD all OFF, Gain = 1)

Channel	0				1				2				3				4				5				6				7			
Switch	U12				U13				U14				U15				U16				U17				U18				U19			
	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
Setting																																
Gain																																

- Other Modules in System _____
  _____
  _____
- Data Acquisition Boards Installed _____
  _____

Documentation Comment Form

National Instruments encourages you to comment on the documentation supplied with our products. This information helps us provide quality products to meet your needs.

Title: **SCXI-1140 User Manual**

Edition Date: **September 1994**

Part Number: **320410B-01**

Please comment on the completeness, clarity, and organization of the manual.

If you find errors in the manual, please record the page numbers and describe the errors.

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Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

°	degrees
Ω	ohms
A	amperes
ACH#	data acquisition board analog input channel number
A/D	analog-to-digital
AWG	American Wire Gauge
C	Celsius
CH#+	module positive input channel number
CH#-	module negative input channel number
c/s	counts per second
D/A	digital-to-analog
dB	decibels
DIN	Deutsche Industrie Norme
DIP	dual inline package
FIFO	first-in-first-out
hex	hexadecimal
HSCR	Hardscan Control Register
Hz	hertz
ID	identification
in.	inches
I_I	input current leakage
I_{in}	input current
I/O	input/output
I_{out}	output current
LSB	least significant bit
m	meters
MB	megabytes of memory
MCH#+	module positive output channel number
MCH#-	module negative output channel number
MSB	most significant bit
MTS	multiplexed temperature sensor

ppm	parts per million
RAM	random-access memory
rms	root mean square
RTSI	Real Time System Integration
SCXI	Signal Conditioning eXtensions for Instrumentation (bus)
SDK	Software Developer's Kit
s	seconds
SPI	serial peripheral interface
UL	Underwriters Laboratory
V	volts
VI	virtual instrument
V_{IH}	volts input high
V_{IL}	volts input low
V_{in}	volts in
V_{OH}	volts output high
V_{OL}	volts output low
V_{out}	volts out
VAC	volts alternating current
VDC	volts direct current
Vrms	volts root mean square

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