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EMUL-ST10-PC

Getting Started Guide

Edition 1

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Product Notes

Warranty Information

The emulator board, trace board, pod board, and emulator cable are sold with a one-year warranty starting from the date of purchase. Defective components under warranty will either be repaired or replaced at ICE Technology's discretion.

Pod boards that use a bondout processor are also warranted for one year from the date of purchase except for the processor. The bondout processor will be replaced once if support determines that the failure in the bondout processor was not due to the user's actions. This replacement limit does not apply to the rest of the pod board.

Each optional adapter, cable, and extender is sold with a 90-day warranty, except that it may be subject to repair charges if damage was caused by the user's actions.

Seehau software is sold with no warranty, but upgrades can be obtained at our web site http://www.icetech.com.

ICE Technology makes no other warranties, express or implied, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose. In no event will ICE Technology be liable for consequential damages.

European CE Requirements

The following information is to comply with European CE requirements.

User Responsibility

The in-circuit debugger application, as well as all other unprotected circuits need special mitigation to ensure Electromagnetic Compatibility (EMC).

The user has the responsibility to take required measures in the environment to prevent other activities from disturbances from the debugger application according to the user and installation manual.

If the debugger is used in a harsh environment (field service applications for example), it is the user's responsibility to control that other activities cannot be disturbed in such a way that there might be risk for personal hazard/injuries.

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Special Measures for Electromagnetic Emission Requirements

To reduce the disturbances to meet conducted emission requirements it is necessary to place a ground plane on the table under the pod cable and the connected processor board. The ground plane shall have a low impedance ground connection to the host computer frame. The insulation sheet between the ground plane and circuit boards shall not exceed 1mm of thickness.

System Requirements

CAUTION

Like all Windows applications, the Seehau software requires a minimum amount of free operating system resources. The recommended amount is at least 40%. (This is only a guideline. This percentage might vary depending on your PC.) If your resources are dangerously low, Seehau might become slow, unresponsive or even unstable. If you encounter any of these conditions, check your free resources. If they are below 40%, reboot and limit the number of concurrently running applications. If you are unable to free at least 40% of your operating system resources, contact your system administrator or Technical Support at support@icetech.com.

The following are minimum system requirements:

- Pentium 200 (Pentium II or faster is recommended)
- Single-Processor System
- Windows 95, 98, ME, NT, 2000 Pro
- Random Access Memory (RAM)
  - For Windows 95, 98, ME: 64 MB
  - For Windows NT/2000 Pro: 128 MB

Downloading EMUL–ST10–PC Product Documentation

To download an electronic version of this guide, do the following:

1. Open Nohau's home page at www.icetech.com.
2. Click Publications.
3. Click Nohau Manuals.
4. Scroll down to EMUL–ST10–PC. Then select SeehauST10 to download a PDF version of this guide.

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1 Overview of the EMUL–ST10–PC Emulator System

The EMUL-ST10 emulator consists of an emulator pod board that contains the special ST Microelectronics bondout controller and various logic in the form of advanced CPLDs. An optional second board, the trace memory, plugs on top of the emulator pod board. The current maximum speed of both boards is 50 MHz. The emulator is configured and oprated by Seehau. Seehau also contains the firmware for the CPLDs of the emulator. Updates are easy and complete with each new release of Seehau.

The emulator board has various jumpers, LEDs and test points to configure the emulator hardware to your specifications. Figure 1 is a photo of the top of the emulator board and shows some of the user jumpers, connectors, other features and the bondout controller. The trace board does not have any user facilities available as they are all reflected on the emulator board or are software configured by Seehau. Figure 2 shows the trace board. Do not change any jumpers on the trace board. Trace options are all software configured by the user interface Seehau.

On the bottom of the emulator pod are five connectors in an industry standard configuration designed to connect the bondout emulation controller to the target hardware. This connection can be direct with the appropriate connectors designed on the target board, or through various adapters available from ICE Technology. Figure 3 is a photo of the bottom of the board with the bottom case installed. Note the four large connectors (J8 to J11) and a single small one (JP10). JP10 routes XBUS peripheral signals from future derivatives to be sent to the target. Maximum speeds are maintained by not having these signals switched by logic. These signals will normally be routed physically by the adapter or the target board.

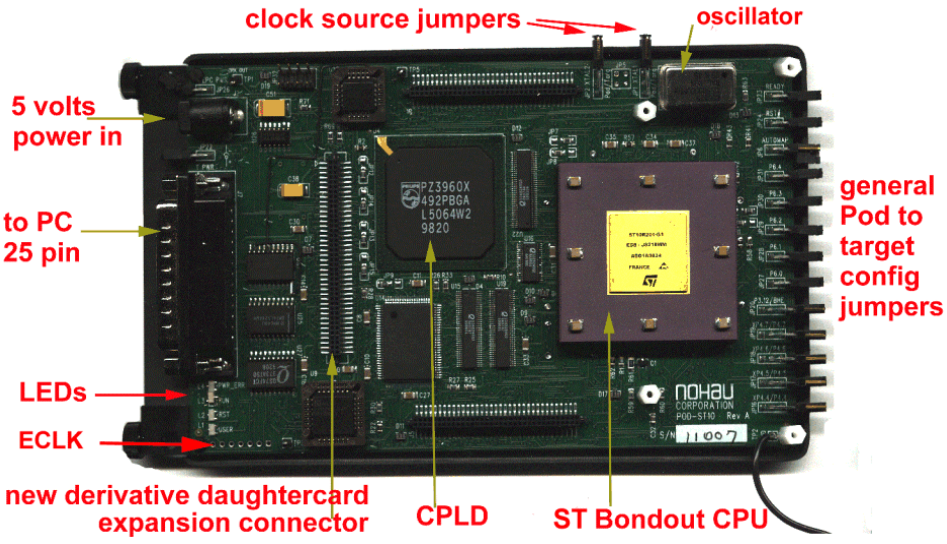


Figure 1. Top View of the Emulator Board

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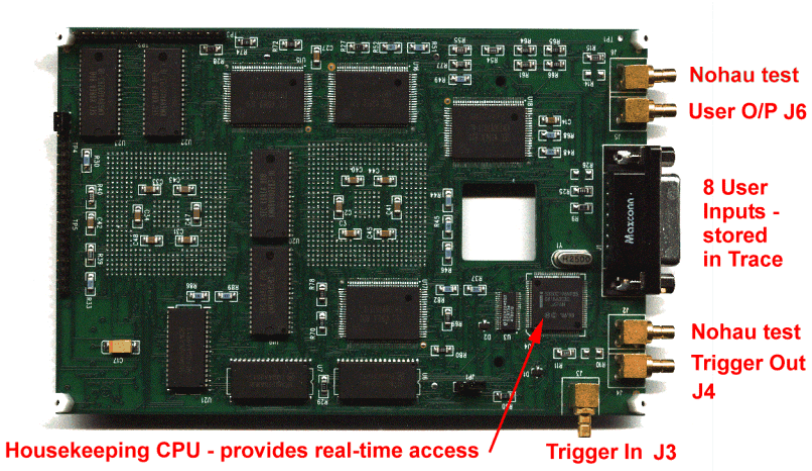


Figure 2. Trace Board

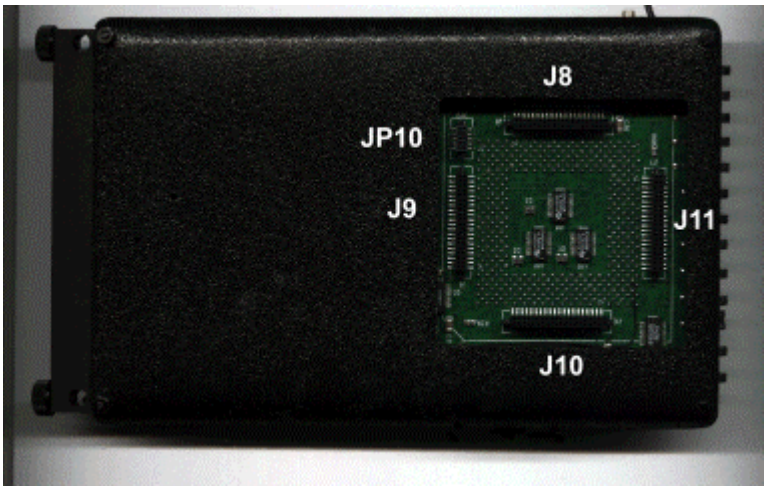


Figure 3. Bottom View of the Emulator Board

The Seehau macro-based GUI is designed to provide a consistent user-friendly interface for all of our in-circuit emulator families. Seehau is a High Level Language (HLL) debugger that allows you to load, run, single-step and stop programs, set and view trace and triggers, modify and view memory contents including SFRs, and set software and hardware breakpoints.

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2 Getting Started

Configuring the Seehau Software

The commands and data used to configure Seehau when it is started is contained in the file Startup.bas. The file Startup.bas is an ASCII file located in the C:\Nohau\SeehauST10\Macro default directory. This file is created by the Seehau Configuration program using user-supplied information about the emulator and its environment. It is not created when Seehau is initially installed. The file Seehau.ini in the C:\Nohau\SeehauST10 directory specifies this startup file.

The configuration can be started by clicking on the Seehau Config icon on your desktop. If you start Seehau and Startup.bas does not exist, Seehau will start the configuration program. This is a good method to restart the emulator configuration over. Simply delete or rename Startup.bas and you can create a new one.

> **Note**
>
> You do not need to have the emulator connected to the PC to run the Seehau Config program. You do need the emulator connected and with the jumpers properly set in for the Seehau regular executive to operate properly.

You can access the Emulator and Trace Setup windows from within Seehau under the **Config** menu item in the main window. Click on **Emulator** or **Trace** for the appropriate setup desired. Note that a more detailed setup is available this way.

This guide assumes you are able to load the Seehau software. Make sure this is done now. If you have trouble loading from diskettes, copy them to a temporay directory on your hard disk and install from there.

It is better to get familiar with the emulator in stand-alone mode before attempting to connect to a target hardware system. The added complications of the target hardware might cause you undue problems at this time. Once you have gained some skills at operating the emulator, it will be easier to connect to your target.

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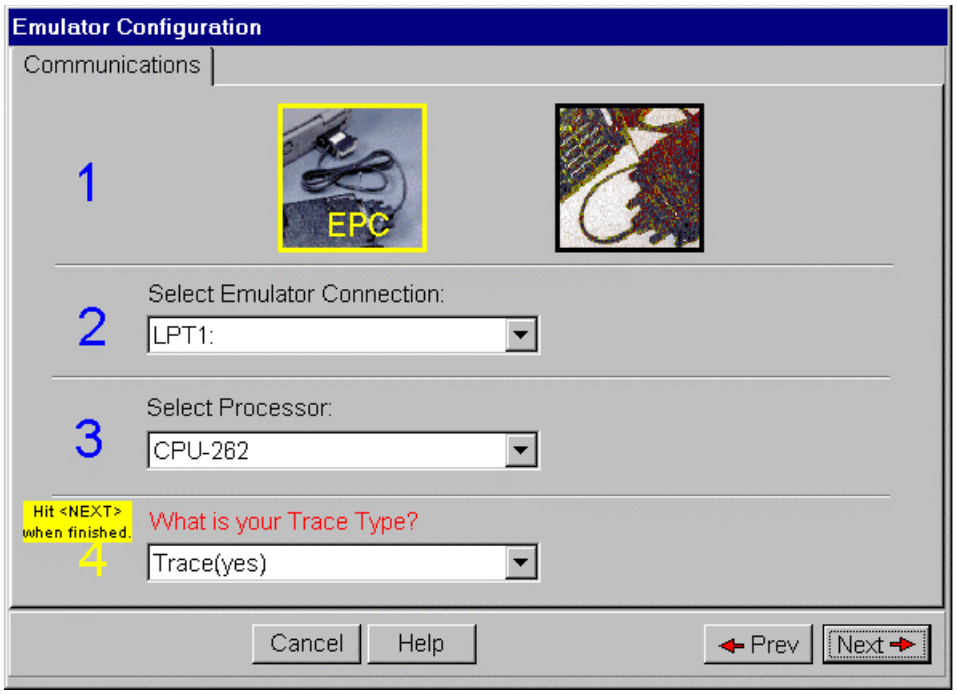


Figure 4. Communications Tab with the EPC Selected

Communications Tab

1. Click on the Seehau Config icon on your desktop. You do not need the emulator connected at this time.

2. The **Emulator Configuration** dialog box opens displaying the **Communications** tabs (Figure 4). You will now configure the emulator. You will need to know what interface connector you are using.

3. Change the settings as indicated.

   The EPC (Enhanced Parallel Cable) and the LC–ISA card are the only appropriate choices for the EMUL–ST10. Figure 4 shows the settings used if you have are using the EPC. The EPC is distinguished by a male/female connector on the end that plugs into your PC parallel port.

   Figure 5 shows the settings for the LC–ISA card. The **Emulator Board Address** field is for the address of the internal communication link from your computer. For the ISA card, the most common address is 200. This setting can be changed on the board. If you are using the EPC, this address is not applicable. The EPC uses address 378 which represents the LPT1 port on your PC.

4. When all the information has been entered in the **Communications** tab, click **Next**. The **Hdw Config** tab opens (Figure 6). It is possible to operate the emulator remotely through a TCP/IP connection. Contact Technical Support for more information, email support@icetech.com.

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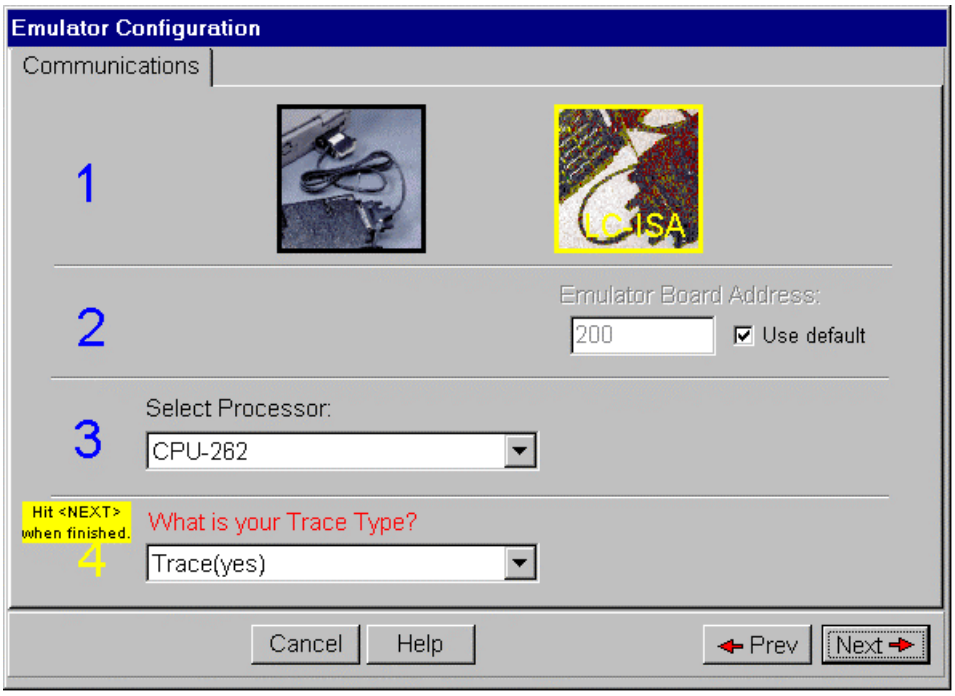


Figure 5. Communications Tab with the LC–ISA Selected

Hardware Configuration Tab

uP Clock—The internal CPU clock. This is usually the clock multiplied by four if the controller is in PLL mode. If your crystal is 12.5 MHz, then the CPU clock is 50 MHz. If you have a 5-MHz crystal installed, the CPU frequency is 20 MHz.. Set it to 50 for the 262. This setting is used only for the calculation of the trace timestamp. It has no effect on the operating speed of the emulation controller.

Processor—This is set to CPU-262. CPU–167 is for the Siemens C166 family of processors. This can be changed only through the configuration program or be editing Startup.bas.

On Chip ROM size—This tells Seehau the size of the on-chip ROM or FLASH memory in your controller. No ROM is indicated here because there is no target. **NONE** is the default setting.

1. Confirm your settings are the same as in Figure 6. Set the frequency to 50 MHz for the ST10. This entry only effects the trace timestamp. It does not effect any other part of the emulator.

2. Click **Next** to enter the data. When Seehau will ask if you are done, click **Yes**.

3. The Seehau configuration program creates Startup.bas and Seehau is now configured to run your emulator.

4. The Seehau configuration program shuts down. Seehau is ready to properly run the emulator.

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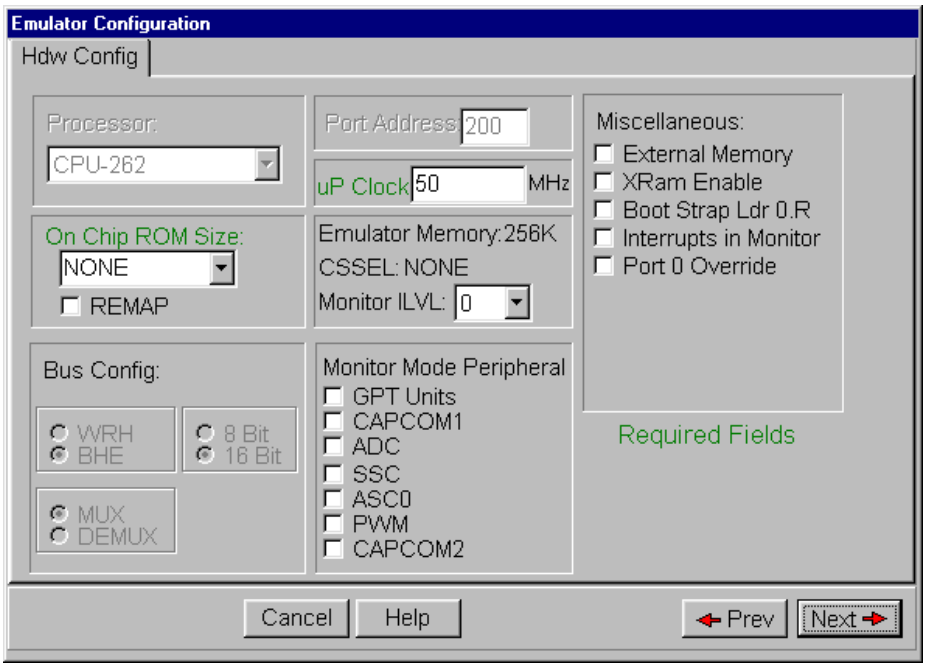


Figure 6. Hdw Config Tab

Now you are ready to run Seehau after you have connected and powered up the emulator.

The emulator is powered by 5 volts regulated at the standard power supply socket. The center pin is positive. The jumper settings will be the default for this part of the guide. The CPU fan must operate or the bondout CPU will overheat and be damaged. This will not be covered under the warranty. Do not connect the power supply to the emulator at this time.

Important Software and Hardware Notes

- Always use Uninstall to unload any existing version of Seehau from your computer before loading in another copy. Do not simply delete the Seehau files and/or folders. Do not install Seehau on top of an existing copy.

- Under My Computer select **Control Panel**, then **Add/Remove Programs**. After Uninstall has run, delete any files and folders that Uninstall did not delete. Save your personal macros and source files first. Pay particular attention to Startup.bas in the Macro directory. You might not want to use your old copy.

- Do not leave the ST10 pod powered for extended periods of time without Seehau active. The pod will be in an uninitialized state with unpredictable results. There are no reports of damage resulting from this.

- Pay attention to the power-up and power-down sequences of the emulator and a target system. When powering up or down the system: the target must never be powered when the pod is not. Power flowing from the target into the bondout controller will damage it. Always power up the pod first, and power it down last.

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Starting the Emulator and Seehau

1. The two clock jumpers must be in the upper position (Pod position).

2. T Pwr (JP22) must be connected. This jumper supplies power to the bondout CPU. This jumper is located between the PC connector and the power supply socket.

3. If you are using the EPC, the EPC PWR jumper (JP26) must be connected to send power to the EPC. This jumper is located beside the power socket opposite side of the T PWR jumper. If you are using the ISA card, this jumper must be left open. Otherwise, the power from the ISA will conflict with the 5-volt power supply.

4. All 13 jumpers on the end edge of the board must be connected. For the five that have dual pins, the position is lower or close to the PC board. All these jumpers might not be needed in order for this example to work.

5. Connect the cable between the PC and the 25-pin connector on the emulator board.

6. Double check your settings.

7. Plug in the 5-volt power supply.

8. The fans will start immediately and the green LED RUN will illuminate with the EPC connected.

9. Double-click the Seehau ST10 icon on your PC desktop.

10. Seehau will configure itself from Startup.bas and might present this message asking if you want to reset the emulator. The green RUN LED is probably on: Click **Yes**. Some Seehau versions will not display this. **Mac** will be displayed in red at the bottom of the main window while Startup.bas is running.

11. The red Reset LED will then light and then both it and the Run LED will go out. Seehau will finish loading itself. Position and size the main window to your preference. You can open up new windows. They are found in the **New** menu item on the Seehau menubar.

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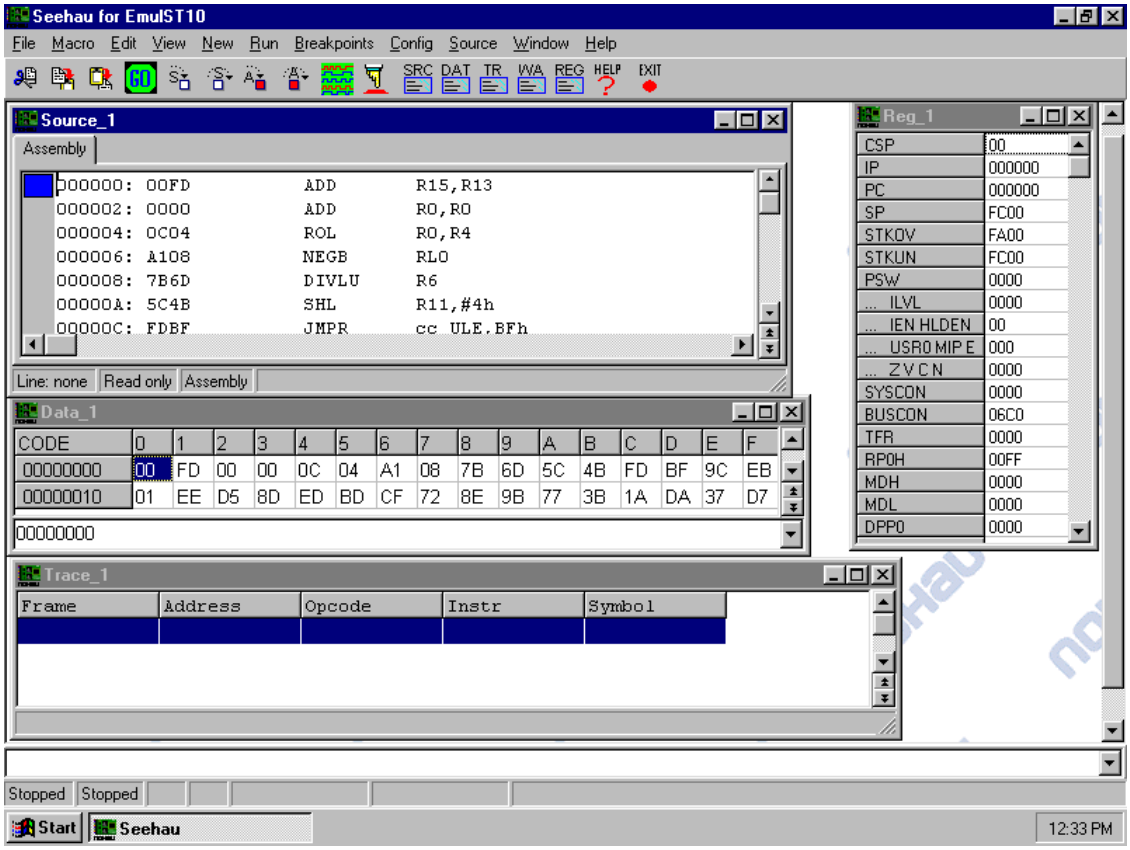


Figure 7. Seehau for EMUL–ST10 Windows

Troubleshooting

- Problems are usually from the EPC PWR, T PWR or the clock incorrectly connected. Review Steps 1, 2, and 3 in the previous section. Make sure the cable to the PC is correctly connected. If you are using the EPC, try it without a printer connected. Do not have the emulator connected to a target system or adapter. You should have a 12.5-MHz oscillator module installed to get a 50-MHz CPU frequency.

- Try another PC. Reload Seehau. If you do this, use the Windows Remove Programs found under My Computer, System. This way, all files and registry entries are properly deleted.

- Use the Task Manager to make sure ncore is no longer running after a Seehau crash.

- If all this fails, contact Technical Support. email support@icetech.com

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Shutting Down Seehau

1. Click on the X in the upper-right corner. Press ALT+X, or from the **File** menu, select **Exit**. The **Save Settings** dialog box opens (Figure 8).
2. You can save your setup in Startup.bas or a macro file of your own naming.
3. If the **Use as Default** option is selected, this file will be used when Seehau is started.
4. This macro will save those items enabled in the **Macro Save Type** field.
5. Click **No Save** and exit from Seehau.

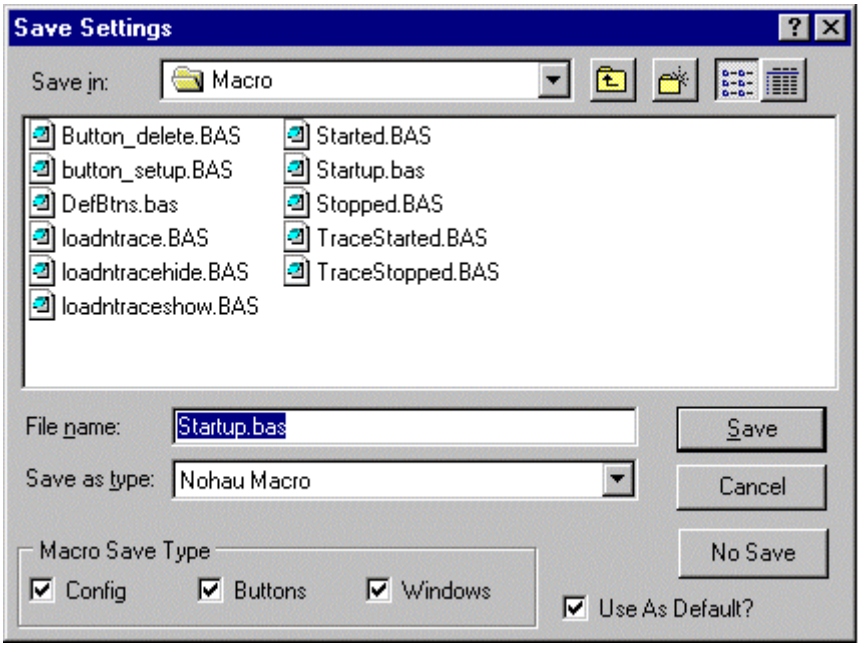


Figure 8. Save Settings Dialog Box

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3 Running the Example Program Timer.abs

We have provided a small example program called Timer.abs located in C:\Nohau\Seehaust10\Examples default directory. The source code, Time.c is also in this directory.

1. Start the emulator as per the instructions in the "Starting the Emulator and Seehau" section.
2. Resize the windows as in Figure 7 but do not add the Trace or Watch windows.
3. From the **File** menu, select **Load Code**, or press CTRL+L. The **Open** dialog box opens (Figure 9).
4. Click on the arrow at the end of the **Files of type** text box and select **ABS Files**. Your window will now look like Figure 9.
5. Highlight **Time.abs** and click **Open**. You can also double-click on Time.abs. Time.abs will load into the emulator. The Source window will show a JMPS at the reset vector (00000). The jump is to _CSTART. This is at memory location 200 and you can scroll there to see it.
6. Click on the Step Into icon and the program will run to the start of MAIN. Note that the **time.c** tab appears on the Source window. You can easily switch between assembly and source language by clicking on these tabs.

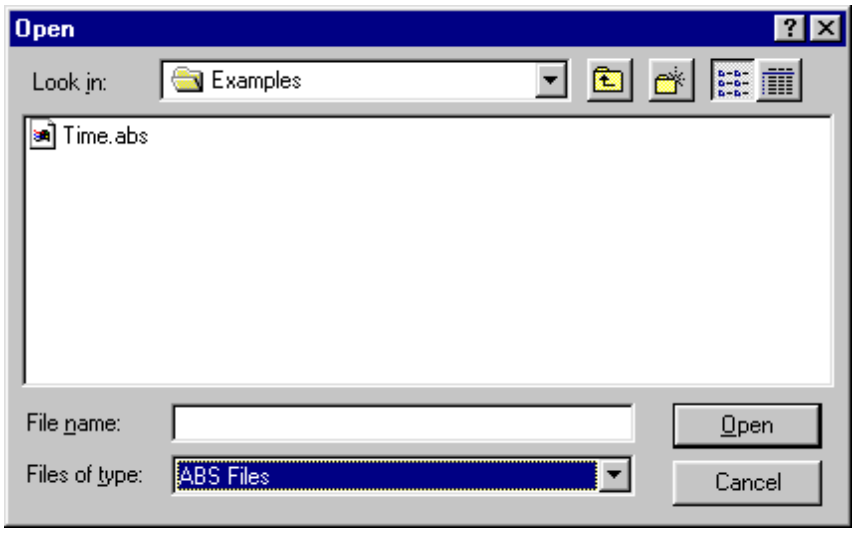


Figure 9. Open Dialog Box

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7. Right-click on the Source window with **time.c** tab selected and select **Mixed Mode**. You will see assembly code mixed in with the appropriate source lines as in Figure 10. Note the program counter (IP) indicated by the blue blocks at the start of MAIN.

8. Remove the Mixed mode from the Source window so only the C source code remains.

9. Click on the Source Step Into icon repeatedly and the program counter will advance through the CPU initialization code. Note that where there is assembly code only, the steps are at that level.

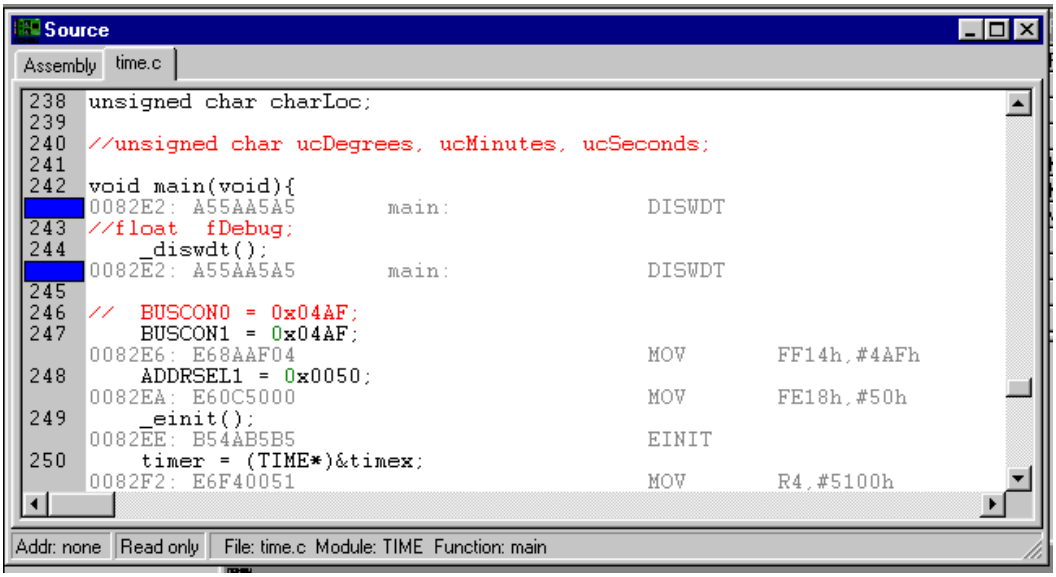


Figure 10. Source Window

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4 Viewing Data in Real-time With Shadow RAM

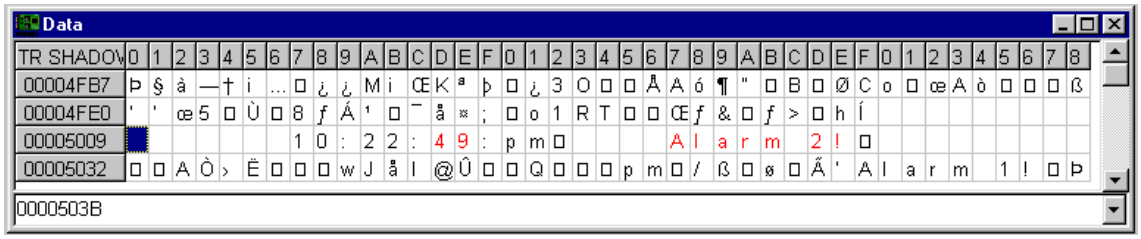


Figure 11. Data Window

The Shadow RAM feature allows you to view memory contents in real-time without stealing cycles from the emulation CPU. This example assumes you have completed all the steps so far in this guide and that Time.abs is still loaded in your emulator. If the data does not display correctly, make sure all the CSx chip-select entries are cleared. These entries are found in the **Mem Map Config** tab under the **Config**, **Emulator** menu item.

1. Open a Data window either by clicking on the Data icon or from the **New** menu, selecting **Data**. A window similar to Figure 11 will open. The data will be in hex: not ASCII as shown. Resize the window as needed.

2. In the address box at the bottom, highlight the existing address and type `5000`. Press ENTER.

3. Right-click on the Data window to open the submenu (Figure 12). The idea is to change the Data window to display the data in ASCII format and retrieve from the Trace Shadow RAM.

4. Select **Display As** and select **ASCII**. Note the viewing options available in this window.

5. Click **OK**.

6. Right-click again and select **Address Space**. Then select **TR SHADOW**.

   The addresss at the bottom represents where the mouse is pointing to. The box highlighted in blue at location 5009 in Figure 11 is the last location where you clicked the mouse on. Data in red indicates that which has been modified by the last instruction executed. You will not see ASCII data shown if Time.c has not been appropriately initialized at these locations.

7. Click on the GO icon or press F9. The program Time.c will run.

   The time will be updated in real-time. No CPU cycles are stolen to accomplish this. Time a little fast ? This program was written with timer values for a 20-MHz clock. It ought to run a little faster at 50 MHz.

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Figure 12. Data Submenu

Explore around Seehau a bit. Seehau has many interesting and useful features. If you want to go on to Chapter 5, “Trace Memory Example,” don’t change any settings. You will need the present settings to continue.

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5 Trace Memory Example

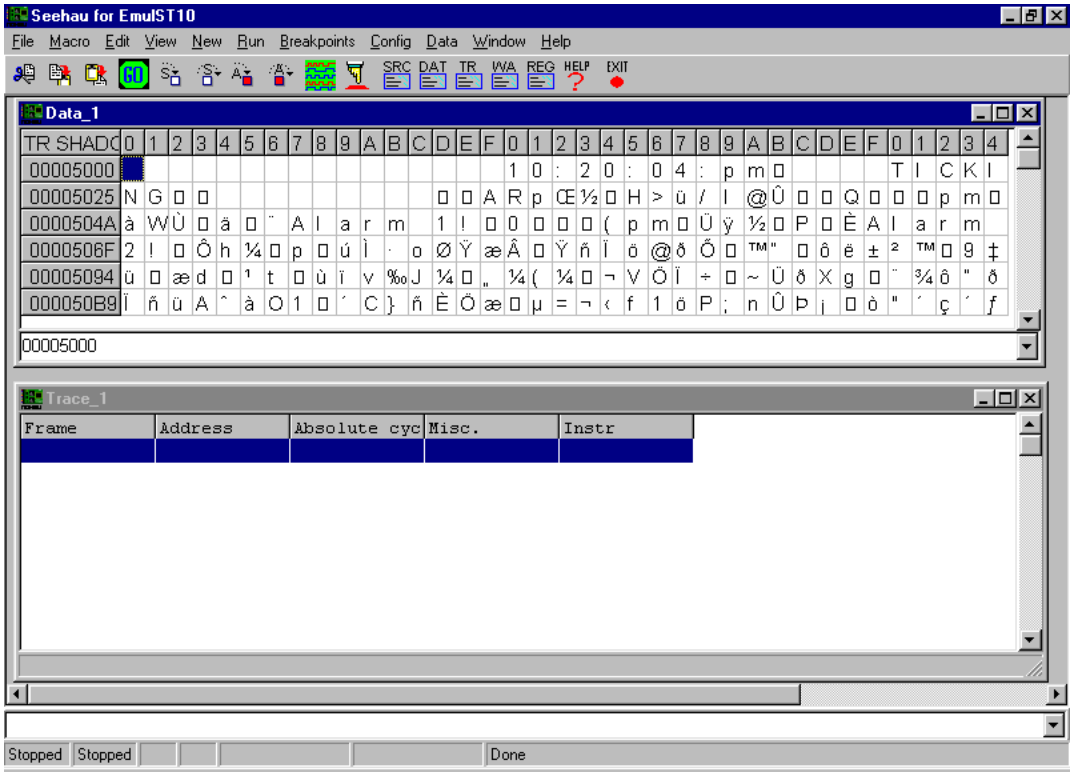


Figure 13. Trace and Data Windows

This chapter discusses trace memory and describes how to set up a trigger to start and stop the trace memory, and stop program execution.

Shadow RAM provides memory contents in real-time. There is no cycle stealing from the emulation controller. While the Time.c program has been running, the trace memory has been operating in the background, also in real-time.

Many emulators can not view the trace without stealing cycles or even stopping the emulation. The Nohau emulator can do this in real-time. It uses a 25-MHz dedicated microcontroller to do all the trace, trigger and Shadow RAM housekeeping chores, rather than stealing cycles from the bondout controller.

1. Ensure the the emulator is running the Time.c program. The two boxes in the bottom left hand corner of the main window will contain **Running** instead of **Stopped** as shown in Figure 13. The GO and TRACE icons are both red in color. You should have the Data window open and displaying the time changing in real-time as shown in Figure 11.

2. Open a new Trace window. You can click on the New Trace icon or from the **New** menu, select **Trace**.

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3. Position the windows similar to Figure 13. You should have the Trace and Data windows visible. The Trace window might have some data recorded in it or empty. This depends on previous emulation runs.

   Note the Trace window is empty as the trace buffer is being filled. It is not possible to view the trace contents at this time. The bar at the bottom of the Trace window will show that the trace memory is already full and how many triggers have occurred. There are no trigger events (Figure 14).

4. Click on the Stop Trace icon. Note that while the changing time values might appear to stumble: this is only in the display. The emulation controller was not slowed down at all. This is genuine real-time operation.

5. The Trace window now contains recorded controller cycles. Figure 14 shows the trace memory. You can add some columns by right-clicking on the Trace window and selecting them.

   Note that in Figure 14 labels, registers and addressing modes are all displayed. Note the Trace window can display the C source code with the resulting assembly code.

6. Start the trace memory by clicking on the Start Trace icon. Note the time does not stop or slow down. Once again, the trace memory is being continously overwritten with new values. The trace memory is a circular buffer. This will continue until the recording is stopped either manually or with a trigger event. The triggers have the ability to start and stop the trace recording.

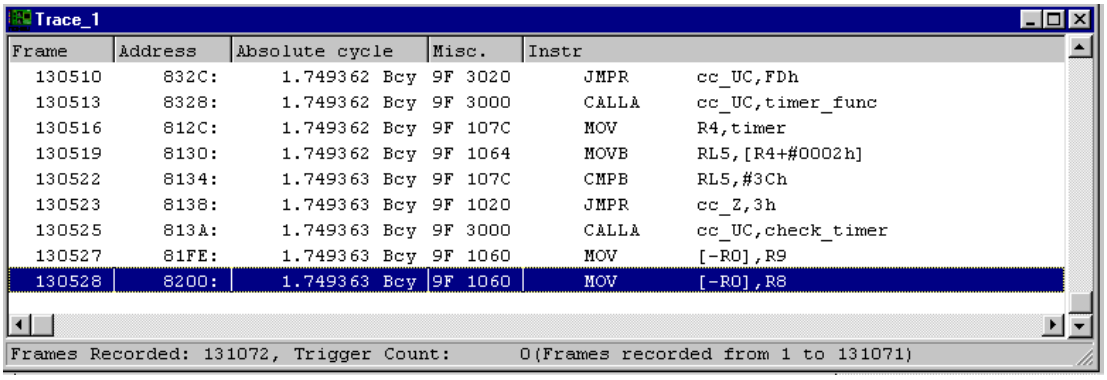


Figure 14. Trace Window Displaying Trace Memory

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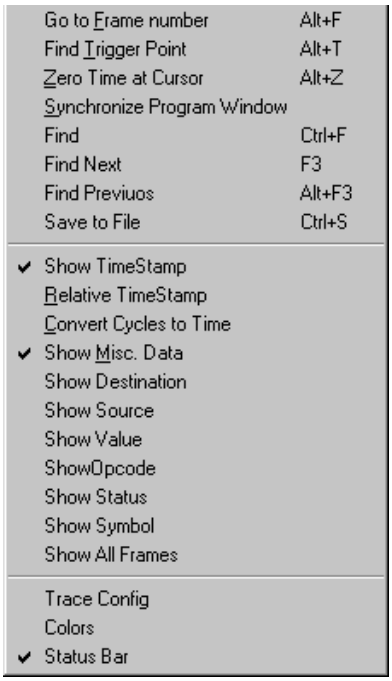


Figure 15. Trace Submenu

The Trace window can display many types of information about the bus cycles. Right-click on the Trace window or from the **Config** menu, select **Trace**. The submenu opens (Figure 15). Click on some of the options to see the various fields available.

The ST10 emulator has extensive trigger facilities to start and stop the trace as well as perform program breaks. The triggers can control cycle recording so that only specified cycles are recorded. The apparent size of the trace memory can be magnified many times by using carefully selected trigger qualifiers. The triggers can also send out external signals.

External events can be recorded in the trace (8 bits) or used as trigger qualifiers.

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6 Setting an Example Trigger

The EMUL–ST10 offers trigger capabilities. You can configure the triggers in real-time. The triggers test for qualified events and start and stop the trace without stealing cycles from the emulation controller. The application program runs at full speed. A break in emulation, by definition, affects real-time operation. This example shows how to set up an effective trigger. The emulation will stop when the seconds MSB memory location is written the value of 4 ASCII (34 hex). The bus cycle responsible for this write will be recorded in the trace memory.

To set up a trigger do the following:

1. Configure Seehau to get a main window similar to Figure 13. Stop emulation and click the Reset icon.

2. From the **Config** menu, select **Trace**, or right-click in the Trace window and select **Trace Config**.The **Trace Configuration** dialog box opens displaying the **Trace Setup** tab (Figure 16).

   There are two versions of the trace setup: Standard and Advanced. Click on **Advanced** to view the Advance features (the button now reads **Standard**). Click on **Standard** to select the Standard version.

   Note there are seven levels of triggers plus a Group (Advanced only). Level 1 is used in this example. The red dot changes to green once you have entered and enabled the qualifier for Level 1.

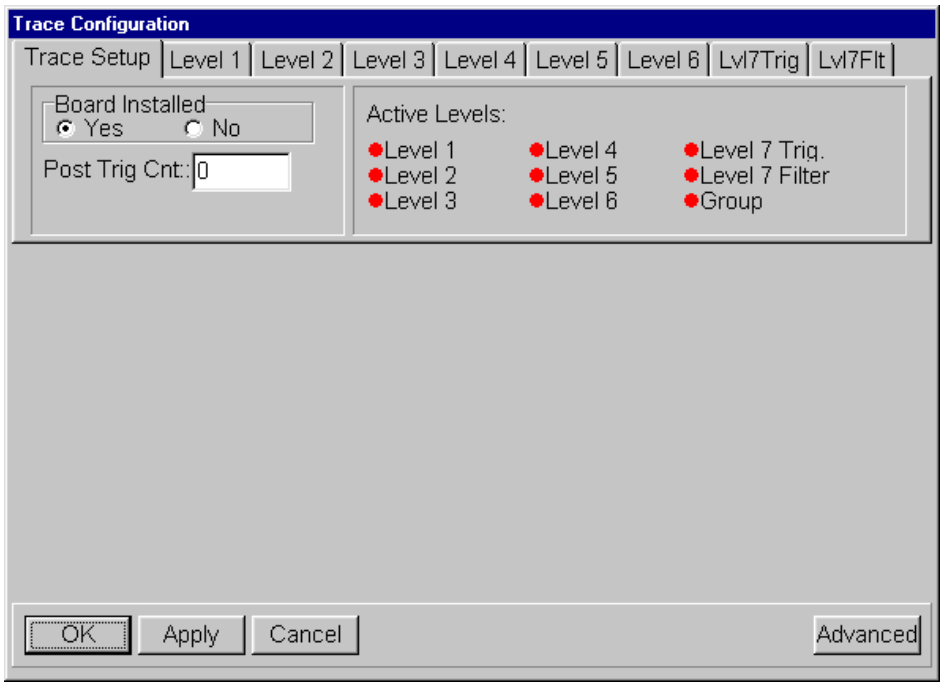


Figure 16. Trace Setup Tab

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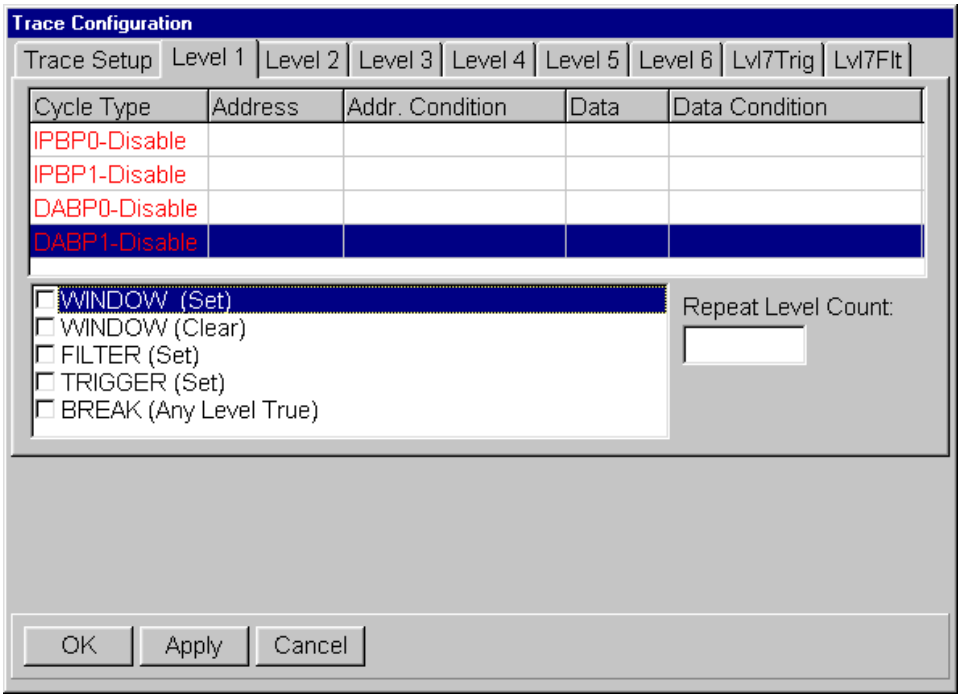


Figure 17. Level 1 Tab

3. Click on the **Level 1** tab (Figure 17). IPBP0 and IPBP1 are address only qualifiers. DABP0 and DABP1 are address and data qualifiers. DABP0 and DABP1 are used in this example. All qualifiers are disabled at this point. (See Chapter 8, "Trace Memory and Trigger Mechanisms" for more information.)

4. Click on the DABP0 line and right-click on the highlighted line. The **Edit Cycle Type** dialog box opens (Figure 18).

5. Enter the fields as shown and ensure the **Enabled** option is selected. Address and data are not case sensitive.

6. Fill in the **Address**, **Data**, **Data Mask**, and **Write** text boxes. The Enabled will load itself. Then click **OK**.

   A modified Figure 17 will open. Note that both DABP0 and DABP1 are enabled with the appropriate data. The qualifier is now properly set. DABP1 has a window similar to Figure 18.

7. Click on the DABP1 line and right-click to open the menu. Confirm it has the same settings as Figure 18.

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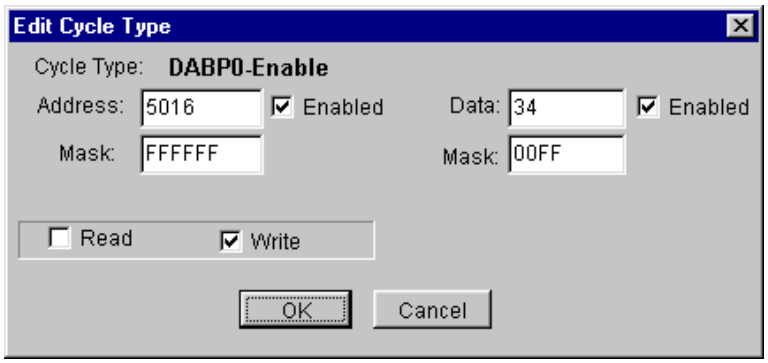


Figure 18. Edit Cycle Type Dialog Box

8. Enter 1 in the **Repeat Level Count**. This box must have a value of at least 1 or no trigger will occur. The **Repeat Level Count** is the number of times an event must occurr before a trigger (action) will happen.

9. Select the **Break (Any Level True)** and **Filter (Set)** options. This will break the emulation and record only that cycle which caused a write of 34 to memory location 5016.

10. Click **OK** to close the **Trace Configuration** dialog box. You should have a Trace window that looks similar to Figure 13.

11. Click the GO icon in the Seehau toolbar to start emulation. When the value at address 5016 becomes ASCII 4 (hex 34), the emulation will break and the cycle will be displayed as shown in Figure 19. Only one line is shown since that is the program stopped at the first event.

12. Right-click in the Trace window to open the submenu. Right-click and select **Show Destination**, **Show Value** and **Convert Cycles to Time** to get the same fields as shown in Figure 19. Note that address 5016 and data 34 are recorded.

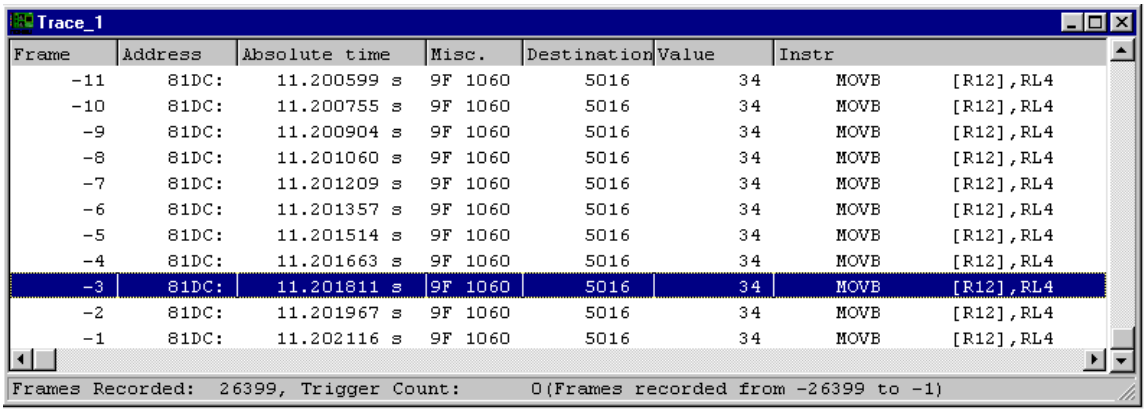


Figure 19. Trace Window Displaying Cycle

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13. In the **Level 1** tab, clear the **Break (Any Level True)** option so the emulation will not be stopped.

14. Click on the Reset and GO icons to restart emulation. You can also make this change on-the-fly without losing real-time performance.

15. Note the number of cycles recorded in the trace memory increasing as the value in 5017 equals 34. This information is shown at the bottom of the Trace window. Stop the trace by clicking on the Trace icon and the cycles will be displayed as in Figure 19. Each cycle has a timestamp indication when it occurred.

16. Open the submenu and enable some more fields. Not all cycles have been recorded: only those selected in the trigger qualifiers.

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7 POD–ST10, Rev. A

The pod information is clearly marked on the upper side of the board near the power connector. Figure 21 shows the location of the various jumpers and test points.

LED Indicators

Normal operation with emulation stopped has L3 RUN illuminated. All other LEDs will be off. With a user program running, L3 will go out. The red RESET LED L2 lights when Seehau is performing a system reset.

Function	Description
L1: USER	This is a yellow LED the user can affect by applying standard TTL levels to TP3. TP3 is active low - grounding TP3 turns on L1.
L2 RST: RESET	This red LED indicates the application of a reset signal by the Seehau software. The emulator will be in the reset state when powered with a 5-volt supply but without a cable connected to the PC connector J7. You can reset the emulator by selecting **Reset Chip** in the **Run** menu or clicking on the RESET icon on the toolbar. The commands Run_Reset and Run_Fullreset will also reset the emulator. These commands can be entered in the command dialog box or through a macro.
L3: RUN	This green LED indicates whether the Nohau monitor program or a User program is running. L3 illuminated means the user program is running.
L4 PWR_ERR: Power Error	If this LED lights, the correct 5-volt supply is not connected. This can occur if the 5-volt regulated supply is not connected to J2 and the PC communications connector J7 is connected. L4 is a red LED.

Emulator Pinouts

Designation	Function	Description
TP1	**Breakout**	This output indicates if the emulator is in Monitor mode or is running user code. It is connected to the RUN LED L3. This output is usually used for customers who have multiple emulators connected to the target board. It provides a means to synchronize them together. TP1 is high when the Nohau monitor is running.
TP2	**GND**	The emulator ground connection and a black ground wire with a clip is soldered to this point. Connect this clip to a secure ground (or earth) connection on your target hardware. Do this before connecting the emulator processor pins to the target.
TP3		This input activates LED L1 USER. TP3 is active low: this action turns L1 on.
TP4		Not present.
TP5		This test point is used to program a serial EEPROM. There is no user use for this connector.

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Designation	Function	Description
JP1, JP2	**XTAL1, XTAL2**	These jumpers determine whether the on-board pod clock (U2) or the target clock is used for emulation. These jumpers must be changed in tandem as a pair. The default is set to the Pod position (the upper positions) and U2 provides the clock signal to the pod controller. The pod will supply the clock to the target if you jumper all three of the pins together. In this case, make sure the target clock is disconnected.
JP5		Reserved for future emulator enhancements.
JP22	**T PWR**	+5 volts is supplied from the pod power supply through JP22 to the bondout controller. During normal operation with a target board, 5-volt power for the bondout controller U1 will be supplied by the target and JP22 must be removed. The pod power supply must still be connected to supply power for the rest of the emulator. JP22 is used for stand-alone operation (without a target board). JP22 will send power to the target if left jumpered. If the target has power, this can cause a conflict so JP22 must be removed. If the target has no internal power supply, the pod is able to supply a small amount, less than 500 ma, to power the target. This can be useful for very small targets with low current consumption. **Note**: When powering up or down the system: the target must never be powered when the pod is not. Power flowing from the target into the bondout controller can damage it. Always power up the pod first, and power it down last. Do not leave the pod powered up without the target power applied for more than two minutes. This situation stresses the I/O circuitry of the bondout chip and will cause permanent damage. Do not leave the pod powered without the Seehau software running it. The pod will be in an uninitialized state with unpredictable results.
JP25		This unpopulated connector is used for testing the pod by Nohau. Pin 6 (ECLK) can be used to measure the CPU clock frequency. This pin is the second from the end of the pod board closest to L1, the USER LED. Pin 7 (EMUL#) indicates if the pod is in User or Monitor mode. This pin is closest to the edge of the board. This signal is connected to the RUN LED. The rest of the pins provide no useful information.
JP26	**EPC PWR**	This jumper supplies the EPC with 5 volts. If this special cable is not used, remove JP26. The ISA board does not need power from the pod and JP26 must be removed.
JP32		This 8-pin connector is used by Nohau to program a serial EEPROM and to supply power to the cooling fans. It has no user use.
J1		This connector connects to a small daughterboard to supply XBUS peripherals not supported by the bondout controller. This allows the emulation of derivatives not yet introduced and prevents obsolescence of the emulator. Some of these signals will be sent to the target through JP10 on the underside of the pod.
J5, J6		The optional trace memory board connects to these two connectors.
J8, J9, J10, J11		Connection of the bondout controller signals to the target. This is an industry standard connector and can be directly connected to appropriate target boards or through various adapters available from Nohau.
JP10		This 10-pin connector is used to send XBUS peripheral signals from the optional daughterboard to the target.

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Edge Jumpers

These jumpers are listed in physical order.

Designation	Function	Description
JP23	**READY**	This jumper connects the READY input signal between the target and the pod controller. The READY signal is used to terminate a bus cycle and is useful when external devices have a long or indeterminate access times. READY is activated in certain address ranges as determined by the BUSCON registers. If the READY signal is not asserted for a bus cycle that it is activated for in BUSCON, the processor will stop. Only a reset or a watchdog timeout can restore operation at this point (or the assertion of READY). Since the bondout controller on the pod is used for some housekeeping when emulation is not running, suspending it can cause Seehau to stop responding. Remove JP3 to prevent this. The default is JP23 connected.
JP24	**RST#**	This jumper connects the pod and target reset pins together. The RST is the master reset pin. A target peripheral with the ability to assert this signal might not be desirable. Remove the jumper on JP24 to prevent the pod controller from being reset from the target. JP24 is connected in by default. A reset on the pod controller will not be passed to the target board.
JP6	**AUTOMAP**	This jumper determines whether memory mapping is controlled by Seehau or the chip select pins setup contained in the ADDRSEL1 through ADDRSEL4 registers. The **Mem Map Config** tab shown in Figure 20 is in the **Config** menu. AUTOMAP determines whether the numerical addresses specified in the window or the chip selects selected are passed to the target board. The default is JP6 not connected.
JP27 … JP31		The controller provides five programmable chip select pins (CS0-CS4) that are output on parallel Port 6 if so programmed as an alternate function. These are pins P6.0 through P6.4. If these pins are not used as chip selects, they can be used as general purpose I/O ports. JP27 through JP31 connect these five pins to the target. They do not create the mapping signals from the chip selects as in previous Nohau emulators. All mapping is done in the pod controller U1. The default is JP27 through JP31 connected.
JP20	**P3.12 or BHE**	If you configure P3.12 as an I/O pin, place JP20 on the P3.12 side (upper position). If you configure P3.12 as either BHE or WRH, place JP20 on the BHE side (lower position). The default is BHE (lower position). In the process of mapping sections of memory to the target, the RD, WR and BHE signals are not passed to the target directly. The mapping function of the emulator switches off the pod memories as required. However, as the signals map memory access to the pod, it gates off the RD, WR and BHE signals from the bondout controller to the target. When P3.12 is configured as a standard I/O pin, you would not want it gated off by the pod logic. When the jumper shunt is in the P3.12 position, it passes directly from the bondout controller to the target. When the jumper shunt is in the BHE position, P3.12 gates off and pulls high during memory accesses to the pod as required.

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Designation	Function	Description
JP16 … JP19		XP4.4/P4.4 through XP4.7 through P4.7: These jumpers select whether the upper four bits of Port 4 supplied to the target come from the bond-out controller or from a daughterboard connected to J1. The default is all jumpers are set to P4.x (the lower positions). The XBUS is an internal representation of the external bus. This bus is used internally to connect various peripherals to the CPU. These peripherals look like external devices to the CPU even though they are on-chip and are accessed as such. Internal peripherals are also on the XBUS. The bondout controller U1 used for emulation contains most peripherals. If a certain XBUS Peripheral is available on the bondout chip on the pod, then this peripheral will be used to provide the peripheral to the target. For those derivatives that use peripherals not on the bondout controller, a daughterboard connected to J1 will contain a regular series controller that contains this XBUS peripheral. JP16 through JP19 must be set so these signals are sent from the daughterboard to the target (XP4.4 through XP4.7 - the upper positions).

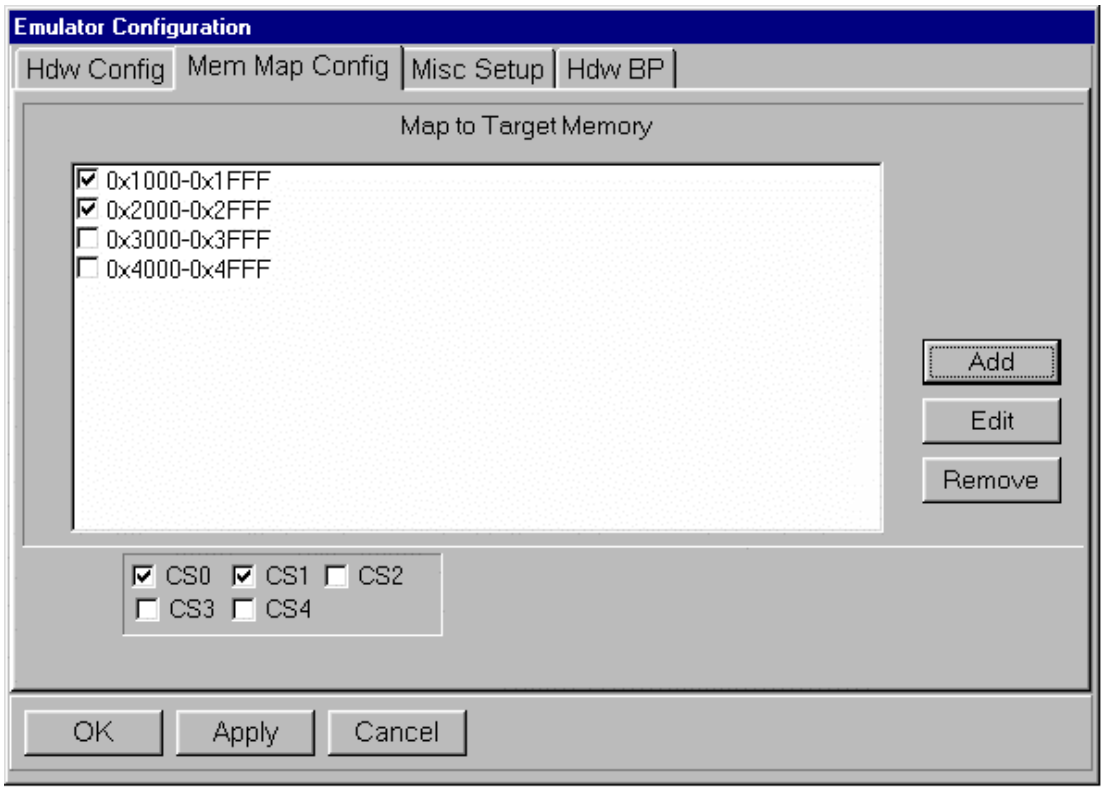


Figure 20. Mem Map Config Tab

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Default Jumper Settings

This list is for stand-alone operation without a target connected. Do not change any jumpers on the trace board.

Pod Board

- JP1 and JP2—Upper position (Pod)
- JP32—Fans connected to this jumper (for ST10)
- JP22—On
- JP26—Off (On if using the EPC)

The 13 jumpers on the edge of pod board are all connected. If a jumper has three pins (JP16 to JP20), the position is lower or close to the circuit board.

Trace Board

The TP4 jumper is installed at the end of this connector close to U23. Do not change this jumper.

There is a three-position jumper near the gold trigger in/out connectors. This jumper should be in the position closest to the gold connectors. Do not change this jumper. It selects power voltages and your pod might not survive. There is no warranty for this easily identified condition.

Trace User Input Connector: J1

The trace board contains a 15-pin D shell connector. Refer to Figure 2 for its location. This connector provides eight user input signals to be recorded in the trace memory under the Misc. column. These are TTL level inputs. The Trigger In (J3) is also available on this connector. A special socket with clips is available from Nohau as part number TR167 Probe. The pin assignments are as follows:

Pin	Name
1	Vcc 5-volt
2	External In 0
3	External In 1
4	External In 2
5	External In 3
6	External In 4
7	External In 5
8	External In 6
9	External In 7
11	Trigger In
15	Ground

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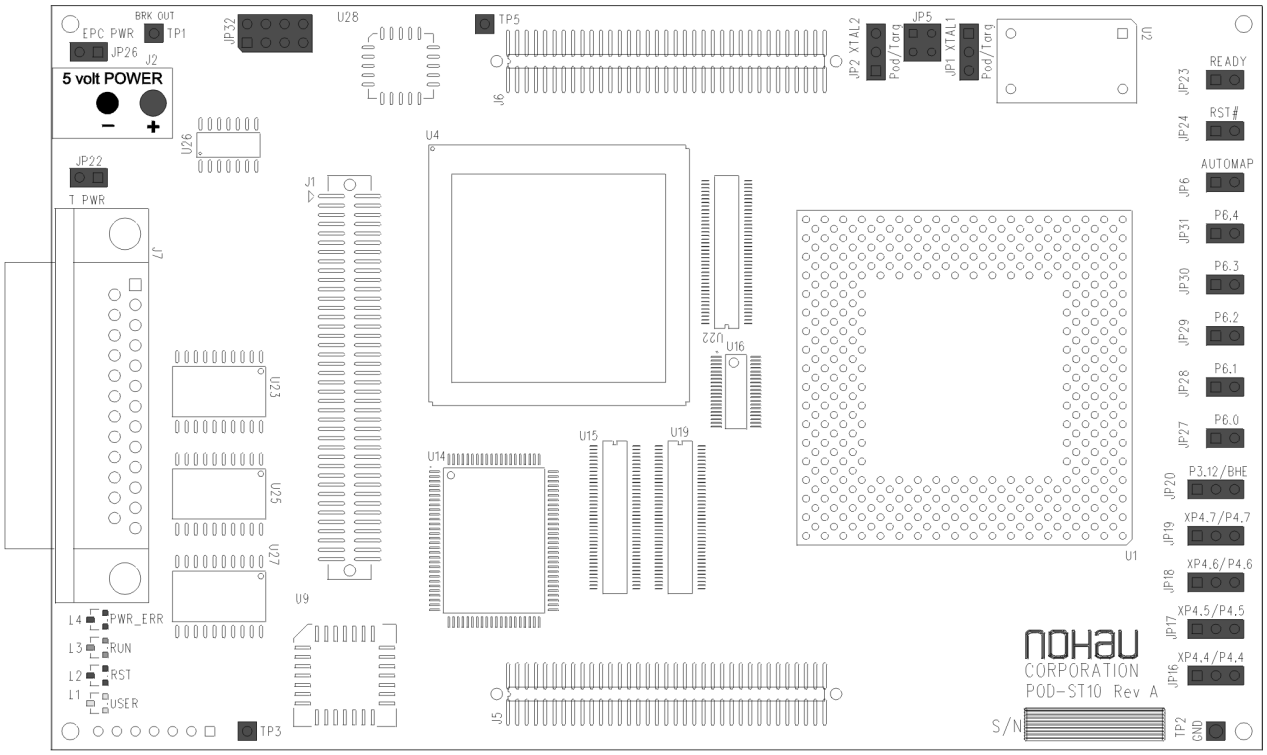


Figure 21. POD–ST10, Rev. A Board Layout

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8 Trace Memory and Trigger Mechanisms

Overview

The Nohau EMUL–ST10–PC is an advanced emulator with speeds of 50 or 80 MHz. This chapter describes the trace and trigger configurations for the 50-MHz version. The 80-MHz version is slightly different and is covered in *Application Note #103*. The EMUL–ST10–PC supports all ST10 derivatives plus many from the Infineon C166 family such as the C167, C161 and C163. It does not support the Infineon C164 or the C161U.

The EMUL–ST10–PC uses a compact two-board design for decreased weight. One board contains the bondout controller, adapter connections and support logic. The second board is the optional trace memory which includes Shadow RAM and triggers. This chapter discusses the configuration of the trace board.

The trace board contains hardware and firmware for the trace memory, triggers, hardware breakpoints, performance analysis, code coverage, external triggers (in and out), and an general purpose user output connector. The trace board contains its own housekeeping microcontroller. This allows the trace to be started and stopped and other functions to be operated without stealing cycles from the emulation controller. Nohau trace boards can be configured and viewed in real-time and on-the-fly.

Figure 22 gives an overview of the trace and trigger mechanism. There are four basic trigger mechanisms present in the EMUL–ST10–PC as shown in Figure 22. They are Level 1 to 6 Breakpoints and Triggers, Level 7 Trigger, Level 7 Filter and the 16-Instruction Pointer Control. This mechanism provides for the hardware breakpoints but not the software breakpoints. The trace card is optional and can easily be added later.

Qualifier data can be entered as addresses, data, SFRs and external signals. They can be entered as numerical hex values or symbols, all with additional values. For example, Timer. sec +6 is valid. These are combined and compared in each of the four selection mechanisms and sent to the trigger state machine. These signals from the selection mechanisms are then combined in an AND/OR output array and then sent to the emulator hardware. The external input signals are sent to each of the six levels of breakpoints if they are enabled.

Levels 1 through 6 and the Instruction Pointers (IP Control) are provided by the ST10 bondout chip. Level 7 Filter and Trigger are Nohau proprietary trace functions. Levels 1 through 6 will be discussed later in more detail. The six levels can be operated independently or can be pre-qualified by the preceding level. For example, in order for Level 6 to happen, it can be configured such that Level 5 must have already occurred, or each level can be independent of the other.

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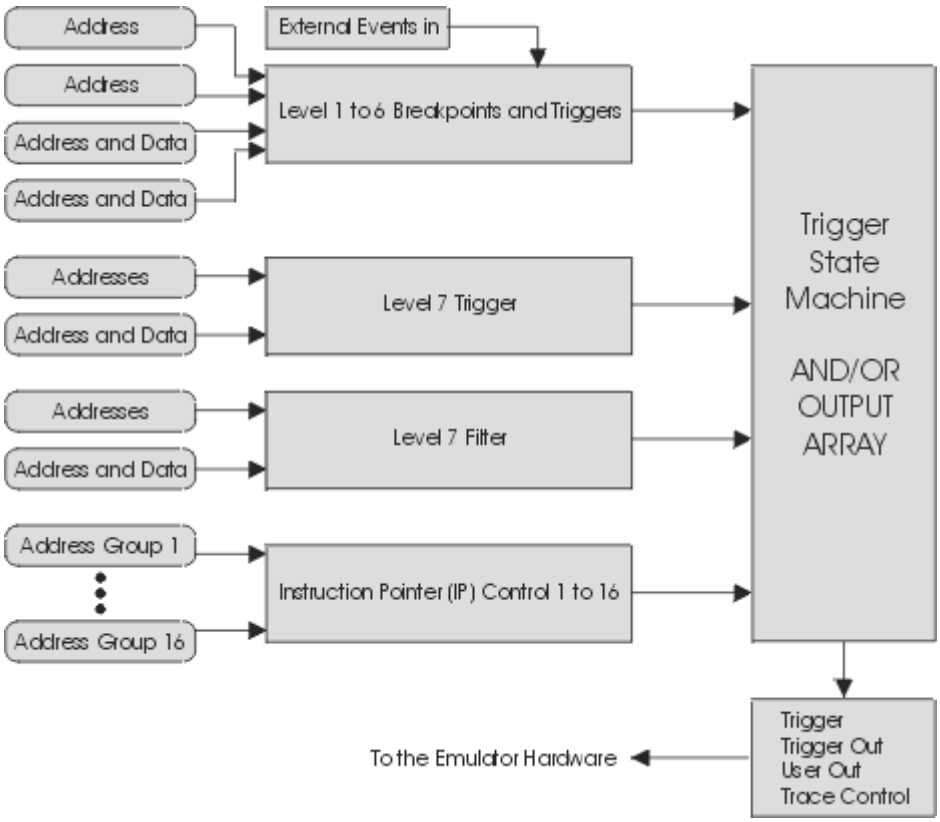


Figure 22. Trigger Mechanisms Diagram

There are two general modes of operation: Standard and Advanced. They are selected by the button found at the bottom right corner of Figure 23. The Standard mode presets some of the Advanced mode settings making setting up simpler. The Advanced settings offer all the features of the ST10 bondout. This guide uses the Advanced setting throughout. The Standard setting will remove many of the window boxes from view. These fields are preset with default values to simplify trigger setup.

Note the trigger configuration screens were changed during November 1999. The previous mnemonics were changed to intuitive English phrases. A translation table is provided at the end of this chapter. Existing macros will not be affected by these changes.

You can use the triggers to perform these types of operations:

- Break emulation if a specified address and/or data pattern is encountered.
- Record specific CPU cycles in the trace buffer.
- Determine if certain operations take too much or too little time to execute.
- Calculate the time taken for a specified operation such as a function or functions.
- Start and stop the trace recording.
- Send a signal out as certain conditions happen or cause an external input to cause a trigger.

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- You can save any number of trace configurations and easily recall them with a button.
- Various combinations of qualifiers are possible to provide sophisticated qualifiers.
- Temporarily “park ”a trigger with a click.

Trace Setup Tab

You can open the **Trace Configuration** dialog box displaying the **Trace Setup** tab (Figure 23) by either selecting **Trace** from the **Config** menu, or right-clicking in the Trace window. The **Trace Setup** tab shown in Figure 23 is for the ST Microelectronics ST10 family. Tabs for other CPU families will be similar. This discussion is for the Advanced mode. The Standard mode has many of these values either not available or have unchangeable default values. Click on the button in the bottom right corner to switch modes.

Trace Type—This field indicates to Seehau if the trace board is installed. There is one type of trace board so you do not need to specify anything other than it exists or not. In the EMUL–ST10–PC emulator systems, trace memory is an optional add-on board to the emulator pod. The Trace_TraceBoard command is found in the Startup. bas file which is executed when Seehau software is started and specifies this attribute.

Active Levels—The status of the various levels is indicated here. A red dot means the specified level is disabled while a green dot indicated it is enabled. A check box in each qualifier in each level tab is used to toggle these values. The various levels are discussed later in this guide.

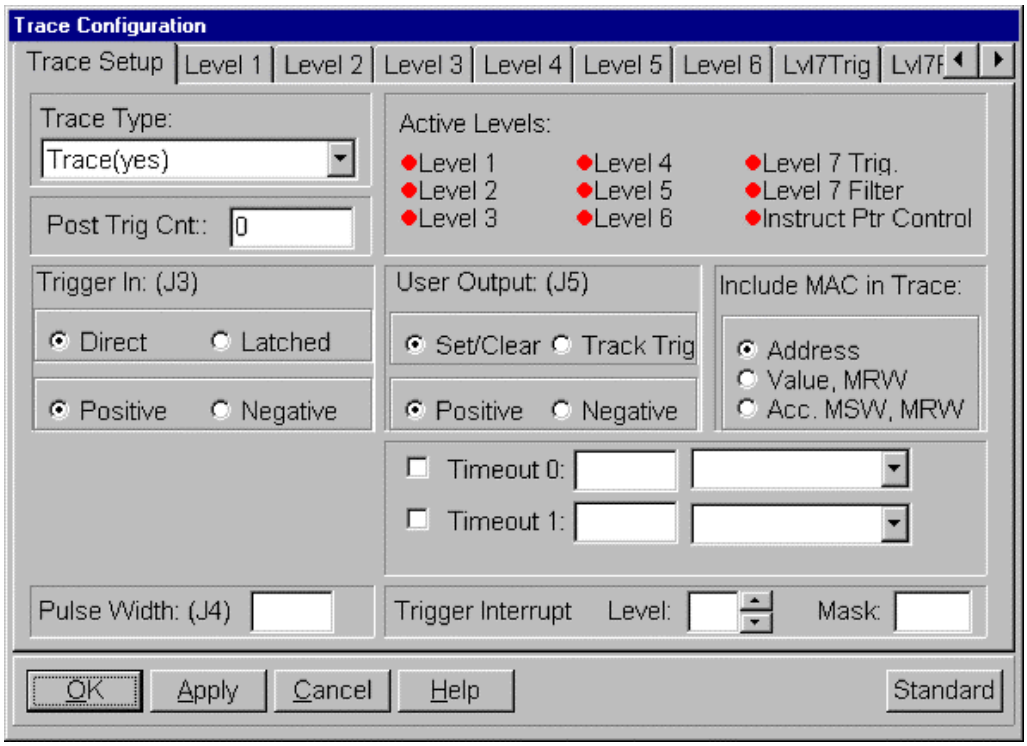


Figure 23. Trace Configuration Dialog Box Displaying the Trace Setup Tab

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Post Trig Cnt—This selects how many frames are recorded in the trace memory after the trigger has occurred. Triggers are programmed to occur when a particular condition is true. Example: address 500F is written with the value 5E. This can be viewed as the "when something happens." When this becomes true, the emulator performs the action you have programmed. This could be to break emulation, start or stop the trace or send an external signal to the outside world. Look at this as "what will then be done."

This can be useful to see what happened not only before the trigger occurred, but also what happened afterwards. If this is set to 7 for example, then the trace will record the cycle of interest plus the next six cycles that follow. The exact number of cycles recorded can vary a small amount depending on the state of the CPU pipeline which is fully decoded in the EMUL-ST10 emulator. A decimal number is entered up to 128K.

Trigger IN:(J3)—An external TTL level signal can be used as an input to cause a trigger. This connector is J3. This input signal can be positive or negative edge sensing according to the setting selected here. The signal can either be latched or free floating (Direct) according to the setting selected. This signal is sampled during each processor frame and cleared at this time.

Trigger OUT (J4)—There is a trigger output connector (J4) on the trace board that is pulsed when a trigger occurs in a level when the "Trigger -stop trace and pulse Trigger Out "is checked in that level. The trigger OUT will be active even after the trace has stopped.

Pulse Width—This box sets the pulse width of the pulse sent out J4. This value is 5 bits and is entered 1 to 20 Hexadecimal (1 to 20)and its units are in CPU cycles. A "1 "gives a pulse width of approximately 140 ns and 20 gives 2. 2 usec. This results from a 50-MHz CPU clock. This sets the USER OUT width also.

User Output (J5)—There is a USER output connector (J5) on the trace board that can be set or cleared according to how it is set in the triggers. This area in Figure 2 sets the characteristics of this TTL level output. This output works even if the trace has been stopped.

- **Pulse Width**—See Pulse Width above for details.

- **Set/Clear**—If Set/Clear is set, the value of the USER output will change according to the **Turn User output ON** and the **Turn User output OFF** options in the Level tabs which are discussed later. When this output is turned on it will stay in this state until the **Clear** option occurs. Normally two triggers are used to turn the USER off and on. This feature is mutually exclusive to the **Track Trig** feature.

- **Track Trig**—**Track Trig** provides for an output pulse that is active only when the trigger condition is true and the **Turn User output ON** option is selected. The output waveform tracks the state of the trigger. This occurs on a cycle by cycle basis. The pulse width is selected in the **Pulse Width** field.

- **Positive/Negative**—The polarity of the output can be selected either positive or negative and is effective for both the **Set/Clear** and **Track Trig** options.

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Timeout—There are two 12-bit timers used to create a true trigger condition if an event's timing is over or under a user selected number of CPU instruction cycles. Examples: an ISR (interrupt service routine) takes too long (or too short) to occur or takes too long (or too short) in its execution time. These timers are 12 bits in length and values from 0 to 3FF can be entered.

There are two **Enable** options located just before **Timeout 0** and **Timeout 1**. The next box is for the timeout value in instruction cycles of the target CPU. The last box holds values for the prescaler of the timers. The prescaler value is selected by clicking on the arrow and clicking on the appropriate selection. Values are divide by 1, 2 ^10, 2 ^20 and 2 ^30. The timers are selected under the Level tabs.

Trigger Interrupt Level & Mask—This gives the trigger state machine a priority within the microcontroller interrupt structure. This setting can be used to block a trigger when a interrupt service routine is at a lower level than the trigger state machine. The trigger state machine is essentially the entire trigger mechanism of the ST10 bondout controller. The level can be set by priority number (Level) or can be bit selected on a level by level basis (Mask).

Include MAC in Trace—This selects which information from the ST10 MAC unit is recorded in the trace memory. This box and the selections made are valid only during the execution of a MAC instruction.

- **Address**—The operand address of the MAC instruction is recorded.
- **Value, MRW**—The operand and the MRW (MAC Repeat Word) are recorded.
- **Acc. MSW, MRW**—The Accumulator, MSW (MAC Status Word) and the MRW (MAC Repeat Word) are recorded in the trace buffer.

Level 1 through Level 6 Tabs

The ST bondout processor provides for six levels of triggers. These are represented by the six Level tabs in Figure 24. These six levels are provided by the ST bondout chip and are controlled through the Seehau interface. Level 1 is shown selected in Figure 24.

The six levels are equal in priority to each other unless the **Previous level must become true first** option is selected. Associated with each level are two data qualifiers and two address qualifiers. These are shown as "Level 1 to 6 Breakpoints and Triggers" in Figure 22. You can include external signals, other levels (even itself), flags, timers and an external input. Figure 25 is a block diagram showing one of the six levels. Figure 26 is the same block diagram but with the Preset Address AND Data mode selected. The only difference is the two AND and one OR gates that are selected in Figure 26. This mode allows an address qualifier to be ANDd with a Data qualifier.

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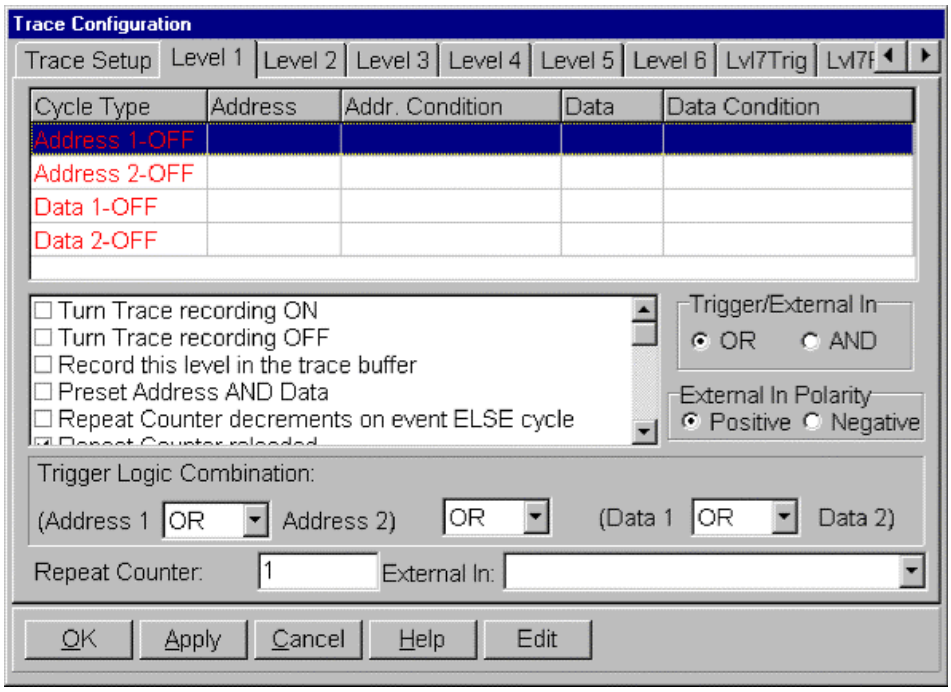


Figure 24. Level 1 Tab

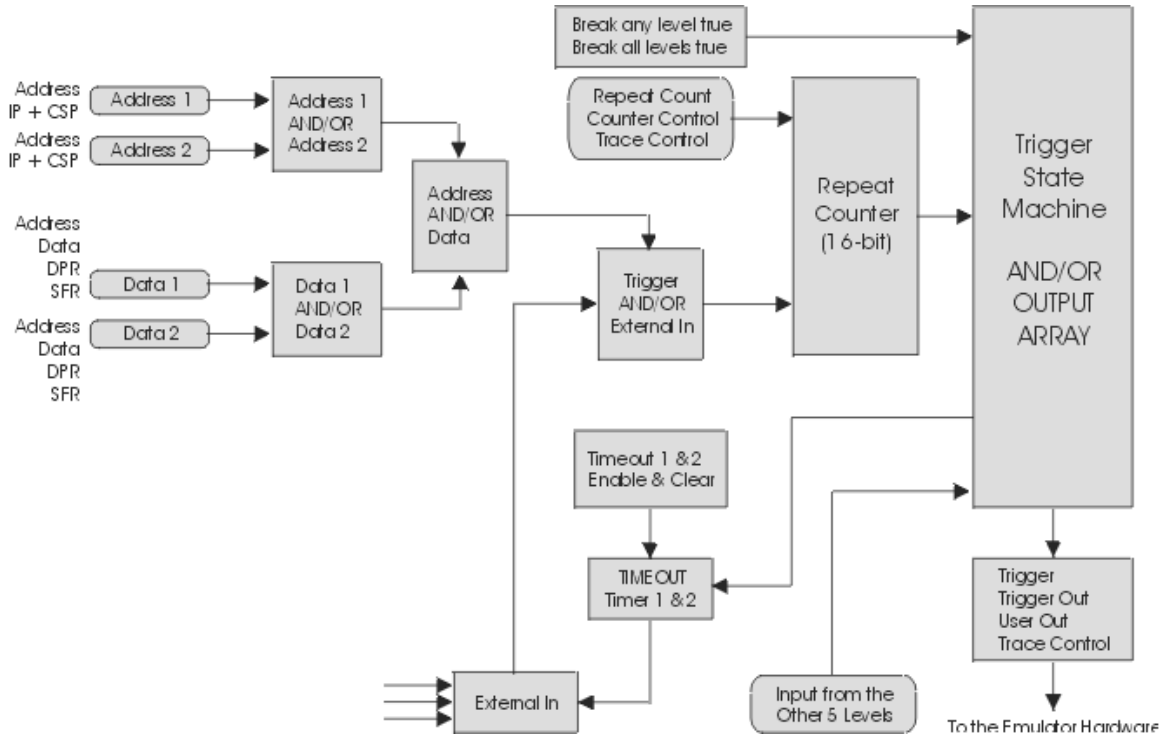


Figure 25. Nornal Address AND Data Mode Diagram

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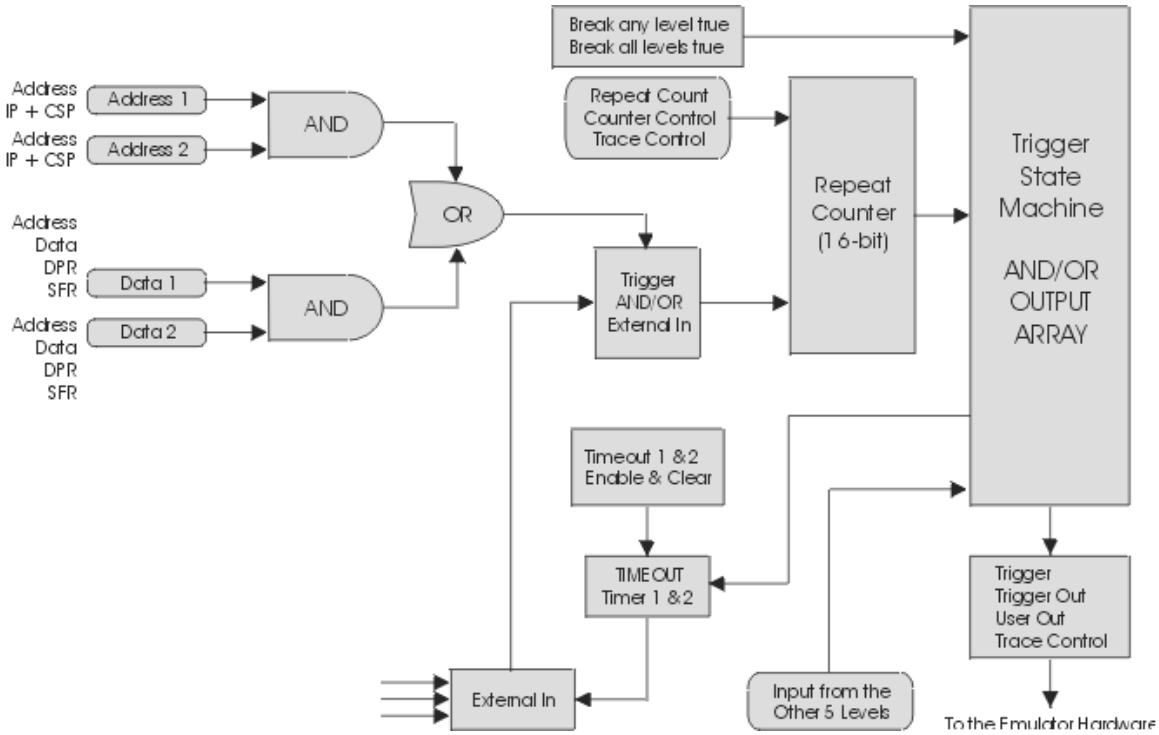


Figure 26. Preset Address AND Data Mode Diagram

Definitions

Qualifier—The specifications that partially define a condition you want to examine. “If address =5012 ”is a qualifier. “If address =5012 AND data write =FE ”is also a qualifier. You can make many types of qualifiers.

Event—This is the qualifier becoming true. You now choose what is to be done.

Task—What is to be done when the qualifier becomes an event. When the qualifier becomes true and therefore the event happens: do a specified task. A task is specified by you in the Trace Configuration window. There are plenty of examples of tasks. To “record this level in the trace” is a good example. A trigger is a signal passed to the trace hardware to tell it to stop recording the trace memory and other to precipitate other tasks.

The trigger is also available as a TTL output signal on a connector (J4) and can be used to trigger an oscilloscope or provide a signal to external hardware. A break is a signal to the emulator hardware to stop the emulation. A task can be a flag used to pass information about an event to another qualifier. An example is when one event has occurred and this fact is needed as input by another qualifier somewhere else. “Previous level must become true first ”is a good example.

> **Note**
>
> When most people mention a trigger, they are usually referring to the qualifier or the entire system.

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Definitions of the Level 1 – 6 Tabs

Refer to Figure 24. The names in parenthesis are from the older window and are for reference.

Cycle Type

- **Address 1-OFF and Address 2-OFF**—Each is an address or an address range that are ORd or ANDd together. Breakpoint occurs before execution for a break event and after execution for a trigger event. These are not the same breakpoints as set in the Source window. Double-click or right-click to enter or modify data. The OFF shown will turn to a ON when data is entered and the **Enabled** options in the Edit windows are selected.

- **Data 1-OFF and Data 2-OFF**—Each is an address or an address range that are ORd or ANDd together. Events occur after execution for a qualifier becoming true. Double-click or right-click to enter or modify data. The OFF shown will turn to a ON when data is entered and the **Enabled** options in the Edit windows are selected.

Task Options Window—These settings activate specific tasks of the trigger system. Most are registers in the ST bondout chip. The bondout mnemonic is indicated in parenthesis and is useful for comparing older documentation and macros. If an option is selected, then the associated statement is TRUE.

- **Turn Trace recording ON (Window (Set))**—This setting starts the trace recording when the trigger qualifier becomes true. This is the same as Window mode used in other Nohau emulators. Associated with the trace buffer control.

- **Turn Trace recording OFF (Window (Clear))**—This setting stops the trace recording when the trigger qualifier becomes true. Normally one level is used to turn the trace on and another to turn it off. One trigger is used to start the recording when it becomes true and a second trigger is used to stop the trace when it then becomes true.

  This is often used to record the cycles occurring not only inside a specified function, but also those of any functions called by this function. In contrast, the “Record this level in the trace buffer”(Filter mode) will record only those cycles executed within the function as configured. Combinations with external events such as the Trigger IN are legal. Associated with the trace buffer control.

- **Record this level in the trace buffer (Filter (Set))**—Cycles are recorded in the trace buffer only while the trigger is active. Combinations with external events such as the Trigger IN are legal.

  The trace is only recording while a qualifier is true. This mode is address dependent. A range of addresses is set and all cycles executed within this range will be recorded. If a function is specified to be recorded by using a start and end address: calls to functions outside of this address range will not be recorded. When control returns to the calling function within the specified address range, recording will resume. The recording will wrap around once the memory is filled. Associated with the trace buffer control.

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- **Preset Address AND Data (BC_MOD)**—Refer to Figure 25. Note that Address 1 and Address 2 can be ANDd or ORd with each other. Data 1 and Data 2 can also be ANDd or ORd with each other. These two outputs can then further be ANDd or ORd together, producing an output that is then fed into the Trigger AND/OR External In logic. These attributes are configured in the **Trigger Logic Combination** group shown in Figure 24.

  Preset Address AND Data provides for a special configuration not provided for in the aforementioned combinations which is shown in Figure 26. If Preset Address AND Data is set, it overrides the settings of the **Trigger Logic Combination** group. This represents the bondout mnemonics BCMB_IP, BCMB_DA and BC_ID.

  Refer to Figure 26. This is the configuration resulting when Preset Address AND Data is enabled. Note Address 1 is ANDd with Data 1. This was not possible with the configuration available in Figure 25. Address 2 and Data 2 are also ANDd together and subsequently ORd with Address 1 AND Data 1. The **Trigger Logic Combination** field will not be correct and will have no effect on the trigger configuration logic. Address 1 is swapped with Data 1. A partial Trace Configuration window with the correct information is shown in Figure 27. This issue will be fixed in a future version of Seehau. This is the only entry here that is not a task.

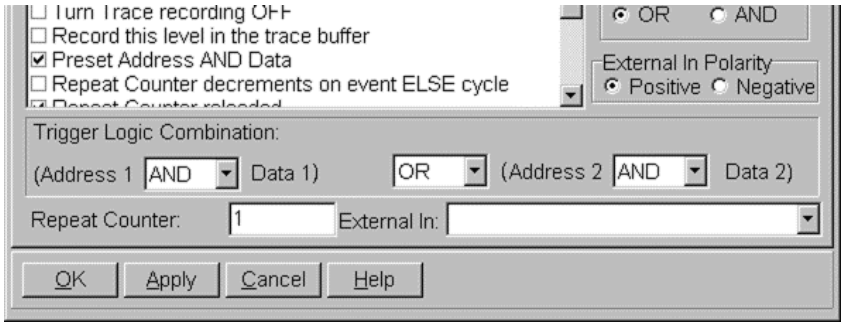


Figure 27. Configuration With Preset Address AND Data Selected

Repeat Counter—Each level has a 16-bit counter that essentially determines how often an event must happen before the trigger is generated. The value used in this counter is called the repeat count and is entered in the **Repeat Counter** field shown in Figure 24 and Figure 27. For example, If the repeat level count =4, then the trigger will be activated by the qualifiers becoming true four times. If the repeat counter =0, the trigger will not occur. The largest number that can be entered is FFFF. The following three entries are associated with the **Repeat Counter**.

Repeat Counter decrements on event ELSE cycle (BC_CIC (Event Mode/Cycle Mode))—This selects whether the repeat counter decrements in the Event or Cycle mode. Cycle mode is a counter decrement on each instruction cycle. Event mode is a decrement on each event. The event results from a signal which is the input to the counter from the block is labeled “Trigger AND/OR External In” in Figure 26 when a qualifier becomes true. If selected, it is in Event mode. Is associated with the **Repeat Counter**.

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Repeat Counter reloaded (BC_CAR (Reload))—This is a binary attribute input defining if the repeat counter should be reloaded with the repeat counter value once the counter has cycled and sent a trigger signal to the trigger state machine. If this option is selected, the counter will be reloaded once the counter limit is reached and the action can be repeated. If it is cleared, the counter is not reloaded. Essentially, the trigger will then occur only once in this case and can be called a one-shot mode. This options should be selected for general purpose trace and trigger operation. Associated with the **Repeat Counter**.

Repeat Counter reloaded while in Cycle Mode (BC_MCA (Atomic/Cumulative))—This binary attribute input determines if the counter is reloaded or not when qualifier becomes not true when the counter is in the Cycle mode. Cycle mode is a counter decrement on each instruction cycle and is set by "Repeat Counter decrements on event ELSE cycle" previously described. If **Repeat Counter reloaded while in Cycle Mode** is selected, it is in Atomic mode. If it is cleared, it is in Cumulative mode.

The input to the counter is the event signal which occurs each time a qualifier becomes true (an event). While this event is true (asserted), each instruction cycle will result in a decrement of the repeat counter. If the counter reaches zero, a trigger signal is sent to the trigger state machine.

If the counter does not reach zero by the time the event becomes not true, (not asserted), it will be either reloaded (Atomic mode) or not changed (Cumulative mode).

In Atomic mode, the counter must reach zero in the prescribed number of instruction cycles (the counter contents) in order for it to make an event. This is useful if you are looking for events that take longer than this prescribed number of cycles. If the event signal does not stay asserted for long enough, no matter how many times it occurs, an event will not be created.

In Cumulative mode, the counter is not reloaded when the event becomes not true. The next time the event does become true, the counter will continue to decrement form the existing counter value. When the required number of instruction cycles have occurred, even if they are not of any certain duration, an event will eventually be generated. If this option is selected, the counter is reloaded. Associated with the **Repeat Counter**.

Make this level always true (bypass mode) (FRC_MBE (Force MBE))—This attribute forces the Trigger AND/OR External In signal to be always true, effectively bypassing the selected level. This setting has the effect of making the qualifier true for a given level.

This would be most useful when using the **Break Emulation if all levels are true** setting. This setting ANDs the repeat counter output signals from all six levels in the trigger state machine. All six levels must therefore be true for assertion in the outputs of the AND/OR output array. This setting forces a specified level to be asserted, effectively forcing it true and removing it from the equation. This happens if this option is selected.

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Previous level must become true first (PL_CMB (Previous Level Dependence))—This is the only time a level has a priority over another level. This allows one level to affect the next level. In order to have a level affect any other level (for example, not the next level), select the appropriate action in **External In** shown in Figure 24. In order for a level to become true, the previous level must also be true. For example, if Level 5 has this attribute set, Level 4 must be true in order for Level 5 to become true. Level 1 can never be conditioned with this attribute since it is the first level. Select this option to enable this feature.

Trigger State Machine—This mechanism feeds signals from each level to the AND/OR array which determines how the repeat counter signals will be used. There is only one AND/OR array in the emulator and all levels share it. Each repeat counter output for any individual level is used for the Trace Control, USER OUT and the Trigger OUT connectors. The trigger signal (not the same signal as Trigger OUT) is used as a signal for the rest of the emulator hardware and is generally used to stop the trace recording. The following twelve attributes found in the task options area configure the trigger state machine. They are actually registers in this machine and there is a set for each of the six trigger state machines. See Figure 25 for the block diagram.

Trigger -stop trace and pulse Trigger Out (Trigger (Set))—This attribute sets the trigger to be active when the associated qualifiers become true. This trigger signal is used to activate the specified task and is provided on the trigger output connector (J4) on the ST10 trace board. This attribute is always in Track Trig mode therefore the output signal tracks the event. Select this option to activate this feature.

Turn User Output ON (USER (Set))—This attribute sets the user output connector (J6) on the ST10 trace board. This output will go high when a qualifier is asserted. This output will be latched high until turned off. Select this option to activate this feature.

Turn User Output OFF (USER (Clear))—This attribute clears the user output connector (J6) on the ST10 trace board. This output will go low when a qualifier is asserted. Select this option to activate this feature.

TIMEOUT—There are two 12-bit timeout counters 0 and 1 in the AND/OR array. This means they are shared by all levels. They are set in the Trace Setup window. (See Figure 23.) The timeout commands are always in the Set/Clear mode. These timers clear the repeat counters when they count up to 3FF and if enabled for a given level. The timeout counters are connected to the particular level through the **External In** dialog box(Figure 24). The timeout timers get their clocking input from the output at the Trigger AND/OR External In logic which becomes true when a qualifier becomes true. The timer load value and prescaler is entered in Figure 23.

Enable Timeout 0 (TIMEOUT 0 (Enable))—This attribute is used to enable the Timeout Counter 0. It is loaded with the value set in Figure 23. The counter increments each time an event happens. It clears the timer counter when it reaches 3FF if **Timeout x clears the Repeat Counter** is enabled.

Disable Timeout 0 TIMEOUT 0 (Clear))—This attribute is used to clear the timeout counter 0 when a specified event happens.

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Enable Timeout 1 TIMEOUT 1 (Enable))—This attribute is used to enable Timeout Counter 1. It is loaded with the value set in Figure 23. The counter increments each time an event happens. It clears the timer counter when it reaches 3FF if **Timeout x clears the Repeat Counter** is enabled.

Disable Timeout 1 TIMEOUT 1 (Clear))—This attribute is used to clear Timeout Counter 0 when a specified event happens.

Timeout 0 clears the Repeat Counter, Status Register (LC_CT0)—This enables Timeout 0 to clear the timer counter when it reaches 3FF. The status register is a register that indicates to Seehau events that have become true. This attribute clears this register.

Timeout 1 clears the Repeat Counter, Status Register (LC_CT1)—This enables Timeout 1 to clear the timer counter when it reaches 3FF. The status register is a register that indicates to Seehau events that have become true. This attribute clears this register.

Break emulation if this level is true (Break (Any Level True)(OR))—When the event happens (for example, when the qualifier becomes true) emulation will be halted and the trace board will be stopped. This attribute is ORd with the other level break emulation attributes.

Break emulation if all levels are true (Break (All Levels True)(AND))—When the event happens (for example, when the qualifier becomes true) emulation will be halted and the trace board will be stopped if all other levels are true. This attribute is ANDd with the other level break emulation attributes. All the six levels must be true for emulation and trace recording will be stopped. Recall a specified level can be turned off with the **Make this level always true (bypass mode)** attribute.

Entering Data into Level 1 – 6

Figure 28 shows the **Level 1** tab of the **Trace Configuration** dialog box. This is similar to Figure 24 but has a qualifier entered in **Data 1**. Each level has two addresses and two address/data qualifiers and they are shown here. The ON or OFF in the label field indicates if this particular qualifier is enabled or not. Figure 28 shows a Data qualifier enable for a write of 3400 to address 5017.

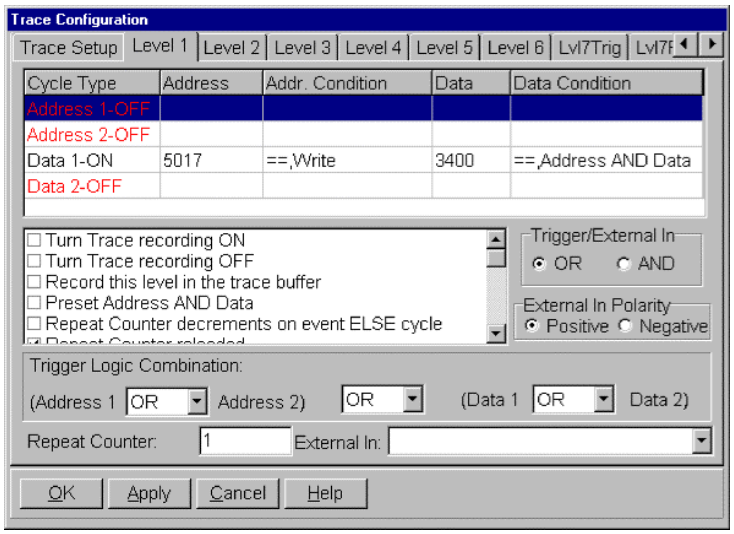


Figure 28. Level 1 Tab

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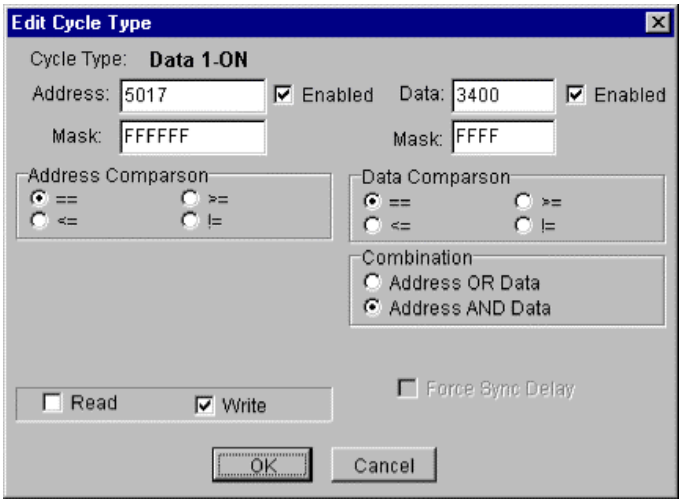


Figure 29. Edit Cycle Type Dialog Box

To enter or edit data either double-click on the required address or data line or right-click on the line. Right-clicking also enables you to remove the line. Figure 29 will open up. Figure 29 is for Data: Address has the Data field unavailable and has added a new option, **Force Sync Delay**. **Force Sync Delay** is used only for the address qualifiers. It is likely that the address event (for example, an address match) will occur at a slightly different time therefore the combined event will not occur. The first event is delayed to coincide with the second event. This effect is automatically enabled for the two data qualifiers.

If the two **Enable** options are cleared, the qualifier will be disabled, the word OFF will appear in Figure 28 and if the other three qualifiers are disabled, the green enable light will go off in Figure 23.

You can type the symbol name in place of the 5017 and show +7 can also be used. You can also copy the symbol name from the symbol browser found under the **View** menu item. Note the various combinations that can be entered in this window. Examples using these windows are given at the end of this chapter.

Level 7 Trigger Tab

The Level 7 mechanism was developed by Nohau to provide additional trigger abilities to the ST10 bondout. Level 7 operates on data read and write cycles and not on instruction fetches. This type of data access is easy to implement in the trigger mechanism and use because it does not use the instruction queue as an address access would. The number of address and data combinations that can be entered is virtually unlimited but is purposely limited to around 50 for practical reasons. Level 7 will only stop the trace recording and not break.

Level 7 Trigger is used to cause a break when the specified qualifiers become true. Level 7 Filter is used to allow only those R/W cycles specified to be recorded in the trace memory and is discussed later.

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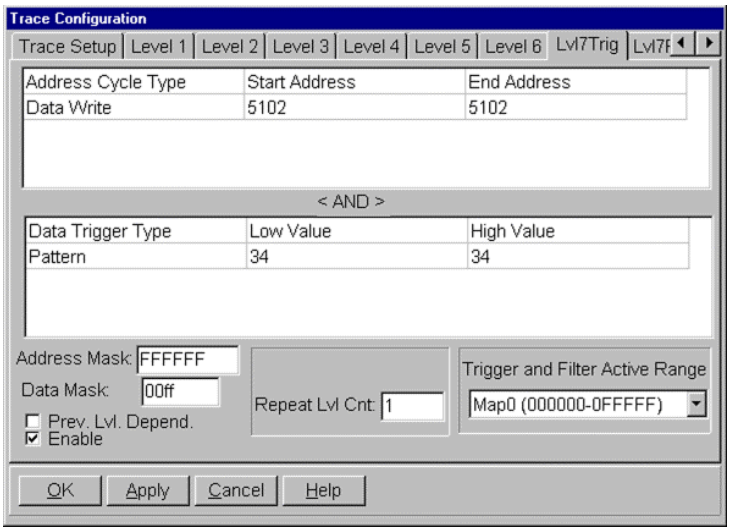


Figure 30. Level 7 Trigger Tab

Figure 30 shows the **Level 7 Trigger** tab in the **Trace Configuration** dialog box. To open this tab, from the **Config** menu, select **Trace**, and then click on **Lvl7Trig**.

Address Cycle Type—The read or write address qualifier is specified in this field. The address field can contain a single address (as shown) or a range of addresses. Addresses are entered, edited or removed by highlighting the appropriate line and doing a right-click on it or double-clicking on an existing line which opens the **Edit Trigger Qualifier** dialog box (Figure 31).

Note the addresses have already been entered. Note the various data accesses that are allowed.

Data Trigger Type—The data qualifier is specified in this field. Data is entered, edited or removed by highlighting the appropriate line and doing a right click on it. The dialog box in Figure 32 will open up. This field can contain a range or a pattern of data. Recent values are available in the drop-down list. Pattern specifies only one value to be placed in the **Begin** field. Range uses both fields to specify a value range. If this field is empty, then the data value will be *don't care* when the address specified in Figure 31 becomes true.



Figure 31. Edit Trigger Qualifier Dialog Box (Cycle Type)

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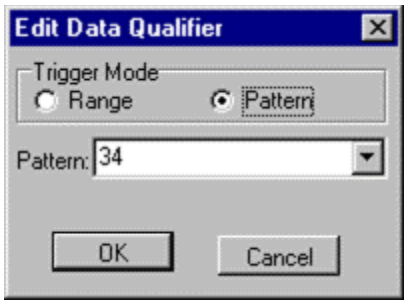


Figure 32. Edit Trigger Qualifier Dialog Box (Trigger Mode)

Address Mask—All address comparisons are done on the full 24-bit address. This field allows masking of the address on a bit-by-bit basis and is entered as a hexadecimal value. A bit set to zero will give that position a *don't care* value. A one will make that position relevant to the address comparison. This mask is global to all addresses listed.

Data Mask—This allows bit positions to be given a *don't care* status similar to the **Address Mask**.

Prev. Lvl. Depend—Previous level dependency allows Level 7 to be connected to Level 6. Level 7 will generate an event only if a Level 6 is also true.

Enable—Enables or disables the Level 7 Trigger. Ideal for temporary parking of the triggers without deleting them. Select this option to allow the filters to be active.

Repeat Lvl. Cnt—The repeat level count is a 16-bit counter that determines how often an event must happen before the trigger is generated. The value used in this counter is called the repeat level count. If the repeat level count =4, then the trigger will be activated by the qualifiers becoming true four times. This is not the same counter as the repeat counter in Levels 1 through 6 but it performs the same function.

Trigger and Filter Active Range—This field is provided to prevent aliasing or memory wrap-around issues from affecting the triggers. The triggers will be effective only if the qualifiers become true in the specified range.

Address and Cycle Type & Data Trigger Type Combinations

There can be 50 addresses and 50 data values. The addresses are all ORd together. The data values are all ORd together with themselves. These two groups are then ANDd together. This means that for setups with more than one entry in each type, a given address is not paired up with a given data value. If there is only one entry in each of the two windows, they are by default paired with each other. (Refer to the "Level 7 Trigger Example" section.)

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Level 7 Filter Tab

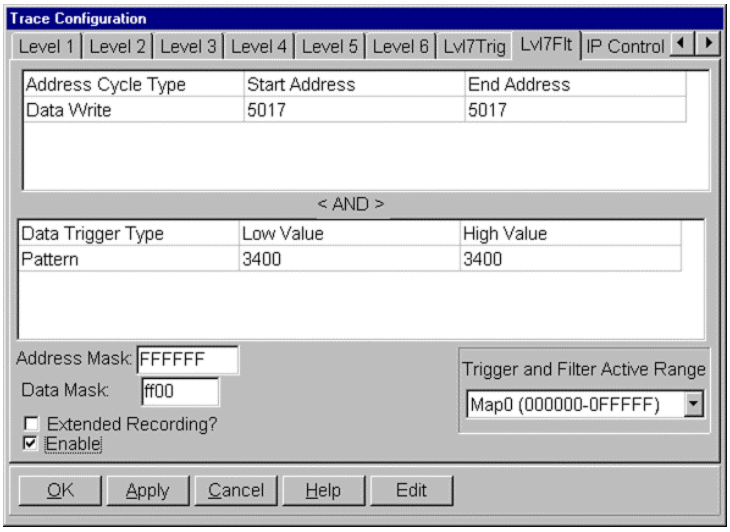


Figure 33. Level 7 Filter Tab

Level 7 Filter is used to allow only those R/W cycles specified to be recorded in the trace memory. The Level 7 Filter is very similar to the Level 7 Trigger in its configuration. (Refer to the "Level 7 Trigger Tab" section.) This filter is functionally equivalent to the **Record this level in the trace buffer** task.

Figure 33 shows the **Level 7 Filter** tab in the **Trace Configuration** dialog box. To open this tab, from the **Config** menu, select **Trace**, and then click on **Lvl7Flt**. Qualifiers are entered the same way as for the Level 7 Triggers. All submenus and fields are identical.

Extended Recording?—This field allows for the trace memory to continue recording for a specified number of cycles after the trigger has happened. This captures some cycles after the trigger event has occurred.

The filter settings shown in Figure 33 result in the trace display in Figure 34. Note the writes of 3400 to address 5017 by the MOVB instruction with an opcode of B92C located at address 442.

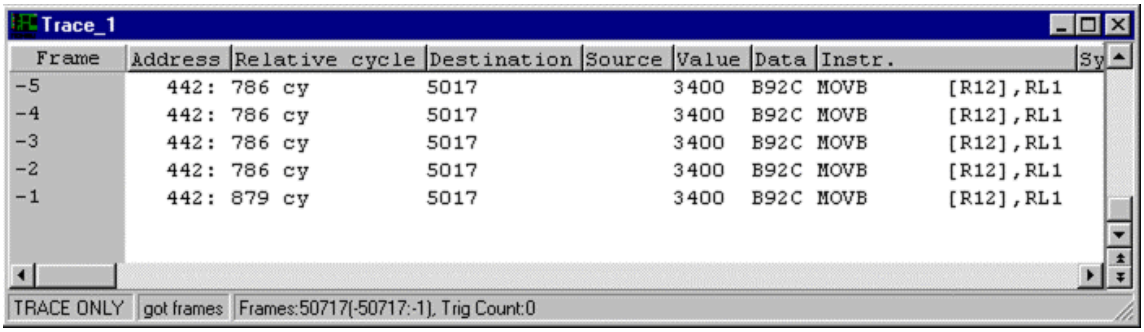


Figure 34. Trace_1 Window Displaying Extended Recording

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Instruction Pointer Control Tab (IP Control)

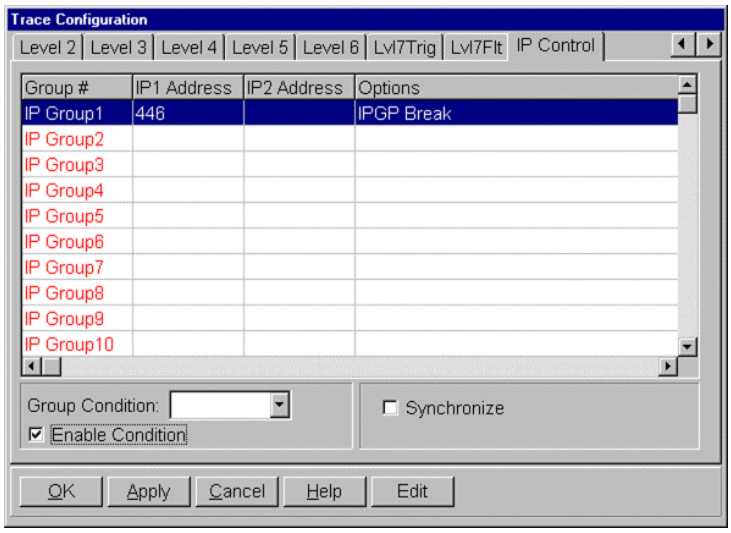


Figure 35. IP Control Tab

The last tab in the **Trace Configuration** dialog box is the **IP Control** tab. This is the bondout facility used for the hardware breakpoints used in the Source window. There are 16 groups and each group consists of two address qualifiers. These two address qualifiers can be used for two address comparisons or one range comparison with the CPU instruction pointer. Data values are not used as qualifiers. Groups are only available in the Advanced Trace mode.

Figure 35 shows the **IP Control** tab in the **Trace Configuration** dialog box. To open this tab, from the **Config** menu, select **Trace**, and then click on **IP Control**. An example address is entered in Group 1.

Group #—These 16 fields contain addresses used as qualifiers. Each group is ORd together.

Group Condition—This qualifies the 16 Groups to Levels 1 through 6 events. This is global to all 16 group members. The specified level must be true for any group member to become true.

Enable Condition—This enables or disables the **Group Condition**.

Synchronize—This enables or disables the synchronization of address events with data qualifiers from another level if so selected. This ensures that the address creating a data action will correctly be ANDd with that data qualifier. This is in spite of each qualifier potentially occurring at slightly different times.

Editing a Group Member

Click on one of the group types to highlight its line. Double-click on this line and the **Edit Group** dialog box opens (Figure 36). This dialog box is where the address qualifiers are entered. You can also right-click on it to get the remove and edit functions. A simple example is provided at the end of this chapter.

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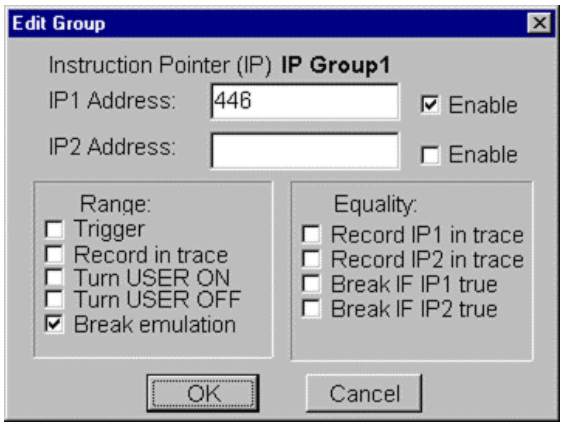


Figure 36. Edit Group Dialog Box

IPG0 Address and IPG1 Address—IPG0 and IPG1 are the two address qualifiers. Enable these by selecting the **Enable** options.

Range—The Range mode compares IPG0 and IPG1 with the current CPU instruction pointer following this equation:
IPG0 =<current IP <IPG1

If a match occurs, the following actions can be selected:

- **Trigger**: This is a signal that causes the trace recording to stop.
- **Record in trace**: This signal is used to turn the trace recording on while the qualifier is true.
- **Turn User ON**: This signal is sent to the USER Output connector J6 on the trace board. USER is set high by this selection. See Figure 2.
- **Turn User OFF**: This signal clears the USER Output connector J6.
- **Break emulation**: This selection causes the emulation to stop.

Equality—IPGP0 and IPGP1 can be configured as the Range or Equality mode. Equality is comparing IPGP0 and IPGP1 with the instruction pointer and creating an event if a match is made. An event will create an action. These actions are listed in the **Equality** group (Figure 36).

- **Record IP1 in trace**: When IPGP0 becomes true, the cycles responsible are recorded in the trace memory.
- **Record IP2 in trace**: When IPGP1 becomes true, the cycles responsible are recorded in the trace memory.
- **Break if IP1 true**: When IPGP0 becomes true, the emulation will be stopped.
- **Break if IP2 true**: When IPGP1 becomes true, the emulation will be stopped.

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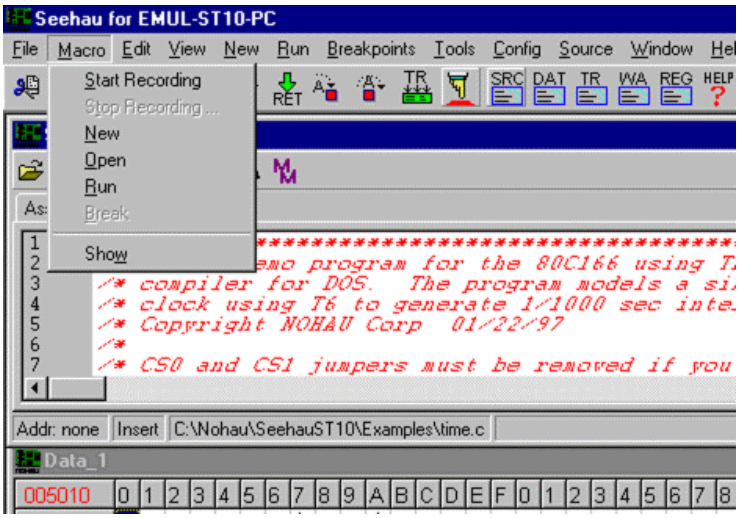


Figure 37. Macro Menu

Saving the Trace Configuration

The entries you have made can be saved to a macro. This macro can be started manually under the **Macro**, **Run** menu item or a button can be created on the toolbar. There are two methods of creating macros:

- Manually by creating the text file filename. bas

  This method is not recommended as a detailed knowledge of the macro commands will be needed. It is easier to make this *. bas file with the macro recorder found in the **Macro/Start Recording** menu. Manually editing an existing file is easy and recommended with the built-in macro editor under the **Macro**, **Show** menu item or with any ASCII text editor.

- Using the built-in Macro Recorder

  In the **Macro** menu item, there are two items used to start and stop the macro recording. All your keystrokes will be saved to a Filename. bas file of your choosing. Such a file is run either with a button you create or manually with the **Macro**, **Run** menu item (Figure 37).

  A macro can also be created from a configuration window that has an **Apply** button. The present settings of the configuration menu will be saved at one time. This is useful for saving a series of settings that have been subsequently modified and the exact key sequence is not available.

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Saving Configuration Macros

The **Trace Configuration** dialog box must be open and the **Apply** button visible. (See Figure 33.)

1. From the **Macro** menu, select **Start Recording**. The **Trace Configuration** dialog box will close.

2. Reopen the **Trace Configuration** dialog box from the appropriate menu item. Click **Apply**. The settings associated with this window will be saved.

3. From the **Macro** menu, select **Stop Recording**.

4. The **Save Macro** dialog box will open giving you the opportunity to choose the filename for the newly created macro. Enter a filename of your choosing and click **Save**. The macro is ready to use and will accurately recreate your configuration settings. You can also easily make a button to activate your macro. This feature is found under **Config**, **Buttons**.

Trace Memory Examples

The timer example as described in Chapter 3, “Running the Example Program Timer.abs” and repeated in Figure 38 showed the Shadow RAM providing memory contents in real-time. Recall there is no cycle stealing from the emulation controller. While the Time. c program has been running, the trace memory has been operating in the background, also in real-time.

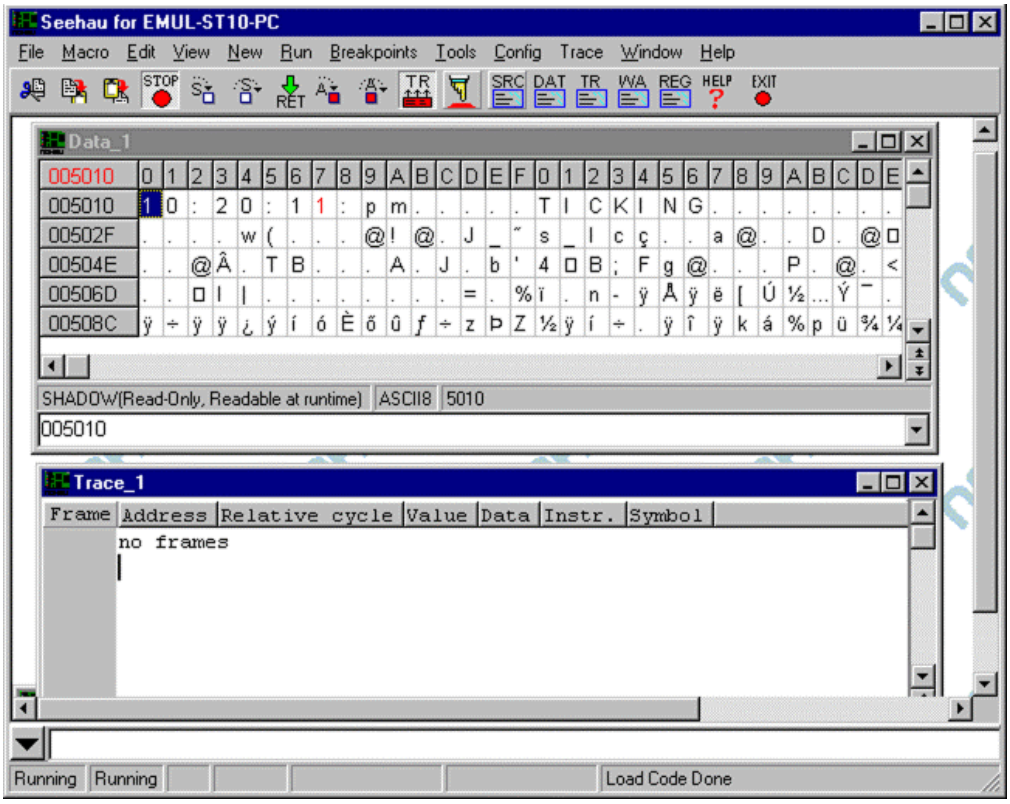


Figure 38. Trace Memory Examples in the Data and Trace Windows

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Many emulators are unable to view the trace without stealing cycles or even stopping the emulation. The Nohau emulator can do this in real-time. It uses a dedicated microcontroller to do all the trace, trigger and Shadow RAM housekeeping chores, rather than stealing cycles from the bondout controller.

1. Ensure the emulator is running the Time. c program. The file you want to load is Time. abs. The two boxes in the bottom left hand corner of the main window will contain “Running ”instead of “Stopped ”as shown in Figure 38. The GO and TRACE icons are both red in color. You should have the Data window open and displaying the time changing in real-time as shown in Figure 38.

2. Open a Trace window if necessary. You can click on the New Trace icon or from the **New** menu select **Trace**.

3. Position the windows similar to Figure 34. You should have the Trace and Data windows visible. The Trace window might have some data recorded in it or empty. This depends on previous emulation runs.

   Note the Trace window is empty as the trace buffer is being filled. It is not possible to view the trace contents at this time. The bar at the bottom of the Trace window will show that the trace memory is already full and how many triggers have occurred. There are no trigger events (see Figure 35).

4. Click on the Stop Trace icon. Note that while the changing time values might appear to stumble, this is only in the display. The emulation controller was not slowed down at all. This is genuine real-time operation.

   The Trace window now contains recorded controller cycles and trace memory (Figure 39). You can add additional columns by right-clicking in the Trace window and selecting them.

   Note that in Figure 39 labels, registers, source code and addressing modes are all displayed. Note the Trace window will have the ability to display C source code with the resulting assembly code.

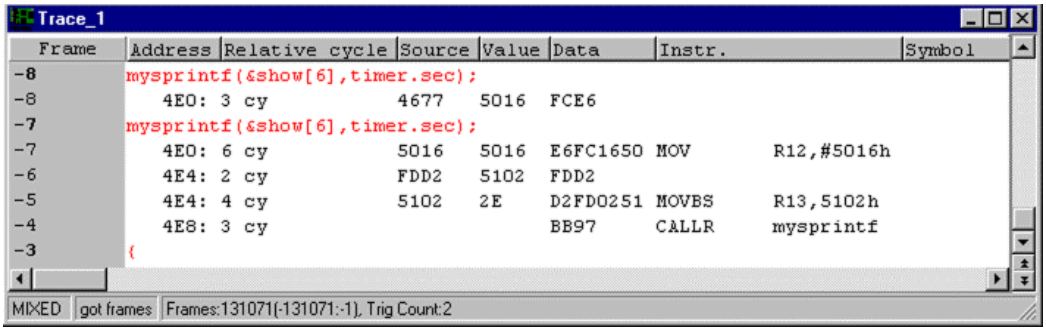


Figure 39. Trace Window Displaying Recorded Controller Cycles

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5. Start the trace memory by clicking on the Start Trace icon. Note the time does not stop or slow down. Once again, the trace memory is being continuously overwritten with new values. The trace memory is a circular buffer. This will continue until the recording is stopped either manually or with a trigger event. Note the triggers have the ability to start and stop the trace recording.

The Trace window can display many types of information about the bus cycles. Right-click on the Trace window or open up the menu in **Config**, **Trace** (see Figure 40). These are the options used to create Figure 39. Click on some of the options to see the various fields available. The source code can be enabled under Display mode.

The ST10 emulator has extensive trigger facilities to start and stop the trace as well as perform program breaks. The triggers can control cycle recording so that only specified cycles are recorded. The apparent size of the trace memory can be magnified many times by using carefully selected trigger qualifiers. The triggers can also send out external signals.

External events present on J7 can be recorded in the trace (8 bits).

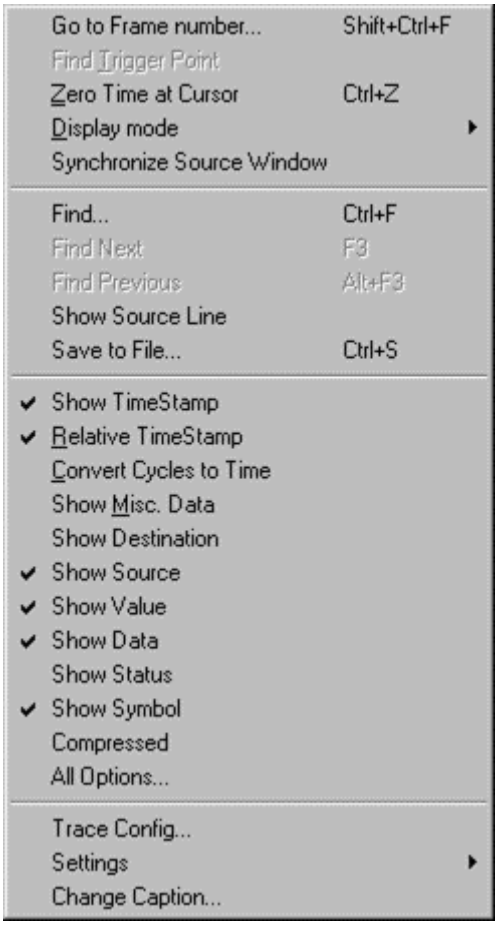


Figure 40. Trace Submenu

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Level 1 – 6 Trigger Example

All Nohau emulators contain sophisticated and versatile triggers. The EMUL–ST10 offers trigger capabilities. You can configure the triggers in real-time. The triggers test for qualified events, perform tasks and start and stop the trace all without stealing cycles from the emulation controller. The application program always run full speed. A break in emulation, by definition, affects real-time operation. This example will show how to setup a simple yet effective trigger. The emulation will stop when the seconds MSB memory location is written the value of 4 ASCII (34 hex). The bus cycle responsible for this write will be recorded in the trace memory.

1. Configure Seehau to display a main window similar to Figure 38. Stop emulation and press the Reset icon.

2. Open the **Trace Configuration** dialog box under **Config**, **Trace** or right-click in the **Trace** window and select the **Trace Config** item. The **Trace Setup** tab opens (Figure 41). Note the button labeled **Advanced**. There are two versions of the Trace window for the ST10 emulator: Standard and Advanced. Click on this button to see some of the Advance features. We will use the Standard mode here, so click again so the button reads **Advanced** and the Standard mode is therefore selected.

   Note there are seven levels of triggers plus a Group (Advanced only). We will use only Level 1 in this example. The red dot will change to green once we have entered and enabled the qualifier for Level 1.

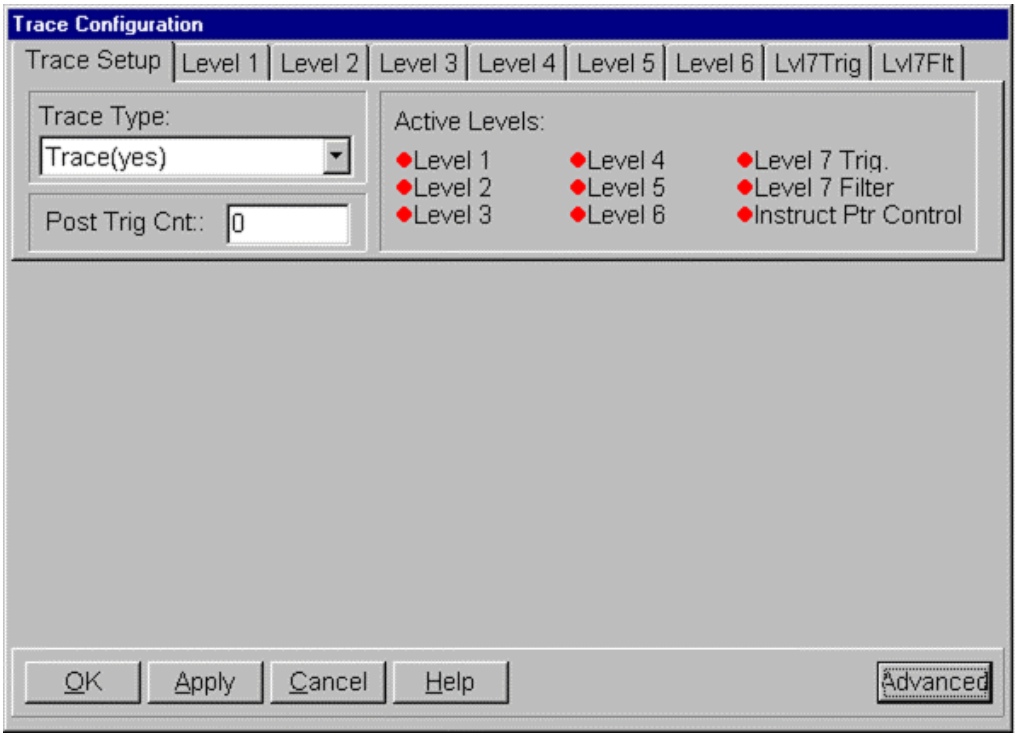


Figure 41. Trace Setup Tab

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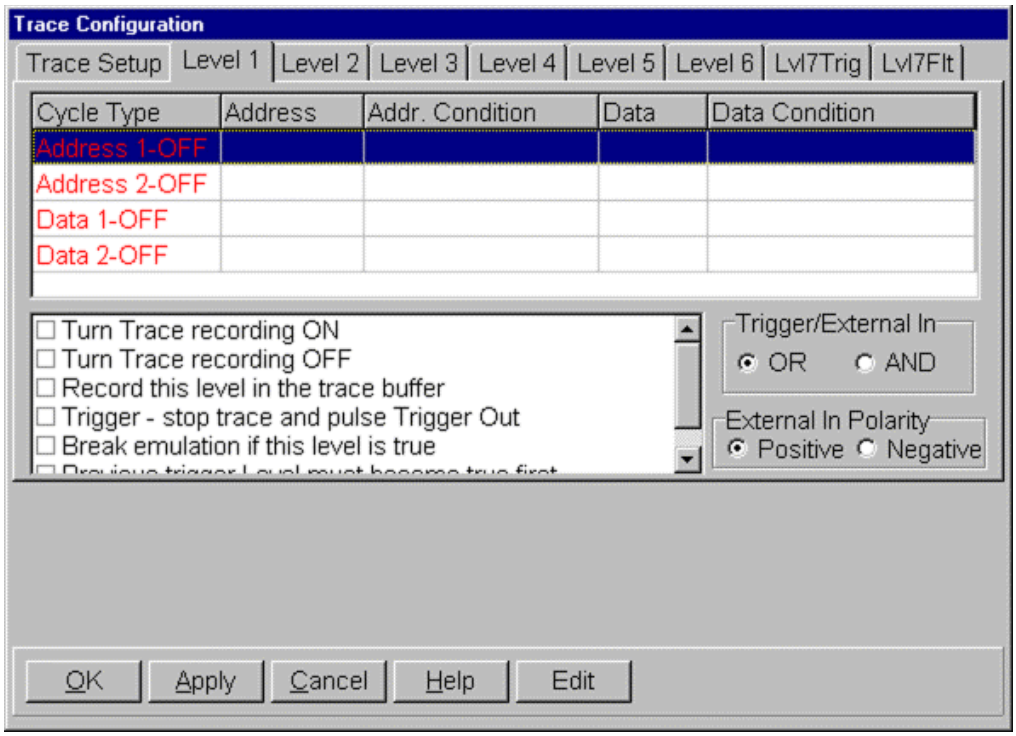


Figure 42. Level 1 Tab

3. Click on the **Level 1** tab (Figure 42). Address 1 and Address 2 are address only qualifiers. Data 1 and Data 2 are address and data qualifiers. We will use Data 1 and Data 2 in this example. All qualifiers are disabled at this point.

4. Click on the Data 1 line and right-click (or double-click) on the highlighted line. An empty **Edit Cycle Type** dialog box opens (Figure 43). Enter the fields as shown and ensure the **Enabled** options are seletced. Address and data are not case sensitive. You need to fill in the **Address**, **Data**, **Data Mask** and the **Write** fields. Click **OK**. Data 2 will automatically be filled in with the same data as Data 1.

5. In Figure 44, note that both Data 1 and Data 2 are enabled with the appropriate data and are turned ON. The qualifier is now properly set. Data 1 has a window similar to Figure 39. Click on the Data 2 line and right-click as before to open this tab. Confirm it has the same settings as Figure 43.

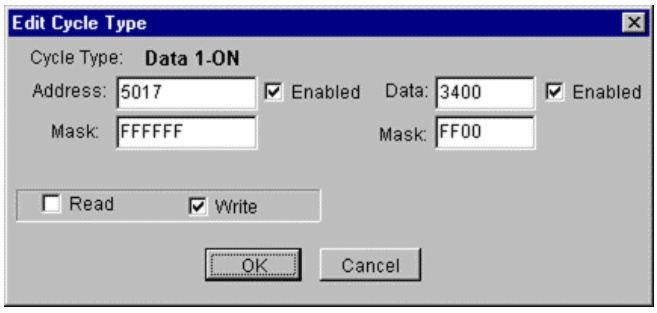


Figure 43. Edit Cycle Type Dialog Box

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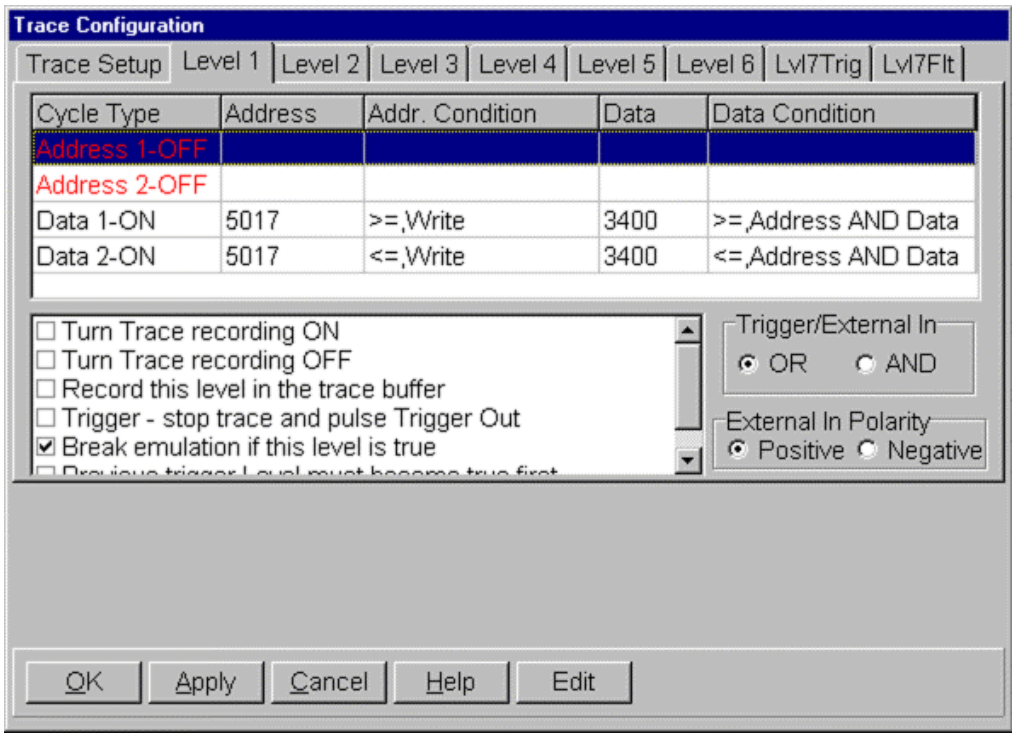


Figure 44. Example Trigger in the Level 1 Tab

6. Select the **Break emulation if this level is true** option. This will break the emulation and record only that cycle which caused a write of 34 to memory location 5017. Click **OK** to close the **Trace Configuration** dialog box.

7. You must enter the value of 34 as 3400 because 5017 is an odd address, we are trying to trigger on a byte write (MOVB) and the ST10 is a 16-bit machine. The mask value of FF00 ensures only the 34 becomes the data of the qualifier. If you were using an address of 5016, the values used would be 0034 and 00FF. The leading zero of the 0034 can be discarded leaving 34. For 16-bit data qualifiers, these rules do not apply.

8. You should have a window that looks similar to Figure 38. Click on GO and the emulation will run. When the value at address 5017 becomes ASCII 4 (hex 34), the emulation will break and the instruction cycles will be displayed as in the Trace window in Figure 45. The compressed feature is turned on.

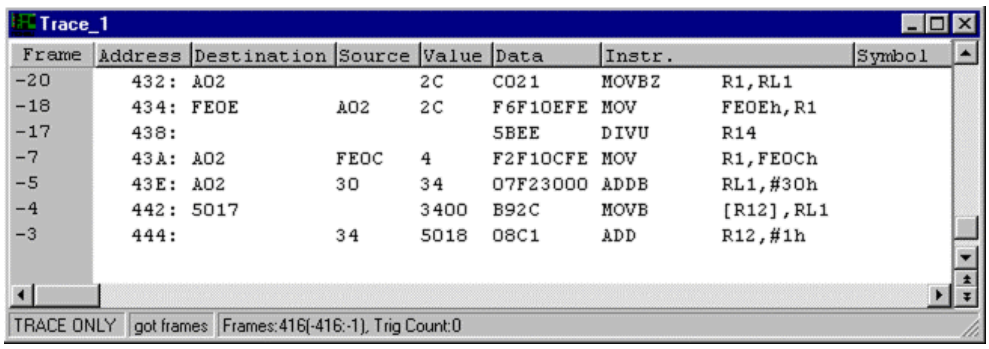


Figure 45. Trace Window Displaying Instruction Cycles

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Frame #-4 contains the write of 3400 to address 5017 with the MOVB instruction at address 442 !Frame #-3 is the last instruction executed. R12 at this time contains 5018 and before this add #1, it contained 5017. The present value of R12 can be seen in the register window. R1 contains 0034 at this time.

9. Select the **Record this level in the trace buffer** option shown in Figure 44 and run the program again. Only the instruction that caused the trigger will show in the trace. You can focus on only the data you want.

10. In the **Level 1** tab, clear **Break emulation if this level is true** so the emulation will not be stopped.

11. Click on the Reset and GO icons to restart emulation. Note you could also make this change on-the-fly without losing real-time performance.

12. Note the number of cycles recorded in the trace memory increasing as the value in 5017 equals 34. This information is shown at the bottom of the Trace window. Stop the trace by clicking on the Trace icon and the cycles will be displayed as in Figure 25. Each cycle has a timestamp indication when it occurred.

13. Open the submenu and enable some more fields. Remember that not all cycles have been recorded, only those selected in the trigger qualifiers. This is only a small part of the trigger facilities of the ST10 emulator. This example does not begin to show the true capabilities of the emulator.

> **Note**
>
> You can select the Advanced mode and begin to configure some extremely powerful triggers.
>
> A trigger will turn the trace off at Frame #0. The actual displayed value of the trigger point will vary a small amount due to the CPU pipeline effect.

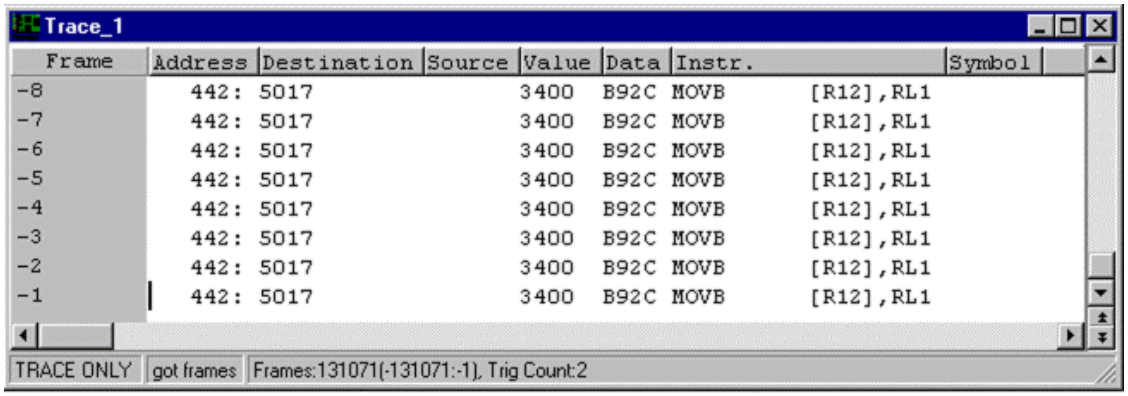


Figure 46. Trace Window Displaying Cycles

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Level 7 Trigger Example

1. Load the Timer. abs example program.

2. Set the Level 7 Trigger as in Figures 47, 48, and 49. Figure 47 and Figure 48 are accessible by right-clicking on the address and data areas of Figure 49. Set the **Data Mask** in Figure 49 to FF00. This will ensure the trigger looks only at the low byte. Make sure only the Level 7 Trigger is active.

3. Open a Data window and set it to display 8-bit ASCII and from the address space TR Shadow. View address show or 5017. Open a Trace window.

4. Start the emulation by clicking on the GO icon.

5. When address 5017 contains hex 34 (ASCII 4), the trace recording will stop. The Trace icon turns green.

6. The trigger point is located at Frame 0 in the Trace window. Scroll to this position if necessary. From the submenu selected by right-clicking on the Trace window, select the **Value** field. Your Trace window will look similar to Figure 45. Note that value 34 was stored at 5017 by the MOVB instruction at Frame 0.

The trace memory is filled with the previous 128K cycles that preceded the trigger at Frame 0.

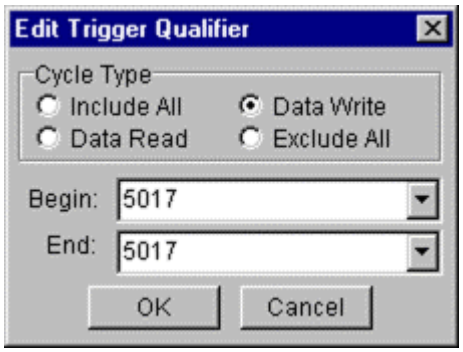


Figure 47. Edit Trigger Qualifier (Cycle Type) for the Level 7 Trigger Example

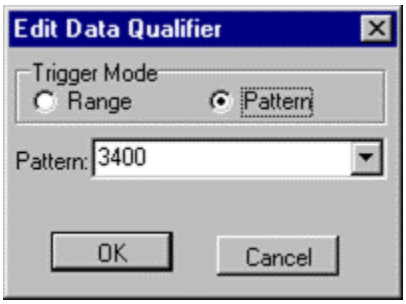


Figure 48. Edit Trigger Qualifier (Trigger Mode) for the Level 7 Trigger Example

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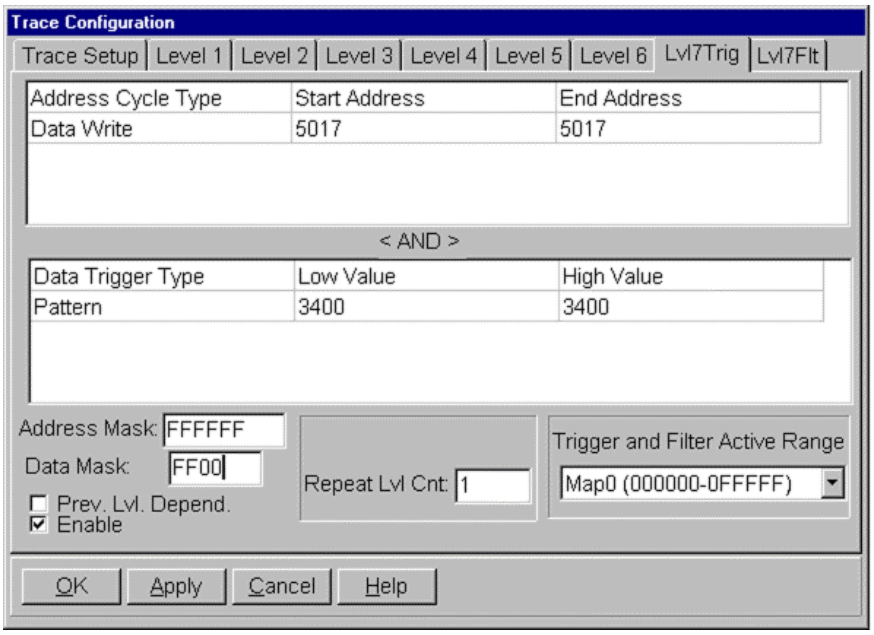


Figure 49. Level 7 Trigger Tab for the Level 7 Trigger Example

Level 7 Filter Example

1. Load the Timer. abs example program.

2. Set the Level 7 Filter as in Figure 50. Right-click to open up the submenus to enter the data. Make sure only Level 7 Filter is active so other triggers do not become events and confuse the situation.

3. Open a Data window and set it to display ASCII and from the address space Shadow or TR Shadow. Shadow is the Nohau Shadow memory and TR Shadow is the ST10 bondout Shadow memory. View address 5017 or type in show. Open a Trace window. Arrange these windows for your convenience.

4. Start the emulation by clicking on the GO icon.

5. When address 5017 is written with a 34, this cycle will be recorded. The trace will not stop recording. Note that every 1 second or so the **Frames Recorded** field increases. The time is shown with the **Relative Timestamp** field selected in the Trace submenu.

6. Stop the trace recording by clicking on the Trace icon. The Trace window in Figure 51 will display a series of MOVB instructions. From the submenu selected by right-clicking on the Trace window, select various fields to yield a display similar to Figure 51. You can also filter in Levels 1-6 by using the **Record this level** in the trace buffer attribute.

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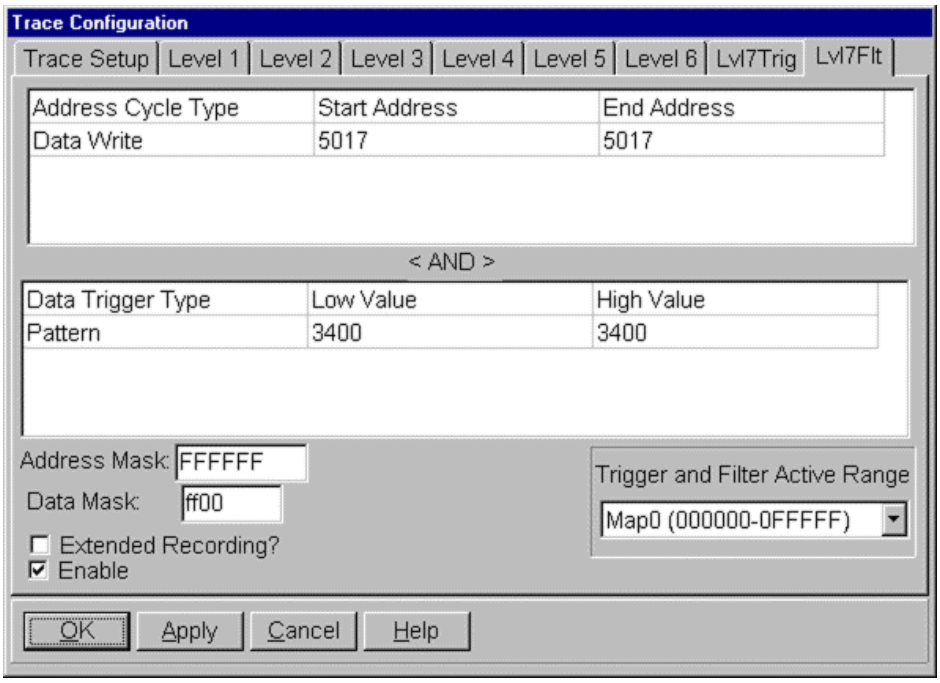


Figure 50. Level 7 Filter Tab for the Level 7 Filter Example

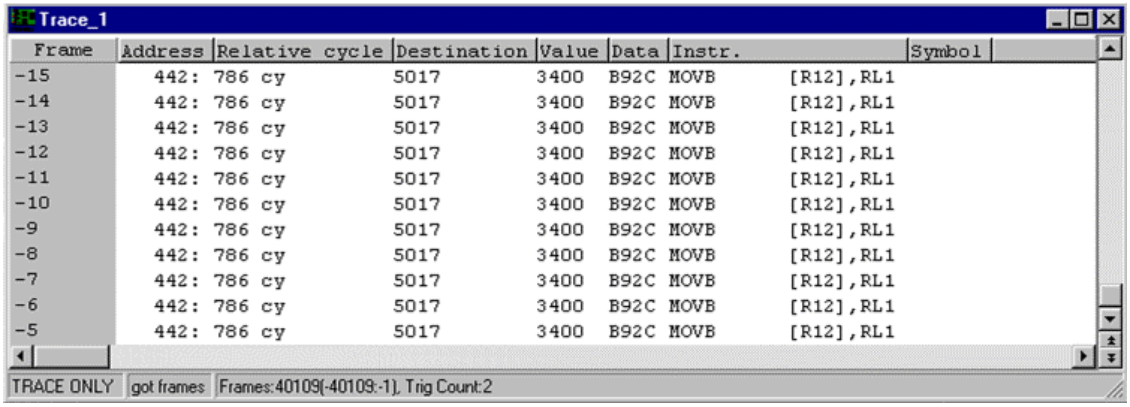


Figure 51. Trace Window for the Level 7 Filter Example

The trace memory is filled with only writes of 34 to memory location 5017. Note each instruction occurs 786 machine cycles from each other. You can also convert this to time in the submenu. Experiment with different settings of the submenu.

If you do not put appropriate data qualifiers in the **Data Trigger Type** fields, all writes to 5017 will get recorded in the trace buffer.

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Group Breakpoints Examples

1. Set up Seehau and load the example program Timer. abs.

2. Open a Source, Data and Trace window and position them in the main Seehau window to your preferences.

3. Configure the **IP Group 1** as shown in Figure 52. Make sure the two **Enable** options are selected. Figure 53 will be the configuration result. Click **OK** to enter the qualifiers into the emulator.

4. Click on the GO icon to start the program.

5. The emulation will stop when a fetch of 442 occurs. This will be the last or second last instruction from the end in the trace window.

6. Experiment with different settings in the **Edit Group** dialog box shown in Figure 52.

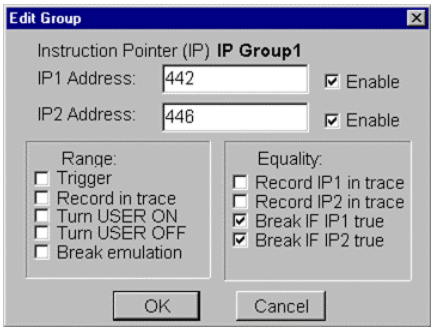


Figure 52. Edit Group Dialog Box for the Group Breakpoints Example

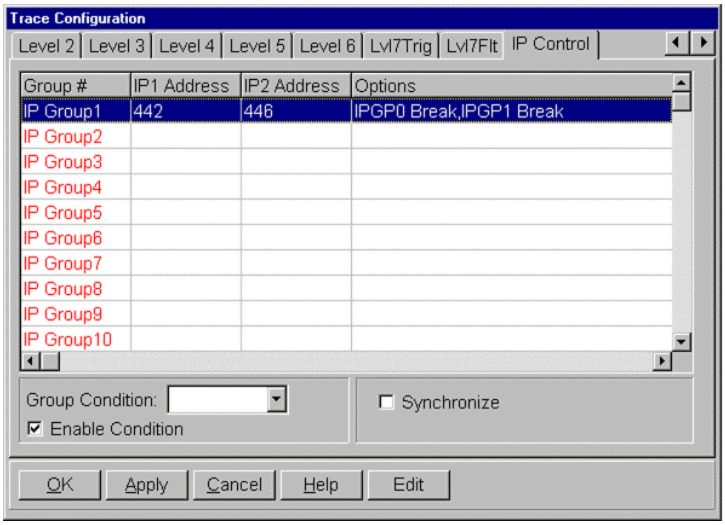


Figure 53. IP Control Tab for the Group Breakpoints Example

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Trace Configuration Modification Conversion Table

In November 1999, the Trace Configuration tabs were modified to provide more intuitive English wording. The ST10 bondout mnemonics were previously used and caused some user difficulty. This list details the changes that were made. The macro commands are unchanged therefore use the old mnemonics. The old *ST10 Quick Start* can be obtained from the Nohau web site for historical reference. www.icetech.com

Old	New
Window (Set)	Turn Trace recording ON
Window (Clear)	Turn Trace Recording OFF
Filter (Set)	Record this level in the trace buffer
Trigger (Set)	Trigger -stop trace and pulse Trigger Out
Break (Any level true)	Break emulation if this level is true
Break (All levels true)	Break emulation if all levels are true
BC_CAR	Repeat Counter reloaded
BC_CIC	Repeat Counter decrements on event ELSE cycle
BC_MCA	Repeat Counter reloaded while in Cycle Mode
FRC_MBE	Make this Level always true (bypass mode)
PL_CMB	Previous Level must become true first
USER (Set)	Turn User Output ON
USER (Clear)	Turn User Output OFF
TIMEOUT 0 (Enable)	Enable Timeout 0
TIMEOUT 0 (Disable)	Disable Timeout 0
TIMEOUT 1 (Enable)	Enable Timeout 1
TIMEOUT 1 (Disable)	Disable Timeout 1
LC_CT0	Timeout 0 clears the Repeat Counter, Status Register
LC_CT1	Timeout 1 clears the Repeat Counter, Status Register
BC_MOD	Preset Address AND Data

Notes

- No features are added or removed.
- There is a direct one-to-one correlation between the old and new versions.
- Customer macros will not need modification.

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Changes to the EXTC Window

Old	New
No external source	No changes
Level 1 (memorized)	Level 1 has occurred (latched)
through	
Level 6 (memorized)	Level 6 has occurred (latched)
ILV1(current)<ILV1(prog)	CPU Int. level <Trigger Int. Level
MAC flag C carry generated	No changes
through	
MAC flag SL: Limit flag	No changes
MAC flag or combination	All 4 MAC flags ORd together
Timer-out 0	Timeout 0 =3FF
Timer-out 1	Timeout 1 =3FF
External Trigger IN 0	External Trigger IN (J3)

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Changes to the Edit Cycle Type Dialog Box Levels 1 – 6

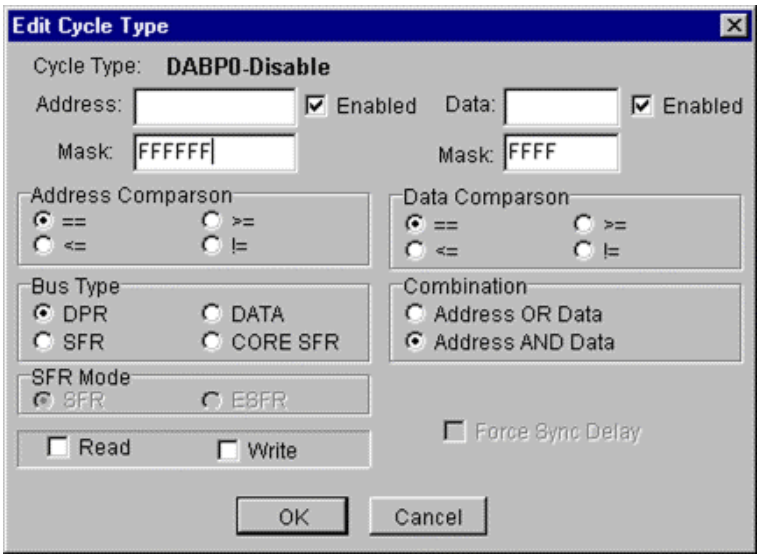


Figure 54. Old Edit Cycle Type Dialog Box

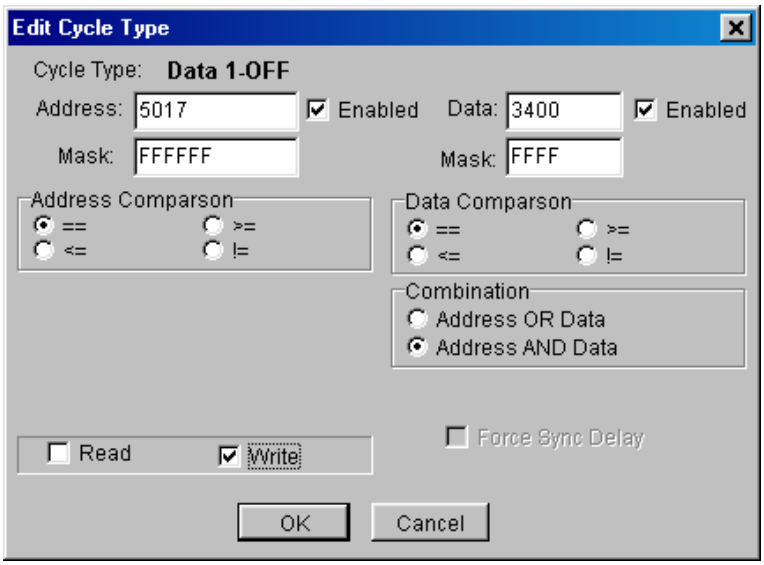


Figure 55. New Edit Cycle Type Dialog Box

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