

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*

Data Sheet
February 1997

microelectronics group

Lucent Technologies
Bell Labs Innovations

ATT3000 Series Field-Programmable Gate Arrays

Features

- High performance:
  - — Up to 270 MHz toggle rates
  - — 4-input LUT delays <2.7 ns
- User-programmable gate arrays
  - — Unlimited reprogrammability
  - — Easy design iteration through in-system logic changes
- Flexible array architecture:
  - — Compatible arrays ranging from 1500 to 6000 gate logic complexity
  - — Extensive register, combinatorial, and I/O capabilities
  - — Low-skew clock nets
  - — High fan-out signal distribution
  - — Internal 3-state bus capabilities
  - — TTL or CMOS input thresholds
  - — On-chip oscillator amplifier
- Standard product availability:
  - — Low-power 0.55 µm CMOS, static memory technology
  - — Pin-for-pin compatible with *Xilinx* XC3000** and *XC3100** families
  - — Cost-effective for volume production
  - — 100% factory pretested
  - — Selectable configuration modes
- *ORCA*™ Foundry for ATT3000 Development System support
- All FPGAs processed on a QML-certified line
- Extensive packaging options

Description

The CMOS ATT3000 Series Field-Programmable Gate Array (FPGA) family provides a group of high-density, digital integrated circuits. Their regular, extendable, flexible, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O blocks, a core array of logic blocks, and resources for interconnection. The general structure of an FPGA is shown in Figure 1.

The *ORCA* Foundry for ATT3000 Development System provides automatic place and route of netlists. Logic and timing simulation are available as design verification alternatives. The design editor is used for interactive design optimization and to compile the data pattern that represents the configuration program.

The FPGA's user-logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The program data resides externally in an EEPROM, EPROM, or ROM on the application circuit board, or on a floppy disk or hard disk. On-chip initialization logic provides for optional automatic loading of program data at powerup. A serial configuration PROM can provide a very simple serial configuration program storage.

* *Xilinx*, *XC3000,* and *XC3100* are registered trademarks of Xilinx, Inc.

Table 1. ATT3000 Series FPGAs

FPGA	Max Logic Gates	Typical Gate Range	Configurable Logic Blocks	Array	User I/Os Max	Flip-Flops	Horizontal Long Lines	Configuration Data Bits
ATT3020	1,500	1,000—1,500	64	8 x 8	64	256	16	14,779
ATT3030	2,000	1,500—2,000	100	10 x 10	80	360	20	22,176
ATT3042	3,000	2,000—3,000	144	12 x 12	96	480	24	30,784
ATT3064	4,500	3,500—4,500	224	16 x 14	120	688	32	46,064
ATT3090	6,000	5,000—6,000	320	20 x 16	144	928	40	64,160

Table of Contents

Contents	Page
Features	1
Description	1
Architecture	3
Configuration Memory	4
I/O Block	5
Summary of I/O Options	6
Configurable Logic Block	7
Programmable Interconnect	9
General-Purpose Interconnect	10
Direct Interconnect	11
Long Lines	13
Internal Buses	14
Crystal Oscillator	16
Configuration	17
Initialization Phase	17
Configuration Data	19
Configuration Modes	22
Master Mode	22
Peripheral Mode	24
Slave Mode	25
Daisy Chain	26
Special Configuration Functions	27
Input Thresholds	27
Readback	27
Reprogram	28
DONE Pull-Up	28
DONE Timing	28
RESET Timing	28
Crystal Oscillator Division	28

Contents	Page
Performance	29
Device Performance	29
Logic Block Performance	30
Interconnect Performance	30
Power	32
Power Distribution	32
Power Dissipation	33
Pin Information	34
Pin Assignments	39
Package Thermal Characteristics	50
Package Coplanarity	51
Package Parasitics	51
Absolute Maximum Ratings	53
Electrical Characteristics	54
Outline Diagrams	68
Terms and Definitions	68
44-Pin PLCC	68
68-Pin PLCC	69
84-Pin PLCC	70
100-Pin QFP	71
100-Pin TQFP	72
132-Pin PPGA	73
144-Pin TQFP	74
160-Pin QFP	75
175-Pin PPGA	76
208-Pin SQFP	77
Ordering Information	78

Architecture

The perimeter of configurable I/O blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of configurable logic blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed-circuit board traces connecting MSI/SSI packages.

The blocks' logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors. These functions of the FPGA are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the FPGA at powerup and may be reloaded on command. The FPGA includes logic and control signals to implement automatic or passive configuration. Program data may be either bit serial or byte parallel. The *ORCA* Foundry for ATT3000 Development System generates the configuration program bit stream used to configure the FPGA. The memory loading process is independent of the user logic functions.

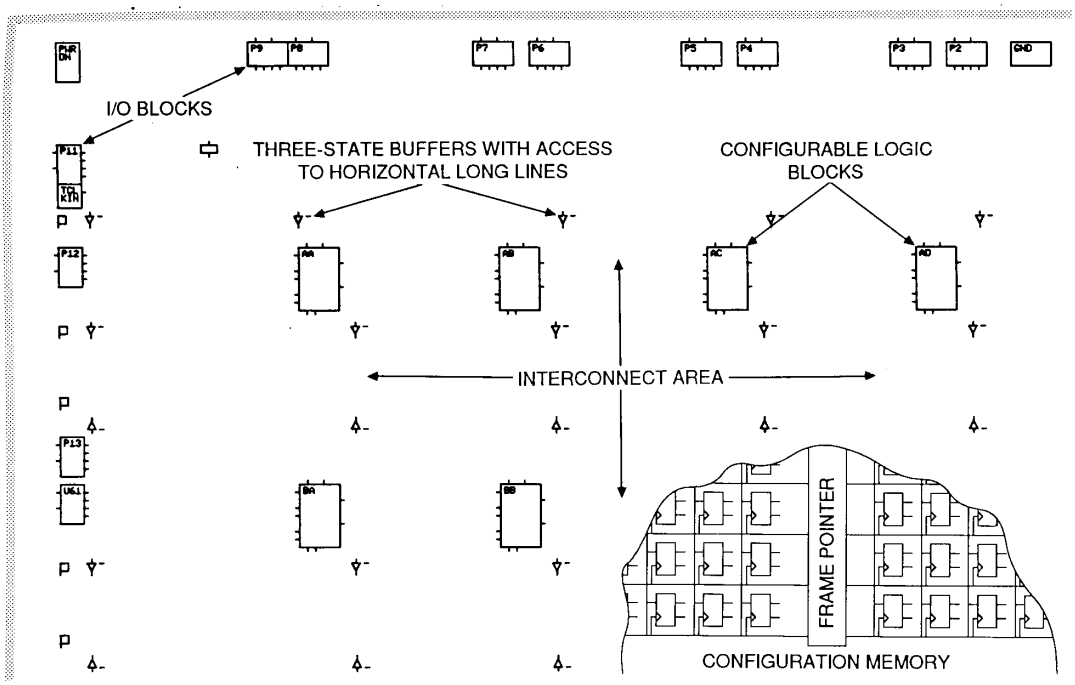


Figure 1. Field-Programmable Gate Array Structure

Configuration Memory

The static memory cell used for the configuration memory in the FPGA has been designed specifically for high reliability and noise immunity. Integrity of the FPGA configuration memory based on this design is ensured even under various adverse conditions. Compared with other programming alternatives, static memory is believed to provide the best combination of high density, high performance, high reliability, and comprehensive testability.

As shown in Figure 2, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written to during configuration and only read from during readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.

The memory cell outputs Q and $\overline{Q}$ use full ground and V_{CC} levels and provide continuous, direct control. The additional capacitive load and the absence of address decoding and sense amplifiers provide high stability to the cell. Due to their structure, the configuration memory cells are not affected by extreme power supply excursions or very high levels of alpha particle radiation. Soft errors have not been observed in reliability testing.

Two methods of loading configuration data use serial data, while three use byte-wide data. The internal configuration logic utilizes framing information, embedded in the program data by the *ORCA* Foundry Development System, to direct memory cell loading. The serial data framing and length count preamble provide programming compatibility for mixes of various Lucent programmable gate arrays in a synchronous, serial, daisy-chain fashion.

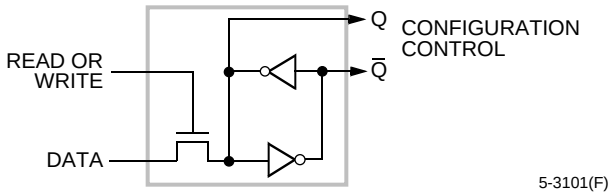


Figure 2. Static Configuration Memory Cell

I/O Block

Each user-configurable I/O block (IOB), shown in Figure 3, provides an interface between the external package pin of the device and the internal user logic. Each IOB includes both registered and direct input paths and a programmable 3-state output buffer which may be driven by a registered or direct output signal. Configuration options allow each IOB an inversion, a controlled slew rate, and a high-impedance pull-up. Each input circuit also provides input clamping diodes to provide electrostatic protection and circuits to inhibit latch-up produced by input currents.

The input buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOB can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element which may be configured as a positive-edge triggered D flip-flop or a low-level transparent latch. The sense of the clock can be inverted (negative edge/high transparent) as long as all IOBs on the same clock net use the same clock sense. Clock/load signals (IOB pins .ik and .ok) can be selected from either of two die edge metal lines. I/O storage elements are reset during configuration or by the active-low chip $\overline{\text{RESET}}$ input. Both direct input (from IOB pin .i) and registered input (from IOB pin .q) signals are available for interconnect.

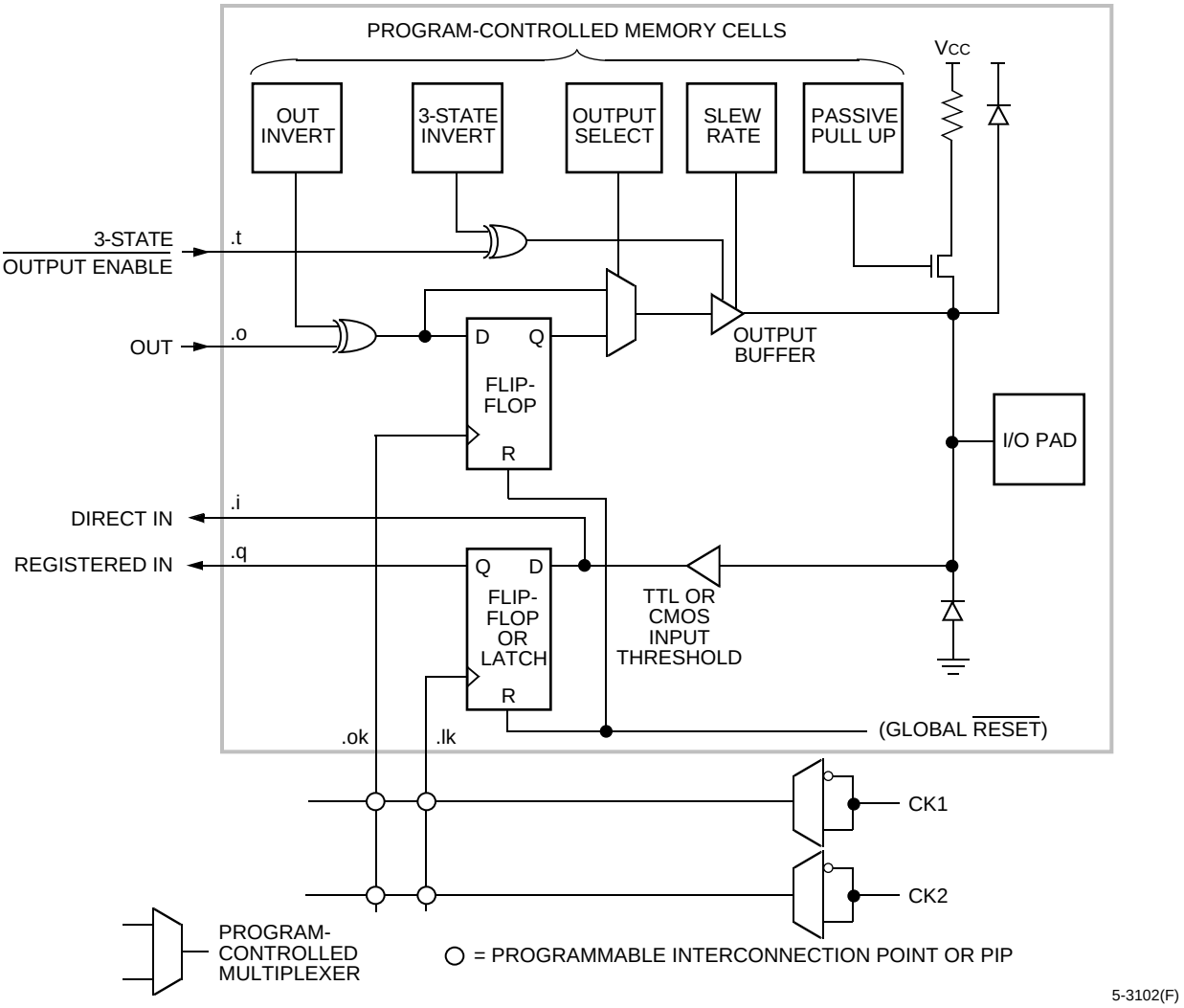


Figure 3. Input/Output Block

I/O Block (continued)

For reliable operation, inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces sensitivity to input noise. Each user IOB includes a programmable high-impedance pull-up resistor which is selected by the program to provide a constant high for otherwise undriven package pins. Normal CMOS handling precautions should be observed.

Flip-flop loop delays for the IOB and logic block flip-flops are approximately 3 ns. This short delay provides good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition which can result from assertion of the clock during data transitions. Because of the short loop delay characteristic in the FPGA, the IOB flip-flops can be used to synchronize external signals applied to the device. When synchronized in the IOB, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing path delays.

Output buffers of the IOBs provide CMOS-compatible 4 mA source-or-sink drive for high fan-out CMOS or TTL compatible signal levels. The network driving IOB pin .o becomes the registered or direct data source for the output buffer. The 3-state control signal (IOB pin .t) can control output activity. An open-drain type output may be obtained by using the same signal for driving the output and 3-state signal nets so that the buffer output is enabled only for a LOW.

Configuration program bits for each IOB control features such as optional output register, logical signal inversion, and 3-state and slew rate control of the output.

The program-controlled memory cells in Figure 3 control the following options:

- Logical inversion of the output is controlled by one configuration program bit per IOB.
- Logical 3-state control of each IOB output buffer is determined by the states of configuration program bits which turn the buffer on or off or select the output buffer 3-state control interconnection (IOB pin .t). When this IOB output control signal is high, a logic 1, the buffer is disabled and the package pin is high impedance. When this IOB output control signal is low, a logic 0, the buffer is enabled and the package pin is active. Inversion of the buffer 3-state control logic sense (output enable) is controlled by an additional configuration program bit.
- Direct or registered output is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied (IOB pin .ok) by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased output transition speed can be selected to improve critical timing. Slower transitions reduce capacitive load peak currents of noncritical outputs and minimize system noise.
- A high-impedance pull-up resistor may be used to prevent unused inputs from floating.

Summary of I/O Options

- Inputs
  —Direct
  —Flip-flop/latch
  —CMOS/TTL threshold (chip inputs)
  —Pull-up resistor/open circuit
- Outputs
  —Direct/registered
  —Inverted/not
  —3-state/on/off
  —Full speed/slew limited
  —3-state/output enable (inverse)

Configurable Logic Block

The array of configurable logic blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. The ATT3020 has 64 such blocks arranged in eight rows and eight columns. The *ORCA* Foundry Development System is used to compile the configuration data for loading into the internal configuration memory to define the operation and interconnection of each block. User definition of CLBs and their interconnecting networks may be done by automatic translation from a schematic capture logic diagram or optionally by installing library or user macros.

Each CLB has a combinatorial logic section, two flip-flops, and an internal control section; see Figure 4 below. There are five logic inputs (.a, .b, .c, .d, and .e); a common clock input (.k); an asynchronous direct reset input (.rd); and an enable clock (.ec). All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs (.x and .y) which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, data-in (.di). Both flip-flops in each CLB share the asynchronous reset (.rd) which, when enabled and high, is dominant over clocked inputs. All flip-flops are reset by the active-low chip input, $\overline{\text{RESET}}$, or during the configuration process.

The flip-flops share the enable clock (.ec) which, when low, recirculates the flip-flops' present states and inhibits its response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input (.k), as well as its active sense within each logic block. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.

The combinatorial logic portion of the logic block uses a 32 x 1 look-up table to implement Boolean functions. Variables selected from the five logic inputs and the two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike-free for single-input variable changes. This technique can generate two independent logic functions of up to four variables each as shown in Figure 5A, or a single function of five variables as shown in Figure 5B, or some functions of seven variables as shown in Figure 5C.

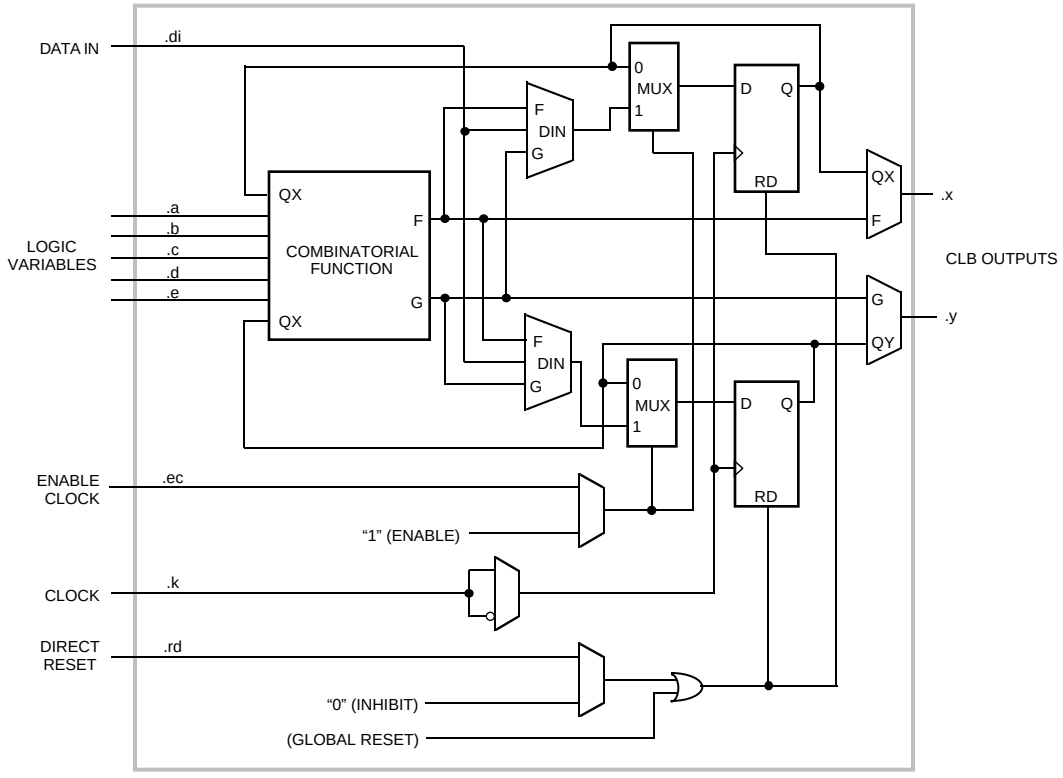
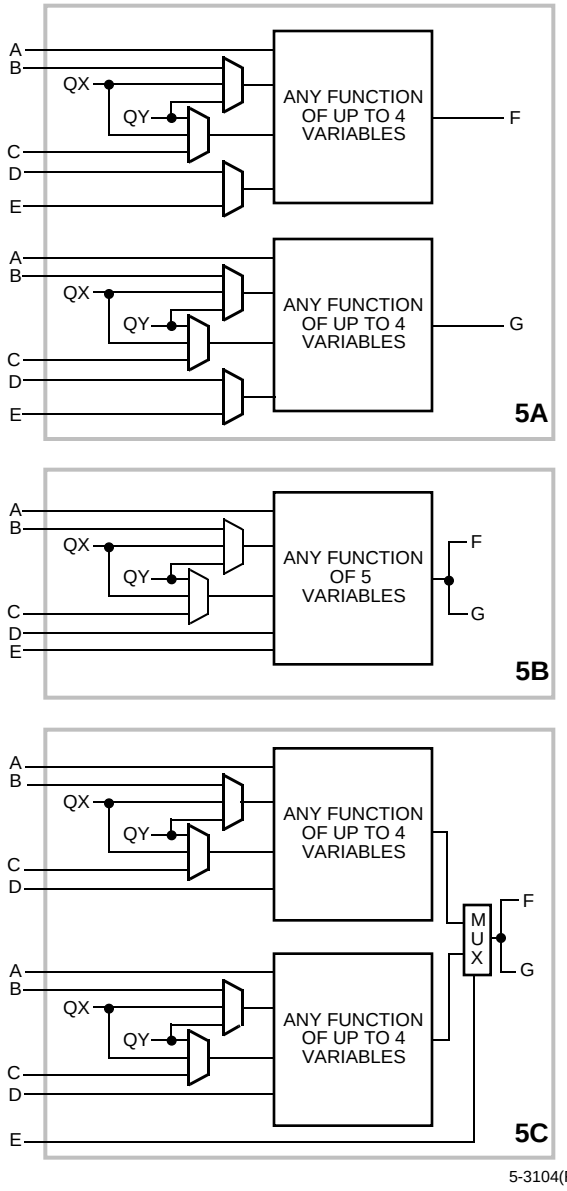


Figure 4. Configurable Logic Block

Configurable Logic Block (continued)



5A. Combinatorial Logic Option 1 generates two functions of four variables each. One variable, A, must be common to both functions. The second and third variables can be any choice among B, C, Qx, and Qy. The fourth variable can be either D or E.

5B. Combinatorial Logic Option 2 generates any function of five variables: A, D, E, and two choices among B, C, Qx, Qy.

5C. Combinatorial Logic Option 3 allows variable E to select between two functions of four variables: both have common inputs, A and D, and any choice among B, C, Qx, and Qy for the remaining two variables. Option 3 can then implement some functions of six or seven variables.

Figure 5. Combinatorial Logic Diagram

Figure 6 shows a modulo 8 binary counter with parallel enable. It uses one CLB of each type. The partial functions of six or seven variables are implemented by using the input variable (.e) to dynamically select between two functions of four different variables. For the two functions of four variables each, the independent results (F and G) may be used as data inputs to either flip-flop or logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops allows the interchange of CLB outputs to optimize routing efficiencies of the networks interconnecting the logic and IOBs.

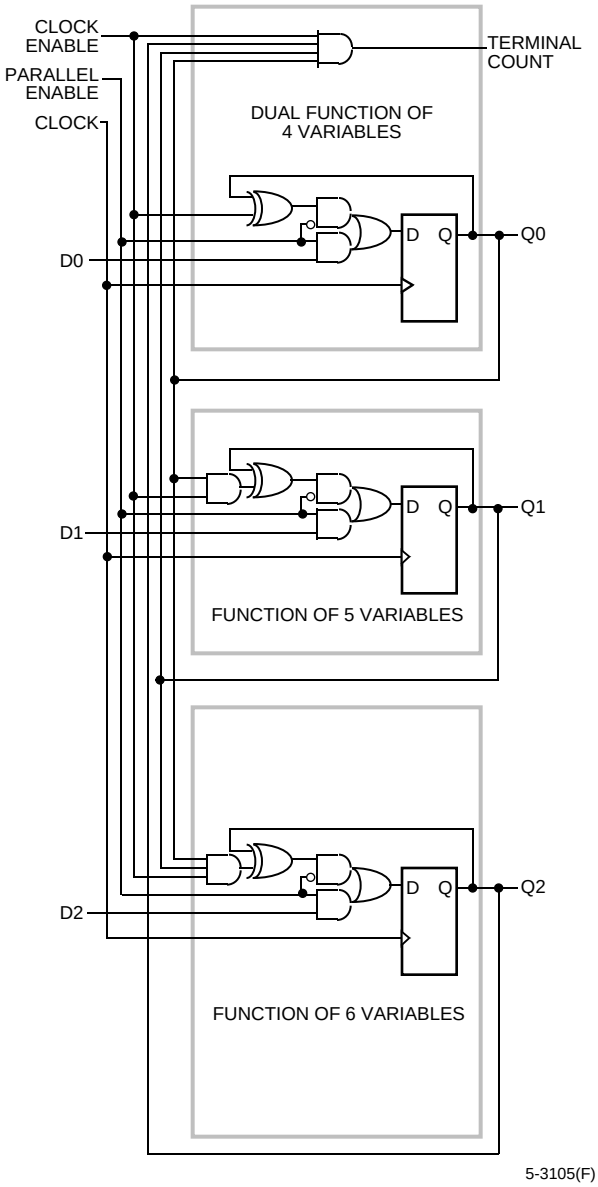


Figure 6. C8BCP Macro

Programmable Interconnect

Programmable interconnection resources in the FPGA provide routing paths to connect inputs and outputs of the IOBs and logic blocks into logical networks. Interconnections between blocks are composed from a two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins.

Figure 7 is an example of a routed net. The *ORCA* Foundry Development System provides automatic routing of these interconnections. Interactive routing is also available for design optimization. The inputs of the logic or IOBs are multiplexers which can be programmed to select an input network from the adjacent interconnect segments. Since the switch connections to block inputs are unidirectional (as are block outputs), they are usable only for block input connection and not routing. Figure 8 illustrates routing access to logic block input variables, control inputs, and block outputs.

Three types of metal resources are provided to accommodate various network interconnect requirements:

- General-purpose interconnect
- Direct connection
- Long lines (multiplexed buses and wide-AND gates)

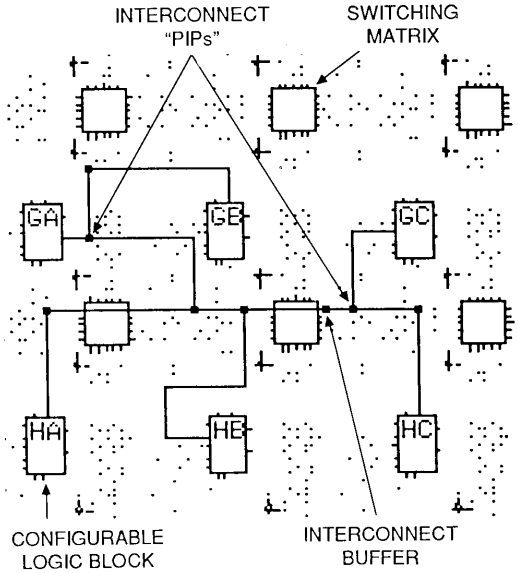


Figure 7. Example of Routing Resources

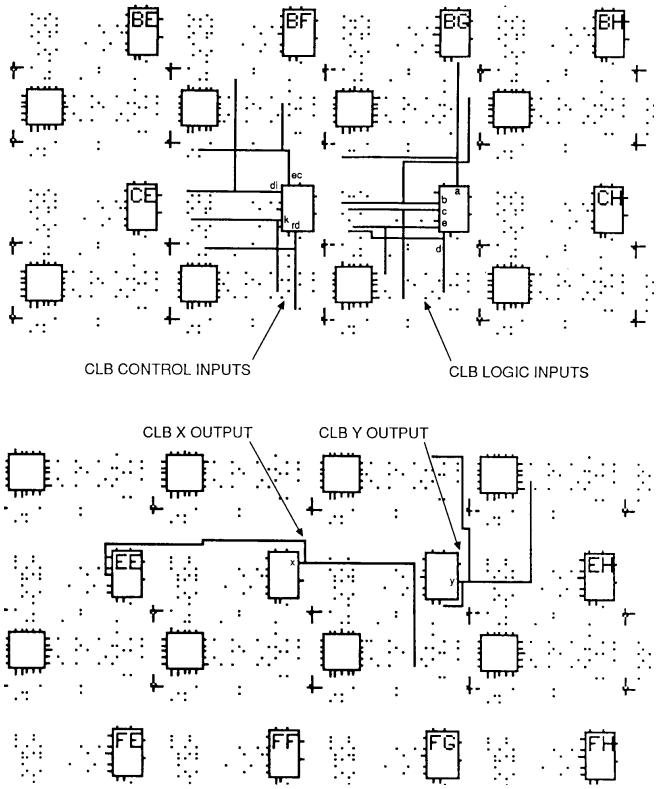


Figure 8. CLB Input and Output Routing

Programmable Interconnect (continued)

General-Purpose Interconnect

General-purpose interconnect, as shown in Figure 9, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and IOBs. Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all nonconducting. The connections through the switch matrix may be established by automatic or interactive routing by selecting the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in Figure 10.

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matrices, above and to the right. The other PIPs adjacent to the matrices are accessed to or from long lines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator in the *ORCA* Foundry Development System automatically calculates and displays the block, interconnect, and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is also provided by the development system.

Some of the interconnect PIPs are directional, as indicated below:

- ND is a nondirectional interconnection.
- D:H->V is a PIP which drives from a horizontal to a vertical line.
- D:V->H is a PIP which drives from a vertical to a horizontal line.
- D:C->T is a T-PIP which drives from a cross of a T to the tail.
- D:CW is a corner PIP which drives in the clockwise direction.
- P0 indicates the PIP is nonconducting; P1 is on.

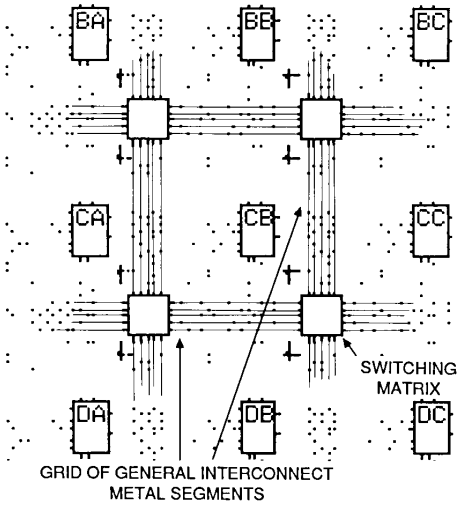


Figure 9. FPGA General-Purpose Interconnect

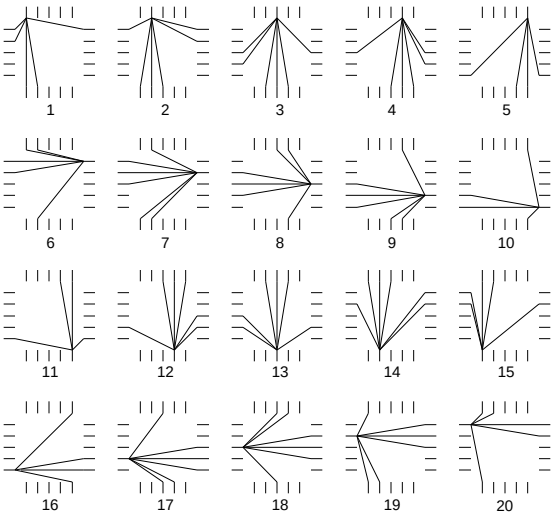


Figure 10. Switch Matrix Interconnection Options

Programmable Interconnect (continued)

Direct Interconnect

Direct interconnect (shown in Figure 11) provides the most efficient implementation of networks between adjacent logic or IOBs. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each CLB, the .x output may be connected directly to the .b input of the CLB immediately to its right and to the .c input of the CLB to its left. The .y output can use direct interconnect to drive the .d input of the block immediately above, and the .a input of the block below. Direct interconnect should be used to maximize the speed of high-performance portions of logic. Where logic blocks are adjacent to IOBs, direct connect is provided alternately to the IOB inputs (.i) and outputs (.o) on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of IOBs with CLBs are shown in Figure 12.

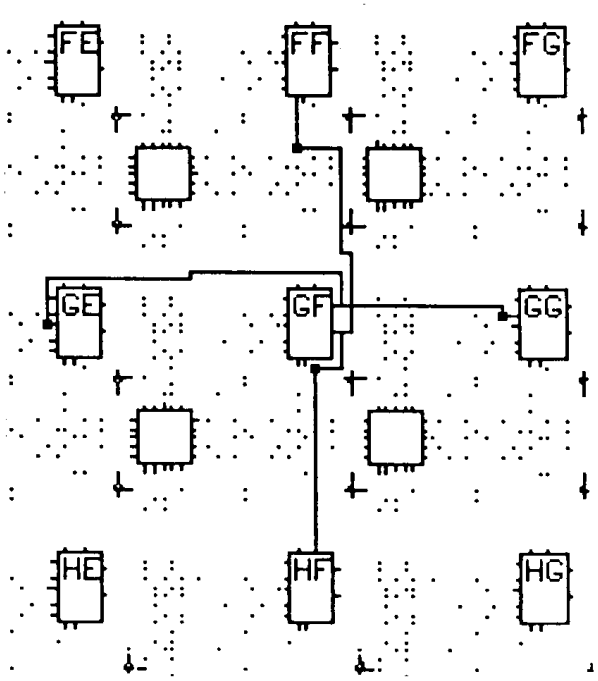


Figure 11. Direct Interconnect

Programmable Interconnect (continued)

Figure 12. ATT3020 Die Edge I/O Blocks with Direct Access to Adjacent CLB

Programmable Interconnect (continued)

Long Lines

The long lines bypass the switch matrices and are intended primarily for signals which must travel a long distance, or must have minimum skew among multiple destinations. Long lines, shown in Figure 13, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical long lines, and each interconnection row has two horizontal long lines. Additionally, two long lines are located adjacent to the outer sets of switching matrices. Two vertical long lines in each column are connectable half-length lines, except on the ATT3020, where only the outer long lines serve that function.

Long lines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low-skew control or clock line within each column of logic blocks. Interconnections of these long lines are shown in Figure 14. Isolation buffers are provided at each input to a long line and are enabled automatically by the development system when a connection is made.

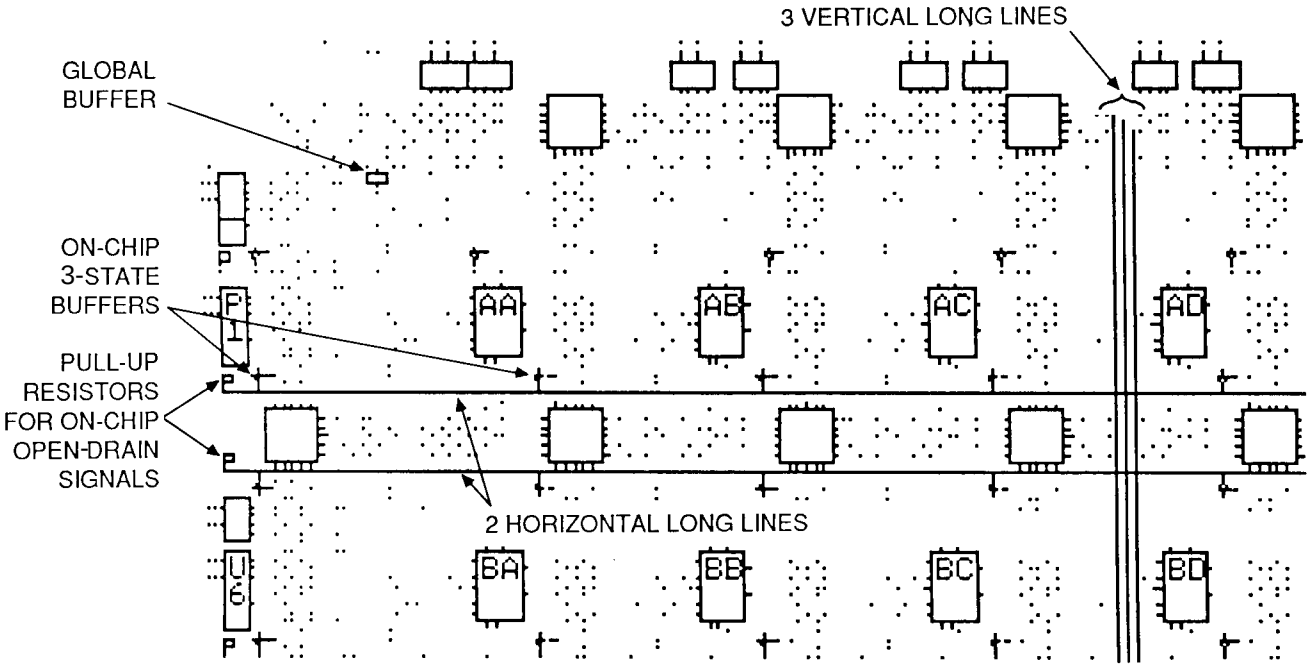


Figure 13. Horizontal and Vertical Long Lines in the FPGA

Programmable Interconnect (continued)

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all .k inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the I/O and logic blocks. Configuration bits for the .k input to each logic block can select this global line, or another routing resource, as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, offers direct access to this buffer and is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal long line that can drive programmed connections to a vertical long line in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's long lines can be selected to drive the .k inputs of the logic blocks. CMOS threshold, high-speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Buses

A pair of 3-state buffers is located adjacent to each CLB. These buffers allow logic to drive the horizontal long lines. Logical operation of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long line bus by applying a low logic level on its 3-state control line (see Figure 15A). The user is required to avoid contention that can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input creates an open-drain wired-AND function. A logical high on both buffer inputs creates a high impedance which represents no contention. A logical low enables the buffer to drive the long line low (see Figure 15B). Pull-up resistors are available at each end of the long line to provide a high output when all connected buffers are nonconducting. This forms fast, wide gating functions. When data drives the inputs and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state buses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Figure 16 shows 3-state buffers, long lines, and pull-up resistors.

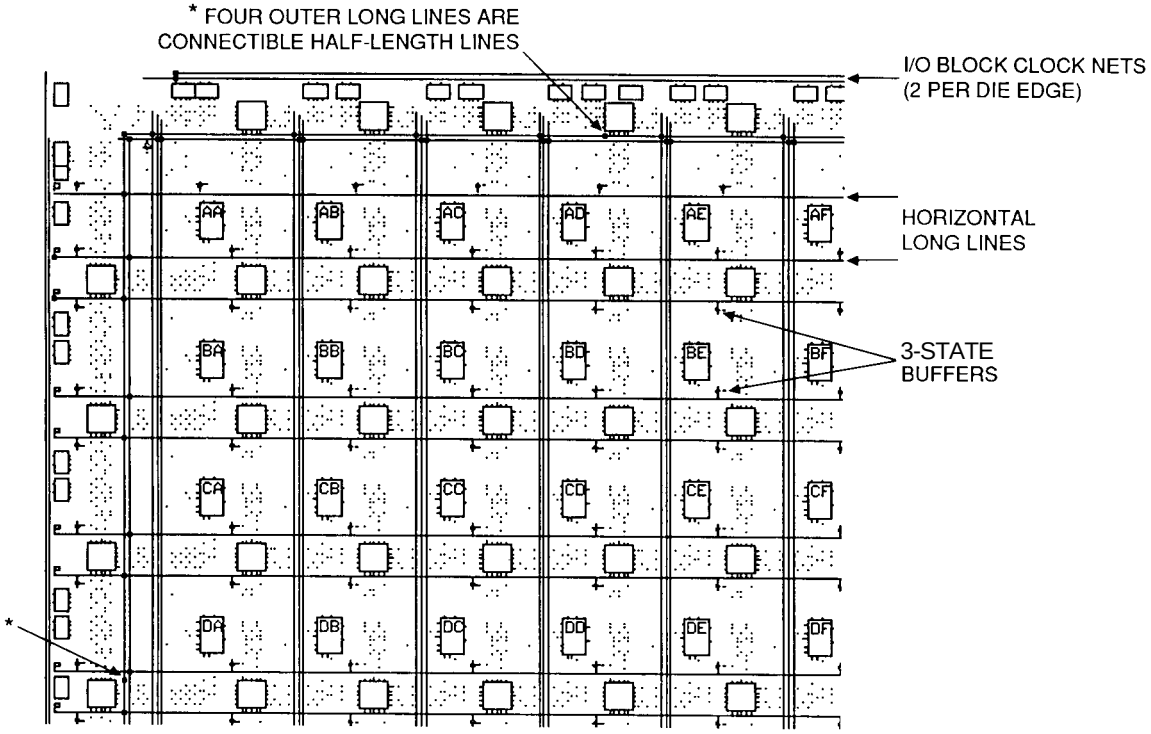


Figure 14. Programmable Interconnection of Long Lines

Programmable Interconnect (continued)

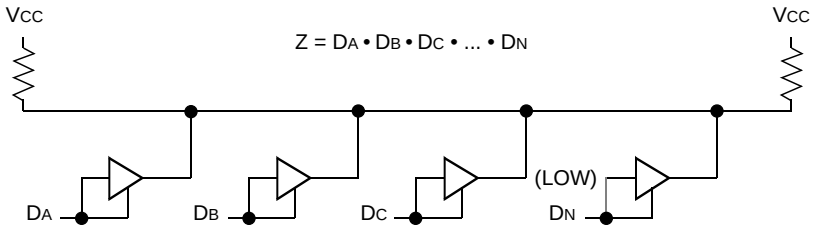


Figure 15A. 3-State Buffers Implement a Wired-AND Function

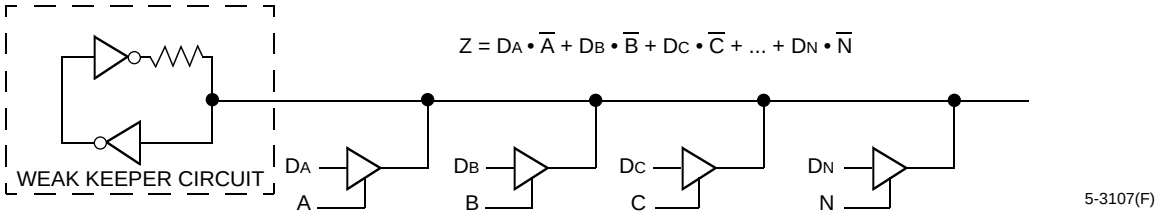


Figure 15B. 3-State Buffers Implement a Multiplexer

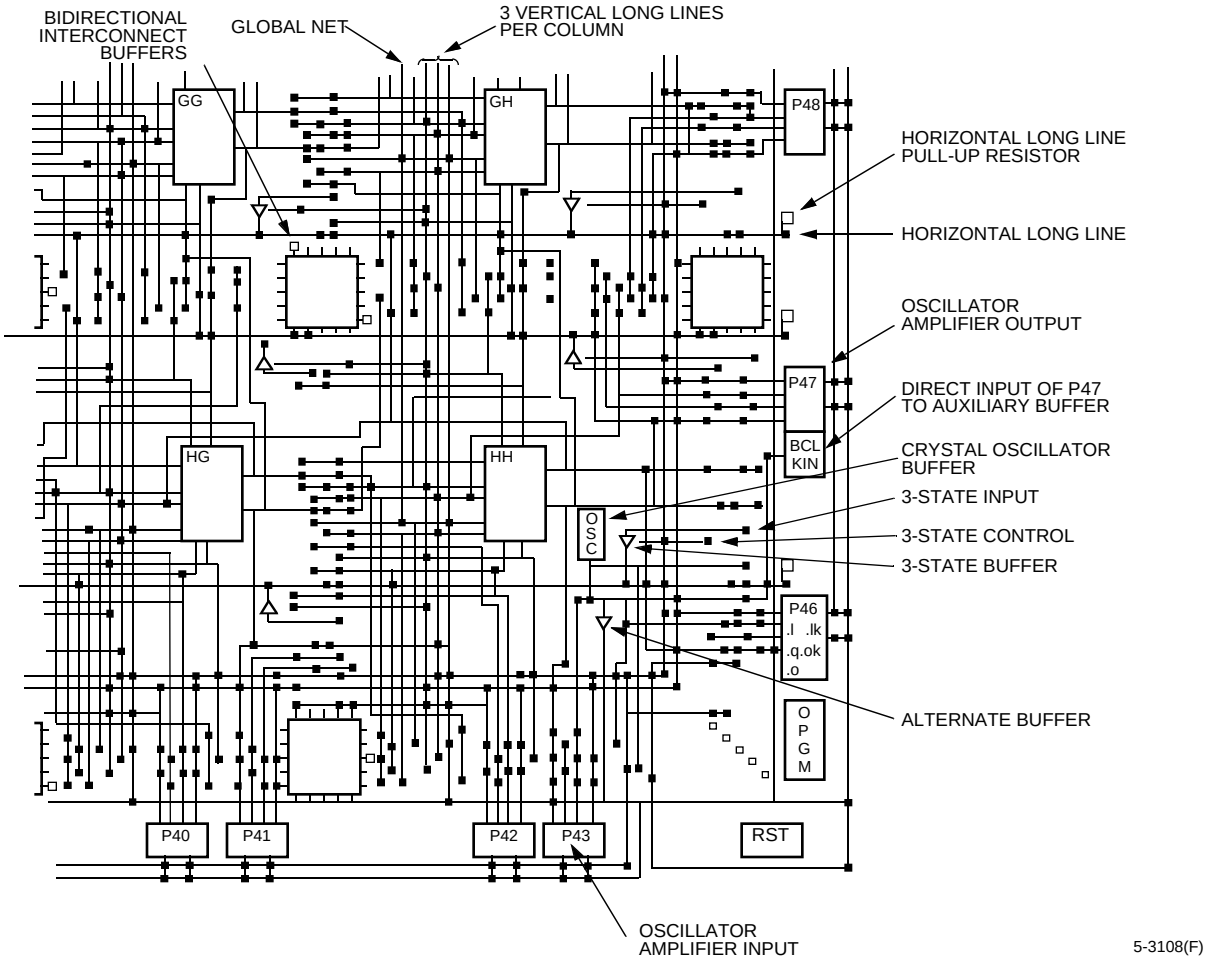
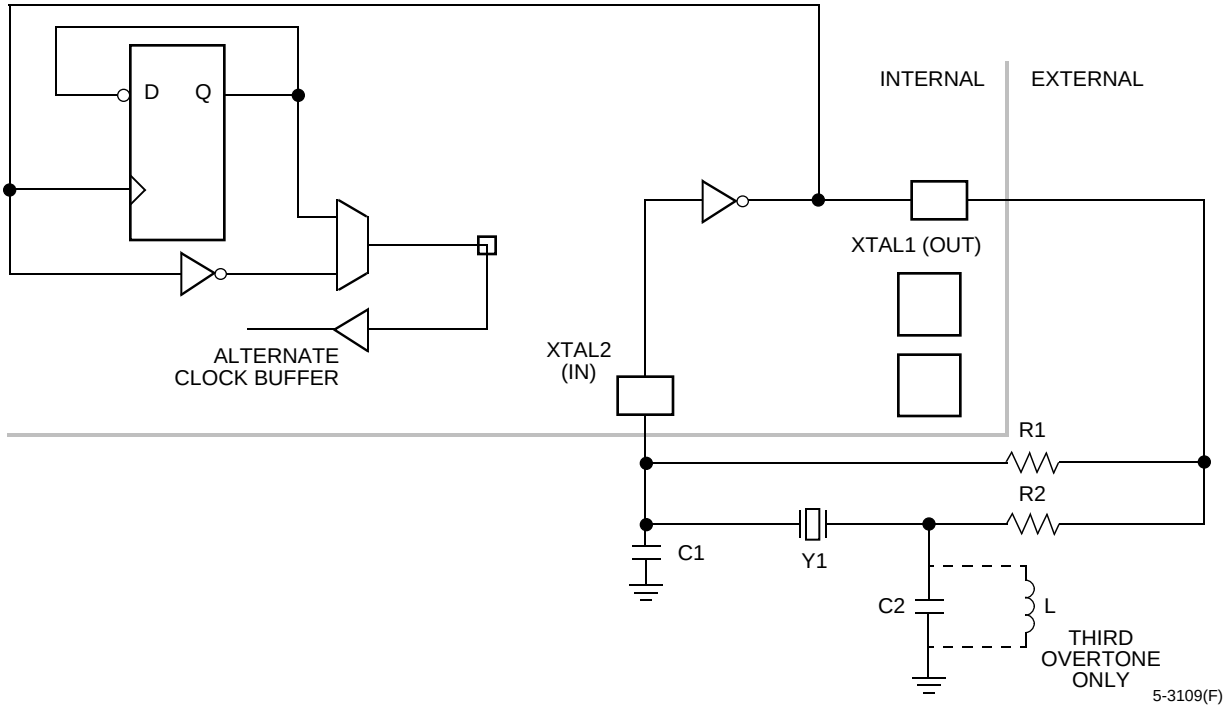


Figure 16. Lower-Right Corner of ATT3020

Programmable Interconnect (continued)

Crystal Oscillator

Figure 16 shows the location of an internal high-speed inverting amplifier which may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured and connected as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 17. A divide-by-two option is available to ensure symmetry. The oscillator circuit becomes active before configuration is complete in order to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 17, the feedback resistor, R1, between output and input biases the amplifier at threshold. The value should be as large as is practical to minimize loading of the crystal. The inversion of the amplifier, together with the R-C networks and an AT cut series resonant crystal, produces the 360° phase shift of the Pierce oscillator. A series resistor, R2, may be included to add to the amplifier output impedance when needed for phase shift control or crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by an inductor across C2. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.



Suggested component values:

R1—0.5 MΩ to 1 MΩ
R2—0 kΩ to 1 kΩ (may be required for low frequency, phase shift, and/or compensation level for Crystal Q)
C1, C2—10 pF to 40 pF
Y1—1 MHz to 20 MHz AT cut series resonant

Pin	44-Pin PLCC	68-Pin PLCC	84-Pin PLCC	100-Pin		132-Pin PPGA	144-Pin TQFP	160-Pin QFP	175-Pin PPGA	208-Pin SQFP
				QFP	TQFP					
XTAL1 (OUT)	30	47	57	82	79	P13	75	82	T14	110
XTAL2 (IN)	26	43	53	76	73	M13	69	76	P15	100

Figure 17. Crystal Oscillator Inverter

Configuration

Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When VCC reaches the voltage where portions of the FPGA begin to operate (2.5 V to 3 V), the programmable I/O output buffers are disabled and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time, the power-down mode is inhibited. The initialization state time-out (about 11 ms to 33 ms) is determined by a 14-bit counter driven by a self-generated, internal timer. This nominal 1 MHz timer is subject to variations with process, temperature, and power supply over the range of 0.5 MHz to 1.5 MHz. As shown in Table 2, five configuration mode choices are available, as determined by the input levels of three mode pins: M0, M1, and M2.

Table 2. Configuration Modes

M0	M1	M2	Clock	Mode	Data
0	0	0	Active	Master	Bit Serial
0	0	1	Active	Master	Byte Wide (Address = 0000 up)
0	1	0	—	Reserved	—
0	1	1	Active	Master	Byte Wide (Address = FFFF down)
1	0	0	—	Reserved	—
1	0	1	Active	Peripheral	Byte Wide
1	1	0	—	Reserved	—
1	1	1	Passive	Slave	Bit Serial

In master configuration mode, the FPGA becomes the source of configuration clock (CCLK). Beginning configuration of devices using peripheral or slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a master configuration mode extends its initialization state using four times the delay (43 ms to 130 ms) to ensure that all daisy-chained slave devices it may be driving will be ready, even if the master is very fast and the slave(s), very slow (see Figure 18). At the end of initialization, the FPGA enters the clear state where it clears configuration memory. The active-low, open-drain initialization signal $\overline{\text{INIT}}$ indicates when the initialization and clear states are complete. The FPGA tests for the absence of an external active-low $\overline{\text{RESET}}$ before it makes a final sample of the mode lines and enters the configuration state. An external wired-AND of one or more $\overline{\text{INIT}}$ pins can be used to control configuration by the assertion of the active-low $\overline{\text{RESET}}$ of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a reassertion of $\overline{\text{RESET}}$ for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the clear state to clear the partially loaded configuration memory words. The FPGA will then resample $\overline{\text{RESET}}$ and the mode lines before reentering the configuration state.

A reprogram is initiated when a configured FPGA senses a high-to-low transition on the DONE/$\overline{\text{PROG}}$ package pin. The FPGA returns to the clear state where configuration memory is cleared and mode lines resampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Configuration (continued)

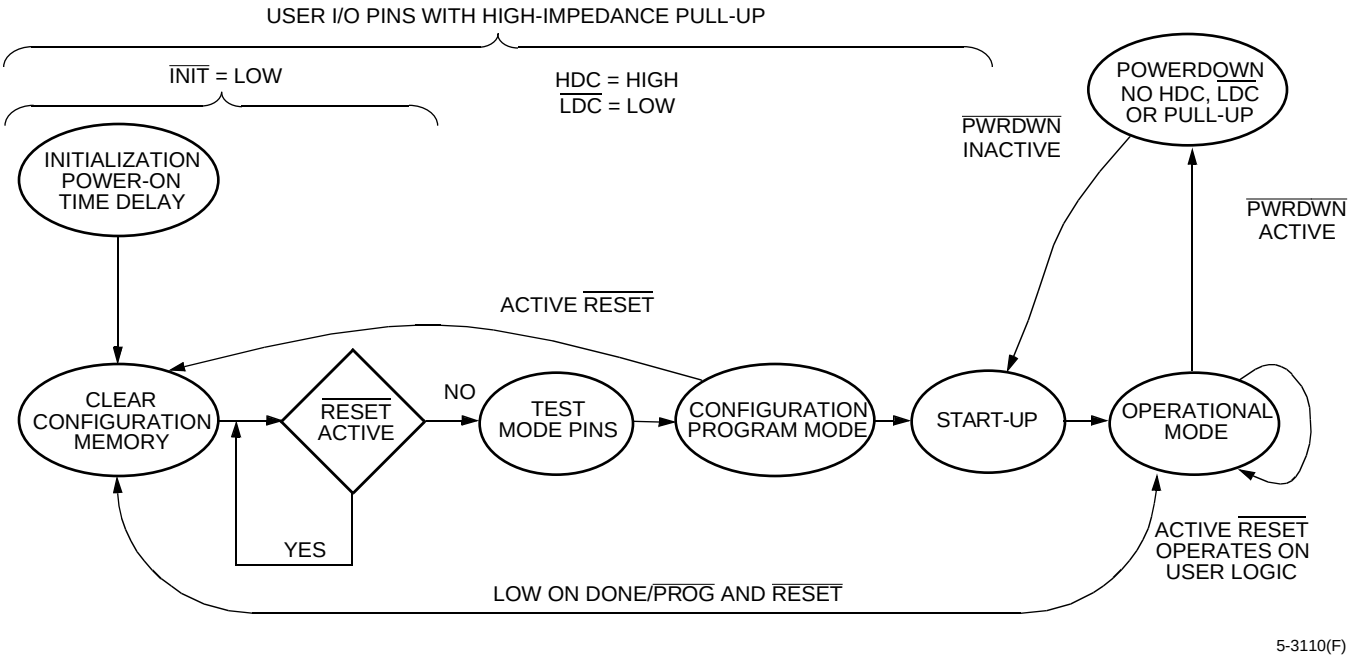


Figure 18. State Diagram of Configuration Process for Powerup and Reprogram

Length count control allows a system of multiple FPGAs in assorted sizes to begin operation in a synchronized fashion. The configuration program generated by the *ORCA* Foundry Development System begins with a preamble of 111111110010 (binary), followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 19. All FPGAs connected in series read and shift preamble and length count in (on positive) and out (on negative) CCLK edges. An FPGA which has received the preamble and length count then presents a HIGH data out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not compare, the FPGA shifts any additional data through, as it did for preamble and length count.

When the FPGA configuration memory is full and the length count compares, the FPGA will execute a synchronous start-up sequence and become operational (see Figure 20 on page 20). Two CCLK cycles after the completion of loading configuration data, the user I/O pins are enabled as configured. As selected in *ORCA* Foundry, the internal user-logic reset is released either one clock cycle before or after the I/O pins become active. A similar timing selection is programmable for the DONE/$\overline{\text{PROG}}$ output signal. DONE/$\overline{\text{PROG}}$ may also be programmed to be an open drain or include a pull-up resistor to accommodate wired-ANDing. The high during configuration (HDC) and low during configuration ($\overline{\text{LDC}}$) are two user I/O pins which are driven active when an FPGA is in initialization, clear, or configure states. These signals and DONE/$\overline{\text{PROG}}$ provide for control of external logic signals such as reset, bus enable, or PROM enable during configuration.

For parallel master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

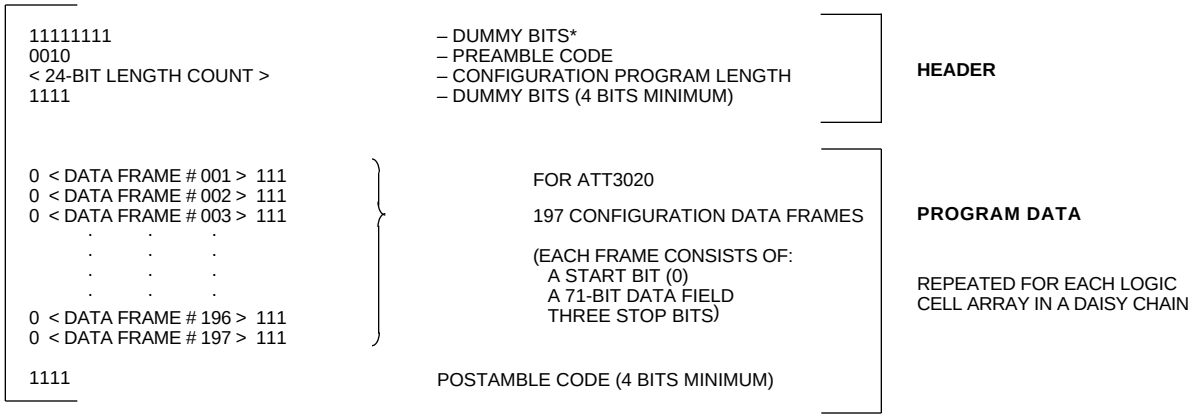
User I/O inputs can be programmed to be either TTL or CMOS compatible thresholds. At powerup, all inputs have TTL thresholds and can change to CMOS thresholds at the completion of configuration, if the user has selected CMOS thresholds. The threshold of $\overline{\text{PWRDWN}}$ and the direct clock inputs are fixed at a CMOS level.

If the crystal oscillator is used, it will begin operation before configuration is complete to allow time for stabilization before it is connected to the internal circuitry.

Configuration (continued)

Configuration Data

Configuration data to define the function and interconnection within an FPGA are loaded from an external storage at powerup and on a reprogram signal. Several methods of automatic and controlled loading of the required data are available. Logic levels applied to mode selection pins at the start of configuration time determine the method to be used (see Table 2). The data may be either bit-serial or byte-parallel, depending on the configuration mode. Various Lucent programmable gate arrays have different sizes and numbers of data frames. For the ATT3020, configuration requires 14779 bits for each device, arranged in 197 data frames. An additional 40 bits are used in the header (see Figure 20).



* The FPGA devices require four dummy bits minimum.

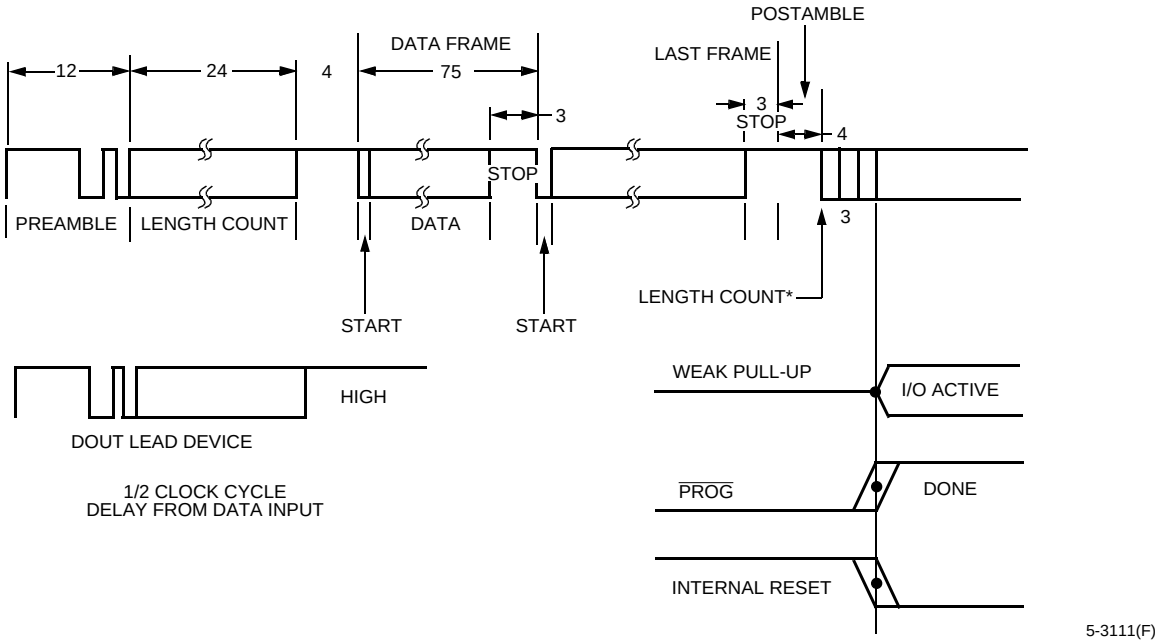
Figure 19. Internal Configuration Data Structure

Configuration (continued)

Table 3. ATT3000 Device Configuration Data

Device	ATT3020	ATT3030	ATT3042	ATT3064	ATT3090
Gates	1500	2000	3000	4500	6000
CLBs (row x column)	64 (8 x 8)	100 (10 x 10)	144 (12 x 12)	224 (16 x 14)	320 (20 x 16)
IOBs	64	80	96	120	144
Flip-flops	256	360	480	688	928
Bits-per-frame (with 1 start/3 stop)	75	92	108	140	172
Frames	197	241	285	329	373
Program Data = Bits * Frames + 4 (excludes header)	14779	22176	30784	46064	64160
PROM Size (bits) = Program Data + 40-bit Headers	14819	22216	30824	46104	64200

Note: The length count produced by the bit stream generation program = [(40-bit preamble + sum of program data + 1 per daisy-chain device) rounded up to a multiple of 8] – (2 ≤ K ≤ 4), where K is a function of DONE and $\overline{\text{RESET}}$ timing selected. An additional 8 is added if the roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.



* The configuration data consists of a composite 40-bit preamble/length count, followed by one or more concatenated FPGA programs, separated by 4-bit postambles. An additional final postamble bit is added for each slave device, and the result rounded up to byte boundary. The length count is two less than the number of resulting bits. Timing of the assertion of DONE and termination of the internal RESET may each be programmed to occur one cycle before or after the I/O outputs become active.

Figure 20. FPGA Configuration and Start-Up

Configuration (continued)

The specific data format for each device is produced by the bit stream generation program, and one or more of these files can then be combined and appended to a length count preamble and be transformed into a PROM format file by the PROM generation program of the *ORCA* Foundry Development System. The tie option of the bit stream generation program defines output levels of unused blocks of a design and connects these to unused routing resources. This prevents indeterminate levels which might produce parasitic supply currents. This tie option can be omitted for quick breadboard iterations where a few additional mA of I_{CC} are acceptable.

The configuration bit stream begins with high preamble bits, a 4-bit preamble code, and a 24-bit length count. When configuration is initiated, a counter in the FPGA is set to 0 and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the FPGA, it is internally assembled into a data word. As each data word is completely assembled, it is loaded in parallel into one word of the internal configuration memory array. The configuration loading process is complete when the current length count equals the loaded length count and the required configuration program data frames have been written. Internal user flip-flops are held reset during configuration.

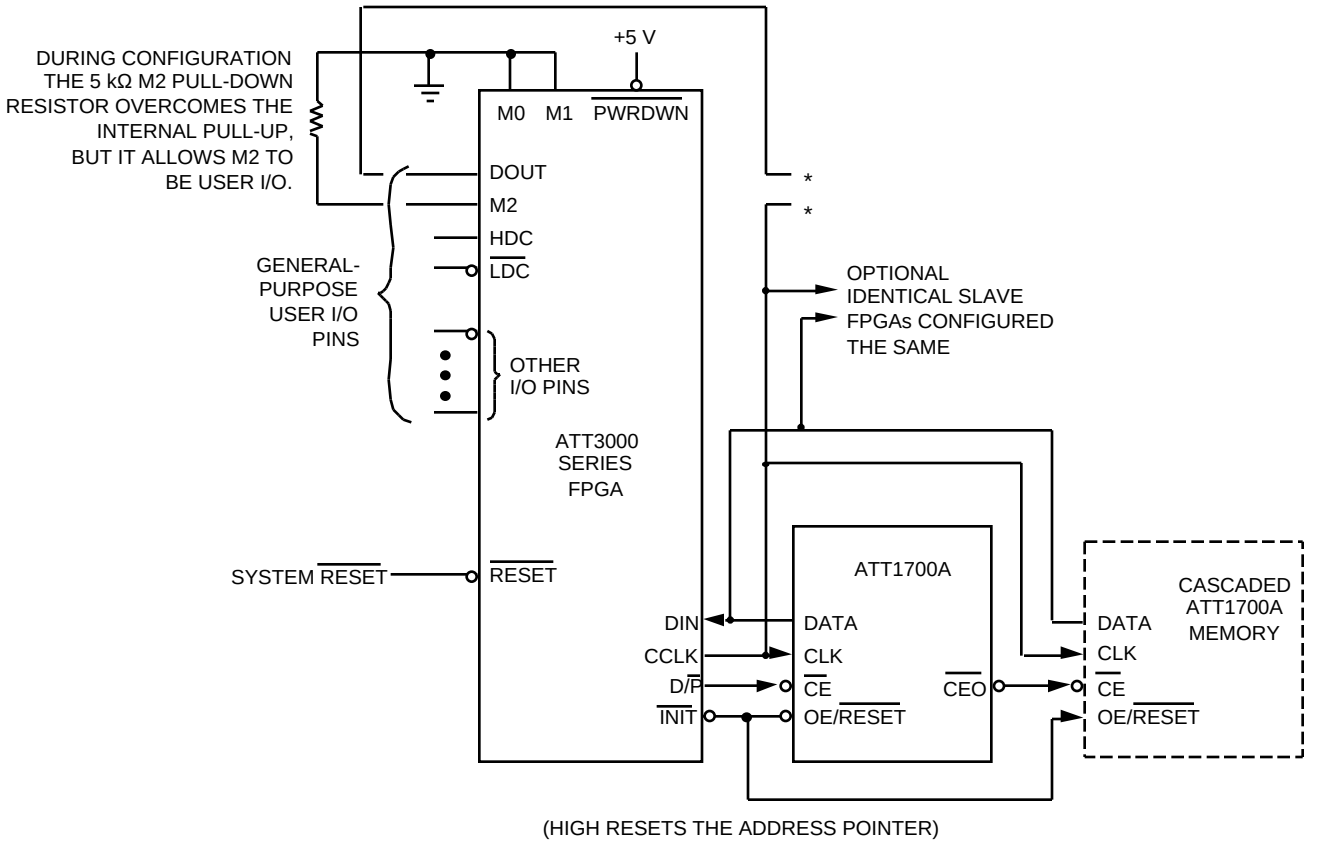
Two user-programmable pins are defined in the unconfigured FPGA: high during configuration (HDC) and low during configuration ($\overline{\text{LDC}}$), and DONE/$\overline{\text{PROG}}$ may be used as external control signals during configuration. In master mode configurations, it is convenient to use $\overline{\text{LDC}}$ as an active-low EPROM chip enable. After the last configuration data bit is loaded and the length count compares, the user I/O pins become active. Options in the bit stream generation program allow timing choices of one clock earlier or later for the timing of the end of the internal logic reset and the assertion of the DONE signal. The open-drain DONE/$\overline{\text{PROG}}$ output can be AND-tied with multiple FPGAs and used as an active-high READY, an active-low PROM enable, or a RESET to other portions of the system. The state diagram of Figure 18 illustrates the configuration process.

Configuration Modes

Master Mode

In master mode, the FPGA automatically loads configuration data from an external memory device. There are three master modes which use the internal timing source to supply the configuration clock (CCLK) to time the incoming data. Serial master mode uses serial configuration data supplied to data-in (DIN) from a synchronous serial source such as the serial configuration PROM shown in Figure 21. Parallel master low and master high modes automatically use parallel data supplied to the D[7:0] pins in response to the 16-bit address generated by the FPGA. Figure 22 shows an example of the parallel master mode connections required. The FPGA HEX starting address is 0000 and increments for master low mode, and it is FFFF and decrements for master high mode. These two modes provide address compatibility with microprocessors which begin execution from opposite ends of memory.

For master high or low, data bytes are read in parallel by each read clock ($\overline{RCLK}$) and internally serialized by the configuration clock. As each data byte is read, the least significant bit of the next byte, D0, becomes the next bit in the internal serial configuration word. One master mode FPGA can be used to interface the configuration program-store, and pass additional concatenated configuration data to additional FPGAs in a serial daisy-chain fashion. CCLK is provided for the slaved devices, and their serialized data is supplied from DOUT to DIN, DOUT to DIN, etc.



Note: The serial configuration PROM supports automatic loading of configuration programs up to 36/64/128 Kbits. Multiple devices can be cascaded to support additional FPGAs. An early DONE inhibits the data output one CCLK cycle before the FPGA I/O becomes active.

Figure 21. Master Serial Mode

Configuration Modes (continued)

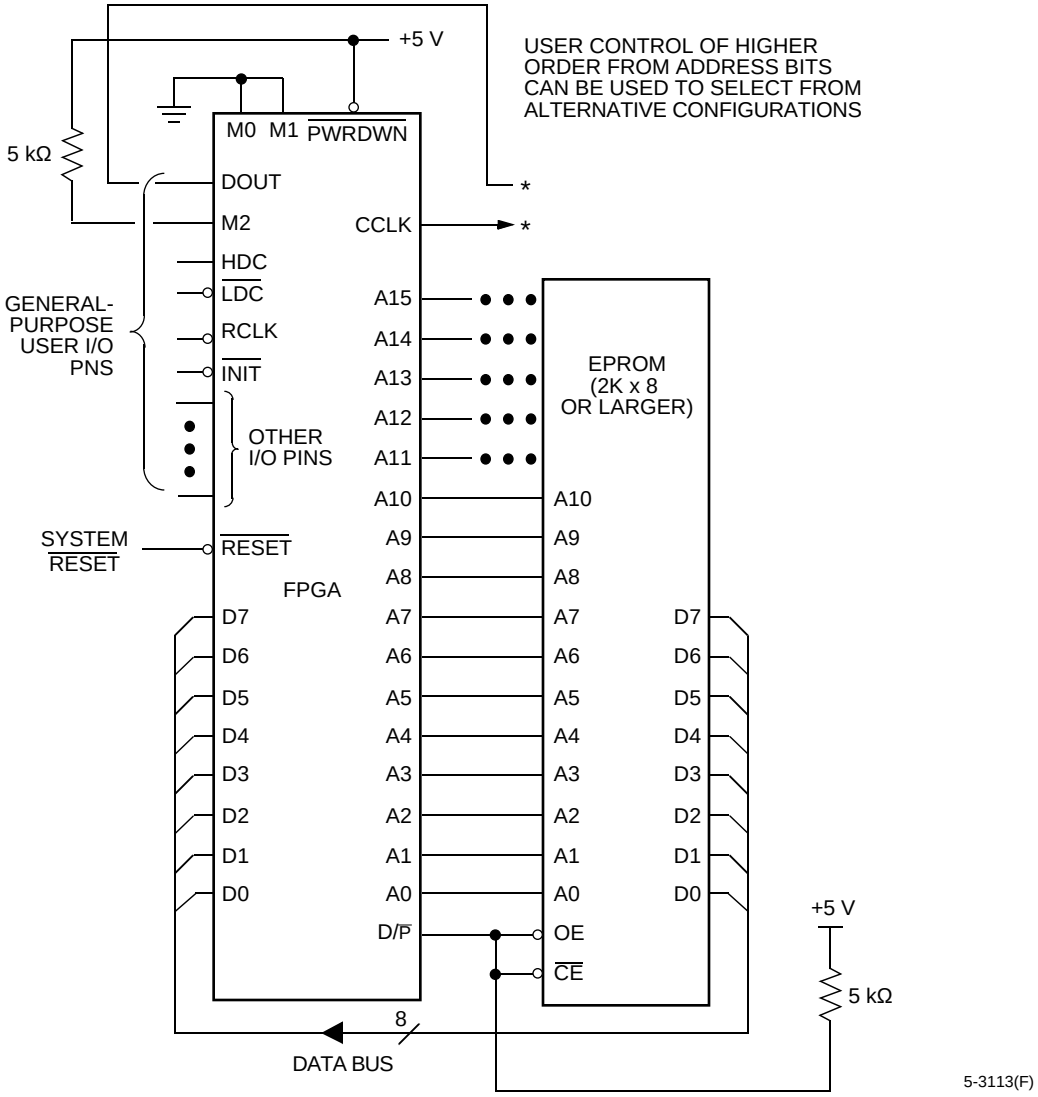


Figure 22. Master Parallel Mode

Configuration Modes (continued)

Peripheral Mode

Peripheral mode provides a simplified interface through which the device may be loaded byte-wide, as a processor peripheral. Figure 23 shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active-low write strobe ($\overline{WS}$), and two active-low and one active-high chip selects ($\overline{CS0}$, $\overline{CS1}$, CS2). If all of these signals are not available, the unused inputs should be driven to their respective active levels. The FPGA will accept 1 byte of configuration data on the D[7:0] inputs for each selected processor write cycle. Each byte of data is loaded into a buffer register. The FPGA generates a CCLK from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on data out (DOUT). An output HIGH on READY/$\overline{BUSY}$ pin indicates the completion of loading for each byte when the input register is ready for a new byte. As with master modes, peripheral mode may also be used as a lead device for a daisy-chain of slave devices.

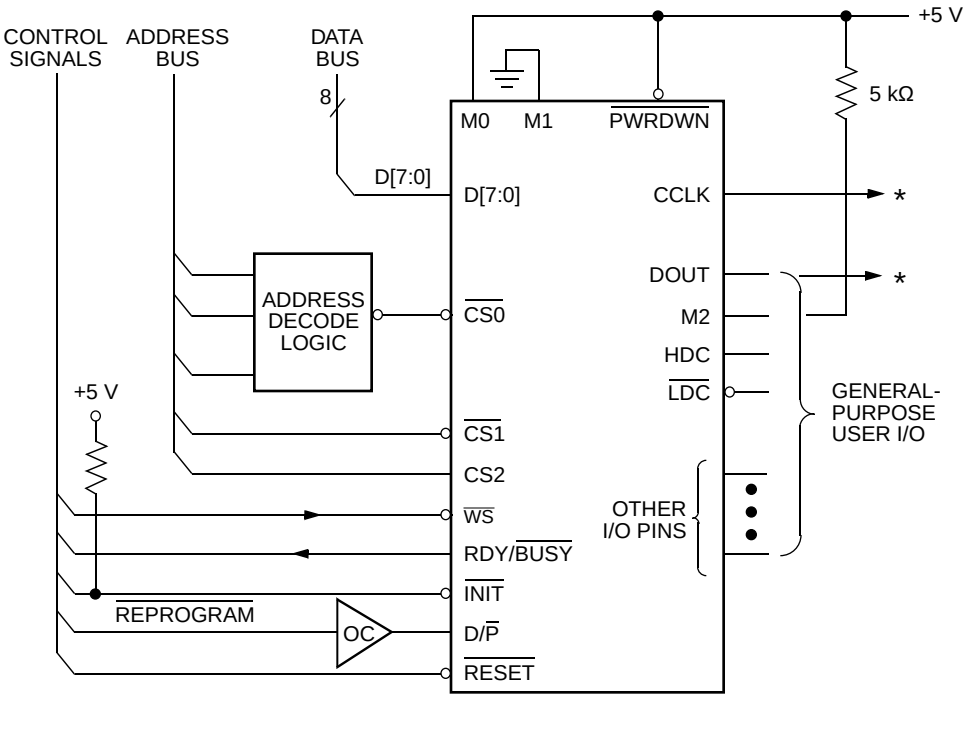


Figure 23. Peripheral Mode

Configuration Modes (continued)

Slave Mode

Slave mode provides a simple interface for loading the FPGA configuration as shown in Figure 24. Serial data is supplied in conjunction with a synchronizing input clock. Most slave mode applications are in daisy-chain configurations in which the data input is supplied by the previous FPGA's data out, while the clock is supplied by a lead device in master or peripheral mode. Data may also be supplied by a processor or other special circuits.

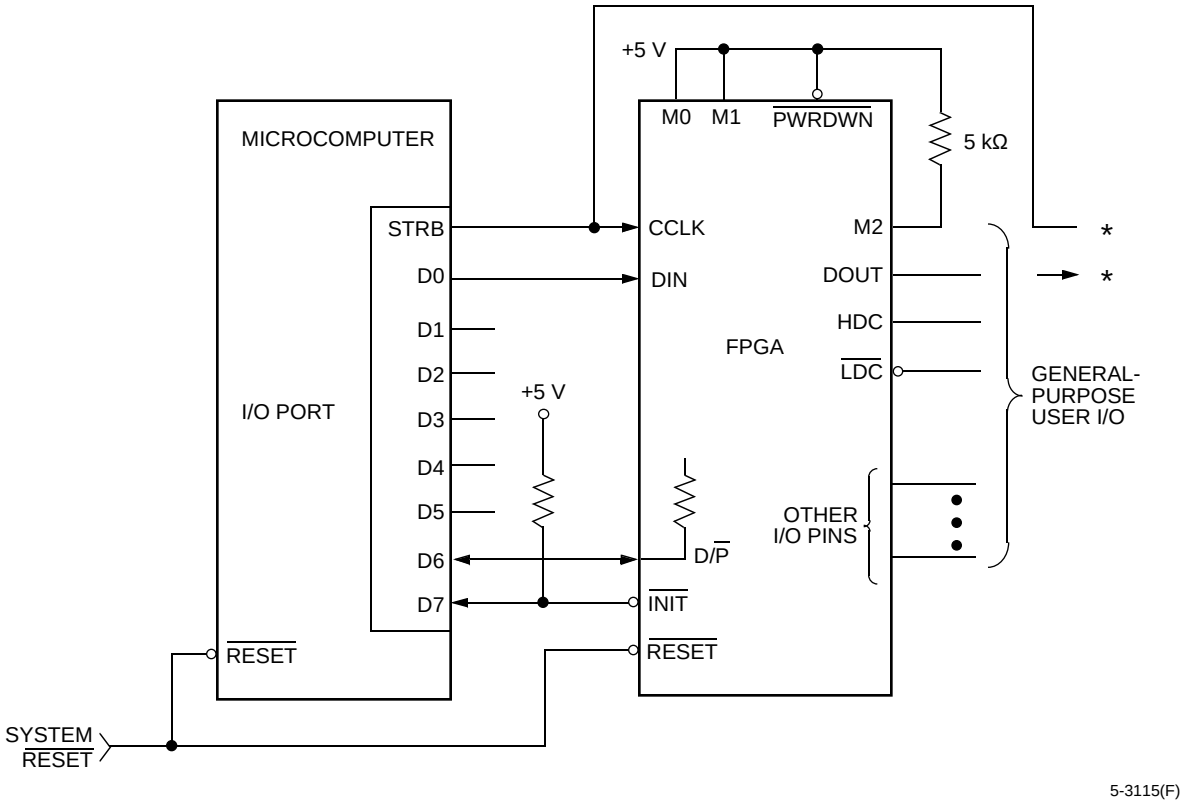


Figure 24. Slave Mode

Configuration Modes (continued)

Daisy Chain

The *ORCA* Foundry for ATT3000 Development System is used to create a composite configuration bit stream for selected FPGAs including a preamble, a length count for the total bit stream, multiple concatenated data programs, a postamble, plus an additional fill bit per device in the serial chain. After loading and passing on the preamble and length count to a possible daisy chain, a lead device will load its configuration data frames while providing a high DOUT to possible downstream devices as shown in Figure 25. Loading continues while the lead device has received its configuration program and the current length count has not reached the full value. Additional data is passed through the lead device and appears on the data out (DOUT) pin in serial form. The lead device also generates the CCLK to synchronize the serial output data and data in of downstream FPGAs. Data is read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel master mode device uses its internal timing generator to produce an internal CCLK of eight times its EPROM address rate, while a peripheral mode device produces a burst of eight CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.

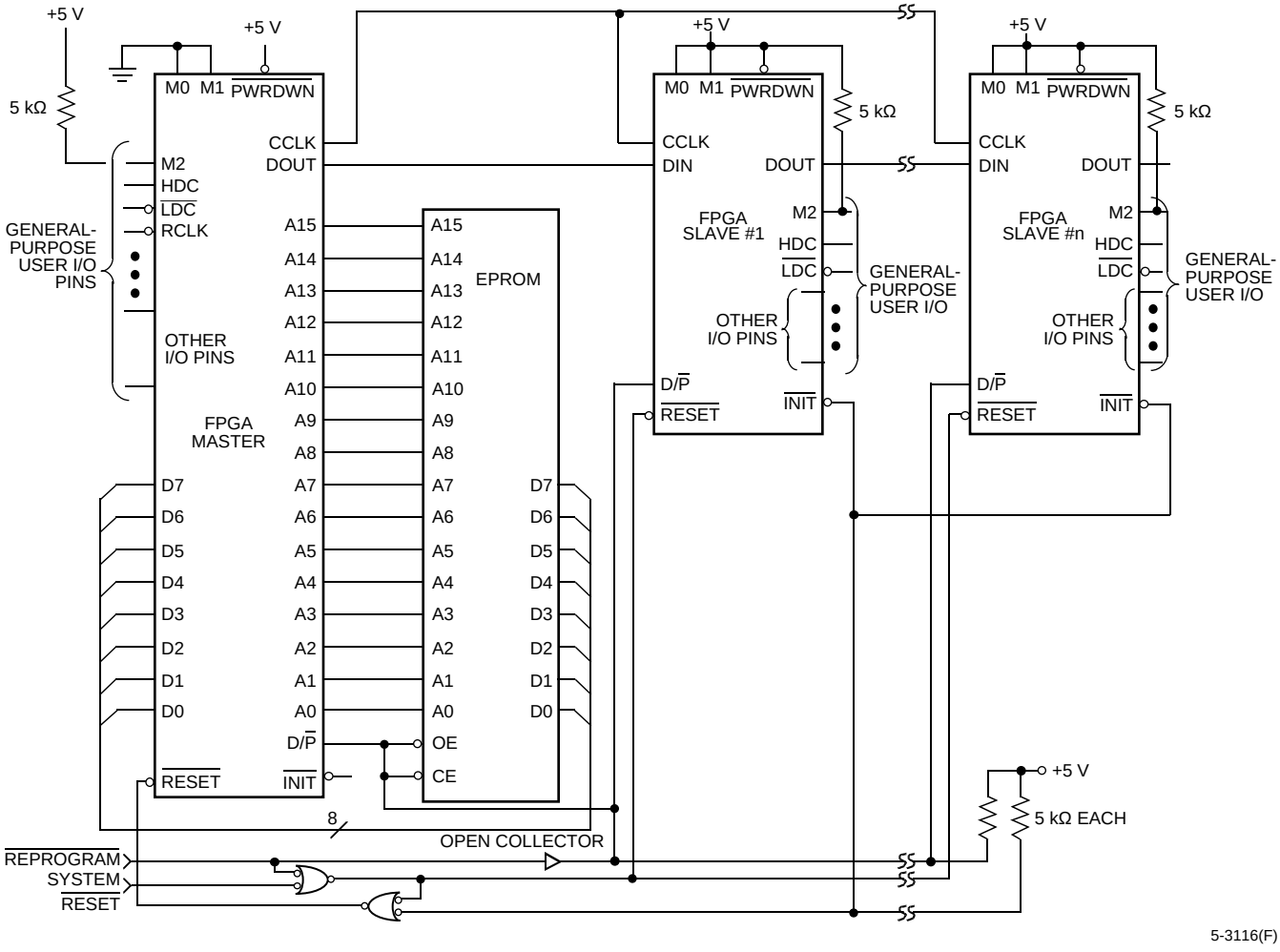


Figure 25. Master Mode with Daisy-Chained Slave Mode Devices

Special Configuration Functions

The configuration data includes control over several special functions in addition to the normal user logic functions and interconnects:

- Input thresholds
- Readback enable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal development system bit stream generation process.

Input Thresholds

Prior to the completion of configuration, all FPGA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the $\overline{\text{PWRDWN}}$ input and direct clocks which always have a CMOS input. Prior to the completion of configuration, the user I/O pins each have a high-impedance pull-up. The configuration program can be used to enable the IOB pull-up resistors in the operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of an FPGA may be read back if it has been programmed with a bit stream in which the readback option has been enabled. Readback may be used for verification of configuration and as a method for determining the state of internal logic nodes. There are three options in generating the configuration bit stream:

- **Never** will inhibit the readback capability.
- **One-time** will inhibit readback after one readback has been executed to verify the configuration.
- **On-command** will allow unrestricted use of readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1, and CCLK are used. The initiation of readback is produced by a low-to-high transition of the M0/RTRIG (read trigger) pin. Once the readback command has been given, the input CCLK is driven by external logic to read back each data bit in a format similar to loading. After two dummy bits, the first data frame is shifted out on the M1/RDATA (read data) pin. The logic polarity of the readback data is always inverted, such that a zero in configuration becomes a one in readback and vice versa. Each readback frame has one start bit and one stop bit per frame (configuration writes at least 3 stop bits per frame). All data frames must be read back to complete the process and return the mode select and CCLK pins to their normal functions.

The readback data includes the current state of each internal logic block storage element, and the state of the input (.i and .ri) connection pins on each IOB. The data is imbedded into unused configuration bit positions during readback. This state information is used by the FPGA development system in-circuit verifier to provide visibility into the internal operation of the logic while the system is operating. To read back a uniform time sample of all storage elements, it may be necessary to inhibit the system clock.

Special Configuration Functions
(continued)

Reprogram

The FPGA configuration memory can be rewritten while the device is operating in the user's system. To initiate a reprogramming cycle, the dual-function package pin DONE/$\overline{\text{PROG}}$ must be given a high-to-low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the FPGA's internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the clear state and clears the configuration memory before it prompts **INITIALIZED**. Since this clear operation uses chip-individual internal timing, the master might complete the clear operation and then start configuration before the slave has completed the clear operation. To avoid this, wire-AND the slave $\overline{\text{INIT}}$ pins and use them to force a $\overline{\text{RESET}}$ on the master (see Figure 25). Reprogram control is often implemented by using an external open-collector driver which pulls DONE/$\overline{\text{PROG}}$ low. Once it recognizes a stable request, the FPGA will hold a low until the new configuration has been completed. Even if the reprogram request is externally held low beyond the configuration period, the FPGA will begin operation upon completion of configuration.

DONE Pull-Up

DONE/$\overline{\text{PROG}}$ is an open-drain I/O pin that indicates the FPGA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the development system when the bit stream generation program is executed. The DONE/$\overline{\text{PROG}}$ pins of multiple FPGAs in a daisy chain may be connected together to indicate that all are DONE or to direct them all to reprogram.

DONE Timing

The timing of the DONE status signal can be controlled by a selection in the bit stream generation program to occur a CCLK cycle before, or after, the timing of outputs being activated (see Figure 20). This facilitates control of external functions, such as a PROM enable or holding a system in a wait-state.

RESET Timing

As with DONE timing, the timing of the release of the internal RESET can be controlled by a selection in the bit stream generation program to occur a CCLK cycle before, or after, the timing of outputs being enabled (see Figure 20). This reset maintains all user-programmable flip-flops and latches in a zero state during configuration.

Crystal Oscillator Division

A selection in the bit stream generation program allows the user to incorporate a dedicated divide-by-two flip-flop in the crystal oscillator function. This provides higher assurance of a symmetrical timing signal. Although the frequency stability of crystal oscillators is high, the symmetry of the waveform can be affected by bias or feedback drive.

Performance

Device Performance

The high performance of the FPGA is due in part to the manufacturing process, which is similar to that used for high-speed CMOS static memories. Performance can be measured in terms of minimum propagation times for logic elements. The parameter which traditionally describes the overall performance of a gate array is the toggle frequency of a flip-flop. The configuration for determining the toggle performance of the FPGA is shown in Figure 26. The flip-flop output Q is fed back through the combinatorial logic as Q to form the toggle flip-flop.

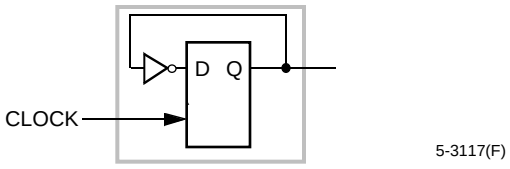


Figure 26. Toggle Flip-Flop

FPGA performance is determined by the timing of critical paths, including both the fixed timing for the logic and storage elements in that path, and the timing associated with the routing of the network. Examples of internal worst-case timing are included in the performance data to allow the user to make the best use of the capabilities of the device. The *ORCA* Foundry Development System timing calculator or *ORCA* Foundry-generated simulation models should be used to calculate worst-case paths by using actual impedance and loading information.

Figure 27 shows a variety of elements which are involved in determining system performance. Table 20 gives the parameter values for the different speed grades. Actual measurement of internal timing is not practical, and often only the sum of component timing is relevant as in the case of input to output. The relationship between input and output timing is arbitrary, and only the total determines performance.

Timing components of internal functions may be determined by the measurement of differences at the pins of the package. A synchronous logic function which involves a clock to block-output and a block-input to clock setup is capable of higher-speed operation than a logic configuration of two synchronous blocks with an extra combinatorial block level between them. System clock rates to 60% of the toggle frequency are practical for logic in which an extra combinatorial level is located between synchronized blocks. This allows implementation of functions of up to 25 variables. The use of the wired-AND is also available for wide, high-speed functions.

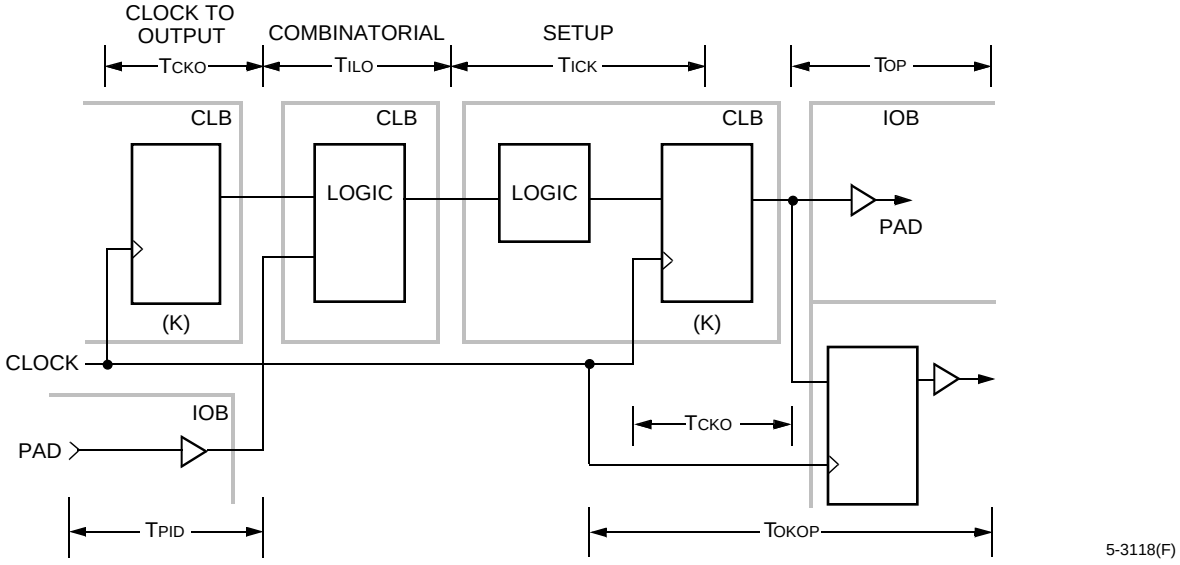


Figure 27. Examples of Primary Block Speed Factors

Performance (continued)

Logic Block Performance

Logic block performance is expressed as the propagation time from the interconnect point at the input of the combinatorial logic to the output of the block in the interconnect area. Combinatorial performance is independent of the specific logic function because of the table look-up based implementation. Timing is different when the combinatorial logic is used in conjunction with the storage element. For the combinatorial logic function driving the data input of the storage element, the critical timing is data setup relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing of signals produced by storage elements. Loading of a logic block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the logic block is a function of supply voltage and temperature (see Figures 28 and 29).

Interconnect Performance

Interconnect performance depends on the routing resource used to implement the signal path. As discussed earlier, direct interconnect from block to block provides a fast path for a signal. The single metal segment used for long lines exhibits low resistance from end to end, but relatively high capacitance. Signals driven through a programmable switch will have the additional impedance of the switch added to their normal drive impedance.

General-purpose interconnect performance depends on the number of switches and segments used, the presence of the bidirectional repowering buffers, and the overall loading on the signal path at all points along the path. In calculating the worst-case timing for a general interconnect path, the timing calculator portion of the *ORCA* Foundry Development System accounts for all of these elements.

As an approximation, interconnect timing is proportional to the summation of totals of local metal segments beyond each programmable switch. In effect, the time is a sum of R-C time each approximated by an R times the total C it drives. The R of the switch and the C of the interconnect are functions of the particular device performance grade.

For a string of three local interconnects, the approximate time at the first segment after the first switch resistance would be three units—an additional two units after the next switch plus an additional unit after the last switch in the chain. The interconnect R-C chain terminates at each repowering buffer. The capacitance of the actual block inputs is not significant; the capacitance is in the interconnect metal and switches. Figure 30 illustrates this.

Performance (continued)

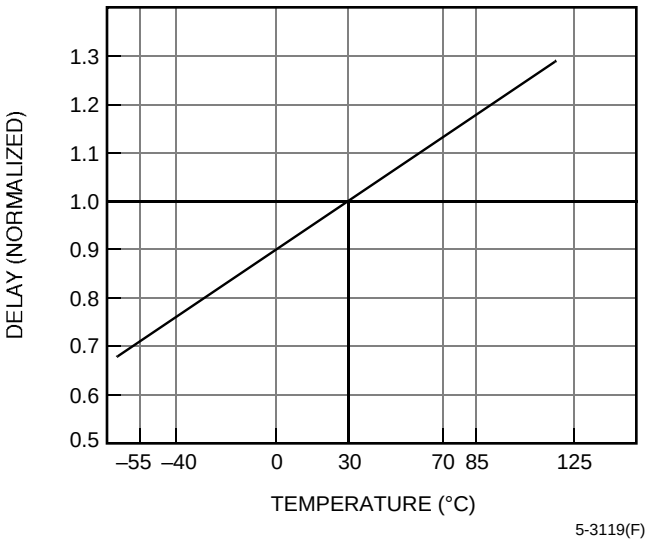


Figure 28. Change in Speed Performance

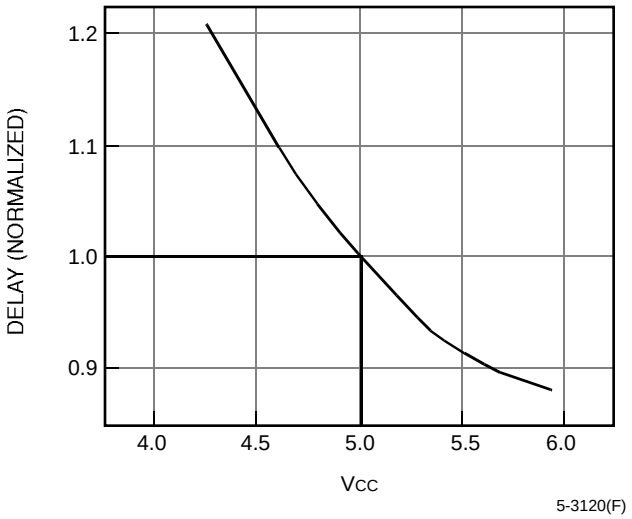


Figure 29. Speed Performance of a CMOS Device

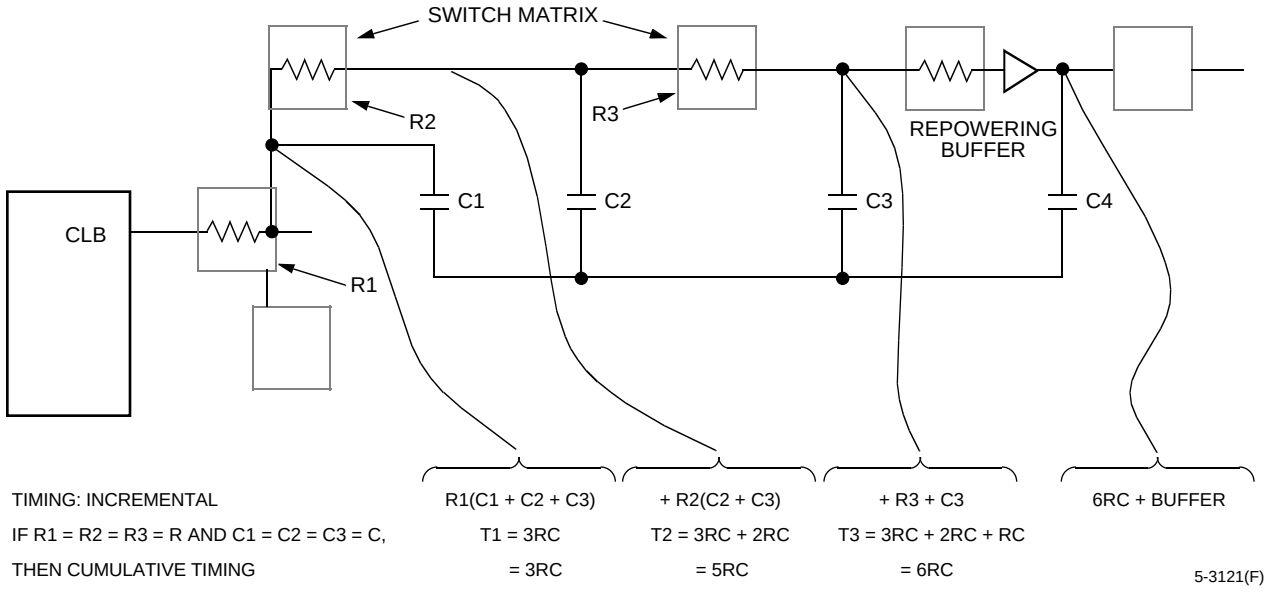


Figure 30. Interconnection Timing Example

Power

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated VCC and ground ring surrounding the logic array provides power to the I/O drivers (see Figure 31 below). An independent matrix of VCC and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, provided that the external package power pins are all connected and appropriately decoupled. Typically, a 0.1 µF capacitor connected near the VCC and ground pins of the package will provide adequate decoupling.

Output buffers which drive the specified 4 mA loads under worst-case conditions may drive 25 to 30 times this amount under best-case process conditions. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The IOB output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical.

Slew-limited outputs maintain their dc drive capability but generate less external reflections and internal noise. More than 32 fast outputs should not be switching in the same direction simultaneously.

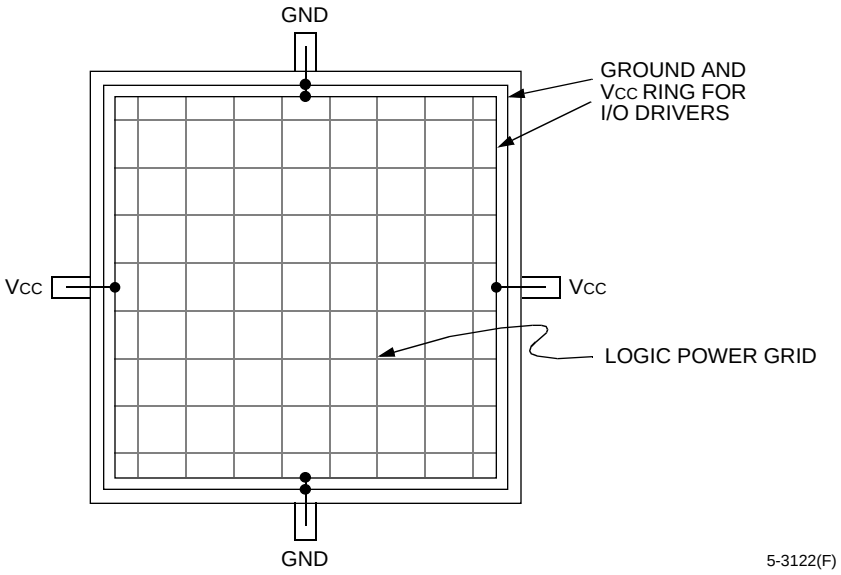


Figure 31. FPGA Power Distribution

Power (continued)

Power Dissipation

The FPGA exhibits the low power consumption characteristic of CMOS ICs. The configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells that hold the configuration data is very low and may be maintained in a powerdown mode.

Typically, most of the power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 µW/pF/MHz per output. Another component of I/O power is the dc loading on each output pin by devices driven by the FPGA.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an FPGA, the fraction of nodes changing on a given clock is typically low (10% to 20%). For example, in a large binary counter, the average clock cycle produces changes equal to one CLB output at the clock frequency. Typical global clock buffer power is between 1.7 mW/MHz for the ATT3020 and 3.5 mW/MHz for the ATT3090. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each configurable logic block output requires about 0.22 mW/MHz of its output frequency:

Total Power = V_{CC} + I_{CCO} + External (dc + Capacitive) + Internal (CLB + IOB + Long Line + Pull-up)

Because the control storage of the FPGA is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The FPGA has built-in powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Powerdown data retention is possible with a simple battery backup circuit, because the power requirement is extremely low. For retention at 2.4 V, the required current is typically on the order of 50 nA.

To force the FPGA into the powerdown state, the user must pull the $\overline{\text{PWRDWN}}$ pin low and continue to supply a retention voltage to the V_{CC} pins of the package. When normal power is restored, V_{CC} is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a high. The FPGA resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal I/O and logic block storage elements will be reset, the outputs will become enabled, and the DONE/$\overline{\text{PROG}}$ pin will be released. No configuration programming is involved.

When the power supply is removed from a CMOS device, it is possible to supply some power from an input signal. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an I/O will cause the positive protection diode to conduct and drive the power pin. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

Pin Information

Table 4. Permanently Dedicated Pins

Symbol	Name/Description
V_{CC}	Two to eight (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.
GND	Two to eight (depending on package type) connections to ground. All must be connected.
$\overline{PWRDWN}$	A low on this CMOS compatible input stops all internal activity to minimize V_{CC} power, and puts all output buffers in a high-impedance state; configuration is retained. When the $\overline{PWRDWN}$ pin returns high, the device returns to operation with the same sequence of buffer enable and DONE/$\overline{PROG}$ as at the completion of configuration. All internal storage elements are reset. If not used, $\overline{PWRDWN}$ must be tied to V_{CC}.
$\overline{RESET}$	This is an active-low input which has three functions: ■ Prior to the start of configuration, a low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{RESET}$ are complete, the levels of the M lines are sampled and configuration begins. ■ If $\overline{RESET}$ is asserted during a configuration, the FPGA is reinitialized and will restart the configuration at the termination of $\overline{RESET}$. ■ If $\overline{RESET}$ is asserted after configuration is complete, it will provide an asynchronous reset of all IOB and CLB storage elements of the FPGA.
CCLK	**Configuration Clock**. During configuration, this is an output of an FPGA in master mode or peripheral mode. FPGAs in slave mode use it as a clock input. During a readback operation, it is a clock input for the configuration data being filtered out.
DONE/ $\overline{PROG}$	**DONE Output**. Configurable as open drain with or without an internal pull-up resistor. At the completion of configuration, the circuitry of the FPGA becomes active in a synchronous order, and DONE may be programmed to occur one cycle before or after that occurs. Once configuration is done, a high-to-low transition of this pin will cause an initialization of the FPGA and start a reconfiguration.
M0/RTRIG	**Mode 0**. This input, M1, and M2 are sampled before the start of configuration to establish the configuration mode to be used. After configuration is complete, a low-to-high transition acts as a read trigger to initiate a readback of configuration and storage-element data clocked by CCLK.
M1/$\overline{RDATA}$	**Mode 1**. This input, M0, and M2 are sampled before the start of configuration to establish the configuration mode to be used. After configuration is complete, this pin is the active-low output of the readback data.

Pin Information (continued)

Table 5. I/O Pins with Special Functions

Symbol	Name/Description
M2	**Mode 2**. This input has a passive pull-up during configuration. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin becomes a user-programmable I/O pin.
HDC	**High During Configuration**. HDC is held at a high level by the FPGA until after configuration. It is available as a control output indicating that configuration is not yet completed. After configuration, this pin is a user I/O pin.
$\overline{\text{LDC}}$	**Low During Configuration**. This active-low signal is held at a low level by the FPGA until after configuration. It is available as a control output indicating that configuration is not yet completed. It is particularly useful in master mode as a low enable for an EPROM. After configuration, this pin is a user I/O pin. If used as a low EPROM enable, it must be programmed as a high after configuration.
$\overline{\text{INIT}}$	This is an active-low, open-drain output which is held low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired-AND of several slave mode devices, a hold-off signal for a master mode device. After configuration, this pin becomes a user-programmable I/O pin.
BCLKIN	This is a direct CMOS level input to the alternate clock buffer (auxiliary buffer) in the lower right corner.
XTL1	This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.
XTL2	This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the *ORCA* Foundry bit stream generation program.
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$, CS2, $\overline{\text{WS}}$	These four inputs represent a set of signals, three active-low and one active-high, which are used in the peripheral mode to control configuration data entry. The assertion of all four generates a write to the internal data buffer. The removal of any assertion clocks in the D[7:0] data present. In the master parallel mode, $\overline{\text{WS}}$ and CS2 are the A0 and A1 outputs. After configuration, the pins are user-programmable I/O pins.

Pin Information (continued)

Table 5. I/O Pins with Special Functions (continued)

Symbol	Name/Description
$\overline{\text{RCLK}}$	During master parallel mode configuration, $\overline{\text{RCLK}}$ represents a read of an external dynamic memory device (normally not used).
RDY/$\overline{\text{BUSY}}$	During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmed I/O pin.
D[7:0]	This set of eight pins represents the parallel configuration byte for the parallel master and peripheral modes. After configuration is complete, they are user-programmed I/O pins.
A[15:0]	This set of 16 pins presents an address output for a configuration EPROM during master parallel mode. After configuration is complete, they are user-programmed I/O pins.
DIN	This user I/O pin is used as serial data input during slave or master serial configuration. This pin is data zero input in master or peripheral configuration mode.
DOUT	This user I/O pin is used during configuration to output serial configuration data for daisy-chained slaves' data in.
TCLKIN	This is a direct CMOS level input to the global clock buffer.
I/O	**Input/Output (Unrestricted)**. May be programmed by the user to be input and/or output pin following configuration. Some of these pins present a high-impedance pull-up (see next page) or perform other functions before configuration is complete (see above).

Pin Information (continued)

Table 6A. ATT3000 Family Configuration (44, 68, and 84 PLCC; 100 QFP; and 100 TQFP)

Configuration Mode (M2:M1:M0)					44 PLCC*	68 PLCC	84 PLCC†	100 QFP	100 TQFP	User Operation
Slave (1:1:1)	Master-Serial (0:0:0)	Peripheral (1:0:1)	Master-High (1:1:0)	Master-Low (1:0:0)						
$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	7	10	12	29	26	$\overline{\text{PWRDWN}}$
VCC	VCC	VCC	VCC	VCC	12	18	22	41	38	VCC
M1 (High)	M1 (Low)	M1 (Low)	M1 (High)	M1 (Low)	16	25	31	52	49	$\overline{\text{RDATA}}$
M0 (High)	M0 (Low)	M0 (Low)	M0 (High)	M0 (Low)	17	26	32	54	51	RTRIG
M2 (High)	M2 (Low)	M2 (High)	M2 (High)	M2 (Low)	18	27	33	56	53	I/O
HDC (High)	HDC (High)	HDC (High)	HDC (High)	HDC (High)	19	28	34	57	54	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	20	30	36	59	56	I/O
INIT‡	INIT‡	INIT‡	INIT‡	INIT‡	22	34	42	65	62	I/O
GND	GND	GND	GND	GND	23	35	43	66	63	GND
					26	43	53	76	73	XTL2–I/O
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	27	44	54	78	75	$\overline{\text{RESET}}$
DONE	DONE	DONE	DONE	DONE	28	45	55	80	77	$\overline{\text{PROG}}$
		D7	D7	D7	—	46	56	81	78	I/O
					30	47	57	82	79	XTL1–I/O
		D6	D6	D6	—	48	58	83	80	I/O
		D5	D5	D5	—	49	60	87	84	I/O
		$\overline{\text{CS0}}$	—	—	—	50	61	88	85	I/O
		D4	D4	D4	—	51	62	89	86	I/O
VCC	VCC	VCC	VCC	VCC	34	52	64	91	88	VCC
		D3	D3	D3	—	53	65	92	89	I/O
		$\overline{\text{CS1}}$	—	—	—	54	66	93	90	I/O
		D2	D2	D2	—	55	67	94	91	I/O
		D1	D1	D1	—	56	70	98	95	I/O
		RDY/$\overline{\text{BUSY}}$	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$	—	57	71	99	96	I/O
DIN	DIN	D0	D0	D0	38	58	72	100	97	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	39	59	73	1	98	I/O
CCLK	CCLK	CCLK	CCLK	CCLK	40	60	74	2	99	CCLK
		$\overline{\text{WS}}$	A0	A0	—	61	75	5	2	I/O
		CS2	A1	A1	—	62	76	6	3	I/O
			A2	A2	—	63	77	8	5	I/O
			A3	A3	—	64	78	9	6	I/O
			A15	A15	—	65	81	12	9	I/O
			A4	A4	—	66	82	13	10	I/O
			A14	A14	—	67	83	14	11	I/O
			A5	A5	—	68	84	15	12	I/O
GND	GND	GND	GND	GND	1	1	1	16	13	GND
			A13	A13	—	2	2	17	14	I/O
			A6	A6	—	3	3	18	15	I/O
			A12	A12	—	4	4	19	16	I/O
			A7	A7	—	5	5	20	17	I/O
			A11	A11	—	6	8	23	20	I/O
			A8	A8	—	7	9	24	21	I/O
			A10	A10	—	8	10	25	22	I/O
			A9	A9	—	9	11	26	23	I/O

Represents a 50 kΩ to 100 kΩ pull-up.

* Peripheral mode and master parallel mode are not supported in the 44-pin PLCC package; see Table 7.

† Pin assignments for the ATT3064/ATT3090 differ from those shown; see page 42.

‡ $\overline{\text{INIT}}$ is an open-drain output during configuration.

Pin Information (continued)

Table 6B. ATT3000 Family Configuration (132 PPGA, 144 TQFP, 160 QFP, 175 PPGA, 208 SQFP)

Configuration Mode (M2:M1:M0)					132 PPGA	144 TQFP	160 QFP	175 PPGA	208 SQFP	User Operation
Slave (1:1:1)	Master-Serial (0:0:0)	Peripheral (1:0:1)	Master-High (1:1:0)	Master-Low (1:0:0)						
$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	A1	1	159	B2	3	$\overline{\text{PWRDWN}}$
VCC	VCC	VCC	VCC	VCC	C8	19	20	D9	26	VCC
M1 (High)	M1 (Low)	M1 (Low)	M1 (High)	M1 (Low)	B13	36	40	B14	48	$\overline{\text{RDATA}}$
M0 (High)	M0 (Low)	M0 (Low)	M0 (High)	M0 (Low)	A14	38	42	B15	50	RTRIG
M2 (High)	M2 (Low)	M2 (High)	M2 (High)	M2 (Low)	C13	40	44	C15	56	I/O
HDC (High)	HDC (High)	HDC (High)	HDC (High)	HDC (High)	B14	41	45	E14	57	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	D14	45	49	D16	61	I/O
INIT*	INIT*	INIT*	INIT*	INIT*	G14	53	59	H15	77	I/O
GND	GND	GND	GND	GND	H12	55	19	J14	25	GND
					M13	69	76	P15	100	XTL2–I/O
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	P14	71	78	R15	102	$\overline{\text{RESET}}$
DONE	DONE	DONE	DONE	DONE	N13	73	80	R14	107	$\overline{\text{PROG}}$
		D7	D7	D7	M12	74	81	N13	109	I/O
					P13	75	82	T14	110	XTL1–I/O
		D6	D6	D6	N11	78	86	P12	115	I/O
		D5	D5	D5	M9	84	92	T11	122	I/O
		$\overline{\text{CS0}}$	—	—	N9	85	93	R10	123	I/O
		D4	D4	D4	N8	88	98	R9	128	I/O
VCC	VCC	VCC	VCC	VCC	M8	90	100	N9	130	VCC
		D3	D3	D3	N7	92	102	P8	132	I/O
		$\overline{\text{CS1}}$	—	—	P6	93	103	R8	133	I/O
		D2	D2	D2	M6	96	108	R7	138	I/O
		D1	D1	D1	M5	102	114	R5	145	I/O
		RDY/$\overline{\text{BUSY}}$	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$	N4	103	115	P5	146	I/O
DIN	DIN	D0	D0	D0	N2	106	119	R3	151	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	M3	107	120	N4	152	I/O
CCLK	CCLK	CCLK	CCLK	CCLK	P1	108	121	R2	153	CCLK
		$\overline{\text{WS}}$	A0	A0	M2	111	124	P2	161	I/O
		CS2	A1	A1	N1	112	125	M3	162	I/O
			A2	A2	L2	115	128	P1	165	I/O
			A3	A3	L1	116	129	N1	166	I/O
			A15	A15	K1	119	132	M1	172	I/O
			A4	A4	J2	120	133	L2	173	I/O
			A14	A14	H1	123	136	K2	178	I/O
			A5	A5	H2	124	137	K1	179	I/O
GND	GND	GND	GND	GND	H3	126	139	J3	182	GND
			A13	A13	G2	128	141	H2	184	I/O
			A6	A6	G1	129	142	H1	185	I/O
			A12	A12	F2	133	147	F2	192	I/O
			A7	A7	E1	134	148	E1	193	I/O
			A11	A11	D1	137	151	D1	199	I/O
			A8	A8	D2	138	152	C1	200	I/O
			A10	A10	B1	141	155	E3	203	I/O
			A9	A9	C2	142	156	C2	204	I/O

☐ Represents a 50 kΩ to 100 kΩ pull-up.

* $\overline{\text{INIT}}$ is an open-drain output during configuration.

Pin Assignments

Table 7. ATT3030 44-Pin PLCC Pinout

Pin No.	Function	Pin No.	Function
1	GND	23	GND
2	I/O	24	I/O
3	I/O	25	I/O
4	I/O	26	XTL2–I/O
5	I/O	27	$\overline{\text{RESET}}$
6	I/O	28	DONE–$\overline{\text{PROG}}$
7	$\overline{\text{PWRDWN}}$	29	I/O
8	TCLKIN–I/O	30	XTL1–BCLKIN–I/O
9	I/O	31	I/O
10	I/O	32	I/O
11	I/O	33	I/O
12	V_{CC}	34	V_{CC}
13	I/O	35	I/O
14	I/O	36	I/O
15	I/O	37	I/O
16	M1–$\overline{\text{RDATA}}$	38	DIN–I/O
17	M0–RTRIG	39	DOUT–I/O
18	M2–I/O	40	CCLK
19	HDC–I/O	41	I/O
20	$\overline{\text{LDC}}$–I/O	42	I/O
21	I/O	43	I/O
22	$\overline{\text{INIT}}$–I/O	44	I/O

Notes:
Peripheral mode and master parallel mode are not supported in the M44 package.

Parallel address and data pins are not assigned.

Pin Assignments (continued)

Table 8. ATT3020, ATT3030, and ATT3042; 68-Pin PLCC and 84-Pin PLCC Pinout*

Pin Numbers		Function	Pin Numbers		Function
68 PLCC	84 PLCC		68 PLCC	84 PLCC	
10	12	$\overline{\text{PWRDWN}}$	38	46	I/O
11	13	TCLKIN–I/O	39	47	I/O
—	14	I/O†	40	48	I/O
12	15	I/O	41	49	I/O
13	16	I/O	—	50	I/O†
—	17	I/O	—	51	I/O†
14	18	I/O	42	52	I/O
15	19	I/O	43	53	XTL2–I/O
16	20	I/O	44	54	$\overline{\text{RESET}}$
17	21	I/O	45	55	DONE–$\overline{\text{PROG}}$
18	22	V_{CC}	46	56	D7–I/O
19	23	I/O	47	57	XTL1–BCLKIN–I/O
—	24	I/O	48	58	D6–I/O
20	25	I/O	—	59	I/O
21	26	I/O	49	60	D5–I/O
22	27	I/O	50	61	$\overline{\text{CS0}}$–I/O
—	28	I/O	51	62	D4–I/O
23	29	I/O	—	63	I/O
24	30	I/O	52	64	V_{CC}
25	31	M1–$\overline{\text{RDATA}}$	53	65	D3–I/O
26	32	M0–RTRIG	54	66	$\overline{\text{CS1}}$–I/O
27	33	M2–I/O	55	67	D2–I/O
28	34	HDC–I/O	—	68	I/O
29	35	I/O	—	69	I/O†
30	36	$\overline{\text{LDC}}$–I/O	56	70	D1–I/O
31	37	I/O	57	71	RDY/$\overline{\text{BUSY}}$–$\overline{\text{RCLK}}$–I/O
—	38	I/O†	58	72	D0–DIN–I/O
32	39	I/O	59	73	DOUT–I/O
33	40	I/O	60	74	CCLK
—	41	I/O†	61	75	A0–$\overline{\text{WS}}$–I/O
34	42	$\overline{\text{INIT}}$–I/O	62	76	A1–CS2–I/O
35	43	GND	63	77	A2–I/O
36	44	I/O	64	78	A3–I/O
37	45	I/O	—	79	I/O†

* Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

† Indicates unconnected package pins for the ATT3020.

Pin Assignments (continued)

Table 8. ATT3020, ATT3030, and ATT3042; 68-Pin PLCC and 84-Pin PLCC Pinout* (continued)

Pin Numbers		Function	Pin Numbers		Function
68 PLCC	84 PLCC		68 PLCC	84 PLCC	
—	80	I/O†	4	4	A12–I/O
65	81	A15–I/O	5	5	A7–I/O
66	82	A4–I/O	—	6	I/O†
67	83	A14–I/O	—	7	I/O†
68	84	A5–I/O	6	8	A11–I/O
1	1	GND	7	9	A8–I/O
2	2	A13–I/O	8	10	A10–I/O
3	3	A6–I/O	9	11	A9–I/O

* Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

† Indicates unconnected package pins for the ATT3020.

Note: Table 8 describes the pin assignments for three different chips in two different packages. The function column lists 84 of the 118 pads on the ATT3042 and 84 of the 98 pads on the ATT3030. Ten pads [indicated with a dagger (†)] do not exist on the ATT3020, which has 74 pads; therefore, the corresponding pins on the 84-pin packages have no connections to an ATT3020.

Pin Assignments (continued)

Table 9. ATT3064 and ATT3090 84-Pin PLCC Pinout

84 PLCC	Function	84 PLCC	Function	84 PLCC	Function
12	$\overline{\text{PWRDWN}}$	40	I/O	68	D2–I/O*
13	TCLKIN–I/O	41	$\overline{\text{INIT}}$–I/O*	69	I/O
14	I/O	42	VCC*	70	D1–I/O
15	I/O	43	GND	71	RDY/$\overline{\text{BUSY}}$–$\overline{\text{RCLK}}$–I/O
16	I/O	44	I/O	72	D0–DIN–I/O
17	I/O	45	I/O	73	DOUT–I/O
18	I/O	46	I/O	74	CCLK
19	I/O	47	I/O	75	A0–$\overline{\text{WS}}$–I/O
20	I/O	48	I/O	76	A1–CS2–I/O
21	GND*	49	I/O	77	A2–I/O
22	VCC	50	I/O	78	A3–I/O
23	I/O	51	I/O	79	I/O*
24	I/O	52	I/O	80	I/O*
25	I/O	53	XTL2–I/O	81	A15–I/O
26	I/O	54	$\overline{\text{RESET}}$	82	A4–I/O
27	I/O	55	DONE–$\overline{\text{PROG}}$	83	A14–I/O
28	I/O	56	D7–I/O	84	A5–I/O
29	I/O	57	XTL1–BCLKIN–I/O	1	GND
30	I/O	58	D6–I/O	2	VCC*
31	M1–$\overline{\text{RDATA}}$	59	I/O	3	A13–I/O*
32	M0–RTRIG	60	D5–I/O	4	A6–I/O*
33	M2–I/O	61	$\overline{\text{CS0}}$–I/O	5	A12–I/O*
34	HDC–I/O	62	D4–I/O	6	A7–I/O*
35	I/O	63	I/O	7	I/O
36	$\overline{\text{LDC}}$–I/O	64	VCC	8	A11–I/O
37	I/O	65	GND*	9	A8–I/O
38	I/O	66	D3–I/O*	10	A10–I/O
39	I/O	67	$\overline{\text{CS1}}$–I/O*	11	A9–I/O

* Different pin definition than ATT3020/ATT3030/ATT3042 PC84 package.

Note: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

Pin Assignments (continued)

Table 10. ATT3020, ATT3030, and ATT3042 100-Pin QFP Pinout

100 QFP	Function	100 QFP	Function	100 QFP	Function
16	GND	50	I/O*	84	I/O*
17	A13–I/O	51	I/O*	85	I/O*
18	A6–I/O	52	M1–$\overline{\text{RDATA}}$	86	I/O
19	A12–I/O	53	GND*	87	D5–I/O
20	A7–I/O	54	M0–RTRIG	88	$\overline{\text{CS0}}$–I/O
21	I/O*	55	VCC*	89	D4–I/O
22	I/O*	56	M2–I/O	90	I/O
23	A11–I/O	57	HDC–I/O	91	VCC
24	A8–I/O	58	I/O	92	D3–I/O
25	A10–I/O	59	$\overline{\text{LDC}}$–I/O	93	$\overline{\text{CS1}}$–I/O
26	A9–I/O	60	I/O*	94	D2–I/O
27*	VCC	61	I/O*	95	I/O
28*	GND	62	I/O	96	I/O*
29	$\overline{\text{PWRDWN}}$	63	I/O	97	I/O*
30	TCLKIN–I/O	64	I/O	98	D1–I/O
31	I/O**	65	$\overline{\text{INIT}}$–I/O	99	$\overline{\text{RCLK}}$–RDY/$\overline{\text{BUSY}}$–I/O
32	I/O*	66	GND	100	D0–DIN–I/O
33	I/O*	67	I/O	1	DOUT–I/O
34	I/O	68	I/O	2	CCLK
35	I/O	69	I/O	3	VCC*
36	I/O	70	I/O	4	GND*
37	I/O	71	I/O	5	A0–$\overline{\text{WS}}$–I/O
38	I/O	72	I/O	6	A1–CS2–I/O
39	I/O	73	I/O	7	I/O**
40	I/O	74	I/O*	8	A2–I/O
41	VCC	75	I/O*	9	A3–I/O
42	I/O	76	XTL2–I/O	10	I/O*
43	I/O	77*	GND	11	I/O*
44	I/O	78	$\overline{\text{RESET}}$	12	A15–I/O
45	I/O	79	VCC*	13	A4–I/O
46	I/O	80	DONE–$\overline{\text{PROG}}$	14	A14–I/O
47	I/O	81	D7–I/O	15	A5–I/O
48	I/O	82	XTL1–BCLKIN–I/O	—	—
49	I/O	83	D6–I/O	—	—

* Only 100 of the 118 pads on the ATT3042 are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the ATT3030, which has 98 pads; therefore, the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the ATT3020, which has 74 pads; therefore, the corresponding pins have no connections.

Note: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

Pin Assignments (continued)

Table 11. ATT3030, ATT3042, and ATT3064 100-Pin TQFP Pinout

100 TQFP	Function	100 TQFP	Function	100 TQFP	Function
13	GND	47	I/O	81	I/O
14	A13–I/O	48	I/O	82	I/O
15	A6–I/O	49	M1–$\overline{\text{RDATA}}$	83	I/O
16	A12–I/O	50	GND	84	D5–I/O
17	A7–I/O	51	M0–RTRIG	85	$\overline{\text{CS0}}$–I/O
18	I/O	52	VCC	86	D4–I/O
19	I/O	53	M2–I/O	87	I/O
20	A11–I/O	54	HDC–I/O	88	VCC
21	A8–I/O	55	I/O	89	D3–I/O
22	A10–I/O	56	$\overline{\text{LDC}}$–I/O	90	$\overline{\text{CS1}}$–I/O
23	A9–I/O	57	I/O	91	D2–I/O
24	VCC	58	I/O	92	I/O
25	GND	59	I/O	93	I/O
26	$\overline{\text{PWRDWN}}$	60	I/O	94	I/O
27	TCLKIN–I/O	61	I/O	95	D1–I/O
28	I/O*	62	$\overline{\text{INIT}}$–I/O	96	$\overline{\text{RCLK}}$–RDY/$\overline{\text{BUSY}}$–I/O
29	I/O	63	GND	97	D0–DIN–I/O
30	I/O	64	I/O	98	DOUT–I/O
31	I/O	65	I/O	99	CCLK
32	I/O	66	I/O	100	VCC
33	I/O	67	I/O	1	GND
34	I/O	68	I/O	2	A0–$\overline{\text{WS}}$–I/O
35	I/O	69	I/O	3	A1–CS2–I/O
36	I/O	70	I/O	4	I/O*
37	I/O	71	I/O	5	A2–I/O
38	VCC	72	I/O	6	A3–I/O
39	I/O	73	XTL2–I/O	7	I/O
40	I/O	74	GND	8	I/O
41	I/O	75	$\overline{\text{RESET}}$	9	A15–I/O
42	I/O	76	VCC	10	A4–I/O
43	I/O	77	DONE–$\overline{\text{PROG}}$	11	A14–I/O
44	I/O	78	D7–I/O	12	A5–I/O
45	I/O	79	XTL1–BCLKIN–I/O	—	—
46	I/O	80	D6–I/O	—	—

* Indicates unconnected package pins for the ATT3030.

Note: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

Pin Assignments (continued)

Table 12. ATT3042 and ATT3064 132-Pin PPGA Pinout

132 PPGA	Function	132 PPGA	Function	132 PPGA	Function
C4	GND	F12	I/O	N6	I/O*
A1	$\overline{\text{PWRDWN}}$	E14	I/O	P5	I/O*
C3	TCLKIN–I/O	F13	I/O	M6	D2–I/O
B2	I/O	F14	I/O	N5	I/O
B3	I/O	G13	I/O	P4	I/O
A2	I/O*	G14	$\overline{\text{INIT}}$–I/O	P3	I/O
B4	I/O	G12	VCC	M5	D1–I/O
C5	I/O	H12	GND	N4	$\overline{\text{RCLK}}$–RDY/$\overline{\text{BUSY}}$–I/O
A3	I/O*	H14	I/O	P2	I/O
A4	I/O	H13	I/O	N3	I/O
B5	I/O	J14	I/O	N2	D0–DIN–I/O
C6	I/O	J13	I/O	M3	DOUT–I/O
A5	I/O	K14	I/O	P1	CCLK
B6	I/O	J12	I/O	M4	VCC
A6	I/O	K13	I/O	L3	GND
B7	I/O	L14	I/O*	M2	A0–$\overline{\text{WS}}$–I/O
C7	GND	L13	I/O	N1	A1–CS2–I/O
C8	VCC	K12	I/O	M1	I/O
A7	I/O	M14	I/O	K3	I/O
B8	I/O	N14	I/O	L2	A2–I/O
A8	I/O	M13	XTL2–I/O	L1	A3–I/O
A9	I/O	L12	GND	K2	I/O
B9	I/O	P14	$\overline{\text{RESET}}$	J3	I/O
C9	I/O	M11	VCC	K1	A15–I/O
A10	I/O	N13	DONE–$\overline{\text{PROG}}$	J2	A4–I/O
B10	I/O	M12	D7–I/O	J1	I/O*
A11	I/O*	P13	XTL1–BCLKIN–I/O	H1	A14–I/O
C10	I/O	N12	I/O	H2	A5–I/O
B11	I/O	P12	I/O	H3	GND
A12	I/O*	N11	D6–I/O	G3	VCC
B12	I/O	M10	I/O	G2	A13–I/O
A13	I/O*	P11	I/O*	G1	A6–I/O
C12	I/O	N10	I/O	F1	I/O*
B13	M1–$\overline{\text{RDATA}}$	P10	I/O	F2	A12–I/O
C11	GND	M9	D5–I/O	E1	A7–I/O
A14	M0–RTRIG	N9	$\overline{\text{CS0}}$–I/O	F3	I/O
D12	VCC	P9	I/O*	E2	I/O
C13	M2–I/O	P8	I/O*	D1	A11–I/O
B14	HDC–I/O	N8	D4–I/O	D2	A8–I/O
C14	I/O	P7	I/O	E3	I/O
E12	I/O	M8	VCC	C1	I/O
D13	I/O	M7	GND	B1	A10–I/O
D14	$\overline{\text{LDC}}$–I/O	N7	D3–I/O	C2	A9–I/O
E13	I/O*	P6	$\overline{\text{CS1}}$–I/O	D3	VCC

* Indicates unconnected package pins for the ATT3030.

Note: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

Pin Assignments (continued)

Table 13. ATT3042 and ATT3064 144-Pin TQFP Pinout

144 TQFP	Function	144 TQFP	Function	144 TQFP	Function	144 TQFP	Function
1	$\overline{\text{PWRDWN}}$	37	GND	73	DONE—$\overline{\text{PROG}}$	109	VCC
2	TCLKIN—I/O	38	M0–RTRIG	74	D7–I/O	110	GND
3	I/O*	39	VCC	75	XTL1–BCLKIN–I/O	111	A0–$\overline{\text{WS}}$–I/O
4	I/O	40	M2–I/O	76	I/O	112	A1–CS2–I/O
5	I/O	41	HDC–I/O	77	I/O	113	I/O
6	I/O*	42	I/O	78	D6–I/O	114	I/O
7	I/O	43	I/O	79	I/O	115	A2–I/O
8	I/O	44	I/O	80	I/O*	116	A3–I/O
9	I/O*	45	$\overline{\text{LDC}}$—I/O	81	I/O	117	I/O
10	I/O	46	I/O*	82	I/O	118	I/O
11	I/O	47	I/O	83	I/O*	119	A15–I/O
12	I/O	48	I/O	84	D5–I/O	120	A4–I/O
13	I/O	49	I/O	85	$\overline{\text{CS0}}$–I/O	121	I/O*
14	I/O	50	I/O*	86	I/O*	122	I/O*
15	I/O*	51	I/O	87	I/O*	123	A14–I/O
16	I/O	52	I/O	88	D4–I/O	124	A5–I/O
17	I/O	53	$\overline{\text{INIT}}$–I/O	89	I/O	125	—
18	GND	54	VCC	90	VCC	126	GND
19	VCC	55	GND	91	GND	127	VCC
20	I/O	56	I/O	92	D3—I/O	128	A13–I/O
21	I/O	57	I/O	93	$\overline{\text{CS1}}$—I/O	129	A6–I/O
22	I/O	58	I/O	94	I/O*	130	I/O*
23	I/O	59	I/O	95	I/O*	131	—
24	I/O	60	I/O	96	D2—I/O	132	I/O*
25	I/O	61	I/O	97	I/O	133	A12–I/O
26	I/O	62	I/O	98	I/O	134	A7–I/O
27	I/O	63	I/O*	99	I/O*	135	I/O
28	I/O*	64	I/O*	100	I/O	136	I/O
29	I/O	65	I/O	101	I/O*	137	A11–I/O
30	I/O	66	I/O	102	D1—I/O	138	A8–I/O
31	I/O*	67	I/O	103	$\overline{\text{RCLK}}$—$\overline{\text{BUSY}}$/RDY—I/O	139	I/O
32	I/O*	68	I/O	104	I/O	140	I/O
33	I/O	69	XTL2—I/O	105	I/O	141	A10–I/O
34	I/O*	70	GND	106	D0—DIN—I/O	142	A9–I/O
35	I/O	71	$\overline{\text{RESET}}$	107	DOUT–I/O	143	VCC
36	M1–$\overline{\text{RDATA}}$	72	VCC	108	CCLK	144	GND

* Indicates unconnected package pins for the ATT3042.

Note: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

Pin Assignments (continued)

Table 14. ATT3064 and ATT3090 160-Pin QFP Pinout

160 QFP	Function	160 QFP	Function	160 QFP	Function	160 QFP	Function
1	I/O*	41	GND	81	D7–I/O	121	CCLK
2	I/O*	42	M0–RTRIG	82	XTL1–BCLKIN–I/O	122	VCC
3	I/O*	43	VCC	83	I/O*	123	GND
4	I/O	44	M2–I/O	84	I/O	124	A0–$\overline{WS}$–I/O
5	I/O	45	HDC–I/O	85	I/O	125	A1–CS2–I/O
6	I/O	46	I/O	86	D6–I/O	126	I/O
7	I/O	47	I/O	87	I/O	127	I/O
8	I/O	48	I/O	88	I/O	128	A2–I/O
9	I/O	49	$\overline{LDC}$–I/O	89	I/O	129	A3–I/O
10	I/O	50	I/O*	90	I/O	130	I/O
11	I/O	51	I/O*	91	I/O	131	I/O
12	I/O	52	I/O	92	D5–I/O	132	A15–I/O
13	I/O	53	I/O	93	$\overline{CS0}$ – I/O	133	A4–I/O
14	I/O	54	I/O	94	I/O*	134	I/O
15	I/O	55	I/O	95	I/O*	135	I/O
16	I/O	56	I/O	96	I/O	136	A14–I/O
17	I/O	57	I/O	97	I/O	137	A5–I/O
18	I/O	58	I/O	98	D4–I/O	138	I/O*
19	GND	59	$\overline{INIT}$–I/O	99	I/O	139	GND
20	VCC	60	VCC	100	VCC	140	VCC
21	I/O*	61	GND	101	GND	141	A13–I/O
22	I/O	62	I/O	102	D3–I/O	142	A6–I/O
23	I/O	63	I/O	103	$\overline{CS1}$–I/O	143	I/O*
24	I/O	64	I/O	104	I/O	144	I/O*
25	I/O	65	I/O	105	I/O	145	I/O
26	I/O	66	I/O	106	I/O*	146	I/O
27	I/O	67	I/O	107	I/O*	147	A12–I/O
28	I/O	68	I/O	108	D2–I/O	148	A7–I/O
29	I/O	69	I/O	109	I/O	149	I/O
30	I/O	70	I/O	110	I/O	150	I/O
31	I/O	71	I/O	111	I/O	151	A11–I/O
32	I/O	72	I/O	112	I/O	152	A8–I/O
33	I/O	73	I/O	113	I/O	153	I/O
34	I/O	74	I/O	114	D1–I/O	154	I/O
35	I/O	75	I/O*	115	$\overline{RCLK}$–$\overline{RDY}$/$\overline{BUSY}$–I/O	155	A10–I/O
36	I/O	76	XTL2–I/O	116	I/O	156	A9–I/O
37	I/O	77	GND	117	I/O	157	VCC
38	I/O*	78	$\overline{RESET}$	118	I/O*	158	GND
39	I/O*	79	VCC	119	D0–DIN–I/O	159	$\overline{PWRDWN}$
40	M1–$\overline{RDATA}$	80	DONE–$\overline{PROG}$	120	DOUT–I/O	160	TCLKIN–I/O

* Indicates unconnected package pins for the ATT3064.

Note: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

Pin Assignments (continued)

Table 15. ATT3000 Family 175-Pin PPGA Pinout

175 PPGA	Function	175 PPGA	Function	175 PPGA	Function	175 PPGA	Function
B2	$\overline{\text{PWRDWN}}$	D13	I/O	R14	DONE–$\overline{\text{PROG}}$	R3	D0–DIN–I/O
D4	TCLKIN–I/O	B14	M1–$\overline{\text{RDATA}}$	N13	D7–I/O	N4	DOUT–I/O
B3	I/O	C14	GND	T14	XTL1–BCLKIN–I/O	R2	CCLK
C4	I/O	B15	M0–RTRIG	P13	I/O	P3	VCC
B4	I/O	D14	VCC	R13	I/O	N3	GND
A4	I/O	C15	M2–I/O	T13	I/O	P2	A0–$\overline{\text{WS}}$–I/O
D5	I/O	E14	HDC–I/O	N12	I/O	M3	A1–CS2–I/O
C5	I/O	B16	I/O	P12	D6–I/O	R1	I/O
B5	I/O	D15	I/O	R12	I/O	N2	I/O
A5	I/O	C16	I/O	T12	I/O	P1	A2–I/O
C6	I/O	D16	$\overline{\text{LDC}}$–I/O	P11	I/O	N1	A3–I/O
D6	I/O	F14	I/O	N11	I/O	L3	I/O
B6	I/O	E15	I/O	R11	I/O	M2	I/O
A6	I/O	E16	I/O	T11	D5–I/O	M1	A15–I/O
B7	I/O	F15	I/O	R10	$\overline{\text{CS0}}$–I/O	L2	A4–I/O
C7	I/O	F16	I/O	P10	I/O	L1	I/O
D7	I/O	G14	I/O	N10	I/O	K3	I/O
A7	I/O	G15	I/O	T10	I/O	K2	A14–I/O
A8	I/O	G16	I/O	T9	I/O	K1	A5–I/O
B8	I/O	H16	I/O	R9	D4–I/O	J1	I/O
C8	I/O	H15	$\overline{\text{INIT}}$–I/O	P9	I/O	J2	I/O
D8	GND	H14	VCC	N9	VCC	J3	GND
D9	VCC	J14	GND	N8	GND	H3	VCC
C9	I/O	J15	I/O	P8	D3–I/O	H2	A13–I/O
B9	I/O	J16	I/O	R8	$\overline{\text{CS1}}$–I/O	H1	A6–I/O
A9	I/O	K16	I/O	T8	I/O	G1	I/O
A10	I/O	K15	I/O	T7	I/O	G2	I/O
D10	I/O	K14	I/O	N7	I/O	G3	I/O
C10	I/O	L16	I/O	P7	I/O	F1	I/O
B10	I/O	L15	I/O	R7	D2–I/O	F2	A12–I/O
A11	I/O	M16	I/O	T6	I/O	E1	A7–I/O
B11	I/O	M15	I/O	R6	I/O	E2	I/O
D11	I/O	L14	I/O	N6	I/O	F3	I/O
C11	I/O	N16	I/O	P6	I/O	D1	A11–I/O
A12	I/O	P16	I/O	T5	I/O	C1	A8–I/O
B12	I/O	N15	I/O	R5	D1–I/O	D2	I/O
C12	I/O	R16	I/O	P5	RDY/$\overline{\text{BUSY}}$–$\overline{\text{RCLK}}$–I/O	B1	I/O
D12	I/O	M14	I/O	N5	I/O	E3	A10–I/O
A13	I/O	P15	XTL2–I/O	T4	I/O	C2	A9–I/O
B13	I/O	N14	GND	R4	I/O	D3	VCC
C13	I/O	R15	$\overline{\text{RESET}}$	P4	I/O	C3	GND
A14	I/O	P14	VCC	—	—	—	—

Note:Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited. Pins A2, A3, A15, A16, T1, T2, T3, T15, and T16 are not connected. Pin A1 does not exist.

Pin Assignments (continued)

Table 16. ATT3000 Family 208-Pin SQFP Pinout

208 SQFP	Function	208 SQFP	Function	208 SQFP	Function	208 SQFP	Function
1	—	53	—	105	—	157	—
2	GND	54	—	106	VCC	158	—
3	$\overline{\text{PWRDWN}}$	55	VCC	107	DONE–$\overline{\text{PROG}}$	159	—
4	TCLKIN–I/O	56	M2–I/O	108	—	160	GND
5	I/O	57	HDC–I/O	109	D7–I/O	161	A0–$\overline{\text{WS}}$–I/O
6	I/O	58	I/O	110	XTL1–BCLKIN–I/O	162	A1–CS2–I/O
7	I/O	59	I/O	111	I/O	163	I/O
8	I/O	60	I/O	112	I/O	164	I/O
9	I/O	61	$\overline{\text{LDC}}$–I/O	113	I/O	165	A2–I/O
10	I/O	62	I/O	114	I/O	166	A3–I/O
11	I/O	63	I/O	115	D6–I/O	167	I/O
12	I/O	64	—	116	I/O	168	I/O
13	I/O	65	—	117	I/O	169	—
14	I/O	66	—	118	I/O	170	—
15	I/O	67	—	119	—	171	—
16	I/O	68	I/O	120	I/O	172	A15–I/O
17	I/O	69	I/O	121	I/O	173	A4–I/O
18	I/O	70	I/O	122	D5–I/O	174	I/O
19	I/O	71	I/O	123	$\overline{\text{CS0}}$–I/O	175	I/O
20	I/O	72	—	124	I/O	176	—
21	I/O	73	—	125	I/O	177	—
22	I/O	74	I/O	126	I/O	178	A14–I/O
23	I/O	75	I/O	127	I/O	179	A5–I/O
24	I/O	76	I/O	128	D4–I/O	180	I/O
25	GND	77	$\overline{\text{INIT}}$–I/O	129	I/O	181	I/O
26	VCC	78	VCC	130	VCC	182	GND
27	I/O	79	GND	131	GND	183	VCC
28	I/O	80	I/O	132	D3–I/O	184	A13–I/O
29	I/O	81	I/O	133	$\overline{\text{CS1}}$–I/O	185	A6–I/O
30	I/O	82	I/O	134	I/O	186	I/O
31	I/O	83	—	135	I/O	187	I/O
32	I/O	84	—	136	I/O	188	—
33	I/O	85	I/O	137	I/O	189	—
34	I/O	86	I/O	138	D2–I/O	190	I/O
35	I/O	87	I/O	139	I/O	191	I/O
36	I/O	88	I/O	140	I/O	192	A12–I/O
37	—	89	I/O	141	I/O	193	A7–I/O
38	I/O	90	—	142	—	194	—
39	I/O	91	—	143	I/O	195	—
40	I/O	92	—	144	I/O	196	—
41	I/O	93	I/O	145	D1–I/O	197	I/O
42	I/O	94	I/O	146	RDY/$\overline{\text{BUSY}}$–$\overline{\text{RCLK}}$–I/O	198	I/O
43	I/O	95	I/O	147	I/O	199	A11–I/O
44	I/O	96	I/O	148	I/O	200	A8–I/O
45	I/O	97	I/O	149	I/O	201	I/O
46	I/O	98	I/O	150	I/O	202	I/O
47	I/O	99	I/O	151	D0–DIN–I/O	203	A10–I/O
48	M1–$\overline{\text{RDATA}}$	100	XTL2–I/O	152	DOUT–I/O	204	A9–I/O
49	GND	101	GND	153	CCLK	205	VCC
50	M0–RTRIG	102	$\overline{\text{RESET}}$	154	VCC	206	—
51	—	103	—	155	—	207	—
52	—	104	—	156	—	208	—

Note: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

Package Thermal Characteristics

When silicon die junction temperature is below the recommended junction temperature of 125 °C, the temperature-activated failure mechanisms are minimized. There are four major factors that affect the thermal resistance value: silicon device size/paddle size, board-mounting configuration (board density, multilayer nature of board), package type and size, and system airflow over the package. The values in the table below reflect the capability of the various package types to dissipate heat at given airflow rates. The numbers represent the delta °C/W between the ambient temperature and the device junction temperature.

To test package thermal characteristics, a single package containing a 0.269 in. sq. test IC of each configuration is mounted at the center of a printed-circuit board (PCB) measuring 8 in. x 13 in. x 0.062 in. The assembled PCB is mounted vertically in the center of the rectangular test section of a wind tunnel. The walls of the wind tunnel simulate adjacent boards in the electronic rack and can be adjusted to study the effects of PCB spacing. Forced air at room temperature is supplied by a pair of push-pull blowers which can be regulated to supply the desired air velocities. The air velocity is measured with a hot-wire anemometer at the center of the channel, 3 in. upstream from the package.

A typical test consists of regulating the wind tunnel blowers to obtain the desired air velocity and applying power to the test IC. The power to the IC is adjusted until the maximum junction temperature (as measured by its diodes) reaches 115 °C to 120 °C. The thermal resistance Θ_{JA} (°C/W) is computed by using the power supplied to the IC, junction temperature, ambient temperature, and air velocity:

$$\Theta_{JA} = \frac{T_J - T_A}{Q_C}$$

where:

T_J = peak temperature on the active surface of the IC

T_A = ambient air temperature

Q_C = IC power

The tests are repeated at several velocities from 0 fpm (feet per minute) to 1000 fpm.

The definition of the junction to case thermal resistance Θ_{JC} is:

$$\Theta_{JC} = \frac{T_J - T_C}{Q_C}$$

where:

T_C = temperature measured to the thermocouple at the top dead center of the package

The actual Θ_{JC} measurement performed at Lucent, Θ_{J-TDC}, uses a different package mounting arrangement than the one defined for Θ_{JC} in MIL-STD-883D and SEMI standards. Please contact Lucent for a diagram.

The maximum power dissipation for a package is calculated from the maximum junction temperature, maximum operating temperature, and the junction to ambient characteristic Θ_{JA}. The maximum power dissipation for commercial grade ICs is calculated as follows: max power (watts) = (125 °C – 70 °C) x ($1/\Theta_{JA}$), where 125 °C is the maximum junction temperature. Table 17 lists the ATT3000 plastic package thermal characteristics.

Package Thermal Characteristics (continued)

Table 17. ATT3000 Plastic Package Thermal Characteristics

Package	Q_{JA} (°C/W)			Q_{JC} (°C/W)	Max Power (70 °C—0 fpm)
	0 fpm	200 fpm	400 fpm		
44-Pin PLCC	49	43	40	—	1.12 W
68-Pin PLCC	43	38	35	11	1.28 W
84-Pin PLCC	40	35	32	9	1.38 W
100-Pin QFP	81	67	64	11	0.68 W
100-Pin TQFP	61	49	46	6	0.90 W
132-Pin PPGA	22	18	16	—	2.50 W
144-Pin TQFP	52	39	36	4	1.06 W
160-Pin QFP	40	36	32	8	1.38 W
175-Pin PPGA	23	20	17	—	2.39 W
208-Pin SQFP	37	33	29	8	1.49 W

Package Coplanarity

The coplanarity of Lucent Technologies postmolded packages is 4 mils. The coplanarity of the SQFP and TQFP packages is 3.15 mils.

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 18 lists eight parasitics associated with the ATT3000 packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

Four inductances in nH are listed: L_W and L_L, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead.

The parasitic values in Table 18 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C1 and C2 capacitors. The PGAs contain power and ground planes that will make the inductance value for power and ground leads the minimum value listed. The PGAs also have a significant range of parasitic values. This is due to the large variation in internal trace lengths and is also due to two signal metal layers that are separated from the ground plane by different distances. The upper signal layer is more inductive but less capacitive than the closer, lower signal layer.

Package Parasitics (continued)

Table 18. Package Parasitics

Package Type	L_W	M_W	R_W	C_1	C_2	C_M	L_L	M_L
44-Pin PLCC	3	1	140	0.5	0.5	0.3	5—6	2—2.5
68-Pin PLCC	3	1	140	0.5	0.5	0.4	6—9	3—4
84-Pin PLCC	3	1	140	1	1	0.5	7—11	3—6
100-Pin QFP	3	1	160	1	1	0.5	7—9	4—5
100-Pin TQFP	3	1	150	0.5	0.5	0.4	4—6	2—3
132-Pin PPGA	3	1	150	1	1	0.25	4—10	0.5—1
144-Pin TQFP	3	1	140	1	1	0.6	4—6	2—2.5
160-Pin QFP	4	1.5	180	1.5	1.5	1	10—13	6—8
175-Pin PPGA	3	1	150	1	1	0.3	5—11	1—1.5
208-Pin SQFP	4	2	200	1	1	1	7—10	4—6

* Leads designated as ground (power) can be connected to the ground plane, reducing the trace inductance to the minimum value listed.

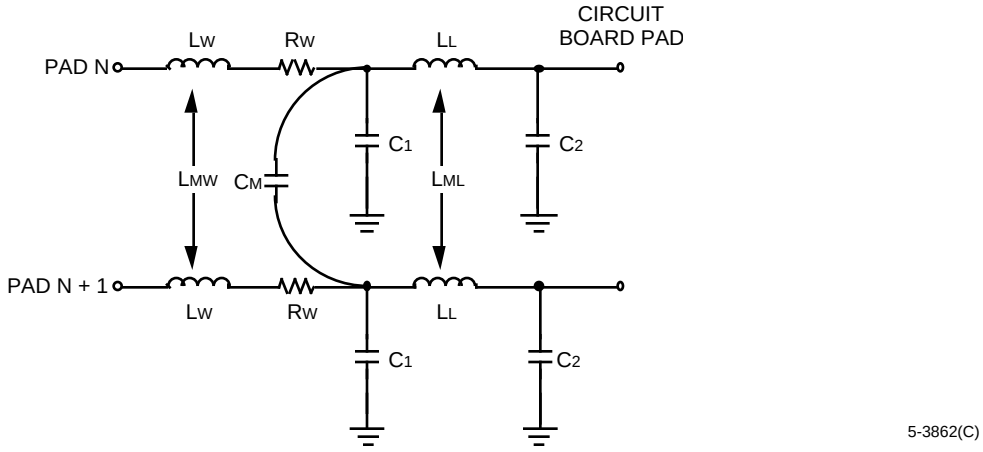


Figure 32. Package Parasitics

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Supply Voltage Relative to GND	V_{CC}	–0.5	7.0	V
Input Voltage Relative to GND	V_{IN}	–0.5	0.5	V
Voltage Applied to 3-state Output	V_{TS}	–0.5	0.5	V
Storage Temperature (ambient)	T_{stg}	–65	150	°C
Maximum Soldering Temperature (10 seconds at 1/16 in.)	T_{SOL}	—	260	°C
Junction Temperature	T_J	—	125	°C

Electrical Characteristics

Table 19. dc Electrical Characteristics Over Operating Conditions

Commercial: V_{CC} = 5.0 V ± 5%; 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{CC} = 5.0 ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Parameter/Conditions	Symbol	-50, -70, -100, and -125		-3, -4, and -5		Unit
		Min	Max	Min	Max	
High-level Input Voltage						
CMOS Level	V_{IHC}	70%	100%	70%	100%	V
TTL Level	V_{IHT}	2.0	V_{CC}	2.0	V_{CC}	V
Low-level Input Voltage						
CMOS Level	V_{ILC}	0	20%	0	20%	V
TTL Level	V_{ILT}	0	0.8	0	0.8	V
Output Voltage						
High						
(I_{OH} = –4 mA)	V_{OH}	3.86	—	—	—	V
(I_{OH} = –8 mA)	V_{OH}	—	—	3.86	—	V
Low						
(I_{OL} = 4 mA)	V_{OL}	—	0.40	—	—	V
(I_{OL} = 8 mA)	V_{OL}	—	—	—	0.40	V
Input Signal Transition Time	T_{IN}	—	250	—	250	ns
Powerdown Supply Current	I_{CCPD}					
ATT3020		—	50	—	50	µA
ATT3030		—	80	—	80	µA
ATT3042		—	120	—	120	µA
ATT3064		—	170	—	170	µA
ATT3090		—	250	—	250	µA
Quiescent FPGA Supply Current (in addition to ICCPD)	I_{CCO}					
CMOS Inputs				—	10	mA
ATT3020		—	500	—	500	µA
ATT3030		—	500	—	500	µA
ATT3042		—	500	—	500	µA
ATT3064		—	500	—	500	µA
ATT3090		—	500	—	500	µA
TTL Inputs		—	10	—	20	mA
Leakage Current	I_{IL}	–10	10	–10	10	µA
Input Capacitance*	C_{IN}					
All Packages Except 175-PGA:						
All Pins Except XTL1/XTL2		—	10	—	10	pF
XTL1 and XTL2		—	15	—	15	pF
175-PGA Package:						
All Pins Except XTL1/XTL2		—	15	—	15	pF
XTL1 and XTL2		—	20	—	20	pF
Pad Pull-up* (when selected) (at V_{IN} = 0 V)	I_{RIN}	0.02	0.17	0.02	0.17	mA
Horizontal Long-line Pull-up (when selected) at Logic LOW	I_{RLL}	0.2	2.5	0.2	2.8	mA

* Sample tested.

Note: With no output current loads, no active input or long-line pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a bit stream generation program tie option.

Electrical Characteristics (continued)

Table 20. CLB Switching Characteristics (-50, -70, -100, and -125)

Commercial: V_{CC} = 5.0 V ± 5%; 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{CC} = 5.0 ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Description	Symbol		-50		-70		-100		-125		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay	1	TILO	—	14.0	—	9.0	—	7.0	—	5.5	ns
Sequential Delay											
Clock K to Outputs x or y	8	TCKO	—	12.0	—	6.0	—	5.0	—	4.5	ns
Clock K to Outputs x or y when Q Returned Through Function Generators F or G to Drives x or y	—	TQLO	—	23.0	—	13.0	—	10.0	—	8.0	ns
Setup Time											
Logic Variables	2	TICK	12.0	—	8.0	—	7.0	—	5.5	—	ns
Data In	4	TDICK	8.0	—	5.0	—	4.0	—	3.0	—	ns
Enable Clock	6	TECCK	10.0	—	7.0	—	5.0	—	4.5	—	ns
Reset Direct Active	—	TRDCK	1.0	—	1.0	—	1.0	—	1.0	—	ns
Hold Time											
Logic Variables	3	TCKI	1.0	—	0	—	0	—	0	—	ns
Data In	5	TCKDI	6.0	—	4.0	—	2.0	—	1.5	—	ns
Enable Clock	7	TCKEC	0	—	0	—	0	—	0	—	ns
Clock											
High Time*	11	TCH	9.0	—	5.0	—	4.0	—	3.0	—	ns
Low Time*	12	TCL	9.0	—	5.0	—	4.0	—	3.0	—	ns
Flip-Flop Toggle Rate*	—	FCLK	50	—	70	—	100	—	125	—	MHz
Reset Direct (rd)											
rd Width	13	TRPW	12.0	—	8.0	—	7.0	—	6.0	—	ns
Delay from rd to Outputs x, y	9	TRIO	—	12.0	—	8.0	—	7.0	—	6.0	ns
Master Reset (MR)											
MR Width	—	TMRW	30	—	25	—	21	—	20	—	ns
Delay from MR to Outputs x, y	—	TMRQ	—	27	—	23	—	19	—	17	ns

* These parameters are for clock pulses within an FPGA device. For externally applied clock, increase values by 20%.

Note: The CLB K to Q output delay (TCKO—#8) of any CLB, plus the shortest possible interconnect delay, is always longer than the data in hold time requirement (TCKDI—#5) of any CLB on the same die.

Electrical Characteristics (continued)

Table 21. CLB Switching Characteristics (-3, -4, and -5)

Commercial: V_{CC} = 5.0 V ± 5%; 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{CC} = 5.0 ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Description	Symbol		-5		-4		-3		Unit
			Min	Max	Min	Max	Min	Max	
Combinatorial Delay	1	TILO	—	4.1	—	3.3	—	2.7	ns
Sequential Delay									
Clock K to Outputs x or y	8	TCKO	—	3.1	—	2.5	—	2.1	ns
Clock K to Outputs x or y when Q Returned Through Function Generators F or G to Drives x or y	—	TQLO	—	6.3	—	5.2	—	4.3	ns
Setup Time									
Logic Variables	2	TICK	3.1	—	2.5	—	2.1	—	ns
Data In	4	TDICK	2.0	—	1.6	—	1.4	—	ns
Enable Clock	6	TECCK	3.8	—	3.2	—	2.7	—	ns
Reset Direct Active	—	TRDCK	1.0	—	1.0	—	1.0	—	ns
Hold Time									
Logic Variables	3	TCKI	0	—	0	—	0	—	ns
Data In	5	TCKDI	1.2	—	1.0	—	0.9	—	ns
Enable Clock	7	TCKEC	1.0	—	0.8	—	0.7	—	ns
Clock									
High Time*	11	TCH	2.4	—	2.0	—	1.6	—	ns
Low Time*	12	TCL	2.4	—	2.0	—	1.6	—	ns
Flip-Flop Toggle Rate*	—	FCLK	190	—	230	—	270	—	MHz
Reset Direct (rd)									
rd Width	13	TRPW	3.8	—	3.2	—	2.7	—	ns
Delay from rd to Outputs x, y	9	TRIO	—	4.4	—	3.7	—	3.1	ns
Master Reset (MR)									
MR Width	—	TMRW	18.0	—	15.0	—	13.0	—	ns
Delay from MR to Outputs x, y	—	TMRQ	—	17.0	—	14.0	—	12.0	ns

* These parameters are for clock pulses within an FPGA device. For externally applied clock, increase values by 20%.

Note: The CLB K to Q output delay (TCKO—#8) of any CLB, plus the shortest possible interconnect delay, is always longer than the data in hold time requirement (TCKDI—#5) of any CLB on the same die.

Electrical Characteristics (continued)

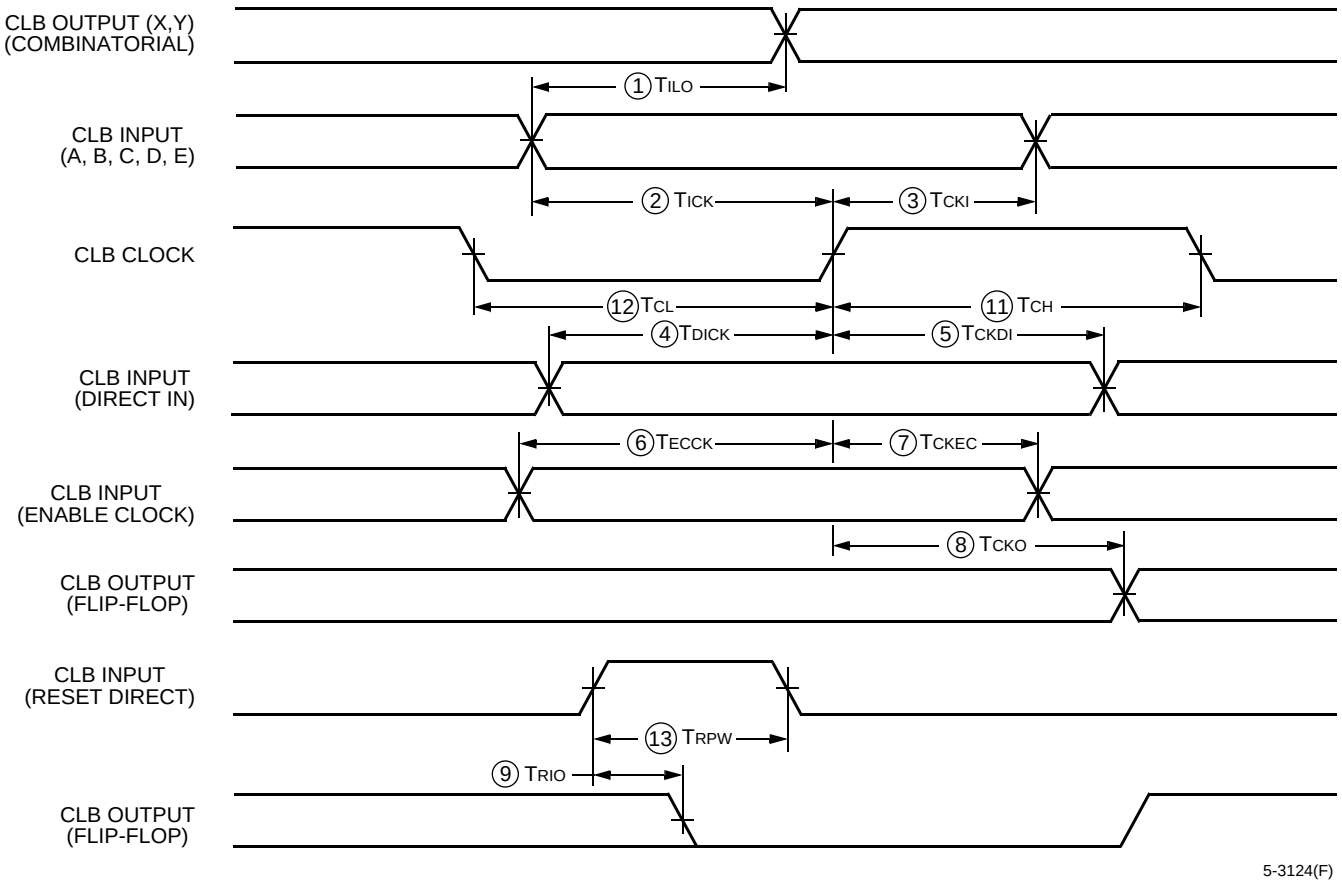


Figure 33. CLB Switching Characteristics

Electrical Characteristics (continued)

Table 22. IOB Switching Characteristics (-50, -70, -100, and -125)

Commercial: V_{CC} = 5.0 V ± 5%; 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{CC} = 5.0 ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Description	Symbol		-50		-70		-100		-125		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Delays											
Pad to Direct In	3	TPID	—	9.0	—	6.0	—	4.0	—	3.0	ns
Pad to Registered In	—	TPTG	—	34.0	—	21.0	—	17.0	—	16.0	ns
Clock to Registered In	4	TIKRI	—	11.0	—	5.5	—	4.0	—	3.0	ns
Setup Time (Input):											
Clock Setup Time	1	TPICK	30.0	—	20.0	—	17.0	—	16.0	—	ns
Output Delays											
Clock to Pad											
Fast	7	TOKPO	—	18.0	—	13.0	—	10.0	—	9.0	ns
Slew-rate Limited	7	TOKPO	—	43.0	—	33.0	—	27.0	—	24.0	ns
Output to Pad											
Fast	10	TOPF	—	15.0	—	9.0	—	6.0	—	5.0	ns
Slew-rate Limited	10	TOPS	—	40.0	—	29.0	—	23.0	—	20.0	ns
3-state to Pad Hi-Z											
Fast	9	TTSHZ	—	10.0	—	8.0	—	8.0	—	7.0	ns
Slew-rate Limited	9	TTSHZ	—	37.0	—	28.0	—	25.0	—	24.0	ns
3-state to Pad Valid											
Fast	8	TTSON	—	20.0	—	14.0	—	12.0	—	11.0	ns
Slew-rate Limited	8	TTSON	—	45.0	—	34.0	—	29.0	—	27.0	ns
Setup and Hold Times (output)											
Clock Setup Time	5	TOCK	15.0	—	10.0	—	9.0	—	8.0	—	ns
Clock Hold Time	6	TOKO	0	—	0	—	0	—	0	—	ns
Clock											
High Time*	11	TCH	9.0	—	5.0	—	4.0	—	3.0	—	ns
Low Time*	12	TCL	9.0	—	5.0	—	4.0	—	3.0	—	ns
Max. Flip-Flop Toggle*	—	FCLK	—	50	—	70	—	100	—	125	MHz
Master Reset Delays											
$\overline{\text{RESET}}$ to:											
Registered In	13	TRRI	—	35	—	25	—	24	—	23	ns
Output Pad (fast)	15	TRPO	—	50	—	35	—	33	—	29	ns
Output Pad (slew-rate limited)	15	TRPO	—	68	—	53	—	45	—	42	ns

* These parameters are for clock pulses within an FPGA device. For externally applied clock, increase values by 20%.

Notes:
Timing is measured at pin threshold with 50 pF external capacitive loads (including test fixture).

Typical fast mode output rise/fall times are 2 ns and will increase approximately 2%/pF of additional load.

Typical slew-rate limited output rise/fall times are approximately 4 times longer.

A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 200 pF per power/ground pin pair. For slew-rate limited outputs, this total is 4 times larger. Exceeding this maximum capacitive load can result in ground bounce of >1.5 V amplitude and <5 ns duration, which may cause problems when the FPGA drives clocks and other asynchronous signals.

Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

Input pad setup time is specified with respect to the internal clock (ik).

To calculate system setup time, subtract clock delay (pad to ik) from the input pad setup time value. Input pad hold time with respect to the internal clock (ik) is negative. This means that pad levels changed immediately before the internal clock edge (ik) will not be recognized.

Electrical Characteristics (continued)

Table 23. IOB Switching Characteristics (-3, -4, and -5)

Commercial: V_{CC} = 5.0 V ± 5%; 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{CC} = 5.0 ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Description	Symbol		-5		-4		-3		Unit
			Min	Max	Min	Max	Min	Max	
Input Delays									
Pad to Direct In	3	T_{PID}	—	2.8	—	2.5	—	2.2	ns
Pad to Registered In	—	T_{PTG}	—	16.0	—	15.0	—	13.0	ns
Clock to Registered In	4	T_{IKRI}	—	2.8	—	2.5	—	2.2	ns
Setup Time (Input):									
Clock Setup Time	1	T_{PICK}	15.0	—	14.0	—	12.0	—	ns
Output Delays									
Clock to Pad									
Fast	7	T_{OKPO}	—	5.5	—	5.0	—	4.4	ns
Slew-rate Limited	7	T_{OKPO}	—	14.0	—	12.0	—	10.0	ns
Output to Pad									
Fast	10	T_{OPF}	—	4.1	—	3.7	—	3.3	ns
Slew-rate Limited	10	T_{OPS}	—	13.0	—	11.0	—	9.0	ns
3-state to Pad Hi-Z									
Fast	9	T_{TSHZ}	—	6.9	—	6.2	—	5.5	ns
Slew-rate Limited	9	T_{TSHZ}	—	21.0	—	19.0	—	17.0	ns
3-state to Pad Valid									
Fast	8	T_{TSON}	—	12.0	—	10.0	—	9.0	ns
Slew-rate Limited	8	T_{TSON}	—	20.0	—	17.0	—	15.0	ns
Setup and Hold Times (output)									
Clock Setup Time	5	T_{OCK}	6.2	—	5.6	—	5.0	—	ns
Clock Hold Time	6	T_{OKO}	0	—	0	—	0	—	ns
Clock									
High Time*	11	T_{CH}	2.4	—	2.0	—	1.6	—	ns
Low Time*	12	T_{CL}	2.4	—	2.0	—	1.6	—	ns
Max. Flip-Flop Toggle*	—	F_{CLK}	190	—	230	—	270	—	MHz
Master Reset Delays									
$\overline{\text{RESET}}$ to:									
Registered In	13	T_{RRI}	—	18	—	15	—	13	ns
Output Pad (fast)	15	T_{RPO}	—	24	—	20	—	17	ns
Output Pad (slew-rate limited)	15	T_{RPO}	—	32	—	27	—	23	ns

* These parameters are for clock pulses within an FPGA device. For externally applied clock, increase values by 20%.

Notes:
Timing is measured at pin threshold with 50 pF external capacitive loads (including test fixture).

Typical fast mode output rise/fall times are 2 ns and will increase approximately 2%/pF of additional load.

Typical slew-rate limited output rise/fall times are approximately 4 times longer.

A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 200 pF per power/ground pin pair. For slew-rate limited outputs, this total is 4 times larger. Exceeding this maximum capacitive load can result in ground bounce of >1.5 V amplitude and <5 ns duration, which may cause problems when the FPGA drives clocks and other asynchronous signals.

Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

Input pad setup time is specified with respect to the internal clock (ik).

To calculate system setup time, subtract clock delay (pad to ik) from the input pad setup time value. Input pad hold time with respect to the internal clock (ik) is negative. This means that pad levels changed immediately before the internal clock edge (ik) will not be recognized.

Electrical Characteristics (continued)

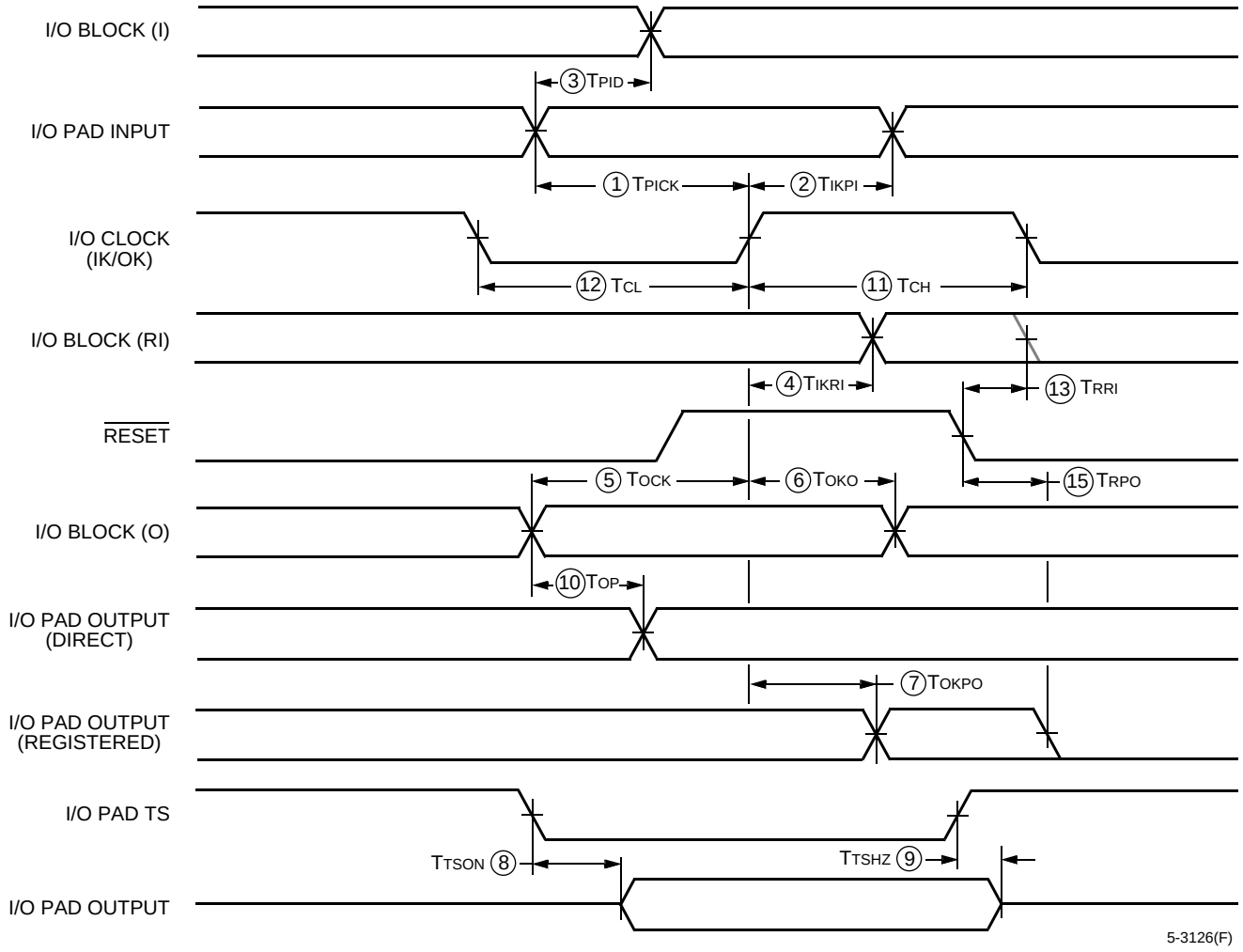


Figure 34. IOB Switching Characteristics

Electrical Characteristics (continued)

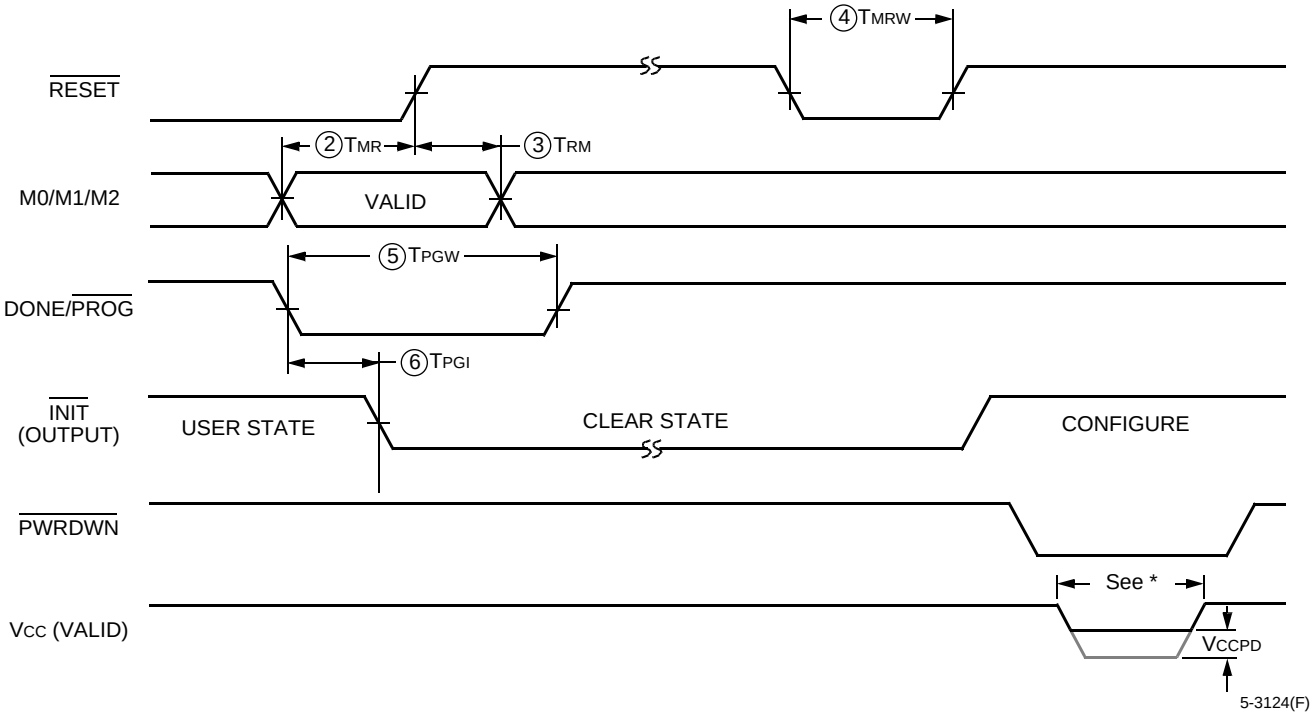
Table 24. Buffer (Internal) Switching Characteristics

Commercial: V_{CC} = 5.0 V ± 5%; 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{CC} = 5.0 ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Description	Symbol	-50	-70	-100	-125	-5	-4	-3	Unit
		Max	Max	Max	Max	Max	Max	Max	
Global and Alternate Clock Distribution*:									
Either Normal IOB Input Pad to Clock Buffer Input or	T_{PID}	10.0	8.0	7.5	7.0	6.8	6.5	5.6	ns
Fast (CMOS only) Input Pad to Clock Buffer Input	T_{PIDC}	8.0	6.5	6.0	5.7	5.4	5.1	4.3	ns
TBUF Driving a Horizontal Long Line (LL)*:									
I to LL While T Is Low (buffer active)	T_{IO}	8.0	5.0	4.7	4.5	4.1	3.7	3.1	ns
T↓ to LL Active and Valid with Single Pull-up Resistor	T_{ON}	12.0	11.0	10.0	9.0	5.6	5.0	4.2	ns
T↓ to LL Active and Valid with Pair of Pull-up Resistors	T_{ON}	14.0	12.0	11.0	10.0	7.1	6.5	5.7	ns
T↑ to LL High with Single Pull-up Resistor	T_{PUS}	42.0	24.0	22.0	17.0	15.6	13.5	11.4	ns
T↑ to LL High with Pair of Pull-up Resistors	T_{PUF}	22.0	17.0	15.0	12.0	12.0	10.5	8.8	ns
Bidirectional Buffer Delay	T_{BIDI}	6.0	2.0	1.8	1.7	1.4	1.2	1.0	ns

* Timing is based on the ATT3042; for other devices, see timing calculator in *ORCA* Foundry.

Electrical Characteristics (continued)



* At powerup, VCC must rise from 2 V to VCC minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET low until VCC has reached 4 V. A very long VCC rise time of >100 ms or a nonmonotonically rising VCC may require a >1 µs high level on RESET, followed by a >6 µs low level on RESET and DONE/PROG after VCC has reached 4 V.

Figure 35. General FPGA Switching Characteristics

Testing of the switching characteristics is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Actual worst-case timing is provided by the timing calculator or simulation.

Table 25. General FPGA Switching Characteristics

Signal	Description	Symbol	Min	Max	Unit
RESET*	M0, M1, and M2 Setup Time M0, M1, and M2 Hold Time RESET Width (LOW) Required for Abort	TMR (2) TRM (3) TMRW (4)	1 4.5 6	— — —	µs µs µs
DONE/PROG	Width Low Required for Reconfiguration INIT Response After DONE/PROG is Pulled Low	TPGW (5) TPGI (6)	6 —	— 7	µs µs
VCC†	Powerdown VCC (commercial/industrial)	VCCPD	2.3	—	V

* RESET timing relative to valid mode lines (M0, M1, M2) is relevant when RESET is used to delay configuration.
† PWRDWN transitions must occur while VCC > 4 V.

Electrical Characteristics (continued)

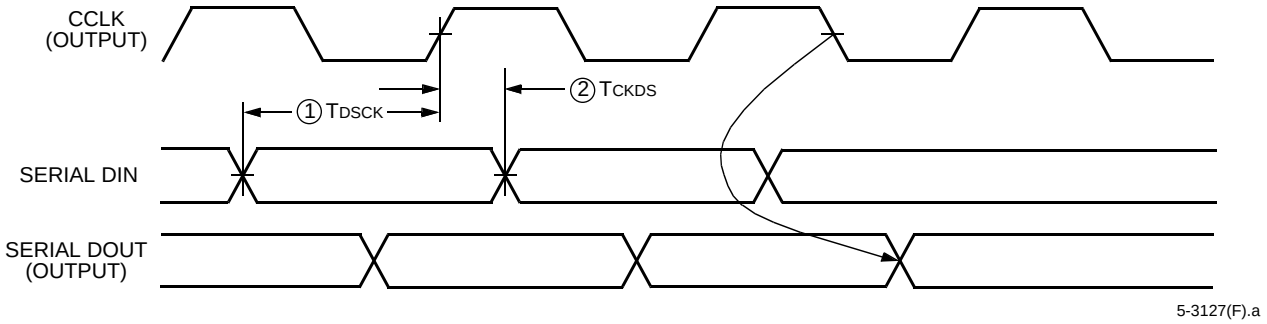


Figure 36. Master Serial Mode Switching Characteristics

Table 26. Master Serial Mode Switching Characteristics

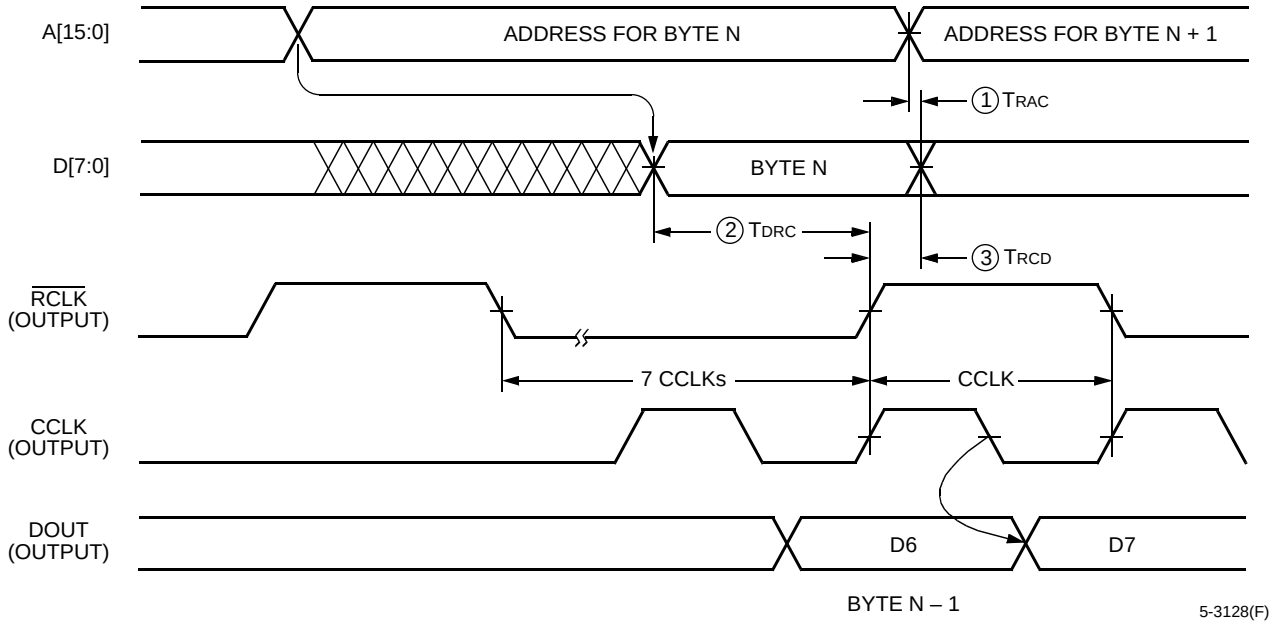
Signal	Description	Symbol		Min	Max	Unit
CCLK	Data-in Setup	1	T_{DSCK}	60	—	ns
	Data-in Hold	2	T_{CKDS}	0	—	ns

Notes:
At powerup, V_{CC} must rise from 2.0 V to V_{CC} minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{\text{RESET}}$ low until V_{CC} has reached 4.0 V. A very long V_{CC} rise time of >100 ms, or a nonmonotonically rising V_{CC} may require a >1 µs high level on $\overline{\text{RESET}}$, followed by >6 µs low level on $\overline{\text{RESET}}$ and D/$\overline{\text{P}}$ after V_{CC} has reached 4.0 V.

Configuration can be controlled by holding $\overline{\text{RESET}}$ low with or until after the $\overline{\text{INIT}}$ of all daisy-chain slave mode devices is high.

Master serial mode timing is based on slave mode testing.

Electrical Characteristics (continued)



Note: The EPROM requirements in this timing diagram are extremely relaxed; EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

Figure 37. Master Parallel Mode Switching Characteristics

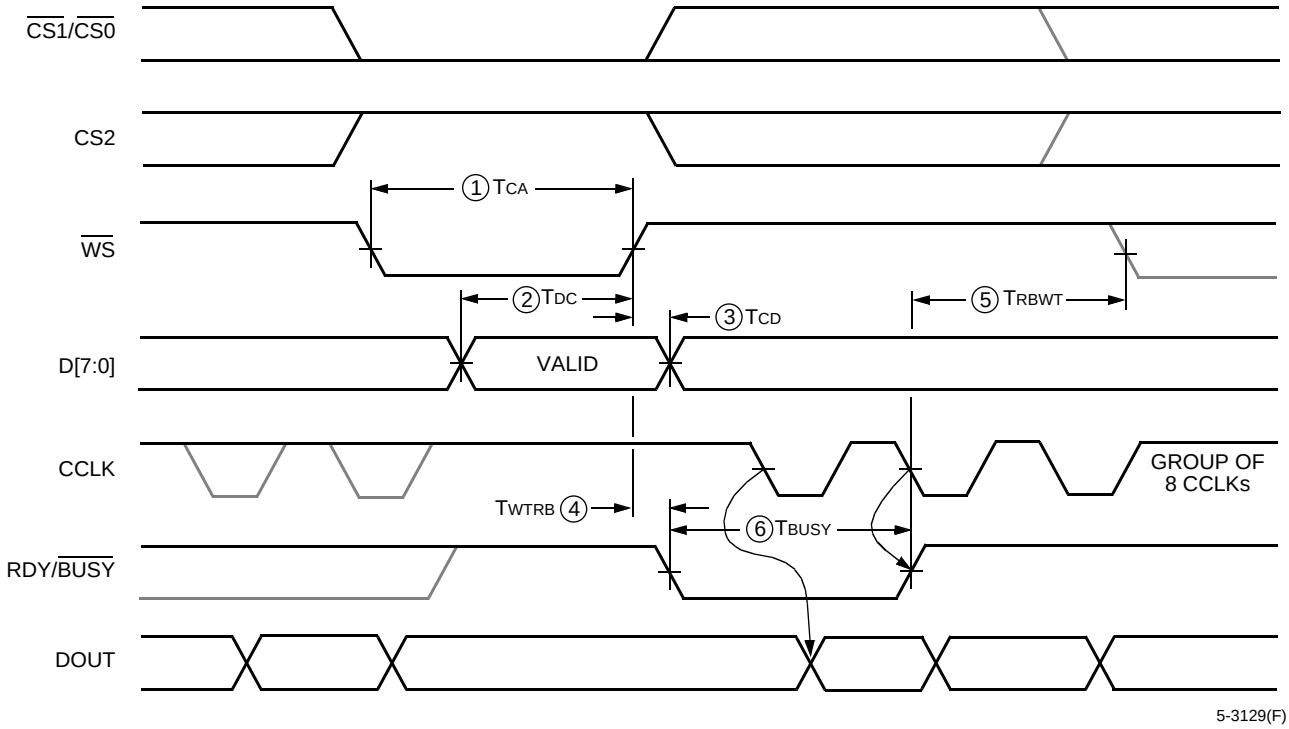
Table 27. Master Parallel Mode Switching Characteristics

Signal	Description	Symbol		Min	Max	Unit
RCLK	To Address Valid	1	T_{RAC}	0	200	ns
	To Data Setup	2	T_{DRC}	60	—	ns
	To Data Hold	3	T_{RCD}	0	—	ns
	RCLK High	—	T_{RCH}	600	—	ns
	RCLK Low	—	T_{RCL}	4.0	—	µs

Notes:
At powerup, V_{CC} must rise from 2.0 V to V_{CC} minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{RESET}$ low until V_{CC} has reached 4.0 V. A very long V_{CC} rise time of >100 ms, or a nonmonotonically rising V_{CC} may require a >1 µs high level on $\overline{RESET}$, followed by >6 µs low level on $\overline{RESET}$ and D/$\overline{P}$ after V_{CC} has reached 4.0 V.

Configuration can be controlled by holding $\overline{RESET}$ low with or until after the $\overline{INIT}$ of all daisy-chain slave mode devices is high.

Electrical Characteristics (continued)



Note: The requirements in this timing diagram are extremely relaxed; data need not be held beyond the rising edge of WS. BUSY will go active within 60 ns after the end of WS. BUSY will stay active for several microseconds. WS may be asserted immediately after the end of BUSY.

Figure 38. Peripheral Mode Switching Characteristics

Table 28. Peripheral Mode Switching Characteristics

Signal	Description	Symbol		Min	Max	Unit
Write Signal	Effective Write Time Required (Assertion of CS0, CS1, CS2, WS)	1	TCA	100	—	ns
D[7:0]	DIN Setup Time Required	2	TDC	60	—	ns
	DIN Hold TIme Required	3	TCD	0	—	ns
RDY/BUSY	RDY/BUSY Delay after End of WS	4	TWTRB	—	60	ns
	Earliest Next WS after End of BUSY	5	TRBWT	0	—	ns
	BUSY Low Time Generated	6	TBUSY	2.5	9	CCLK Periods

Notes:

At powerup, VCC must rise from 2.0 V to VCC minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET low until VCC has reached 4.0 V. A very long VCC rise time of >100 ms, or a nonmonotonically rising VCC may require a >1 µs high level on RESET, followed by >6 µs low level on RESET and D/P after VCC has reached 4.0 V.

Configuration must be delayed until the INIT of all FPGAs is high.

Time from end of WS to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.

CCLK and DOUT timing is tested in slave mode.

TBUSY indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest TBUSY occurs when a byte is loaded into an empty parallel-to-serial converter. The longest TBUSY occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

Electrical Characteristics (continued)

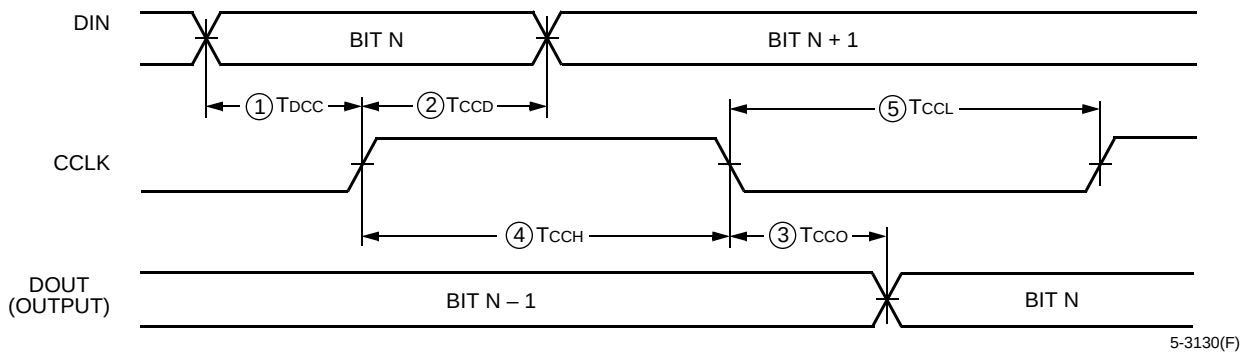


Figure 39. Slave Mode Switching Characteristics

Table 29. Slave Mode Switching Characteristics

Commercial: V_{CC} = 5.0 V ± 5%; 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{CC} = 5.0 ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Signal	Description	Symbol		Min	Max	Unit
CCLK	To DOUT	3	T_{CCO}	—	100	ns
	DIN Setup	1	T_{DCC}	60	—	ns
	DIN Hold	2	T_{CCD}	0	—	ns
	HIGH Time	4	T_{CCH}	0.05	—	µs
	LOW Time	5	T_{CCL}	0.05	5.0	µs
	Frequency	—	F_{CC}	—	10.0	MHz

Notes:
The maximum limit of CCLK LOW time is caused by dynamic circuitry inside the FPGA device.

Configuration must be delayed until the $\overline{INIT}$ of all FPGAs is high.

At powerup, V_{CC} must rise from 2.0 V to V_{CC} minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{RESET}$ low until V_{CC} has reached 4.0 V. A very long V_{CC} rise time of >100 ms, or a nonmonotonically rising V_{CC}, may require a >1 µs high level on $\overline{RESET}$, followed by >6 µs low level on $\overline{RESET}$ and D/$\overline{P}$ after V_{CC} has reached 4.0 V.

Electrical Characteristics (continued)

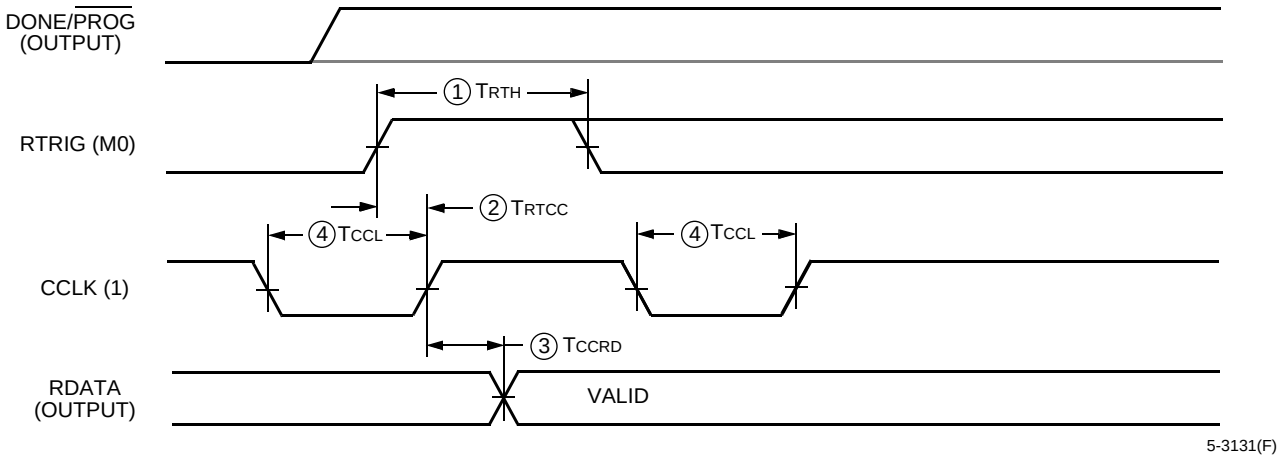


Figure 40. Program Readback Switching Characteristics

Table 30. Program Readback Switching Characteristics

Commercial: V_{CC} = 5.0 V ± 5%; 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{CC} = 5.0 ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Signal	Description	Symbol		Min	Max	Unit
RTRIG	RTRIG HIGH	1	T_{RTH}	250	—	ns
CCLK	RTRIG Setup	2	T_{RTCC}	200	—	ns
	$\overline{RDATA}$ Delay	3	T_{CCRD}	—	100	ns
	HIGH Time	5	T_{CCH}	0.5	—	µs
	LOW Time	4	T_{CCL}	0.5	5.0	µs

Notes:
During readback, CCLK frequency may not exceed 1 MHz.

RTRIG (M0 positive transition) must not be done until after one clock following active I/O pins.

Readback should not be initiated until after configuration is complete.

Outline Diagrams

Terms and Definitions

Basic Size (BSC): The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

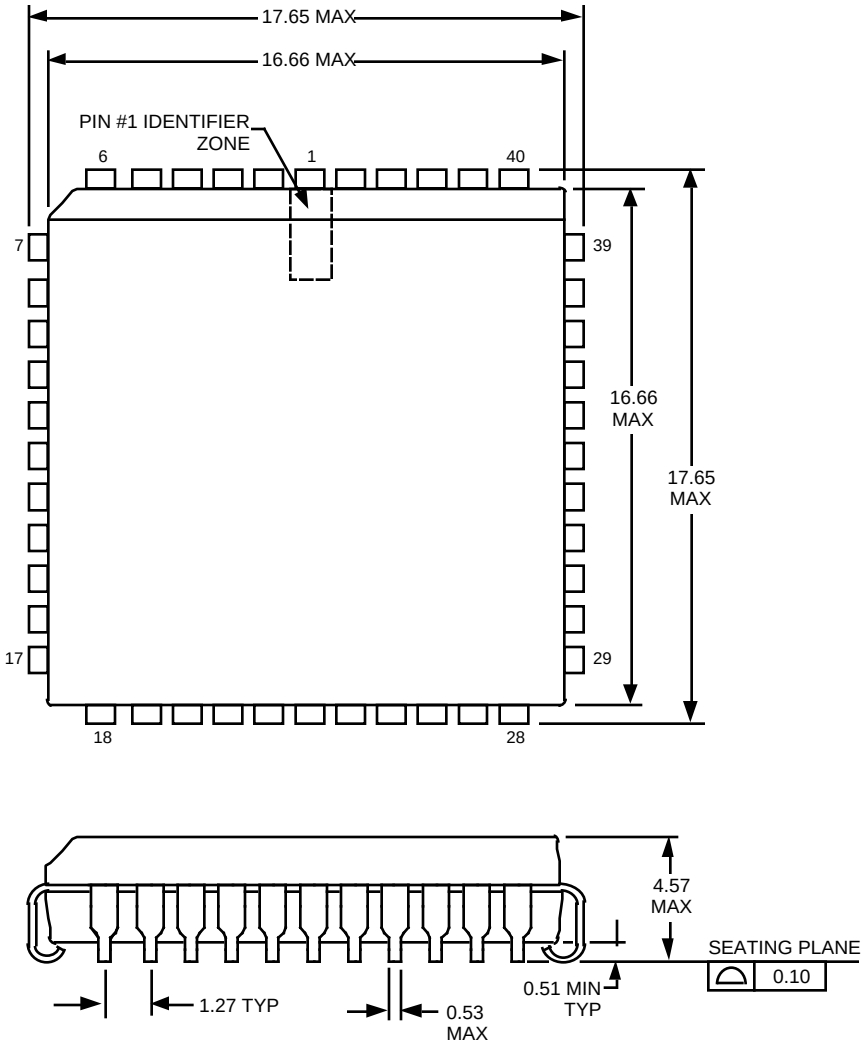
Typical (TYP): When specified after a dimension, indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

Reference (REF): The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or Maximum (MAX): Indicates the minimum or maximum allowable size of a dimension.

44-Pin PLCC

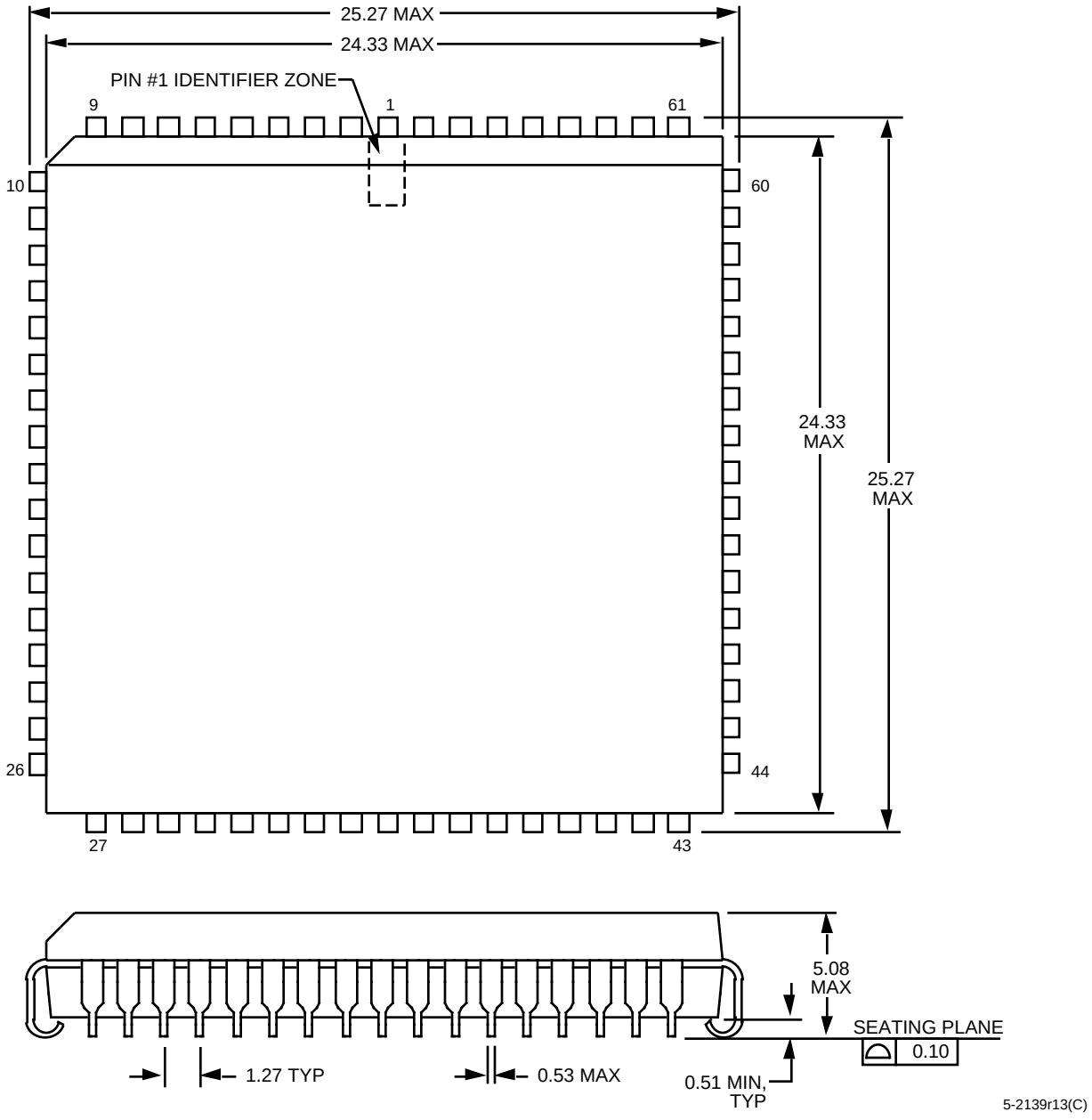
Dimensions are in millimeters.



Outline Diagrams (continued)

68-Pin PLCC

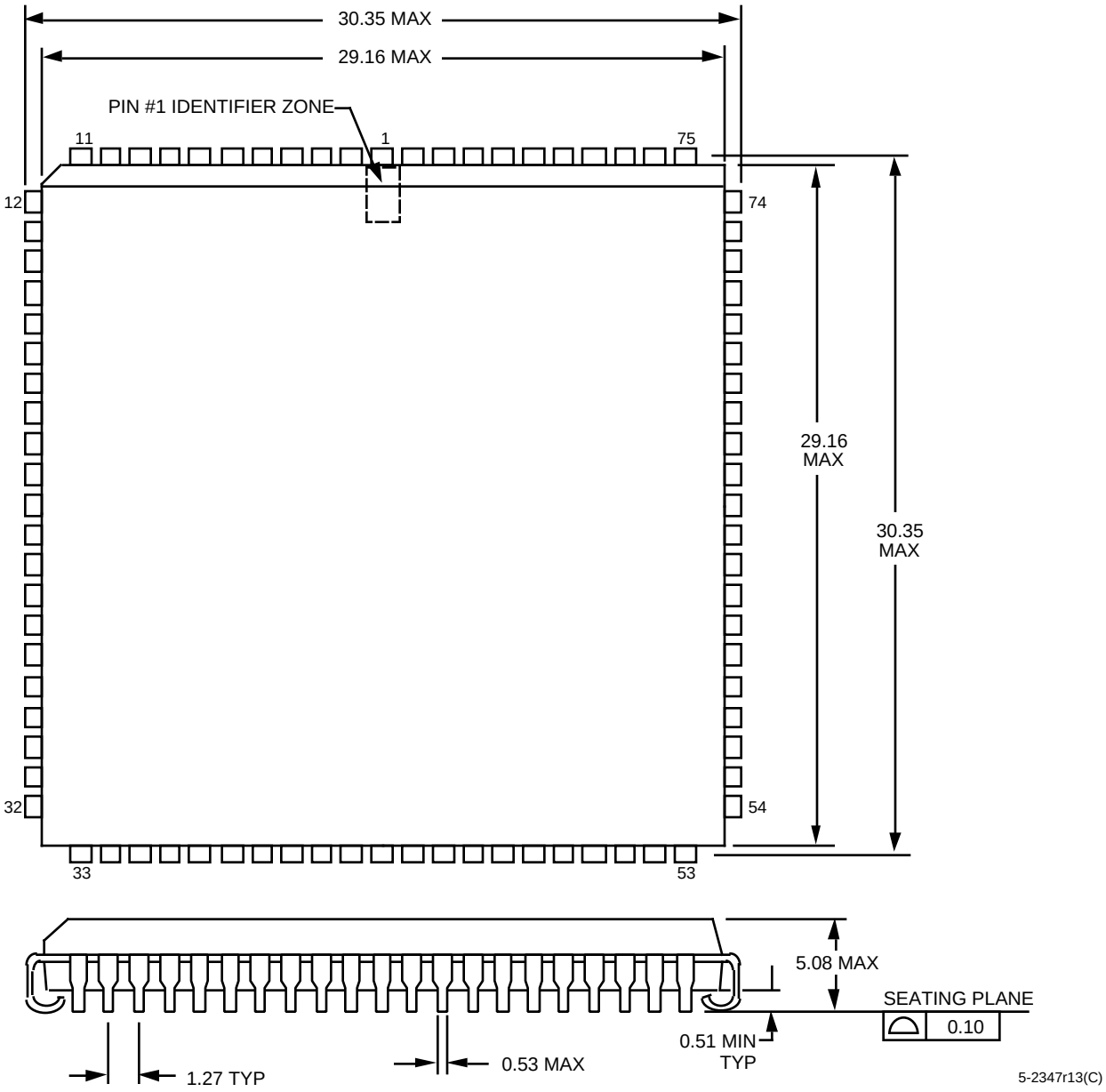
Dimensions are in millimeters.



Outline Diagrams (continued)

84-Pin PLCC

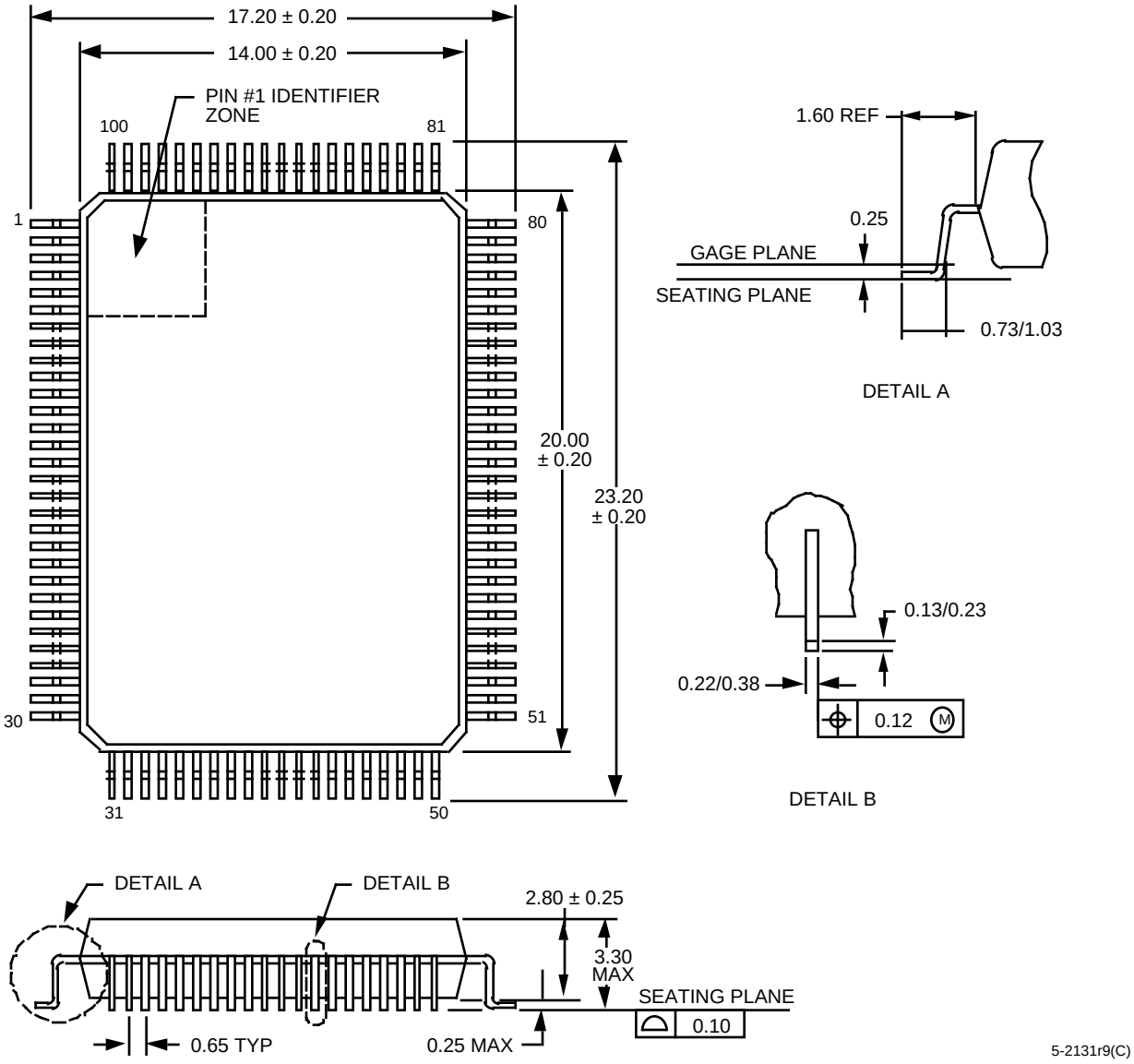
Dimensions are in millimeters.



Outline Diagrams (continued)

100-Pin QFP

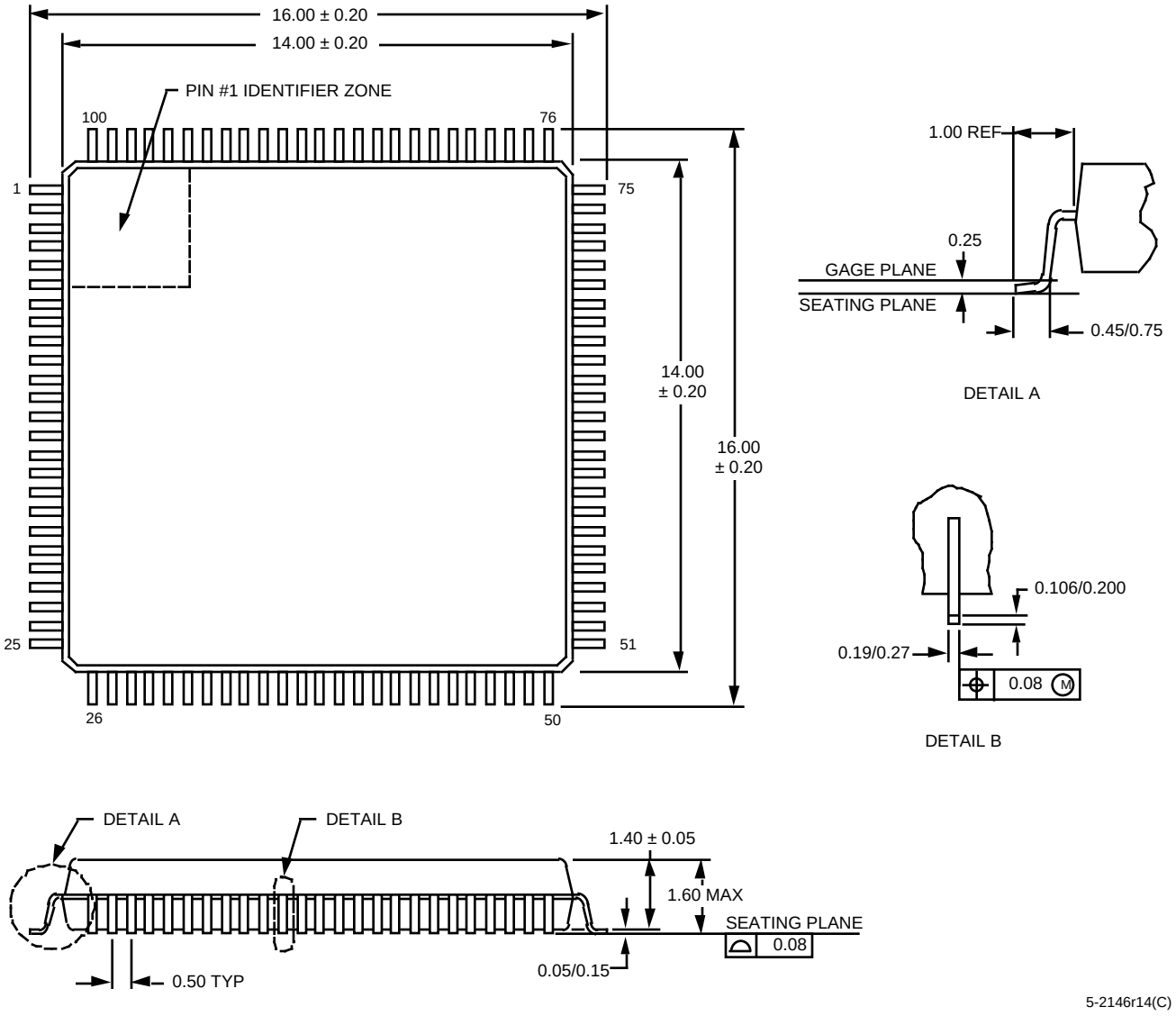
Dimensions are in millimeters.



Outline Diagrams (continued)

100-Pin TQFP

Dimensions are in millimeters.

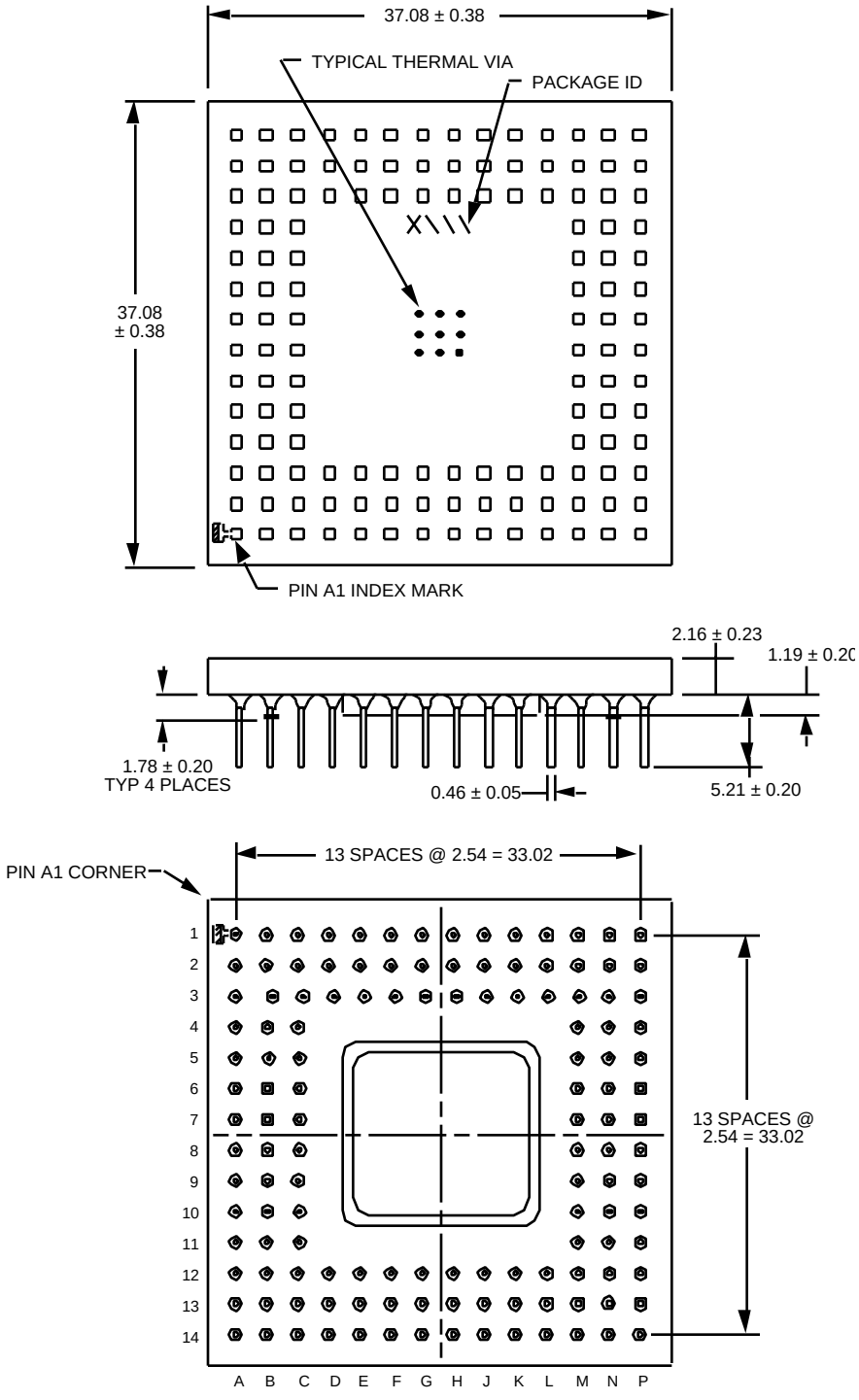


5-2146r14(C)

Outline Diagrams (continued)

132-Pin PPGA

Dimensions are in millimeters.

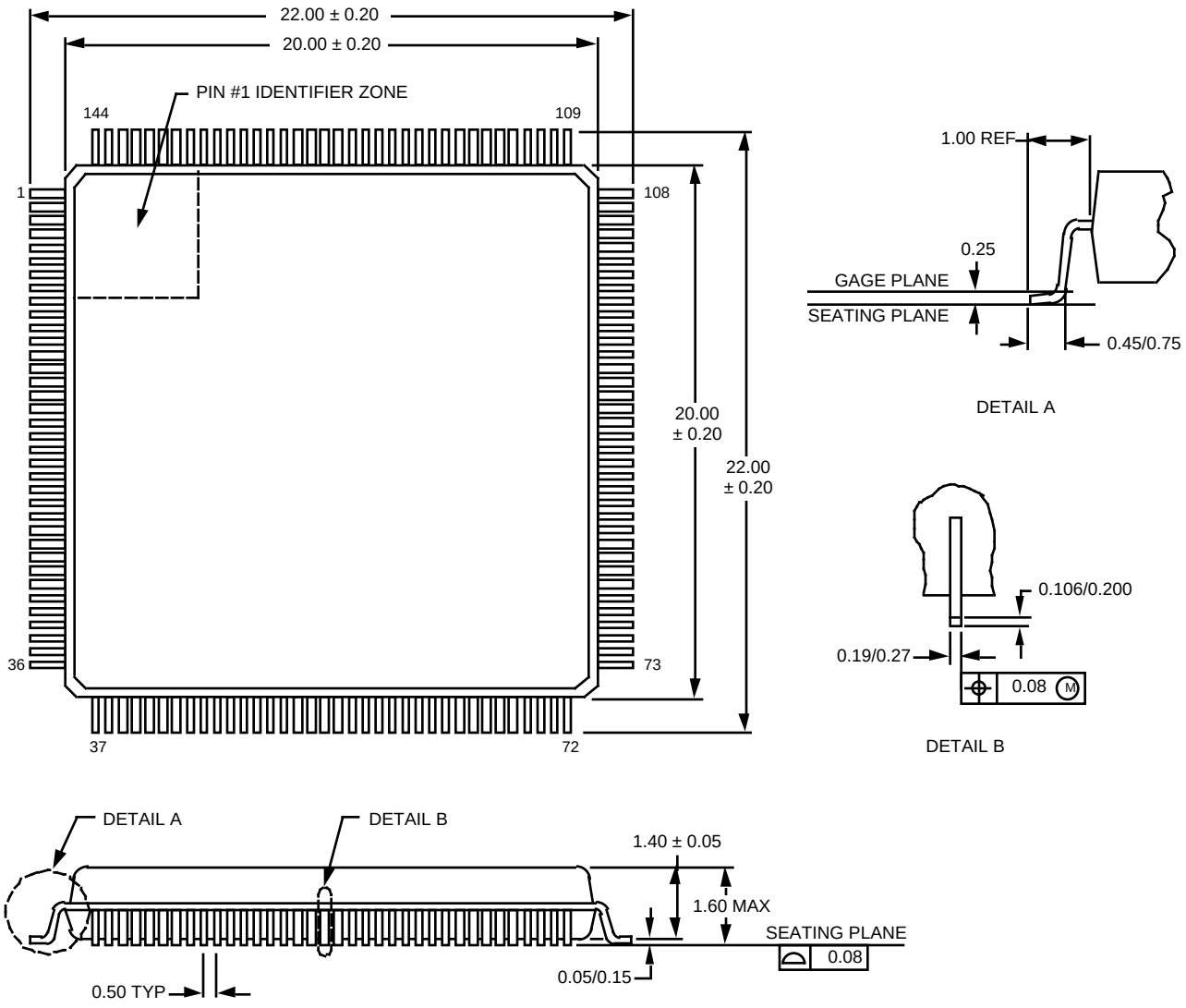


5-2115(C)

Outline Diagrams (continued)

144-Pin TQFP

Dimensions are in millimeters.

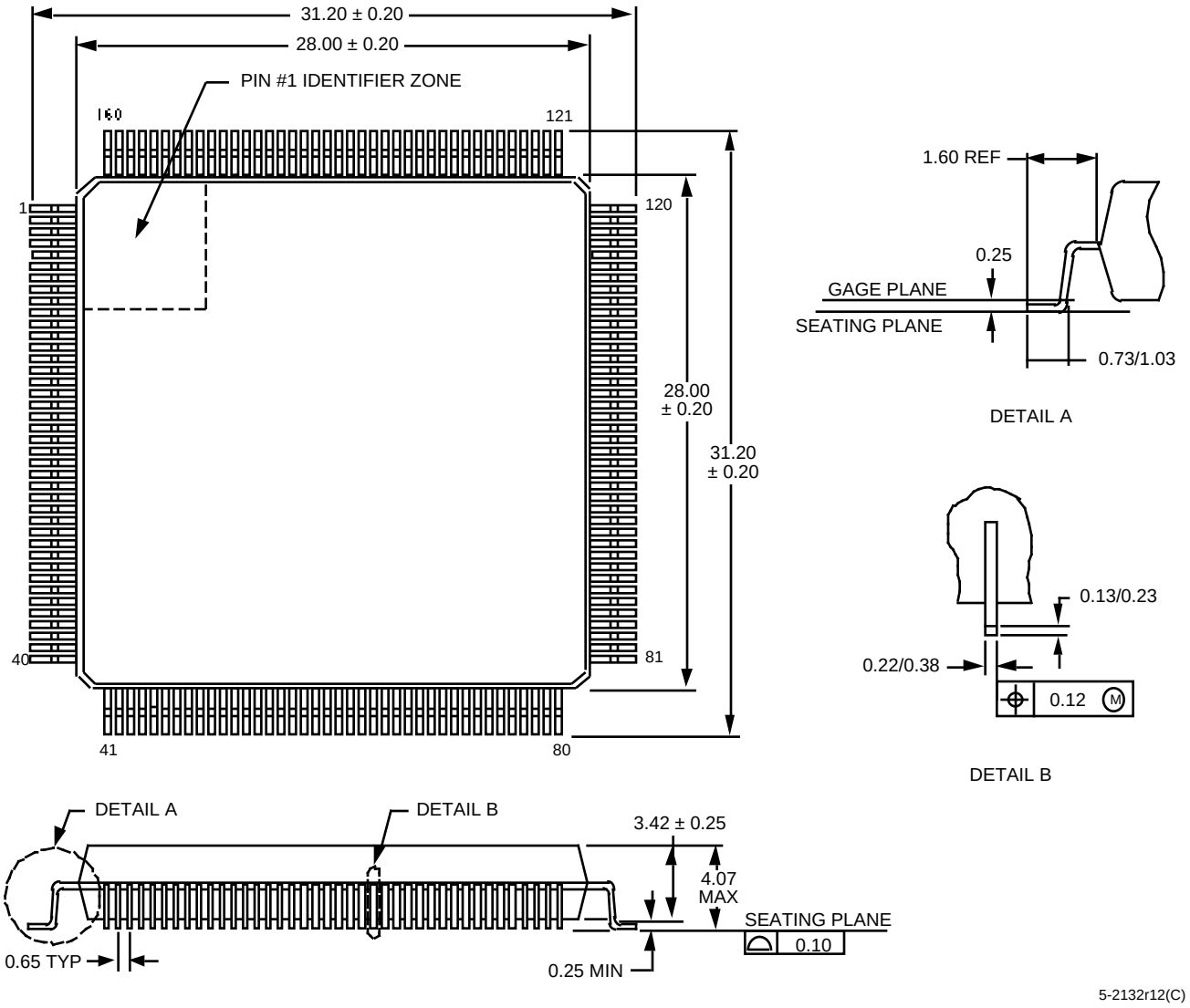


5-3815r5(C)

Outline Diagrams (continued)

160-Pin QFP

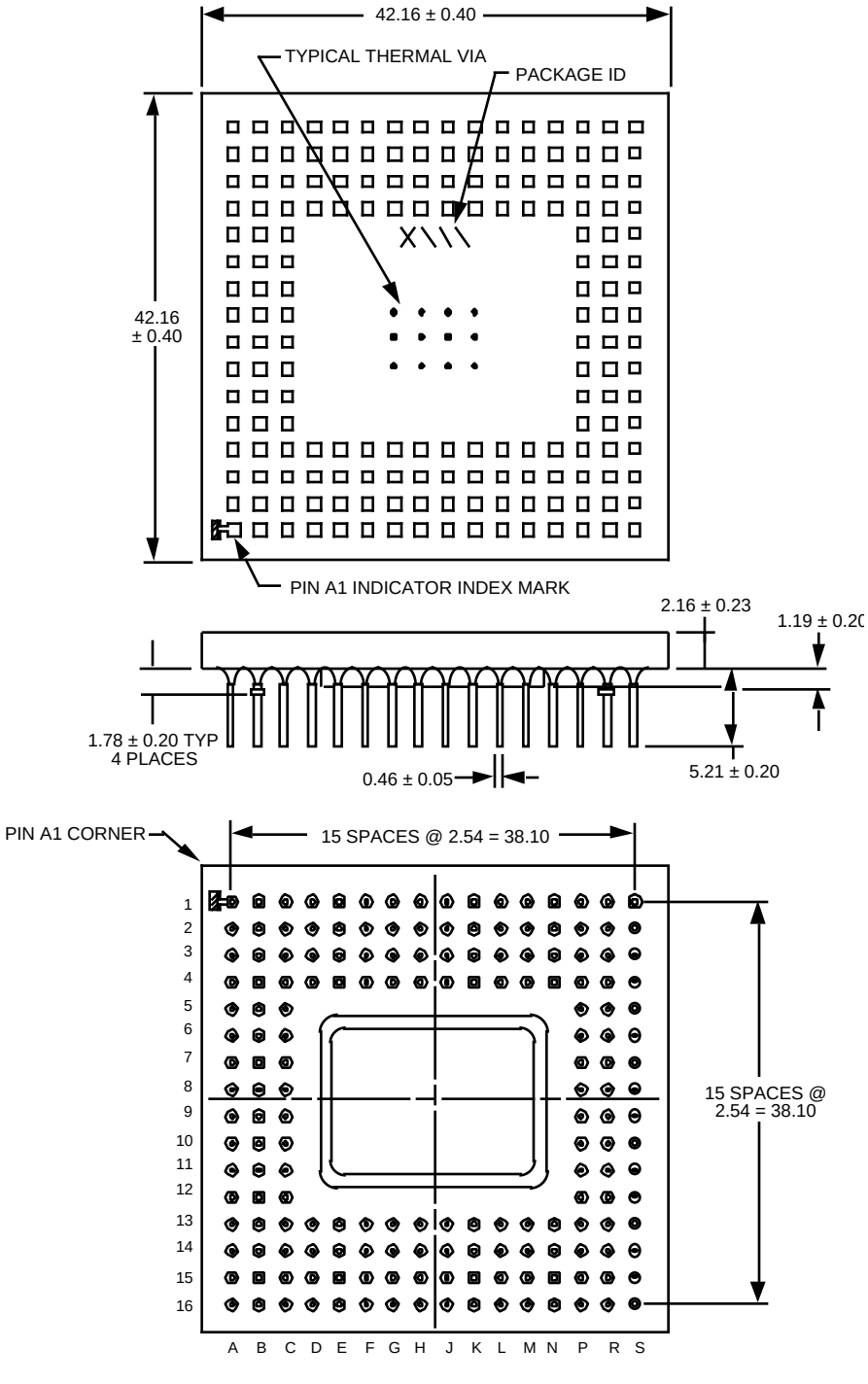
Dimensions are in millimeters.



Outline Diagrams (continued)

175-Pin PPGA

Dimensions are in inches.

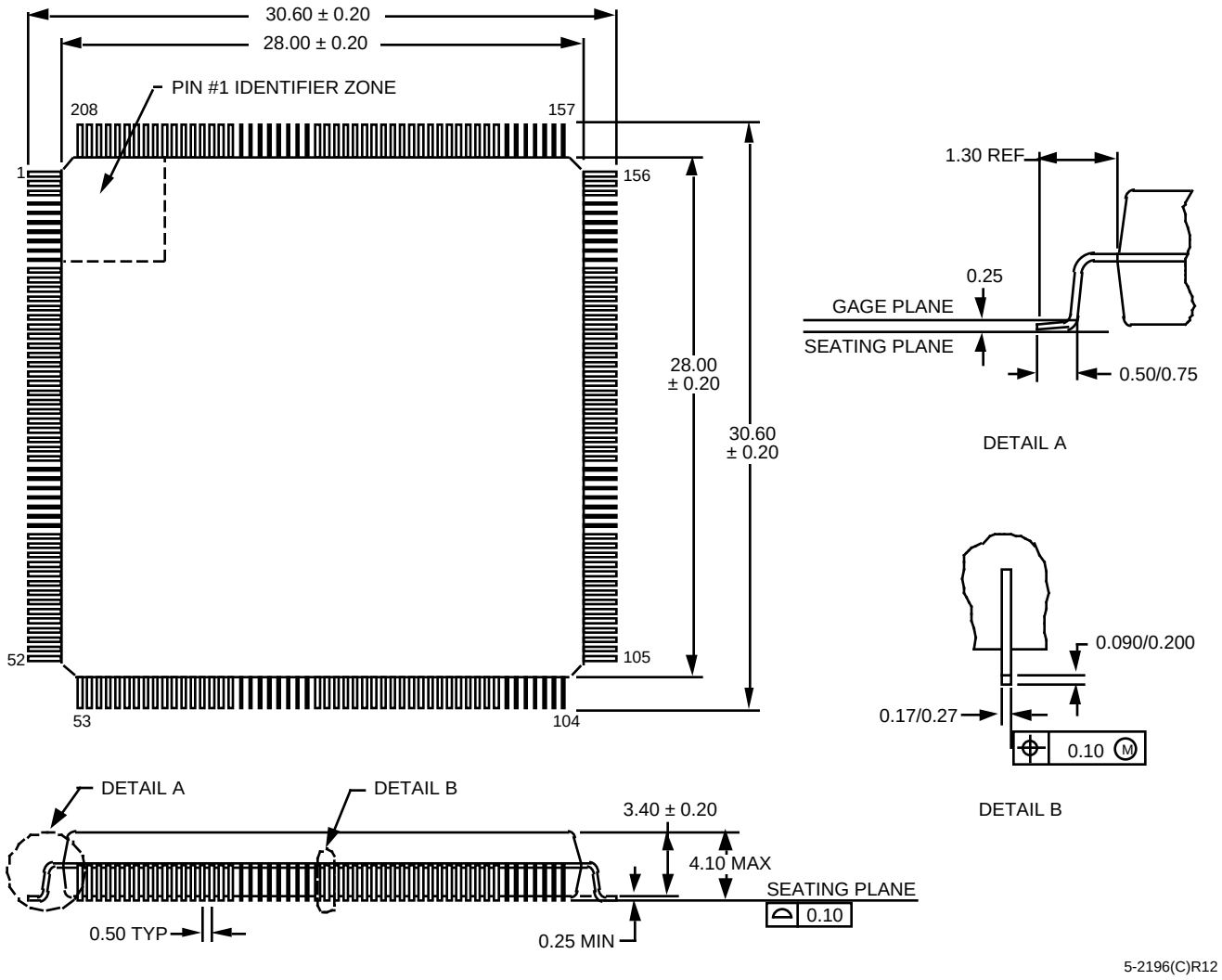


5-2116(C)

Outline Diagrams (continued)

208-Pin SQFP

Dimensions are in millimeters.



Ordering Information

The ATT3000 Series includes standard and high-performance FPGAs. The part nomenclature uses two different suffixes for speed designation. The lower-speed ATT3000 Series devices use a flip-flop toggle rate (-50, -70, -100, -125), which corresponds to *XC3000* Series nomenclature. The ATT3000 Series High-Performance FPGAs use a suffix which is an approximation of the look-up table delay (-5, -4, and -3), which corresponds to *XC3100* nomenclature.

For packaging options, burn-in diagrams, and/or package assembly information, call 1-800-EASY-FPG(A) or 1-800-327-9374.

Example: ATT3020, 100 MHz, 68-Lead PLCC, Industrial Temperature

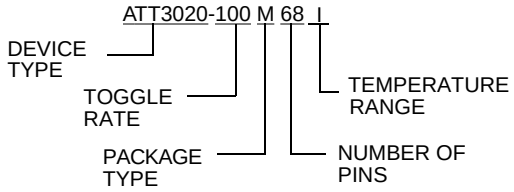


Table 31. FPGA Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	–40 °C to +85 °C

Table 32. FPGA Package Options

Symbol	Description
H	Plastic Pin Grid Array
J	Quad Flat Pack
M	Plastic Leaded Chip Carrier
S	Shrink Quad Flat Pack
T	Thin Quad Flat Pack

Ordering Information (continued)

Table 33. ATT3000 Series Package Matrix

Device	Speed	44-Pin PLCC	68-Pin PLCC	84-Pin PLCC	100-Pin		132-Pin PPGA	144-Pin TQFP	160-Pin QFP	175-Pin PPGA	208-Pin SQFP
					QFP	TQFP					
		M44	M68	M84	J100	T100	H132	T144	J160	H175	S208
ATT3020	-70	—	CI	CI	CI	—	—	—	—	—	—
	-100	—	CI	CI	CI	—	—	—	—	—	—
	-125	—	CI	CI	CI	—	—	—	—	—	—
	-5	—	CI	CI	CI	—	—	—	—	—	—
	-4	—	C	C	C	—	—	—	—	—	—
	-3	—	C	C	C	—	—	—	—	—	—
ATT3030	-70	CI	CI	CI	CI	CI	—	—	—	—	—
	-100	CI	CI	CI	CI	CI	—	—	—	—	—
	-125	CI	CI	CI	CI	CI	—	—	—	—	—
	-5	CI	CI	CI	CI	CI	—	—	—	—	—
	-4	C	C	C	C	C	—	—	—	—	—
	-3	C	C	C	C	C	—	—	—	—	—
ATT3042	-70	—	—	CI	CI	CI	CI	CI	—	—	—
	-100	—	—	CI	CI	CI	CI	CI	—	—	—
	-125	—	—	CI	CI	CI	CI	CI	—	—	—
	-5	—	—	CI	CI	CI	CI	CI	—	—	—
	-4	—	—	C	C	C	C	C	—	—	—
	-3	—	—	C	C	C	C	C	—	—	—
ATT3064	-70	—	—	CI	—	CI	CI	CI	CI	—	—
	-100	—	—	CI	—	CI	CI	CI	CI	—	—
	-125	—	—	CI	—	CI	CI	CI	CI	—	—
	-5	—	—	CI	—	CI	CI	CI	CI	—	—
	-4	—	—	C	—	C	C	C	C	—	—
	-3	—	—	C	—	C	C	C	C	—	—
ATT3090	-70	—	—	CI	—	—	—	—	CI	CI	CI
	-100	—	—	CI	—	—	—	—	CI	CI	CI
	-125	—	—	CI	—	—	—	—	CI	CI	CI
	-5	—	—	CI	—	—	—	—	CI	CI	CI
	-4	—	—	C	—	—	—	—	C	C	C
	-3	—	—	C	—	—	—	—	C	C	C

Key: C = commercial, I = industrial.

For FPGA technical applications support, please call 1-800-327-9374. Outside the U.S.A., please call 1-610-712-4331.

For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: **http://www.lucent.com/micro/fpga**

U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 1-610-712-4106 (In CANADA: **1-800-553-2448**, FAX 1-610-712-4106), e-mail **docmaster@micro.lucent.com**

ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495

JAPAN: Microelectronics Group, Lucent Technologies Semiconductor Marketing Ltd., 2-7-18, Higashi-Gotanda, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1770, FAX (81) 3 5421 1785

For data requests in Europe:

MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1734 324 299**, FAX (44) 1734 328 148

For technical inquiries in Europe:

CENTRAL EUROPE: **(49) 89 95086 0** (Munich), NORTHERN EUROPE: **(44) 1344 865 900** (Bracknell UK),
FRANCE: **(33) 1 41 45 77 00** (Paris), SOUTHERN EUROPE: **(39) 2 6601 1800** (Milan) or **(34) 1 807 1700** (Madrid)

Lucent Technologies Inc. reserves the right to make changes to the product(s) or information contained herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of any such product(s) or information. *ORCA* is a trademark of Lucent Technologies Inc. Foundry is a trademark of Xilinx, Inc.

Copyright © 1997 Lucent Technologies Inc.
All Rights Reserved
Printed in U.S.A.

February 1997
DS97-048FPGA (Replaces DS94-177FPGA)

microelectronics group

Lucent Technologies
Bell Labs Innovations

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP