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VPX55H-3 3U VPX DC/DC Converter

500-Watt Ruggedized Converter
Plug-in Module, Conduction-Cooled, Six Outputs

Made in the USA
Certified Small Business

Description

NAI's VPX55H-3 is a 500 Watt DC/DC Converter that plugs directly into a standard 3U VPX chassis with a VITA 62 0.8" power supply slot. This off-the-shelf solution for VITA 46.0 and VITA 65 systems is compatible with VPX specifications; supports all VITA standard I/O, signals, and features; and conforms to the VITA 62 mechanical and electrical requirements for modular power supplies.

The VPX55H-3 switching power supply is conduction-cooled through the card edge/wedgelock. It accepts +28 VDC input voltage and provides six outputs at 500 Watts.

The VPX55H-3 can be used either as a single-stage module or a back-end module in a multiple power supply configuration. It supports a variety of standard features, including continuous Background Built-in-Test (BIT); remote error sensing; and protection against transients, over-voltage, over-current, and short-circuits. With its intelligent design, the VPX55H-3 also has the flexibility to address special needs. Also included are reverse polarity protection and optional current share.

This COTS converter is specifically designed with NAVMAT component derating for rugged defense and industrial applications. It is also designed to meet the many harsh environmental requirements of military applications.



Features

- Ideal for rugged 3U VPX power applications
- Standard VPX-compatible connectors and I/O per VITA 62
- Compatible with System Management Bus per VITA 46.11
- Off-the-shelf solution for VITA 46.0 and VITA 65 systems
- Supports all VITA standard I/O, signals, and features
- Accepts +28 VDC input
- Provides six outputs and I/O at 500 Watts
- Continuous Background Built-in-Test (BIT)
- User Programmable
- Current share
- Input transient protection per MIL-STD-704F
- Integrated EMI filtering per MIL-STD-461F; CE102 standalone compliant
- Environmentals per MIL-STD-810G and VITA 47
- Operates at full load through the entire -40°C to +85°C temperature range

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Electrical Specifications

DC Input Characteristics	
Input	+28 VDC (+16 VDC to +36 VDC range)
EMI/RFI	Designed to meet the requirements of MIL-STD-461F; CE102 standalone compliant (**without** additional filtering); refer to typical CE102 scan on page 9
Input Transient Protection	Per MIL-STD-704F
Output Power	500 Watts max (see Output Power Table, page 3)
Output Voltage	VPX outputs standard (see Output Power Table, page 3)
Efficiency	89% typical; refer to typical efficiency scan on page 9
Switching Frequency	200KHz
Line Regulation	Within 0.5% or 20 mV (whichever is greater) for low to high line changes at constant load. For current share units: 1.5% for VS1, VS2, VS3; 2% for +3.3 VDC_Aux, +12 VDC_Aux, -12 VDC_Aux
Load Regulation	0.5% or 20 mV (whichever is greater) for 0 to 100% of rated load at nominal input line with remote sense. 1% for -12 VDC_Aux , +12 VDC_Aux, +3.3 VDC_Aux; For current share units: 1.5% for VS1, VS2, VS3, +3.3 VDC_Aux; 2% for +12 VDC_Aux, -12 VDC_Aux
PARD (Noise and Ripple)	1% or 50 mV p-p max per VITA 62; measurements are made with a 20 MHz bandwidth instrument connected on load wires < 5 inches from power supply and terminated with 1uF capacitors across load lines
Load Transient Recovery	Output voltage returns to regulation limits within 0.5 msec, half to full load
Load Transient Under/Overshoot	5% of nominal output voltage set point (1.4 V max); 2.5% for VS3
Short Circuit Protection	Protected for continuous short circuit with automatic recovery
Current Limiting	All outputs 125% to 130%
Over Voltage Protection	Automatic electronic shutdown if outputs exceed 125% ±10%
Remote Error Sensing	Sensing pins compensate for up to 0.5 V drop on VS1 to VS3 outputs
Isolation Voltage	500 VDC input to output and input to case; 100 VDC output to case
Insulation Resistance	50 Mega Ohm at 500 VDC

All specifications are subject to change without notice.

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Additional Specifications

Physical/Environmental	
Temperature Range	Operating: -40°C to +85°C at 100% load (temperature measured at card edge, conduction via card edge); Storage: -55°C to +105°C per VITA 47 CC4)
Temperature Coefficient	0.01% per °C
Shock	30 G's each axis per MIL-STD-810G, Method 516.6, Procedure 1; Hammer shock per MIL-S 901, ½ sine wave per VITA 47 OS2
Acceleration	6 G's per MIL-STD-810G, Method 513.6, Procedure II
Vibration	Per MIL-STD-810G, Method 514, Procedure 1; Per VITA 47, Class V3
Humidity	95% at 71°C per MIL-STD-810G, Method 507.5 (non-condensing)
Altitude	1,500 feet below sea level to +60,000 feet above sea level per VITA 47
Salt & Fog	Per MIL-STD-810G, Method 509.5
Sand/Dust	Per MIL-STD-810G, Method 510.5
Fungus	Per MIL-STD-810G, Method 508.6
ESD	15 kV EN61000-4-2 per VITA 47
Enclosure	Aluminum housing to aluminum baseplate
Dimensions	See Mechanical Layout
Finish	Chemical film IAW MIL-DTL-5541, Type II, Class 3
Interface	50 Micro-Inch Gold on contacts; plated tails for tin whisker mitigation; See Connector Part Numbers below
Weight	1.4 lbs. Typical

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Signal Types

Signal	Description
ENABLE*	Turns off all of the output voltages, including 3.3 V_AUX, when signal is High. ENABLE* is pulled Low by using a mechanical switch which connects it to SIGNAL_RETURN. A Logic output can also be used to drive the ENABLE*. Opening the switch would turn off all the outputs; closing the switch or applying the Logic output would enable the outputs to come on depending on the state of INHIBIT*. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with INHIBIT*, this signal determines the output power status of the VPX55H-3 (see Power Status Table below).
INHIBIT*	Turns off all the output voltages. In most implementations, the signal is expected to leave 3.3 V_AUX on. Pulling INHIBIT* Low turns off VS1, VS2, VS3, and ±12 VDC_Aux outputs. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with ENABLE*, this signal determines the output power status of the VPX55H-3 (see Power Status Table below).
SYSRESET*	An active low open-collector line driven by the Power Monitor module. Signal ensures a clean, stabilized startup based on monitoring the output voltage levels in accordance with VITA 46.0, paragraph 4.8.11. Timing can be factory customized.
FAIL*	Indicates failure when any of the outputs are not within specification. Signal complies with VITA 65 for active Low. FAIL* signal is Open Drain. It is expected that there will be a pull-up resistor on the backplane.
VBAT	Provides a low-power +3.3 VDC @ 1A output to other plug-in modules. Intent is to supply power to low current devices, such as Real Time Clocks, when other outputs are off. While connected internally to the +3.3 VDC_Aux output, the signal provides a separate line dedicated to low power needs and has its own overcurrent protection. The signal is controlled thru power status, along with the +3.3 VDC_Aux output (see Power Status Table below).
Geographical Addressing	As defined in VITA 46
Current Share	Allows multiple supplies to share system load for VS1-VS3 outputs. Connection per designated pins each output.
Protocol	Per VITA 46.11 System Management Bus.
Status LED	See LED Status table below

LED Status

LED State	Meaning
Off	Input Low
Green (Steady)	Vout OK; All outputs are good
Red (Steady)	Fail; Follows same logic as FAIL* signal
Blinking Green	Unit disabled
Blinking Red	Over Voltage or Over Temperature (all outputs are off)

Power Status

Control Input States		Power Output States	
ENABLE*	INHIBIT*	+3.3V_AUX	VS1, VS2, VS3, +12V_AUX & -12V_AUX
High	High	Off	Off
High	Low	Off	Off
Low	High	On	On
Low	Low	On	Off

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I²C Communication

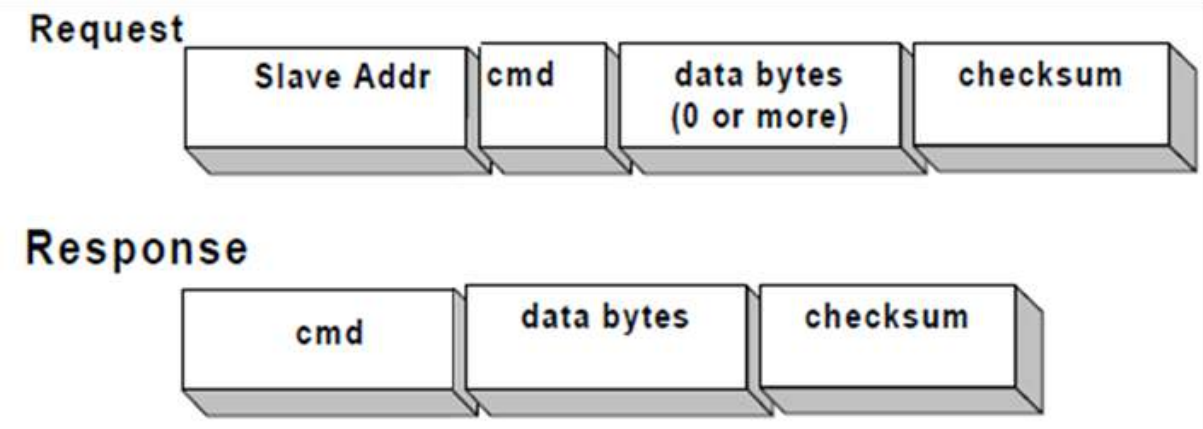
1. **Hardware Interface.**
   Electrical interface is based on I2C parameters at 100 kHz. The backplane or I2C master controller should provide pull up resistors on SDA and SCL lines to a 3.3V rail.

2. **Address.**
   The I2C Address is 7 bits. Default base address is 0x20. *GA0, and *GA1 provides 2 LSB's for the address.

   The *GA pins have pull-up resistors internal to the power supply to 3.3V. When left open, the address will be 0x20, with both grounded the address will be 0x23, see table below.

Pin		I2C Address
*GA1	*GA0	
Pin B5	Pin A5	
High	High	0x20
High	Gnd	0x21
Gnd	High	0x22
Gnd	Gnd	0x23

3. **Data Read - Get Sensor Reading results**



	Byte	Data Field	Data
Request Data	1	cmd	See table
	2 to n-1	Data If Required by cmd or Zero ChkSum* if no Data required.	
	n	Zero ChkSum* if Data was required by cmd	
Response Data	1	Completion Code – Echo cmd Number	
	2 to n-1	Per cmd Response	
	n	Zero ChkSum	

Note : Slave address should not be included in Zero Checksum calculation.

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4. Commands

Sensor #	Name	Description
21H	Composite Sensor	64 bytes of scanned sensor data. Data is continually scanned and available for report. Data consists of 2 bytes of data for each of the 11 sensors and FRU data.
55H	Status Write Command	Writes Status byte on Composite Sensor.
44H	Firmware release date	22 byte response. Month/Day/Year Hr/Min/Sec in ASCII form.
45H	Hardware Address	3 byte response. Reports address set by GA0*-GA1*

4.1 Composite Sensor Read Command – 21H

Response BYTE #	Data Type	Meaning
0	Completion Code – 21h	Echo of the command
1	Status Register 0, MS Bit	Refer to table below
2-3	Signed Integer, MSB First	Temperature as follows °C = (Reading * 100 / 16384)
4-5	U Integer, MSB First	Voltage on VS1, 12V = 16384
6-7	U Integer, MSB First	Voltage on VS2, 3.3 = 16384
8-9	U Integer, MSB First	Voltage on VS3, 5V = 16384
10-11	U Integer, MSB First	Voltage on 3.3Aux, 3.3V = 16384
12-13	U Integer, MSB First	Voltage on +12V Aux, 12V = 16384
14-15	U Integer, MSB First	Absolute Voltage on -12V Aux, 12V = 16384
16-17	U Integer, MSB First	Current on VS1, 30A = 16384
18-19	U Integer, MSB First	Current on VS2, 20A = 16384
20-21	U Integer, MSB First	Current on VS3, 40A = 16384
22-23	U Integer, MSB First	Current on 3.3Aux, 4A = 16384
24-25	U Integer, MSB First	Current on +12VAux, 1A = 16384
26-27	U Integer, MSB First	Absolute Current on -12VAux, 2.5A = 16384
28-29	U Integer, MSB First	Internal Reference, 2.5V = 16384
30-31	U Integer, MSB First	Input Voltage 28V = 16384
32-51	Character String	Part Number
52-53	U Integer, MSB First	S/N Hi
54-55	U Integer, MSB First	S/N Low
56-57	U Integer, MSB First	Date Code (Year/Week)
58-59	Character String	Hardware Rev
60-61	Character String	Firmware Rev
62	Reserved	Reserved
63	Zero Checksum	Value required to make the sum of bytes 0 to 62 add to a multiple of 256 (decimal).

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Status Reg 0		R/Set	R/Set	R/W	R/W	R/W	R	R
Bit	7	6	5	4	3	2	1	0
	x	FAIL	OTWarning	SWPriority	*SW Inh	*SW En	*HW Inh	*HW En

Bits 5 AND 6 (OTWarning - FAIL) are Read and write. They are clear at startup. User can set them with a Status Write command. Hardware will clear them if there is a fault.

Bit 4 (SWPriority) is Read and write. It is clear at Startup. When clear the unit will be controlled by the hardware enable and inhibit signals. When set, the unit will be controlled by the SW inhibit and enable signals.

Bits 3 and 2 (SWInh SWEn) are read and write. Their logic works the same as the logic for the hardware Enable and Inhibit.

*SWEnable	*SWInhibit	OUTPUTS
0	0	INHIBIT (3.3V Aux is On, all other outputs are off)
0	1	ON
1	0	OFF
1	1	OFF

Bits 1 and 0 (HWIn - HWEn) are read only. They show the state of *Enable and *Inhibit pins while SWPriority is low.

4.2 Status Write Command - 55H

BYTE #	Data Type	Meaning
0	U Character – 55H	Command
1	U Character	Data
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

The command to write to Status byte is 55h, followed by 8-bit data then zero checksum.

Example: To send a command to clear the faults and turn on all the outputs, the following sequence must be sent.
55h 78h 33h;

55h is the command needed to write to status byte zero.
78h data for byte zero,

Bit 7 set: don't care bit.
Bit 6 set: FAIL signal is high, software will clear it if unit fails
Bit 5 set: OTWarning signal is high, software will clear it if unit is close to 75 degrees.
Bit 4 set: Software has priority to enable/disable unit.
Bit 3 set: SWInhibit is high
Bit 2 low: SWEnable is low.

33h Value to achieve a sum of zero.

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4.3 Firmware release date – 44H

Response BYTE #	Data Type	Meaning
0	Completion Code – 44H	Echo of the command
1-20	Character String	Date
21	Zero Checksum	Value required to make the sum of bytes 0 to 20 add to a multiple of 256 (decimal).

4.4 Hardware Address – 45H

Response BYTE #	Data Type	Meaning
0	Completion Code – 45H	Echo of the command
1	U Character	I2C Hardware Address
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

Output Power

500-Watt Power*		
Designation	**Volts**	**Amps**
VS1	+12	30
VS2	+3.3	20
VS3	+5.0	40
+12_Aux	+12	3**
-12_Aux	-12	3**
+3.3_Aux	+3.3	4

***Total output power limited to 500 Watts**
**** Uses UD pins to get 3 Amps (refer to pinout Table)**

Connector Specifications

Unit	Backplane
P0: TE Connectivity p/n 2314578-2	**J0:** 2 TE Connectivity p/n 2309390-1

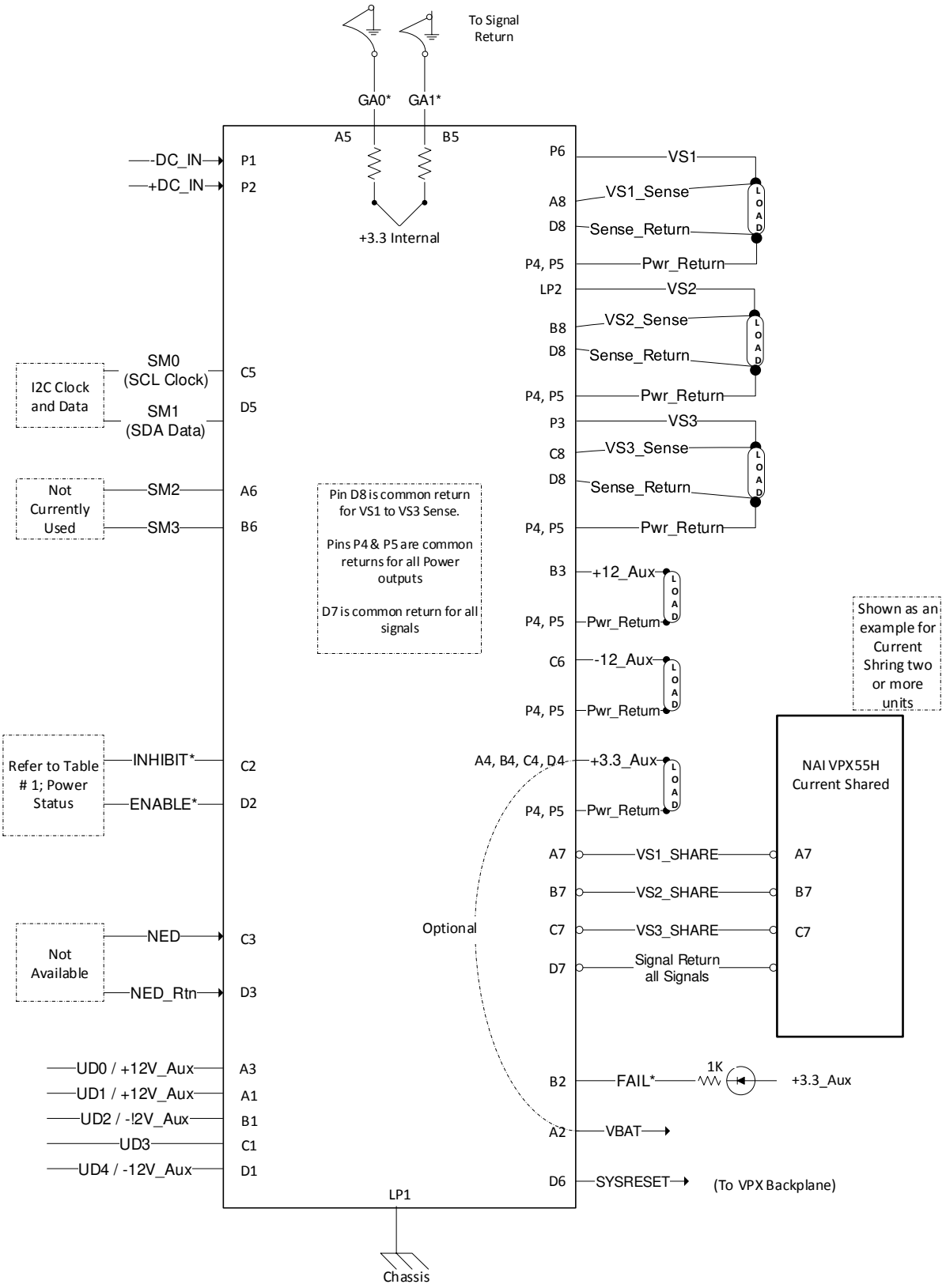
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Pinout Designations (P0)

Pin #	Rated Current (A)	Pin Name (Std)	Pin Name (Code 03)	Description	Pin #	Rated Current (A)	Pin Name (Std)	Pin Name (Code 03)	Description
P1	40A	-DC_IN/ACN	-DC_IN/ACN	28Vdc Input Rtn	B5	<1A	GA1*	GA1*	Geographical Address
P2	40A	+DC_IN/ACL	+DC_IN/ACL	+28Vdc Input	C5	<1A	SM0	SM0	System Mgmt. Bus line (I^2C Clock)
LP1	20A	CHASSIS	CHASSIS	Chassis Ground	D5	<1A	SM1	SM1	System Mgmt. Bus line (I^2C Data)
A1	<1A	+12 V_AUX	UD1	+12Vdc_Aux Output / User Defined 1	A6	<1A	SM2	SM2	Not Currently Used
B1	<1A	-12 V_AUX	UD2	-12Vdc_Aux Output / User Defined 2	B6	<1A	SM3	SM3	Not Currently Used
C1	<1A	UD3	UD3	User Defined 3	C6	<1.5A	-12 V_AUX	-12 V_AUX	-12Vdc_Aux Output
D1	<1A	-12 V_AUX	UD4	-12Vdc_Aux Output / User Defined 4	D6	<1A	SYS_RESET*	SYS_RESET*	Active Low Open Collector
A2	<1A	VBAT (optional)	VBAT (optional)	Connected internally to +3.3Vdc_Aux	A7	<1A	VS1_SHARE	VS1_SHARE	Current Share VS1
B2	<1A	FAIL*	FAIL*	Active Low Open Collector	B7	<1A	VS2_SHARE	VS2_SHARE	Current Share VS2
C2	<1A	INHIBIT*	INHIBIT*	Used with ENABLE* See power status table	C7	<1A	VS3_SHARE	VS3_SHARE	Current Share VS3
D2	<1A	ENABLE*	ENABLE*	Used with INHIBIT* See power status table	D7	<1A	SIGNAL_RETURN	SIGNAL_RETURN	Common Signal Return
A3	<1A	+12 V_AUX	UD0	+12Vdc_Aux Output / User Defined 0	A8	<1A	VS1_SENSE	VS1_SENSE	Remote Sense VS1
B3	<1.5A	+12 V_AUX	+12 V_AUX	+12Vdc_Aux Output	B8	<1A	VS2_SENSE	VS2_SENSE	Remote Sense VS2
C3	<1A	NED	NED	***FEATURE NOT AVAILABLE***	C8	<1A	VS3_SENSE	VS3_SENSE	Remote Sense VS3
D3	<1A	NED_RETURN	NED_RETURN	***FEATURE NOT AVAILABLE***	D8	<1A	SENSE_RETURN	SENSE_RETURN	Common Remote Sense Return
A4	<1.5A	+3.3 V_AUX	+3.3 V_AUX	+3.3Vdc Aux Output	P3	40A	VS3	VS3	VS3 Output
B4	<1.5A	+3.3 V_AUX	+3.3 V_AUX	+3.3Vdc Aux Output	P4	40A	POWER_RETURN	POWER_RETURN	Common Output Return
C4	<1.5A	+3.3 V_AUX	+3.3 V_AUX	+3.3Vdc Aux Output	P5	40A	POWER_RETURN	POWER_RETURN	Common Output Return
D4	<1.5A	+3.3 V_AUX	+3.3 V_AUX	+3.3Vdc Aux Output	LP2	20A	VS2	VS2	VS2 Output
A5	<1A	GA0*	GA0*	Geographical Address	P6	40A	VS1	VS1	VS1 Output

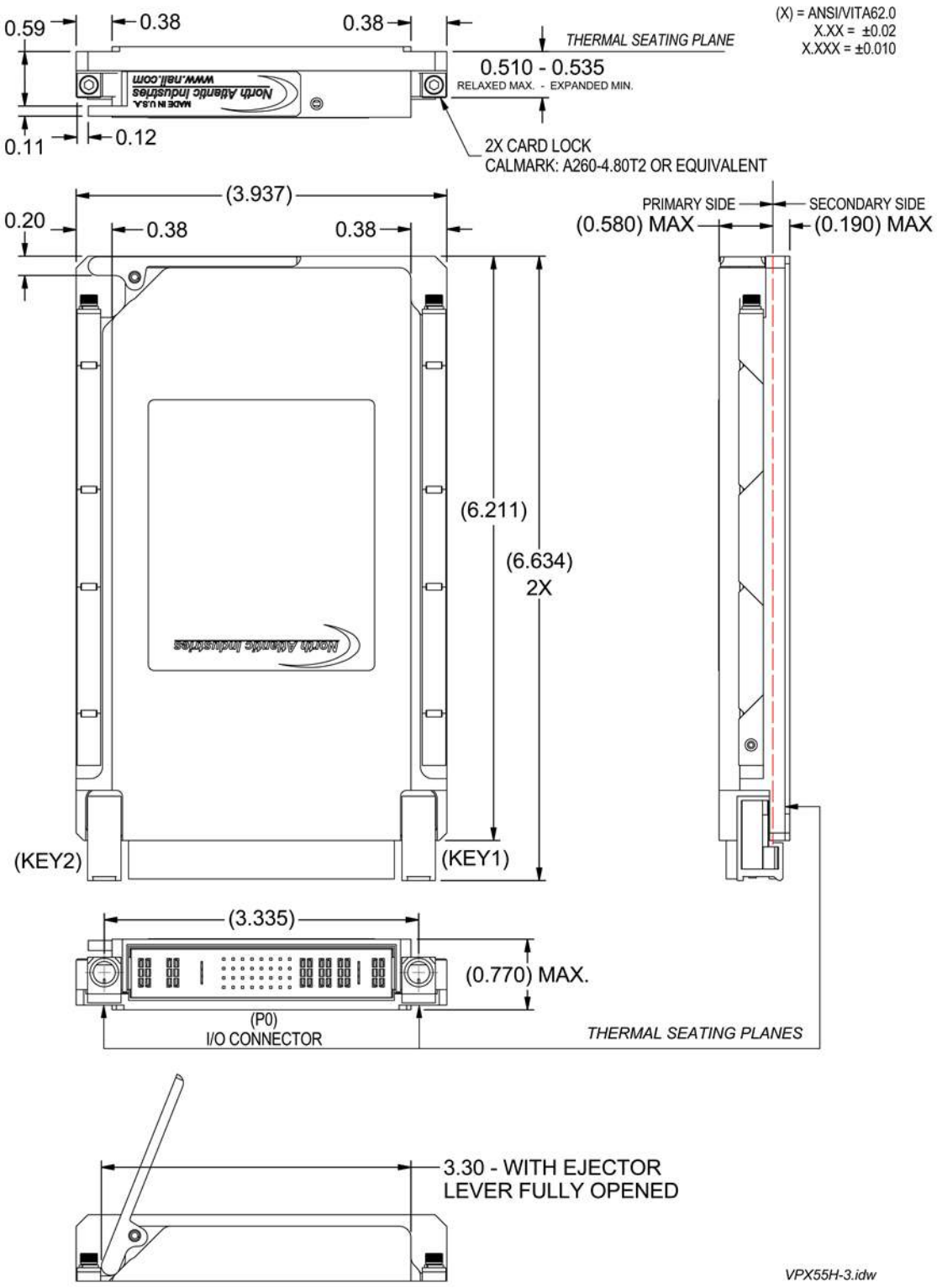
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VPX55H-3 Connections



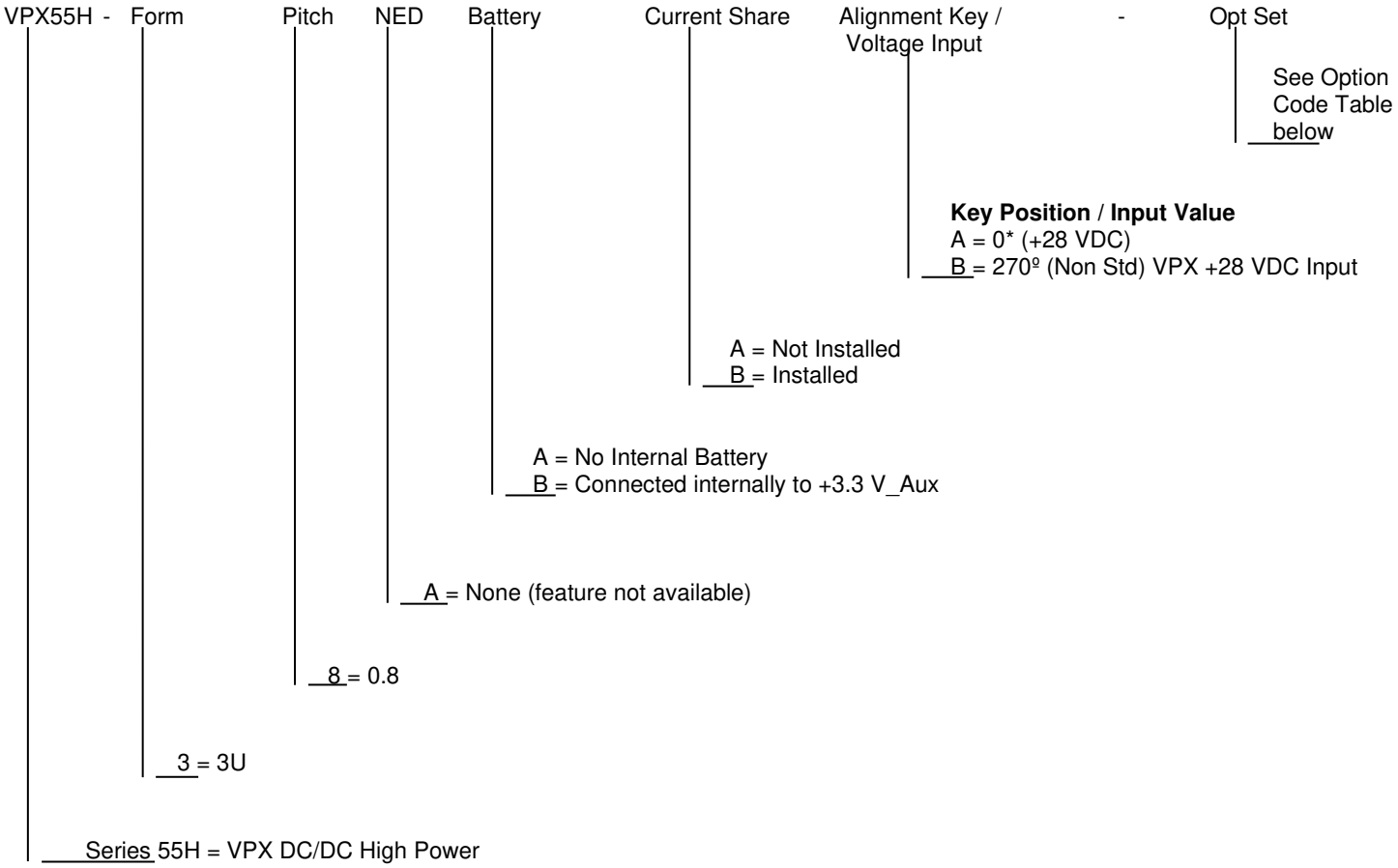
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Mechanical Layout



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Ordering Information



Example: VPX55H-38AABA-00 = 3U VPX DC/DC Converter; 0.8” pitch; no NED feature; no internal battery; current share on VS1, VS2, and VS3; +28 VDC innput; 500-Watt output power

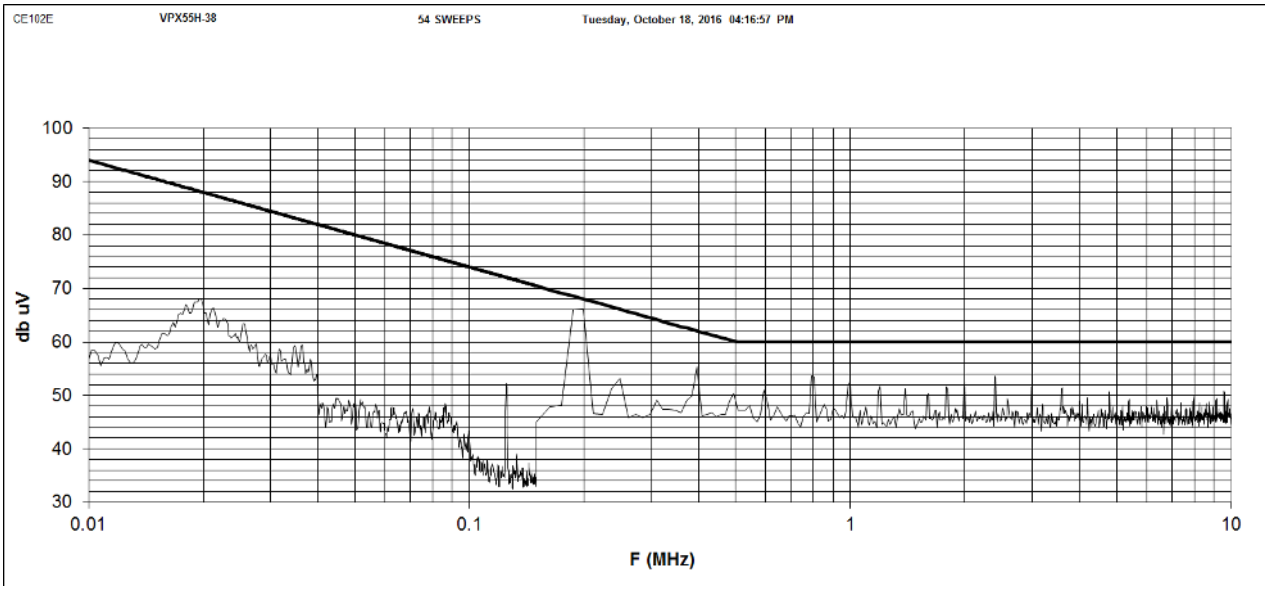
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Option Code Table

Code	Description
00	Standard unit, no additional options
01	VS1 will be +11Vdc (instead of +12Vdc) when unit is plugged into (7 bit) Geographical Address slot 0X23; -12Vdc_Aux has 2.5A power. Part number for this version can only be VPX55H-38AAAA-01 (Current Share is not available for this version)
02	For VPX55H-38AAAA-02, VS3 will be +5.15Vdc (instead of +5.0Vdc) when unit is plugged into (7 bit) Geographical Address slot 0X21. Current Share is not available for this version.
03	Pins A1, B1, C1, D1 and A3 assigned as UD0 to UD4 instead of +/-12Vdc_Aux output pins
04	Modified to meet DO160G Section 16 Category Z 80Vdc transient. The power supply will shut off and automatically recover during this transient. For a 50V transient, the unit will operate continuously
05	Reserved
06	• Custom timing on the SYS_RESET*; Shall be asserted under all conditions when any of the voltages are not above minimum operating levels as specified in VITA 46.0 section 4.8.12.4 . SYS_RESET* shall be de-asserted 300 +/- 25 ms after all output power supply rails are within their operating ranges as defined in VITA 46.0 sections 3.2.2.1 and 3.2.2.3 • Output Rail Sequencing; Primary output rail power up sequence in the following order: +12 VDC, +5 VDC, +3.3 VDC. All output rails shall rise and fall monotonically during power transition states. ○ Additional Enable* functionality; When the module is powered but ENABLE* is not active, all power rail outputs shall measure less than 250mV (-250mV for the -12V_AUX rail).

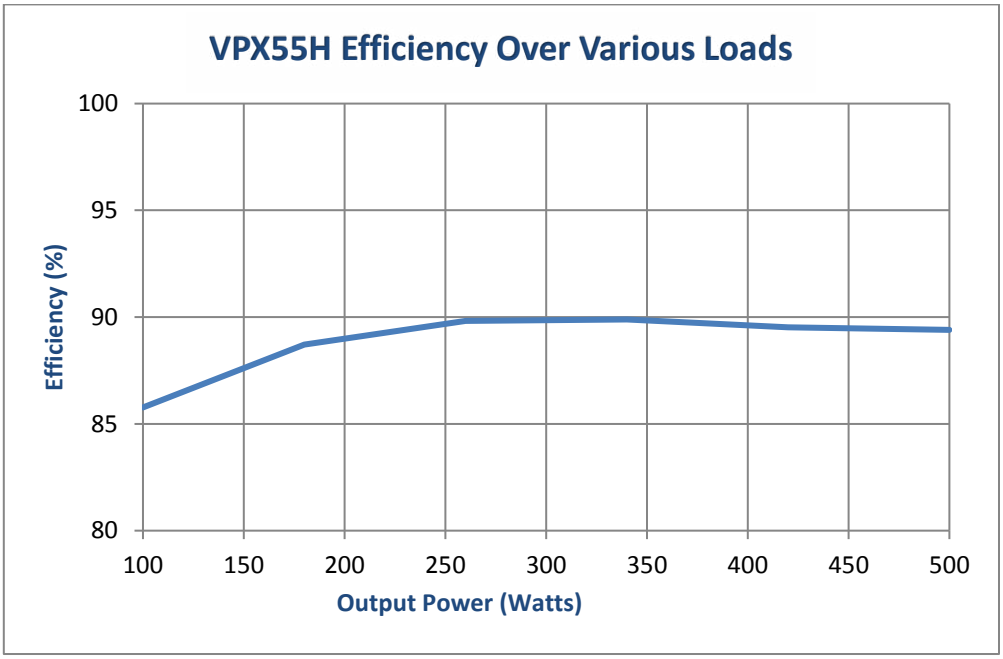
Performance Data

Typical CE102 EMI Performance as a Standalone Unit (under Full Load with no External Filtering)



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Typical Efficiency



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