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Operation/Maintenance Manual for **Model VXI 5388 Synchro/Resolver Processor**

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This manual applies to all units labeled with the model number 405088-1. The identification label is located on the rear panel between the P1 and P2 connectors.

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WARNING

SAFETY SUMMARY

GENERAL SAFETY NOTICES

The following general safety notices supplement the specific warnings and cautions appearing elsewhere in this manual. They are recommended precautions that must be understood and applied during operation and maintenance of the equipment covered herein.

DO NOT REPAIR OR ADJUST ALONE

Under no circumstances should repair or adjustment of energized equipment be attempted alone. The immediate presence of someone capable of rendering aid is required.

HIGH VOLTAGE IS USED IN THE OPERATION OF THIS EQUIPMENT

DEATH ON CONTACT may result if personnel fail to observe safety precautions. Learn the areas containing high voltage on this equipment. Be careful not to contact high-voltage connections when installing, operating, or maintaining this equipment.

SAFETY NOTICES APPLICABLE TO THIS TECHNICAL MANUAL

WARNINGS

The following warning appears on pages 5-1, 5-6 and 5-7 in this manual, and are repeated here for emphasis.

WARNING

Dangerous voltages may be present in the unit when the side cover is removed.

CAUTIONS

The following caution appears on pages 5-1, 5-6 and 5-7 in this manual, and is repeated here for emphasis.

CAUTION

The Model 5388 is electrostatically sensitive. Failure to comply with safeguards could damage the equipment. Refer to DOD-HDBK-263 for ESD sensitive equipment handling procedure.

The following caution appears on page 3-1 in this manual, and is repeated here for emphasis.

CAUTION

VXIbus card slot 0 cannot be used by the Model 5388. Slot 0 is reserved for a controller device (e.g., a CPU).

SECTION 1

GENERAL INFORMATION

1-1 INTRODUCTION

This manual provides the operation and maintenance instructions for the Model 5388 VXI Synchro-Resolver Processor (NAI P/N 405088) shown in figure 1-1, hereinafter referred to as Model 5388. Operation and maintenance information is presented in the following nine sections.

1-1.1 General Information. This section describes the purpose and gives a physical description of the Model 5388. Included in this section are Model 5388 specifications and special tools and test equipment required to maintain the Model 5388.

1-1.2 Theory of Operation. This section includes an overall block diagram discussion of the Model 5388; a systems software discussion including state diagrams; Model 5388 functional circuit interrelationships and a circuit board description based on detailed functional signal flow and schematic diagrams.

1-1.3 User Interface. This section contains installation instructions and information for interfacing the Model 5388 with external systems. It includes NATIVE programming commands, SIM/API operation instructions, railroad diagrams, and data input/output formats.

1-1.4 MATE/CIIL Programming Option. This section describes the Modular Automatic Test Equipment (MATE) Control Interface Intermediate Language (CIIL) operation and programming of the Model 5388. It includes programming commands, railroad diagrams, and data input/output formats.

1-1.5 Adjustment and Calibration. This section includes a schedule for periodic Model 5388 performance checkout, performance test procedures, and calibration and adjustment procedures. Test setup diagrams are also included.

1-1.6 Troubleshooting. This section provides troubleshooting instructions for isolating faults to the circuit group level of the Model 5388. Troubleshooting is based on symptoms derived from performing the performance checkout procedure and possible malfunctions which occur during normal use of the Model 5388.

1-1.7 Parts List. This section contains replaceable parts lists, federal supply codes of manufacturers (FSCM), parts location diagrams, and a list of manufacturers of parts used by the Model 5388.

1-1.8 Schematic Diagrams. This section contains schematic diagrams for the Model 5388.

1-1.9 Update Information. This section provides Product Revision Sheet (PRS) data which updates the Model 5388 to the latest configuration available.

1-2 PURPOSE

The Model 5388 IAC (Instrument on a Card) is a multi-functional instrument that combines a Synchro/Resolver Simulator (SIM) and Angle Position Indicator (API) on a single C-size VXI (VME bus Extension for Instrument) card.

The Model 5388 is configured for message based serial communications protocol which complies to VXIbus specifications. Typical applications include synchro or resolver alignment, gyro testing, fire control system testing, and servo system alignment.

1-3 PHYSICAL DESCRIPTION

The Model 5388 is packaged as shown in figure 1-1.

The Model 5388 is an instrument on a card (IAC) designed for use in a VXIbus card cage. The front panel contains the following:

a. Status Indicators
   (1) POWER
   (2) FAIL
   (3) MODID
   (4) SFI
   (5) RST

b. J1 -Simulator (Digital-to-Synchro) Output and Reference Input Connector

c. J2 -Angle Position Indicator (API) (Synchro-to-Digital) Input and Reference Input Connector

A complete description of the function and use of these indicators and communication ports is provided in Section 3. The Model 5388, shown in figure 1-1, consists of two major circuit card assemblies (CCA) which are configured for VXI card cage rack mounting. They are as follows:

a. Mother CCA A1

b. Daughter CCA A2

The Model 5388 is secured to the VXI card cage assembly with captive screws.

1-4 FEATURES AND OPTIONS

The Model 5388 is available with various options and custom configurations. To determine features and options, a two digit number is assigned in accordance with table 1-1.

For example, a Model 5388 with no MATE Language option and 400 Hz to 10 kHz Simulator would have a feature/option number of 5388-F11.

VXI 5388-F	1	1
	F1	F2

VXI 5388-F11

Table 1-1. Features and Options

Feature		Option
No.	Description	
F1	MATE Language	1. NATIVE Only 2. MATE/CIIL and NATIVE
F2	Frequency	1. 400 Hz to 10 kHz 2. 47 Hz to 400 Hz

1-5 REFERENCE DOCUMENTS

Recommended reference documents for use with the Model 5388 include:

a. VXIbus System Specification Revision 1.3 (Issue Date: 7/14/89)

b. MATE Control Interface Intermediate Language - Standard 2806763, Revision C

c. MOD 1 - MATE User's Group Action Traveler - CIIL Definitions.

1-6 SPECIFICATIONS

The technical features and capabilities of the API are compiled in specification table 1-2.

1-7 SPECIAL TOOLS AND TEST EQUIPMENT

Table 1-3 lists the special tools and standard test equipment required to maintain the Model 5388. The equipment listed or equivalents may be used.

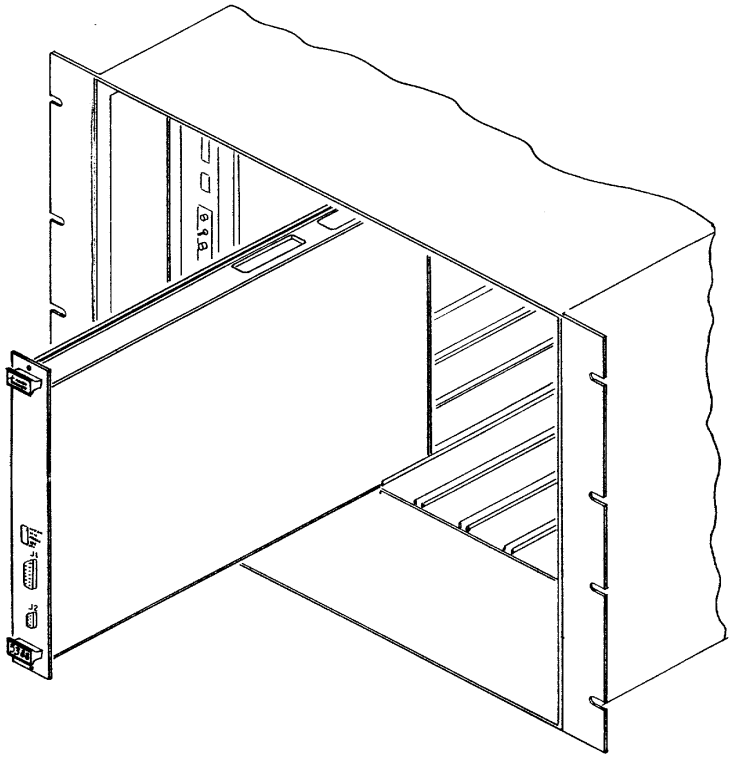


Figure 1-1. Model 5388

Table 1-2. Specifications (@ 25°C± 5°C)

Item	Specification
ANGLE POSITION MEASUREMENT	
Signal Input	
Configuration	Synchro or Resolver
Line-to-Line Voltage	2 to 90 Vrms, Programmable
Impedance	200 k ohms
Frequency	400 Hz to 10 kHz 47 Hz to 400 Hz
Reference Input	
Configuration	Synchro or Resolver
Line-to-Line Voltage	2 to 115 Vrms
Impedance	200 k ohms
Frequency	400 Hz to 10 kHz 47 Hz to 400 Hz
Resolution	0.001 degrees

Accuracy	(11.8-90 Vrms)	(2-11.7 Vrms)
400 Hz	0.002° + (2 x API Resolution)	0.004° + (2 x API Resolution)
2 kHz	0.003° + (2 x API Resolution)	0.006° + (2 x API Resolution)
10 kHz	0.013° + (2 x API Resolution)	0.018° + (2 x API Resolution)

Angular Range	0.000 to 359.999 degrees
AutoPhase Correction	±80 degrees
Data States	Track or Freeze

Tracking Rate

400Hz - 10kHz with Line-to-Line voltage ≥ 10 Vrms:
100 x (API Resolution / 0.001) degrees/second Minimum
47 Hz - 399Hz or Line-to-Line voltage < 10 Vrms:
50 x (API Resolution / 0.001) degrees/second Minimum

Settling Time

400Hz - 10kHz with Line-to-Line voltage ≥ 10 Vrms:

API Resolution = 0.001	2.5 second for 180° step change
API Resolution = 0.01	1.5 second for 180° step change
API Resolution = 0.1	1.0 second for 180° step change

47 Hz - 399Hz or Line-to-Line voltage < 10 Vrms:

API Resolution = 0.001	4.5 second for 180° step change
API Resolution = 0.01	3.0 second for 180° step change
API Resolution = 0.1	2.3 second for 180° step change

ANGLE POSITION SIMULATOR	
Signal Output	
Configuration	Synchro or Resolver
Line-to-Line Voltage	2 to 90 Vrms, Programmable

Table 1-2. Specifications (Continued)

Item		Specification
Impedance @ 400 Hz		11.8 V 26 V 90 V .4 +j.01W.4 + j.03W.6 + j.1W
Frequency		400 Hz to 10 kHz 47 Hz to 400 Hz
Reference Input		
Voltage		2 to 115 Vrms, Programmable
Impedance		200 k ohms minimum
Frequency		400 Hz to 10 kHz 47 Hz to 400 Hz
Resolution		0.001 degrees
Accuracy	@ 400 Hz	0.003 degrees No Load 0.004 degrees 1.5 VA load 0.006 degrees 3.0 VA load 0.009 degrees 6.0 VA load
	@ 10 kHz	0.015 degrees No Load 0.03 degrees 1.5 VA load*
*Loading Spec assumes to a 70° Inductive Load		
Angular Range		0.000 to 359.999 degrees
Data States		Track or Freeze
Tracking Rate		
Programmable		0.001 to 999.999 deg/sec
Functions		Fixed Angle, Constant Velocity, Triangular, Variable
GENERAL		
Interface		VXI Standard 1.2 MATE/CIIL
Connectors		P1 - Standard 15-pin, D-Type, male (supplied). See table 7-1. P2 - Standard 9-pin, D-Type, female (supplied). See table 7-1.
Control		Messaged Based, word serial
Configuration		Single C-size VXI Standard
POWER		
+5 Vdc		2.2 A
+12 Vdc		260 mA
-12 Vdc		200 mA
±24 Vdc		80 mA - No Load 450mA rms - 6 VA Load 900mA Peak - 6 VA Load

Table 1-2. Specifications (Continued)

Item	Specification
Temperature	
Operating	0 to 50 degrees C
Storage	-40 to 75 degrees C
Humidity	95% maximum noncondensing
Dimensions	9.187" x 13.386" x 1.2" 233 mm x 340 mm x 30 mm
Weight	6.2 lbs. (2.8 Kgs)
Cooling Requirements	
6 VA Load	1.9 mm H_2O @ 2.3 liter/sec
No Load	1.9 mm H_2O @ 1.4 liter/sec

Table 1-3. Special Tools and Test Equipment

Equipment	Minimum Use/Critical Specifications	Manufacturer & Model No.
Resolver-Synchro Simulator	Frequency: 60-400 Hz Range: 00.000° to 359.999° Accuracy: 10 arc second Modes: Synchro or Resolver Synchro Conventions meet MIL-S-20708A Resolver Conventions meet MIL-R-21530	North Atlantic Instruments, Models 5300 Synchro/Resolver Simulator
Resolver-Synchro Bridge		North Atlantic Instruments, Models 540/10 and 540/20
Phase Angle Voltmeter	Frequency: 47 - 10 kHz Sensitivity: 0.003 V to 100 V Voltage Accuracy: ±0.2% full scale Phase Accuracy: ±0.1°	North Atlantic Instruments, 2250 Phase Angle Voltmeter
Oscillator (Variable Signal Source), 90 V, 6 W, 10 k		Krohn-Hite 4000A with DC10A
Oscilloscope		Tektronix 454
Logic Analyzer (Optional)		Nicolet Paratronics Corporation NPC-700

1-8 EQUIPMENT REVISION LEVEL STATUS

Table 1-4 lists the major assemblies of the Model 5388 and the current revision level status of each assembly. For subsequent updates to Model 5388 assemblies refer to SECTION 9 UPDATE INFORMATION.

Table 1-4. Revision Level Status of Major Assemblies

Ref Des	Description	NAI P/N	Current Revision
A1	Mother CCA	789373-3	J
A1	Mother CCA	789373-4	J
A2	Daughter CCA	789104-1	G

SECTION 2

THEORY OF OPERATION

2-1 INTRODUCTION

This section contains theory of operation for the Model 5388 which is discussed at two levels. The first level presents an overall description of Model 5388 architecture and is supported by an overall block diagram (figure 2-1). The second level, a more detailed description of Model 5388 circuit interrelationships, is referenced to expanded block diagrams in figures 2-2, 2-3 and 2-4 and schematic diagrams in figures 8-1 and 8-2.

In addition, state diagrams are included to describe the VXIbus and its function (figure 2-5).

2-2 OVERALL BLOCK DIAGRAM DISCUSSION

The Model 5388 is a multifunction instrument that combines a Synchro/Resolver Simulator (SIM) and Angle Position Indicator (API) on a C-size VXI circuit card (A1). It is configured for message-based serial communications protocol which complies to VXIbus specifications. System and device interconnection is made via D-type connectors on the front panel.

As shown in figure 2-1, the architecture of the Model 5388 is organized into functional sections and is discussed in the following subparagraphs.

2-2.1 Synchro-to-Digital Converter. The synchro and resolver signals used for angle position measurements are applied to front panel D-type connector J2. The synchro signals (S1-S4) and reference signals (RH and RL) are input to isolation relays K13, K14, and K15. When closed the isolation relays connect the synchro input signals (S1-S4) and reference input signals (RH and RL) to the S/D Converter circuits. (Refer to paragraph 2-3 for a detailed discussion of the S/D Converter circuitry.) The output signals of the S/D Converter circuitry are read by Local Microprocessor U19 which transmits angle data via the VXI interface bus to the host.

2-2.2 Digital-to-Synchro Converter. The Model 5388 can simulate synchro and resolver signals for numerous applications. The simulated synchro and resolver signals are output from front panel D-type connector J1. The synchro signals (S1-S4) and reference signals (RH and RL) are isolated by isolation relays K2, K1, and K4. When closed the isolation relays connect the synchro output signals (S1-S4) and reference input signals (RH and RL) to output connector J1. The D/S Converter data is organized by Local Microprocessor U19 which receives signal simulation setup instructions via the VXI communications bus from the host.

2-2.3 Local Microprocessor. The Local Microprocessor U19 is a MC68000 microprocessor which operates at 8 MHz and has asynchronous 16-bit data and 24-bit address buses. It interfaces with all the required external logic for interrupt, address bus, data bus, and data transfer control. The microprocessor handles all communications between the VXIbus interface, the host, and the S/D and D/S Converter circuitry. It also processes calibration data and utilizes it to correct S/D input angle and D/S output angle errors.

2-2.4 VXIbus Interface. The VXIbus interface bus contains the necessary configuration registers, interrupt generators, and data registers for communicating angle position indications and angle simulations to and from the host.

2-2.5 Test Reference Generator. The Test Reference Generator is a fixed sinewave oscillator which produces a 400 Hz sinewave. The sinewave output signal is used for self-testing purposes.

2-3 S/D CONVERTER CIRCUITRY (figure 2-2)

The S/D Converter circuitry is designed with an NAI closed servo loop (refer to schematic diagrams 8-1 and 8-2). This system continuously tracks the analog input data with a precision electronic Scott-T transformer, sine and cosine multiplier D/A converters, phase detector, integrator, interrupt generator, and Digital Signal Processor (DSP).

When the Model 5388 is in the Resolver mode, signals input to J2 pass through isolation relays K13, K12 and K14. The signals are sent directly to sine and cosine differential amplifier circuitry (U72 and U73) which reduce the signal amplitude to enable further signal processing. These differential amplifiers can be adjusted for voltage gain and common mode rejection.

The signals are inverted by amplifiers U68 (sine) and U50 (cosine) and made available to sine and cosine D/A Converters via Quadrant Selection circuitry (U60).

When the Model 5388 is selected for the Synchro mode, input signal APIS1 is switched into the cosine differential amplifier (U67-3) through relay K15. The output of amplifier U67 attenuates signals APIS2 minus APIS1.

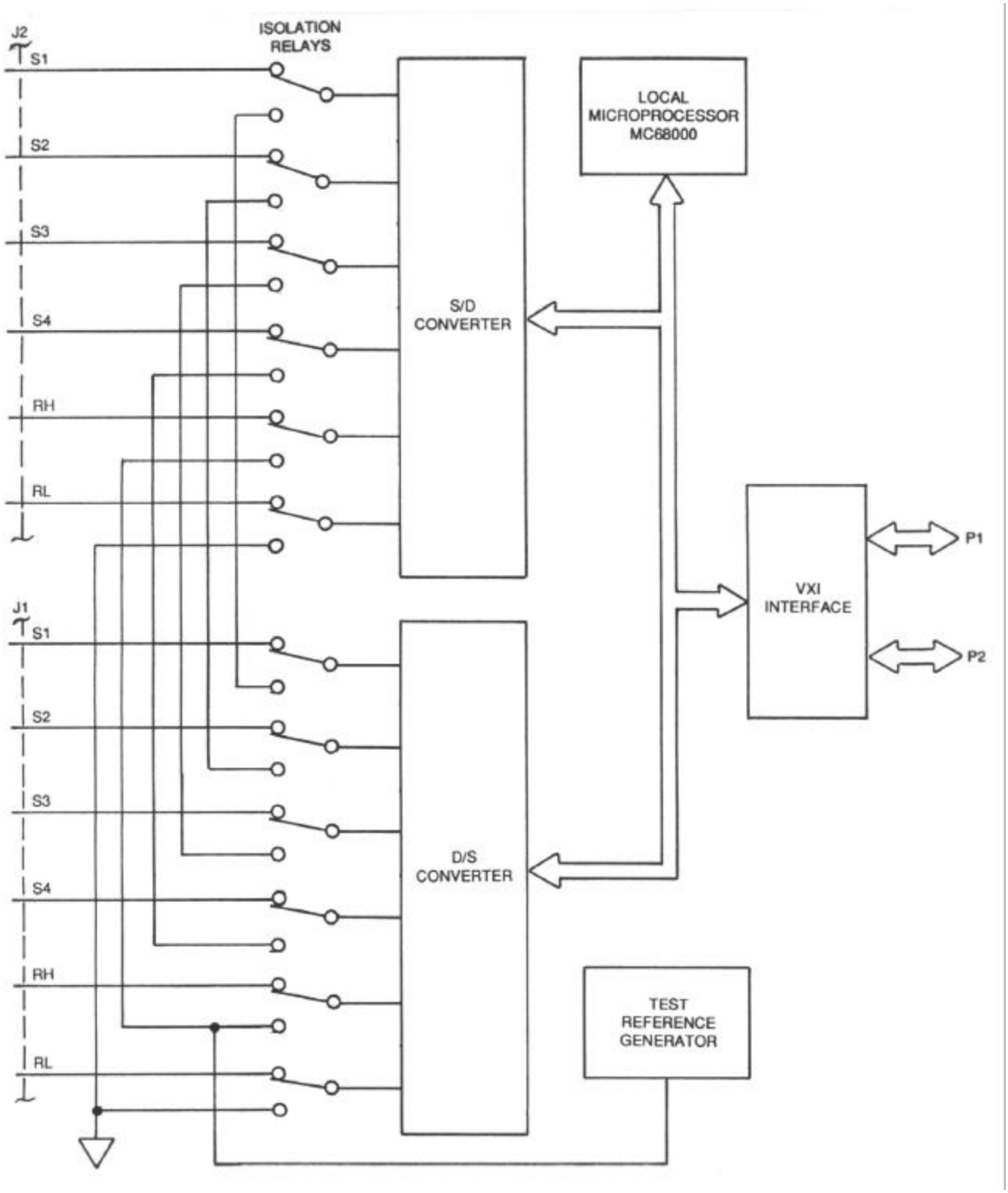


Figure 2-1. Model 5388, Overall Block Diagram

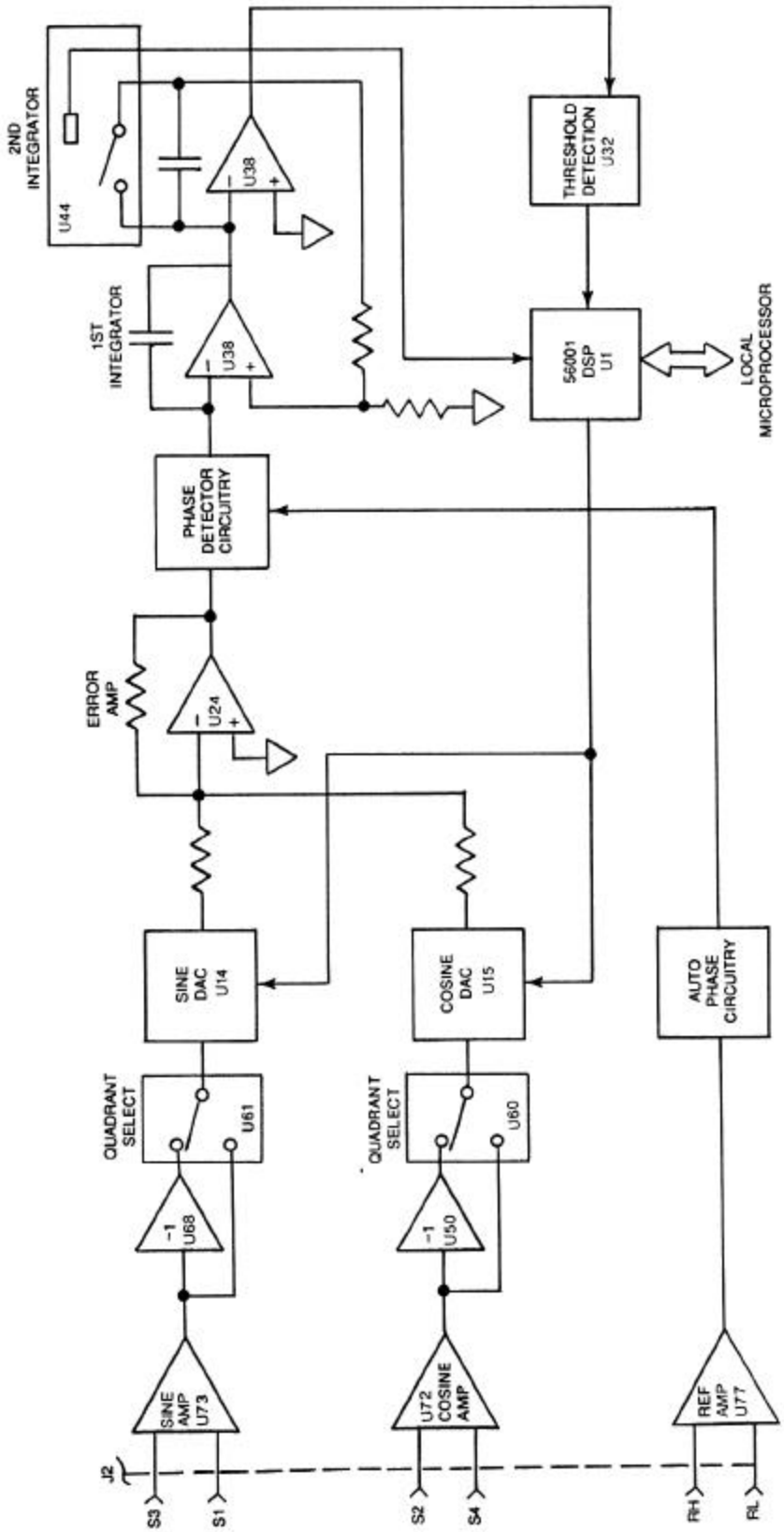


Figure 2-2. S/D Converter, Block Diagram

When this signal is combined in amplifier U67 with signal SIN q, signal COS q is generated. Signals SIN q and COS q are fed to sine and cosine multiplier D/A converters (U14 and U15). Sine and cosine D/A converters and error amp (U24) provide the following trigonometric function:

SIN q COS q - COS q SIN a = SIN(q - a) = ERROR SIGNAL

where: q is the input shaft angle
a is the internally generated angle

When the two angles are equal to zero the Error Signal level goes zero.

The Error Signal level is amplified, depending upon the line-to-line voltage input, by a gain configured D/A Converter U36. The gain is calculated by the micro-processor which maintains a constant sensitivity level of 2 V per degree at the output of gain D/A Converter U36.

The Error Signal output of gain D/A Converter U36 is applied to the Null circuitry. This circuit has two main functions: Phase Sensitive Detection and Interrupt Generation.

2-3.1 Phase Sensitive Detection Circuit. The Phase Detection circuit consists of an inverting amplifier (U38) and an analog switch (U44). The Error Signal is full wave detected when the analog switch is switched by the internally generated Reference squarewave signal REFSQR.

In most S/D Converters, the Reference signal to the Null circuit is supplied externally from the same signal source that excites the synchro. Since all synchros generate phase shift, their output signal is phase shifted in respect to the Reference signal (usually 5° to 10°). For optimum performance, the Reference signal applied to the S/D Converter should be phase shifted by the same amount as the synchro signal. The Model 5388 API contains an autophase circuit which eliminates the need for external Reference signal correction. This circuit can correct up to ± 80° of Synchro phase shift.

Phase correction is obtained by deriving an internal Reference squarewave from the synchro signals. This is accomplished by first selecting the larger of either the sine signal or cosine signal. Amplifier U45 and associated components form two full wave rectifiers. Their output signals are compared by Comparator U74. The larger of the two signals (sine or cosine) is routed through analog switch U70 and inverted by inverter amplifier U51. Analog switch U61 forms a Phase Sensitive Detector which is switched by the external Reference signal squared up by Cmparator U77. Comparator U74 determines whether the internal signal or its inverted version are inphase with the external signal. The most inphase signal of the two is routed to Comparator U77 which converts the sinewave signal to a squarewave. This signal (REFSQR) is sent to the Null circuitry.

2-3.2 Interrupt Generator Circuit. After phase detection is accomplished the Error Signal is sent to the first and second integrator amplifier circuitry (U38). Analog switches U31, U44, and U25 switch the timing components to form two null circuits which accommodate two different frequency speeds: high and low frequencies. (The low frequency circuit provides more filtering but lower speeds.)

When the voltage output of the second integrator amplifier circuit exceeds the threshold voltage set by R31 and Z23 or R30 and Z23, Comparator U32 generates one of two interrupts (A or B) to the DSP. If signal -IRQA is set the current angle is *incremented* by .001° within the DSP. If signal -IRQB is set then the angle is *decremented* by .001°. After the angle increment and decrement process new sine and cosine values are calculated and applied to sine and cosine multiplier D/A Converters U14 and U15.

This process of phase detection and interrupt generation continues as the DSP tries to drive the Error Signal to zero. When the error voltage is close to zero the Model 5388 API has determined the input angle or is producing the same angular rate that the input signals have.

2-4 D/S CONVERTER CIRCUITRY (Figure 2-3)

The D/S Converter circuitry consists of an input stage, scaling Digital-to-Analog Converter (DAC) circuit, sine and cosine D/A Converters, and power amplifiers (refer to schematic diagrams 8-1 and 8-2).

Reference input signals are processed through Differential Input Attenuator amplifier circuit U28. This circuit reduces any large input reference voltages down to usable levels. Relay K11, DAC U30, and amplifier U29 form a programmable scaling DAC Gain/Attenuator circuit. By amplifying or attenuating the input signal (via DAC input code DB0-DB13), any output voltage ranging from 2 V to 90 V can be derived from any input voltage ranging from 2 V to 115 V.

The output signal is inverted by U34 and both signal polarities are then made available for the sine and cosine D/A Converters via the Quadrant Selection circuitry. Quadrant Selection circuitry (U43) selects and amplifies (U59) the Reference signal or inverted Reference signal for each DAC depending upon the programmed angle data.

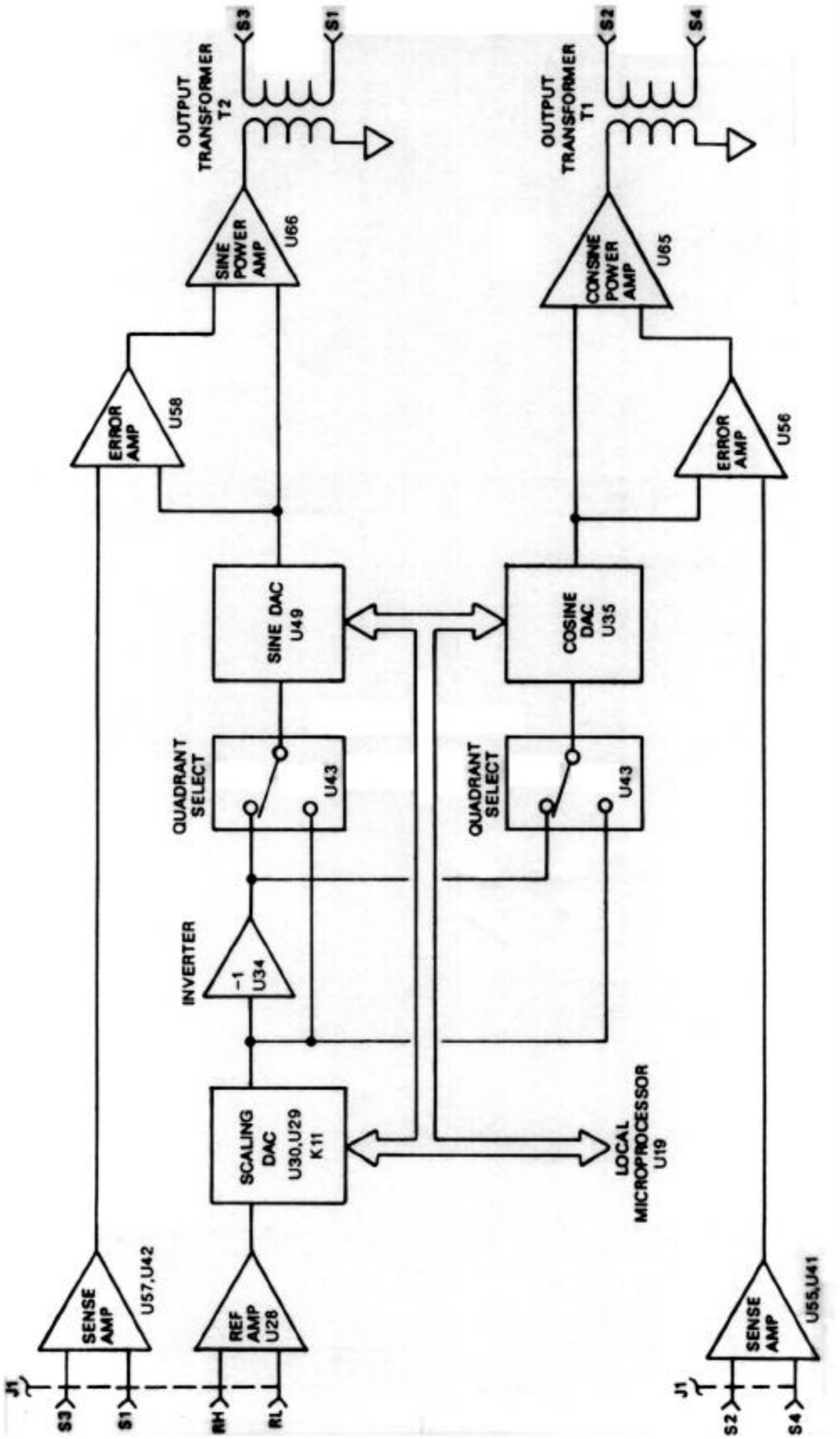


Figure 2-3. D/S Converter, Block Diagram

U49 (sine) and U35 (cosine) are multiplying D/A Converters and are programmed by MC68000 microprocessor U19. Sine DAC U49 is programmed to the sine of the commanded angle and cosine DAC U35 is programmed to the cosine of the commanded angle.

The sine and cosine DAC signals are sent to separate sine and cosine output amplifiers. These output amplifiers employ feedback to reduce loading errors. U57 and U55 are Sense Input stages that sense the *output voltage* of Output Transformers T1 and T2. The output voltages are amplified further by amplifiers U42 and U41 depending upon which T1 or T2 Transformer tap is in use. These signals are compared to the multiplier DAC signals being input to Power Amplifier Stages U66 and U65 by Error Amplifiers U58 and U56. The output error signal is then summed into the input of the sine or cosine Power Amplifier Stage to correct the final output signal. Power Amplifiers U66 and U65 drive Output Transformers T1 and T2 which, in turn, step up the final output signal depending upon which output transformer tap is selected.

2-5 MICROPROCESSOR SECTION FUNCTIONAL DESCRIPTION

The purpose of the microprocessor section is to control the overall operation of the Model 5388 by means of internal system software programs.

The microprocessor section contains the following circuitry:

a. MC68000 microprocessor
b. Reset/halt logic
c. Address, data, and control buffers
d. Address decode logic
e. Data transfer acknowledge logic
f. Bus error generation logic
g. Interrupt handling logic
h. Programmable Timer Module (PTM)
i Status buffer
j. Memory

These various circuits and their operation are described in the following subparagraphs.

2-5.1 MC68000 Microprocessor. The MC68000 is a 16-bit microprocessor (U19) which operates at 10 MHz and controls the overall functions of the Model 5388. The microprocessor contains asynchronous 16-bit data and 24-bit address busses as shown in figure 2-4. The signals used are described in the following subparagraphs.

2-5.1.1 Address Bus (MA1 - MA23). This 24-bit bus provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines MA1, MA2, and MA3 determine which interrupt level is being serviced.

2-5.1.2 Data Bus (MD0 - MD15). This is the general purpose data path into and out of the microprocessor. It can handle data in either word (16-bit) or byte (8-bit) lengths.

2-5.1.2.1 Address Strobe (-MAS). This signal indicates that there is a valid address on the address bus.

2-5.1.2.2 Read/Write (-MWRITE). This signal defines the data bus transfer as a Read cycle (-MWRITE = 1) or Write cycle (-MWRITE = 0) and works along with the data strobes.

2-5.1.2.3 Upper and Lower Data Strobes (-UDS, -LDS). These signals control the flow of data on the data bus and also help determine the state of the internal address line (MA0). When -UDS is active low (0), the upper data byte will be active. Likewise, when -LDS is active low (0), the lower data byte will be active. Thus, word (16-bit) accesses will occur on only even addresses, while byte (8-bit) accesses can occur on even or odd addresses.

2-5.1.2.4 Data Transfer Acknowledge (-MDTACK). This input indicates that the data transfer is completed. During read cycles the occurrence of -MDTACK causes the data to be latched and the bus cycle terminated. During write cycles it causes the bus cycle to terminate.

2-5.1.2.5 Interrupt Control [-IPL(0), -IPL(1), -IPL(2)]. These inputs indicate the encoded priority level when a device requests an interrupt. Level seven is highest and unmaskable; level zero indicates no interrupt.

2-5.1.2.6 Bus Error (-MBERR). This input informs the microprocessor that a problem exists with the current cycle being executed.

2-5.1.2.7 Reset (-MRESET). This is a bidirectional signal that starts a system initialization sequence in response to an external reset signal. An internal reset may be generated by execution of the RESET instruction. A total system reset is the result of external -MHALT and -MRESET signals applied at the same time.

2-5.1.2.8 Halt (-MHALT). When this bidirectional signal is driven low, it will cause the processor to stop at the completion of the current bus cycle.

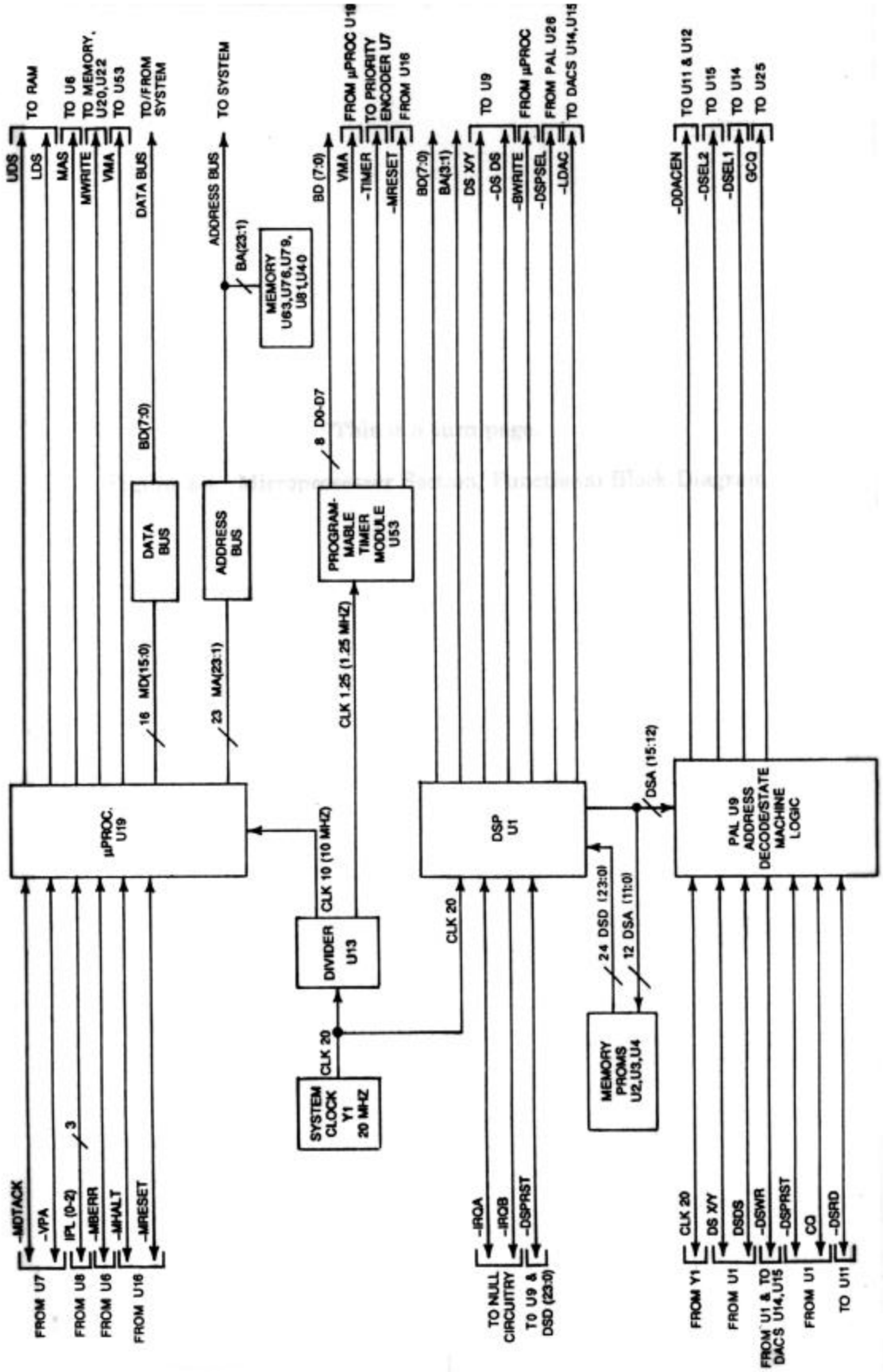


Figure 2-4. Microprocessor Section, Functional Block Diagram

2-5.1.2.9 Enable (ECLK). This signal is the standard M6800 type peripheral device enable signal. It is running at 1 MHz (six clock pulses low, four clocks pulses high).

2-5.1.2.10 Valid Peripheral Address (-VPA). This input indicates that the MC68A40 PTM has been addressed and that data transfer should be synchronized with the Enable (ECLK) signal. This input also indicates that the processor should use automatic vectoring when an interrupt occurs. -VPA is generated by the data transfer acknowledge logic.

2-5.1.2.11 Valid Memory Address (-VMA). This output is used to indicate to the PTM that there is a valid address on the address bus and the processor is synchronized to Enable (ECLK). This signal responds to a -VPA input which indicates that the peripheral is an M6800 device.

2-5.1.2.12 Processor Status [FC(2:0)]. These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed. The information is valid whenever -MAS is active. When all three outputs are high the microprocessor is executing an interrupt acknowledge cycle.

2-5.1.2.13 Clock (CLK10). The clock input is a 10 MHz signal used for development of the internal clocks needed by the processor.

2-5.2 Reset/Halt Logic. The reset/halt logic (U16A, U16B, U16C, Z2A) receives the master reset signal (-DEVRST) from the VXI Daughterboard (A2) and generates -MHALT for the microprocessor and -MRESET for the microprocessor and the PTM.

2-5.3 Address, Data, and Control Buffers. The microprocessor address bus MA(23:1) is buffered by octal buffers U18, U27, and U23 to become signals BA(23:1). BA(0) exists only for logic simulation purposes.

Data bus signals MD(15:0) are buffered by octal bus transceivers U20 and U22 to become BD(15:0). Data flows in the direction MD(15:0) -> BD(15:0) during a write cycle (MWRITE = high) and in the direction MD(15:0) <- BD(15:0) during a read cycle (MWRITE = 0).

Octal buffer U33 is used to buffer the following control signals: -MAS (becomes -BAS), -MWRITE (-BWRITE), and ECLK (BECLK). Inverter U10 buffers and inverts the remaining control signals: -UDS (becomes UDS), -LDS (LDS), -MAS (MAS), -MWRITE (MWRITE), and -VMA (VMA).

2-5.4 Address Decode Logic. The address decode logic consists of PALs U39 and U26. They accept as inputs buffered address lines BA(23:15), buffered read/write line -BWRITE, modified write enable pulse -WE, and buffered address strobe -BAS.

The PALs output device select signals to memory (-EPROM, -RAM, and -E2PROM), to the VXI Daughterboard (A2) data low register (-MR0EEN), to the DSP (-DSPSEL), to the status buffer (-STATUS), to the PTM (-MC6840), to the D/A converters (-SINDAC, -COSDAC, -LLDAC, and -GAINDAC), to the D/A bus buffers (-MDACEN), and to the data transfer acknowledge logic (-LMDSEL, -MMDSEL, -E2PROM, and -MC6840). They also output write signals to the VXI Daughterboard (A2) (-VXICTL0, -VXICTL1, -MR0ECK, and -TEST), to the DSP reset control flip-flop (-DSPCTL), to the DSP (-DSPSEL), to the relay control port (-RELAYS), and to the D/A converters (-SINDAC and -COSDAC).

2-5.5 Data Transfer Acknowledge Logic. The data transfer acknowledge logic consists of PAL U7 which contains an internal shift register. At the start of a bus cycle the microprocessor will place an address on MA(23:1) which is buffered and becomes BA(23:1). Buffered address strobe (-BAS) will then be asserted and received by the shift register. This shifted address strobe will be combined with the select signals from the address decode logic (-LMDSEL, -MMDSEL, and -E2PROM) to create the data transfer acknowledge (-MDTACK) signal. This signal indicates that the data transfer is completed.

During read cycles the occurrence of -MDTACK causes the data to be latched and the bus cycle terminated. During write cycles it causes the bus cycle to terminate. The shift register creates different delays for -MDTACK based on the access speed of the various devices connected to the microprocessor buses.

PAL U7 also generates a shortened Write Enable pulse (-WE) with a width determined by the number of wait states used by the internal -MDTACK shift register. -WE is used by the address decode logic and the memory to ensure that data is stable when a write occurs.

2-5.6 Bus Error Generation Logic. The bus error signal (-MBERR) is generated by quad flip-flop U6. U6 counts BECLK pulses that occur after MAS becomes asserted. If MAS is still asserted after four rising edges of BECLK (between 3 and 4 micro-seconds), U6 will generate error signal -MBERR.

2-5.7 Interrupt Handling Logic. The interrupt handling logic must prioritize incoming requests and generate interrupt acknowledge signals back to the interrupt sources. Interrupt prioritization is accomplished with an 8-to-3 Priority Encoder (U8). The inputs to U8 are: (1) -INTVRD, VXI read interrupt; (2) -INTVWR, VXI write interrupt; and (3) -TIMER, PTM interrupt. Whenever one or more of these inputs is active low, a binary code for the highest priority input will be output to the micro-processor on lines -IPL(2:0). -TIMER is the highest priority input and -INTVRD is the lowest.

When an interrupt request is made to the micro-processor it is made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is greater than the current processor priority, the microprocessor places the interrupt level on address lines MA(3:1), sets all the microprocessor status bits FC(2:0) high, and asserts the address strobe, -MAS. PAL U7 generates -VPA by decoding the microprocessor status bits and the buffered address strobe, -BAS. Since -VPA is asserted the microprocessor will then use an internally generated vector that is a function of the interrupt being serviced; this is known as "autovectoring".

PAL U7 also generates an interrupt acknowledge signal, -IACKEN, by decoding the microprocessor status bits and the buffered address strobe, -BAS. -IACKEN is used in conjunction with buffered address lines BA(3:1) to create interrupt acknowledge signals for the various interrupts by a 3-to-8 Demultiplexer (U17). The microprocessor will then branch to the interrupt service routine pointed to by the interrupt vector.

2-5.8 Programmable Timer Module (PTM). The PTM (U53) is used to generate time delays and interrupts as required by the system software. It receives two clocks: BECLK (1 MHz) from the micro-processor, and CLK1.25 (1.25 MHz) from the DSP clock generation logic. Either clock may be used to generate the delays and interrupts.

2-5.9 Status Buffer. The status buffer consists of parts of two octal buffers (U62 and U33) and is a Read Only Memory location used to test for various conditions relevant to the operation of the instrument. The information available by reading the buffer is as follows: VXI interrupt pending, default VXI interrupt level, VXI -WRRDY signal, VXI -RDRDY signal, API stability, high/low frequency unit, and calibration/normal operation mode.

2-5.10 Memory. The memory consists of the following: two 64K x 8 bit Ultraviolet Erasable Programmable Read Only Memories (UVEPROMS - U63 and U76) organized as 64K x 16 bits, two 8K x 8 static random access memories (SRAM - U79 and U81) organized as 8K x 16 bits, and one 8K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM - U40).

2-6 DIGITAL SIGNAL PROCESSOR (DSP) SECTION FUNCTIONAL DESCRIPTION

The DSP is a dedicated microprocessor optimized to perform floating point calculations. It calculates the sine and cosine values of the Model 5388 API and SIM (figure 2-4).

The Digital Signal Processor Section contains the following circuitry:

a. DSP56001 Digital Signal Processor
b. Clock Generation Logic
c. Address Decode/State Machine Logic
d. Memory

The various circuits and their operation are described in the following subparagraphs.

2-6.1 Digital Signal Processor (DSP). The DSP (U1) is a Motorola DSP56001 operating at 20 MHz. As used in the 5388 it contains 512 words of 24-bit program RAM, an 8-bit parallel host interface port, and a 9bit general purpose parallel port. The host interface port appears as several memory locations in the microprocessor address space. The DSP signals used are described in the following subparagraphs.

2-6.1.1 Address Bus [DSA(15:0)]. This 16-bit bus specifies the address for external program and data memory accesses.

2-6.1.2 Data Bus [DSD(23:0)]. This 24-bit bus is the general purpose data path for external program and data memory accesses.

2-6.1.3 Data Memory Select (-DSDS). This output is asserted only when external data memory is referenced.

2-6.1.4 X/Y Select (DSXY). This output selects which external data memory space (X or Y) is referenced by data memory select (-DSDS).

2-6.1.5 Read Enable (-DSRD). This output is asserted to read external memory on the data bus [DSD(23:0)].

2-6.1.6 Write Enable (-DSWR). This output is asserted to write external memory on the data bus

[DSD(23:0)].

2-6.1.7 Mode Select A/External Interrupt Request A (-IRQA) and Mode Select B/External Interrupt Request B (-IRQB). These two inputs have dual functions:

a. To select the initial chip operating mode.
b. To receive an interrupt request from an external source.

Mode Select A and Mode Select B are latched in the DSP when the reset line (-DSPRST) transitions from low to high. After leaving the Reset state, the Mode Select A and Mode Select B pins automatically change to External Interrupt Request A and External Interrupt Request B.

2-6.1.8 Reset (-DSPRST). This signal when asserted, initializes the DSP. When negated, the initial DSP operating mode is latched from the Mode Select A and Mode Select B pins.

2-6.1.9 Extal (-CLK20). This is the clock input which receives a 20 MHz signal used for development of the internal clocks needed by the DSP.

2-6.1.10 Host Data Bus [BD(7:0)]. This bidirectional data bus is used to transfer data between the MC68000 microprocessor and the DSP.

2-6.1.11 Host Address [BA(3:1)]. These inputs provide the address selection for each Host Interface register within the DSP.

2-6.1.12 Host Read/Write (-BWRITE). This input defines each host processor access as a Read cycle (-BWRITE = 1) or Write cycle (-BWRITE = 0). It works with the HOST ENABLE input data transfer function.

2-6.1.13 Host Enable (-DSPSEL). This input enables a data transfer on the host data bus. When -DSPSEL is asserted and -BWRITE is high, the HOST DATA BUS becomes an output and the DSP date may be read by the microprocessor. When -DSPSEL is asserted and -BWRITE is low, the HOST DATA BUS becomes an input and the microprocessor data is latched inside the DSP when -DSPSEL is negated. -DSPSEL is generated by the microprocessor address decode logic.

2-6.2 Clock Generation Logic. The master clock (CLK20) is generated by 20 MHz oscillator Y1. Gate U4 insures that the clock meets the voltage level requirements of the DSP. CLK20 is divided by 2 to generate a 10 MHz clock (CLK10) which goes to Microprocessor U19 and to the data transfer acknowledge logic. CLK20 is also divided by 16 to generate a 1.25 MHz clock (CLK1.25) which goes to the Programmable Timer Module (U53).

2-6.3 Address Decode/State Machine Logic. The address decode/state machine logic consists of PAL U9. It accepts as inputs address lines DSA(15:12), data memory select -DSDS, X/Y select DSXY, read enable -DSRD, write enable -DSWR, reset -DSPRST, and buffered master clock -CLK20. It outputs device select signals to memory (DSROM) and to the API Bridge sine and cosine DACs (-DSEL1 and -DSEL2) and an enable signal to the DAC data bus buffer (-DDACEN).

The state machine generates the required pulse widths for -DSEL1 and -DSEL2 based upon whether the DSP is performing a read or a write of the sine and cosine DACs. PAL U9 also serves as a programmable inverter for the cosine quadrant input signal CQ based on control input signal ASYN (API synchro/resolver mode).

2-6.4 Memory. The memory consists of three 4K x 8-bit Programmable Read Only Memories (PROMs - U2, U3, and U4) organized as 4K x 24-bits. These PROMs contain sine and cosine data for the API.

2-7 VXIbus OVERALL DESCRIPTION

The VXI section is located on a separate circuit card (A2) which mounts on to the motherboard (figure 8-2). Its purpose is to provide communication between the VXIbus and the instrument, and it is configured as a message based servant. All communications take place using the VXIbus Message Based device protocols. The VXIbus consists of four busses:

a. Data Transfer Bus (DTB)
b. Priority Interrupt Bus
c. Arbitration Bus
d. Utility Bus

The signals used from each bus are described in the following paragraphs.

NOTE

Refer to document entitled "VXIbus System Specifications Revision 1.3" dated 7/14/89 for additional information.

2-7.1 Data Transfer Bus. The VXIbus includes a high speed asynchronous parallel Data Transfer Bus (DTB). Controller devices use the DTB to select storage locations provided by Servant devices, and to transfer data to and from those locations. Some Controller and Servant devices use all the DTB lines, while others use only a subset.

2-7.1.1 Address Bus A(15:1). This 15-bit bus provides the address for selecting the device and its internal registers. The base address of the device's internal registers is determined by the device's Logical Address. The Logical Address is indicated by the value of the eight address bits A(13:6). Address bits A(15) and

A(14) are always high, and the base address is

LA * 64 + 49152

where: LA is the device's Logical Address. (The internal registers are discussed in paragraph 2-9.)

2-7.1.2 Address Modifier AM(5:0). The address modifier lines allow the Controller device to pass additional binary information to the device during data transfers. The address modifier lines must have a value of either 29H or 2DH in order for the data transfer to take place.

2-7.1.3 Data Bus D(15:0). This is the general purpose data path into and out of the VXI section. It can handle data in either word (16-bit) or byte (8-bit) lengths.

2-7.1.4 Address Strobe -AS. A falling edge on this signal line indicates to the device that the address is stable on the VXI address bus and can be captured.

2-7.1.5 Data Strobe Zero/One -DS0/-DS1. These signals select byte locations for data transfer. When -DS0 is low, data is transferred on the lower or odd byte. When -DS1 is low, data is transferred on the upper or even byte. Both strobes may be active at the same time. The data strobe and associated byte nomenclatures are summarized in table 2-1.

Table 2-1. Data Strobe Zero/One Nomenclature

-DS1	-DS0
D(15:8)	D(7:0)
EVEN	ODD
BYTE(0)	BYTE(1)

The data strobes serve additional functions. During write cycles, the first data strobe falling edge indicates when the Controller device has placed valid data on the data bus. On read cycles, the first data strobe rising edge tells the slave device when it can remove data from the data bus.

2-7.1.6 Data Transfer Acknowledge -DTACK. The device drives -DTACK low to indicate that it has successfully received the data during a write cycle. On a read cycle, the device drives -DTACK low to indicate that it has placed data on the data bus.

2-7.1.7 Bus Error -BERR. This signal is not currently used by the VXIbus hardware. It is connected to the VXIbus section for troubleshooting purposes only. Signal -BERR is driven low to indicate that the data transfer has failed. For example, if a Controller device tries to access a nonexistent device, a -DTACK would never occur and therefore the Bus Timer on the Controller device would drive -BERR low after a specified period of time.

2-7.1.8 Read/Write -WRITE. This signal defines the data transfer as a read cycle (-WRITE = 1) or write cycle (-WRITE = 0). During a read cycle, the data direction is from the device to the Controller. During a write cycle, the data direction is from the Controller to the device.

2-7.1.9 Longword -LWORD. This signal is not currently used by the VXIbus hardware. It is connected to the VXI section for troubleshooting purposes. It will be driven low by the Controller device during quad byte transfers. Since the VXI section does not support this type of data transfer, it should never be low while the device is selected.

2-7.2 Priority Interrupt Bus. The VXIbus includes a Priority Interrupt Bus (PIB) which provides the signal lines needed to generate and service interrupts. INTERRUPTERS use the PIB to send interrupt requests to INTERRUPT HANDLERS which respond to these requests.

2-7.2.1 Interrupt Request Lines -IRQ(7:1). The device requests interrupts by driving one of the interrupt request lines low. Typically, -IRQ(7) has the highest priority.

2-7.2.2 Interrupt Acknowledge -IACK. The -IACK signal is driven by an interrupt handler, typically located on the Slot 0 Controller device, when it has been given control of the VXIbus in response to the assertion of one of the interrupt request lines.

2-7.2.3 Interrupt Acknowledge Daisy-Chain -IACKIN/-IACKOUT. Each of the seven interrupt request lines may be shared by more than one interrupter. The interrupt acknowledge daisy-chain prevents more than one interrupter from responding to an interrupt acknowledge cycle. When the IACK DAISY-CHAIN DRIVER, located on the Slot 0 Controller device, senses that the -IACK line has gone low, it will drive its -IACKOUT line low. This line is connected to the -IACKIN line of the next slot, Slot 1. The -IACKOUT line of Slot 1 is connected to the -IACKIN line of Slot 2, and so on through the rest of the slots in the card cage. (Slots that are empty should have their -IACKIN line shorted to their -IACKOUT line in order to propagate the interrupt acknowledge signal to the next slot.) If a device senses -IACKIN low but has not requested an interrupt of the level being acknowledged then it, in turn, will drive its -IACKOUT line low. If a device senses -IACKIN low and has requested an interrupt of the proper level then it will not drive its -IACKOUT line low. This prevents other devices from responding to the interrupt acknowledge cycle.

2-7.3 Arbitration Bus. There are no signals used from this bus.

2-7.4 Utility Bus. The Utility Bus supplies periodic timing, initialization and diagnostic capability for the VXIbus. The following paragraphs identify and define the signal lines and modules which provide utility functions for the VXIbus.

2-7.4.1 System Clock SYSCLK. The system clock is an independent, 16 MHz, 50 percent duty cycle square wave. It has no fixed phase relationship with other VXIbus timing. Signal SYSCLK is buffered by octal buffer U5 and then goes to counter U18 where it is divided by two to create an 8 MHz clock (CLK8). Signal CLK8 is used to generate timing within the VXI section. It goes to the sequencer register U15, to the sequencer U20, and to the interrupt shift register U25.

2-7.4.2 System Reset -SYSRESET. This open-collector signal is driven low, typically by the Slot 0 Controller device, for a minimum of 200 milliseconds to reset the system.

2-7.4.3 System Failure -SYSFAIL. This open-collector signal is driven low by the device at power-up. It will be released if the device successfully passes self-test, or if the device fails self-test and the Sysfail Inhibit bit is set in the device's Control Register. The Control Register is described in paragraph 2-9.4.

2-7.4.4 Module Identification MODID. This signal is used to determine the slot location of the device. The Slot 0 Controller has a separate MODID line for each slot in the card cage. By asserting a particular MODID line and then reading the Status Register of each device, the slot location of each device can be determined. The Status Register is described in paragraph 2-9.3.

2-8 VXIbus FUNCTIONAL DESCRIPTION

Throughout this discussion reference will be made to figure 2-5, the VXI Sequencer State diagram. This diagram describes the sequence of events as defined by Sequencer U20 and is explained by the following example.

> A particular state is represented by two characters, a comma, and then a third character as in (27,A).
>
> The first two characters are the hex value of the six output control pins: -SAS, U20 pin 14; -VDBEN, U20 pin 21; -VWR, U20 pin 22; -VRD, U20 pin 15; -VDTACK, U20 pin 16; and -IACKRST, U20 pin 23. -SAS is the most significant bit and -IACKRST is the least significant. Therefore, for this example, the first two characters "27" represent the fact that -VDBEN and -VWR are low, and -SAS, -VRD, -VDTACK, and -IACKRST are all high.
>
> The third character is the hex value of the four state pins: -S(3), U20 pin 17; -S(2), U20 pin 18; -S(1), U20 pin 19; and -S(0), U20 pin 20. -S(3) is the most significant bit and -S(0) is the least significant bit. Therefore, for this example, the third character "A" represents the fact that -S(2) and -S(0) are low, and -S(3) and -S(1) are high.

2-8.1 Power-On Reset Sequence. At power-up the VXI Sequencer will enter state (00,0). On subsequent CLK8 pulses it will transition through two "do-nothing" states (29,F) and (3F,F) and then into the idle state (3F,E). It will remain in this state until the VXIbus initiates a data transfer. The data transfer starts when VXIbus control signal -AS is driven low by the Slot 0 Controller. Signal -AS is buffered by octal buffer U10 to become -VAS, which goes to U15. U15 is clocked by signal CLK8 and is used to synchronize the many asynchronous VXI events before they are presented to the sequencer. This helps remove any spurious noise from getting into the sequencer. When -VAS goes low, the next pulse of CLK8 latches it into U5, where it is then sampled by the sequencer on the next pulse of CLK8. This causes the sequencer to advance to state (3F,C), which provides a short delay for the VXI address to stabilize.

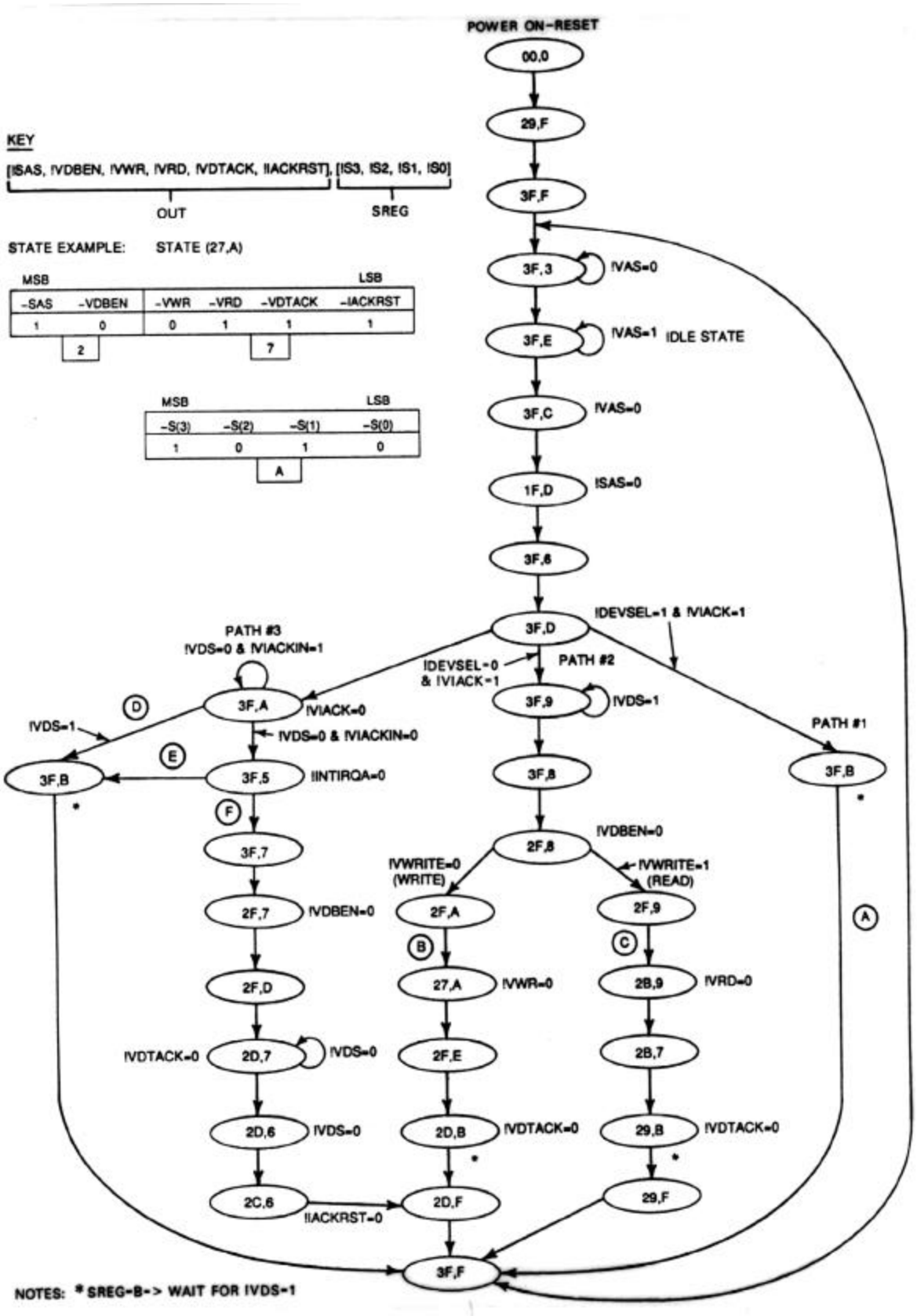


Figure 2-5. VXI Sequencer State Diagram

In the next state, (1F,D), signal -SAS is asserted by the sequencer. -SAS is a 125 nanosecond negative-going pulse which latches the VXI address A(15:1), address modifiers AM(5:0), longword flag -LWORD, and interrupt acknowledge -IACK into registers U6, U8, and U11. -SAS is deasserted in state (3F,6). While in state (3F,6), latched address bits VA(13:6) are compared to the device's Logical Address (which has been set up by switch A2SW1 on the VXI circuit card A2) by comparator U3. If the latched address bits match the Logical Address set up by the switch, then the Address Valid signal, -ADRVLD, will go low. Device selection continues with VXI board address decoder PAL U9. If latched address bits VA(15:14) are both high, -ADRVLD is low, -VAS is low, and the value of the latched address modifiers VAM(5:0) is either 29H or 2DH, then the Device Select signal, -DEVSEL, will go low.

The next state (3F,D) is the most important since it determines which of three major paths the sequencer will follow. If any of the device select criteria previously discussed has failed, indicating that the device was not selected, -DEVSEL will be high. If the latched Interrupt Acknowledge signal, -VIACK is also high, indicating that this is not an Interrupt Acknowledge cycle, then the sequencer will proceed to state (3F,B).

2-8.2 Sequencer Path #1. In state (3F,B), or any other of the form (XX,B), where X means "don't care", the sequencer will remain in the state until the latched address strobe -VAS and the combined data strobe -VDS are both high. -VDS will be high if, and only if, both buffered data strobes, -VDS0 and -VDS1, are high.

2-8.3 Sequencer Path #2. The second path will be followed if -DEVSEL is low and -IACK is high. This is a data transfer cycle to this device. The next state is (3F,9). The sequencer will remain in this state until -VDS goes low, is latched into the sequencer register U15, and is sampled by the sequencer. Typically, -VDS will go low at about the same time as -VAS and the sequencer will remain in this state for only one period of CLK8 and then continue on through state (3F,8) and into state (2F,8). In state (2F,8) the VXI Data Bus Enable signal, -VDBEN, will be asserted low. -VDBEN goes to the VXI communication control PAL U21, where it is combined with the buffered data strobes. -DS0 is buffered by U10 to become -VDS0; it is combined with -VDBEN in PAL U21 to create -VDBEN0. Likewise, -DS1 is buffered by U5 to become -VDS1, and is combined with -VDBEN in PAL U21 to create -VDBEN1. Signals -VDBEN0 and -VDBEN1 enable VXIbus transceivers U1 and U2, respectively.
The next state is determined by signal -WRITE, which is buffered by U10 (-VWRITE), latched into U15, and sampled by the sequencer. A VXI write cycle, indicated by a low level on -WRITE, will cause the sequencer to proceed to state (2F,A), and then to state (27,A). In this state the internal VXI write pulse, -VWR, is forced low. -VWR is combined with -VDS0, -VDS1, and address bits VA(5:1) in PAL U21 to generate write pulses -VR04C0, -VR0EC0, and -VR0EC1 to the VXI registers. -VR04C0 writes to the Control Register (address 04H) U16, while -VR0EC0 and -VR0EC1 write to the lower and upper bytes of the Data Low Register (address 0EH), U31 and U19, respectively. The data on the VXIbus at the time of the pulse will be written into the registers.

In the next state (2F,E), -VWR is forced inactive high, resulting in a 125 nanosecond negative pulse. In the following state (2D,B), the internal VXI data transfer acknowledge signal -VDTACK is forced low. -VDTACK is inverted by open-collector NAND gate U7B and then again by U7C, where it becomes -DTACK and goes out to the VXI bus. The sequencer will remain in state (2D,B) until -VAS and -VDS are both high, signaling the end of the cycle. It then will transition through state (2D,F) and into (3F,F) where -VDTACK is force back to its inactive high state. The sequencer will then return to the idle state (3F,E) to await the next cycle.

A VXI read cycle, indicated by a high level on -WRITE, will cause the sequencer to proceed from state (2F,8), through state (2F,9), to state (2B,9). In state (2B,9) the internal VXI Read signal, -VRD, is asserted. -VRD is combined with address bits VA(5:1) in PAL U21 to generate Read signals -VRROEN and -VR0EEN to the VXI registers. -VRROEN enables reading of the ID Register (address 00H), the Device Type Register (address 02H), the Status Register (address 04H), the Protocol Register (address 08H), and the Response Register (address 0AH). These registers are located in PALs U26/U27 and are selected by address bits VA(5:1). -VR0EEN enables reading of the Data Low Register (address 0EH) U19/U31.

The sequencer then goes through state (2B,7) and into state (29,B). In this state, the internal VXI Data Transfer Acknowledge signal -VDTACK is forced low. The sequencer will remain in state (29,B) until -VAS and -VDS are both high, signaling the end of the cycle, and then will transition through state (29,F) and into (3F,F) where -VDTACK is force back to its inactive high state. -VDBEN and -VRD will also be forced back to the inactive high state. If this was a read of the Data Low Register, then

-VR0EEN, which also goes to ready flag PAL U22, will go inactive high. The rising edge of signal -VR0EEN does two things inside of U22:

(1) it forces -RDRDY high, informing the VXIbus Slot 0 Controller that there is no longer data available in the Data Low Register and,
(2) it forces -INTVRD low, interrupting the microprocessor to tell it that the VXIbus has performed a read of the Data Low Register and that it is safe to place more data there. The VXI Sequencer will then return to the idle state (3F,E) to await the next cycle.

2-8.4 Sequencer Path #3. The third and final major path will be followed if signal -IACK is low. This initiates an interrupt acknowledge cycle. Before the state flow for the interrupt acknowledge cycle is described, an explanation of how an interrupt is handled is required and is as follows.

As part of the power-up routine, the microprocessor will read the status port on Mother CCA A1. Data bits BD(3:1) represent the binary coding of switch A1SW1-3 through A1SW1-1, which is the default VXI interrupt level. This value is written to the lower VXI control register U29 via signal -VXICTL0. When the device requires servicing via an interrupt, a logic high is written to the VXI interrupt flip-flop U17B. This forces the Q output, LIBIT, high and the QN output low. The QN output enables the interrupt decoder U14. Based on the value of the latched interrupt level from U29, IA(2:0), one of the eight outputs of U14 will go low. That low signal will propagate through open-collector buffer U12 and drive one of the interrupt request lines, -IRQ(7:1), low. The Interrupt Handler will detect that one of the interrupt request lines is low and, at the appropriate time, will drive the interrupt acknowledge line -IACK low. The Daisy-Chain Driver will respond by forcing its -IACKOUT line low. The interrupt acknowledge cycle and its sequencer state flow are described in the following paragraphs.

On the device, the sequencer detects that -IACK is low and transitions from state (3F,D) to state (3F,A). Due to VXI timing the address strobe, -AS, and the combined data strobe, -VDS, should be low. If, in state (3F,A) -VDS has gone high or goes high, then the interrupt cycle has ended (it was probably intended for another device) and the sequencer will go on through states (3F,B) and (3F,F) and back to the idle state (3F,E).

However, if -VDS remains low, the sequencer will wait for the daisy-chain signal -IACKIN to go low. -IACKIN is buffered by U10, to become -VIACKIN, and latched by U15 before it enters the sequencer. -VDS is inverted by inverter U13A to become VDS, which goes to shift register U25. U25 is held in the clear state whenever -VDS is inactive high. Signal -VIACKIN serves three functions:

(1) it tells the sequencer to exit the interrupt idle state (3F,A) and go to state (3F,5)
(2) it goes to 4-bit comparator U28 to help determine whether or not the interrupt was intended for this device
(3) it is inverted by inverter U24F and presented to shift register U25 as signal VIACKIN.

Comparator U28 checks to see if the following three criteria are all met:

(1) that the VXI address bits, VA(3:1), representing the interrupt level being acknowledged match the device's current interrupt level, IA(2:0)
(2) that the device has indeed requested an interrupt and LIBIT is high
(3) that the device's -IACKIN signal has gone low.

If they are all met, then the interrupt was intended for this device, and the Internal Interrupt Request Acknowledge signal (INTIRQA) will go high.

While the comparator function takes place, VIACKIN is shifted through U25 by CLK8. This provides a delay for the comparator to receive the latched VXI address bits, VA(3:1), and do its work. After six CLK8 pulses, IACKCLK will go high to sample INTIRQA into flip-flop U17A. If INTIRQA is high when IACKCLK occurs, then the interrupt is for this device and -IACKOUT will remain high. The device will respond with its Logical Address and the reason for the interrupt by forcing -INTIRQA low, enabling buffers U10A and U5A and register U23. If INTIRQA is low when IACKCLK occurs, then the interrupt is not for this device, and will therefore be passed down the daisy-chain by forcing -IACKOUT low.

In state (3F,5) the sequencer tests -INTIRQA. If this signal is high, the sequencer will go through states (3F,B) and (3F,F) and back to the idle state (3F,E). If -INTIRQA is low, the sequencer will go through state (3F,7) to state (2F,7) where the VXI Data Bus Enable signal, -VDBEN, will be asserted low to enable VXIbus transceivers U1 and U2. The sequencer then continues through state (2F,D) to state (2D,7). In this state, the internal VXI Data Transfer Acknowledge signal, -VDTACK, is forced low. The sequencer will remain in state (2D,7) until -VDS goes high, signaling the end of the interrupt acknowledge cycle. It will then transition through

state (2D,6) and into (2C,6) where -IACKRST is forced low to clear the interrupt bit, LIBIT, via U4C. The sequencer will then go through states (2D,F) and (3F,F) and return to the idle state (3F,E) to await the next cycle.

The VXI registers supported are described in the following paragraphs.

2-9 VXI REGISTERS

The following diagram contains the register map for the registers of the VXIbus device. These registers are located in the A16 address space by the Logical Address selector as described in paragraph 2-7.1.1.

$0E_{16}$	Data Low Register
$0A_{16}$	Response Register
08_{16}	Protocol Register
04_{16}	Status/Control Register
02_{16}	Device Type
00_{16}	ID Register

The VXIbus fields of the register map are defined in the following subparagraphs.

2-9.1 ID Register. A read of this 16-bit register provides information about the device's configuration. Its contents are defined as follows:

Bit #	Contents
15 <- 14	Device Class
13 <- 12	Address Space
11 <- 0	Manufacturer ID

2-9.1.1 Device Class. This field indicates the classification of the VXIbus device as follows:

Value	Class
10	Message Based

2-9.1.2 Address Space. This field indicates the addressing mode of the device's operational registers as follows:

Value	Mode
11	A16 Only

2-9.1.3 Manufacturer ID. This number uniquely identifies the manufacturer of the device. The North Atlantic Industries' ID number is: $4089_{10} = FF9_{16}$.

2-9.2 Device Type. This 16-bit register contains a device dependent type identifier. The read contents of this register are defined as follows:

Bit #	Contents
15 <- 0	Model Code

The Model Code field contains a unique card identifier which is defined by the manufacturer. In the case of an A16 only device, this field occupies all 16 bits of the Device Type register.

The model code for the Model 5388 D/S-S/D is $256_{10} = 0100_{16}$.

2-9.3 Status Register. A read of this register provides information about the Device's status as defined as follows:

Bit #	Contents
15	A24/A32 Active
14	MODID*
13 <- 4	Device Dependent
3	Ready
2	Passed
1 <- 0	Device Dependent

2-9.3.1 A24/A32 Active. This bit is always 0.

2-9.3.2 MODID*. A one (1) in this field indicates that the device is not selected via the P2 MODID line. A zero (0) indicates that the device is selected by a high state on the P2 MODID line.

2-9.3.3 Ready. This field serves two purposes:

a. After the power-on initialization sequence, a one (1) in this field in combination with a zero (0) in the *Passed* field indicates that the device has failed register initialization.
b. After the power-on initialization sequence, a one (1) in this field in combination with a one (1) in the *Passed* field indicates that the device is ready to execute its full set of operational commands.

2-9.3.4 Passed. A zero (0) in this field indicates that the device is either executing or has failed its self-test. A one (1) indicates that the self-test has successfully completed.

NOTE

The device dependent bits are always zero (0).

2-9.4 Control Register. A write to this register causes specific actions to be executed by the device.

These actions are described as follows:

Bit #	Contents
15	A24/A32 Enable
14 <- 2	Device Dependent
1	Sysfail Inhibit
0	Reset

2-9.4.1 A24/A32 Enable. A one (1) in this field enables access to the device's A24 or A32 VMEbus registers. A zero (0) disables such access.

2-9.4.2 Device Dependent. The bits in this field are available to the device designer for device and/or application specific control.

2-9.4.3 Sysfail Inhibit. A one (1) in this field disables the device from driving the SYSFAIL* line.

2-9.4.4 Reset. A one (1) in this field forces the device into a reset state.

2-9.5 Protocol Register. The read contents of this 16-bit register indicate which protocols the device supports, and indicate additional communication capabilities of the device. They are described as follows:

Bit #	Contents
15	CMDR*
14	Signal Register
13	Master*
12	Interrupter
11	FHS*
10	Shared Memory*
9 <- 4	RESERVED
3 <- 0	Dev Dep

2-9.5.1 CMDR*. A one (1) in this field indicates that the device has *Servant Only* capability. A zero (0) in this field indicates that the device has both Servant and Commander capability. This bit is a one (1).

2-9.5.2 Signal Register*. A zero (0) in this field indicates that the device has a Signal Register. This bit is a one (1).

2-9.5.3 Master*. A zero (0) in this field indicates that the device has VMEbus Master capability. This bit is a one (1).

2-9.5.4 Interrupter. A one (1) in this field indicates that the device has Interrupter capability. This bit is a one (1).

2-9.5.5 FHS*. A zero (0) in this field indicates that this device's data registers support the Fast Handshake Mode. A one (1) indicates that only the normal transfer mode is implemented. This bit is one (1).

2-9.5.6 Shared Memory*. A zero (0) in this field indicates that this device supports the optional Shared Memory protocol and implements one or both of the A24 Pointer and A32 Pointer registers. A one (1) indicates that the shared memory protocol is not supported. This bit is a one (1).

2-9.5.7 RESERVED. Reserved for future definition and must default to all ones ($3F_{16}$).

2-9.5.8 Dev Dep. These Device Dependent bits may be defined by the device's manufacturer. These bits are all zeroes (0).

2-9.6 Response Register. A read of this 16-bit register returns the status of the device's communication registers and their associated functions.

The Message Based device's Response Register indicates critical device status information. Each bit indicates a single status item as follows:

Bit #	Contents
15	0
14	RESERVED
13	DOR
12	DIR
11	ERR*
10	Read Ready
9	Write Ready
8	FHS Active*
7	Locked*
6 <- 0	Device Dependent

2-9.6.1 Bit 15. Bit 15 is always zero (0).

2-9.6.2 RESERVED. This bit is reserved for future VXIbus definition. Its value is always one (1).

2-9.6.3 DOR (Data Out Ready). A one indicates that the device is ready to output data to its Commander.

2-9.6.4 DIR (Data In Ready). A one indicates that the device is ready to accept data from its Commander.

2-9.6.5 Err* (Error). A zero (0) indicates that an error has occurred in the serial protocol (Word Serial) and has not yet been reported. The nature of the error may be read using the *Read Protocol Error* command. A one (1) indicates that no errors are pending.

2-9.6.6 Read Ready. A one indicates that its data registers contain data to be read. This bit is set when data from internal operations is available in the Data Low and Data High registers. It is cleared to zero by a

read of the Data Low Register.

2-9.6.7 Write Ready. A one indicates that this device is ready for data transfers to its data registers. This bit is set when the device is ready for a write to any of the data registers. It is cleared by a write to the Data Low Register.

2-9.6.8 FHS Active*. A zero indicates that Fast Handshakes are currently enabled for this device's Servant registers. This bit is cleared (to 0) whenever the Fast Handshake Mode is entered, and set (to 1) any time the device exits the Fast Handshake Mode. This bit is always a one (1).

2-9.6.9 Locked*. A zero indicates that the Commander of this device has *locked access* to it from other local sources (e.g., local lockout of IEEE-488). This bit is always a one (1).

2-9.6.10 Device Dependent. The bits in this field are available to the device designer for device and/or application specific status information. These bits are always zero (0).

2-9.7 Data Low Register. A write to this register is the least significant word of write data. A write to this register causes the device to execute some action based on the data written to the Data Low Register. A read of this register is the least significant word of read data.

SECTION 3

USER INTERFACE

3-1 INTRODUCTION

This section describes the installation, operation, and programming of the Model 5388 VXI Synchro/Resolver Processor using the NATIVE Mode language option.

3-2 UNPACKING AND INSPECTION

The Model 5388 has been thoroughly tested, inspected, and evaluated at the factory. Care has been taken in the design of the wrapping and packaging material to insure that no damage results from mishandling.

a. Remove the unit from the shipping container. Save container for future use in storing or shipping.

b. Visually check the contents of the shipping container against the shipping list.

c. Check for damage to unit and notify the carrier if it is damaged.

3-3 INSTALLATION INSTRUCTIONS

The Model 5388 is designed to be used in a standard VXIbus card cage. The following preliminary setup procedures must be performed before the Model 5388 can be installed. The unit has been factory tested but it is recommended that the user perform the checkout procedures listed in Section 5.

Table 3-1 and 3-2 list pin designations for front panel connectors J1 and J2.

3-3.1 Initial Setup. Before the Model 5388 can be installed the user must select the following:

a. VXIbus Card Cage Slot and Address
b. VXIbus Interrupt Priority Level

Table 3-1. J1 Pin Designations

Pin	Signal Name	Function
1	SRSS1	ü
2	SRSS2	ý Simulator Outputs
3	SRSS3	ï
4	SRSS4	þ
5	SRSRH	
6	SRSRL	} Reference Inputs
7	SPARE	
8	SPARE	
9	GND	Used for test purposes only
		ü
10	FBS1	ý Simulator Sense Inputs
11	FBS2	ï
12	FBS3	þ
13	FBS4	

NOTE: J1 mating connector: P1, 15-pin, male, D-type connector (see table 7-1).

Table 3-2. J2 Pin Designations

Pi	Signal Name	Function
1	APIS1	ü
2	APIS2	ý Angle Position Indicator
3	APIS3	ï Inputs
4	APIS4	þ
5	APIRH	Angle Position Indicator
6	APIRL	} Reference Inputs
7	SPARE	
8	SPARE	
9	GND	Used for test purposes only

NOTE: J2 mating connector: P2, 9-pin, female, D-type connector (see table 7-1).

3-3.1.1 VXI Address Selection. The Model 5388 allows the selection of 256 (0-255) VXI address locations. To set and assign a VXI address to a card slot, proceed as follows:

CAUTION

VXIbus card slot 0 cannot be used by the Model 5388. Slot 0 is reserved for a controller device only (e.g., a CPU).

a. Select desired VXI card cage slot (e.g., slot 5).
b. Locate 8-position binary switch A2SW1 and set switch for desired address (figure 3-1).

For example, to select VXI address *37* set switch A2SW1 as follows:

A2SW1 Switch Settings								Address Example	Binary Equivalent
-1 (LSB)	-2	-3	-4	-5	-6	-7	-8 (MSB)	37	0010 0101
O	C	O	C	C	O	C	C		

O = Open (HI) C = Closed (LO)

When the switch A1SW1-4 (MSB) is closed, the Model 5388 will be compatible with VXI version 1.3. When switch A1SW1-4 is open, the Model 5388 will be compatible with VXI version 2.

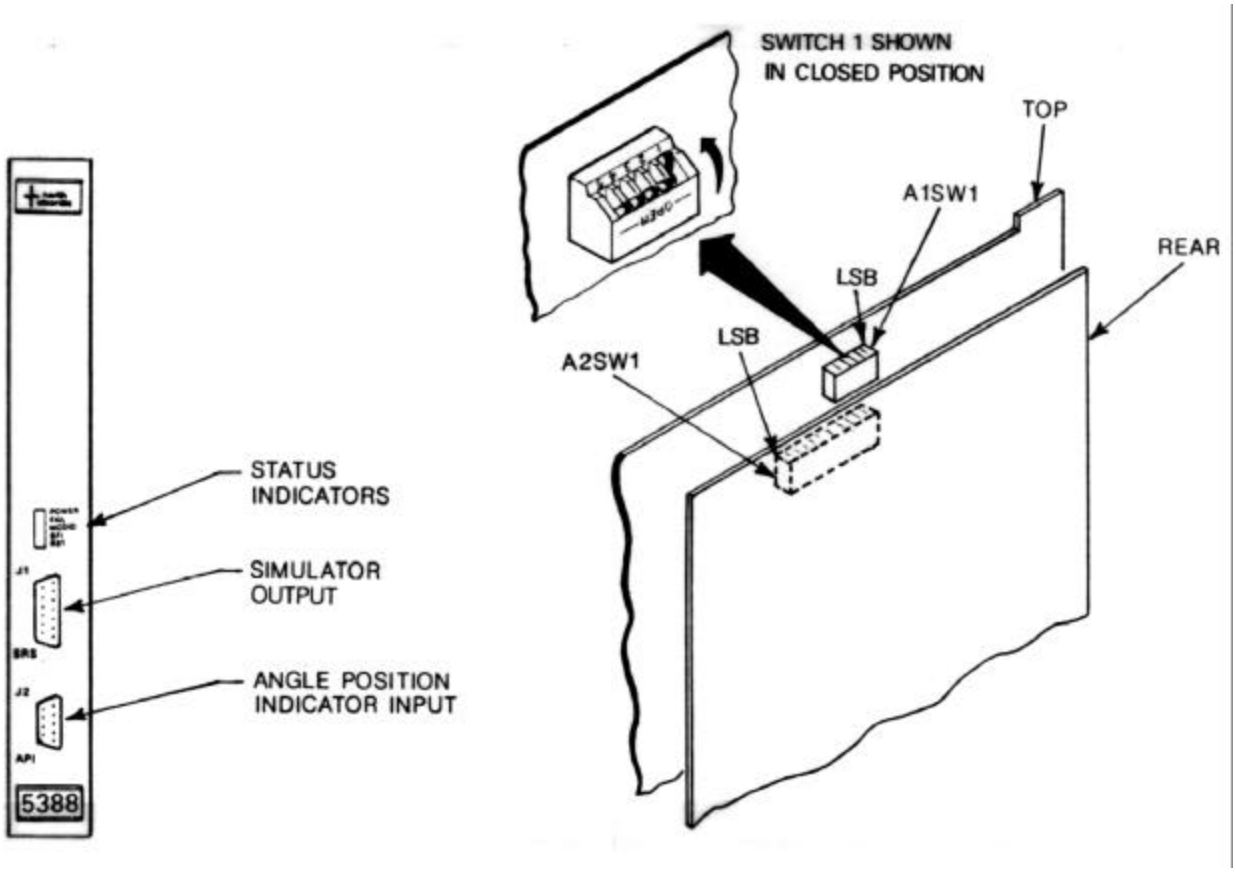


Figure 3-1. Front Panel Controls, Indicators and Setup Switch Locations

3-3.1.2 Setting VXIbus Interrupt Priority Levels. The VXIbus has seven interrupt priority levels which are selected by A1SW1 or by external VXI software commands. To select interrupt priority level set switch A1SW1 as desired (refer to table 3-3 and figure 3-1).

3-3.2 Model 5388 Installation. To install the Model 5388 into a standard VXIbus card cage, proceed as follows:

CAUTION

VXIbus card slot 0 cannot be used by the Model 5388. Slot 0 is reserved for a controller device (e.g., a CPU).

a. Set VXIbus address and interrupt priority level (refer to paragraph 3-3.1.2).
b. Turn off power to VXIbus card cage.
c. Insert Model 5388 into desired card cage slot and tighten securing screws.
d. Turn on power to VXIbus card cage.

3-3.3 Feedback Sense Jumpers. The Model 5388 Simulator has factory set internal jumpers which connect the Feedback Sense lines S1-S4 to the J1 front panel inputs (figure 3-2). The connections can be made internally or externally depending upon the desired loading accuracy.

3-3.3.1 Internal Jumper Connections. The Feedback Sense jumpers are internally set so no special wiring is needed when in the Simulator mode. If greater loading accuracy is needed, external connections are recommended.

3-3.3.2 External Connections. For optimum loading accuracy the Feedback Sense jumpers must be removed and, using external connectors, the unit should be connected directly at the load. Refer to figure 3-2 and table 3-1.

3-3.4 VXI REVISION LEVEL. The Model 5388 supports VXI Revision levels 1.2 and 1.3. The Revision level is selectable via switch A1SW1-4. When using the Model 5388 with Revision 1.2 Slot Zero Controllers set the switch to the open position. If a Revision 1.3 Slot Zero Controller is being used, set the switch to the closed position. See Figure 3-1 from A1SW1 switch location.

A1SW1-4	VXI Revision
Open	1.2
Closed	1.3

Table 3-3. VXIbus Interrupt Priority Level Switch (A1SW1)

NOTE

Once set, the position of switch A1SW1 becomes the default setting. The interrupt level may be modified using a software command. The interrupt level returns to its default setting whenever system power is cycled off to on.

A1SW1- Switch Settings			Interrupt Priority Level	Binary Equivalent
-1 (LSB)	-2	-3 (MSB)		
C	C	C	0 = No interrupt	000
O	C	C	1 = Lowest Priority	001
C	O	C	2	010
O	O	C	3	011
C	C	O	4	100
O	C	O	5	101
C	O	O	6	110
O	O	O	7 = Highest Priority	111

O = Open (Hi)
C = Closed (Low)

NOTE: Closed position = Switch position set *towards* PC board.

3-4 FRONT PANEL CONTROLS AND INDICATORS

Table 3-4 and figure 3-1 describe and illustrate the controls and indicators located on the front panel.

Change 1

3-5 NATIVE MODE OPERATION

The NATIVE Mode command language is specifically designed to control the NAI Model 5388 synchro/resolver simulator (SIM) and angle position indicator (API) functions.

3-5.1 Entering the NATIVE Mode. If MATE/CIIL is installed, the Model 5388 powers up in the MATE/CIIL command mode, and must be placed in the NATIVE Mode before sending NATIVE Mode programming commands.

If MATE/CIIL is not installed, then the unit will automatically power-up in NATIVE mode.

To *enter* the NATIVE Mode a **GAL** (Go Alternative Language) command must be executed to switch the Model 5388 from the MATE/CIIL Mode to the NATIVE Mode. (Refer to tables 4-3 and 4-6 for API and SIM CIIL command definitions, respectively).

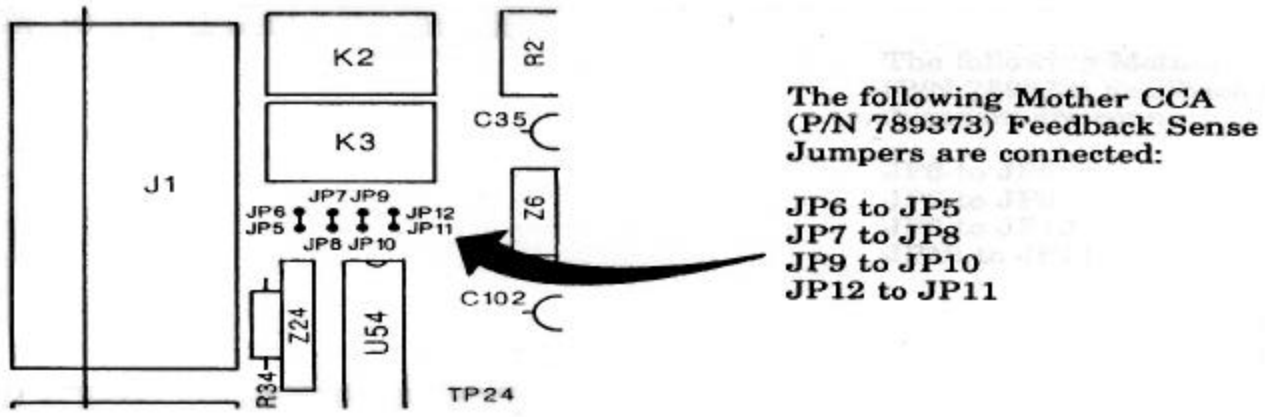


Figure 3-2. Feedback Sense Jumpers

Table 3-4. Front Panel Controls and Indicators

Control/Indicator	Function
Status Indicators	
POWER	Power on indicator. When lit, indicates system is receiving +5 Vdc.
FAIL	Indicator lights on power-up. Indicator goes out after unit successfully passes system self-test procedures. If indicator stays lit device has failed self-test.
MODID	Modular Identification. When lit, indicates device is selected by a high state on the P2 MODID line. NOTE: Illumination of this indicator depends upon controller in slot 0.
SFI	Sysfail Inhibit. Lights when the controller sets (to 1) the Sysfail Inhibit bit in the device's control register. Disables unit from driving the SYSFAIL line and locking up system.
RST	Reset. Lights when controller sets (to 1) the Reset bit in the device control register. When Reset bit is cleared (to 0) the device will begin another self-test sequence.
J1	Digital-to-Synchro Simulator (SIM).
J2	Synchro-to-Digital Angle Position Indicator (API).

3-5.2 Exiting the NATIVE Mode. (MATE/CIIL units only) To *exit* the NATIVE mode, enter any valid Model 5388 MATE/CIIL command and the Model 5388 will return to the MATE/CIIL Mode.

3-5.3 Input/Output Command Notation. The following tables list syntax notations and general definitions which describe various input and output command strings.

Table 3-5. Formal Syntax Notation

Notation	Definition
< >	item definition or reference
[ ]	optional item
( )	grouping braces
::=	"is defined to be"
|	alteration (or)
...	optional repetition of immediately preceding item or group

3-5.4 Error Messages. Error messages are built and placed in the output buffer as a result of receiving invalid NATIVE Mode command strings.

The absence of error is indicated when the **space** <cr><lf> message is returned in response to the **STAT** command.

There are three main types of NATIVE Mode command errors:

a. Invalid NATIVE Mode commands
b. Invalid numeric input values
c. Invalid out-of-range numeric values

3-5.4.1 NATIVE Mode Command Error Message. If the NATIVE command language parser receives an invalid command the following error message is built and sent to the output buffer:

NATIVE MODE COMMAND ERROR - EXPECTED CMD RECEIVED *XXXX*

where: *XXXX* is replaced with the invalid input token.

Table 3-6. General Command Definitions

Notation	Definition
<value>	**(**ASCII encoded scientific number **|** ASCII encoded decimal number **|** ASCII encoded integer **)** All *<values>* The resolution of *<values>* is three digits to the right of the decimal point. Higher resolutions will be accepted but truncated to three digits to the right of the decimal point.
<scientific number>	**[+|-][***<digit>***...]<dp>***<digit>***...E<+|->***<digit>***[***<digit>***]**
<decimal number>	**([+|-]***<digit>***...<dp>[***<digit>***...] |[+|-]<dp>***<digit>***...)**
<integer>	**[+|-]***<digit>***...**
<digit>	(0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9)
<b>	one or more ASCII blank space characters
<dp>	ASCII decimal point (period) "."
<cr>	ASCII carriage return character
<lf>	ASCII line feed character

Table 3-7. NATIVE Mode Command String Formats

Command String	Command Format
<command string>	**(***<set up command string>* | *<query command string>* **|** *<API angle read command >* | *<API maintenance angle command>* | *<system query command>* | *<instrument test command>***) <cr><lf>**
<set up command string>	**(***<SIM set up command>***[<b>***<set up command string>***] |** *<API set up command>***[<b>***<set up command string>***])**
<query command string>	**([***<set up command string>***<b>]** *<API query command>* **|** **[***<set up command string>***<b>]** *<SIM query command>* **)**
<SIM set up command>	**(SD | SS | SR | SL<b>***<value>* **|** **SI<b>***<value>* **|** **SA<b>***<value>* **|** **SV<b>***<value>* **|** **SE<b>***<value>* **)**
<API set up command>	**(AD | AS | AR | AT | AH | ATA | ATD |** **AL<b>***<value>* **|** **AF<b>***<value>* **)**
<API query command>	**(QARS | QATH | QAL | QAF | QA)**
<SIM query command>	**(QSRS | QSL | QSI | QSF |** **QSA | QSV | QSE | QS)**
<API angle read command>	**(AA | ASA [<b>***<value>***])**
<API maintenance angle command>	**AMA<b>***<value>*
<system query command>	**(STAT | VER)**
<system test command>	**(TEST)**

3-5.4.2 NATIVE Mode Numeric Input Error Message. If the NATIVE command language parser is expecting a numeric value (i.e., after processing a command that must be followed by a value) and receives an invalid numeric string, the following error message is built and sent to the output buffer:

NATIVE MODE NUMERIC INPUT ERROR - EXPECTED *XXXX* ***RECEIVED*** *YYYY*

where: *XXXX* is replaced with one of the following types of values expected:

Voltage
Reference Voltage
Frequency
Angle
Angle Rate
End Angle

where: *YYYY* is replaced with the invalid numeric string.

3-5.4.3 NATIVE Mode Value Range Error Message. If the NATIVE command language parser is expecting a numeric value (i.e., after processing a command that must be followed by a value) and receives an out-of-range value, the following error message is built and sent to the output buffer:

NATIVE MODE VALUE RANGE ERROR - EXPECTED *XXXX* **RECEIVED** *YYYY*

where: *XXXX* is replaced with one of the following types of values expected:

Voltage
Reference Voltage
Frequency
Angle
Angle Rate
End Angle

where: *YYYY* is replaced with the numeric string.

3-6 THE ANGLE POSITION INDICATOR (API) OPERATION

The API mode allows the Model 5388 to use all the functions of an Angle Position Indicator (API) instrument. The following paragraphs describe the various programming commands which allow API operation.

3-6.1 API Setup Commands. Table 3-8 defines API setup commands which are specially designed to configure the Model 5388 for API functions.

3-6.2 API Angle Reading Command. The following command defines an API angle reading.

Command	Definition
AA	API Angle. The ASCII value of the current angle is placed in the output buffer.

3-6.3 API Read Stable Angle Command. The following defines the API stable angle command.

Command	Definition
ASA[<b><*value*>**]**	.100<*value (seconds)*<60.00 The API Read Stable angle command waits for API to stabilize or time out. It returns an *angle* or *timeout* error message. If optional value is not included, a default value of three seconds is used for the timeout value. <*Value*> defines the stability timeout default length. *Stability* is defined as: No change in input angle for 100 milliseconds.

Table 3-8. API Setup Commands

Command	Definition
AD	API Default. Model 5388 is set to its power-up *default values* as follows: Track Mode Mode = Resolver Input Line-to-Line Voltage = 90 V Frequency = 400 Hz
AS	API Synchro Mode. Model 5388 is set to Synchro Mode.
AR	API Resolver Mode. Model 5388 is set to Resolver Mode.
AT	API Track. Model 5388 is set to Track Mode.
AH	API Hold. Model 5388 is set to Hold (freeze) Mode.
AL<b><*value*>	API Line-to-Line Voltage. Model 5388 input line-to-line voltage is set to *value.* Range : 2 £ *value (V)* £ 90
AF<b><*value*>	API Frequency. Model 5388 input frequency is set to *value.* Since calibration data is dependent upon frequency, the frequency command should always be used on power-up or the input frequency will change. Range : 47 £ *value (Hz)* £ 10000
ARES<b><*value*>	API Resolution. Model 5388 API resolution is set to <*value*> Range: 0.001 ≤ *value* (Degrees) ≤ 0.1
ATA	API Trigger Arm. Model 5388 API Trigger Mode is set to ARMED.
ATD	API Trigger Disarm. Model 5388 API Trigger Mode is set to DISARMED.

3-6.4 API Maintenance Angle Command. The following defines the API maintenance angle command.

Command	Definition
AMA<b><*value*>	API Maintenance Angle. The Model 5388 is internally set to the value of the input angle. It is also set to Hold (freeze) Mode. This mode can be exited by issuing an API Track command. The API Maintenance Angle command can also be used to preset (approximately) the Model 5388 to a known angle and improve settling time.

3-6.5 API Query Commands. Table 3-9 defines API query commands which allow the user to determine the present Model 5388 API modes in operation.

3-6.6 Command String Examples. Table 3-10 lists and defines examples of typical command strings used by the Model 5388 API.

NOTE

If a command string contains a *Query* or API *Angle Read* command, it should be the only such command in the string, and it must be the last command in the string. An error message is *not* generated and all commands after it are ignored when:

a. one or more *Query* or *Angle Read* commands are in the string, or
b. it is the last command in the string.

3-6.7 API Resolution Command. The following defines the API resolution command.

Command	Definition
ARES<b><*value*>	API Resolution Command. The API resolution is set to *value.* <*value*> defines the smallest angular increment in degrees ths API can sense. The allowable rang for <*value*> is: $0.001 \leq value\ 0. \leq 1$

3-6.8 API Trigger Command. The API trigger command allows the current angle measurement to be latched in response to a low-to-high TTL transition at the trigger pin of the API connector and read at the next API angle reading command. The latched angle will be retriggerable, allowing the latched angle to be updated if another trigger signal occurs before the previously latched angle has been read. The trigger function will be independent of the API track and hold functions. If a trigger occurs while the API is in track mode, the API will continue tracking once the current angle has been latched. The trigger state query function informs the user as to the current state. In addition to explicit disarm trigger function, trigger may be disarmed by issuing the API Default command or by running Self-test.

Table 3-9. API Query Commands

Command	Definition
QARS	Query API Resolver Synchro Mode. A response string of *RESOLVER* is built if the current API mode is Resolver Mode. *SYNCHRO* is the response string built if API is in Synchro Mode.
QATH	Query API Track Hold Mode. A response string of *TRACK* is built if the API is tracking. *HOLD* is the response string built if Model 5388 is in Hold (freeze) Mode.
QAL	Query API Line-to-Line Voltage. The current value of the Model 5388 input line-to-line voltage is converted to an ASCII string and placed in the output buffer.
QAF	Query API Frequency. The current value of the Model 5388 input frequency is converted to an ASCII string and placed in the output buffer.
QA	Query API. All API values as per the above query commands are built into one response string. The QA string returned has the following format: API**<b>STATUS<b>-<b>MODE<b>:<b> RESOLVER / SYNCHRO <b> TRACK / FREEZE** **<b>INPUT<b>L<b>TO<b>L<b>VOLTAGE<b>:<b>**<*value*>**<b>V** **<b>INPUT<b>FREQUENCY<b>:<b>**<*value*>**<Hz><cr><lf>** NOTE: All <*values*> are output to three digits to the right of the decimal point (i.e., 350.000).
QAT	Query API Trigger State. There are three possible responses to this query depending on whether the API Trigger mode is armed, disarmed, or armed and triggered: DISARMED ARMED TRIGGERED

Table 3-10. Command String Examples

Command String	Action
AR AL *26*	Set Model 5388 to Resolver Mode. Set Model 5388 line-to-line voltage to 26 volts. The response string is set to the message: **space <cr lf>**.
AR AL *26* **QA**	Set Model 5388 to Resolver Mode. Set Model 5388 line-to-line voltage to 26 volts. The response string is filled by the query API command handler.
AR AL QA	An error is discovered trying to parse the Model 5388 line-to-line voltage. An error message is generated and command string processing is stopped. Error Message: **NATIVE MODE NUMERIC INPUT ERROR - EXPECTED VOLTAGE RECEIVED QA** NOTE The Model 5388 is *not* set to Resolver Mode at this time, but will be set to Resolver Mode upon receipt of the next valid NATIVE Mode command.
AR AW AA	An error is discovered trying to parse the **AW** command (**AW** is not a valid NATIVE Mode command). An error message is generated and command string processing is stopped. Error Message: **NATIVE MODE COMMAND ERROR - EXPECTED CMD RECEIVED AW** NOTE The Model 5388 is *not* set to Resolver Mode at this time, but will be set to Resolver Mode upon receipt of the next valid NATIVE Mode command.
AR AL *20000000* **AA**	A range error is discovered checking the 20 million value against the Model 5388 line-to-line voltage limits. An error message is generated and command string processing is stopped. Error Message: **NATIVE MODE VALUE RANGE ERROR - EXPECTED VOLTAGE RECEIVED 20000000** NOTE The Model 5388 is *not* set to Resolver Mode at this time, but will be set to Resolver Mode upon receipt of the next valid NATIVE Mode command.

3-7 RESOLVER SIMULATOR (SIM) OPERATION

The SIM mode allows the Model 5388 to use all the functions of a synchro/resolver simulator instrument. The following paragraphs describe the various programming commands which allow synchro/resolver simulation.

3-7.1 Synchro/Resolver Simulator Setup Commands. Table 3-11 defines synchro/resolver simulator setup commands which are specifically designed to configure the Model 5388 for SIM functions.

Table 3-11. SIM Operation

Command	Definition
SD	SIM Default. Model 5388 is set to its power up *default values*. Mode = Resolver Output L-L Voltage = 2V Reference = 115V Frequency = 400 Hz Angle - 0.000°
SS	SIM Synchro Mode. Model 5388 is set to Synchro Mode.
SR	SIM Resolver Mode. Model 5388 is set to Resolver Mode.
SL<b><*value*>	SIM Line-to-Line Voltage. Model 5388 output line-to-line voltage is set to *value*.
SI<b><*value*>	SIM Input Reference Voltage. Model 5388 input reference voltage is set to *value.* Range : 2 £ *value (V)* £ 90
SF<b><*value*>	SIM Frequency. Model 5388 frequency is set to *value*. Since calibration data is dependent upon frequency, the frequency command should always be used on power-up or the input frequency will change.

Table 3-11. SIM Operation (Continued)

Command	Definition
SA<b><*value*>	SIM Angle. Model 5388 output angle is set to *value*.
SV<b><*value*>	SIM Velocity. This value is an angle rate in degrees per second that the simulator angle will rotate at. Making this value zero causes the simulator to exit rotation mode and output a fixed angle. Range : -1000 £ *value (D/S)* £ 1000
SE<b><*value*>SI	M End Angle. This command, in conjunction with an **SV** command with a non-zero value, places the Model 5388 in the Triangular Mode. The simulator rotation is from SA angle to SE angle and back at a rate of SV degrees per second. Once in the Triangular Mode a new SE value can be issued to change the end boundary. The Triangular Mode is exited by issuing an **SV** command with a velocity of 0. To reenter Triangular Mode a new Velocity and End Angle command must be reissued.

3-7.2 Synchro/Resolver Simulator Query Commands. Table 3-12 lists and defines *query* commands which allow the user to determine Model 5388 SIM modes and data values in current operation.

Table 3-12. SIM Query Commands

Command	Definition
QSRS	Query SIM Resolver Synchro Mode. A response string of *RESOLVER* is built if the current SIM mode is the Resolver Mode. *SYNCHRO* is the response string built if SIM is in Synchro Mode.
QSL	Query SIM Line-to-Line Voltage. The current value of the Model 5388 output line-to-line voltage is converted to an ASCII string and placed in the output buffer.
QSI	Query SIM Input Reference Voltage. The current value of the Model 5388 input reference voltage is converted to an ASCII string and placed in the output buffer.
QSF	Query SIM Frequency. The current value of the Model 5388 input frequency is converted to an ASCII string and placed in the output buffer.
QSA	Query SIM Angle. The current value of the Model 5388 output angle is converted to an ASCII string and placed in the output buffer.
QSV	Query SIM Velocity. The current value of the Model 5388 velocity (angle rate) is converted to an ASCII string and placed in the output buffer.
QSE	Query SIM End Angle. The current value of the Model 5388 end angle is converted to an ASCII string and placed in the output buffer.
QS	Query SIM. All SIM values as per the above query commands are built into one response string. The QS string returned has the following format: **SIM<b>STATUS<b>-<b>MODE<b>:<b>** RESOLVER / SYNCHRO **<b>OUTPUT** **<b>L<b>TO<b>L<b>VOLTAGE<b>:<b>**<*value*>**<b>V** **<b>INPUT<b>REFERENCE<b>VOLTAGE<b>:<b>**<*value*>**<b>V** **<b>FREQUENCY<b>:<b>**<*value*>**<b>Hz** **<b>OUTPUT<b>ANGLE<b>:<b>**<*value*>**DEGREES<cr><lf>** NOTE: All <*values*> are output to three digits to the right of the decimal point (i.e., 350.000).

3-8 SELF TEST

The Model 5388 contains an internal self-test program that functionally verifies the operation of the entire instrument. The format of the self-test command is:

TEST<cr><lf>

The self-test requires approximately 60 seconds to complete. When finished a self-test status message is placed in the output buffer. This message can take 1 of 2 forms:

"<b>SELF TEST PASSED" if the test was successful or

"SELF TEST FAILURE - <description>" if the test fails.

where <description> is an ASCII string which describes the nature of the failure.

3-9 SYSTEM VERSION COMMAND

To identify the Manufacturer, Model number, Firmware Version and VXI version, use the following command:

VER<cr><lf>

Response will be of the following form:

NAI SRP Rev-5.7 08-AUG-95 MODEL 5388 VXI 1.3<cr><lf>

SECTION 4

MATE/CIIL PROGRAMMING OPTION

4-1 INTRODUCTION

This section describes the operation and programming of the Model 5388 using the Modular Automatic Test Equipment (MATE) Control Interface Intermediate Language (CIIL) option. Since the Model 5388 can function as either an Angle Position Indicator (API) or Synchro/Resolver Simulator (SIM) the following is divided into two parts:

a. Angle Position Indicator (API) MATE/CIIL Programming

b. Synchro/Resolver Simulator (SIM) MATE/CIIL Programming.

4-1.1 MATE/CIIL Functions. The CIIL option allows the Model 5388 to communicate with the MATE controller and *powers-up in the MATE/CIIL mode.* The MATE/CIIL option automatically determines which mode, SIM or API, is being programmed. It provides the following functions:

a. Accepts control computer input and translates the standard program instructions of the MATE Control Interface Intermediate Language (CIIL) into that required by the Model 5388.
b. Upon command sends measurement responses to the control computer.
c. Provides the means to perform Confidence and Self-Test procedures.
d. Controls the isolation relays.
e. Generates status messages.

4-1.2 Reference Documents. Recommended reference documents for use with this option include:

a. MATE Control Interface Intermediate Language - Standard 2806763, Rev. C.
b. MOD 1 - MATE User's Group Action Traveler - CIIL Definitions.
c. NATIVE Command Language for NAI Model 5388.

4-2 MODEL 5388 API MATE/CIIL PROGRAMMING

The following paragraphs describe the operation and MATE/CIIL programming of the Model 5388 when it is configured for use as an angle position indicator (API).

The following notation in table 4-1 is used to describe various input and output strings.

Table 4-1. Elemental Notation

Notation	Description
|	Exclusive OR
<>	The boundaries of a field or structure of inseparable items.
<b>	One ASCII blank
[ ]	An optional field, item, or structure.
...	The field or structure may be repeated as often as required.
<cr><lf>	ASCII encoded carriage return followed by line feed.
<*setcode*>	SET | SRX | SRN
<*noun*>	SYN or RSL
<*mchar*>	Four ASCII encoded characters. See table 4-3 for a complete list.
<*modifier*>	Four ASCII encoded characters. See table 4-3 for a complete list.
<*chan num*>	1 or 2 digit number indicating the channel number.
<*value*>	Any ASCII encoded number in floating point, engineering, or integer notation.

4-2.1 Inputs. There are nine input transmission types applicable to the Model 5388 API in the CIIL language. At the start of each type the instrument will be *listen addressed* by the control computer. The end of the transmission will be indicated by **<cr><lf>**. Each transmission type begins with its own characteristic <*verb*>. They are as follows:

Table 4-2. Transmission Inputs

Input	Description
FNC	Set up the instrument
INX	Initiate the measurement
FTH	Transmit the measurement result to the control computer
CLS	Close the input path
OPN	Open the input path
RST	Reset the instrument
STA	Report status
IST	Initiate built-in-test
CNF	Initiate confidence test

As a general rule, anywhere one **<b>** (blank) is indicated, the Model 5388 API will accept multiple blanks as if they were one blank.

4-2.1.1 Format of FNC. The FNC string is used to set up the instrument prior to making a measurement. The general format of the FNC string is:

FNC<b><*noun*>**<b>**<*mchar*>**<b>:CH**<*chan num*>
<b><*setcode*>**<b><ANGL><b>**<*value*>
[<b><*setcode*>**<b>**<*modifier*>**<b>**<*value*>**]…<cr><lf>**

where:

<*noun*> Defines the type of signal to be measured:

SYN - selects synchro
RSL - selects resolver

If any other <*noun*> appears an error message will be generated.

<*mchar*> Defines the characteristic of the signal to be measured. The only <*mchar*> applicable to the Model 5388 API is:

ANGL - measures angle

If any other <*mchar*> appears an error message will be generated.

<*chan num*> Specifies the input channel. In the acts as a single channel device. Therefore only channel 1 or 01 may be specified.

<*set code*> Defined as the ASCII sequences of

SRX, SET, or SRN. If the same <modifier> appears more than once with a different <*set code*>, the Model 5388 API will use the one with the highest priority. The order of priority is:

1. **SRX** 2. **SET** 3. **SRN**

<*modifier*> Modifiers program certain features of the Model 5388 API. The modifiers recognized by the Model 5388 API are:

Modifier	Description
ANGL	Angle
ANRT	Angle Rate. If equal to zero then stability is checked.
VOLT	Voltage. Sets line-to-line voltage.
FREQ	Frequency. Selects null circuit specification if angle is <360 Hz. If <360 Hz then *slow* null circuit speed is selected. If >360 Hz then *fast* null circuit speed is selected.

Also selects internal calibration data to be used.

Any other modifiers appearing in the input string will be ignored.

<*value*> This is an ASCII encoded number in floating point, engineering, or integer notation. The value following all <*modifier*> fields is checked to insure that it is within the limits given as follows:

47	£	FREQUENCY	£ 10000
2	£	VOLTAGE	£ 90
-1000	£	ANGLE-RATE	£ 1000
0	£	ANGLE	£ 359.999

4-2.1.2 Format of INX. The INX string instructs the Model 5388 API to make a measurement. The general format of the INX string is:

INX<b><*mchar*>**<cr><lf>**

Since the Model 5388 API only recognizes the ANGL <*mchar*> the INX string will always be as follows:

INX<b>ANGL<cr><lf>

If any other <*mchar*> appears in the INXstring an error message will be generated (table 4-4).

4-2.1.3 Format of FTH. The FTH string instructs the Model 5388 API to return the measurement result to the control computer. The general format of the FTH string is:

FTH<b><*mchar*>**<cr><lf>**

Since the Model 5388 API only recognizes the ANGL <*mchar*> the FTH string will always be as follows:

FTH<b>ANGL<cr><lf>

If any other <*mchar*> appears in the FTH string an error message will be generated (table 4-4).

4-2.1.4 Format of CLS. The format of the CLS message can be either of the following:

CLS<b>:CH*1***<cr><lf>** or **CLS<b>:CH***01***<cr><lf>**

The CLS command closes the API isolation relays and connects input signal to input connector J1.

4-2.1.5 Format of OPN. The format of the OPN string can be either of the following:

OPN<b>:CH*1***<cr><lf>** or **OPN<b>:CH***01***<cr><lf>**

The OPN command opens the API isolation relays and disconnects input signal from input connector J1.

4-2.1.6 Format of RST. The RST command causes the Model 5388 API to reset the current measurement. The format of RST is:

RST<b><*noun*>**<b>**<*mchar*>**<b>:CH**<*chan num*>
<cr><lf>

The <*noun*> must match the <*noun*> in the previous FNC message and the <*mchar*> must be ANGL, otherwise this command will be ignored.

RST also causes the unit to reset to its initial power-up conditions.

4-2.1.7 Format of STA. The STA command instructs the Model 5388 API to return the status of the instrument. The format of this command is:

STA<cr><lf>

The STA command will return a **<b><cr><lf>** if no error exists.

4-2.1.8 Format of IST. The IST command instructs the Model 5388 to perform an Internal Self-Test procedure. After the test is completed the result can be obtained using the STA command. No messages are allowed to be sent to the Model 5388 API while the test is in progress or an error message will be generated. The format of the IST is:

IST<cr><lf>

<IST Time**>** is 60 seconds.

4-2.1.9 Format of CNF. The CNF command instructs the Model 5388 API to perform a Confidence Test. After the test is completed the result can be obtained using the STA command. No messages are allowed to be sent to the Model 5388 API while the test is in progress or an error message will be generated. The format of the CNF is:

CNF<cr><lf>

<CNF Time**>** is 25 seconds.

4-2.2 Outputs. Error messages are generated for the following basic reasons:

a. Syntax errors
b. Values out of range
c. Failure of CNF or IST
d. Measurement time-outs

Once an error is loaded into the output buffer it will remain there until it is read by the control computer, or until an RST or DCL command is issued. If an error exists when a request for data is made (FTH), the error message will be transmitted in place of the data. Error messages have one of the following forms:

F05API00 (DEV): <*ASCII message*>**<cr><lf>**

F07API00 (MOD): <*ASCII message*>**<cr><lf>**

F07API00 (DEV): <*ASCII message*>**<cr><lf>**

The first form is used if a measurement cannot be completed in the allotted amount of time. The other forms are used to report syntax errors, CNF and IST problems, and <*value*> range errors. See table 4-4 for explanation of error messages.

4-2.2.1 Response to INX. After receiving the INX command, the Model 5388 API will load the output buffer with the maximum amount of time (in seconds) that it will take to make the measurement. For the Model 5388 API this time will always be five seconds. The format of this transmission is:

<b>*5***<cr><lf>**

4-2.2.2 Response to FTH. After receiving the FTH command and after completion of the measurement, the Model 5388 API will load the measurement result into the output buffer. The format of this transmission is:

<b><*value*>**<cr><lf>**

The field <*value*> will contain the synchro or resolver angle in degrees. A typical transmission would be:

<b>*315.000***<cr><lf>**

4-2.2.3 Response to STA. The response to STA will be either:

<b><cr><lf> or an error message

STA is typically used after a CNF or IST to determine whether or not the test was successful. The **<b><cr><lf>** message indicates no errors were found.

Table 4-3. API CIIL Codes

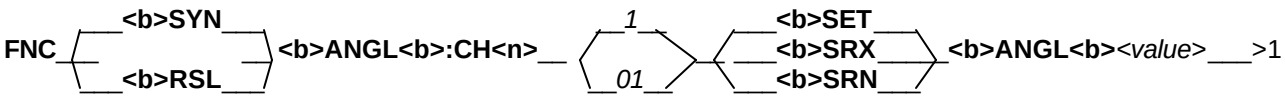
CIIL	Description
<*verbs*>:	
FNC	function
OPN	open
CLS	close
STA	status
RST	reset
CNF	confidence test
IST	BIT test
INX	initiate
FTH	fetch
<*setcodes*>:	
SET	set
SRX	set maximum
SRN	set minimum
<*nouns*>:	
SYN	synchro
RSL	resolver
<*mchars*>:	
ANGL	angle
<*modifiers*>:	
ANGL	angle
ANRT	angle rate
VOLT	voltage
FREQ	frequency

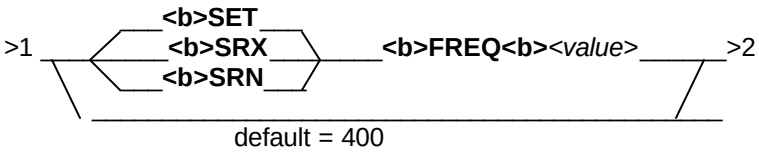
Table 4-4. API Error Messages

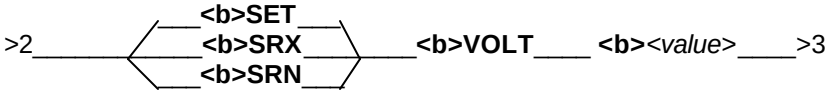
Error Type	Error Message
Modifier	**F07API00 (MOD): CMD ERROR-EXPECTED** *XXXX* **RECEIVED** *YYYY* where: *XXXX* is replaced by one of the following categories of invalid input tokens: <verbs> <setcodes> <nouns> <mchars> <modifiers> where: *YYYY* is replaced by the invalid token input. For example: <noun> **S***L***N** is input to FNC set up string instead of **S***Y***N**. The error token **SLN** is received.
Timing Error	**F05API (DEV): TIMEOUT ERROR**

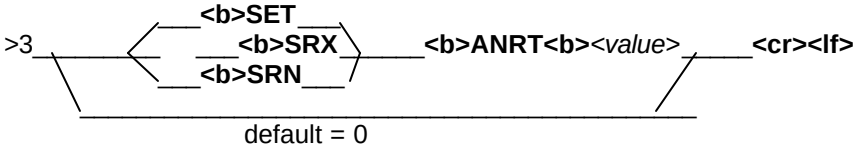
4-3 MODEL 5388 API RAILROAD DIAGRAMS

The following are typical Railroad diagrams for programming the Model 5388 API.









NOTE

Range of <*value*>

VOLT	=	2	£	<*value*> (V)	£	90
REFV	=	2	£	<*value*> (V)	£	115
FREQ	=	47	£	<*value*> (Hz)	£	10000
ANRT	=	-1000	£	<*value*> (Deg/Sec)	£	1000
ANGL	=	0	£	<*value*> (Deg)	£	359.999

4-4 SIM MATE/CIIL PROGRAMMING

The following describes the operation and MATE/CIIL programming of the Model 5388 when it is configured for use as a synchro/resolver simulator (SIM).

The following notation in table 4-5 shall be used to describe various input and output strings.

Table 4-5. Elemental Notation

Notation	Description
|	Exclusive OR
<>	The boundaries of a field or structure of inseparable items.
<b>	One ASCII blank
[ ]	An optional field, item, or structure.
...	The field or structure may be repeated as often as required.
<cr><lf>	ASCII encoded carriage return followed by line feed.
<*setcode*>	SET | SRX | SRN
<*noun*>	SYN or RSL
<*modifier*>	Four ASCII encoded characters.
<*chan num*>	See table 4-6 for a complete list.
<*value*>	1 or 2 digit number indicating the channel number.
	Any ASCII encoded number in floating point, engineering, or integer notation.

4-4.1 Inputs. There are seven input transmission types applicable to the Model 5388 in the CIIL language. At the start of each type the instrument will be *listen addressed* by the control computer. The end of the transmission will be indicated by **<cr><lf>**. Each transmission type begins with its own characteristic <*verb*>. They are as follows:

FNC Setup the instrument
CLS Close the output path
OPN Open the output path
RST Reset the instrument
STA Report status
IST Initiate built-in-test
CNF Initiate confidence test

As a general rule, anywhere one **<b>** (blank) is indicated, the Model 5388 will accept multiple blanks as if they were one blank.

4-4.1.1 Format of FNC. The FNC string is used to set up the instrument. The general format of the FNC string is:

FNC<b><*noun*>**<b>:CH**<*chan num*>

[<b><*setcode*>**<b>**<*modifier*>**<b>**<*value*>**]...<cr><lf>**

where:

<*noun*> Defines the type of signal to be generated:

SYN - selects synchro
RSL - selects resolver

If any other <*noun*> appears an error message will be generated.

<*chan num*> Specifies the input channel. The <*chan num*> must be specified as *0* or *00*.

<*set code*> Defined as the ASCII sequences of SRX, SET, or SRN. If the same <*modifier*> appears more than once with a different <*set code*>, the Model 5388 will use the one with the highest priority. The order of priority is:

1. **SET**
2. **SRN**
3. **SRX**

<*modifier*> Modifiers program features of the Model 5388. Modifiers are checked to verify that they are within the capabilities of the unit. The modifiers recognized by the Model 5388 are:

Modifier	Description
ANGL	angle
ANRT	angle rate
REFV	reference voltage
VOLT	output L-L voltage
FREQ	frequency

If any other modifiers appear an error message will be generated.

[value] This is an ASCII encoded number in floating point, engineering, or integer notation. The value following all <*modifier*> fields is checked to insure that it is within the limits given as follows:

47	£	FREQ	£ 10000
-1000	£	ANGLE-RATE	£ 1000
0	£	ANGLE	£ 359.999
2	£	VOLT	£ 90
2	£	REFV	£ 115

4-4.1.2 Format of CLS. The format of the CLS message can be either of the following:

CLS<b>:CH*0***<cr><lf>** or **CLS<b>:CH***00***<cr><lf>**

The CLS command closes the isolation relays and connects the output signal to output connector J2.

4-4.1.3 Format of OPN. The format of the OPN string can be either of the following:

OPN<b>:CH*0***<cr><lf>** or **OPN<b>:CH***00***<cr><lf>**

The OPN command opens isolation relays and disconnects the output signal from output connector J2.

4-4.1.4 Format of RST. The RST command causes the Model 5388 to reset to the initial power-up state. The format of RST is:

RST<b><*noun*>**<b>:CH**<*chan num*>**<cr><lf>**

The <*noun*> must match the <*noun*> in the previous FNC message or this command will be ignored.

4-4.1.5 Format of STA. The STA command instructs the Model 5388 to return the status of the instrument. The format of this command is:

STA<cr><lf>

4-4.1.6 Format of IST. The IST command instructs the Model 5388 to perform an Internal Self-Test procedure. After the test is completed the result can be obtained using the STA command. No messages are allowed to be sent to the Model 5388 while the test is in progress or an error message will be generated. The format of the IST is:

IST<cr><lf>

IST time is 60 seconds.

4-4.1.7 Format of CNF. The CNF command instructs the Model 5388 to perform a confidence test. The format of the CNF is:

CNF<cr><lf>

CNF time is 25 seconds.

4-4.2 Outputs

4-4.2.1 Response to STA. The response to STA will be either:

<b><cr><lf> or an error message

STA is typically used after the unit is setup to determine if it was programmed properly, and also after a CNF or IST. The **<b><cr><lf>** message indicates no errors were found.

4-4.2.2 Errors. Error messages are generated for the following basic reasons:

a. Syntax errors
b. Values out-of-range
c. Failure of CNF or IST

Once an error is loaded into the output buffer it will remain there until it is read by the control computer, or until an RST or DCL command is issued. Error messages have the following form:

F07SRS00 (MOD): <*ASCII message*>**<cr><lf>**

See table 4-7 for explanation of error messages.

Table 4-6. SIM CIIL Codes

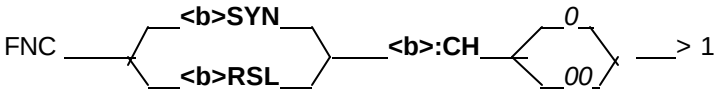
CIIL	Description
<*verbs*>:	
FNC	function
OPN	open
CLS	close
STA	status
RST	reset
CNF	confidence test
IST	BIT test
<*setcodes*>:	
SET	set
SRX	set maximum
SRN	set minimum
<*nouns*>:	
SYN	synchro
RSL	resolver
<*modifiers*>:	
ANGL	angle
ANRT	angle rate
REFV	reference voltage
VOLT	voltage
FREQ	frequency

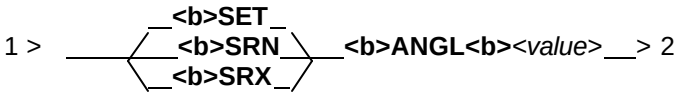
Table 4-7. SIM Error Messages

Error Type	Error Message
Modifier	**F07SRS00 (MOD): CMD ERROR-EXPECTED** *XXXX* **RECEIVED** *YYYY* where: *XXXX* is replaced by one of the following categories of invalid input tokens: <verbs> <setcodes> <nouns> <mchars> <modifiers> where: *YYYY* is replaced by the invalid token input. For example: <noun> **S***L***N** is input to FNC set up string instead of **S***Y***N**. The error token **SLN** is received.
Timing Error	**F05SRS00 (DEV): TIMEOUT ERROR**

4-5 MODEL 5388 CIIL RAILROAD DIAGRAMS

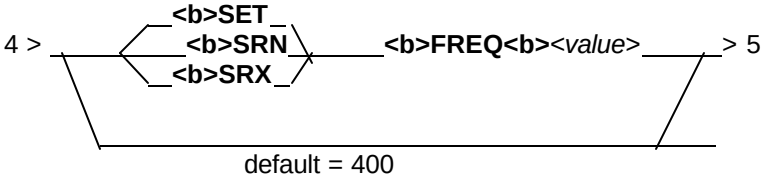
The following are typical CIIL Railroad Diagrams which are used for programming the Model 5388 SIM.

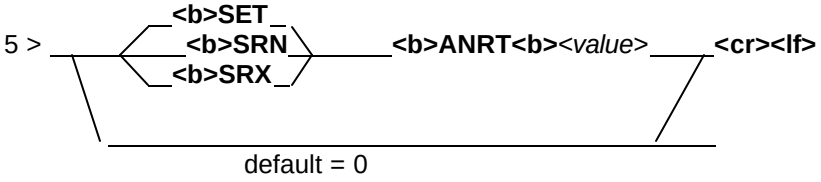












NOTE

Range of <*value*>

VOLT	=	2	£	<*value*> (V)	£	90
REFV	=	2	£	<*value*> (V)	£	115
FREQ	=	47	£	<*value*> (Hz)	£	10000
ANRT	=	-1000	£	<*value*> (Deg/Sec)	£	1000
ANGL	=	0	£	<*value*> (Deg)	£	359.999

SECTION 5

ADJUSTMENT AND CALIBRATION

5-1 INTRODUCTION

This section contains adjustment, calibration, and checkout instructions for the Model 5388. Refer to table 1-3 for the test equipment required to perform the procedures in this section.

5-2 PERFORMANCE SCHEDULE

Table 5-1 lists the performance tests recommended for the Model 5388 on a semiannual basis. If performance tests indicate an out of specification condition the unit should be recalibrated as described in paragraph 5-5. After Model 5388 API or SIM repair, all alignments pertaining to that repair (API or SIM) must be performed followed by the complete checkout procedure and performance tests provided in paragraph 5-3.

Table 5-1. Semiannual Performance Tests

Procedure	Reference Paragraph
Performance Tests	5-3.3
API	5-3.3.2
SIM	5-3.3.3

WARNING

Dangerous voltages may be present in the unit when the side cover is removed.

CAUTION

The Model 5388 is electrostatically sensitive. Failure to comply with safeguards could damage the equipment. Refer to DOD-HDBK-263 for ESD sensitive equipment handling procedure.

5-3 CHECKOUT

Checkout for the Model 5388 consists of the group of checkout procedures provided in paragraphs 5-3.1 and performance test procedures in paragraphs 5-3.3.2 and 5-3.3.3. Each procedure is presented in a step-by-step format and references a test equipment setup figure. The test equipment setup figure illustrates the complement of test equipment necessary to perform the test and shows all the required interconnections between the test equipment and the Model 5388. Pretest conditions are stated for all performance and adjustment procedures. Refer to table 1-3 for specific test equipment requirements. If the result of any test is not as described in the procedure, refer to the troubleshooting procedures provided in Section 6 of this manual.

The following checkout procedure verifies the correct functionality of the Model 5388. It is recommended that this procedure be performed in a VXI card cage using a Slot 0 Controller when the unit is initially received.

5-3.1 API Checkout Procedure.

a. Set up equipment as shown in figure 5-1.
b. Adjust variable signal source to 26 V, 400 Hz.
c. Program the Model 5388 API using the following NATIVE mode commands:

AL *90*
AF *400*
AS

d. Adjust Model 530/10 Simulator to Synchro mode, 90 V, 0 degrees.
e. Using the **ASA** command, program Model 5388 to read API angle.
f. The measured API angle should be equal to the input simulator angle± 0.004 degrees.
g. Repeat steps 5-3.1.d through 5-3.1.f for angles 10^{o} through 350^{o} in 10^{o} steps.
h. Program the Model 5388 using the following NATIVE mode commands:

AL *11.8*
AF *400*
AR

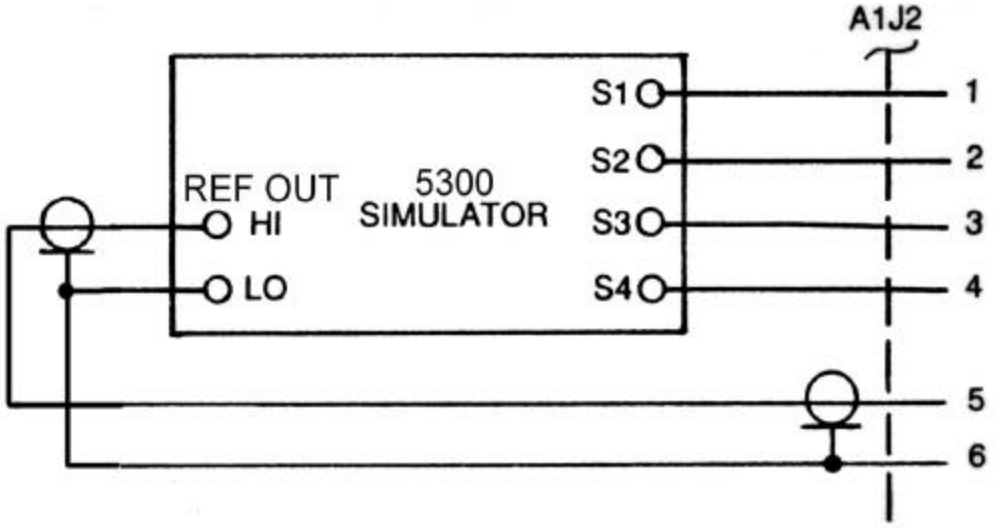


Figure 5-1. API Checkout Procedure Equipment, Setup Diagram

i. Set the Model 5300 Simulator to Resolver mode, 11.8 V, 0 degrees.
j. Using the **ASA** command, program Model 5388 to read API angle.
k. The measured API angle should be equal to the simulator angle± 0.004 degrees.
l. Repeat steps 5-3.1.i and 5-3.1.k for angles 10° through 350° in 10° steps.

5-3.2 Simulator Checkout Procedure.

a. Set up equipment as shown in figure 5-2.
b. Adjust variable signal source to 26 V, 400 Hz.
c. Adjust Model 540/10 Bridge to Synchro mode, 0 degrees.
d. Program Model 5388 SIM using the following NATIVE mode commands:

SI *26*
SL *90*
SS
SA *0*

e. While observing the Phase Angle Voltmeter, adjust Model 540/10 Bridge for an inphase null (0 V).
f. The Model 540/10 Bridge angle should be equal to the programmed angle± 0.003 degrees.
g. Repeat steps 5-3.2.d through 5-3.2.f for angles 10° through 350° in 10° steps. NOTE: The value following command **SA** (see step 5-3.2.d) is the new angle increment to be programmed.
h. Adjust the Model 540/10 Bridge to Resolver mode, 0 degrees.
i. Program Model 5388 SIM using the following NATIVE mode commands:

SI *26*
SL *11.8*
SA *0*
SR

j. While observing the Phase Angle Voltmeter, adjust Model 540/10 Bridge for an inphase null (O V).

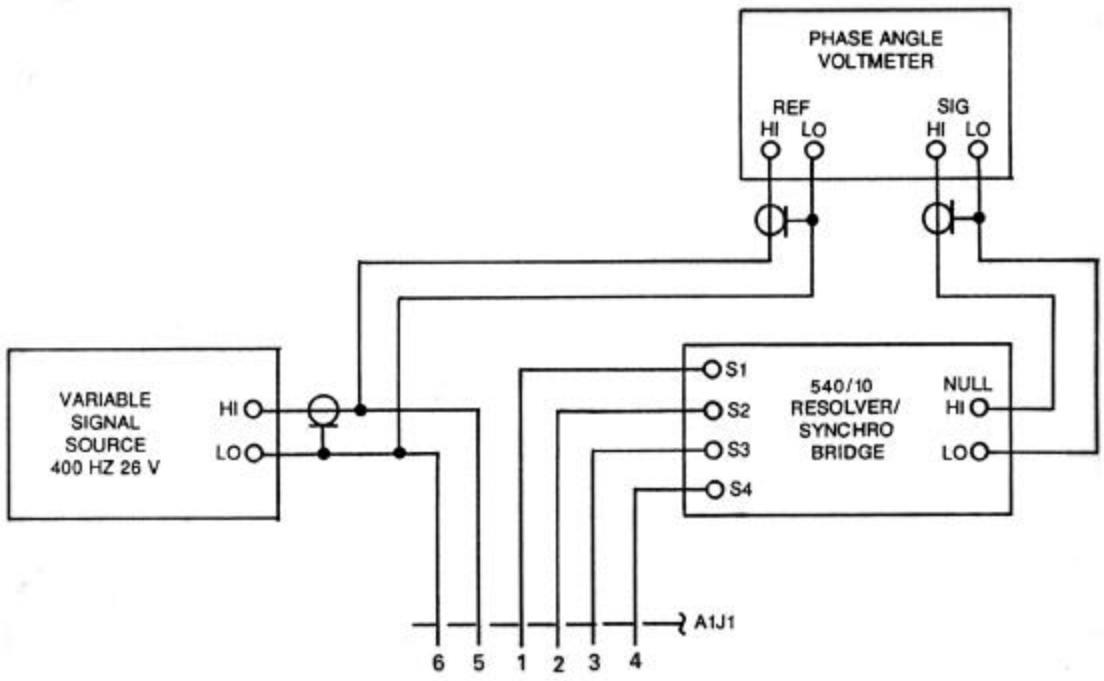


Figure 5-2. Simulator Checkout Procedure Equipment, Setup Diagram

k. The Model 540/10 Bridge angle should be equal to the programmed angle± 0.003 degrees.
l. Repeat step 5-3.2.i through 5-3.2.k for angles 10^{o} through 350^{o} in 10^{o} steps. NOTE: The value following command **SA** (see step 5-3.2.h) is the new angle increment to be programmed.
m. Proceed to paragraph 5-3.3 and complete all performance tests before using the Model 5388.

5-3.3 Performance Tests. The performance of the Model 5388 must be verified semiannually by a qualified technician (refer to table 5-1). If performance tests indicate an out of specification condition then the Model 5388 must be recalibrated as described in paragraph 5-5. After calibration is complete the following performance tests in paragraphs 5-3.3.2 and 5-3.3.3 must be performed again.

5-3.3.1 Pretest Conditions.

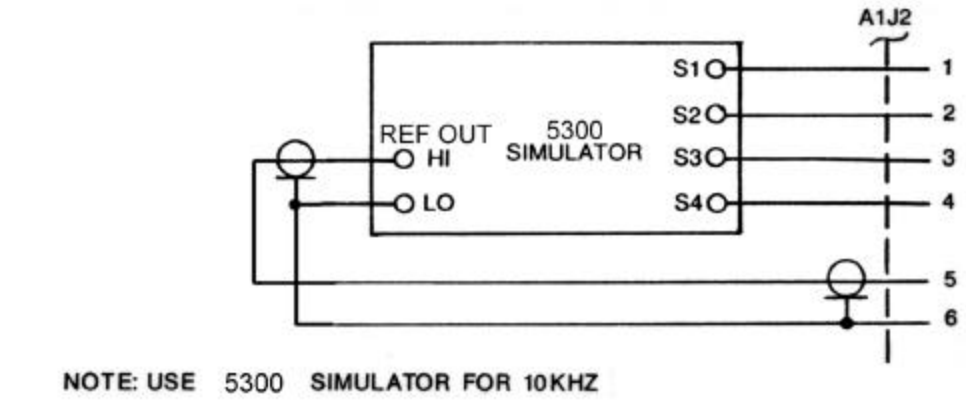
a. Turn on Model 5388 and all test equipment.
b. Warm up Model 5388 and all test equipment for thirty minutes.

5-3.3.2 API Performance Test.

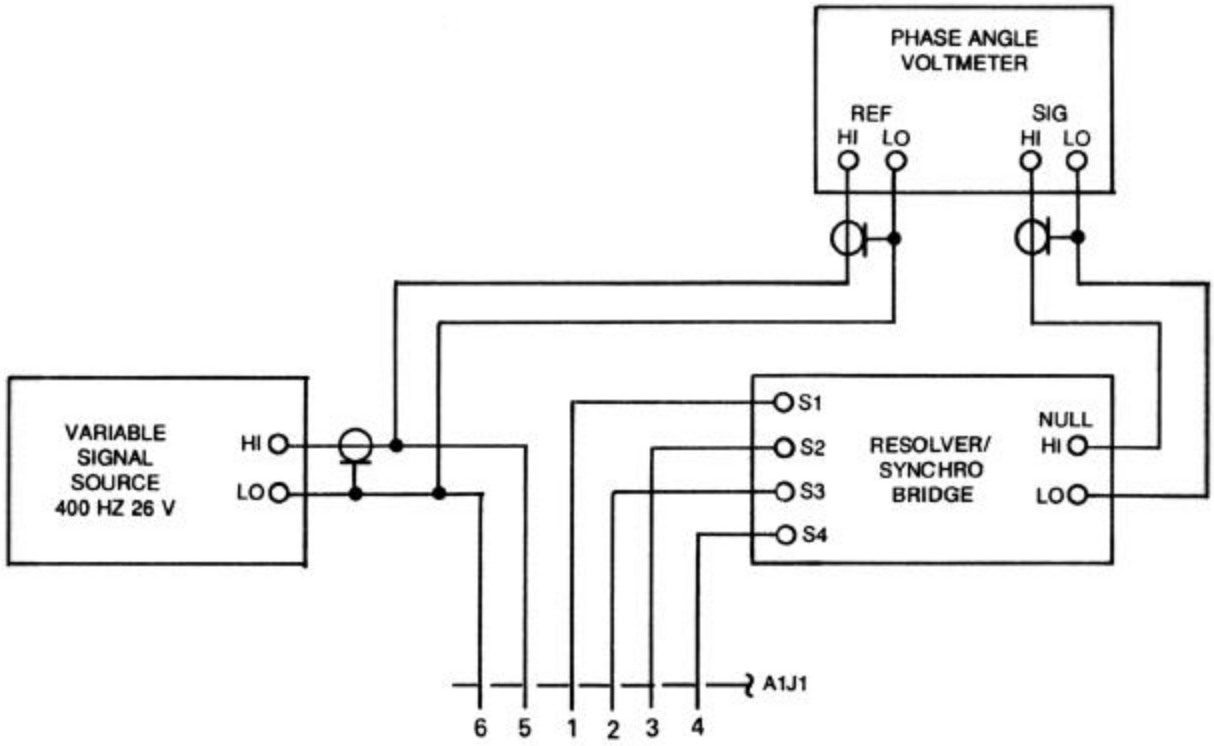
a. Set up test equipment as shown in figure 5-3A.
b. The performance of the Model 5388 API is to be tested at the frequencies, voltages, and modes listed in table 5-2.
c. Set the simulator selector switch to the proper mode for the test being performed.

NOTE

Make sure to use the correct model simulator for the correct frequency as indicated in table 5-3.



A



B

Figure 5-3. Model 5388 API/SIM Performance Test Equipment, Setup Diagram

Table 5-2. Model 5388 API/SIM Performance Test Specifications

Frequency	L-L Voltage	Mode	Limit
50 (47-1000 Hz model only)	11.8, 26, 90	synchro	.003
400 Hz	11.8, 26, 90	synchro	.003
400 Hz	2, 11.8, 26, 90	resolver	.003
1000 Hz	11.8, 26, 90	synchro	.003
1000 Hz	2, 11.8, 26, 90	resolver	.003
10,000 Hz (360-10,000 Hz model only)	2, 11.8, 26, 90	resolver	.015

Table 5-3. Test Frequency and Corresponding Simulator/Bridge Model Number

Test Frequency	Model Number	
	Bridge	SIM
50	540/20	5300
400	540/10	5300
1000	540/10	5300
10,000	540/20	5300

d. Adjust variable voltage source to 26 V at the frequency to be tested (refer to table 5-2).
e. Program the Model 5388 to the proper mode (Synchro or Resolver), line-to-line voltage, and frequency. For example:

If the performance test being run is at 400 Hz, Resolver mode, 11.8 V then program the Model 5388 API with the following NATIVE language command string (see Section 3 for details):

AR AL *11.8* **SF** *400*

f. Set simulator to 0 degree.
g. Using the ASA command, program Model 5388 API to read API angle. The difference between the API angle reading and the simulator angle should be within the *limit* specification given in table 5-2.
h. Repeat steps 5-3.3.2.f and 5-3.3.2.g for angles 10^o through 350^o in 10^o steps.
i. Repeat steps 5-3.3.2.c through 5-3.3.2.h for each combination of frequency, voltage, and mode listed in table 5-2.

5-3.3.3 Simulator (SIM) Performance Test.

Change 1

a. Set up test equipment as shown in figure 5-3B.
b. The performance of the Model 5388 SIM is to be tested at the frequencies, voltages, and modes listed in table 5-2.
c. Set the bridge selector switch to the proper mode for the test being performed (refer to table 5-2).

NOTE

Make sure to use the correct model bridge for the correct frequency as indicated in table 5-3.

d. Adjust variable voltage source to 26 V at the frequency to be tested (refer to table 5-2).
e. Program the Model 5388 SIM to the proper mode (Synchro or Resolver), frequency, input voltage, and angle. For example:

If the performance test is being run at 400 Hz, Resolver mode, 11.8 V then program the Model 5388 SIM with the following NATIVE language command string (see Section 3 for details):

SR SI *26* **SL** *11.8* **SF** *400*

f. Adjust bridge for an inphase null on the phase angle voltmeter. The difference between the bridge angle reading and the SIM reading should be within the *Limit* specification given in table 5-2.
g. Repeat steps 5-3.3.3.e and 5-3.3.3.f for angles 10^o through 360^o in 10^o steps.
h. Repeat steps 5-3.3.3.c through 5-3.3.3.g for each combination of frequency, voltage, and mode listed in table 5-2.

5-4 ADJUSTMENT PROCEDURES

Complete adjustment procedures for the Model 5388 are given in the following subparagraphs. These procedures may be performed as a set or as part of periodic maintenance. Refer to figure 7-2 and table 5-4 for the required sequence of alignment procedures.

Each procedure is presented in a step-by-step format and references a test setup figure where applicable. The test setup figure illustrates the complement of test equipment necessary to perform the alignment and shows all the required interconnections between the test equipment and the Model 5388. (Refer to table 1-3 for specific test equipment requirements.) If during performance of any adjustment procedure, the required results cannot be attained, refer to the troubleshooting procedures provided in Section 6 of this manual.

5-4.1 Preadjustment Conditions. The following preadjustment conditions are common to all adjustment procedures. Establish these conditions prior to performing each procedure.

a. With power off, slide Model 5388 out of VXI card cage.
b. Install extender card into card cage.
c. Install Model 5388 into extender card.
d. Warm up Model 5388 and test equipment for 30 minutes.
e. Set all variable signal source outputs to their minimum values.
f. Set the Model 5388 to maintenance mode by sending the command **AMMODE.**

5-4.2 Preadjustment Procedures. Before adjusting the Simulator or Angle Position Indicator circuits of the Model 5388 remove ten screws securing side cover and remove cover. Refer to table 5-4 for adjustment procedure sequence.

Table 5-4. Adjustment Procedure Sequence

Paragraph Number	Adjustment Description
5-4.3.1	Output Amplifier dc Offset
5-4.3.2	Output Amplifier Feedback
5-4.3.3	Output Amplifier Gain
5-4.4.1	Input Amplifier
5-4.4.2	Quadrant
5-4.4.3	Synchro
5-5.3	API Calibration
5-5.4	SIM Calibration

5-4.3 Simulator Adjustment Procedures. The following Simulator adjustment procedures must be performed if the Simulator fails the Performance Test (paragraph 5-3.3.3) after calibration or following a Model 5388 Simulator repair.

Refer to Section 3 for Simulator programming information and to test setup diagrams as necessary.

WARNING

Dangerous voltages may be present in the unit when the side cover is removed.

CAUTION

The Model 5388 is electrostatically sensitive. Failure to comply with safe-guards could damage the equipment. Refer to DOD-HDBK-263 for ESD sensitive equipment handling procedure.

5-4.3.1 Output Amplifier dc Offset Adjustment.

NOTE

The following adjustment procedure uses the **SAR** programming command which *sends uncalibrated raw* angle data.

a. Program the Model 5388 Simulator to 0^{o} (use **SAR** command), Resolver mode, 2 V line-to-line.
b. Install shorting jumper between test points A1TP15 and A1TP13.
c. Connect DC voltmeter between test points A1TP26 (HI) and A1TP13 (LO).
d. Adjust A1R40 for a reading of 0 V$\pm$ 50 mV dc.
e. Remove shorting jumper from test points A1TP15 and A1TP13.
f. Program Model 5388 Simulator to 90^{o} (use **SAR** command), Resolver Mode, 2 V line-to-line.
g. Install shorting jumper between test points A1TP7 and A1TP2.
h. Connect DC voltmeter between test points A1TP25 (HI) and A1TP2 (LO).
i. Adjust A1R41 for a reading of 0 V$\pm$ 50 mV dc.
j. Remove shorting jumper from test points A1TP7 and A1TP10.

Change 1

5-4.3.2 Output Amplifier Feedback Adjustment.

a. Disconnect transformer connectors A1T1P1 and A1T2P1 (figure 7-2).
b. Set up equipment as shown in figure 5-4A.
c. Program Model 5388 Simulator to Resolver mode and output voltage to 90 V.
d. Adjust variable signal source for 90 V, 400 Hz.
e. Adjust A1C43 top adjusting screw to the *closed position* and then turn adjusting screw counter-clockwise fourteen turns.
f. With phase angle voltmeter connected between test points A1TP12 (HI) and A1TP8 (LO), adjust A1R4 for an inphase null reading (0 V).
g. Set up equipment as shown in figure 5-4B.
h. Adjust variable signal source for 90 V, 10 kHz.
i. Connect phase angle voltmeter between test points A1TP12 (HI) and A1TP2 (LO).
j. Adjust A1C112 for a quadrature null reading (0 V) on phase angle voltmeter.
k. Adjust A1R43 for an inphase null reading (0 V) on phase angle voltmeter.
l. Repeat steps 5-4.3.2.j and 5-4.3.2.k until both inphase and quadrature null readings are 0 volts.
m. Reconnect transformer connectors A1T1P1 and A1T2P1.

5-4.3.3 Output Amplifier Gain Adjustment.

NOTE

The following adjustment procedure uses the **SAR** programming command which *sends uncalibrated raw* angle data.

a. Set up equipment as shown in figure 5-5.
b. Adjust variable signal source for 26 V, 400 Hz.
c. Program Model 5388 Simulator as follows:

SI *26*
SL *90*
SA *45*
SR

d. Set Resolver/Synchro Bridge to Resolver mode, 45 degrees.
e. Adjust A1R5 for an inphase null reading (0 V) on the phase angle voltmeter.
f. Program Model 5388 Simulator as follows:

SL *26*

g. Adjust A1R3 for an inphase null reading (0 V) on the phase angle voltmeter.
h. Program Model 5388 Simulator as follows:

SL *11.8*

i. Adjust A1R2 for an inphase null reading (0 V) on the phase angle voltmeter.
j. Program Model 5388 Simulator as follows:

SL *90*
SA *135*

k. Set Resolver/Synchro Bridge angle for 135.000 degrees.
l. Adjust A1R19 for an inphase null reading (0 V) on the phase angle voltmeter.
m. Connect phase angle voltmeter between test points A1TP8 (HI) and A1TP2 (LO).
n. Adjust A1C102 for an inphase null reading (0 V) on phase angle voltmeter.
o. Adjust A1R35 for a quadrature null reading (0 V) on phase angle voltmeter.
p. Repeat steps 5-4.3.3.n and 5-4.3.3.o until both inphase and quadrature null readings are 0 volts.

5-4.4 Angle Position Indicator Adjustment Procedures. The following angle position indicator (API) adjustment procedures must be performed if API fails the Performance Test (paragraph 5-3.3.2) after calibration or following a Model 5388 API repair.

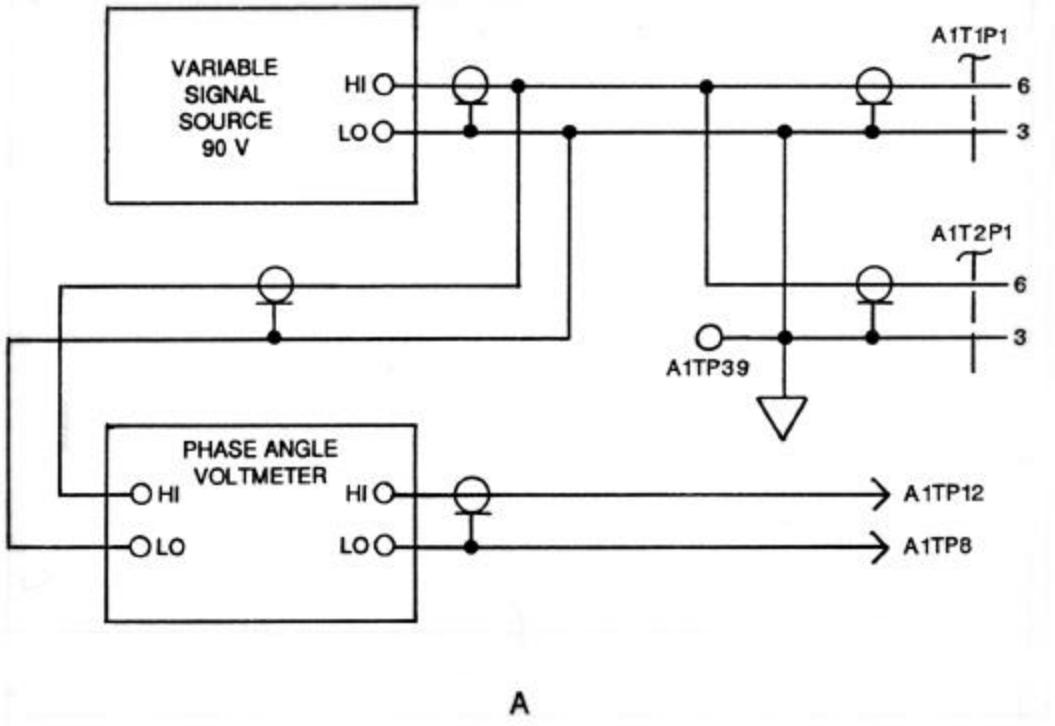
Refer to Section 3 for Angle Position Indicator programming information and to test setup diagrams as necessary.

WARNING

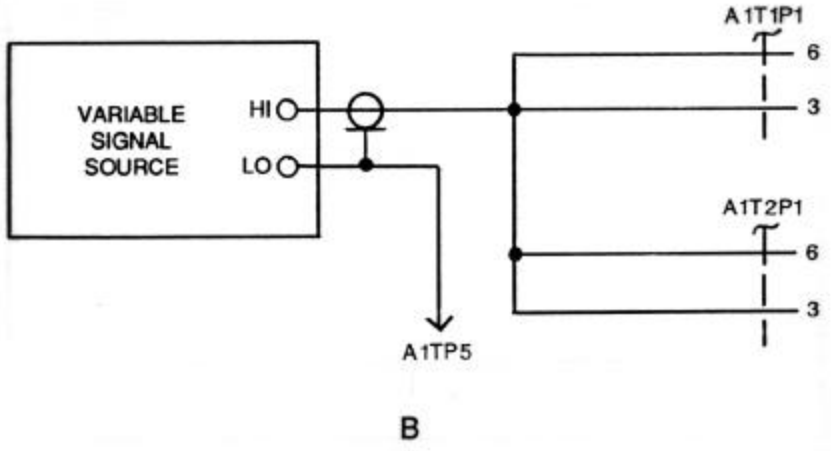
Dangerous voltages may be present in the unit when the side cover is removed.

CAUTION

The Model 5388 is electrostatically sensitive. Failure to comply with safeguards could damage the equipment. Refer to DOD-HDBK-263 for ESD sensitive equipment handling procedure.



A



B

Figure 5-4. Output Amplifier Feedback Adjustment, Test Setup Diagram

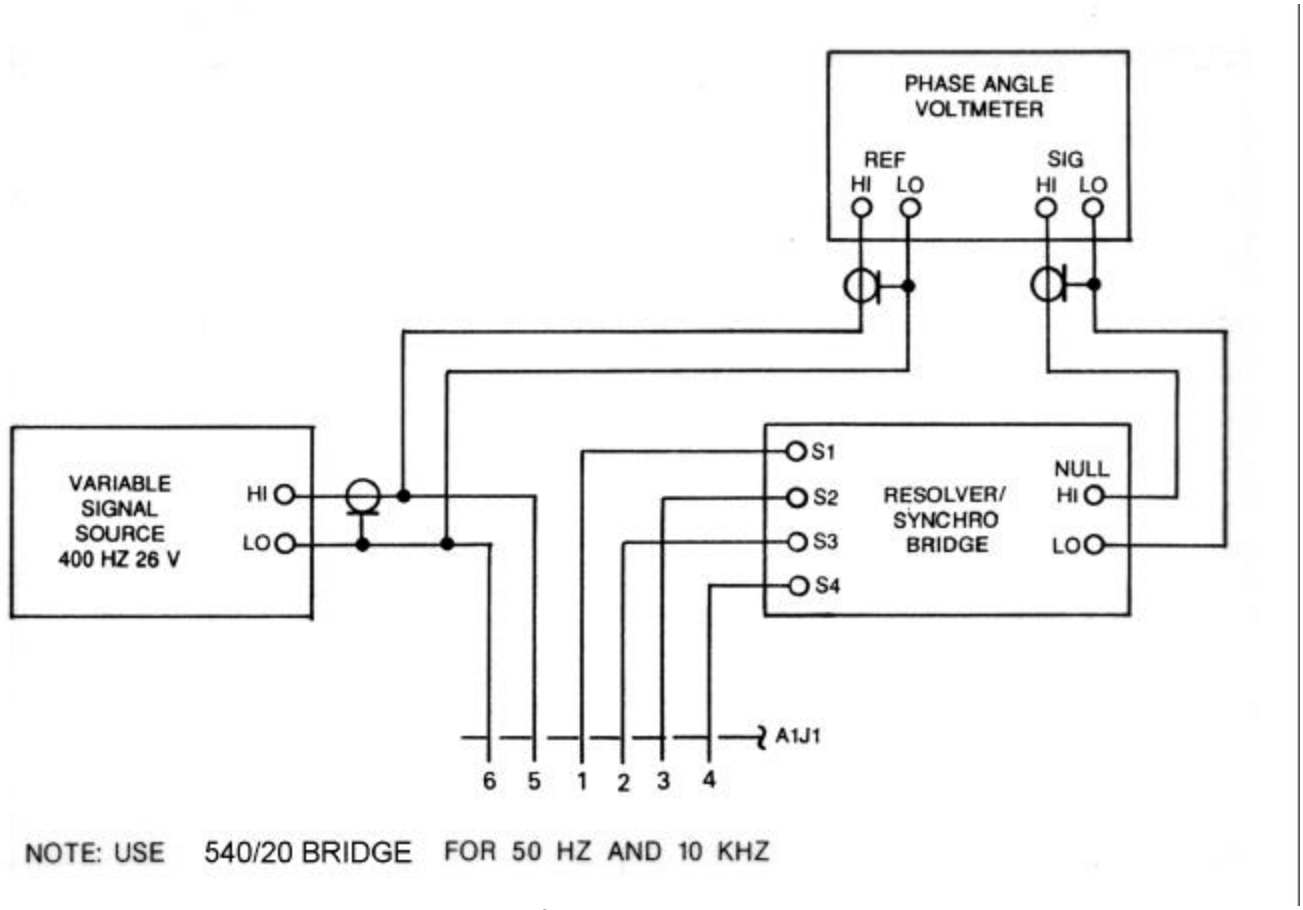


Figure 5-5. Output Amplifier Gain Adjustment, Test Setup Diagram

5-4.4.1 Input Amplifier Adjustment.

a. Set up equipment as shown in figure 5-6A.
b. Adjust A1C137 top adjusting screw to the *closed position* and then turn adjusting screw counterclockwise fourteen turns.
c. Adjust variable signal source to 90 V, 400 Hz.
d. Program Model 5388 API as follows:

AR
AL*90*

e. With phase angle voltmeter connected between test points A1TP31 (HI) and A1TP34 (LO), adjust A1R47 for an inphase null reading (0 V).
f. Adjust variable source signal for 10 kHz.
g. Adjust A1C126 for a quadrature null reading (0 V) on phase angle voltmeter.
h. Set up equipment as shown in figure 5-6B.
i. Adjust variable signal source to 90 V, 10 kHz.
j. With phase angle voltmeter connected between test points A1TP31 (HI) and A1TP32 (LO), adjust A1C141 for a quadrature null reading (0 V).
k. Adjust A1R55 for an inphase null reading (0 V) on p
l. Repeat steps 5-4.4.1.j and 5-4.4.1.k until both inphase and quadrature null readings are 0 volts.
m. Connect phase angle voltmeter between test points A1TP30 (HI) and A1TP29 (LO).
n. Adjust A1C133 for a quadrature null reading (0 V) on phase angle voltmeter.
o. Adjust A1R49 for an inphase null reading (0 V) on phase angle voltmeter.
p. Repeat steps 5-4.4.1.n and 5-4.4.1.o until both inphase and quadrature null readings are 0 volts.

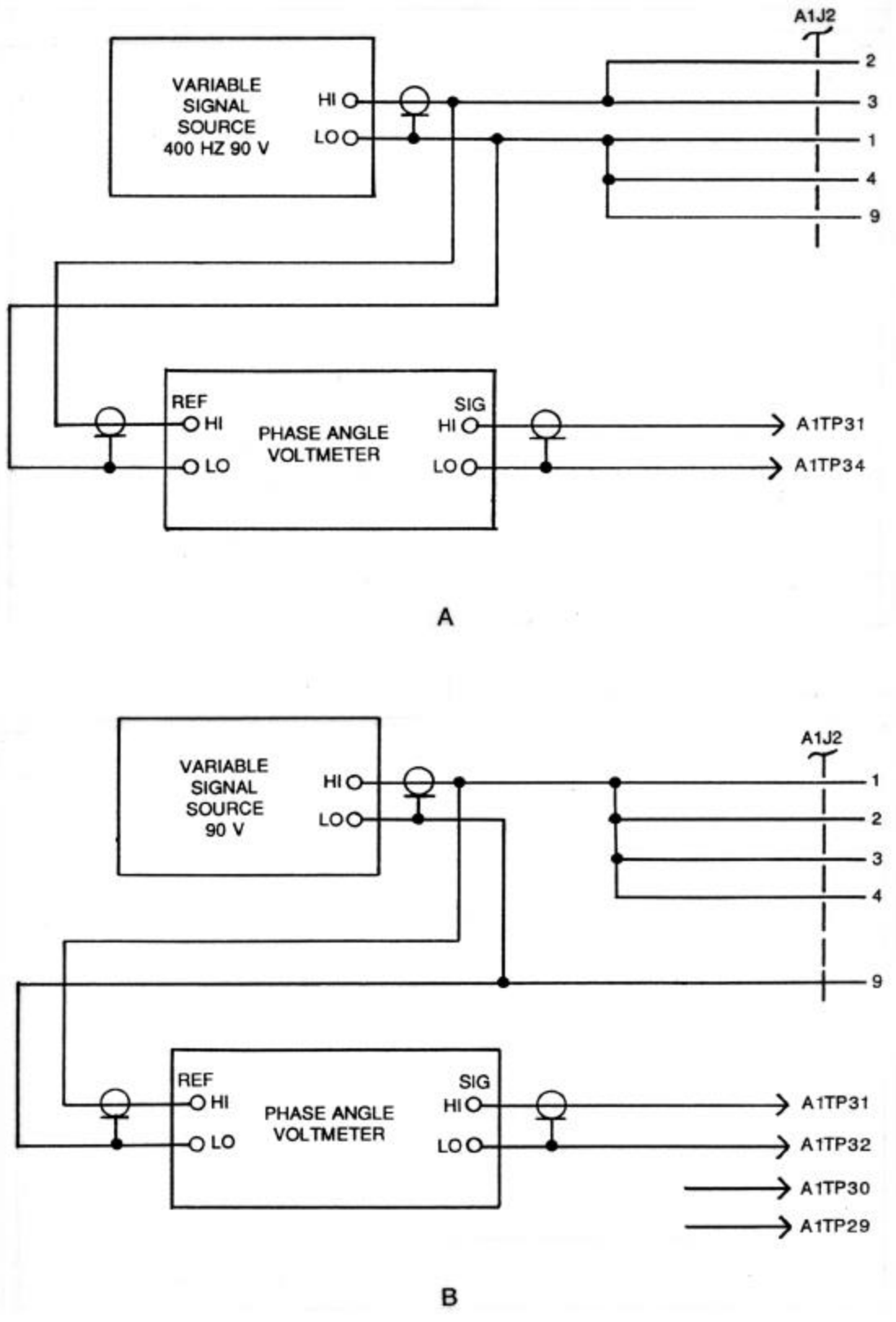


Figure 5-6. Input Amplifier Adjustment, Test Setup Diagram

5-4.4.2 Quadrant Adjustments.

NOTE

The following adjustment procedure uses the **AAR** programming command which *reads uncalibrated raw* angle data.

a. Set up equipment as shown in figure 5-7.
b. Adjust variable signal source to 26 V, 400 Hz.
c. Set up Model 5300 Simulator for 26 V, Resolver mode, 0.000 degrees.
d. Program Model 5388 API to 26 V, Resolver mode, 400 Hz.
e. Using the **AAR** command, program Model 5388 to read the API angle.
f. Adjust A1R25 for a reading of 0.000.
g. Set 5300 Simulator angle to 135.000 degrees.
h. Using the **AAR** command, program Model 5388 to read the API angle.
i. Adjust A1R22 for a reading of 135.000.
j. Set 5300 Simulator angle to 225.000 degrees.
k. Using the **AAR** command, program Model 5388 to read the API angle.
l. Adjust A1R20 for a reading of 225.000.
m. Set 5300 Simulator to 45.000 degrees.
n. Using the **AAR** command, program the Model 5388 to read the API angle.
o. Adjust A1R54 for a reading of 45.000.

5-4.4.3 Synchro Adjustment.

NOTE

The following adjustment procedure uses the **AAR** programming command which *reads uncalibrated raw* angle data.

a. Set up equipment as shown in figure 5-7.
b. Set up Model 5300 Simulator to Synchro mode, 120.000 degrees
c. Program Model 5388 API to Synchro mode, 26 V, 400 Hz.
d. Using the **AAR** command, program Model 5388 to read the API angle.
e. Adjust A1R51 for a reading of 120.000.
f. Set 5300 Simulator angle to 45.000 degrees.
g. Using the **AAR** command, program Model 5388 to read the API angle.
h. Adjust A1R51 for a reading of 120.000.
i. Set 5300 Simulator angle to 45.000 degrees.
j. Using the **AAR** command, program Model 5388 to read the API angle.
k. Adjust A1R50 for a reading of 45.000.

5-5 CALIBRATION PROCEDURES

Calibration of the Model 5388 is accomplished by storing *correction data* for various angles, voltages, and frequencies in one electrically erasable programmable read-only-memory (EEPROM). The correction data is stored in 10 degree steps from 0 to 350 degrees for each voltage and frequency.

a. Frequency Calibration Parameters. The standard calibration voltages and frequencies are listed in tables 5-4 and 5-5.

b. If Model 5388 is used only at a single frequency and voltage, the spot calibration method may be chosen instead of the standard calibration method.

c. Spot Calibration Parameters. If a voltage and frequency spot calibration is needed, its parameters will be a subset of the factory calibration parameters.

Spot calibration is obtained by calibrating at a voltage and frequency greater than, and a voltage and frequency value less than the selected values. These boundaries are chosen from tables 5-4 and 5-5 below. Refer to the following examples:

Example 1 - Voltage Calibration: SIM 22V, 400Hz

a. Determine the voltage boundaries (refer to table 5-5):

12.1 V <22 V <*26 V*

b. Calibrate unit at 12.1 V and 26 V @ 400 Hz.

Example 2 - Frequency Calibration: @ 11.8 V and 800 Hz

a. Determine the frequency boundaries (refer to table 5-4):

2 V <11.8 V <*12 V*
400 Hz <800 Hz <*1000 Hz*

b. Calibrate unit at 400 Hz and 1000 Hz.

Twelve tables, each with thirty-six entries of correction data, are stored for each operating mode (Synchro or Resolver) and for each instrument (Simulator or Angle Position Indicator). This results in forty-eight tables each with thirty-six entries of correction data.

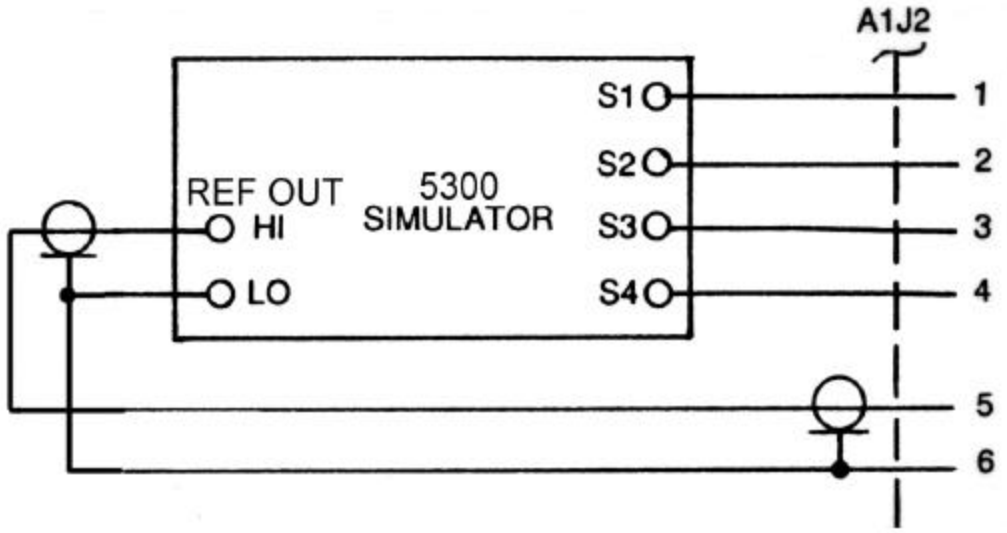


Figure 5-7. Quadrant Adjustments, Test Setup Diagram

In operation, a working calibration table is built by linearly interpolating between the voltage and frequency data in the twelve tables. Degree points between the calibrated angle are also linearly interpolated when using the working tables.

5-5.1 Storing Calibration Data. Calibration data is sent to the Model 5388 over the VXIbus using the following programming commands:

a. **ARLC** - Load API resolver calibration data
b. **ASLC** - Load API synchro calibration data
c. **SRLC** - Load SIM resolver calibration data
d. **SSLC** - Load SIM synchro calibration data

Each command is followed by four numeric fields which indicate the particular table and entry number. The format of these fields are:

<frequency><voltage><index><calibration data>

where: *<frequency>* is an integer that specifies one of the following frequencies:

Table 5-4. Frequency Parameters

Integer	API	SIM Low	SIM High
0	50 Hz	50 Hz	400 Hz
1	400 Hz	400 Hz	1 kHz
2	1 kHz	1 kHz	10 kHz
3	10 kHz	---	---

<voltage> is an integer that specifies one of the following voltages:

Table 5-5. Voltage Parameters

Integer	API	SIM
0	2 V	2 V
1	11.8 V	12 V
2	26 V	12.1 V
3	50 V	26 V
4	90 V	26.1 V
5	---	90 V

<calibration data> is a signed integer indicating the amount of .001 degree increments that must be added in order to correct the data. The range is +127 to -128.

<index> is an integer from 1 to 35 that specifies one of thirty-five angles in 10^{o} steps. For

Change 1

example:

1 = 10° 10 = 100° 35 = 350°

The following examples illustrate how to store calibration correction data.

NOTE

Calibration data is stored differently for low frequency (5388-FX1) and high frequency (5388-FX2) versions. Low frequency version requires that a shunt jumper be installed between pins A1JP1 and A1JP2 for proper operation.

Example 1

+.005 degrees is needed to correct the Model 5388 API in the resolver mode at 30.000 degrees, 90 V line-to-line, 400 Hz. The following command will store this correction in the correct table:

ARLC *0 3 3 +5*

Example 2

-.020 degrees is needed to correct the Model 5388 SIM in the synchro mode at 120.000 degrees, 11.8 V line-to-line, 10 kHz. The following command will store this correction in the correct table:

SRLC *2 1 12 -20*

5-5.2 Calibration Data Verification. Previously stored calibration data can be retrieved by using the following commands:

a. **ARSC** - Sends API resolver calibration data
b. **ASSC** - Sends API synchro calibration data
c. **SRSC** - Sends SIM resolver calibration data
d. **SSSC** - Sends SIM synchro calibration data

Each command is followed by three fields that indicate the table and index number. The format of the fields are as follows:

<frequency><voltage><index>

where: *<frequency>* is an integer that specifies one of the following three frequencies:

		SIM	
Integer	API	Low	High
0	50 Hz	50 Hz	400 Hz
1	400 Hz	400 Hz	1 kHz
2	1 kHz	1 kHz	10 kHz
3	10 kHz	---	---

<voltage> is an integer that specifies one of the following four voltages:

Integer	API	SIM
0	2 V	2 V
1	11.8 V	12 V
2	26 V	12.1 V
3	50 V	26 V
4	90 V	26.1 V
5	---	90 V

<index> is an integer from 1 to 35 that specifies one of thirty-five angles in 10° steps. For example:

1 = 10 10 = 100° 35 = 350°

After the Model 5388 receives one of the calibration data retrieval commands, it loads the output buffer with the stored calibration data in angular format. This data will be transmitted the next time the unit is addressed to talk.

Example 1

Verify that -5 was stored in the API at 270.000 degrees, 10 kHz, 2 V line-to-line, in the Synchro mode by sending the following command:

ASSC *2 0 27*

The Model 5388 will respond with:

-.005

Example 2

Verify that +3 was stored in the Simulator at 0.000 degrees, 200 Hz, 26 V line-to-line, in the Resolver mode by sending the following command:

SRSC *1 2 0*

The Model 5388 will respond with:

+.003

Change 1

5-5.3 API Calibration Procedure. The following procedure is used to calibrate the Model 5388 API. Although it can be performed manually, it is recommended that a computer assisted program based on this procedure be written by the user.

a. Set up equipment as shown in figure 5-8.
b. Set up 530/10 Simulator for 2 V, 400 Hz, Resolver mode, 0.000 degrees.
c. Program Model 5388 API to Resolver mode, 2V line-to-line, 400 Hz.
d. Using **AAR** command, program Model 5388 to read the API angle.
e. Calculate correction data as follows:

Correction Data = (*programmed angle - reading*)

f. Using **ARLC** command, program Model 5388 to send and load the correction data.
g. Verify that correction data was sent by using **ARSC** command.
h. Repeat steps 5-5.3.d through 5-5.3.g for angles 20^{o} through 350^{o} in 10^{o} steps.
i. Repeat steps 5-5.3.d through 5-5.3.h for line-to-line voltages 11.8 and 26 V.

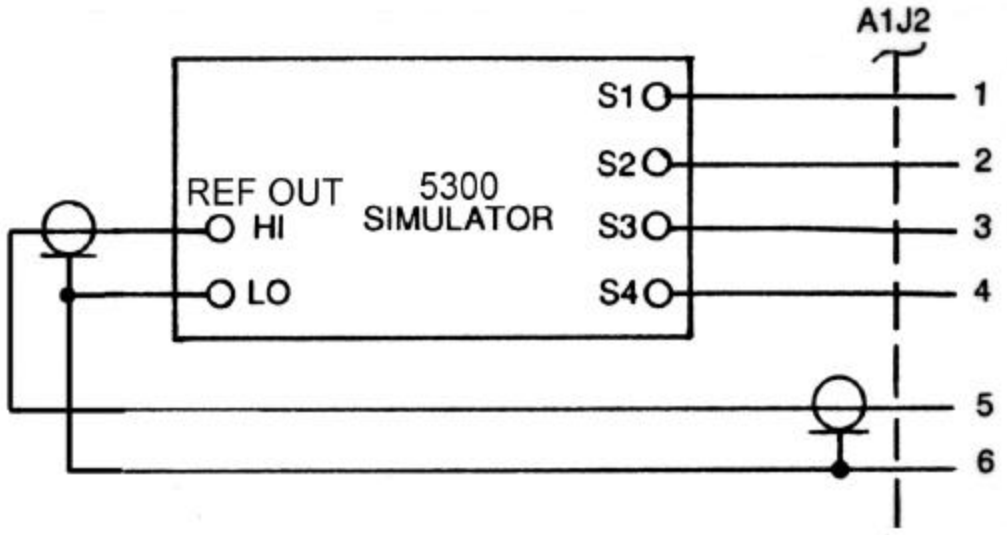


Figure 5-8. API Calibration, Test Setup Diagram

j. Repeat steps 5-5.3.d through 5-5.3.i for frequencies 1 kHz and 10 kHz.
k. Set up 530/10 Simulator for 11.8 V, 50 Hz, Synchro mode, 0.000 degrees.
l. Program Model 5388 API to Resolver mode, 11.8 V, line-to-line, 50 Hz.
m. Using **AAR** command, program the Model 5388 API to read the API angle.
n. Calculate correction data as follows:

Correction Data = (*programmed angle - reading*)

o. Using **ASLC** command, program Model 5388 to send and load correction data.
p. Verify that correction data was stored by using **ASSC** command.
q. Repeat steps 5-5.3.m through 5-5.3.p for angles 20^{o} through 350^{o} in 10^{o} steps.
r. Repeat steps 5-5.3.m through 5-5.3.q for line-to-line voltages 11.8, 26, 50, and 90.
s. Repeat steps 5-5.3.m through 5-5.3.r for frequencies 400 Hz and 1 kHz.

5-5.4 Simulator Calibration Procedure. The following procedure is used to calibrate the Model 5388 Simulator (SIM). Although it can be performed manually, it is recommended that a computer assisted program based on this procedure be written by the user.

a. Set up equipment as shown in figure 5-9.
b. Set up Resolver-Synchro Bridge and variable voltage source for Resolver mode, 0.000 degrees, 400 Hz.
c. Program Model 5388 SIM to Resolver mode, 2 V line-to-line.
d. Using **SAR** command, program Model 5388 Simulator to angle 0.000 degrees.
e. Adjust Resolver-Synchro Bridge for an inphase null (0 V) reading on the phase angle voltmeter.
f. Calculate correction data as follows:

Correction Data = (*programmed angle - bridge angle*)

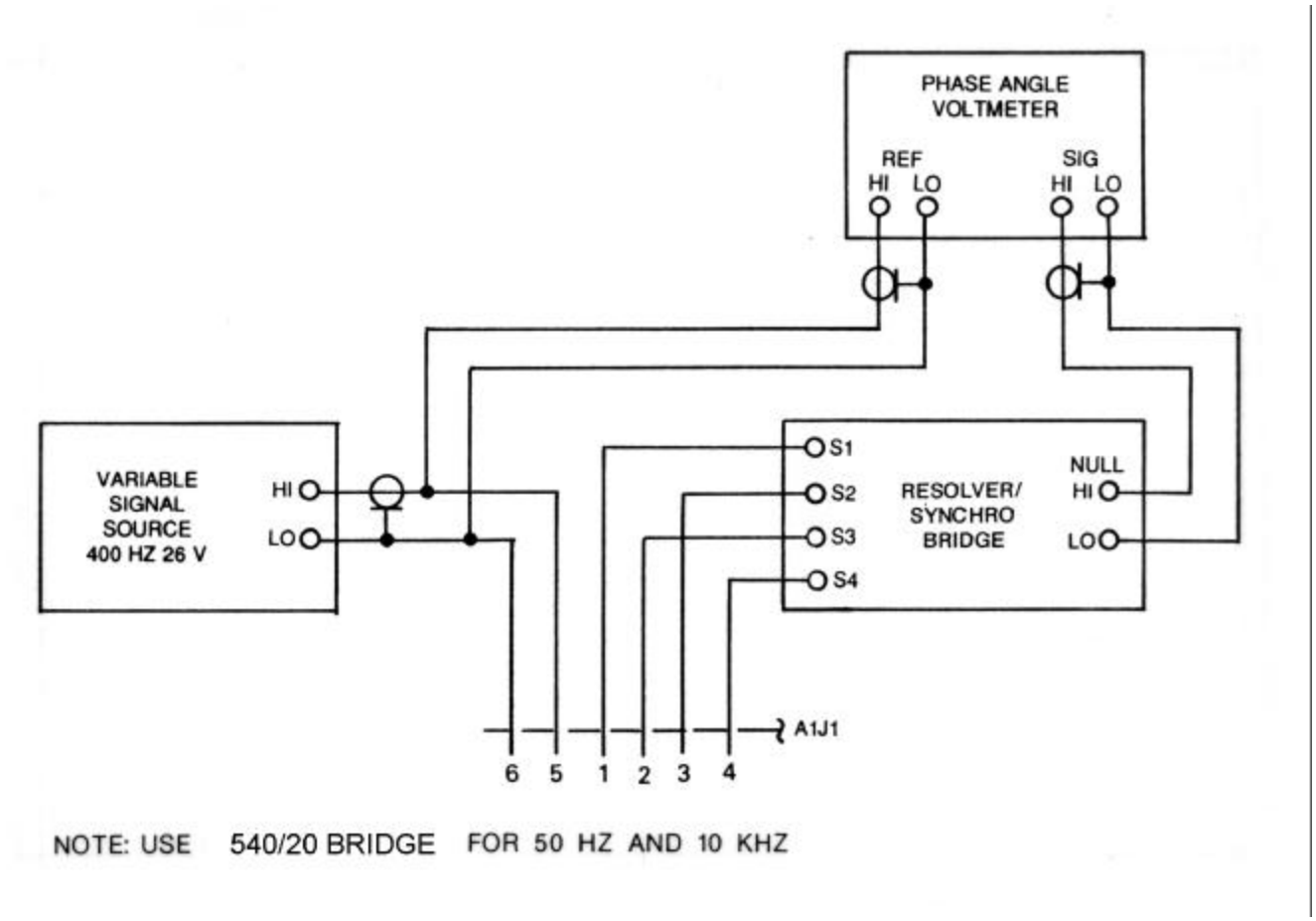


Figure 5-9. Simulator Calibration, Test Setup Diagram

g. Using **SRLC** command, program Model 5388 to send and load correction data.
h. Verify that correction data was sent by using **SRSC** command.
i. Repeat 5-5.4.d through 5-5.4.h for angles 20^{o} through 350^{o} in 10^{o} steps.
j. Repeat steps 5-5.4.d through 5-5.4.i for line-to-line voltages 12, 12.1, 26, 26.1, and 90.
k. Repeat steps 5-5.4.d through 5-5.4.j for frequencies 1 kHz and 10 kHz.
l. Set up Resolver-Synchro Bridge and variable voltage source for Synchro mode, 0.000 degrees, 50 Hz.
m. Program Model 5388 SIM to Synchro mode, 2V line-to-line.
n. Using **SAR** command, program Model 5388 Simulator to angle 0.000 degrees.
o. Adjust Resolver-Synchro Bridge for an inphase null (0 V) reading on the phase angle voltmeter.
p. Calculate correction data as follows:

Correction Data = (*programmed angle - bridge angle*)

q. Using **SSLC** command, program Model 5388 to send and load correction data.
r. Verify that correction data was sent by using **SSSC** command.
s. Repeat steps 5-5.4.o through 5-5.4.s for angles 20^{o} through 350^{o} in 10^{o} steps.
t. Repeat steps 5-5.4.o through 5-5.4.t for line-to-line voltages 12, 12.1, 26, 26.1, and 90.
u. Repeat steps 5-5.4.o through 5-5.4.u for frequencies 400 Hz and 1 kHz.

SECTION 6

TROUBLESHOOTING

6-1 INTRODUCTION

This section contains troubleshooting procedures for the Model 5388. A list of typically correct measurements and corresponding faulty components is contained in tables 6-1 - 6-6. The faulty components listed occur as a result of failures encountered during checkout tests, alignments, and during normal operation.

6-2 TROUBLESHOOTING PROCEDURES

The troubleshooting procedures are arranged in three sections and pertain to the following:

a. Communication Problems
b. Simulator Problems
c. Angle Position Indicator Problems

When a failure is encountered during checkout tests, alignment, or during normal operation of the Model 5388, perform the steps in the following subparagraphs to isolate the faulty circuit.

During the troubleshooting process, refer to the detailed schematic and interconnection diagrams, parts location diagrams, and table 1-3 for test equipment specifications.

WARNING

Dangerous voltages may be present in the unit when the side cover is removed.

CAUTION

The Model 5388 is electrostatically sensitive. Failure to comply with safeguards could damage the equipment. Refer to DOD-HDBK-263 for ESD sensitive equipment handling procedure.

6-3 PRELIMINARY PROCEDURES

In the troubleshooting procedures that follow, it is necessary for the Model 5388 under evaluation to be mounted on an extender card to gain access to appropriate test points. Perform the following steps before proceeding with any troubleshooting procedures:

a. Turn off power to VXI card cage.
b. Slide Model 5388 out of VXI card cage.
c. Install extender card into card cage.
d. Install Model 5388 into extender card.
e. Turn on power to VXI card cage.

6-4 COMMUNICATIONS TROUBLESHOOTING

The following troubleshooting procedures isolate problems with the VXIbus, the microprocessor section, and VXIbus-to-host communications of the Model 5388.

See table 6-1 for Synchro-to-Digital Troubleshooting procedures and table 6-2 for PAL Decode Test.

6-5 SIMULATOR TROUBLESHOOTING

The following troubleshooting procedure isolates problems in the Simulator such as no signal output or incorrect angle readings.

NOTE

The following troubleshooting procedure assumes communications between host and Model 5388 are possible. If not, refer to paragraph 6-4.

To troubleshoot the Model 5388 Simulator, proceed as follows:

1. Send the following command string to the Model 5388:

   SS SI *26* **SL** *12* **SF** *400* **SAR** *45*

2. Apply 26 V at 400 Hz to the REF input J1 pins 5 (HI) and 6 (LO).
3. Using a DMM, check test points and components as described in table 6-3 and replace components as necessary.

Table 6-1. Synchro-to-Digital Troubleshooting

Step #	Procedure	If YES Step	If NO Step
1	Reset Slot 0 Controller Circuit Card Assembly (CCA). (Self-Test is initialized).		
2	Slot 0 CCA fails Self-Test, FAIL LED does not light.	6	3
3	Slot 0 CCA fails Self-Test, FAIL LED lights and stays lit.	15	4
4	Slot 0 CCA passes Self-Test, but communication fails.	20	5
5	For all other failures and general checkout procedures go to PAL Decode Test, Table 6-2.		
6	Using an oscilloscope, monitor signal -MRESET (A1U19-20) while toggling Slot 0 CCA reset function. Signal should toggle when reset function toggles.	8	7
7	Using an oscilloscope, trace signal back through path A1U16-6, A1U16-2, A2U4-6, A2U4-11, A2U5-5, and A2U5-15. Signal should toggle at each point when reset function is toggled. If not, replace devices as needed.	8	
8	Using an oscilloscope, monitor signal -MHALT (A1U19-19) while toggling Slot 0 CCA reset function. Signal should toggle when reset function is toggled.	10	9
9	Using an oscilloscope, trace signal back through path A1U16-4, A1U16-2, A2U4-6, A2U4-11, A2U5-5, and A2U5-15. Signal should toggle at each point when reset function is toggled. If not, replace devices as needed.	10	
10	Using an oscilloscope, verify that pin A1U19-15 is a 10 MHz clock pulse.	14	11
11	Using an oscilloscope, verify that pin A1U13-14 is a 10 MHz clock pulse.		12
12	Using an oscilloscope, verify that signal CLK20 (A1U13-2) is a 20 MHz clock pulse.		13
13	Using an oscilloscope, verify a 20 MHz clock at Oscillator A1Y1-3. If not, check the following A1 CCA devices: Y1, U5, U13, and U7.	14	
14	Using an oscilloscope, monitor microprocessor signal -MDTACK (A1U19-10). There should be activity on this signal. If not, check the following A1 CCA devices and replace as needed: U7, U39, U26, U13, U33, and U19.	15	
15	Does A2 LED code =1?	21	16
16	A2 LED code =2? Timer Test has failed.	17	18
17	Remove DSP (A1U1). Reset Slot 0 CCA. If A2 LED code = 4, reinstall or replace A1U1 (DSP). If not, check the following A1 CCA devices and replace as needed: U53, U13, U7, U26, U33, U18, U20, and U19.		
18	A2 LED code =3? If yes, Status Port Test has failed. Check VXI CCA (A2) and the following A1 CCA devices. Replace as needed: U62, U33, U26, U20, U22, U23, U27, and U19.		19
19	A2 LED code = 4 then DSP Download Test has failed. Check the following A1 CCA devices and replace as needed: U1, U21, Y1, U5, U26, U33, U15, U20, and		20

Table 6-1. Synchro-to-Digital Troubleshooting (Continued)

Step #	Procedure	If YES Step	If NO Step
	U19.		
20	Remove VXI CCA (A2) and replace with new VXI CCA (A2). Repeat steps 1 through 19. If VXI communications function, repair non-functioning VXI CCA (A2) as necessary.	1	
21	RAM Test has failed. Check the following A1 CCA devices and replace as needed: U79, U81, U7, U39, U10, U18, U27, U20, U22, and U19.		

Table 6-2. PAL Decode Test

NOTE

Each of the following procedural steps will generate a single negative-going pulse within the range of 100 to 400 nanoseconds duration on the indicated pin. It is recommended that the pin(s) be monitored with a Logic Analyzer or Storage Oscilloscope.

Step #	Command/Comment	Device/Pin #
1	Enter **GAL** command to begin test (refer to 3-4.1).	NOTE: All ICs are on A1 CCA.
2	Type: **TFR 000000**	U39-23, U39-14
3	Type: **TFR 040000**	U39-22, U39-14
4	Type: **TFW 100000 FFFF**	U39-21, U39-14
5	Type: **TFW 108000 FFFF**	U39-20, U39-14
6	Type: **TFR 110000**	U39-19, U39-14
7	Type: **TFW 110000 0000**	U39-18, U39-14
8	Type: **TFR 118000**	U39-17, U39-14
9	Type: **TFR 120000**	U39-16
10	Type: **TFW 128000 0000**	U39-15, U39-14
	If any of steps 2 through 10 fail, check the following A1 CCA devices and replace as needed: U39, U7, U23, U27, U33, and U19.	

Table 6-2. PAL Decode Test (Continued)

Step #	Command/Comment	Device/Pin #
11	Type: **TFR 200000**	U26-23, U26-14
12	Type: **TFR 208000**	U26-22, U26-14
13	Type: **TFR 210000**	U26-21, U26-14
14	Type: **TFW 218000 FFFF**	U26-20, U26-14
15	Type: **TFR 220000**	U26-19, U26-14, U26-15
16	Type: **TFR 228000**	U26-18, U26-14, U26-15
17	Type: **TFR 230000**	U26-17, U26-14, U26-15
18	Type: **TFR 238000**	U26-16, U26-14, U26-15
	If any of steps 11 through 18 fail, check the following A1 CCA devices and replace as needed: U26, U7, U23, U27, U33, and U19.	

Table 6-3. Simulator (CCA A1) Troubleshooting Chart

Step	Test Point/Pin to be Tested	Correct Measurement	Possible Failure
1	TP3	1.3 V rms	U28,Z5
2	U34 Pin 6	4.0 V rms	U34,U30,K11,Z15
3	U29 Pin 6	4.0 V rms	U29,U30,K11
4	TP28	4.0 V rms	U43,U59
5	TP17	4.0 V rms	U43,U59
6	TP15	3.83 V rms	U49
7	TP7	3.83 V rms	U35
8	U58 Pin 7	3.83 V rms If incorrect, short TP19 to ground. If still incorrect, go to STEP 12	U58,Z15
9	TP26	11.484 V rms	U66,Z27,C119,C120
10	U56 Pin 7	3.83 V rms If incorrect, short TP19 to ground. If still incorrect, go to STEP 14	U56,Z9
11	TP25	11.484 V rms	U65,Z25,C105,C106
12	TP12	.533 V rms	K7,K8,U57,Z11,Z13
13	TP11	3.83 V rms	K9,K10,Z12,U42
14	TP8	.533 V rms	K7,K8,U55,Z6,Z7
15	TP4	3.83 V rms	K5,K6,Z8,U41

6-6 API TROUBLESHOOTING

The API troubleshooting procedures are divided into two main sections:

a. Bridge Circuit
b. Null Circuit

These two sections are addressed with separate troubleshooting procedures. It should be noted that these two sections do interact so a special command is available to disable the Null circuit from causing any change in the Bridge setting. The special command string is as follows:

AMA <*value*>**<CR><LF>**

where: 0 < *value* < 359.999

The **AMA** command causes the Bridge to be set to <*value*> and also to inhibit interrupts to the DSP. This allows the independent troubleshooting of the Bridge and the Null circuits.

6-6.1 Bridge Circuit Troubleshooting

Procedure. To troubleshoot the Bridge circuit, proceed as follows:

1. Send the following command string to the Model 5388:

   AR AL *90* **AMA** *45*

2. Apply 26 V at 400 Hz to the J1 REF input (pins 5 and 6).
3. Apply a 90 V line-to-line, 45.000 degree Resolver signal to Signal inputs J1 S1 - S4 (pins 1 - 4).
4. Using a DMM, check test points and components as described in table 6-4 and replace components as necessary.

Table 6-4. Bridge Circuit (A1) Troubleshooting Chart

Step	Test Point/Pin to be Tested	Correct Measurement	Possible Failure
1	TP31	2.83 V rms	U73,Z32,Z33
2	TP30	2.83 V rms	U72,Z29,Z28,K15
3	TP33	2.83 V rms	U68,U60,Z31
4	TP19	2.83 V rms	U50,U60,Z17
5	U14 Pin 5	2.00 V rms	U14
6	U15 Pin 5	2.00 V rms	U15
7	TP18	0.00 V rms	U24,U36,U37

This procedure checks the Bridge circuitry at 45 degrees. It is possible for the Model 5388 to pass this test and still have a problem in the Bridge. If the problem exists at a known angle, use the **AMA** command at that angle. Test point A1TP18 should go to zero volts whenever the incoming angle and the Bridge angle are equal. If not, this indicates a problem in the API Bridge circuit.

Most subtle problems will probably be associated with multiplying DACs A1U14 and A1U15. Another special command is available to check the DACs. The command string is as follows:

ADAC <*value*> **<CR><LF>**

where: <*value*> is a hex number representing the DAC programmed value

For example:

ADAC *FFFF* Sets both DACs to full-scale LSB.
ADAC *8000* Sets both DACs to half-scale.
ADAC *0000* Sets both DACs to zero.

With the **ADAC** command it can be determined if the input-to-output ratio of the DAC is working properly.

6-6.2 Null Circuit Troubleshooting Procedure. The Null circuit can be programmed for two different frequency ranges by setting analog switches A1U31 and A1U44. If a problem appears only in one frequency range then the associated components are suspect. Table 6-5 lists which components are used for each frequency range.

Table 6-5. Null Circuit Frequency Ranges and Associated Components

Frequency Range	Associated Components (A1)
360 Hz - 10 kHz	R27,C81,C84, and C75
47 Hz - 359 Hz	R32,C86,C85,C75,C78, and C77

a. Null circuit. To troubleshoot the Null circuit, proceed as follows:

(1) Apply appropriate input and Reference signals (J2 pins 5 and 6).

(2) Using an oscilloscope, check A1U44 pin 6 for an internal reference square wave.

(a) The square wave should be 5 V in amplitude at the frequency of the Reference signal.
(b) If the square wave is missing, the problem is in the Autophase circuit.

b. Phase Detector. The output of the Phase Detector is a full wave detection of the error signal. To check this, proceed as follows:

(1) Send the following command string to the Model 5388:

AR AL *90* **AMA** *45*

(2) Apply a 90 V line-to-line Resolver signal set to 45 degrees to input terminals S1 - S4 (J2 pins 1 - 4).
(3) Using a DMM, measure 2 Vrms at TP18. (Note: The Null circuit operates with a constant error sensitivity of 2 V per degree.)
If reading is correct, the Bridge is functioning. If reading is incorrect, the problem is in the null circuit.
(4) Using an oscilloscope, measure a full wave 2.8 V peak rectified signal at A1U44 pin 4.
(5) If the input angle is changed to 44 degrees, A1U44 pin 4 should measure -2.8 V peak.

6-6.3 Autophase Circuit Troubleshooting Procedure. The Autophase circuit generates an internal signal from the input signal. To check the Autophase circuit, proceed as follows:

a. Send the following command to the Model 5388:

AR AL *90* **AMA** *0*

b. Apply a 90 V line-to-line resolver input signal set to 0 degrees to the input terminals S1 - S4 (J2 pins 1 - 4).
c. Using a DMM and oscilloscope measure the values listed in table 6-6 and replace components as necessary.

Table 6-6. Autophase Circuit (A1) Troubleshooting Chart

Step	Test Point Pin to be Tested	Correct Measurement	Possible Failure
1	TP36	12 V Square Wave	U77
2	U51 Pin 1	0.00 V rms	U51,U69
3	U51 Pin 7	4.00 V rms	U51,U69
4	U45 Pin 7	0.00 Vdc	U45,Z22,D2,D1
5	U45 Pin 14	3.62 Vdc	U45,Z21,D3,D22
6	TP34	-12 Vdc	U74,Z34
7	U51 Pin 8	Full Wave Rectified 5.6 V Peak	U51,U70
8	TP37	-12 Vdc	U61,U74
9	U70 Pin 11	4.00 V rms	U70
10	TP35	12 V Square Wave	U77

SECTION 7

PARTS LIST

7-1 INTRODUCTION

This section contains replaceable parts lists and parts location diagrams for the Model 5388.

7-2 PARTS LIST

The parts list contains replaceable parts for the Model 5388. Other, non-replaceable parts may be shown because the parts lists is generated from the North Atlantic internal manufacturing database It is prepared in tabular form and divided into three columns as follows:

7-2.1 Column 1 - Ref Des. Reference designations. Lists alphanumerical reference designations for circuit card assembly replaceable parts shown on schematic and parts location diagrams.

7-2.2 Column 2 - Description. Contains descriptions which identify replaceable parts and in most cases identify manufacturer and manufacturer's part number as it appears in our internal database.

7-2.3 Column 3 - NAI P/N. Lists North Atlantic Instruments part numbers assigned to replaceable parts.

7-3 Paragraph not used

7-4 PARTS LOCATION ILLUSTRATIONS

Parts location illustrations are provided to give the user a quick and positive method for locating parts on specific assemblies being repaired. Each illustration provides reference designations for circuit card components.

The following inserted pages contain Parts Lists and Parts Location Diagrams as shown below:

Table 7-1. Model 5388 Top Assembly Parts List 5388-F11 (Use Parts List 5388B006-1)
Table 7-2. Model 5388 Top Assembly Parts List 5888-F12 (Use Parts List 5388B006-2)
Model 5388 Top Assembly Parts List 5388-F21 (Use Parts List 5388B006-1)
Model 5388 Top Assembly Parts List 5388-F22 (Use Parts List 5388B006-2)

Figure 7-1. Model 5388 Top Assembly Parts Location Diagram 5388B006

NORTH ATLANTIC PARTS LIST FOR: 5388B006-1 6/1/199
PG: 1

ASSY,VXI-CARD"
REV: A

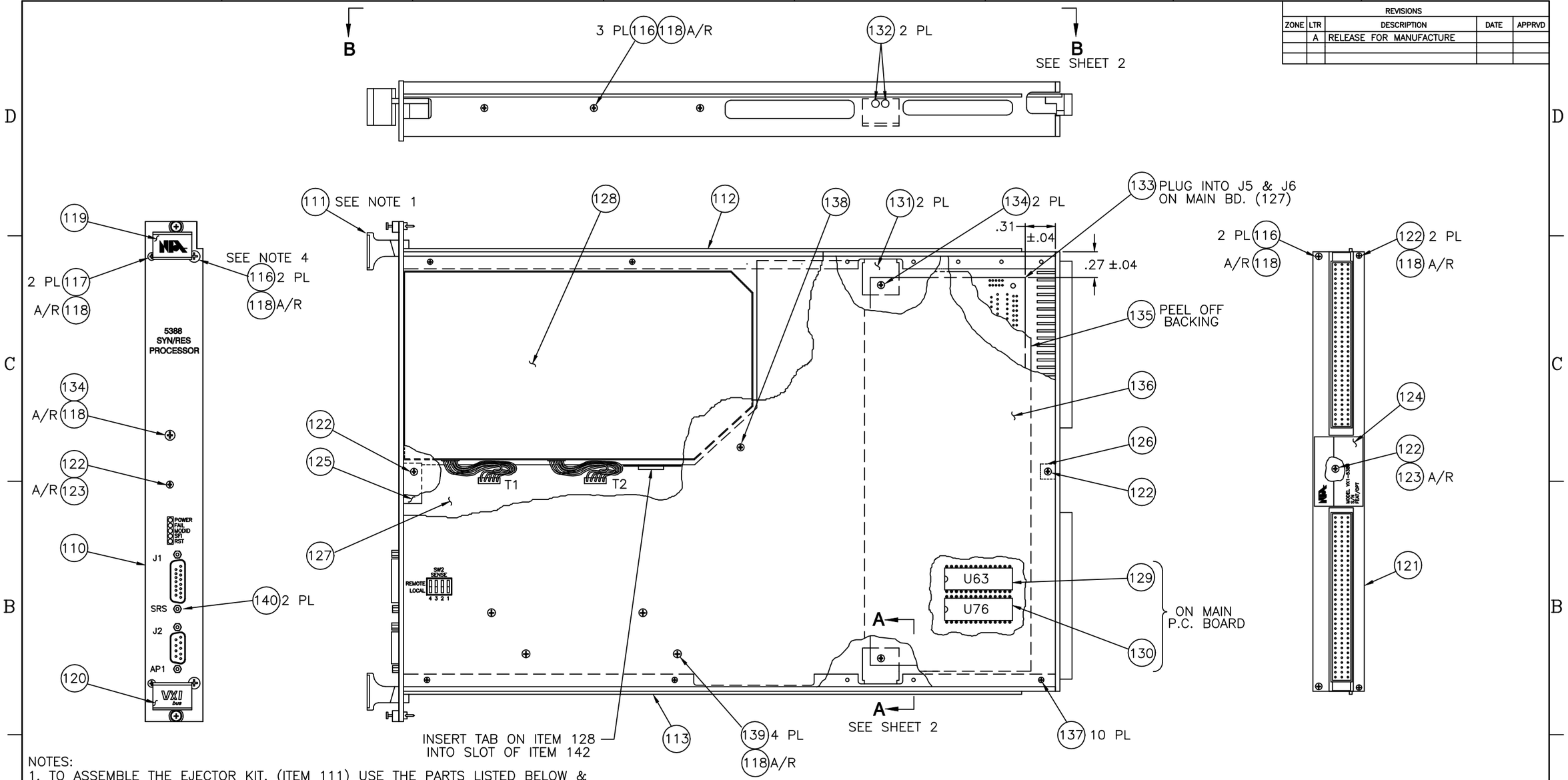
REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
SHIP WITH UNIT	KIT,MATING CONNECTOR MODEL 5388	784022	1
U63	IC,PROGRAMMED REV.B,BLANK=889380	600036	1
U76	IC,PROGRAMMED EPROM & REV.B,BLANK=889380	600037	1

NORTH ATLANTIC PARTS LIST FOR: 5388B006-2 6/1/199
PG: 1

ASSY,VXI-CARD"
REV: A

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART -	QTY
SHIP WITH UNIT	KIT,MATING CONNECTOR MODEL 5388	784022	1
U63	IC,PROGRAMMED REV.B,BLANK=889380	600036	1
U76	IC,PROGRAMMED EPROM & REV.B,BLANK=889380	600037	1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPRVD
	A	RELEASE FOR MANUFACTURE		



NOTES:
1. TO ASSEMBLE THE EJECTOR KIT, (ITEM 111) USE THE PARTS LISTED BELOW & ITEMS 114 & 115 (SECTION C–C). TO ASSEMBLE, SEE NOTE 4.
   - (2) EJECTOR HANDLE
   - (2) ID PLATE
   - (2) EJECTOR HANDLE MTG. BRACKET
   - (2) CAPTIVE SCREW
   - (2) PLASTIC RETAINER
2. IF FEATURE 1, OPTION 2 IS SELECTED, SEE TEST PROCEDURE 758482–1 TO ENABLE OPTION.
3. ITEM 128 & 129 ARE TO BE SHIPPED WITH UNIT IN A KIT BAG AND NOT INSTALLED.
4. WHEN ASSEMBLING FRONT PANEL TO THE RAILS (ITEMS 112 & 113), LEAVE ITEMS 116 & 117 LOOSE UNTIL ITEMS 114 & 115 ARE INSTALLED. USE NEEDLE NOSE PLIERS TO PLACE HEX NUT (ITEM 114) INTO EJECTOR HANDLE. ASSEMBLE SCREW (ITEM 115) INTO TO EJECTOR HANDLE AND THEN TIGTHEN ITEMS 116 & 117, THEN APPLY ITEM 118.

COMPUTER GENERATED DOCUMENT
NO MANUAL CHANGES PERMITTED

SHEET	REVISION
STATUS OF SHEETS	

NEXT ASSY	USED ON
5388B006–5	5388–S3422
5388B006–4	5388–S3420
5388B006–3	5388–S3467
5388B006–2	5388–F12
5388B006–1	5388–F11
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
FRACTIONS ± 1/64
ANGLES ± 1/2 °
DEC. .XX ± 0.02
DEC. .XXX ± 0.005

MATERIAL: SEE P/L 5388B006–*
FINISH: –

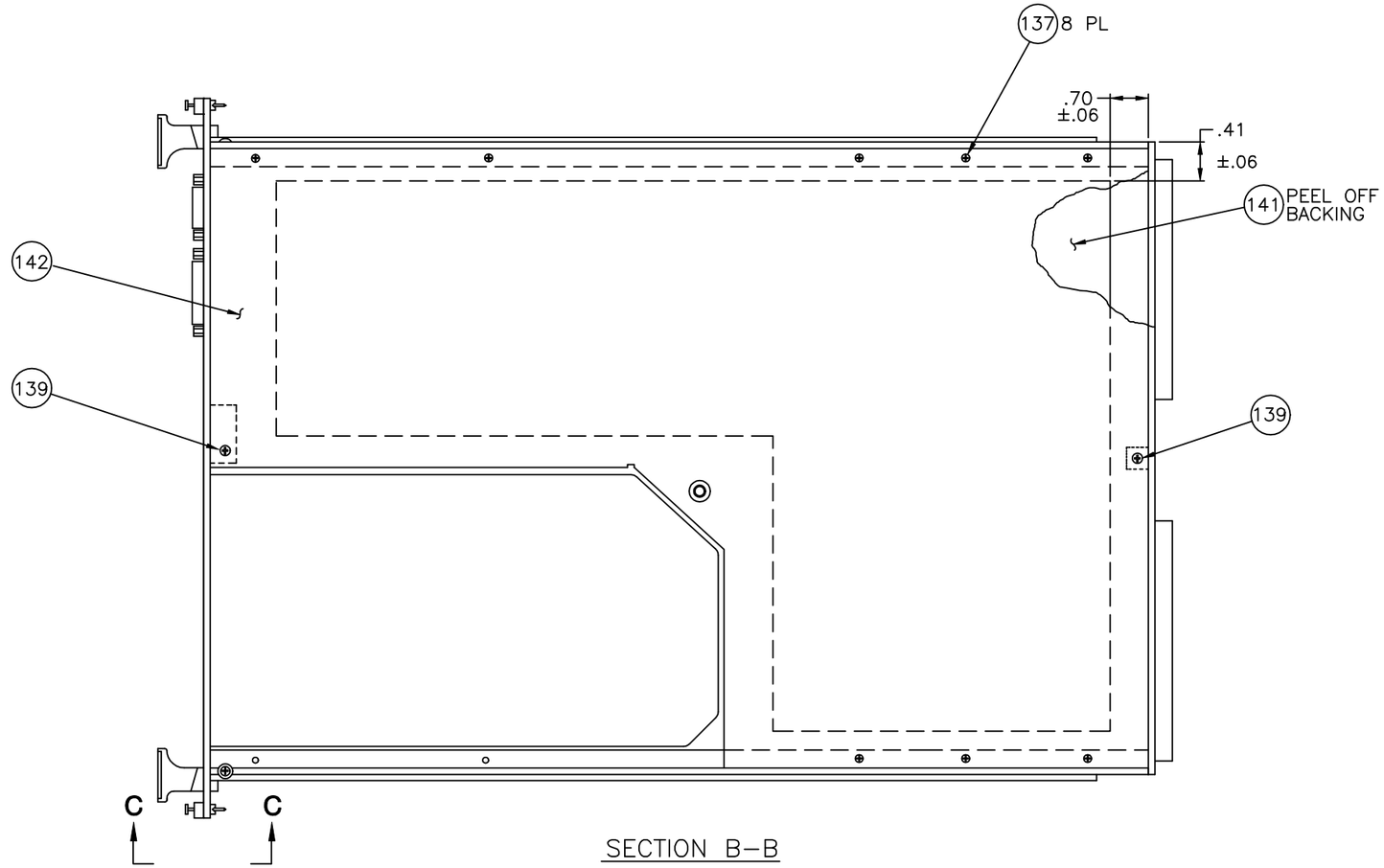
CONTRACT NO.
DRAWN: M. Lewandowski DATE 4/6/98
CHECKED:
A
P
P
D

north atlantic instruments, inc.
170 Wilbur Place, Bohemia, New York 11716-2416

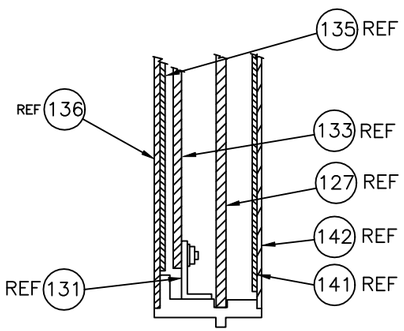
ASSEMBLY, D/S–S/D MODEL 5388

SIZE	CODE ID NO.		REV
D	ØVGU1	5388B006	A
SCALE NONE		SHEET 1 OF 2	

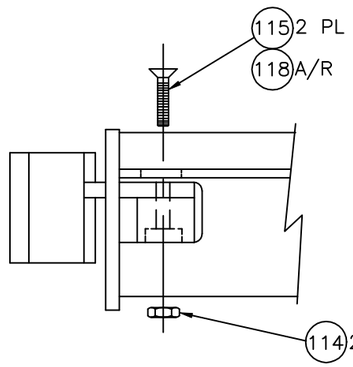
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPRVD



SECTION B–B



SECTION A–A
SCALE: NONE



SECTION C–C
SCALE: NONE
SEE NOTE 4

COMPUTER GENERATED DOCUMENT
NO MANUAL CHANGES PERMITTED

SIZE	CODE ID NO.		
D	ØVGUI	5388B006	A REV
SCALE NONE		SHEET 2 OF 2	

The following inserted pages contain Parts Lists and Parts Location Diagrams as shown below:

Table 7-3. Mother Circuit Card Assembly Parts List 784048-1
Table 7-4. Mother Circuit Card Assembly Parts List 784048-2

Figure 7-2. Mother Circuit Card Assembly Parts Location Diagram 784048

NORTH ATLANTIC PARTS LIST FOR: 784048-0001 6/1/199
PW,ASSY,D/S-S/D,IAC,400-10KHZ"
REV: A

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
C40,41,48,122	CAP,CER,.0039UF,100V,5%,X7R,AX C410C392J1R5CA,KEMET"	889641	4
42,49	CAP,CER,.0047UF,100V,+-10% CK12BX472K	804841	2
38,44	RES,MF,20K,1%,1/8W,50PPM RN55C2002F	810098	2
R5,15	RES,MF,8.25K,1%,1/8W,100PPM RN55D8251F	807017	2

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
C1-C11,14,15,16,19-28,30,31,32,33,34,36,37,38,39,44,45,46,47 50,51,52,54,56,57,59,62-66,69,71,72,73,79,80,82,87-97,100 101,104,103,107,108,111,113,114,117,118,121,123-125,127,129	CAP,CER,.1UF,50V,20%,Z5U,AXIAL SA105E104MAA,AVX	885498	104
C109,110,115,116	CAP,TANT-NON,10UF,35V,10% TDC106K035NSF,MALLORY	810168	4
C12,13,17,18,29,55,58,60,61,67,68,105,106,119,120,128,134, 146,147	CAP,TANT-POL,10UF,25V,20%,RADI 199D106X0025CA1,SPRAGUE	888849	19
C158	CAP,CER,.0018UF,100V10%X7R,RAD AVX/KEMET	CK05BX182K	1
C161	CAP,CER,22PF,200V,+-10%,X7R CK05BX220K	886399	1
C162,163	CAP,MICA,1PF+-.5PF,300V CD5CC010D03,CORNELL DUBILIER	811426	2
C35,43,102,112,126,133,137,141	CAP,VAR,.25-1.5PF,MINI TYPE 273-0001-101,EF JOHNSON	889576	8
C53,70,142	CAP,CER,6PF,200V,+-5%,NPO,AXIA SA102A6R0DAA,AVX,C114G629D2G5C	889643	3
C74	CAP,CER,.056UF,50V,10%,Z5U,AXI C412C563K5U5CA,KEMET OR 5R5CA	889633	1
C75	CAP,CER,100PF,100V+-10%,X7R CK12BX101K	889632	1
C76	CAP,CER,390PF,100V+-10% CK12BX391K	805045	1
C77	CAP,CER,.82UF,50V,+-10% CK06BX824K	805076	1
C78,81	CAP,CER,.33UF,50V,10%,X7R,RAD CK06BX334K	888851	2
C83,143,149,159	CAP,MATCHED,CER,1UF,50V,5% C062C105J5R5CA SELECT 805155	886073	4
C84,99	CAP,CER,.068UF,50V+-10%,Z5U,AX C412C683K5U5CA,KEMET OR 5R5CA	889636	2
C85	CAP,CER,.082UF,50V,10%,X7R,AXI C412C823K5R5CA,KEMET	889638	1
C86	CAP,CER,.39UF,50V,10%,X7R,RAD CK06BX394K	888853	1

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
C98	CAP,AL-EL,100UF,16VDC,+-20% 500D107M016CB2,SPRAGUE	889028	1
D1-5,10,11,12,13,14,15,16,17,18,19,20,21,22	DIODE,SIG,PIV75V,0.010A,4nS 1N4148 OR 1N4153	808974	18
D6,7,8,9	DIODE,RECT,PIV100V,1A 1N4002,MOTOROLA	880112	4
J1	CONN,"D",9-POS,PLUG,RT.A,318MT 1-747250-0 or 747250-4,AMP	889163	1
J2	CONN,"D",15-POS,RCPT,RT.ANGLE 1-745782-2,AMP ONLY	889143	1
K1-K15	RELAY,2 FORM C,12V,1A,NO-LATCH A12W-K,ITT,EA2-12,NEC(NO COTO)	888825	15
LED1,4,5	LED,RED,RECTANGULAR CASE 547-2007,DIALIGHT &	888904	3
LED2,3	LED,GRN,RECTANGULAR CASE 547-2303,DIALIGHT	888903	2
P1,2	CONN,DIN,TYPE-C,96-POS,RT.ANGL 532505-1 or 650473-5,AMP	887395	2
P5,6	CONN,HDR,30-POS,100CTR,2ROW MTSW-130-22-TD-410,SAMTEC	888902	2
R1,81	RES,MF,15K,1%,1/8W,25PPM RN55E1502F	882467	2
R10	RES,MF,5.9 OHM,1%,1/4W 5063JD5R90F,MEPCO CENTRALAB	810899	1
R11,12,13,36,48,52,56	RES,MF,1 OHM,5%,1/3W 5063JD1R000J,MEPCO	889019	7
R18,21,53,61,62,67,73	RES,MF,10K,1%,1/8W,25PPM RN55E1002F	882477	7
R2,50,51	RES,VAR,50OHM,10%100PPM,25TURN 3299W-1-500,BOURNS &	810193	3
R23	RES,MF,71.50K,1%,1/10W,50PPM	RNC55H7152F	1
R24,74	RES,MF,100 OHM,1%,1/8W,50PPM RNC55H1000FS	808143	2

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
R25	RES,VAR,100K,10%,0.5W,TRIM,25T 3299W-1-104 BOURNS ONLY &	810612	1
R26	RES,MF,90.90K,1%,1/8W,50PPM RN55C9092F	808185	1
R27	RES,MF,133K,1%,1/8W,100PPM RN55D1333F	807639	1
R3,4,8,19,20,22,35,43,47,49,54,55,78	RES,VAR,10 OHM,10%,1/2W,TRIM 3299W-1-100,RJR24FW100,22TURN&	888826	13
R30,31,60,63,65,69	RES,MF,1K,1%,1/8W,50PPM RN55C1001F	807464	6
R32	RES,MF,232K,1%,1/10W,100PPM RN55D2323F	888486	1
R33	RES,MF,40.20K,1%,1/8W,100PPM RN55D4022F	806987	1
R34	RES,MF,82.5K,1%,1/8W,50PPM RN55C8252F	806555	1
R37,45	RES,CMPSN,10M,5%,1/4W RCR07G106JS,RLR07C1005G	803389	2
R39,42	RES,WW,0.499 OHM,1%,1W RWR81SR499FR	889018	2
R40,41	RES,VAR,5K,10%,1/2W,TRIM,25TRN 3299W-1-502,BOURNS &	883066	2
R46	RES,CMPSN,5.10 OHM,5%,1/4W RC07GF5R1J	883171	1
R57,64	RES,MF,9.09K,1%,1/8W,50PPM RN55C9091F	884642	2
R58,70,76	RES,CMPSN,1M,5%,1/4W RCR07G105JS,RLR07C1004G	880100	3
R59,66	RES,MF,100K,1%,1/8W,50PPM RN55C1003F	806492	2
R6,14,28,29,68,72	RES,MF,200K,1%,1/8W,50PPM RN55C2003F	807694	6
R7,17	RES,MF,499K,1%,1/4W,50PPM RN60C4993F	806929	2

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
R71	RES,MF,3.32K,1%,1/8W,50PPM RN55C3321F	807631	1
R75	RES,CMPSN,100K,5%,1/4W RCR07G104JS,RLR07C1003GS	880846	1
R77	RES,MF,511 OHM,1%,1/10W,50PPM	RNC55H5110F	1
R80	RES,MF,20M,1%,1/10W,50PPM	RN55C2005F	1
R9,16	RES,MF,1.58K,1%,1/10W,100PPM RN55D1581F	889020	2
SKT,U63,76	SKT,IC,28-POS,LOW PRO,.6SPACNG ICO-628-NGT,SAMTEC	889161	2
SOCKET,U19	SOCKET,PLCC,68-POS,SQUARE QILE68P-410T,BURNDY	888847	1
SW1	SW,DIP,PIANO,4POS,SEALED,0.48" 76PSB04S,GRAYHILL	808518	1
T1,2,JP1&2,JP13&14,JP15&16	CONN,HDR,PRSFIT,SGLROW,6POS 104426-4,AMP	811425	3
TP1-39	CONN,TEST POINT,BLK,LOOPED 5001,KEYSTONE,TP-105-01-00	811348	39
U1	IC,DSP,24BIT,40MHZ DSP56002FC40 MOTOROLA &	810607	1
U10	IC,TTL,INVERTER,HEX 04,SN74ALS04N &	886134	1
U11,12,46,52	IC,CMOS,TRANSCVR,OCTAL,3STATE 245,SN74HCT245N/AN &	889157	4
U13	IC,TTL,CNTR,BINARY,UP,SYNCHRON 161,SN74ALS161BN,TI	888848	1
U14,15,35,49	IC,DAC,16-BIT,VOLT.OUT,DIP 28P 7846,AD7846KN,AD &	888822	4
U16	IC,TTL,INVERTER,HEX,1-INPUT 05,SN74ALS05N	888775	1
U17	IC,TTL,DECODER,3TO8LINE,ADVNCD 138,SN74ALS138N,TI	886107	1

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
U18,23,27,33	IC,TTL,BUFFER,OCTAL,3STATE 244,SN74ALS244N,TI	886109	4
U19	IC,MICROCOMPUTER,CPU,68000 68000,MC68000FN10,MOT NC/NR	888791	1
U2	IC,PROGRAMMED REV.B,BLANK=888783	889023-1	1
U20,22	IC,TTL,TRANSCVR,OCTAL,3STATE 245,SN74ALS245N,TI	886110	2
U21	IC,CMOS,FLIP-FLOP,D,DUAL,POS 74,74HCT74N,NAT	889158	1
U24	IC,OPAMP,SR25V/us,GBW8M,Vos.2m 16,OP16EZ,PMI/AD ONLY	886495	1
U25,31,43,44,47,48,60,61,69,70,83	IC,SW,2-SPDT,Ron50,+-15V,14DIP 303,DG303ACJ,SILICONIX	888824	11
U26	IC,PROGRAMMED REV.B,BLANK=810692,TIBPAL22V10	889026	1
U28,50,56,58,59,67,68,72,73	IC,OPAMP,DUAL,SR3V/us,Vos.5mV 5102,HA3-5102-5,HAR	889008	9
U29,34,41,42,64	IC,OPAMP,SR2.8V/usGBW8M,Vos10u 27,OP-27GZ,PMI &	886028	5
U3	IC,PROGRAMMED REV.B,BLANK=888783	889023-2	1
U30,36	IC,DAC,14-BIT,uP COMPAT,DIP24P 7538,AD7538JN,AD &	888821	2
U32,74	IC,COMP,DUAL,BI-POLAR,PLAS-DIP 393,LM393N,MOT	884448	2
U37	IC,OPAMP,SR100V/us,GBW16MHz 845,AD845KN,AD &	810129	1
U38,45,51	IC,OPAMP,LO-PWR,SR13V/us,GBW3M 084,TL084ACN,TI ONLY	808735	3
U39	IC, PAL,20L10,PROG REV.B,BLANK=810692	889027	1
U4	IC,PROGRAMMED REV.B,BLANK=888783	889023-3	1

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
U40	IC,EEPROM,8KX8,28PINDIP,CMOS 28,AT28C64-25PC,ATMEL OR =	889272	1
U5	IC,CMOS,NAND GATE,QUAD,2-INPUT 00,SN74HCT00N,TI	810384	1
U53	IC,MICROPROC,6800,TIMER,PROGRM 40,MC68A4OP,MC68B40P,MOT OR =	889160	1
U54	IC,CLOCK,VCO WAVE GENENRATOR 8038,ICL8038CCJD,HAR ONLY	886172	1
U55,57	IC,OPAMP,DUAL,VERY LOW NOISE 270,OP270FZ,PMI	888820	2
U6	IC,CMOS,FLIP-FLOP,D,HEX,QUAD 175,SN74HCT175N,	889156	1
U62	IC,CMOS,BUFFER,OCTAL,TRI-STATE 244,SN74HCT244N,orSN74HCT244E	886192	1
U65,66	IC,OPAMP,HI-PWR,SR10V/us,TO-3 541,OPA541AM,BB &	888823	2
U7	IC,PROGRAMMED REV.A,BLANK=888996	889025	1
U71,78	IC,TTL,FLIP-FLOP,D,OCTAL,3STAT 574,SN74ALS574BN	888779	2
U75,80	IC,INTERFACE,DRIVER,7-CHANNEL 1413,MC1413P,new # MCT1413P	808900	2
U77	IC,COMP,DUAL,HI-SPEED 319,LM319N,NAT	883244	1
U79,81	IC,RAM,8Kx8,20 OR 25ns,28PIN 7164,IDT7164S25TP(20TP),IDT	888797	2
U8	IC,TTL,ENCODER,8-3LINE,OCTAL 148,SN74LS148N	883508	1
U9	IC,PROGRAMMED REV.A,BLANK=888855	889024	1
Y1	OSC,20Mhz,CMOS,4P DIP 8 PIN PK 531P-20MHZ,EPSON,SE1212,DIGIKY	810046	1
Z1,2,4	RES,NET,BUS,SIP,3.30KX9,10P 4310R-101-332 &	886057	3

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
Z10,16,17,31	RES,NET,10K PAIR,.005% REV.B	888811	5
Z11	RES,NET,BUS,SIP,3.90KX5,6P,2% BOURNS,100PPM &	4306R-101-392	1
Z18	RES,NET,ISO,SIP,10KX4,8P,1W 4608X-102-103,BOURNS &	889166	1
Z19	RES,NET,ISO,SIP,100KX3,6P,.75W L06-3C104 BKMN/4306R-102-104 &	887978	1
Z21,22	RES,NET,ISO,SIP,100KX4,8P,1W 4308R-102-104,BOURNS &	808628	2
Z23,34	RES,NET,ISO,SIP,3.30KX4,8P,1W 4608X-102-332,BOURNS &	889167	2
Z24	RES,NET,ISO,SIP,10KX3,6P,0.75W 4606-102-103,BOURNS	889168	1
Z25,27	RES,NET,10K,20K,.005% REV.B	888809	2
Z26	RES,NET,ISO,SIP,18KX4,8P,1W 4308R-102-183,BOURNS	889010	1
Z3	RES,NET,2K,2K,.01%,1PPM REV.A	811374	1
Z30	RES,NET,10K,20K,11.1547K REV.B	888810	1
Z5	RES,NET,3-5K,2-100K,.01%RATIO REV.B	888805	1
Z7,13,29,32	RES,NET,4.4444K,100K,0.005% REV.B	810080	4
Z8,12	RES,NET,1K,6.5K,2.46154K REV.B	888806	2
Z9,14,15,20	RES,NET,10K PAIR,PRECISION REV.B	808859	4

NORTH ATLANTIC PARTS LIST FOR: 784048-0002 06/08/199

PW,ASSY,D/S-S/D,IAC,47-400HZ
REV: A

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
C40,48	CAP,CER,.033UF,50V,+-10% CK05BX333K ^	808839	2
C41,122	CAP,MATCHED,CER,8200PF,100V SELECT FROM CK05BX822K	889898	2
C42,49	CAP,CER,.0068UF,100V10%X7R,RAD AVX/KEMET	CK05BX682K	2
R38,44	RES,MF,200K,1%,1/8W,50PPM RN55C2003F	807694	2
R5,15	RES,MF,20K,1%,1/8W,50PPM RN55C2002F ^	810098	2

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
C1-C11,14,15,16,19-28,30,31,32,33,34,36,37,38,39,44,45,46,47 50,51,52,54,56,57,59,62-66,69,71,72,73,79,80,82,87-97,100 101,104,103,107,108,111,113,114,117,118,121,123-125,127,129	CAP,CER,.1UF,50V,20%,Z5U,AXIAL SA105E104MAA,AVX	885498	104
C109,110,115,116	CAP,TANT-NON,10UF,35V,10% TDC106K035NSF,MALLORY	810168	4
C12,13,17,18,29,55,58,60,61,67,68,105,106,119,120,128,134, 146,147	CAP,TANT-POL,10UF,25V,20%,RADI 199D106X0025CA1,SPRAGUE	888849	19
C158	CAP,CER,.0018UF,100V10%X7R,RAD AVX/KEMET	CK05BX182K	1
C161	CAP,CER,22PF,200V,+-10%,X7R CK05BX220K	886399	1
C162,163	CAP,MICA,1PF+-.5PF,300V CD5CC010D03,CORNELL DUBILIER	811426	2
C35,43,102,112,126,133,137,141	CAP,VAR,.25-1.5PF,MINI TYPE 273-0001-101,EF JOHNSON	889576	8
C53,70,142	CAP,CER,6PF,200V,+-5%,NPO,AXIA SA102A6R0DAA,AVX,C114G629D2G5C	889643	3
C74	CAP,CER,.056UF,50V,10%,Z5U,AXI C412C563K5U5CA,KEMET OR 5R5CA	889633	1
C75	CAP,CER,100PF,100V+-10%,X7R CK12BX101K	889632	1
C76	CAP,CER,390PF,100V+-10% CK12BX391K	805045	1
C77	CAP,CER,.82UF,50V,+-10% CK06BX824K	805076	1
C78,81	CAP,CER,.33UF,50V,10%,X7R,RAD CK06BX334K	888851	2
C83,143,149,159	CAP,MATCHED,CER,1UF,50V,5% C062C105J5R5CA SELECT 805155	886073	4
C84,99	CAP,CER,.068UF,50V+-10%,Z5U,AX C412C683K5U5CA,KEMET OR 5R5CA	889636	2
C85	CAP,CER,.082UF,50V,10%,X7R,AXI C412C823K5R5CA,KEMET	889638	1
C86	CAP,CER,.39UF,50V,10%,X7R,RAD CK06BX394K	888853	1

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
C98	CAP,AL-EL,100UF,16VDC,+-20% 500D107M016CB2,SPRAGUE	889028	1
D1-5,10,11,12,13,14,15,16,17,18,19,20,21,22	DIODE,SIG,PIV75V,0.010A,4nS 1N4148 OR 1N4153	808974	18
D6,7,8,9	DIODE,RECT,PIV100V,1A 1N4002,MOTOROLA	880112	4
J1	CONN,"D",9-POS,PLUG,RT.A,318MT 1-747250-0 or 747250-4,AMP	889163	1
J2	CONN,"D",15-POS,RCPT,RT.ANGLE 1-745782-2,AMP ONLY	889143	1
K1-K15	RELAY,2 FORM C,12V,1A,NO-LATCH A12W-K,ITT,EA2-12,NEC(NO COTO)	888825	15
LED1,4,5	LED,RED,RECTANGULAR CASE 547-2007,DIALIGHT &	888904	3
LED2,3	LED,GRN,RECTANGULAR CASE 547-2303,DIALIGHT	888903	2
P1,2	CONN,DIN,TYPE-C,96-POS,RT.ANGL 532505-1 or 650473-5,AMP	887395	2
P5,6	CONN,HDR,30-POS,100CTR,2ROW MTSW-130-22-TD-410,SAMTEC	888902	2
R1,81	RES,MF,15K,1%,1/8W,25PPM RN55E1502F	882467	2
R10	RES,MF,5.9 OHM,1%,1/4W 5063JD5R90F,MEPCO CENTRALAB	810899	1
R11,12,13,36,48,52,56	RES,MF,1 OHM,5%,1/3W 5063JD1R000J,MEPCO	889019	7
R18,21,53,61,62,67,73	RES,MF,10K,1%,1/8W,25PPM RN55E1002F	882477	7
R2,50,51	RES,VAR,50OHM,10%100PPM,25TURN 3299W-1-500,BOURNS &	810193	3
R23	RES,MF,71.50K,1%,1/10W,50PPM	RNC55H7152F	1
R24,74	RES,MF,100 OHM,1%,1/8W,50PPM RNC55H1000FS	808143	2

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
R25	RES,VAR,100K,10%,0.5W,TRIM,25T 3299W-1-104 BOURNS ONLY &	810612	1
R26	RES,MF,90.90K,1%,1/8W,50PPM RN55C9092F	808185	1
R27	RES,MF,133K,1%,1/8W,100PPM RN55D1333F	807639	1
R3,4,8,19,20,22,35,43,47,49,54,55,78	RES,VAR,10 OHM,10%,1/2W,TRIM 3299W-1-100,RJR24FW100,22TURN&	888826	13
R30,31,60,63,65,69	RES,MF,1K,1%,1/8W,50PPM RN55C1001F	807464	6
R32	RES,MF,232K,1%,1/10W,100PPM RN55D2323F	888486	1
R33	RES,MF,40.20K,1%,1/8W,100PPM RN55D4022F	806987	1
R34	RES,MF,82.5K,1%,1/8W,50PPM RN55C8252F	806555	1
R37,45	RES,CMPSN,10M,5%,1/4W RCR07G106JS,RLR07C1005G	803389	2
R39,42	RES,WW,0.499 OHM,1%,1W RWR81SR499FR	889018	2
R40,41	RES,VAR,5K,10%,1/2W,TRIM,25TRN 3299W-1-502,BOURNS &	883066	2
R46	RES,CMPSN,5.10 OHM,5%,1/4W RC07GF5R1J	883171	1
R57,64	RES,MF,9.09K,1%,1/8W,50PPM RN55C9091F	884642	2
R58,70,76	RES,CMPSN,1M,5%,1/4W RCR07G105JS,RLR07C1004G	880100	3
R59,66	RES,MF,100K,1%,1/8W,50PPM RN55C1003F	806492	2
R6,14,28,29,68,72	RES,MF,200K,1%,1/8W,50PPM RN55C2003F	807694	6
R7,17	RES,MF,499K,1%,1/4W,50PPM RN60C4993F	806929	2

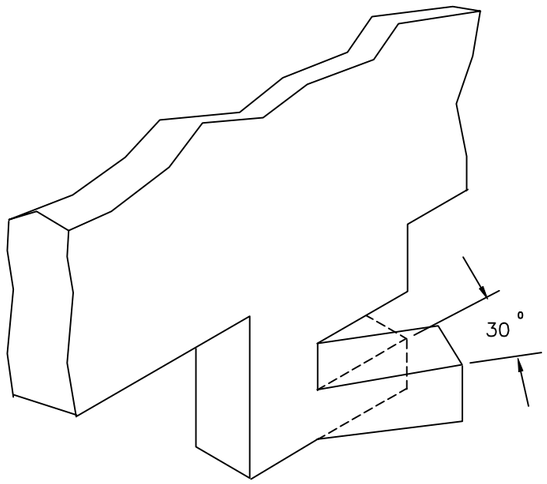
REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
R71	RES,MF,3.32K,1%,1/8W,50PPM RN55C3321F	807631	1
R75	RES,CMPSN,100K,5%,1/4W RCR07G104JS,RLR07C1003GS	880846	1
R77	RES,MF,511 OHM,1%,1/10W,50PPM	RNC55H5110F	1
R80	RES,MF,20M,1%,1/10W,50PPM	RN55C2005F	1
R9,16	RES,MF,1.58K,1%,1/10W,100PPM RN55D1581F	889020	2
SKT,U63,76	SKT,IC,28-POS,LOW PRO,.6SPACNG ICO-628-NGT,SAMTEC	889161	2
SOCKET,U19	SOCKET,PLCC,68-POS,SQUARE QILE68P-410T,BURNDY	888847	1
SW1	SW,DIP,PIANO,4POS,SEALED,0.48" 76PSB04S,GRAYHILL	808518	1
T1,2,JP1&2,JP13&14,JP15&16	CONN,HDR,PRSFIT,SGLROW,6POS 104426-4,AMP	811425	3
TP1-39	CONN,TEST POINT,BLK,LOOPED 5001,KEYSTONE,TP-105-01-00	811348	39
U1	IC,DSP,24BIT,40MHZ DSP56002FC40 MOTOROLA &	810607	1
U10	IC,TTL,INVERTER,HEX 04,SN74ALS04N &	886134	1
U11,12,46,52	IC,CMOS,TRANSCVR,OCTAL,3STATE 245,SN74HCT245N/AN &	889157	4
U13	IC,TTL,CNTR,BINARY,UP,SYNCHRON 161,SN74ALS161BN,TI	888848	1
U14,15,35,49	IC,DAC,16-BIT,VOLT.OUT,DIP 28P 7846,AD7846KN,AD &	888822	4
U16	IC,TTL,INVERTER,HEX,1-INPUT 05,SN74ALS05N	888775	1
U17	IC,TTL,DECODER,3TO8LINE,ADVNCD 138,SN74ALS138N,TI	886107	1

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
U18,23,27,33	IC,TTL,BUFFER,OCTAL,3STATE 244,SN74ALS244N,TI	886109	4
U19	IC,MICROCOMPUTER,CPU,68000 68000,MC68000FN10,MOT NC/NR	888791	1
U2	IC,PROGRAMMED REV.B,BLANK=888783	889023-1	1
U20,22	IC,TTL,TRANSCVR,OCTAL,3STATE 245,SN74ALS245N,TI	886110	2
U21	IC,CMOS,FLIP-FLOP,D,DUAL,POS 74,74HCT74N,NAT	889158	1
U24	IC,OPAMP,SR25V/us,GBW8M,Vos.2m 16,OP16EZ,PMI/AD ONLY	886495	1
U25,31,43,44,47,48,60,61,69,70,83	IC,SW,2-SPDT,Ron50,+-15V,14DIP 303,DG303ACJ,SILICONIX	888824	11
U26	IC,PROGRAMMED REV.B,BLANK=810692,TIBPAL22V10	889026	1
U28,50,56,58,59,67,68,72,73	IC,OPAMP,DUAL,SR3V/us,Vos.5mV 5102,HA3-5102-5,HAR	889008	9
U29,34,41,42,64	IC,OPAMP,SR2.8V/usGBW8M,Vos10u 27,OP-27GZ,PMI &	886028	5
U3	IC,PROGRAMMED REV.B,BLANK=888783	889023-2	1
U30,36	IC,DAC,14-BIT,uP COMPAT,DIP24P 7538,AD7538JN,AD &	888821	2
U32,74	IC,COMP,DUAL,BI-POLAR,PLAS-DIP 393,LM393N,MOT	884448	2
U37	IC,OPAMP,SR100V/us,GBW16MHz 845,AD845KN,AD &	810129	1
U38,45,51	IC,OPAMP,LO-PWR,SR13V/us,GBW3M 084,TL084ACN,TI ONLY	808735	3
U39	IC, PAL,20L10,PROG REV.B,BLANK=810692	889027	1
U4	IC,PROGRAMMED REV.B,BLANK=888783	889023-3	1

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
U40	IC,EEPROM,8KX8,28PINDIP,CMOS 28,AT28C64-25PC,ATMEL OR =	889272	1
U5	IC,CMOS,NAND GATE,QUAD,2-INPUT 00,SN74HCT00N,TI	810384	1
U53	IC,MICROPROC,6800,TIMER,PROGRM 40,MC68A4OP,MC68B40P,MOT OR =	889160	1
U54	IC,CLOCK,VCO WAVE GENENRATOR 8038,ICL8038CCJD,HAR ONLY	886172	1
U55,57	IC,OPAMP,DUAL,VERY LOW NOISE 270,OP270FZ,PMI	888820	2
U6	IC,CMOS,FLIP-FLOP,D,HEX,QUAD 175,SN74HCT175N,	889156	1
U62	IC,CMOS,BUFFER,OCTAL,TRI-STATE 244,SN74HCT244N,orSN74HCT244E	886192	1
U65,66	IC,OPAMP,HI-PWR,SR10V/us,TO-3 541,OPA541AM,BB &	888823	2
U7	IC,PROGRAMMED REV.A,BLANK=888996	889025	1
U71,78	IC,TTL,FLIP-FLOP,D,OCTAL,3STAT 574,SN74ALS574BN	888779	2
U75,80	IC,INTERFACE,DRIVER,7-CHANNEL 1413,MC1413P,new # MCT1413P	808900	2
U77	IC,COMP,DUAL,HI-SPEED 319,LM319N,NAT	883244	1
U79,81	IC,RAM,8Kx8,20 OR 25ns,28PIN 7164,IDT7164S25TP(20TP),IDT	888797	2
U8	IC,TTL,ENCODER,8-3LINE,OCTAL 148,SN74LS148N	883508	1
U9	IC,PROGRAMMED REV.A,BLANK=888855	889024	1
Y1	OSC,20Mhz,CMOS,4P DIP 8 PIN PK 531P-20MHZ,EPSON,SE1212,DIGIKY	810046	1
Z1,2,4	RES,NET,BUS,SIP,3.30KX9,10P 4310R-101-332 &	886057	3

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
Z10,16,17,31	RES,NET,10K PAIR,.005% REV.B	888811	5
Z11	RES,NET,BUS,SIP,3.90KX5,6P,2% BOURNS,100PPM &	4306R-101-392	1
Z18	RES,NET,ISO,SIP,10KX4,8P,1W 4608X-102-103,BOURNS &	889166	1
Z19	RES,NET,ISO,SIP,100KX3,6P,.75W L06-3C104 BKMN/4306R-102-104 &	887978	1
Z21,22	RES,NET,ISO,SIP,100KX4,8P,1W 4308R-102-104,BOURNS &	808628	2
Z23,34	RES,NET,ISO,SIP,3.30KX4,8P,1W 4608X-102-332,BOURNS &	889167	2
Z24	RES,NET,ISO,SIP,10KX3,6P,0.75W 4606-102-103,BOURNS	889168	1
Z25,27	RES,NET,10K,20K,.005% REV.B	888809	2
Z26	RES,NET,ISO,SIP,18KX4,8P,1W 4308R-102-183,BOURNS	889010	1
Z3	RES,NET,2K,2K,.01%,1PPM REV.A	811374	1
Z30	RES,NET,10K,20K,11.1547K REV.B	888810	1
Z5	RES,NET,3-5K,2-100K,.01%RATIO REV.B	888805	1
Z7,13,29,32	RES,NET,4.4444K,100K,0.005% REV.B	810080	4
Z8,12	RES,NET,1K,6.5K,2.46154K REV.B	888806	2
Z9,14,15,20	RES,NET,10K PAIR,PRECISION REV.B	808859	4

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPRVD
	A	RELEASE FOR MANUFACTURE		

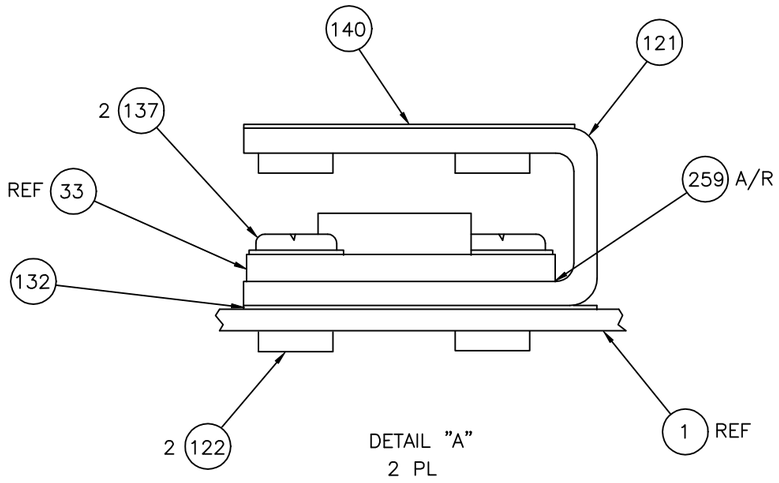


DETAIL "B"
SCALE: NONE

TABLE 1		
REF DES.	784048–2 47HZ – 400HZ	784048–1 400HZ – 10KHZ
C42, C49	0.0068uf	4700pf
C40, C48	0.033uf	3900pf
C41, C122	0.0082uf	3900pf
R38, R44	200k, 1%	20k, 1%
R5, R15	20K, 1%	8.25K, 1%

NOTES:

1. MARK DASH NO. AND REVISION LETTER OF P/L NEARSIDE, APPROX. WHERE SHOWN, WITH .12 HIGH VERTICAL GOTHIC CHARACTERS, IN WHITE EPOXY INK. SEE P/L FOR DASH & REV LETTER.
2. PRIOR TO SOLDERING ALL SHIELDS AND PARTITIONS TO BOARD, TWIST BOTTOM TABS AT APPROX. 30 DEGREES, AS SHOWN IN DETAIL "B". BE SURE TAB DOES NOT SHORT TO ANY OTHER PADS OR LANDS.
3. SEE TABLE 1 FOR ASSEMBLY VARIATIONS.
4. ASSEMBLE AND SOLDER PC BOARD IAW IPC–A–610, CLASS 2.
5. ASSEMBLY PICTURE FOR REF. ONLY. SEE P/L FOR ACTUAL BOARD POPULATION.
6. THREE 6 PIN HEADERS (ITEM #98) ARE REQUIRED PER UNIT. INSERT 2 OF THESE HEADERS AS IS, INTO T1 & T2 POSITIONS. THE THIRD 6 PIN HEADER IS TO BE BROKEN UP INTO (3) TWO PIN HEADERS AND INSERTED INTO HOLES FOR JP1 & JP2, JP13 & JP14 AND JP15 & JP16.



DETAIL "A"
2 PL

COMPUTER GENERATED DOCUMENT
NO MANUAL CHANGES PERMITTED

2	A
1	A
SHEET	REVISION
STATUS OF SHEETS	

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
FRACTIONS ± 1/64
ANGLES ± 1/2 °
DEC. .XX ± 0.02
DEC. .XXX ± 0.005

MATERIAL: SEE SEP P/L 784048–*
FINISH:

CONTRACT NO.
DRAWN: M. BARTNICKI — DATE 11/03/98
CHECKED:
APPD

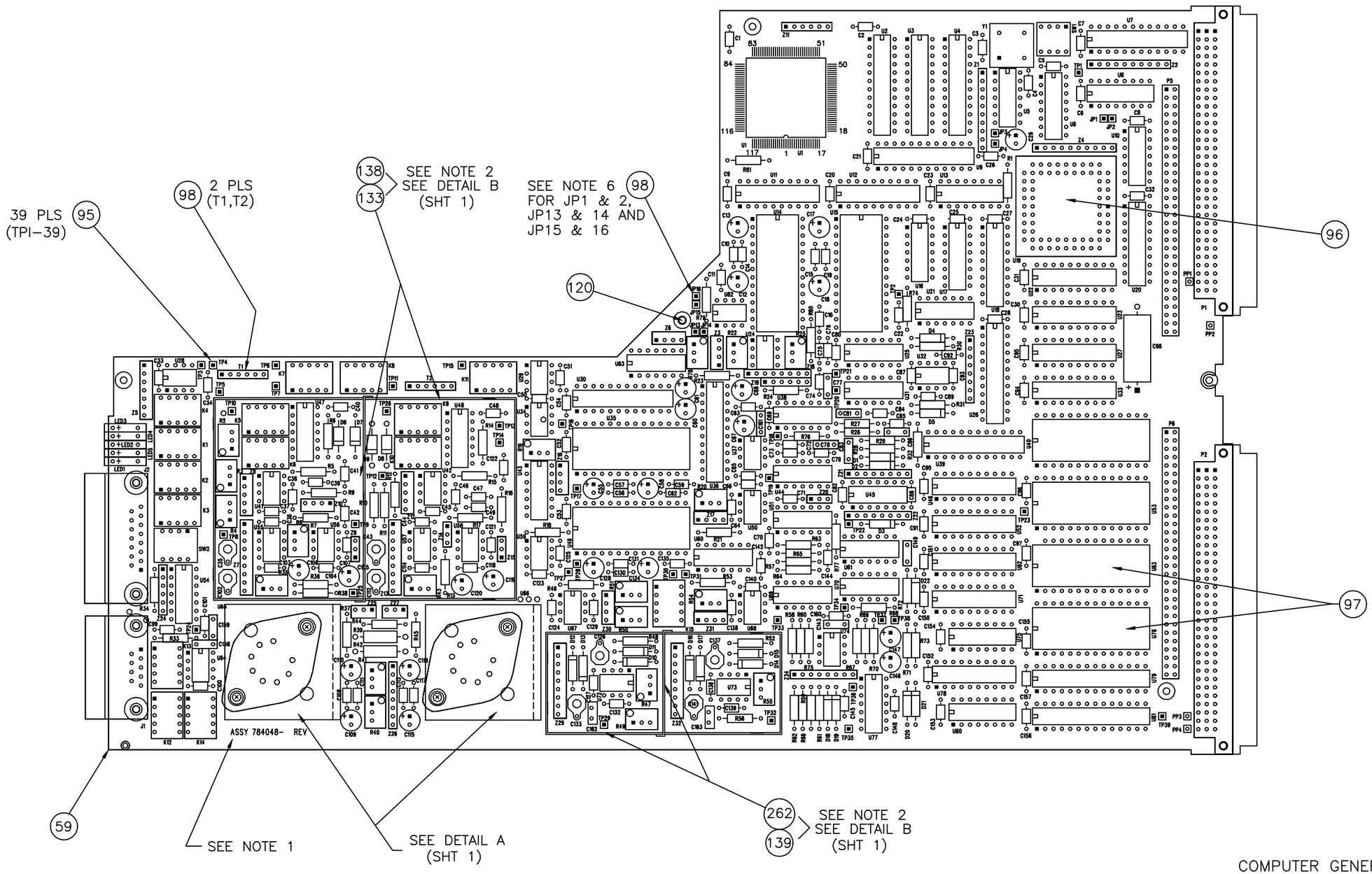
north atlantic instruments, inc.
170 Wilbur Place. Bohemia, New York 11716–2416

PRINTED WIRING ASSEMBLY
D/S – S/D

SIZE	CODE ID NO.		
D	ØVGU1	784048	A REV

SCALE NONE — SHEET 1 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPRVD



COMPUTER GENERATED DOCUMENT
NO MANUAL CHANGES PERMITTED

SIZE	CODE ID NO.		
D	ØVGUI	784048	A
			REV
SCALE NONE		SHEET 2 OF 2	

The following inserted pages contain Parts Lists and Parts Location Diagrams as shown below:

Table 7-5. Daughter Circuit Card Assembly Parts List 789104-0001

Figure 7-3. Daughter Circuit Card Assembly Parts Location Diagram 789104

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
C1-14	CAP,CER,.1UF,50V,20%,Z5U,AXIAL SA105E104MAA,AVX ^	885498	14
C15	CAP,AL-EL,33UF,16VDC,+-20% 500D336M016BA2,SPRAG,D/K P5425	889147	1
CR1	LED,RED,4 ELEM ARRAY 555-4007,DIALIGHT	885422	1
P5,6	CONN,HDR,30-POS,SKT,100CTR2ROW SSW-130-01-T-D,SAMTEC,SLDRTAIL	888898	2
R1	RES,CMPSN,180 OHM,5%,1/4W RCR07G181JS,RLR07C1800GS ^	880364	1
R2	RES,MF,825 OHM,1%,1/8W,100PPM RN55D8250F	885173	1
SW1	SW,DIP,PIANO,8POS,SPST,100x300 435802-1,AMP	883606	1
U1,2	IC,TTL,TRANSCVR,OCTAL,3STATE 645,SN74ALS645A-1N,TI OR EQUAL	888780	2
U12	IC,TTL,TANSCVR,OCTAL,O.C,2ENBL 621,SN74F621N	888784	1
U13	IC,CMOS,INVERTER,HEX 04,SN74HCT04N,	889017	1
U16	IC,CMOS,FLIP-FLOP,OCTAL D,RSET 273,SN74HCT273N,	889012	1
U17	IC,TTL,FLIP-FLOP,D,DUAL,CLR/PR 74,SN74ALS74AN,TI	886105	1
U18	IC,TTL,CNTR,BINARY,UP,SYNCHRON 161,SN74ALS161BN,TI	888848	1
U19,31	IC,CMOS,TRANSCVRS & REG,OCTAL 652,SN74HCT652NT, &	889016	2
U20	IC,PROGRAMMED REV.B,BLANK=888996	889001-0001	1
U21	IC,PROGRAMMED REV.B BLANK=810692 &	889000-0001	1
U22	IC,PROGRAMMED REV.B,BLANK=888794	889002	1

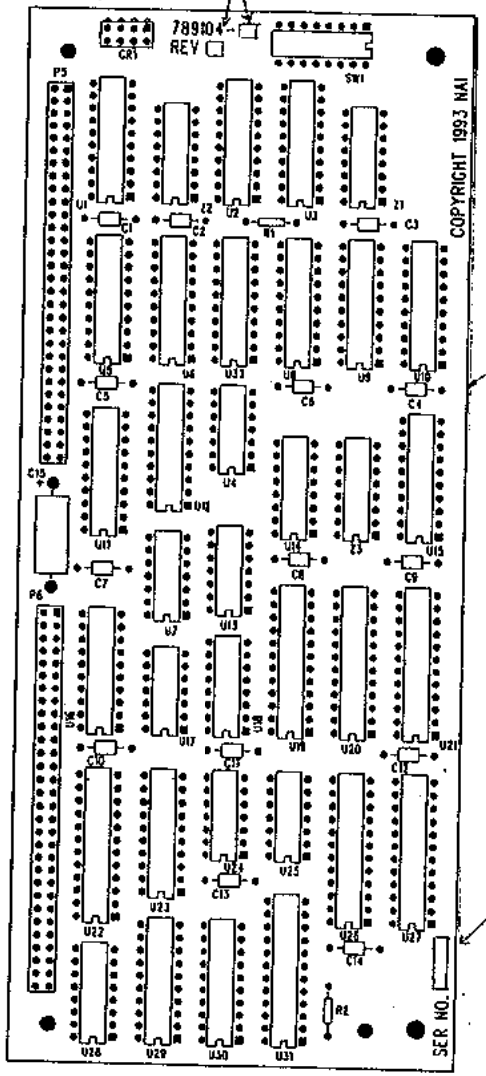
PW ASSY,VXI,D/S-S/D IAC
REV: G

REFERENCE DESIGNATORS	DESCRIPTION / VENDOR PART NO.	NAI PART NO.	QTY
U24	IC,TTL,INVERTER,HEX 04,SN74ALS04N &	886134	1
U25	IC,CMOS,SHIFT REG,SERIAL,8BIT 164,74HCT164,SN74HCT164N,TI	889013	1
U26	IC, PAL,22P10,EVEN REV.B,BLANK=810692 &	889004	1
U27	IC,PROGRAMMED REV.C,BLANK=810692 &	889003	1
U28	IC,CMOS,COMP,4-BIT,MAGNITUDE 85,SN74HCT85N,TI	889015	1
U3	IC,CMOS,COMP,8BIT,MAG/IDENTITY 688,SN74HCT688N,TI	889014	1
U32	IC,TTL,LATCH,OCTAL,TRANSPARENT 373,SN74ALS373AN,TI OR =	810110	1
U4	IC,CMOS,AND GATE,QUAD,2-INPUT 08,SN74HCT08N,	886198	1
U5,10	IC,TTL,BUFFER,OCTAL,3STATE 244,SN74ALS244N,TI	886109	2
U6,8,11,15,23,29,30	IC,CMOS,FLIP-FLOP,D,OCTAL,EDGE 574,SN74HCT574N,SN74HCT574E,TI	889011	7
U7	IC,TTL,NAND GATE,QUAD,2-INPUT 38,SN74S38N,TI &	888785	1
U9	IC,PROGRAMMED REV.A,BLANK=888692	888999	1
Z1,2,3	RES,NET,BUS,DIP,3.30KX15,16P 4116R-002-332 BOURNS &	885964	3
u14	IC,CMOS,DECODER/DMUX,3TO8 LINE 138,SN74HCT138N,	886189	1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	[illegible]	11-3-92	
	B	ECN 29792, NO CHANGE	3-4-93	MS
	C	ECN 30042, NO CHANGE	5-21-93	MD
	D	ECN 30107 NO CHANGE	5-20-94	BM
	E	ECN [illegible]	1-11-95	
	F	ECN 33099, NO CHANGE	1-3-96	RVP
	G	ECN 34659, NO CHANGE	11-1-96	

SEE NOTE 2

SEE NOTE 1



SEE NOTE 1

NOTES:
1. MARK SERIAL NO., DASH NO. AND REVISION LETTER NEARSIDE APPROX WHERE SHOWN WITH .12 HIGH VERTICAL GOTHIC CHARACTERS IN WHITE EPOXY INK PER MIL-STD-130. SEE CONFIGURATION DOCUMENT CD-789104- FOR REVISION LETTER.
2. MAXIMUM SOLDER PIN LENGTH TO BE .060 AFTER WAVE SOLDERING.

DASH #	PRODUCT	REF DES	ITEM	PAL PART NO
-1	405088	U26	22	888904
	D/S-3/D	U27	29	888903
-2	402227	U26	22	888998
	PAV	U27	29	888997

SEE SEPARATE PARTS LIST

		402227	402227
		405088	405088
SHEET	REVISION	NEXT ASSY	USED ON
STATUS OF SHEETS		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± 1/64 ANGLES ± 1/2°
DECIMALS .XX ± .02 .XXX ± .005
MATERIAL
FINISH

CONTRACT NO.
DRAWN LJ E 10/19/94
CHECKED P Thump 10/19/94
ROP 10/19/94
APPD 10/19/94

north atlantic
PRINTED WIRING ASSY.
IAC VXI BOARD

SIZE	CODE IDENT NO.		REV
D	07342	789104-	G

SCALE 2:1 SHEET 1 OF 1

SECTION 8

SCHEMATIC DIAGRAMS

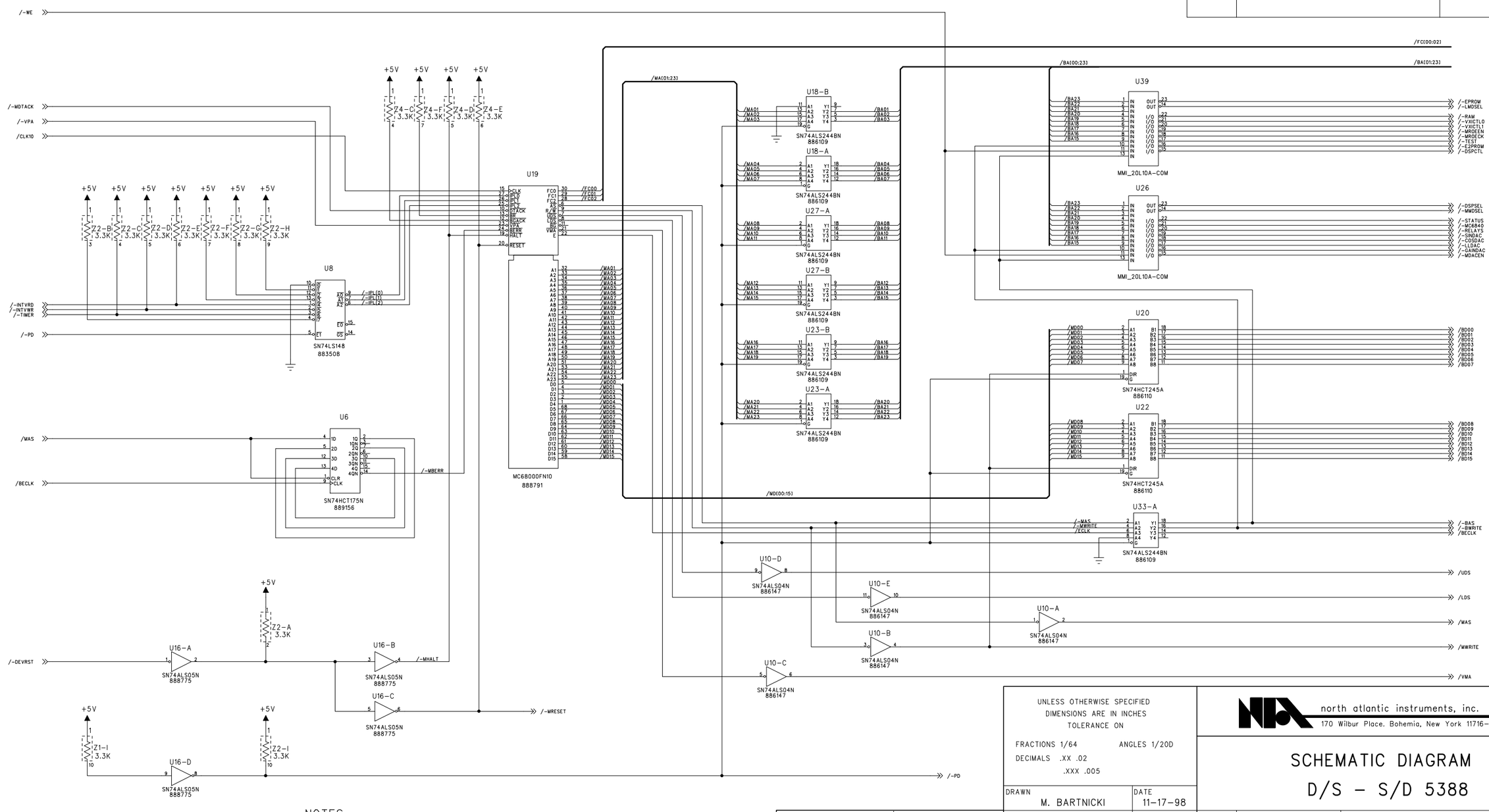
8-1 INTRODUCTION

This section contains schematic diagrams for the Model 5388.

The following inserted pages contain schematic diagrams as follows:

Mother Circuit Card Assembly	Schematic	770035

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE
A	RELEASE FOR MANUFACTURE		



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%. CAPACITANCE VALUES ARE IN MICROFARADS.

784048	5388
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON
FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

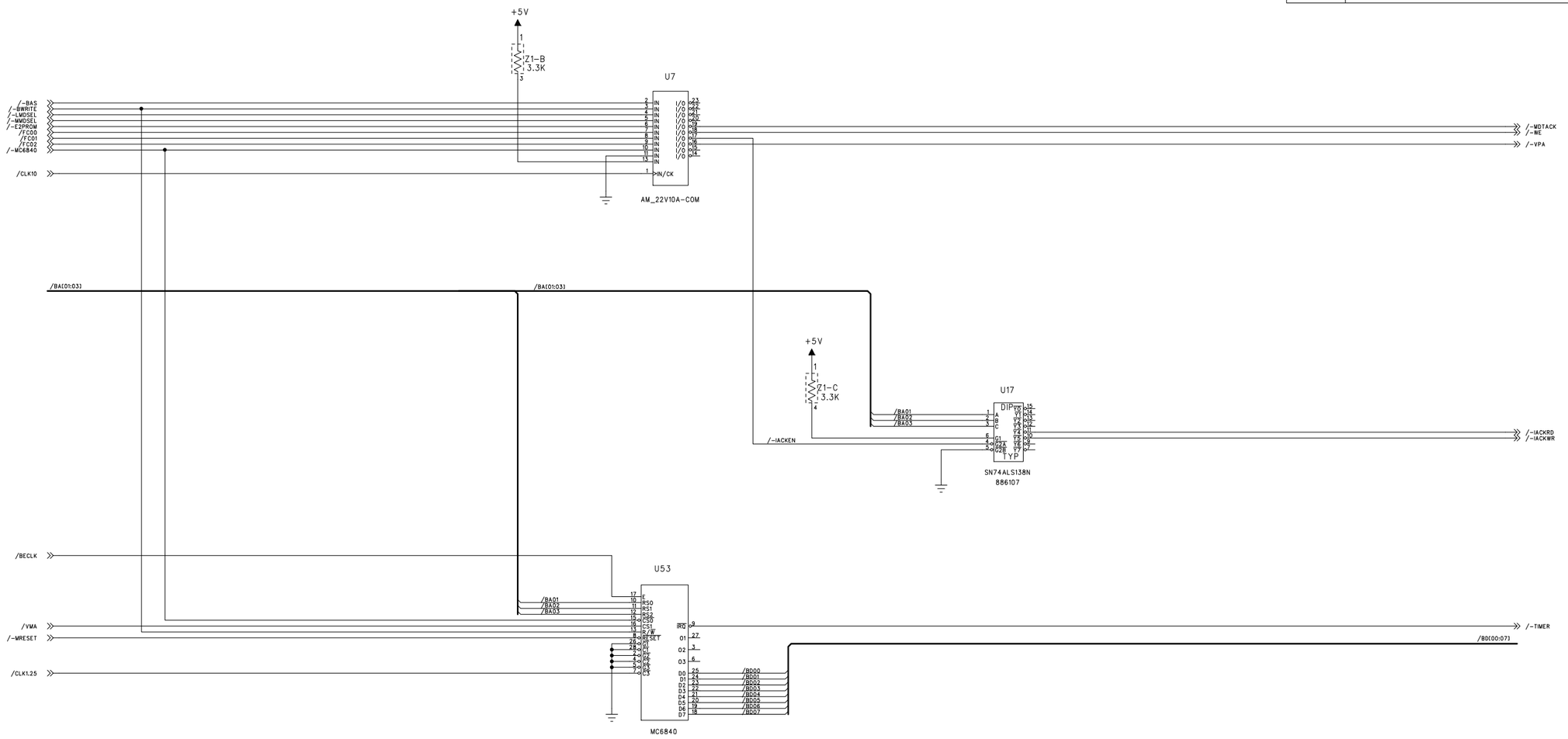
DRAWN	M. BARTNICKI	DATE 11-17-98
CHECKED		
APPROVED		

north atlantic instruments, inc.
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SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 1 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON

FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

DRAWN	DATE
CHECKED	
APPROVED	

NEXT ASSY	USED ON
APPLICATION	

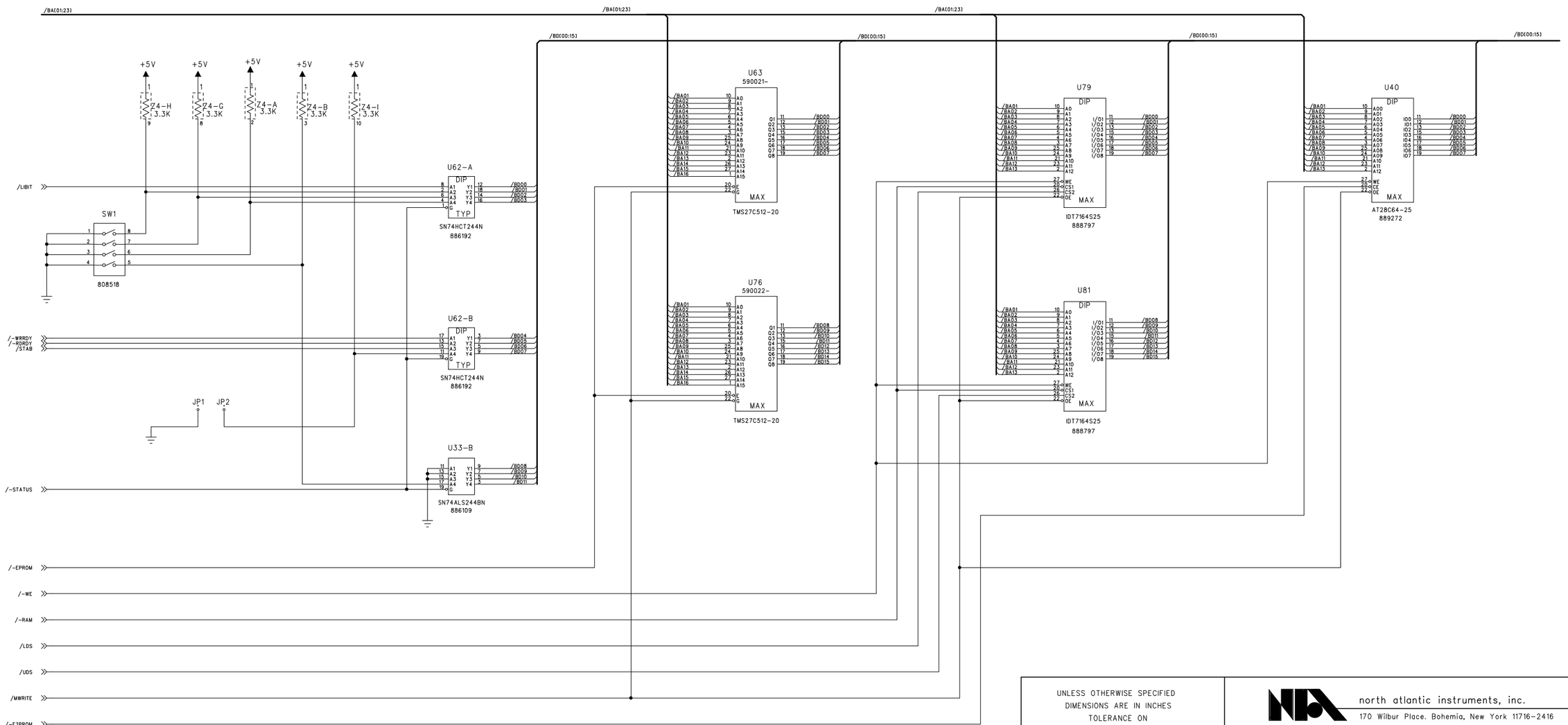
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SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A

SCALE: NONE SHEET 2 OF 14

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON
FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

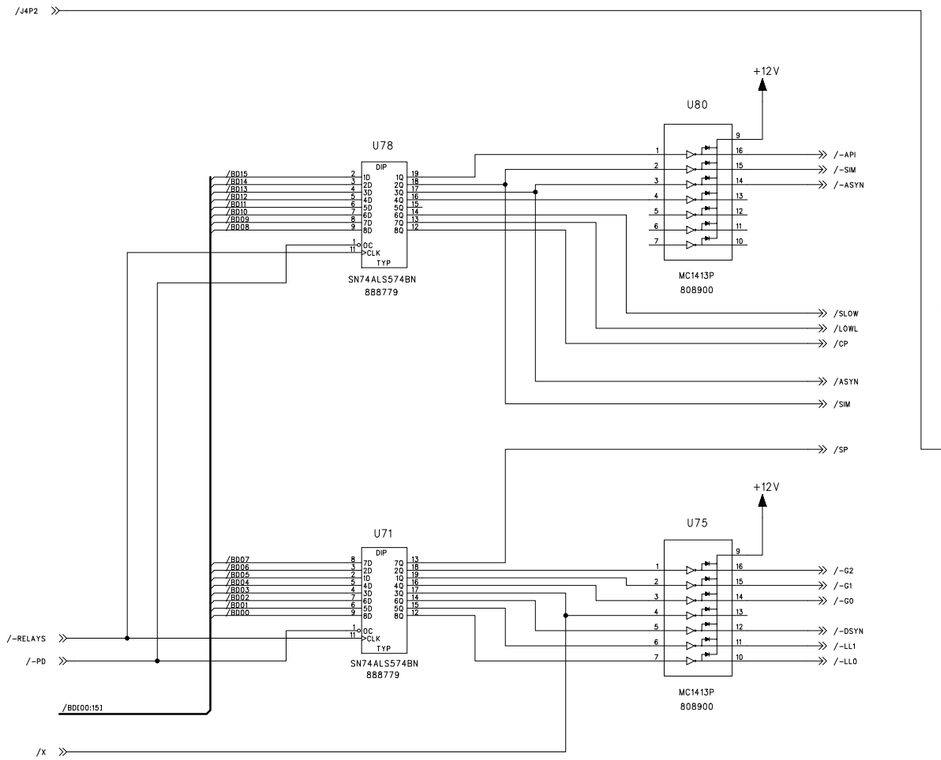
		DRAWN	DATE
		CHECKED	
NEXT ASSY	USED ON	APPROVED	
APPLICATION			

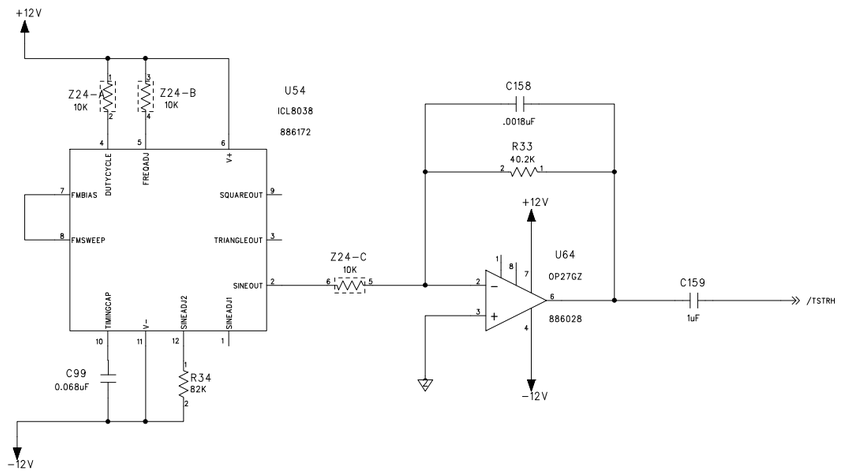
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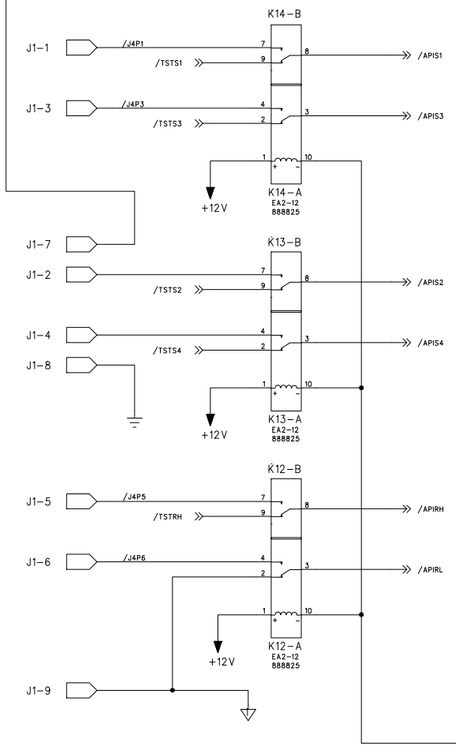
SCHEMATIC DIAGRAM
D/S - S/D 5388

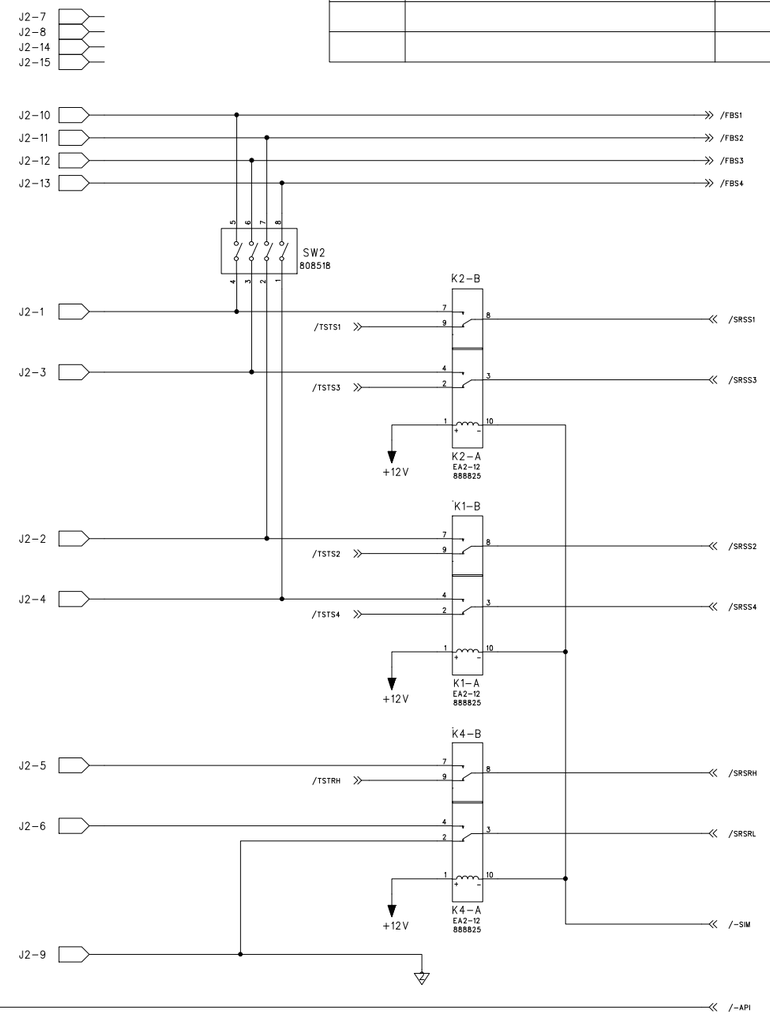
SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 3 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE









UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON

FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

DRAWN	DATE
CHECKED	
APPROVED	

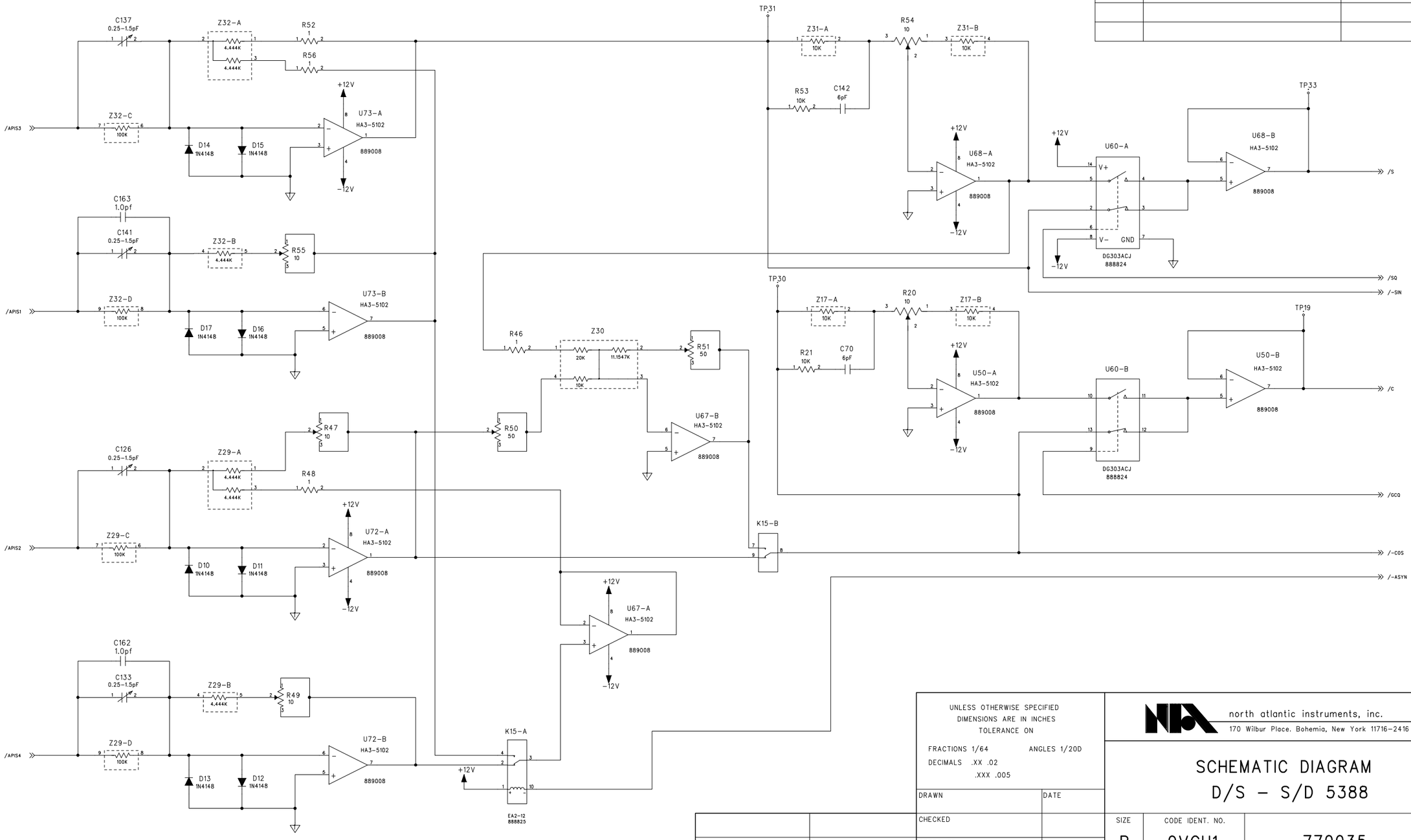
NEXT ASSY	USED ON
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SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 4 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON
FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

DRAWN	DATE
CHECKED	
APPROVED	

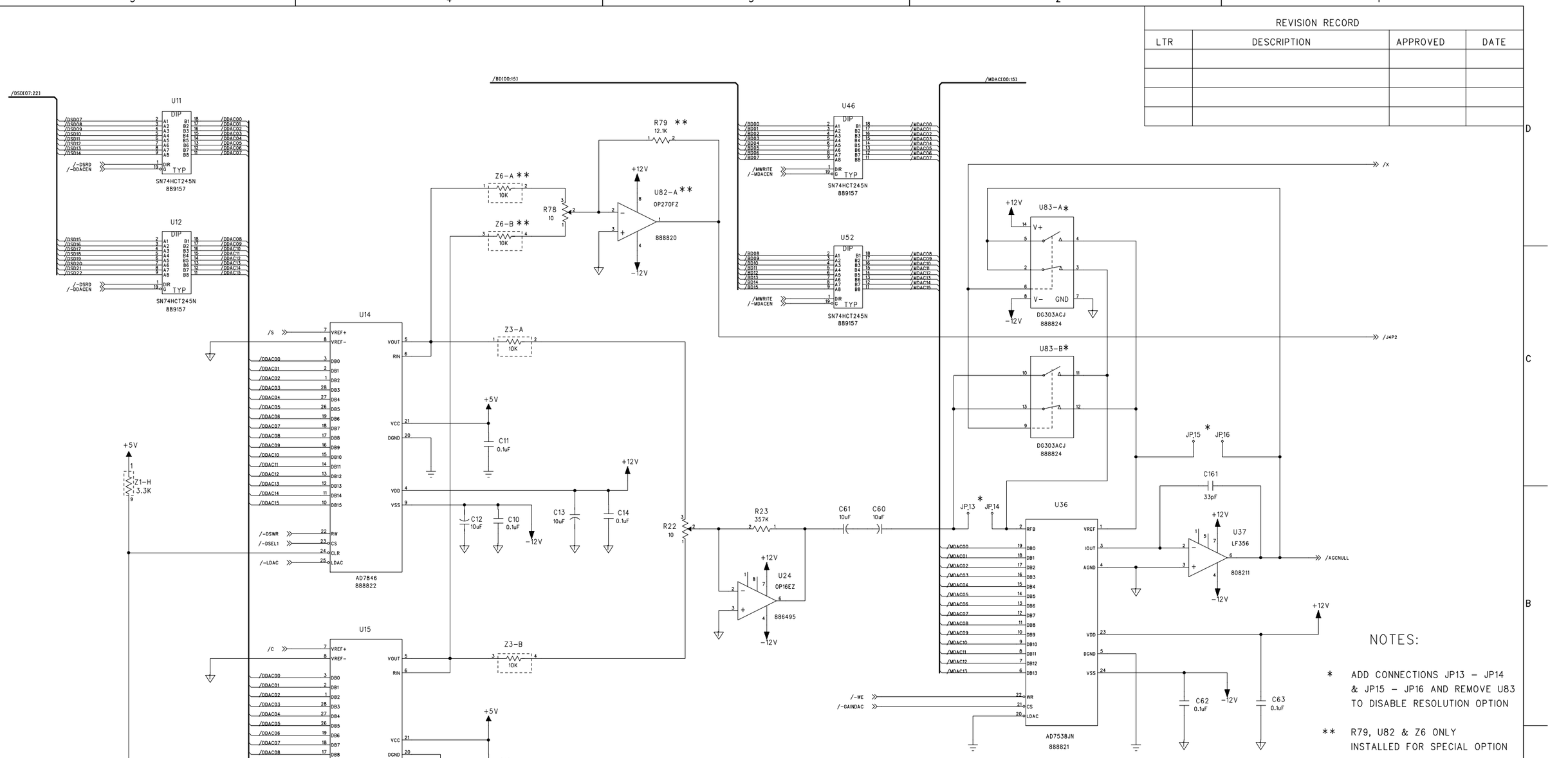
NEXT ASSY	USED ON
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170 Wilbur Place. Bohemia, New York 11716-2416

SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 5 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE



NOTES:

* ADD CONNECTIONS JP13 – JP14 & JP15 – JP16 AND REMOVE U83 TO DISABLE RESOLUTION OPTION

** R79, U82 & Z6 ONLY INSTALLED FOR SPECIAL OPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON
FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

DRAWN	DATE
CHECKED	
APPROVED	

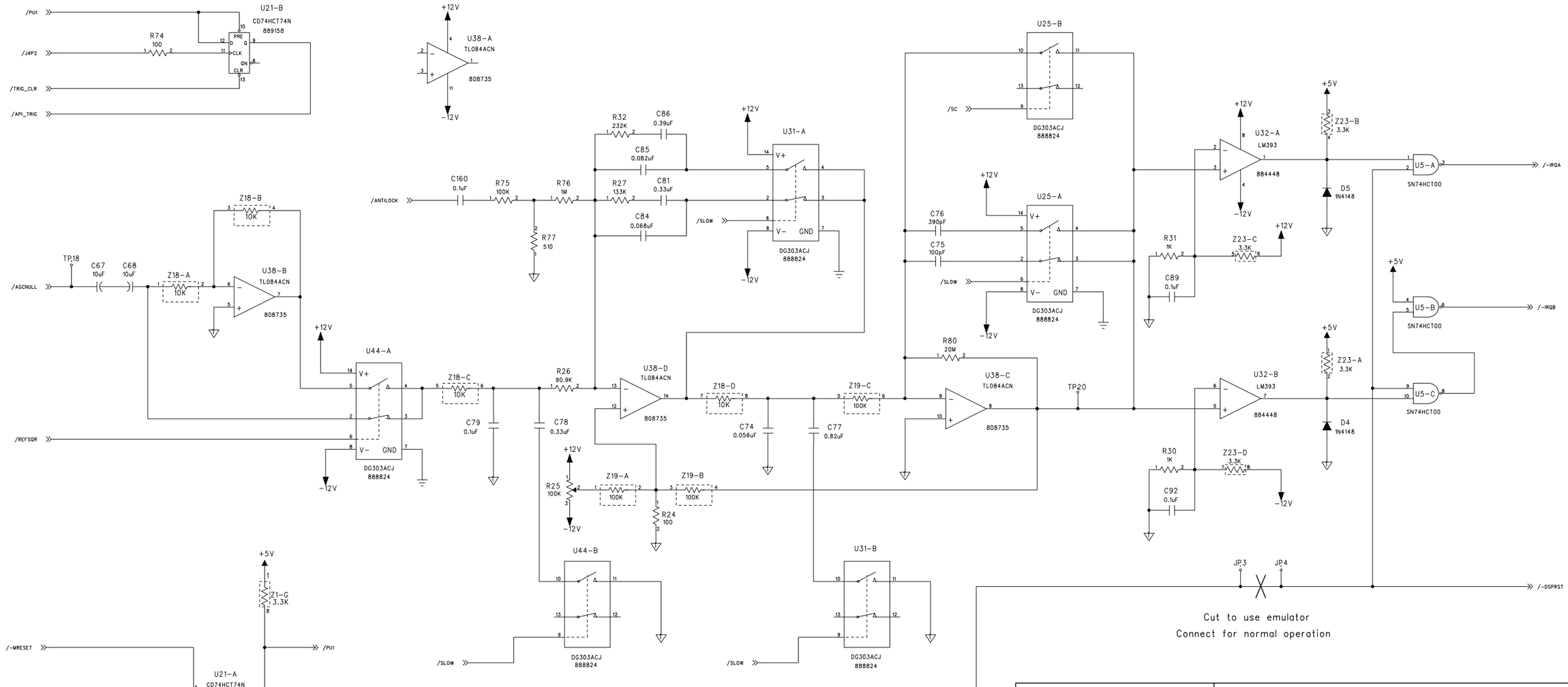
NEXT ASSY	USED ON
APPLICATION	

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SCHEMATIC DIAGRAM
D/S – S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 6 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON	
FRACTIONS 1/64 ANGLES 1/20D	
DECIMALS .XX .02 .XXX .005	
DRAWN	DATE
CHECKED	
APPROVED	

NEXT ASSY	USED ON
APPLICATION	

north atlantic instruments, inc.
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SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 7 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE

U69-B
R63 1K
R64 9.09K
U51-A TL084ACN
808735
DG303ACJ 888824
/LOWL
/-SIN
+12V
-12V
R28 200K
R29 200K
C83 1uF
Z22-D 100K
Z22-C 100K
Z22-B 100K
Z22-A 100K
D2 1N4148
D1 1N4148
U45-A TL084ACN
U45-B TL084ACN
R60 1K
U74-A LM393
884448
Z34-A 3.3K
R58 1M
U61-B
DG303ACJ 888824
R72 200K
R68 200K
C149 1uF
Z21-D 100K
Z21-C 100K
Z21-B 100K
Z21-A 100K
D22 1N4148
D3 1N4148
U45-C TL084ACN
U45-D TL084ACN
U69-A
R65 1K
R57 9.09K
U51-B TL084ACN
/-COS
U61-A
R67 10K
C143 1uF
U74-B LM393
R69 1K
R70 1M
Z34-B 3.3K
/ANTILOCK
U70-A
Z20 10K 10K
U51-C TL084ACN
U70-B
R73 10K
C146 10uF
C147 10uF
R71 3.32K
D21 1N4148
D20 1N4148
U77-B LM319N
883244
TP37
TP35
/REFSQR
TP34
TP36
R59 100K
R66 100K
/APIRL
/APIRH
U77-A LM319N
D18 1N4148
D19 1N4148
Z34-D 3.3K
R61 10K
R62 10K
Z34-C 3.3K

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON
FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

DRAWN	DATE
CHECKED	
APPROVED	

NEXT ASSY	USED ON
APPLICATION	

north atlantic instruments, inc.
170 Wilbur Place. Bohemia, New York 11716-2416

SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 8 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE

+5V
Z1-A 3.3K
Y1
20MHz
OSCILLATOR
U5-D
SN74HCT00
/CLK20
+5V
Z1-F 3.3K
+5V
Z1-E 3.3K
/-IRQA
/-IRQB
/-DSPRST
U1
DSP56002FC40
810607
/-DSRD
/-DSWR
/BD[00:07]
/-DSDS
/DSXY
/BA[01:03]
/-BWRITE
/-DSPSEL
/SC
/SQ
/-LDAC
/STAB
/APL_TRIG
/TRIG_CLR
/DSDI[00:23]
U4
888783
U3
888783
U2
888783
/-DSRD
/DSROM
/DSD23
R1 15K
VCC PINS:
2,9,20,30,37,45,58,66,69,
79,89,97,102,113,124,127
GROUND PINS:
3,5,11,16,22,27,34,36,48,
56,62,67,70,75,81,86,92,
98,99,105,110,116,122,129
NO CONNECTION PINS:
39,40,41,42,49,50,51,52,53
54,119,123,126,128,130,131
+5V
Z11-A 3.90K
+5V
Z11-B 3.90K
+5V
Z11-C 3.90K
R81
15K
+5V
Z1-D 3.3K
U13
SN74ALS161BN
888848
/CLK10
/CLK1.25
U9
AM_22V10A-15
/-DDACEN
/DSROM
/-DSEL2
/-DSEL1
/CQ
/DSA[00:15]
/DSA[00:15]

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON
FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

DRAWN	DATE
CHECKED	
APPROVED	

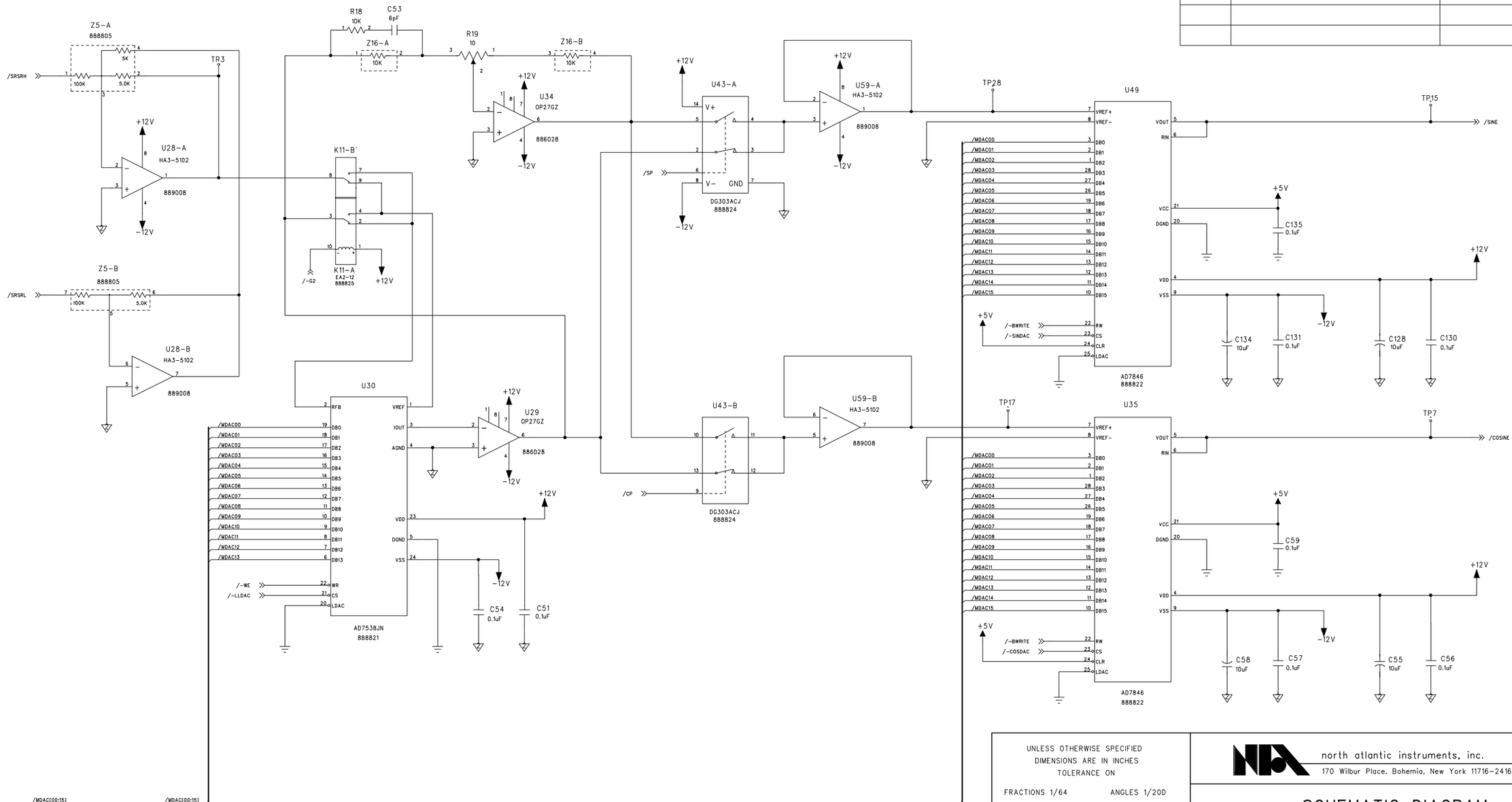
NEXT ASSY	USED ON
APPLICATION	

north atlantic instruments, inc.
170 Wilbur Place. Bohemia, New York 11716-2416

SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 9 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON

FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

DRAWN	DATE
CHECKED	
APPROVED	

NEXT ASSY	USED ON
APPLICATION	

north atlantic instruments, inc.
170 Wilbur Place. Bohemia, New York 11716-2416

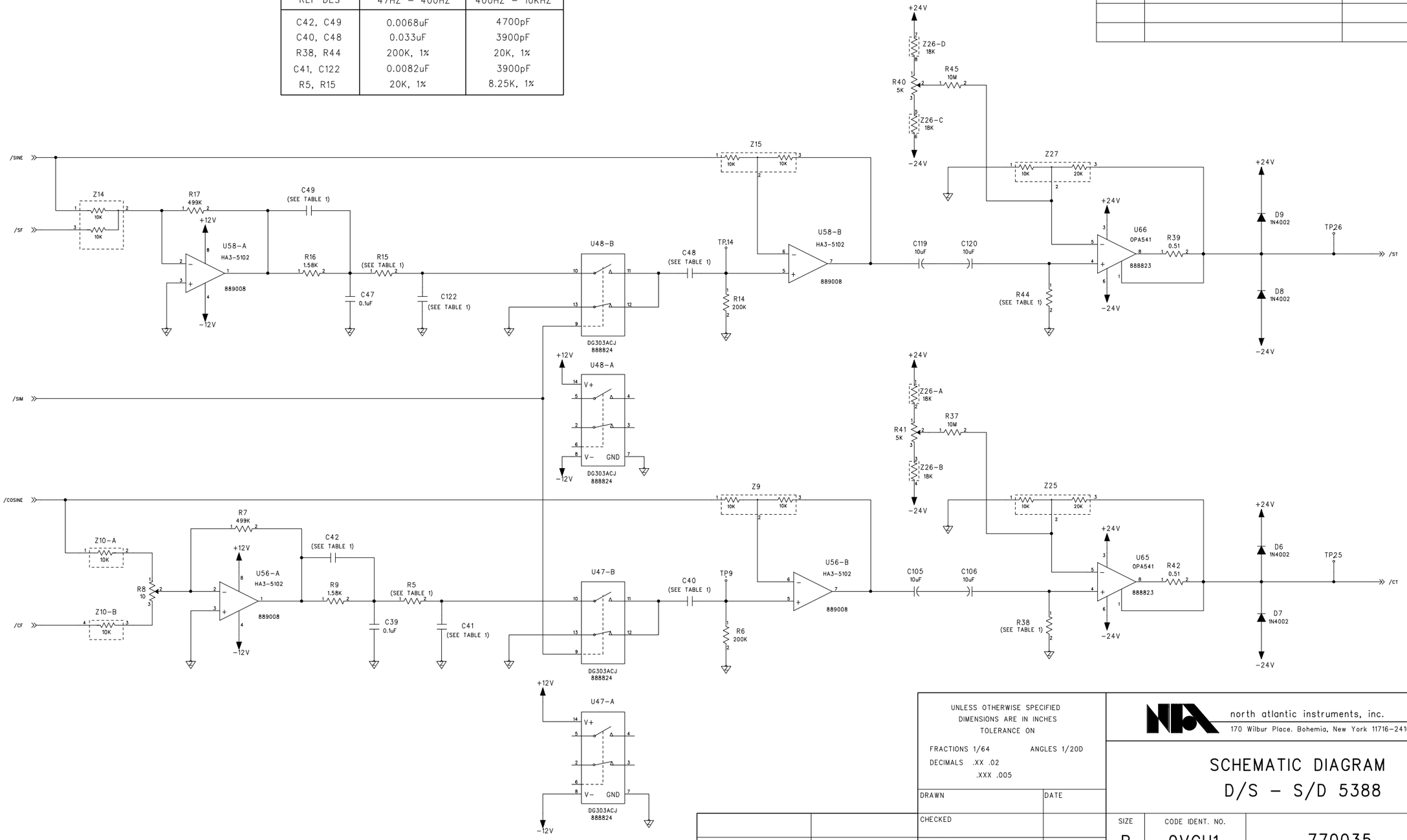
SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 10 OF 14	

TABLE 1

REF DES	789105-2 47HZ - 400HZ	789105-1 400HZ - 10KHZ
C42, C49	0.0068uF	4700pF
C40, C48	0.033uF	3900pF
R38, R44	200K, 1%	20K, 1%
C41, C122	0.0082uF	3900pF
R5, R15	20K, 1%	8.25K, 1%

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON
FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

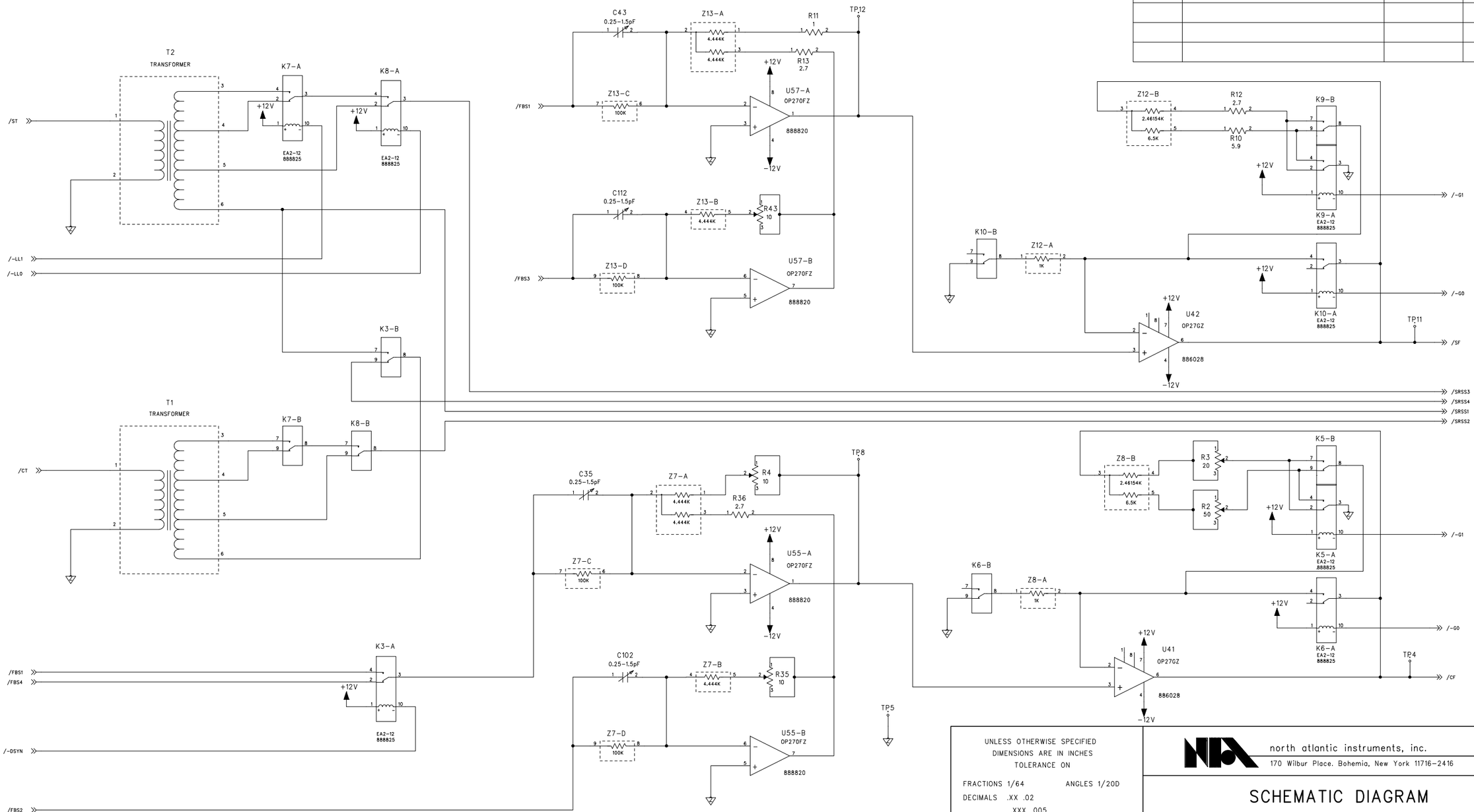
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NEXT ASSY / USED ON	APPROVED	
APPLICATION		

north atlantic instruments, inc.
170 Wilbur Place. Bohemia, New York 11716-2416

SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 11 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON
FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

DRAWN	DATE
CHECKED	
APPROVED	

NEXT ASSY	USED ON
APPLICATION	

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170 Wilbur Place. Bohemia, New York 11716-2416

SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 12 OF 14	

REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE

P1-A1 /D(0) P5-2
P1-A2 /D(1) P5-4
P1-A3 /D(2) P5-6
P1-A4 /D(3) P5-8
P1-A5 /D(4) P5-10
P1-A6 /D(5) P5-12
P1-A7 /D(6) P5-14
P1-A8 /D(7) P5-16
P1-C1 /D(8) P5-1
P1-C2 /D(9) P5-3
P1-C3 /D(10) P5-5
P1-C4 /D(11) P5-7
P1-C5 /D(12) P5-9
P1-C6 /D(13) P5-11
P1-C7 /D(14) P5-13
P1-C8 /D(15) P5-15
P1-B16 /AM(0) P5-26
P1-B17 /AM(1) P5-28
P1-B18 /AM(2) P5-29
P1-B19 /AM(3) P5-31
P1-A23 /AM(4) P5-35
P1-C14 /AM(5) P5-24
P1-C13 /-LWORD P5-22
P1-A20 /-IACK P5-32
P1-A30 /A(1) P5-58
P1-A29 /A(2) P5-54
P1-A28 /A(3) P5-51
P1-A27 /A(4) P5-48
P1-A26 /A(5) P5-45
P1-A25 /A(6) P5-42
P1-A24 /A(7) P5-39
P1-C30 /A(8) P5-55
P1-C29 /A(9) P5-52
P1-C28 /A(10) P5-49
P1-C27 /A(11) P5-46
P1-C26 /A(12) P5-43
P1-C25 /A(13) P5-40
P1-C24 /A(14) P5-37
P1-C23 /A(15) P5-36
P1-A12 /-DS1 P5-21
P1-A13 /-DS0 P5-23
P1-A14 /-WRITE P5-25
P1-A18 /-AS P5-30
P1-C12 /-SYSRESET P5-20
P1-B4
P1-B5
P1-B6
P1-B7
P1-B8
P1-B9
P1-B10
P1-B11

P5-33 /-IACKIN P1-A21
P5-18 /SYSCLK P1-A10
P5-19 /-BERR P1-C11
P5-27 /-DTACK P1-A16
P5-17 /-SYSFAIL P1-C10
P5-56 /-IRQ1 P1-B30
P5-53 /-IRQ2 P1-B29
P5-50 /-IRQ3 P1-B28
P5-47 /-IRQ4 P1-B27
P5-44 /-IRQ5 P1-B26
P5-41 /-IRQ6 P1-B25
P5-38 /-IRQ7 P1-B24
P5-34 /-IACKOUT P1-A22

P6-28 /-IACKWR
P6-27 /-IACKRD
P6-32 /-TEST
P6-35 /-INTVWR
P6-38 /-INTVRD
P6-12 /LIBIT
P6-29 /-MROEEN
P6-30 /-MROECK
P6-39 /BD00
P6-7 /BD01
P6-8 /BD02
P6-9 /BD03
P6-10 /BD04
P6-42 /BD05
P6-13 /BD06
P6-14 /BD07
P6-19 /BD08
P6-20 /BD09
P6-17 /BD10
P6-18 /BD11
P6-15 /BD12
P6-21 /BD13
P6-24 /BD14
P6-23 /BD15
P6-33 /-WRRDY
P6-34 /-RDRDY
P6-22 /-VXICTL0
P6-25 /-DEVRST
P6-46 /-LEDFAIL
P6-26 /-LEDSFI
P6-37 /-LEDRST
P6-36 /-LEDMODID
P6-11 /-VXICTL1
P6-57 /MODID P2-A30

P2-A4
P2-A10
P2-A16
P2-A28
P2-A31
P2-B2
P2-B12
P2-B31
P2-C3
P2-C7
P2-C10
P2-C16
P2-C25
P2-C28
P2-C30

P1-A19
P1-B20
P1-B23
P1-C9

P6-2
P6-4
P6-6

P1-A9
P1-A11
P1-A15
P1-A17

P2-A22
P2-B22
P2-C22

+5V
P6-1
P6-3
P6-5
P1-A32
P1-B32
P1-C32
P2-A25
P2-B1
P2-B13
P2-B32

+12V
P1-C31
P1-A31
-12V

+24V
P2-C31
P2-C32
-24V

+5V
LED4 /-LEDFAIL
LED2 /-LEDMODID
LED5 /-LEDSFI
LED1 /-LEDRST
LED3

P1-B1
P1-B2
P1-B3
P1-B12
P1-B13
P1-B14
P1-B15
P1-B21
P1-B22
P1-B31
P1-C15
P1-C16
P1-C17
P1-C18
P1-C19
P1-C21
P1-C20
P1-C22
P1-M1
P1-M2

P5-57
P5-59
P5-60

P6-16
P6-31
P6-40
P6-41
P6-43
P6-44
P6-45
P6-47
P6-48
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P6-51
P6-52
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P6-54
P6-55
P6-56
P6-58
P6-59
P6-60

P2-A1
P2-A2
P2-A3
P2-A5
P2-A6
P2-A7
P2-A8
P2-A9
P2-A11
P2-A12
P2-A13
P2-A14
P2-A15
P2-A17
P2-A18
P2-A19
P2-A20
P2-A21
P2-A23
P2-A24
P2-A26
P2-A27
P2-A29
P2-A32
P2-M1
P2-M2

P2-B3
P2-B4
P2-B5
P2-B6
P2-B7
P2-B8
P2-B9
P2-B10
P2-B11
P2-B14
P2-B15
P2-B16
P2-B17
P2-B18
P2-B19
P2-B20
P2-B21
P2-B23
P2-B24
P2-B25
P2-B26
P2-B27
P2-B28
P2-B29
P2-B30

P2-C1
P2-C2
P2-C4
P2-C5
P2-C6
P2-C8
P2-C9
P2-C11
P2-C12
P2-C13
P2-C14
P2-C15
P2-C17
P2-C18
P2-C19
P2-C20
P2-C21
P2-C23
P2-C24
P2-C26
P2-C27
P2-C29

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON
FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

DRAWN	DATE
CHECKED	
APPROVED	

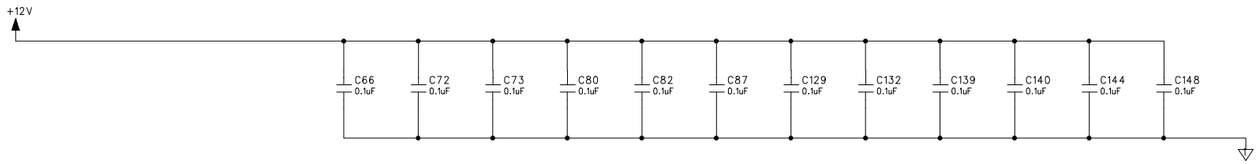
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APPLICATION	

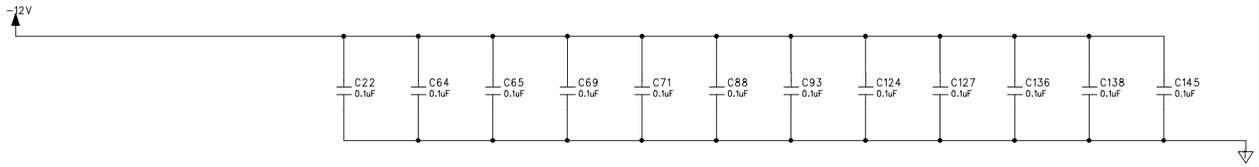
north atlantic instruments, inc.
170 Wilbur Place. Bohemia, New York 11716-2416

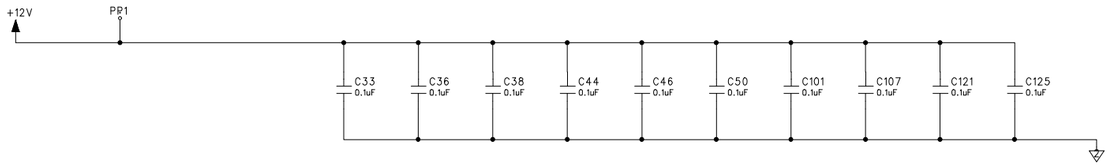
SCHEMATIC DIAGRAM
D/S – S/D 5388

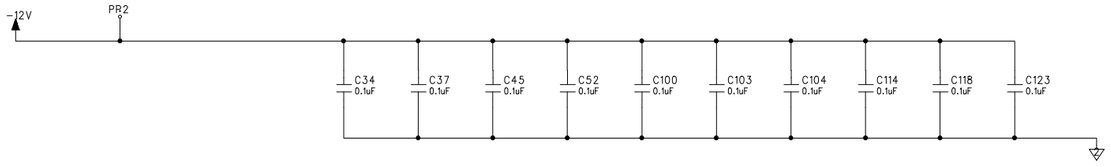
SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 13 OF 14	

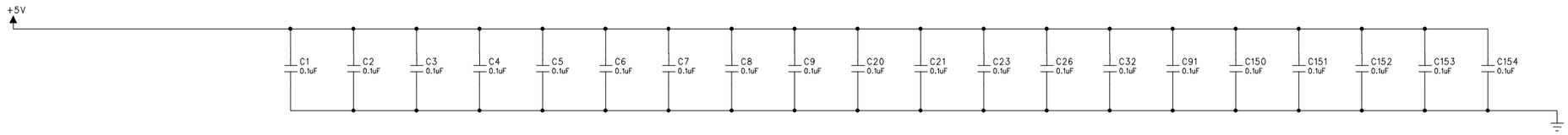
REVISION RECORD			
LTR	DESCRIPTION	APPROVED	DATE

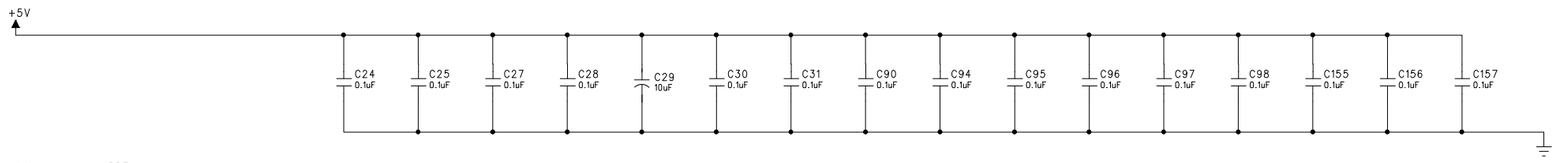


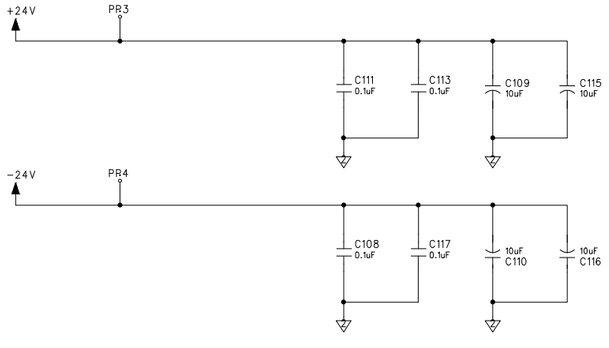


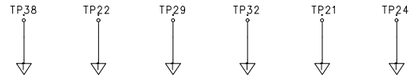


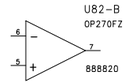












UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON

FRACTIONS 1/64 ANGLES 1/20D
DECIMALS .XX .02
.XXX .005

		DRAWN	DATE
		CHECKED	
NEXT ASSY	USED ON	APPROVED	
APPLICATION			

north atlantic instruments, inc.
170 Wilbur Place. Bohemia, New York 11716-2416

SCHEMATIC DIAGRAM
D/S - S/D 5388

SIZE	CODE IDENT. NO.		REV
B	0VGU1	770035	A
SCALE: NONE		SHEET 14 OF 14	

The following inserted pages contain schematic diagrams as follows:

Daughter Circuit Card Assembly Schematic 769104

769104f.sch-1 - Wed Jun 09 14:24:57 1999

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	F	ECN # 33099	12/10/93	DA

D[00:15]

U1 74ALS645 — -VDBEN0; P5-2 P5-4 P5-6 P5-8 P5-10 P5-12 P5-14 P5-16 (D00–D07); VD00–VD07; B1–B8 (D00–D07)

U2 74ALS645 — -VDBEN1; P5-1 P5-3 P5-5 P5-7 P5-9 P5-11 P5-13 P5-15 (D08–D15); VD08–VD15; B1–B8 (D08–D15)

-LEN, -VDTACK, -VWRITE

U32 74ALS373 — VD08–VD15 (D08–D15); 1 OE, 11 LE; Q0–Q7

U22 20RA10 — P6-29, P6-30, -IACKWR, -IACKRD, P6-28, P6-27, P6-32, -TEST; -MROEEN, -MROECK; -VROEC0, -VROEC1, -MROEEN, -VROEEN, BD00, -MROECK; BD01; IN0–IN9; REG0–REG9; 1 PL, 13 OE

-WRRDY; P6-33; -RDRDY; P6-34; P6-35; P6-38

+5V — Z1-I 3.3K (16, 9); Z1-J 3.3K (16, 10)

U13-E 74HCT04 — 11, 10; -PD1

VD[00:15]

U9 16L8 — VAM2, VAM3, VAM4, VAM5, VAM1, VAM0; IN0–IN9; OUT0, OUT1; I/00–I/05; -DEVSEL

-VAS

VAM[0:5]

U6 74HCT574 — -SAS; P5-26 P5-28 P5-29 P5-35 P5-24 P5-22 P5-32 (AM0–AM5, -LWORD, -IACK); D0–D7; Q0–Q7 (VAM0–VAM5); -VIACK

U11 74HCT574 — P5-58 P5-54 P5-51 P5-48 P5-45 P5-42 P5-39 (A1–A7); D0–D7; Q0–Q7 (VA00–VA07)

U8 74HCT574 — P5-55 P5-52 P5-49 P5-46 P5-43 P5-40 P5-37 P5-36 (A8–A15); D0–D7; Q0–Q7 (VA08–VA15)

+5V — Z1-A 3.3K (1) … Z1-H 3.3K (8)

SW1 DIPSW8 — 1–8 / 16–9

BDA0–BDA7

VA15, VA14

VA[00:15]

U3 74HCT688 — VA06 VA07 VA08 VA09 VA10 VA11 VA12 VA13 (P0–P7); P=Q; -ADRVLD; Q0–Q7; G

BDA[0:7]

NORTH ATLANTIC INSTRUMENTS INC.

SCHEMATIC DIAGRAM
IAC VXI BOARD

SIZE		SHEET	REV
B	769104	1 OF 5	F

VA[00:15]

U10-B
74ALS244
P5-33 -IACKIN
P5-23 -DS0
P5-25 -WRITE
P5-30 -AS
-VIACKIN
-VDS0
-VWRITE
-VAS

U13-B
74HCT04
VAS

U5-B
74ALS244
P5-20 -SYSRESET
P5-21 -DS1
P5-18 SYSCLK
P5-19 -BERR
-VSYSRESET
-VDS1

+5V
Z1-L 3.3K
Z1-M 3.3K
Z1-K 3.3K

U21
20L10
VA02
VA01
VA04
VA05
VA03
-VRO4C0
-VDBEN1
-VROEEN
-VRROEN
-VDBEN0
-VROEC1
-VROEC0
-LEN

U15
74HCT574
-VDS
-DEVSEL
-VIACK
-INTIRQA

U20
22V10
-IACKRST
-VWR
-VDBEN
S0
S1
S2
S3
-VRD
-SAS

Z1-N 3.3K
R1 180

U7-C
74S38
-DTACK
P5-27

U7-B
74S38
-VDTACK

U18
74ALS161

-IACKRST
-SAS
CLKB

U24-D
74ALS04
-LEDSFI
P6-26

U13-C
74HCT04

U7-A
74S38
-SYSFAIL
P5-17

SYSFAILINHIBIT
-PASSED

-MODID

U24-A
74ALS04
P6-57 MODID
R2 825

U24-E
74ALS04
-LEDRST
P6-37

U13-F
74HCT04
RESET

U4-B
74HCT08
-DEVRST
P6-25

U4-D
74HCT08
-IDEVRST

SIZE		SHEET	REV
B	769104	2 OF 5	F

-VROEEN
-VROEC0
-MROECK
-MROEEN
-VROEC1
-VSYSRESET
-VRO4C0
BD[00:15]
VD[00:15]
BDA[0:7]
VA[01:05]
-PASSED READY
-VRROEN
-MODID
-RDRDY
-WRRDY
-INTIRQA
P6-22
P6-11
-VXICTL0
-VXICTL1
-LED[0:3]
-LED0
-LED1
-LED2
-LED3
-ERR
-DOR
-DIR
-LEDFAIL
-LEDMODID
RESET
SYSFAILINHIBIT
P6-46
P6-36

U24-C
74ALS04

CR1
555-4007

+5V

Z2-A
3.3K

Z1-0
3.3K

U10-A
74ALS244

U5-A
74ALS244

U27
22P10

U26
22P10

U16
74HCT273

U23
74HCT574

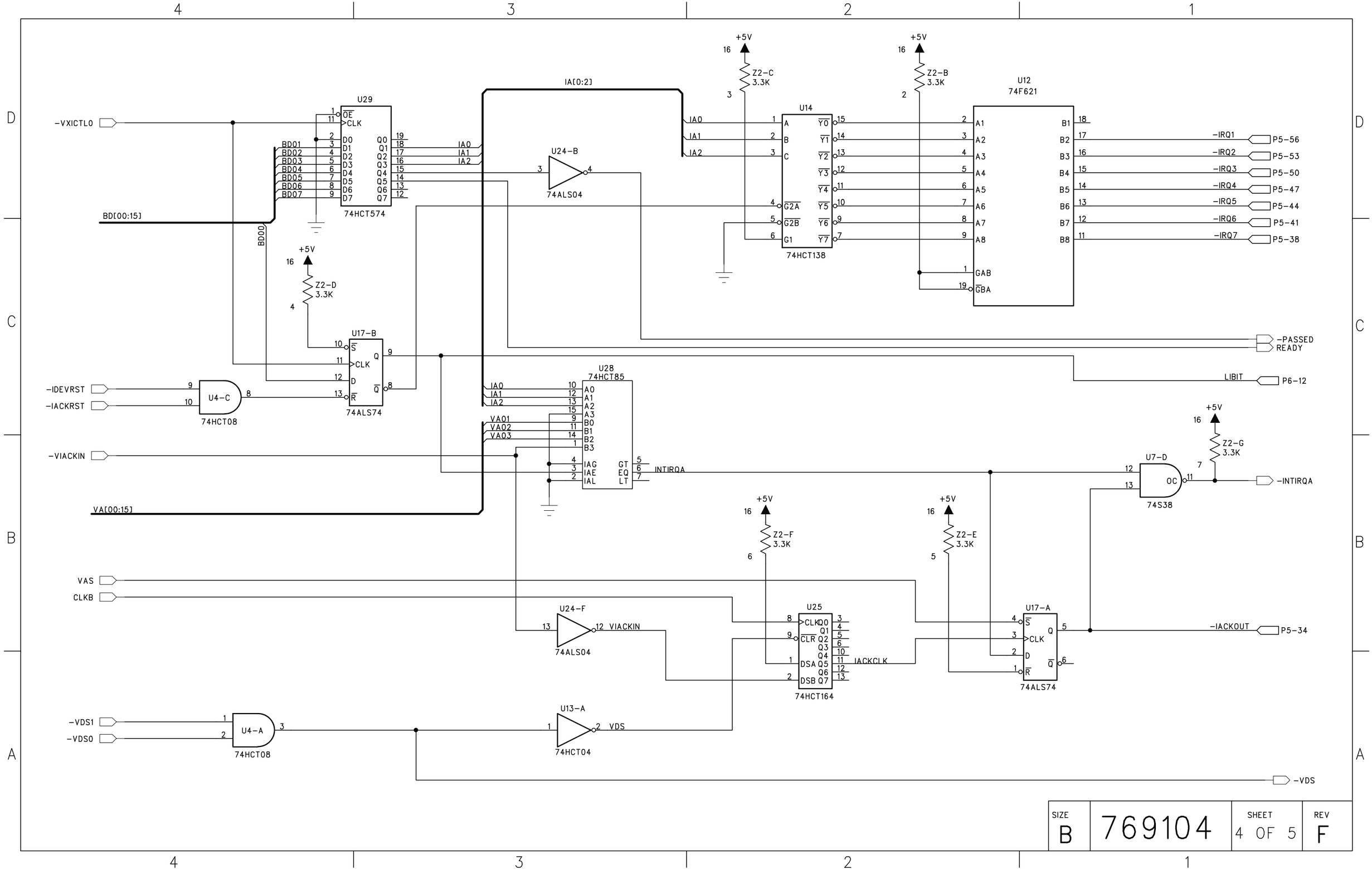
U30
74HCT574

U31
74HCT652

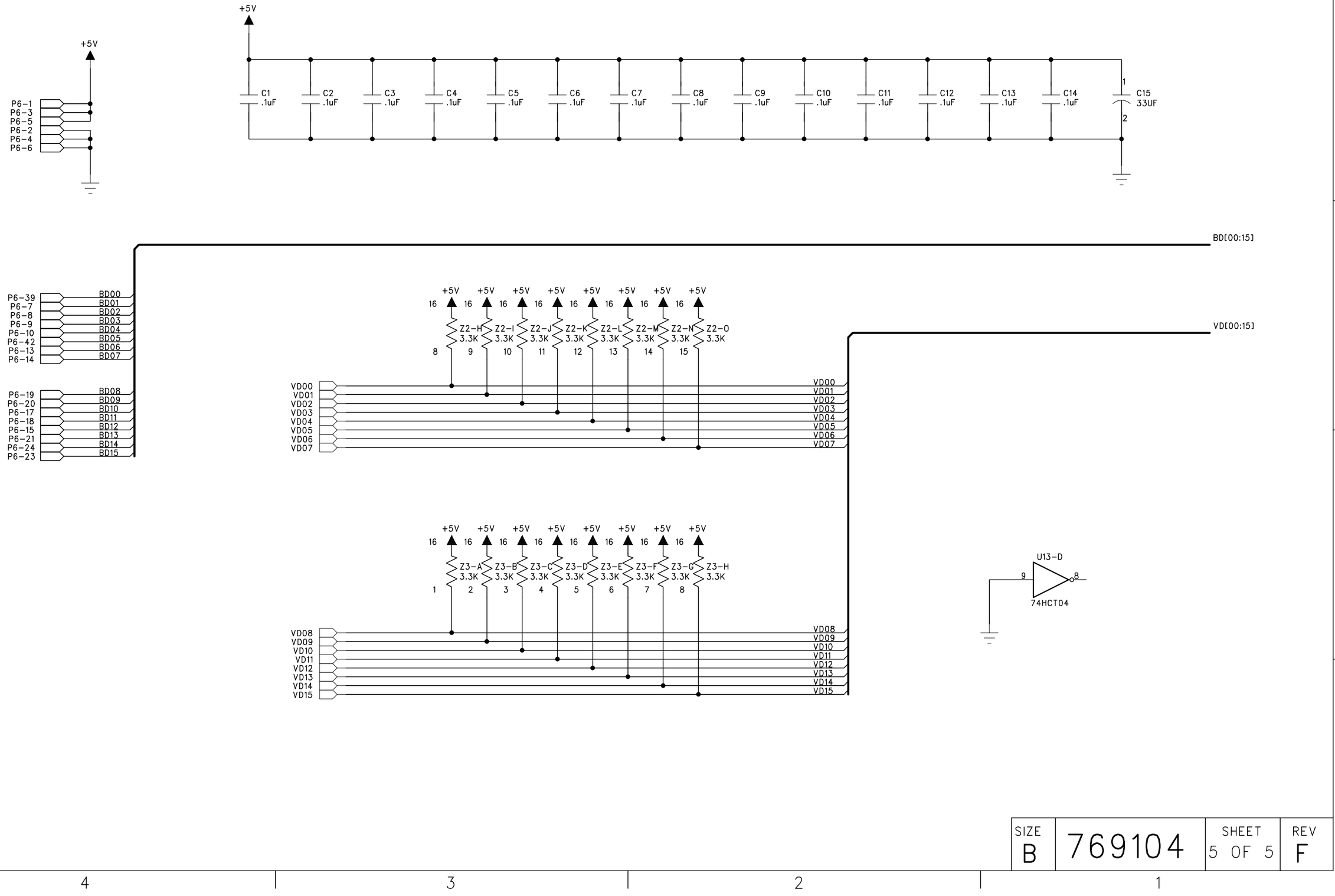
U19
74HCT652

BD[0:15]
VD[00:15]

SIZE		SHEET	REV
B	769104	3 OF 5	F



SIZE		SHEET	REV
B	769104	4 OF 5	F



SIZE	769104	SHEET	REV
B		5 OF 5	F

SECTION 9

UPDATE INFORMATION

9-1 INTRODUCTION

As NAI continues to improve the performance of the Model 5388, corrections and modifications to the manual may be required. This section contains Product Revision Sheet (PRS) data which updates the unit to the most current configuration available.

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