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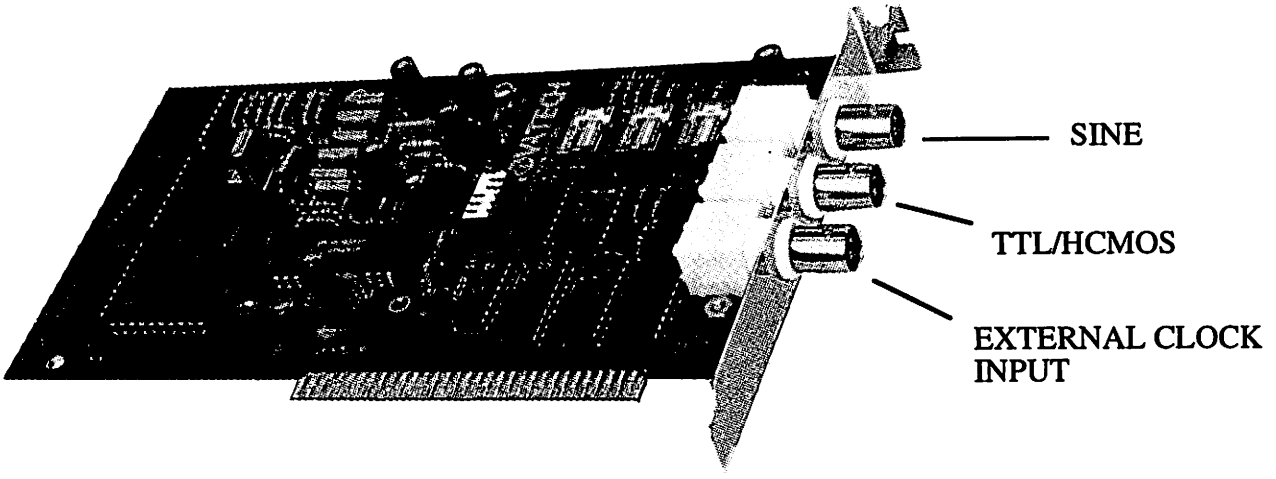
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NOVATECH INSTRUMENTS, INC.
DDS3 PC DIRECT DIGITAL SYNTHESIZER

INSTRUCTION MANUAL



DDS3 PC

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1.0 DESCRIPTION

1.1 The DDS3 PC is a 12 MHz Direct Digital Synthesizer on a printed circuit board for installation in a PC XT, PC AT or later ISA bus computer. The DDS3 PC provides both sine and clock output signals that can be set from 2 Hz to 12 MHz in 2 Hz steps. It also contains a precision 33.554432 MHz crystal oscillator that has 10 ppm accuracy and stability.

1.2 The built in oscillator can be bypassed to enable using an external clock input. In this way an external frequency source can be used as the system clock. This makes it possible to change the DDS3 PC step size and output range and to use a very accurate external frequency standard to increase the DDS3 PC accuracy and stability.

2.0 SPECIFICATIONS

2.1 OUTPUT

TYPES: Sine and HCMOS/TTL Simultaneously
IMPEDANCE: 50 ohms
RANGE: 2 Hz to 12 MHz in 2 Hz steps with internal clock (to 16 MHz with degraded specifications)
SINE AMPLITUDE: +20 dBm (6.3 Vpp) into 50 ohms, +26 dBm (12.6 Vpp) into open circuit (no attenuation)

2.2 SINE OUTPUT ATTENUATION

0 to 70 dB in 10 dB steps , ± 5% (+20dBm to -50dBm output, approx. 2.2 V to 707 µVrms into 50 ohms)

2.3 CONTROL

Output frequency, sinewave attenuation and clock source are set by four bytes of data in I/O address space starting at the base address set by an on-board switch (0338 Hex default). A C-language program is provided as an example. Both compiled and source code files are included. This program allows control of up to 1000 frequencies and amplitudes in the Command File mode or allows interactively setting frequency and amplitude. User programs can be created based upon the information given in this manual.

2.4 SPECTRAL PURITY

PHASE NOISE: < -90 dBc at 1 kHz offset
SPURIOUS: Typically < -55 dBc below 5 MHz, < -45 dBc from 5 to 12 MHz
HARMONIC: < -50 dBc below 5 MHz, < -40 dBc below 12 MHz

2.5 ACCURACY AND STABILITY

Accurate to < ± 5 ppm at 25 ± 2 °C, 24 hrs
Stable to ± 10ppm/year, 20 to 30 °C

2.6 EXTERNAL CLOCK INPUT

The DDS3 PC contains an internal 33.554432 MHz quartz crystal oscillator. It also accepts an external TTL/CMOS clock input of up to 40 MHz. The supplied program allows users to select the external input as the DDS3 PC system clock. An external clock will change the DDS3 PC step size in proportion to its ratio to the internal system clock.

2.7 SWITCHING TIME

NOVATECH supplied software allows frequency to be set in nominal 1 ms time increments and automatically adjusts for PC system speed. Attenuation changes in 10 ms maximum, with maximum of 10 changes per second.

2.8 POWER REQUIREMENTS (From Slot)

Uses <250 mA @ +5 V, <100 mA @ -5 V and <50 mA @ ± 12V.

2.9 CONNECTORS

BNCs provided for Sine Output, HCMOS Output and External Clock Input.

3.0 HARDWARE INSTALLATION

CAUTION

Opening your computer may expose live voltages so be sure to follow proper safety precautions.

WARNING

Before opening your computer or DDS3 PC package, connect the enclosed static strap to your wrist and follow the grounding instructions. Failure to follow static protection precautions may damage your computer or the DDS3 PC.

WARNING

Do not remove the metal bracket attached to the DDS3 PC. The bracket contains insulating washers that must be present. Removing and reinstalling this bracket without these washers could result in damage to the DDS3 PC and to your computer.

3.1 Install the DDS3 PC by plugging it into any PC XT, AT or later ISA bus computer. No switch settings or other adjustments are normally needed.

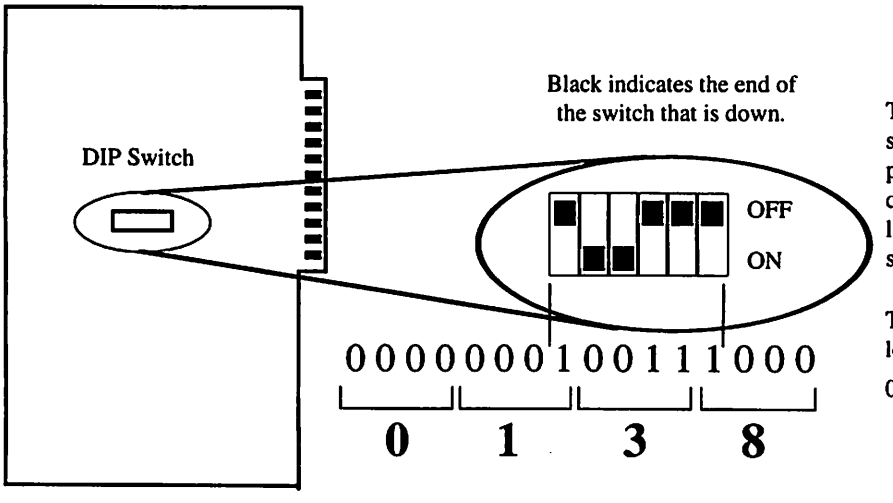
3.2 Locate the DDS3 PC in a slot as far removed from other cards as possible. This will lower noise pickup.

3.3 It may be necessary to change the DDS3 PC default address setting. This would occur if you are using more than one DDS3 PC in a single computer or if the DDS3 PC address conflicts with the address of other installed hardware.

3.4 To change the DDS-3PC address settings, you must change the setting on the DIP switch located on the DDS3 PC PCB (See Figure 1). There is only one DIP switch on the DDS3 PC so it is easy to find. This will establish a new starting address.

The DDS3 PC uses six sequential I/O space address locations on the PC ISA bus. These six addresses are defined by the DIP switch since it establishes the starting address. The DIP switch is set at the factory to 0338 Hex. Allowable settings are from 0200 Hex to 03F8 Hex in 08 Hex steps (0000 hex to 01F8 hex switch setting).

FIGURE 1



NOTE

The DDS3 PC address setting is equal to 0200 Hex plus the three bytes decoded. The bits to the left and right of the DIP switch are are read as 0.

The setting shown to the left provides an address of:

0138 + 0200 = 0338 Hex

4.0 DDS3 PC SOFTWARE

4.1 A C lanquage program called *dds3pc* is provided with the DDS3 PC. It includes a C language source code file and a compiled executable file. The ***dds3pc*** software makes it easy to control the DDS3 PC and can be operated in either an Immediate mode or a File mode. In the File mode, the program executes a sequence of up to 1000 commands from a data file.

4.2 To install the *dds3pc* program, copy all the files from the supplied floppy disk to your hard disk. (Note that it is also possible to run the ***dds3pc*** program from a floppy disk.)

4.3 To run the *dds3pc* program in Immediate Mode, go to the directory containing the ***dds3pc*** files and type ***dds3pc*** after the DOS prompt.

a) The ***dds3pc*** program will take 10 seconds to measure your computer system's operating speed and then **you will be asked for the DDS3 PC address setting.** If you have not changed the address from the default address of 0338 (Hex) then enter 0 and hit the Enter key. If you have changed the address then type in the new address and hit the enter key.

b) You will then be asked for the clock frequency. If you are using the DDS3 PC internal system clock, you must enter 0 or 33554432 and hit the Enter key. However, if you are using an external frequency source connected to the external clock input BNC on the DDS3 PC, then enter the frequency of this external clock and hit the Enter key. The ***dds3pc*** program must know the DDS3 PC system clock frequency in order to generate the correct output frequency. The ***dds3pc*** software will select the External Input if you enter any number except 0 or 33554432.

c) You will then be asked to enter the output frequency. Type in the frequency you would like the DDS3 PC to generate and hit the Enter key. If you enter a frequency that cannot be generated exactly, the ***dds3pc*** program will set the DDS3 PC to the nearest frequency that can be generated.

d) You will then be asked to enter the attenuation. You should enter an attenuation of 0, 10, 20, 30, 40, 50, 60, or 70 and then hit the enter key. The number entered is the value of the attenuation in dB. Every 10dB of attenuation will reduce the DDS3 PC output signal by a factor of 3.1623 Volts. For example, a 30dB attenuation reduces the output voltage by 3.1623^3. (See Table 6 for output values.)

The DDS3 PC output frequency and attenuation will change right after you enter the attenuation and hit the Enter key. This output will be maintained until you turn off the computer or enter a new frequency and attenuation setting.

e) The *dds3pc* program will ask you for frequency and attenuation settings again . It does not ask you for address and clock inputs again. To change the address or clock input you must quit to DOS and run the program again. You can quit the immediate mode and go back to DOS by entering a zero for the output frequency or by holding the control key and hitting c.

4.4 To use the *dds3pc* program in the File Mode you first create a data file containing ***dds3pc*** commands. This can be done using any text editing or word processing program as long as the file is saved as a text file. The ***dds3pc*** commands are listed and explained in Table 1. Table 2 shows a sample data file containing ***dds3pc*** commands.

4.5 To run the *dds3pc* program in the File Mode, go to the directory containing the ***dds3pc*** program and data files and type ***dds3pc*** followed by the data file name that contains the ***dds3pc*** commands. For example to run the example command data file named sample1 you would type "***dds3pc*** sample1" after the DOS prompt.

TABLE 1

dds3pc FILE MODE COMMANDS

EXAMPLE COMMAND	DESCRIPTION
addr 02F0	"Addr" followed by four digits loads the Hex value of the DDS3 PC address into the ***dds3pc*** Program. The default is 0338 and is not required to be entered unless the DDS3 PC address is changed. The example command would use the address 02F0 for the DDS3 PC.
clock 10.00e6	"Clock" followed by a floating point number enters the DDS3 PCsystem clock frequency. If the number is less than 1 or if it is equal to the internal clock frequency then the internal clock is used. If not, then the external clock is automatically selected. The example command would cause the DDS3 PC to use the external clock and assume the external clock frequency is 10 MHz. The clock default is internal and the record is not required unless you are changing to external or going from external back to internal.
out 1.234e6 10 1.25	"Out" followed by three floating point numbers sets the frequency, attenuation and dwell time. Dwell time delays execution of the next "out" command. A dwell time of 0 will cause a pause until the enter key is hit. When paused use Control C to quit. The example command would set the DDS3 PC output to 1.234 MHz set the DDS3 PC attenuation to 10 dB and delay 1.25 seconds before executing the next command
start out 1e6 10 10 out 10e6 20 10 stop	"Out" commands preceded by "start" and followed by "stop" comprise a sweep and will be continually repeated until the user hits a key. The example sequence of commands would set the output to 1 MHz and 10dB attenuation and pause for 10 seconds. It would then set the output to 10 MHz and 20 dB attenuation and pause for 10 seconds and then repeat until a key is hit. Only the last start/stop sequence in the file is repeated. All start/stop sequences in the file are executed at least once.
reset	Sets Frequency to zero and attenuation to 70 dB.
#	Allows adding comments to a file of commands. The ***dds3pc*** program ignores all lines beginning with the # character.

TABLE 2

dds3pc SAMPLE COMMAND FILE

```
# file name sample1
#
# Set system clock to internal 33.554432 MHz oscillator
#
clock 0
#
# Set output to 10 KHz, attenuation to 0 dB and dwell time to 12 seconds
#
out 10000 0 12
#
# Sweep a sequence of three output frequencies and attenuations
# and dwell for 5 seconds at each setting and then repeat the sweep
# until manually stopped from the keyboard
#
start
out 1e6 0 5
out 2e6 10 5
out 4e6 20 5
stop
```

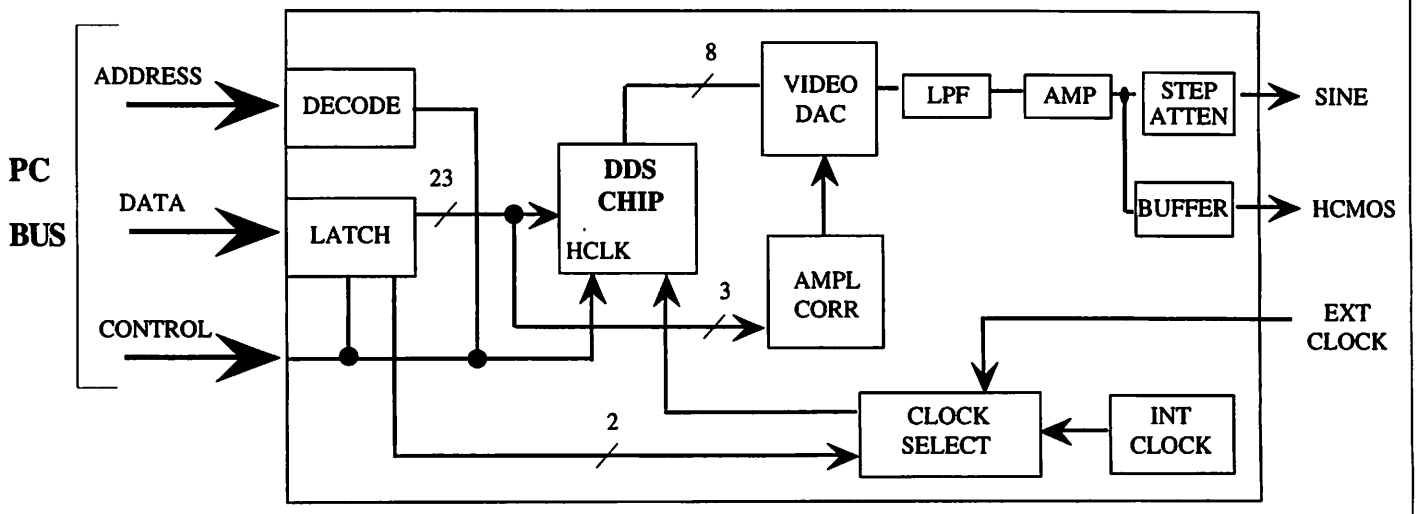
Note: When sweeping, hit any key to stop and exit to DOS

EXPLANATION

The ***dds3pc*** program reads the sample1 text file and looks at the beginning of each line for the keywords **clock**, **out**, **start** and **stop**. When it sees one of these keywords it treats them as commands and operates on the data following the word. If no keyword is found then ***dds3pc*** ignores the line. It is good practice to start comment lines with the character "#" to avoid accidently starting a comment line with a keyword.

When the ***dds3pc*** reads the sample1 file above it will see the first keyword, **clock**, and interpret the 0 that follows to mean use the DDS3 PC internal 33.554432 clock. It will then see the keyword **out** and interpret the 10000 <space> 0 <space> 12 that follows to mean set the DDS3 PC output to 10,000 Hz, set the attenuation to 0 dB and set the dwell time to 12 seconds. Finally it will see the **start**, **out**, **out**, **out** and **stop** keywords. The start keyword is interpreted to mean read the keywords that follow until you get to the stop keyword . When you get to the stop keyword then go back to the start keyword and repeat this sequence over again. Note that the ***dds3pc*** program will read scientific notation. The number 1e6 following the **out** keyword is interpreted as 1,000,000 Hz.

FIGURE 2
DDS3 PC SYSTEM BLOCK DIAGRAM



5.0 DDS3 PC THEORY OF OPERATION

NOTE

If you plan to write your own software or modify the supplied software, please read this section carefully as it contains critical information.

5.1 Refer to the System Block Diagram in Figure 2 for the following discussion. The Host Computer loads data into four 8-bit latches on the DDS3 PC. When the DDS3 PC detects an I/O write signal it decodes the PC address and, if the address matches a DDS3 PC address setting, it latches a data byte from the PC data bus. The four data bytes determine the source for the DDS3 PC system clock and the frequency and amplitude of the DDS3 PC output. Two additional addresses are used for HOP CLK and RESET commands which are executed immediately by the DDS3 PC.

5.2 The DDS3 PC uses six sequential addresses that start with the address number that is set on the DDS3 PC address DIP switch offset by 0200 hex. Table 3 shows the commands executed by the DDS3 PC for each of the six DDS3 PC addresses.

NOTE

The host computer controls are asynchronous to the timing on the DDS3 PC board.

5.3 At every cycle of the DDS3 PC clock, the DDS IC performs a computation and outputs a digital value equal to the computed amplitude of the sinewave at that point in time. This digital output goes to the DDS3 PC eight-bit Digital-to-Analog Converter (DAC) where it is converted to an analog signal. The analog signal from the DAC goes to an 11th order low pass filter, an amplifier, a step attenuator and then to the sine output connector. The sinewave is level shifted and buffered to generate the HCMOS output.

5.4 The computation performed by the 24 bit DDS IC processor on every clock cycle is a two step process. It first determines the phase angle in radians and then it uses the phase angle to calculate the amplitude of the sinewave.

5.5 The determination of phase angle is done using the on-chip phase accumulator. The DDS IC reads the frequency setting that is in the latches whenever it sees a transition on the HCLK line. The binary number read from the latches is stored in the Frequency Control Register inside the DDS IC. The Frequency Control Register value is added to the number in the DDS IC phase accumulator on each clock cycle.

5.6 The phase accumulator value is sent to the on-chip sine computation function where a new sinewave amplitude is computed every clock cycle. The frequency of the sinewave generated in this manner is determined by the value of the number read into the DDS IC Frequency Control Register. The relationship between this binary number and the generated output frequency is governed by the following equation:

$$FG = (FS \times FCR) \div 2^{24}$$

Where:

FG = Frequency Generated
FS = Frequency of System clock
FCR = Frequency Control Register Value
(Maximum FCR is 2^{24} = 16,777,216)

The internal system clock frequency of the DDS3-PC is equal to 2^{25} Hz, which is the decimal value 33,554,432 Hz. For this case the above equation simplifies to:

$$FG = 2 \text{ Hz} \times FCR$$

5.7 The Nyquist theoretical limit for the generated frequency is 50% of the system clock frequency. In practice it is desireable to have a steep rolloff output filter at about 40% of the system clock in order to minimize distortion.

5.8 The DDS3 PC has an 11 pole output filter with a corner frequency at 13.5 MHz which is about 40% of the internal system clock frequency. This is needed for a low distortion output since there are fewer and fewer steps as the output frequency approaches the system clock frequency. For example, there are only 2.5 digital-to-analog conversions per output sinewave cycle when the output is at 40% of the clock frequency.

5.9 If you are using an external clock at a frequency significantly lower than 33 MHz, then the DDS3 PC internal filter may have too high a corner frequency for acceptable harmonic and alias attenuation. You may need to add an external filter at about 40% of your external clock frequency in order to get satisfactory performance in this application.

5.10 The DDS IC is a 24 bit device and can read integer numbers from the Frequency Control Register that are up to 2^{24}=16,777,216 decimal. The smallest step size that can be generated is equal to the system clock frequency divided by this 16,777,216 value. For this reason, it is possible to obtain small step sizes by using a lower frequency external signal source as the system clock. Since the output is AC coupled, the lowest frequency that can be generated is approximately 2 Hz.

TABLE 3
PC BUS COMMANDS

PC BUS ADDRESS	PC BUS DATA	DDS-3PC COMMAND
Base Plus 0	Bit 0	Not Used
	Bit 1	Not Used
	Bit 2	Not Used
	Bit 3	Must Be Set To 0
	Bit 4	0 = Internal, 1 = external clock
	Bit 5	Amplitude Setting Bit 0 (40dB)
	Bit 6	Amplitude Setting Bit 1 (20dB)
	Bit 7	Amplitude Setting Bit 2 (10dB)
Base Plus 1	Don't Care	HOP CLK (Load a new frequency setting)
Base Plus 2	Don't Care	RESET (Sets Frequency Control Register to 0 and attenuation to 70 dB)
Base Plus 3	Bit 0	Frequency Setting Bit 0
	Bit 1	Frequency Setting Bit 1
	Bit 2	Frequency Setting Bit 2
	Bit 3	Frequency Setting Bit 3
	Bit 4	Frequency Setting Bit 4
	Bit 5	Frequency Setting Bit 5
	Bit 6	Frequency Setting Bit 6
	Bit 7	Frequency Setting Bit 7
Base Plus 4	Bit 0	Frequency Setting Bit 8
	Bit 1	Frequency Setting Bit 9
	Bit 2	Frequency Setting Bit 10
	Bit 3	Frequency Setting Bit 11
	Bit 4	Frequency Setting Bit 12
	Bit 5	Frequency Setting Bit 13
	Bit 6	Frequency Setting Bit 14
	Bit 7	Frequency Setting Bit 15
Base Plus 5	Bit 0	Frequency Setting Bit 16
	Bit 1	Frequency Setting Bit 17
	Bit 2	Frequency Setting Bit 18
	Bit 3	Frequency Setting Bit 19
	Bit 4	Frequency Setting Bit 20
	Bit 5	Frequency Setting Bit 21
	Bit 6	Frequency Setting Bit 22
	Bit 7	Not Used

Note1: Base address is between 0200 hex and 03F8 hex. Factory setting is 0338 hex.

Note2: All bits in Base Plus 0 are latched simultaneously. To prevent affecting other bits in the byte the status of the unused bits must be combined into the data byte written by the control software.

TABLE 4
RECOMMENDED TEST EQUIPMENT

ITEM	MINIMUM SPECIFICATION	RECOMMENDED
Oscilloscope	100 MHz	Tektronix TAS465 w/10x Probe
RF Probe	100 kHz to 25 MHz 500 mVrms-10 Vrms	Tektronix P6420 HP 34301A
DMM	3 1/2 Digits, Continuity AC rms, dBm	HP 34401A
50 Ohm Terminator	50 Ohms ±2%, 2 Watts	Tektronix 011-0049-01 Pomona 4119-50
Frequency Counter	8 Digits, ±1ppm	HP 5314A-001
External Signal/ Clock Source	CMOS/TTL output to 40 MHz	Novatech Instruments, Model 2910A

6.0 PERFORMANCE TEST

6.1 Install the DDS3 PC in a PC as directed in section 3 and install and run the ***dds3pc*** software as directed in section 4. The following tests can be performed using the ***dds3pc*** immediate mode to set in the test points. Test files are also provided that contain the test points and enable you to use the ***dds3pc*** file mode to perform the test. The file mode will reduce the amount of typing and thus make it easier and faster to perform the tests.

6.2 Verify the DDS3 PC output frequency by setting the DDS3 PC output frequency to each value shown in Table 5. The "test1" file contains these test points.

a) Connect a Frequency Counter to the DDS3 PC and set the frequency counter gate time to 1 second. Use a 50 ohm feedthrough terminator when connecting the counter.

b) Set the DDS3 PC Sine output frequency to each test point, measure the output with the frequency counter and verify that it is within the tolerance shown in Table 5. Take into consideration the measurement uncertainty of the frequency counter. See Table 4 for a recommended frequency counter.

6.3 Verify the DDS3 PC output attenuation by setting the attenuation to each value shown in Table 6. The ***dds3pc*** Immediate mode should be used to set these test points.

a) Connect an RMS AC meter to the Sine output and set the frequency to 10 KHz.

b) Set the DDS3 PC Sine output attenuation to the values shown in Table 6 and verify that it is within the tolerance shown. Take into consideration the measurement uncertainty of the RMS AC meter. See Table 4 for a recommended RMS AC meter.

TABLE 5
OUTPUT FREQUENCY TEST POINTS

Frequency	Tolerance	Actual
110 Hz	± 2 Hz	_____
1,110 Hz	± 2 Hz	_____
22,220 Hz	± 2 Hz	_____
333,330 Hz	± 2 Hz	_____
4,444,440 Hz	± 22 Hz	_____
8,888,880 Hz	± 44 Hz	_____
11,111,110 Hz	± 56 Hz	_____
12,000,000 Hz	± 60 Hz	_____

TABLE 6
ATTENUATION TEST POINTS

ATTENUATION dB	OPEN CIRCUIT dBm ± 2dBm	50 Ohm dBm ± 2dBm	ACTUAL
0	26	20	_____
10	16	10	_____
20	6	0	_____
30	-4	-10	_____
40	-14	-20	_____
50	-24	-30	_____
60	-34	-40	_____
70	-44	-50	_____
	Vrms ± 25%	Vrms ± 25%	
0	4.5	2.2	_____
10	1.4	.71	_____
20	.45	.22	_____
30	.14	.071	_____
40	.045	.022	_____
50	.014	.007	_____
60	.0045	.0022	_____
70	.0014	.00071	_____

6.4 Verify that the Sine output amplitude is flat across all frequencies by setting the DDS3 PC output frequency to each value shown in Table 7. The file "test2" contains these test points.

a) Connect an RF probe to the Sine output of the DDS3 PC , terminated in 50 ohms, and measure the output of the RF Probe with a DMM.

b) Measure the Sine output at the first frequency. Verify that the Sine output is within ± 2 dB (± 25%) of this first value at all other frequencies. Use the dB feature on the meter if available. Take into consideration the measurement uncertainty of the RF Probe. See Table 4 for recommended RF Probe and DMM.

6.5 Verify the clock output amplitude.
Use an Oscilloscope and a 10x probe and verify that the HCMOS clock output is 4.5V high to 0.5V low and that the symmetry is between 30/70% of time low/high to 70/30% of time low/high. Verify these values at the frequencies shown in Table 5.

6.6 Verify the external clock input feature by using an external signal source with the DDS3 PC external clock input to verify that the DDS3 PC outputs the correct frequencies. The file "test3" contains these test points.

a) Use the ***dds3pc*** software in immediate mode to setup the DDS3 PC for an external 40 MHz clock.

b) Connect an external signal source to the external clock input of the DDS3 PC. Set the external signal source to output 40 MHz.

c) Set the DDS3 PC Sine output frequency to each test point in Table 5. Measure the output with a frequency counter and verify that it is within the tolerance of your 40 MHz clock ± 2 Hz.

TABLE 7

Frequency	Actual	Tolerance
1 MHz	_____	_____
2 MHz	_____	_____
3 MHz	_____	_____
4 MHz	_____	_____
5 MHz	_____	_____
6 MHz	_____	_____
7 MHz	_____	_____
8 MHz	_____	_____
9 MHz	_____	_____
10 MHz	_____	_____
11 MHz	_____	_____
12 MHz	_____	_____

d) The accuracy of the external signal source and the measurement uncertainty of the frequency counter will affect the measurement and must be taken into consideration. See Table 4 for recommended signal source and frequency counter.

6.7 It is possible for the user to **calibrate the DDS3 PC** frequency output if it fails the performance verification described in paragraph 6.2. To do this, use the ***dds3pc*** software in the immediate mode and perform the following:

CAUTION

Opening your computer may expose live voltages so be sure to follow proper safety precautions.

WARNING

Before opening your computer connect the enclosed static strap to your wrist, and follow the grounding instructions. Failure to follow static protection precautions may damage your computer or the DDS3 PC.

a) Set the DDS3 PC to internal clock, attenuation of 0 and 10 MHz output frequency.

b) It may be necessary to use a board extender in order to gain access to capacitor C31.

c) Adjust capacitor C31 with an insulated adjustment tool until the DDS3 PC Sine output reads 10 MHz to better than ± 50 Hz when read with a frequency counter. Be sure to account for the measurement uncertainties of the counter. See Table 4 for a recommended frequency counter. C31 is the only user adjustable component on the DDS3 PC.

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