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SPECIFICATION

NVIDIA Jetson Xavier Developer Kit Carrier Board

Abstract

This document contains recommendations and guidelines for Engineers to follow to create modules for the expansion connectors on the Jetson™ Xavier carrier board as well as understand the capabilities of the other dedicated interface connectors and associated power solutions on the platform.

CAUTION:

1. ALWAYS CONNECT THE JETSON XAVIER & ALL EXTERNAL PERIPHERAL DEVICES BEFORE CONNECTING THE POWER SUPPLY TO THE AC POWER JACK OR TYPE C CONNECTOR.

2. The NVIDIA® Jetson Xavier Developer Kit carrier board contains ESD-sensitive parts. Always use appropriate anti-static and grounding techniques when working with the system. Failure to do so can result in ESD discharge to sensitive pins, and irreparably damage your Jetson Xavier carrier board. NVIDIA will not replace units that have been damaged due to ESD discharge.

Document Change History

Date	Description
August 9, 2018	Initial Release

NVIDIA.

Table of Contents

1.0 INTRODUCTION 4

1.1 Jetson Xavier Feature List 4
1.2 Carrier Board Feature List 4
1.3 Jetson Xavier Carrier Board Block Diagram 5

2.0 JETSON CARRIER BOARD STANDARD CONNECTORS 8

2.1 USB Ports 8
2.2 Gigabit Ethernet Connector 11
2.3 HDMI Connector 12
2.4 PCIe x16 Connector 13
2.5 UFS / Micro SD Card Socket 16
2.6 eSATA / USB 3.1 Type A Connector 17
2.7 M.2, Key E Expansion Slot 18
2.8 M.2, Key M Expansion Slot 20
2.9 Audio Panel Header 22
2.10 JTAG Header 22

3.0 CARRIER BOARD CUSTOM EXPANSION CONNECTIONS 24

3.1 Module Connector 24
3.2 Camera Expansion Header 24
3.3 Expansion Header 28
3.4 Fan Connector 31
3.5 Automation Header 31
3.6 DC Power Jack 32

4.0 MISCELLANEOUS 33

4.1 Buttons, Jumpers & Indicators 33

5.0 INTERFACE POWER 34

1.0 INTRODUCTION

The NVIDIA® Jetson Xavier carrier board is ideal for software development within the Linux environment. Standard connectors are used to access Jetson Xavier features and interfaces, enabling a highly flexible and extensible development platform. Go to https://developer.nvidia.com/embedded-computing or contact your NVIDIA representative for access to software updates and the developer SDK supporting the OS image and host development platform that you want to use. The developer SDK includes an OS image that you will load onto your Jetson Xavier device, supporting documentation, and code samples to help you get started.

1.1 Jetson Xavier Feature List

Applications Processor
- Xavier

Memory
- 16GB 256-bit wide LPDDR4x DRAM
- 32GB eMMC 5.1

Network
- RGMII I/F for 10/100/1000 BASE-T Ethernet

Advanced power management
- Dynamic voltage and frequency scaling
- Multiple clock and power domains
- Thermal Transfer Plate & optional Fan/Heatsink

1.2 Carrier Board Feature List

Connection to Jetson Xavier
- 699-pin (11x65) board-board connector

Storage
- MicroSD Card + UFS combo socket
- USB / eSATA connector

USB
- 2 x USB type C connectors

Wired Network
- Gigabit Ethernet (RJ45 connector)

PCIe
- Standard PCIe® x16 connector (lower x8 used)

Display
- HDMI type A connector
- 2xDP routed to type C connectors

Camera Expansion Header
- 120-pin (2x60) Board-Board
- CSI: 6, x2 – 8, x4 (D-PHY or C-PHY)
- Camera CLK, I2C & Control

M.2 Key E Connector
- PCIe x1 Lane, USB 2.0
- I2S, UART, I2C, Control

M.2 Key M Connector
- PCIe x4 Lane, Control

Expansion Header
- 40-pin (2x20) header
- I2C, SPI, UART, I2S, CAN, D-MIC

UI & Indicators
- Power, Reset & Force Recovery Buttons
- LED: Main 5.0V Supply

Debug
- JTAG Connector (2x5-pin header)

Miscellaneous
- Fan Connector: 5V, PWM & Tach

Power
- DC Jack: 9V to 20V (19V Adapter included)
- Main 5V Supply: NCP81239
- Main 3.3V Supply: TPS53015
- Main 1.8V Buck Supply: APW7307
- USB VBUS Load Switches: RT9715 & APL3511
- 12V Boost (PCIe): NCP81239
- Load Switches/LDOs (SD/HDMI/Display/Camera)

Developer Kit Operating Temperature Range
- 0ºC to 50ºC

1.3 Jetson Xavier Carrier Board Block Diagram

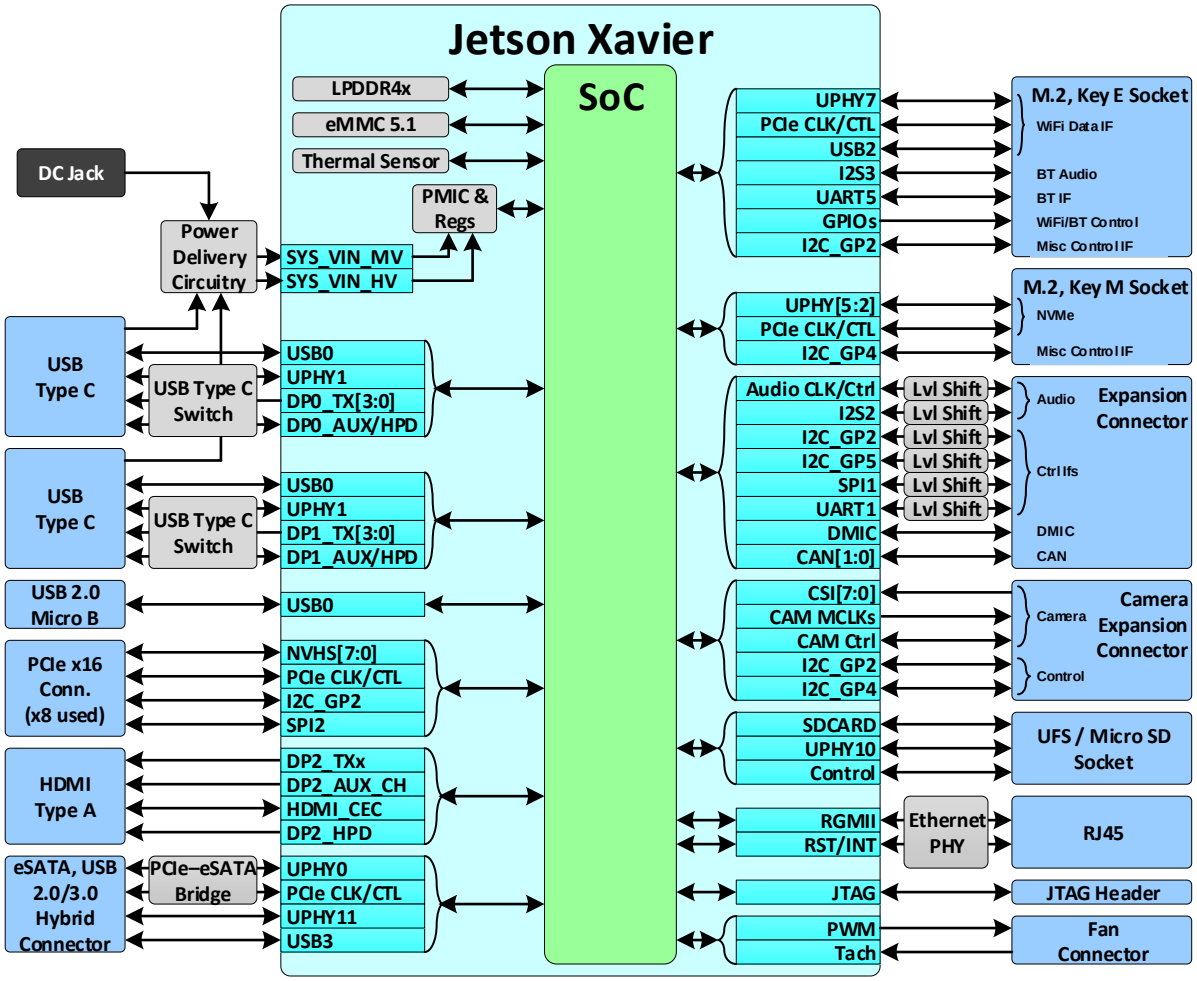
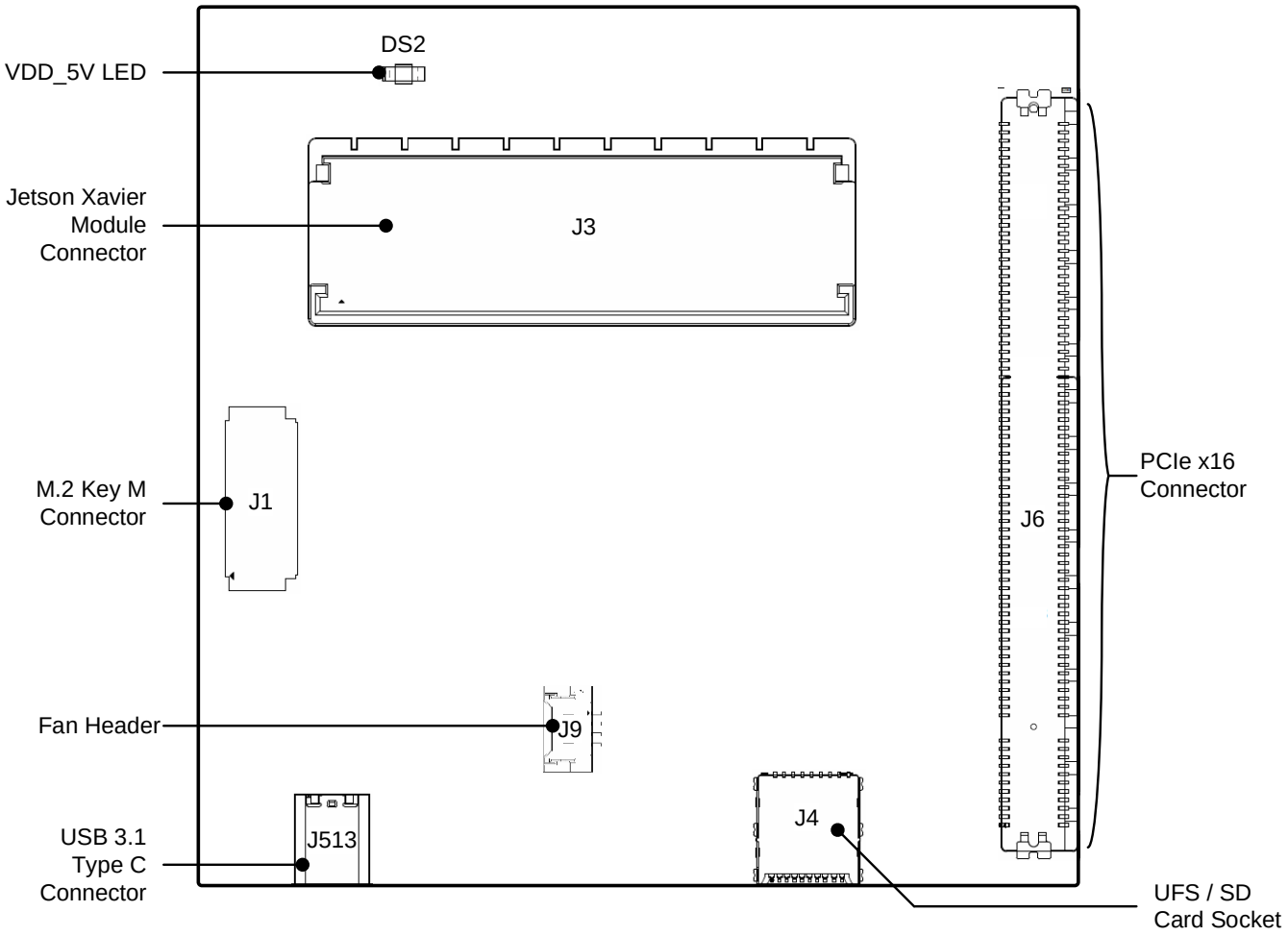
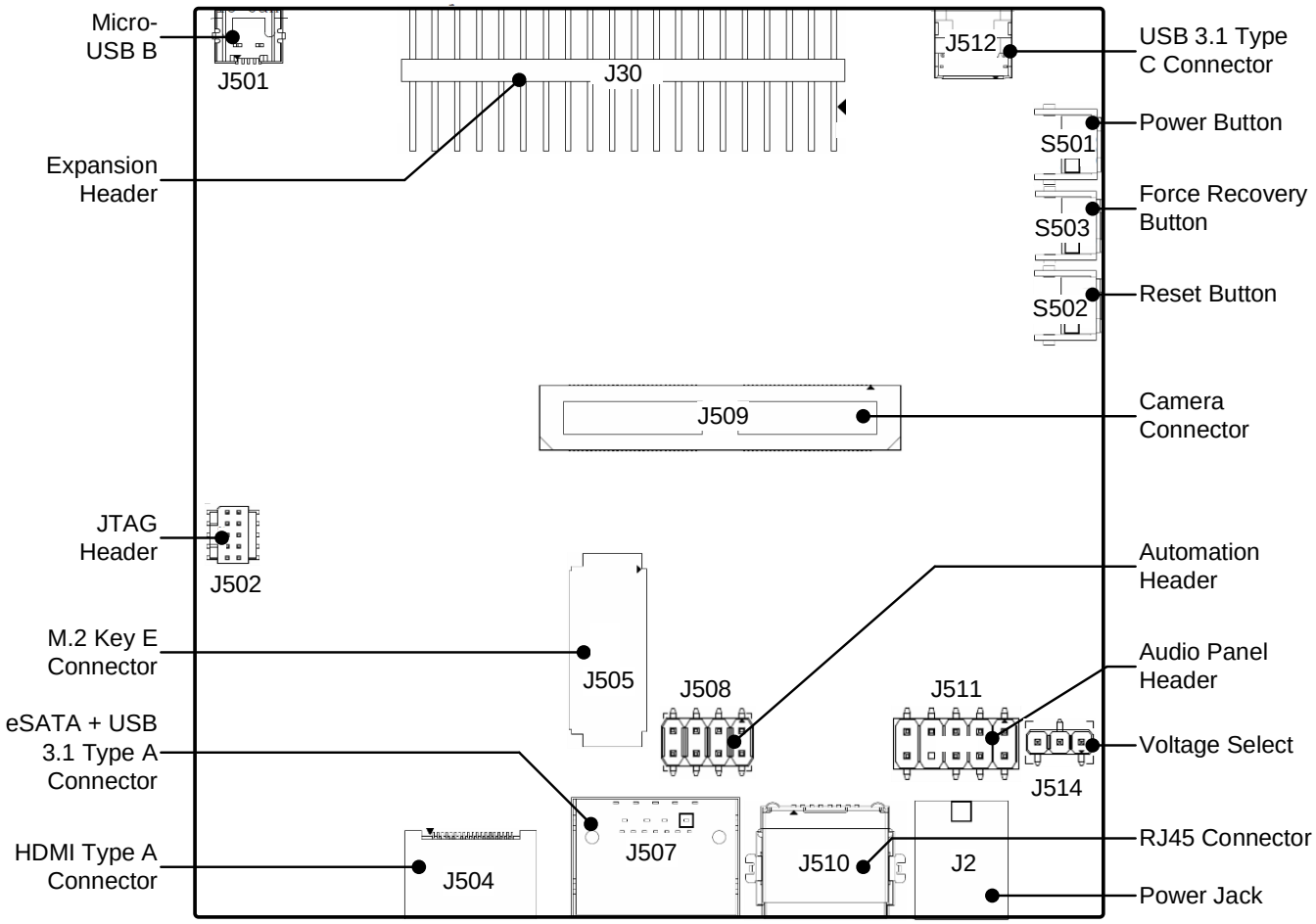


Figure 1. Jetson Xavier Carrier Board Placement (Top View)



J1	M.2 Key M Connector (75-pin)	**J9**	Fan Header (4-pin, 1.25mm pitch)
J3	Jetson Xavier Connector (65x11)	**J513**	USB Type C Connector #2
J4	MicroSD & UFS Socket	**DS2**	VDD_5V LED
J6	PCIe x16 Connector		

Figure 2. Jetson Xavier Carrier Board Placement (Bottom View)



J2	Power Jack
J30	Expansion Header (2x20, 2.54mm pitch)
J501	Micro USB B Connector (for UART console)
J502	JTAG Header (2x5, 1.27 pitch)
J504	HDMI Type A Connector
J505	M.2 Key E Connectivity Connector (75-pin)
J507	eSATA + USB 3.1 Type-A Connector
J508	Automation Header (2x4, 2.54mm pitch)
J509	Camera Connector (2x60, 0.5mm pitch)
J510	RJ45 Ethernet Connector
J511	Audio Panel Header (2x5, 2.54mm pitch)
J512	USB Type C Connector #1
J514	Voltage select for Expansion Header Signal Level Shifters (1x3, 2.54mm pitch)
S501	Power Button
S502	Reset Button
S503	Force Recovery Button

2.0 JETSON CARRIER BOARD STANDARD CONNECTORS

The Jetson Xavier carrier board provides a number of standard expansion connectors to support additional functionality beyond what is integrated on the main platform board. This includes:

- USB 3.1: 2x Type C Connectors
- Gigabit Ethernet: RJ45 Connector
- HDMI: Type A Connector
- PCIe® x16 Connector
- UFS / Micro SD Card Socket
- eSATA: Standard SATA Connector, 22-pin including power
- M.2, Key E Socket
- M.2, Key M Socket
- Audio Panel Header
- JTAG

2.1 USB Ports

The carrier board supports two USB Type C Connectors (J512 & J513 shown in the figure below). These connectors support USB 3.1 and alternately Display Port. The USB connector J512 supports recovery mode. In addition, a USB 2.0 Micro B connector (J501) is supported. This connector provides access to a UART console and the carrier board Power/Reset/Force Recovery signals. Recovery mode is not supported on this connector.

Figure 3. USB Type C Port Connections

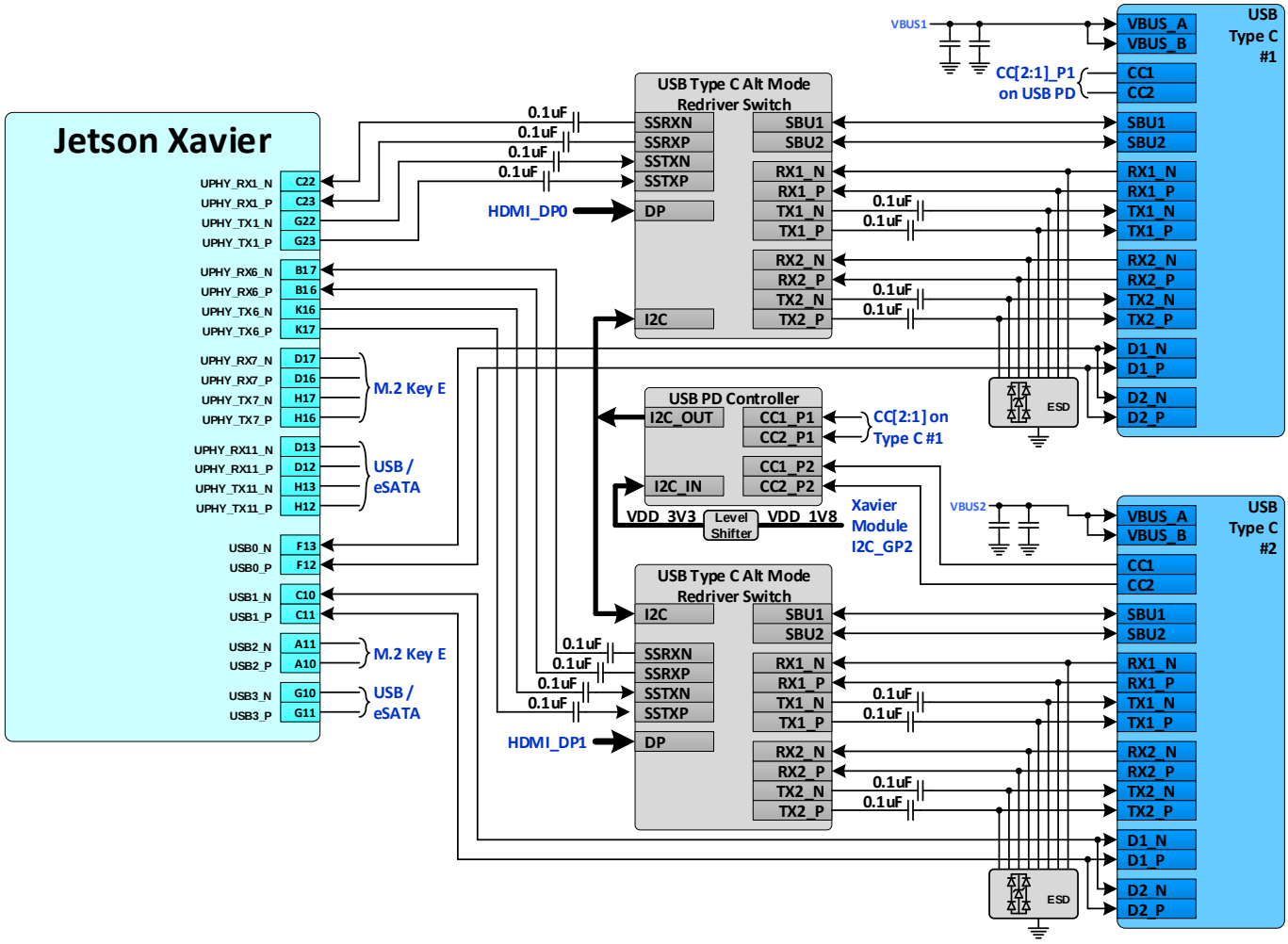


Table 1. USB 3.1 Type C Connector Pin Descriptions (J512)

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/ Direction
A1	GND	–	Ground	Ground	B1	GND	–	Ground	Ground
A2	USB0_TX1_DUT_P	–	USB 3.1 #0 Transmit 1 +	Output	B2	USB0_TX2_DUT_P	–	USB 3.1 #0 Transmit 2 +	Output
A3	USB0_TX1_DUT_N	–	USB 3.1 #0 Transmit 1 –	Output	B3	USB0_TX2_DUT_N	–	USB 3.1 #0 Transmit 2 –	Output
A4	VBUS1	–	USB VBUS Power	Power	B4	VBUS1	–	USB VBUS Power	Power
A5	USB0_CC1_DUT	–	Type C #0 Config Channel 1	Bidir	B5	USB0_CC2_DUT	–	Type C #0 Config Channel 2	Bidir
A6	USB0_D1_P	–	USB 2.0 #0 (Inst. 1) Data +	Bidir	B6	USB0_D2_P	–	USB 2.0 #0 (Inst. 2) Data +	Bidir
A7	USB0_D1_N	–	USB 2.0 #0 (Inst. 1) Data –	Bidir	B7	USB0_D2_N	–	USB 2.0 #0 (Inst. 2) Data –	Bidir
A8	USB0_SBU1_DUT	–	Type C #0 Sideband Use 1	Bidir	B8	USB0_SBU2_DUT	–	Type C #0 Sideband Use 2	Bidir
A9	VBUS1	–	USB VBUS Power	Power	B9	VBUS1	–	USB VBUS Power	Power
A10	USB0_RX2_DUT_N	–	USB 3.1 #0 Receive 2 –	Input	B10	USB0_RX1_DUT_N	–	USB 3.1 #0 Receive 1 –	Input
A11	USB0_RX2_DUT_P	–	USB 3.1 #0 Receive 2 +	Input	B11	USB0_RX1_DUT_P	–	USB 3.1 #0 Receive 1 +	Input
A12	GND	–	Ground	Ground	B12	GND	–	Ground	Ground

Table 2. USB 3.1 Type C Connector Pin Descriptions (J513)

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/ Direction
A1	GND	–	Ground	Ground	B1	GND	–	Ground	Ground
A2	USB1_TX1_DUT_P	–	USB 3.1 #1 Transmit 1 +	Output	B2	USB1_TX2_DUT_P	–	USB 3.1 #1 Transmit 2 +	Output
A3	USB1_TX1_DUT_N	–	USB 3.1 #1 Transmit 1 –	Output	B3	USB1_TX2_DUT_N	–	USB 3.1 #1 Transmit 2 –	Output
A4	VBUS2	–	USB VBUS #2 Power	Power	B4	VBUS2	–	USB VBUS #2 Power	Power

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/ Direction
A5	USB1_CC1_DUT	–	Type C #1 Config Channel 1	Bidir	B5	USB1_CC2_DUT	–	Type C #1 Config Channel 2	Bidir
A6	USB1_DP	–	USB 2.0 #1 Data +	Bidir	B6	USB1_DP	–	USB 2.0 #1 Data +	Bidir
A7	USB1_DN	–	USB 2.0 #1 Data –	Bidir	B7	USB1_DN	–	USB 2.0 #1 Data –	Bidir
A8	USB1_SBU1_DUT	–	Type C #1 Sideband Use 1	Bidir	B8	USB1_SBU2_DUT	–	Type C #1 Sideband Use 2	Bidir
A9	VBUS2	–	USB VBUS #2 Power	Power	B9	VBUS2	–	USB VBUS #2 Power	Power
A10	USB1_RX2_DUT_N	–	USB 3.1 #1 Receive 2 +	Input	B10	USB1_RX1_DUT_N	–	USB 3.1 #1 Receive 1 +	Input
A11	USB1_RX2_DUT_P	–	USB 3.1 #1 Receive 2 –	Input	B11	USB1_RX1_DUT_P	–	USB 3.1 #1 Receive 1 –	Input
A12	GND	–	Ground	Ground	B12	GND	–	Ground	Ground

Legend	Ground	Power	Reserved

Notes:
- The USB[1:0]_TX/RX lines can alternately carry DP signaling. In that case, the SBU pins carry DP_AUX and CC1 pins carry HPD functionality.
- In the Type/Dir column, Output is to USB Connectors. Input is from USB Connectors. Bidir is for Bidirectional signals.

Table 3. USB 2.0 Micro B Connector Pin Descriptions (J501)

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	VBUS	–	VBUS Supply	Power
2	MS_USB_DN	USB0_D–	USB 2.0 #0 Data -	Bidir
3	MS_USB_DP	USB0_D+	USB 2.0 #0 Data +	Bidir
4	NC	–	Unused	–
5	GND	–	Ground	Ground

Legend	Ground	Power	Reserved

Notes: In the Type/Dir column, Output is to USB Connector. Input is from USB Connector. Bidir is for Bidirectional signals.

2.2 Gigabit Ethernet Connector

The carrier board implements an RJ45 connector (J510) along with the necessary magnetics device.

Figure 4. Gigabit LAN Connections

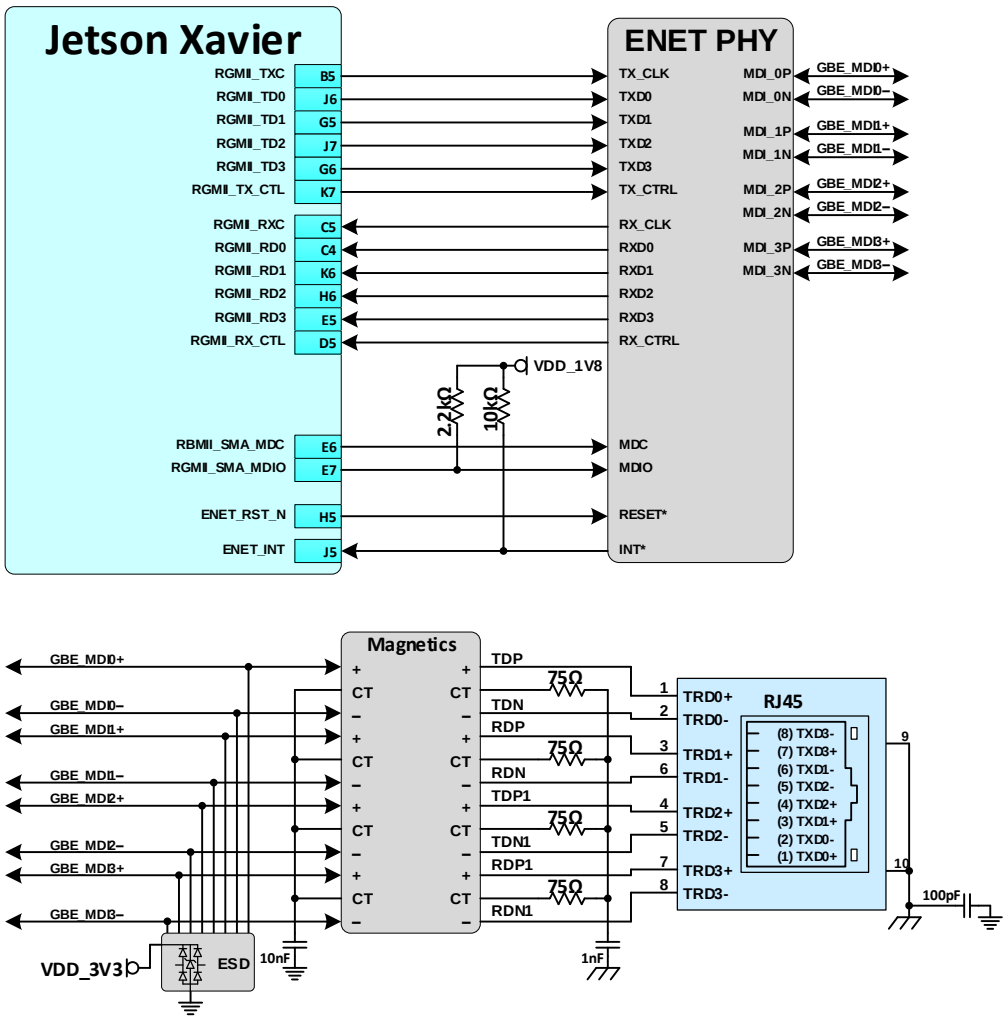


Table 4. Ethernet RJ45 Connector Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
1	RJ45_TD_P	–	Gigabit Ethernet MDI 0+	Bidir
2	RJ45_TD_N	–	Gigabit Ethernet MDI 0–	Bidir
3	RJ45_RD_P	–	Gigabit Ethernet MDI 1+	Bidir
4	RJ45_TD1_P	–	Gigabit Ethernet MDI 2+	Bidir
5	RJ45_TD1_N	–	Gigabit Ethernet MDI 2–	Bidir
6	RJ45_RD_N	–	Gigabit Ethernet MDI 1–	Bidir
7	RJ45_RD1_P	–	Gigabit Ethernet MDI 3+	Bidir
8	RJ45_RD1_N	–	Gigabit Ethernet MDI 3–	Bidir

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to RJ45 Connector. Input is from RJ45 Connector. Bidir is for Bidirectional signals.

2.3 HDMI Connector

A standard HDMI type A connector (J504) is supported.

Figure 5. HDMI Connections

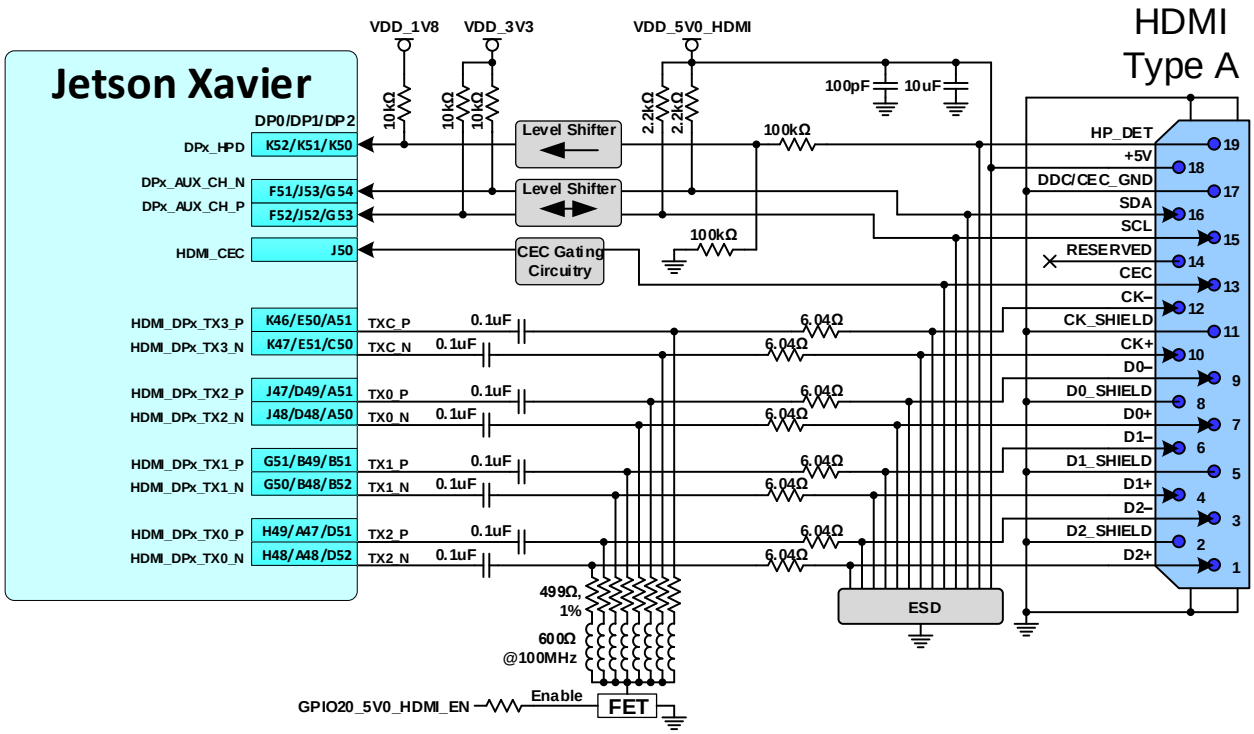


Table 5. HDMI Connector Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
1	IFP_TXD2_CR1	HDMI_DP2_TX0_N	HDMI Transmit Data 2+	Output
2	SHIELD/GND	–	Ground	Ground
3	IFP_TXD2_CR1*	HDMI_DP2_TX0_N	HDMI Transmit Data 2–	Output
4	IFP_TXD1_CR1	HDMI_DP2_TX1_P	HDMI Transmit Data 1+	Output
5	SHIELD/GND	–	Ground	Ground
6	IFP_TXD1_CR1*	HDMI_DP2_TX1_N	HDMI Transmit Data 1–	Output
7	IFP_TXD0_CR1	HDMI_DP2_TX2_P	HDMI Transmit Data 0+	Output
8	SHIELD/GND	–	Ground	Ground
9	IFP_TXD0_CR1*	HDMI_DP2_TX2_N	HDMI Transmit Data 0–	Output
10	IFP_TXC_CR1	HDMI_DP2_TX3_P	HDMI Transmit Clock+	Output
11	SHIELD/GND			
12	IFP_TXC_CR1*	HDMI_DP2_TX3_N	HDMI Transmit Clock–	Output
13	HDMI_CEC_CON	HDMI_CEC	HDMI CEC	Bidir
14	RESERVED	–	Unused	Unused
15	I2CW_SCL_C	DP2_AUX_CH_P	HDMI DDC Clock	Output /OD
16	I2CW_SDA_C	DP2_AUX_CH_N	HDMI DDC Data	Bidir/OD
17	GND	–	Ground	Ground
18	VDD_5V0_HDMI_CON	–	HDMI 5V Power	Power
19	HDMI_C_HPD_C	DP2_HPD	Hot Plug Detect	Input

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to HDMI Connector. Input is from HDMI Connector. Bidir is for Bidirectional signals.

2.4 PCIe x16 Connector

The Jetson carrier board includes a standard PCIe x16 connector (J6). Only the first x8 portion of the connector is used to support up to 8 PCIe lanes.

Figure 6. PCIe x16 Connector Connections

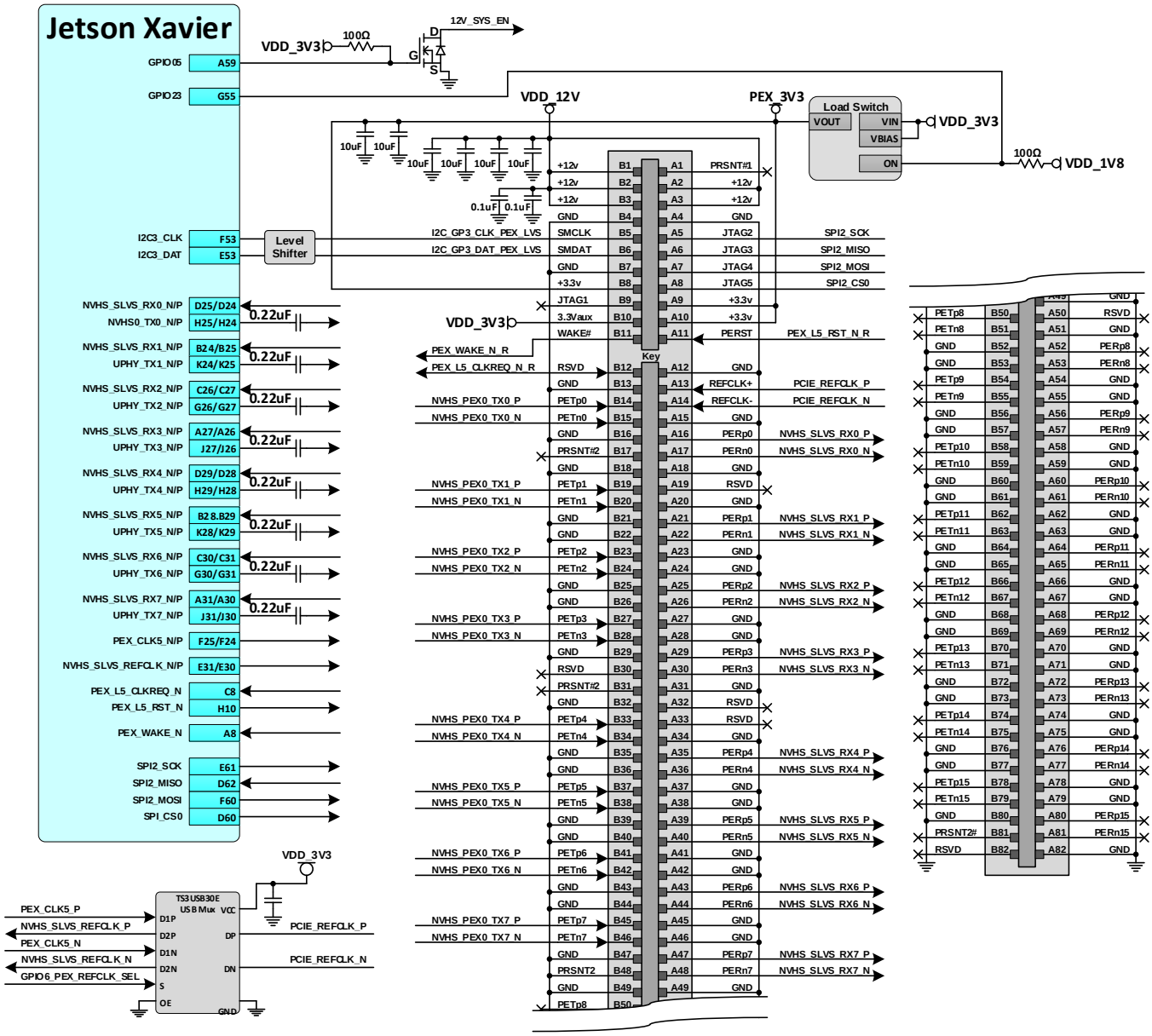


Table 6. PCIe 8-lane Connector Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/ Direction
A1	GND (PRSNT1_N)	–	Ground	Ground	B1	VDD_12V	–	12V Supply	Power
A2	VDD_12V	–	12V Supply	Power	B2	VDD_12V			
A3	VDD_12V				B3	VDD_12V			
A4	GND	–	Ground	Ground	B4	GND	–	Ground	Ground
A5	SPI2_SCK	SPI2_SCK	SPI 2 Clock	Output	B5	GEN1_I2C_SCL_3V3_LVL	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD
A6	SPI2_MISO	SPI2_MISO	SPI 2 Master In/Slave Out	Input	B6	GEN1_I2C_SDA_3V3_LVL	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD
A7	SPI2_MOSI	SPI2_MOSI	SPI 2 Master Out/Slave In	Output	B7	GND	–	Ground	Ground
A8	SPI2_CS0	SPI2_CS0	SPI 2 Chip Select #0	Output	B8	VDD_3V3	–	3.3V supply	Power
A9	VDD_3V3	–	3.3V supply	Power	B9	RSVD	–	Reserved	Reserved
A10	VDD_3V3				B10	RSVD			
A11	PCIE0_L0_RST	PEX0_RST#	PCIe Lane 0 Reset	Output	B11	PCIE_WAKE	PEX_WAKE#	PCIe Wake (Shared)	Input
A12	GND	–	Ground	Ground	B12	PCIE0_L0_CLKREQ	PEX0_CLKREQ#	PCIe Ctlr 0 Clock Req.	Bidir
A13	PCIE_REFCLK_P	PEX_CLK5+ (Note)	PCIe IF 5 Reference Clock +	Output	B13	GND	–	Ground	Ground
A14	PCIE_REFCLK_N	PEX_CLK5– (Note)	PCIe IF 5 Reference Clock –	Output	B14	NVHS_PEX0_TX0_P	NVHS0_TX0_P	PCIe IF 5 Lane 0 Transmit +	Output
A15	GND	–	Ground	Ground	B15	NVHS_PEX0_TX0_N	NVHS0_TX0_N	PCIe IF 5 Lane 0 Transmit –	Output
A16	NVHS_SLVS_RX0_P	NVHS0_SLVS_RX0_P	PCIe IF 5 Lane 4 Receive +	Input	B16	GND	–	Ground	Ground
A17	NVHS_SLVS_RX0_N	NVHS0_SLVS_RX0_N	PCIe IF 5 Lane 4 Receive –	Input	B17	RSVD	–	Reserved	Reserved
A18	GND	–	Ground	Ground	B18	GND	–	Ground	Ground
A19	RSVD	–	Reserved	Reserved	B19	NVHS_PEX0_TX1_P	NVHS0_TX1_P	PCIe IF 5 Lane 1 Transmit +	Output
A20	GND	–	Ground	Ground	B20	NVHS_PEX0_TX1_N	NVHS0_TX1_N	PCIe IF 5 Lane 1 Transmit –	Output
A21	NVHS_SLVS_RX1_P	NVHS0_SLVS_RX1_P	PCIe IF 5 Lane 4 Receive +	Input	B21	GND	–	Ground	Ground
A22	NVHS_SLVS_RX1_N	NVHS0_SLVS_RX1_N	PCIe IF 5 Lane 4 Receive –	Input	B22	GND			
A23	GND	–	Ground	Ground	B23	NVHS_PEX0_TX2_P	NVHS0_TX2_P	PCIe IF 5 Lane 2 Transmit +	Output
A24	GND				B24	NVHS_PEX0_TX2_N	NVHS0_TX2_N	PCIe IF 5 Lane 2 Transmit –	Output
A25	NVHS_SLVS_RX2_P	NVHS0_SLVS_RX2_P	PCIe IF 5 Lane 4 Receive +	Input	B25	GND	–	Ground	Ground
A26	NVHS_SLVS_RX2_N	NVHS0_SLVS_RX2_N	PCIe IF 5 Lane 4 Receive –	Input	B26	GND			
A27	GND	–	Ground	Ground	B27	NVHS_PEX0_TX3_P	NVHS0_TX3_P	PCIe IF 5 Lane 3 Transmit +	Output
A28	GND				B28	NVHS_PEX0_TX3_N	NVHS0_TX3_N	PCIe IF 5 Lane 3 Transmit –	Output
A29	NVHS_SLVS_RX3_P	NVHS0_SLVS_RX3_P	PCIe IF 5 Lane 4 Receive +	Input	B29	GND	–	Ground	Ground
A30	NVHS_SLVS_RX3_N	NVHS0_SLVS_RX3_N	PCIe IF 5 Lane 4 Receive –	Input	B30	RSVD	–	Reserved	Reserved
A31	GND	–	Ground	Ground	B31	RSVD			
A32	RSVD	–	Reserved	Reserved	B32	GND	–	Ground	Ground
A33	RSVD				B33	NVHS_PEX0_TX4_P	NVHS0_TX4_P	PCIe IF 5 Lane 4 Transmit +	Output
A34	GND	–	Ground	Ground	B34	NVHS_PEX0_TX4_N	NVHS0_TX4_N	PCIe IF 5 Lane 4 Transmit –	Output
A35	NVHS_SLVS_RX4_P	NVHS0_SLVS_RX4_P	PCIe IF 5 Lane 4 Receive +	Input	B35	GND	–	Ground	Ground
A36	NVHS_SLVS_RX4_N	NVHS0_SLVS_RX4_N	PCIe IF 5 Lane 4 Receive –	Input	B36	GND			
A37	GND	–	Ground	Ground	B37	NVHS_PEX0_TX5_P	NVHS0_TX5_P	PCIe IF 5 Lane 5 Transmit +	Output
A38	GND				B38	NVHS_PEX0_TX5_N	NVHS0_TX5_N	PCIe IF 5 Lane 5 Transmit –	Output
A39	NVHS_SLVS_RX5_P	NVHS0_SLVS_RX5_P	PCIe IF 5 Lane 5 Receive +	Input	B39	GND	–	Ground	Ground
A40	NVHS_SLVS_RX5_N	NVHS0_SLVS_RX5_N	PCIe IF 5 Lane 5 Receive –	Input	B40	GND			
A41	GND	–	Ground	Ground	B41	NVHS_PEX0_TX6_P	NVHS0_TX6_P	PCIe IF 5 Lane 6 Transmit +	Output
A42	GND				B42	NVHS_PEX0_TX6_N	NVHS0_TX6_N	PCIe IF 5 Lane 6 Transmit –	Output
A43	NVHS_SLVS_RX6_P	NVHS0_SLVS_RX6_P	PCIe IF 5 Lane 6 Receive +	Input	B43	GND	–	Ground	Ground
A44	NVHS_SLVS_RX6_N	NVHS0_SLVS_RX6_N	PCIe IF 5 Lane 6 Receive –	Input	B44	GND			
A45	GND	–	Ground	Ground	B45	NVHS_PEX0_TX7_P	NVHS0_TX7_P	PCIe IF 5 Lane 7 Transmit +	Output
A46	GND				B46	NVHS_PEX0_TX7_N	NVHS0_TX7_N	PCIe IF 5 Lane 7 Transmit –	Output
A47	NVHS_SLVS_RX7_P	NVHS0_SLVS_RX7_P	PCIe IF 5 Lane 7 Receive +	Input	B47	GND	–	Ground	Ground
A48	NVHS_SLVS_RX7_N	NVHS0_SLVS_RX7_N	PCIe IF 5 Lane 7 Receive –	Input	B48	GND			
A49	GND	–	Ground	Ground	B49	GND			

Legend

Ground	Power	Reserved

Notes:

- Table shows only the PCIe x8 section of the connector since this is the only portion used. The connection figure shows the rest of the x16 connections.
- In the Type/Dir column, Output is to the PCIe Connector. Input is from the PCIe Connector. Bidir is for Bidirectional signals.

Table 7. PCIe Related Jetson Xavier Carrier PCB Trace Delays

Jetson Xavier Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for PCI Board (ps)	
		Stripline	Microstrip	Stripline	Microstrip
NVHS0_TX0_N	681.86	1602	1350	920.14	668.14
NVHS0_TX0_P	682.56	1602	1350	919.44	667.44
NVHS0_TX1_N	669.77	1602	1350	932.23	680.23
NVHS0_TX1_P	669.25	1602	1350	932.75	680.75
NVHS0_TX2_N	619.30	1602	1350	982.7	730.7
NVHS0_TX2_P	619.72	1602	1350	982.28	730.28
NVHS0_TX3_N	627.34	1602	1350	974.66	722.66
NVHS0_TX3_P	626.42	1602	1350	975.58	723.58
NVHS0_TX4_N	562.49	1602	1350	1039.51	787.51
NVHS0_TX4_P	561.70	1602	1350	1040.3	788.3
NVHS0_TX5_N	568.55	1602	1350	1033.45	781.45
NVHS0_TX5_P	568.35	1602	1350	1033.65	781.65
NVHS0_TX6_N	504.27	1602	1350	1097.73	845.73
NVHS0_TX6_P	503.48	1602	1350	1098.52	846.52
NVHS0_TX7_N	513.77	1602	1350	1088.23	836.23
NVHS0_TX7_P	514.52	1602	1350	1087.48	835.48
NVHS_SLVS_RX0_N	577.25	1602	1350	1024.75	772.75
NVHS_SLVS_RX0_P	578.10	1602	1350	1023.9	771.9
NVHS_SLVS_RX1_N	539.84	1602	1350	1062.16	810.16
NVHS_SLVS_RX1_P	540.22	1602	1350	1061.78	809.78
NVHS_SLVS_RX2_N	541.04	1602	1350	1060.96	808.96
NVHS_SLVS_RX2_P	540.97	1602	1350	1061.03	809.03
NVHS_SLVS_RX3_N	479.00	1602	1350	1123	871
NVHS_SLVS_RX3_P	479.85	1602	1350	1122.15	870.15
NVHS_SLVS_RX4_N	494.78	1602	1350	1107.22	855.22
NVHS_SLVS_RX4_P	495.67	1602	1350	1106.33	854.33
NVHS_SLVS_RX5_N	485.98	1602	1350	1116.02	864.02
NVHS_SLVS_RX5_P	485.65	1602	1350	1116.35	864.35
NVHS_SLVS_RX6_N	485.14	1602	1350	1116.86	864.86
NVHS_SLVS_RX6_P	485.46	1602	1350	1116.54	864.54
NVHS_SLVS_RX7_N	427.76	1602	1350	1174.24	922.24
NVHS_SLVS_RX7_P	427.99	1602	1350	1174.01	922.01
PCIE_REFCLK_N	783.45	1602	1350	818.55	566.55
PCIE_REFCLK_P	783.37	1602	1350	818.63	566.63

2.5 UFS / Micro SD Card Socket

A Combo UFS / Micro SD Card Socket (J4) is implemented, supporting up to SDR104 mode (UHS-1).

Figure 7. UFS / SD Card Connections

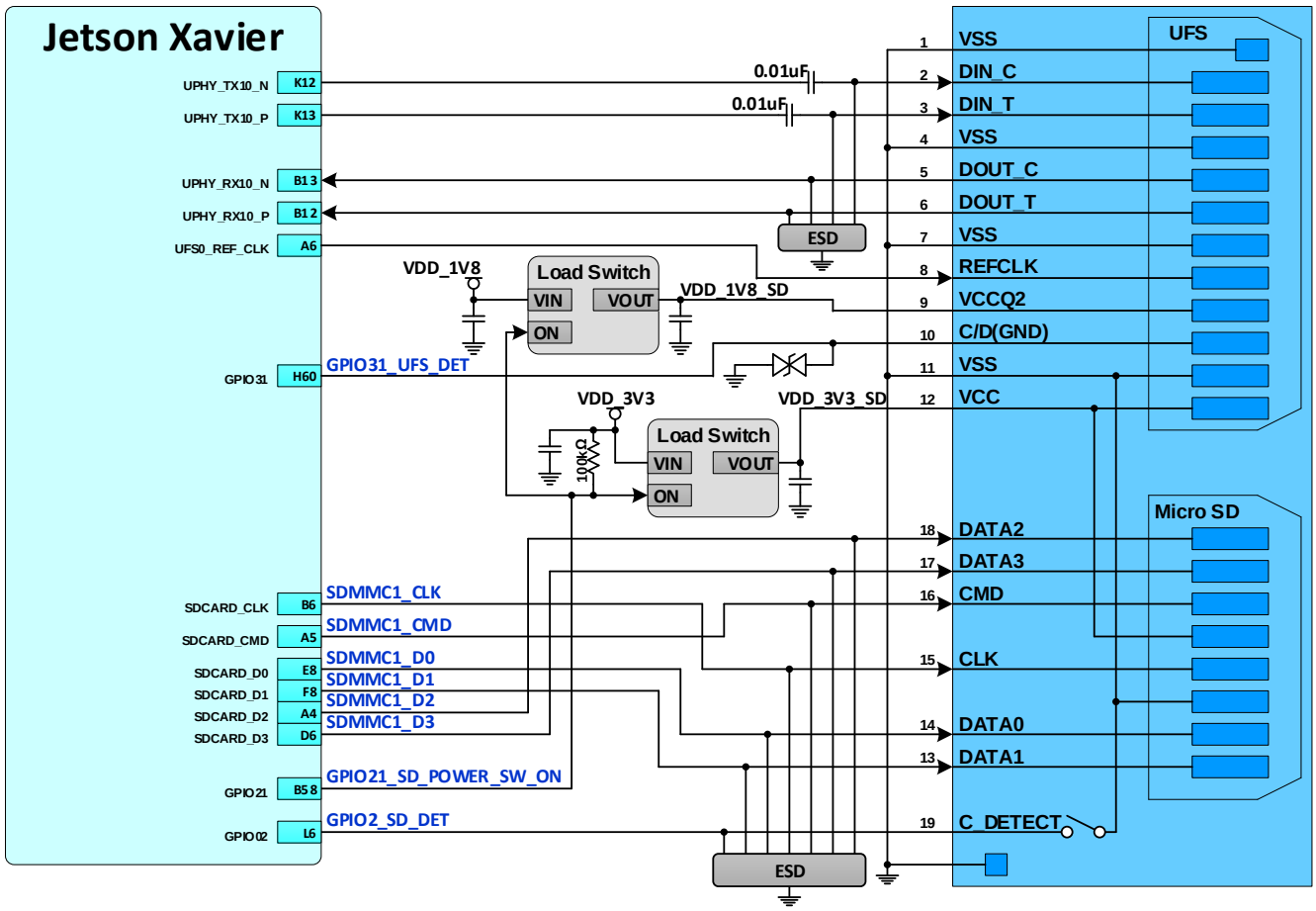


Table 8. UFS / SD Card Combo Socket Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
1	GND	–	Ground	Ground
2	UPHY_TX10_N	UPHY_TX10_N	UFS Transmit –	Output
3	UPHY_TX10_P	UPHY_TX10_P	UFS Transmit +	Output
4	GND	–	Ground	Ground
5	UPHY_RX10_N	UPHY_RX10_N	UFS Receive –	Input
6	UPHY_RX10_P	UPHY_RX10_P	UFS Receive +	Input
7	GND	–	Ground	Ground
8	UFS0_REF_CLK	UFS0_REF_CLK	UFS Reference Clock	Output
9	VDD_1V8_SD	–	1.8V Power for UFS	Power
10	GPIO31_UFS_DET	GPIO31	UFS Card Detect	Input
11	GND			
12	VDD_3V3_SD	–	3.3V Power for UFS & SD	Power
13	SDMMC_D1	SDCARD_D1	SD Card Data #1	Bidir
14	SDMMC_D0	SDCARD_D0	SD Card Data #0	Bidir
15	SDMMC_CLK	SDCARD_CLK	SD Card Clock	Output
16	SDMMC_CMD	SDCARD_CMD	SD Card Command	Bidir
17	SDMMC_D3	SDCARD_D3	SD Card Data #3	Bidir
18	SDMMC_D2	SDCARD_D2	SD Card Data #2	Bidir
19	GPIO2_SD_DET	GPIO02	SD Card, Card Detect	Input

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to Card Socket. Input is from Card Socket. Bidir is for Bidirectional signals.

2.6 eSATA / USB 3.1 Type A Connector

The Jetson Xavier carrier board has a hybrid connector supporting eSATA, USB 3.1 Gen 1 (J507) as shown below.

Figure 8. eSATA Connections

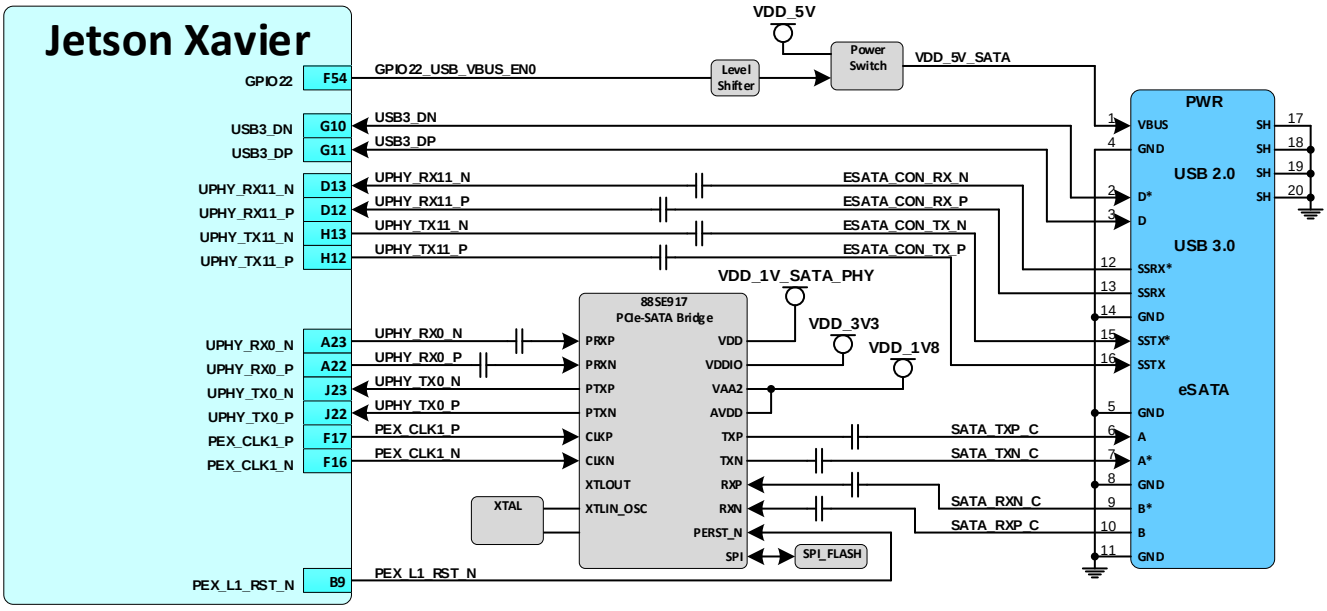


Table 9. Hybrid USB 3.1 Gen 1 & eSATA Connector Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir
1	VBUS	–			11	GND	–	Ground	Ground
2	USB3_DN	USB3_DN	USB 2.0 #3–	Bidir	12	ESATA_CON_RX_N	UPHY_RX11_N	USB 3.1 Receive–	Input
3	USB3_DP	USB3_DP	USB 2.0 #3+	Bidir	13	ESATA_CON_RX_P	UPHY_RX11_P	USB 3.1 Receive+	Input
4	GND	–	Ground	Ground	14	GND	–	Ground	Ground
5	GND				15	ESATA_CON_TX_N	UPHY_TX11_N	USB 3.1 Transmit–	Output
6	SATA_TXP_C	–	SATA Transmit+	Output	16	ESATA_CON_TX_P	UPHY_TX11_P	USB 3.1 Transmit+	Output
7	SATA_TXN_C	–	SATA Transmit–	Output	17	GND	–	Ground	Ground
8	GND	–	Ground	Ground	18	GND			
9	SATA_RXN_C	–	SATA Receive–	Input	19	GND			
10	SATA_RXP_C	–	SATA Receive+	Input	20	GND			

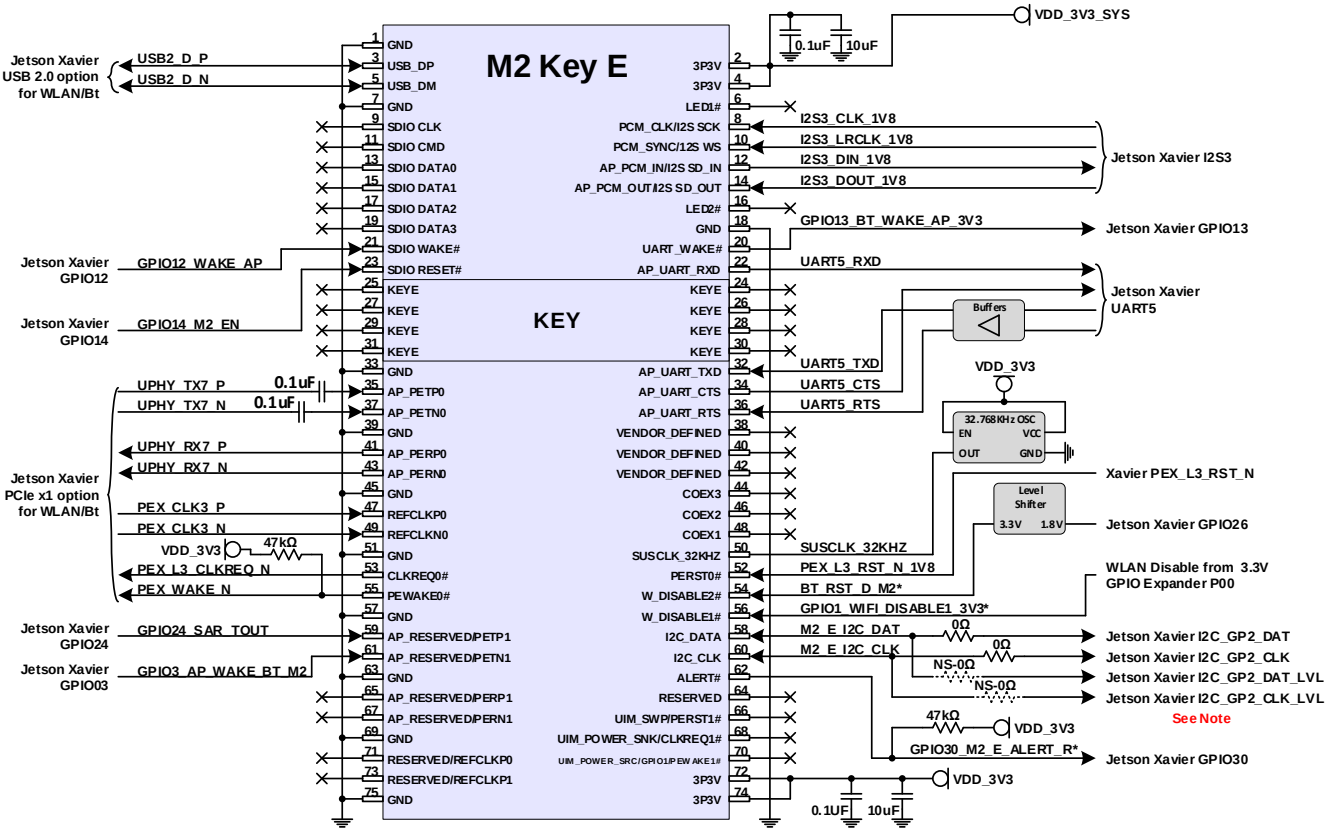
Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to Connector. Input is from Connector. Bidir is for Bidirectional signals.

2.7 M.2, Key E Expansion Slot

The Jetson carrier board includes a M.2, Key E Slot Mini-PCIe Expansion slot (J505). This includes interface options for WLAN/BT including PCIe (x1), USB 2.0, UART, I2S & I2C. The connections & power rails associated with the connector are shown in the figure below.

Figure 9. M.2 Key E Connections



Note: The I2C IF on pins 58 & 60 come by default directly from the Jetson I2C_GP0 (1.8V signaling). Stuffing resistors can be changed to bring the I2C interface after a level shifter (3.3V signaling). For earlier versions of the M.2 Key E revision spec. (prior to revision 1.1), the I2C interface used 3.3V signaling levels. The 1.1 revision changes this to 1.8V signaling levels.

Table 10. M.2, Key E Expansion Slot Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
1	GND	–	Ground	Ground		–	–	–	–
3	USB2_D_P	USB2_D+	USB 2.0 Data +	Bidir	2	VDD_3V3	–	Main 3.3V Supply	Power
5	USB2_D_N	USB2_D–	USB 2.0 Data -	Bidir	4	VDD_3V3			
7	GND	–	Ground	Ground	6	NC	–	Unused	Unused
9	NC	–	Unused	Unused	8	I2S3_CLK	I2S3_CLK	I2S #3 Clock	Bidir
11	NC				10	I2S3_LRCLK	I2S3_LRCLK	I2S #3 Left/Right Clock	Bidir
13	NC				12	I2S3_SDIN	I2S3_SDIN	I2S #3 Data In	Input
15	NC				14	I2S3_SDOUT	I2S3_SDOUT	I2S #3 Data Out	Bidir
17	NC				16	NC	–	Unused	Unused
19	NC				18	GND	–	Ground	Ground
21	GPIO12_M2_ WAKE_AP	GPIO12	WLAN Wake AP	Input	20	GPIO13_BT_WAKE_ AP_3V3	GPIO13	Bluetooth Wake AP	Input
23	GPIO14_M2_EN	GPIO14	WLAN Enable	Output	22	UART5_RXD	UART5_RX	UART #5 Receive	Input
25	NC (Key)	–	Unused	Unused	24	NC (Key)	–	Unused	Unused
27	NC (Key)				26	NC (Key)			
29	NC (Key)				28	NC (Key)			
31	NC (Key)				30	NC (Key)			
33	GND	–	Ground	Ground	32	UART5_TXD	UART5_TX	UART #5 Transmit	Output
35	UPHY_TX_P0_M2	UPHY_TX7_P	PCIe IF #3 Transmit +	Output	34	UART5_CTS	UART5_CTS#	UART #5 Clear to Send	Input
37	UPHY_TX_N0_M2	UPHY_TX7_N	PCIe IF #3 Transmit -	Output	36	UART5_RTS	UART5_RTS#	UART #5 Request to Send	Output
39	GND	–	Ground	Ground	38	GPIO3_AP_WAKE_ BT_M2	GPIO03	AP Wake BT	Output
41	UPHY_RX7_P	UPHY_RX7_P	PCIe IF #3 Receive +	Input	40	NC	–	Unused	Unused
43	UPHY_RX7_N	UPHY_RX7_N	PCIe IF #3 Receive -	Input	42	NC			
45	GND	–	Ground	Ground	44	NC			
47	PEX_CLK3_P	PEX_CLK3_P	PCIe IF #3 Reference clock +	Output	46	NC			
49	PEX_CLK3_N	PEX_CLK3_N	PCIe IF #3 Reference clock -	Output	48	NC			
51	GND	–	Ground	Ground	50	SUSCLK_32KHZ	–	Suspend Clock (32KHz)	Output
53	PEX_L3_CLKREQ_N	PEX_L3_CLKREQ_N	PCIe IF #3 Clock Request	Bidir	52	PEX_L3_RST_N_1V8	PEX_L3_RST_N	PCIe IF #3 Reset	Output
55	PEX_WAKE_N	PEX_WAKE_N	PCIe Wake	Input	54	BT_RST_D_M2*	GPIO26	WLAN Disable #2 (Level Shifted to 3.3V)	Output
57	GND	–	Ground	Ground	56	GPIO1_WIFI_ DISABLE_3V3*	GPIO01	WLAN Disable #1 (Level Shifted to 3.3V)	Output
59	GPIO24_SAR_TOUT	GPIO24	RF Power Control or GPIO	Output	58	I2C_GP2_SDA(_LVS)	I2C_GP2_DAT	General I2C Interface #2 Data. See note.	Bidir/OD
61	GPIO3_AP_WAKE_ BT_M2	GPIO03	AP Wake BT	Output	60	I2C_GP2_SCL(_LVS)	I2C_GP2_CLK	General I2C Interface #2 Clock. See note.	Bidir/OD
63	GND	–	Ground	Ground	62	M2_E_ALERT_L	GPIO30	M.2, Key E Connector Alert	Input
65	NC	–	Unused	Unused	64	NC	–	Unused	Unused
67	NC				66	NC			
69	GND	–	Ground	Ground	68	NC			
71	NC	–	Unused	Unused	70	NC			
73	NC				72	VDD_3V3	–	Main 3.3V Supply	Power
75	GND	–	Ground	Ground	74	VDD_3V3			

Legend

Ground	Power	Reserved

Notes:
- In the Type/Dir column, Output is to M.2 Module. Input is from M.2 Module. Bidir is for Bidirectional signals.
- Prior to the M.2 Key E revision 1.1 spec., the I2C interface was referenced to 3.3V. The 1.1 revision changes this to 1.8V. By default, the carrier board connects these pins to the 1.8V level I2C interface. Stuffing resistors can be changed to connect to the I2C interface through level shifters for 3.3V operation instead.

Table 11. M.2 Key E Related Carrier Board PCB Trace Delays

Jetson Xavier Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for M.2 Module (ps)		Jetson Xavier Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for M.2 Module (ps)	
PCIe					**USB**		**SL**	**MS**	**SL**	**MS**
UPHY_RX7_N	419.41	880	460.59		USB2_DN	372.08	1050	900	677.92	527.92
UPHY_RX7_P	419.93	880	460.07		USB2_DP	371.56	1050	900	678.44	528.44
UPHY_TX7_N	517.03	880	362.97		**I2S**					
UPHY_TX7_P	516.98	880	363.02		I2S3_DIN	554.29	3600		3045.71	
PEX_CLK3_N	433.73	880	446.27		I2S3_DOUT	561.35	3600		3038.65	
PEX_CLK3_P	433.23	880	446.77		I2S3_FS	511.16	3600		3088.84	
					I2S3_SCLK	508.20	3600		3091.80	

Notes: For USB 2.0 max length allowed, the case w/Common-Mode-Choke (CMC) is assumed. Longer length possible wo/CMC.

2.8 M.2, Key M Expansion Slot

The carrier board includes an M.2, Key M Slot NVMe Expansion slot (J1). This includes PCIe (x4) & I2C. The connections & power rails associated with the connector are shown in the figure below.

Figure 10. M.2 Key M Connections

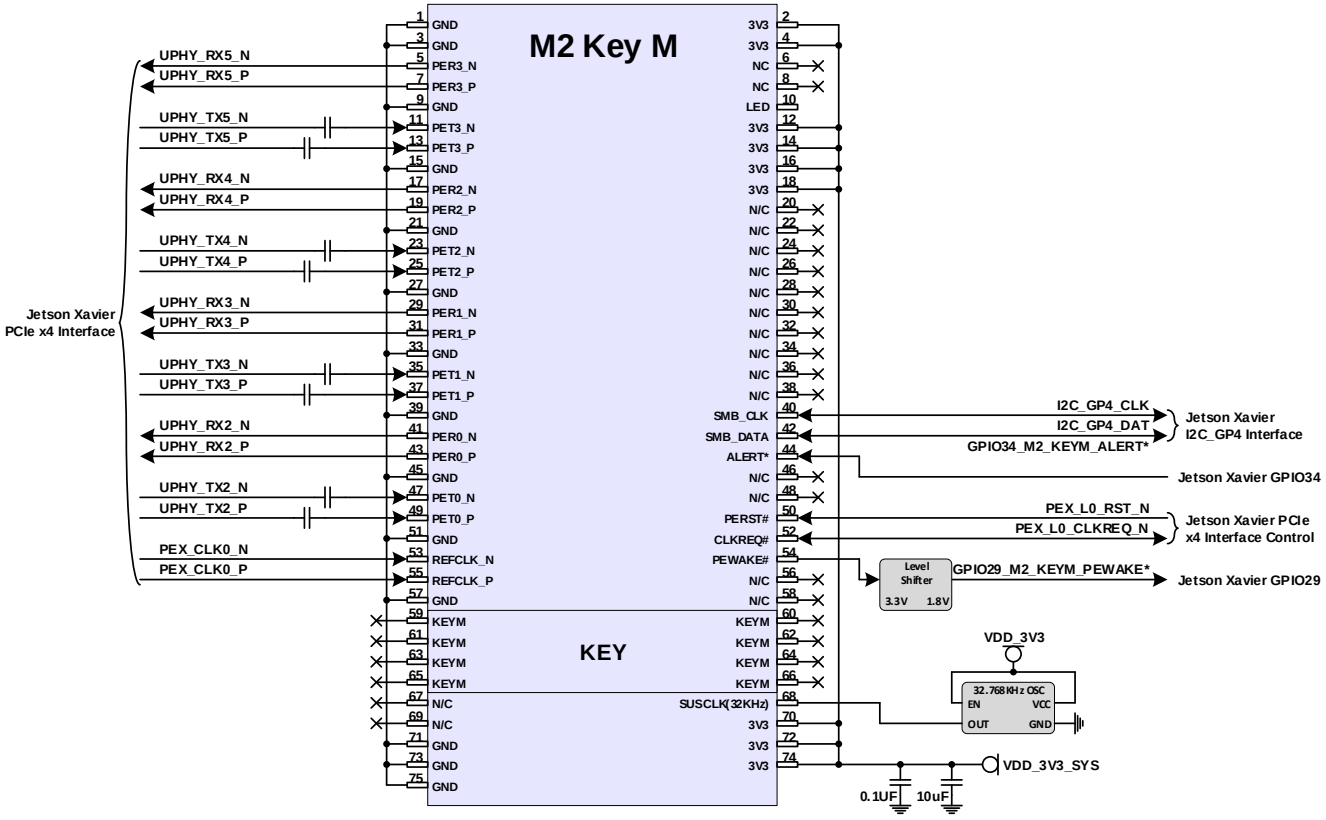


Table 12. M.2, Key M Expansion Slot Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
1	GND	–	Ground	Ground	2	VDD_3V3	–	Main 3.3V Supply	Power
3	GND				4	VDD_3V3			
5	UPHY_RX5_N	UPHY_RX5_N	PCIe IF #0 Lane 5 Receive–	Input	6	NC	–	Unused	Unused
7	UPHY_RX5_P	UPHY_RX5_P	PCIe IF #0 Lane 5 Receive+	Input	8	NC			
9	GND	–	Ground	Ground	10	NC			
11	UPHY_TX_N5_M2	UPHY_TX5_N	PCIe IF #0 Lane 5 Transmit–	Output	12	VDD_3V3	–	Main 3.3V Supply	Power
13	UPHY_TX_P5_M2	UPHY_TX5_P	PCIe IF #0 Lane 5 Transmit+	Output	14	VDD_3V3			
15	GND	–	Ground	Ground	16	VDD_3V3			
17	UPHY_RX4_N	UPHY_RX4_N	PCIe IF #0 Lane 4 Receive–	Input	18	VDD_3V3			
19	UPHY_RX4_P	UPHY_RX4_P	PCIe IF #0 Lane 4 Receive+	Input	20	NC	–	Unused	Unused
21	GND	–	Ground	Ground	22	NC			
23	UPHY_TX_N4_M2	UPHY_TX4_N	PCIe IF #0 Lane 4 Transmit–	Output	24	NC			
25	UPHY_TX_P4_M2	UPHY_TX4_P	PCIe IF #0 Lane 4 Transmit+	Output	26	NC			
27	GND	–	Ground	Ground	28	NC			
29	UPHY_RX3_N	UPHY_RX3_N	PCIe IF #0 Lane 3 Receive–	Input	30	NC			
31	UPHY_RX3_P	UPHY_RX3_P	PCIe IF #0 Lane 3 Receive+	Input	32	NC			
33	GND	–	Ground	Ground	34	NC			
35	UPHY_TX_N3_M2	UPHY_TX3_N	PCIe IF #0 Lane 3 Transmit–	Output	36	NC			
37	UPHY_TX_P3_M2	UPHY_TX3_P	PCIe IF #0 Lane 3 Transmit+	Output	38	NC			
39	GND	–	Ground	Ground	40	I2C_GP4_CLK	I2C_GP4_CLK	General I2C #4 Clock	bidir
41	UPHY_RX2_N	UPHY_RX2_N	PCIe IF #0 Lane 2 Receive–	Input	42	I2C_GP4_DAT	I2C_GP4_DAT	General I2C #4 Data	bidir
43	UPHY_RX2_P	UPHY_RX2_P	PCIe IF #0 Lane 2 Receive+	Input	44	GPIO34_M2_KEYM_ ALERT*	GPIO34	M.2 Key M Alert	Output
45	GND	–	Ground	Ground	46	NC	–	Unused	Unused
47	UPHY_TX_N2_M2	UPHY_TX2_N	PCIe IF #0 Lane 2 Transmit–	Output	48	NC			
49	UPHY_TX_P2_M2	UPHY_TX2_P	PCIe IF #0 Lane 2 Transmit+	Output	50	PEX_L0_RST_N	PEX_L0_RST_N	PCIe IF #0 Reset	Output
51	GND	–	Ground	Ground	52	PEX_L0_CLKREQ_N	PEX_L0_CLKREQ_N	PCIe IF #0 Clock Request	Input
53	PEX_CLK0_N	PEX_CLK0_N	PCIe IF #0 Reference Clock–	Output	54	M2_KEYM_ PEWAKE_3V3*	PEX_WAKE_N	PCIe Wake (Level Shifted from 3.3V to 1.8V)	Input
55	PEX_CLK0_P	PEX_CLK0_P	PCIe IF #0 Reference Clock+	Output	56	NC	–	Unused	Unused
57	GND	–	Ground	Ground	58	NC			
59	NC (Key)	–	Unused	Unused	60	NC (Key)	–	Unused	Unused
61	NC (Key)				62	NC (Key)			
63	NC (Key)				64	NC (Key)			
65	NC (Key)				66	NC (Key)			
67	NC	–	Unused	Unused	68	SUSCLK_32KHZ_ NVME	–	32KHz Suspend Clock	Output
69	NC				70	VDD_3V3	–	Main 3.3V Supply	Power
71	GND	–	Ground	Ground	72	VDD_3V3			
73	GND				74	VDD_3V3			
75	GND								

Legend

Ground	Power	Reserved

Notes: - In the Type/Dir column, Output is to M.2 Module. Input is from M.2 Module. Bidir is for Bidirectional signals.

Table 13. M.2 Key M Related Carrier Board PCB Trace Delays (PCIe up to GEN3)

Jetson Xavier Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for PCI Board (ps)		Jetson Xavier Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for PCI Board (ps)
UPHY_RX2_N	318.73	880	561.27		UPHY_TX2_N	362.21	880	517.79
UPHY_RX2_P	319.51	880	560.49		UPHY_TX2_P	362.63	880	517.37
UPHY_RX3_N	349.10	880	530.90		UPHY_TX3_N	388.76	880	491.24
UPHY_RX3_P	348.44	880	531.56		UPHY_TX3_P	388.81	880	491.19
UPHY_RX4_N	314.37	880	565.63		UPHY_TX4_N	397.00	880	483.00
UPHY_RX4_P	313.73	880	566.27		UPHY_TX4_P	396.15	880	483.85
UPHY_RX5_N	367.24	880	512.76		UPHY_TX5_N	398.34	880	481.66
UPHY_RX5_P	367.66	880	512.34		UPHY_TX5_P	397.45	880	482.55
PEX_CLK0_N	299.38	880	580.62					
PEX_CLK0_P	298.78	880	581.22					

2.9 Audio Panel Header

The Jetson carrier board includes a 10-pin (2x5, 2.54mm pitch) Audio Panel Header (J511). This can be used to connect to a standard PC audio panel to support connections to Microphone, Line-in, Headphones, Powered Speakers, etc.

Figure 11. Audio Panel Header Connections

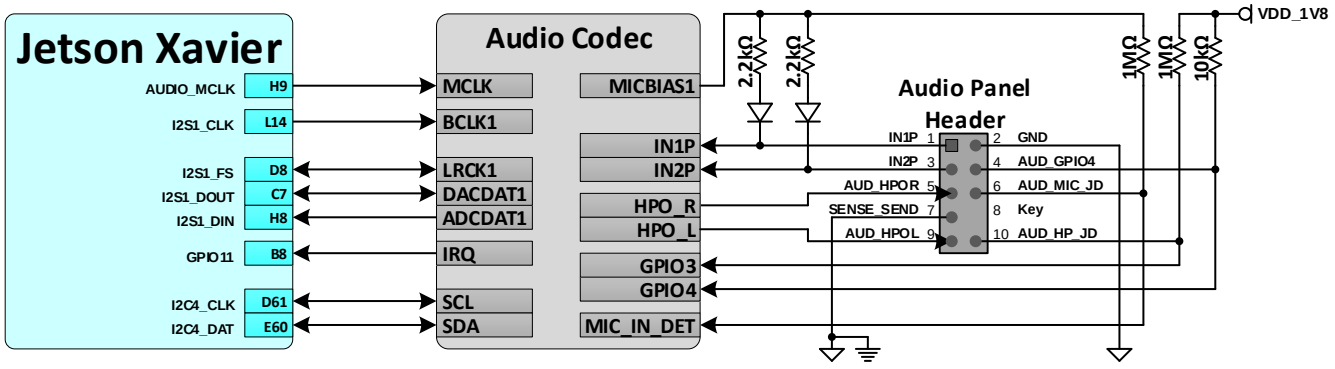


Table 14. Audio Panel Header Descriptions

Pin #	Signal Name	Audio CODEC Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Audio CODEC Pin Name	Usage/Description	Type/Dir Default
1	IN1P	IN1P	Microphone #1 input	Output	2	GND	–	Ground	Ground
3	IN2P	IN2P	Microphone #2 input	Output	4	AUD_GPIO4	GPIO4	Presense – detects if audio dongle is connected to header.	Input
5	AUD_HPOR	HPO_R	Headphone output Right channel	Input	6	AUD_MIC_JD	MIC_IN_DET	Jack/Microphone detect pin	Input
7	SENSE_SEND	NA	Pulled to Analog GND	NA	8	Key	NA	NA	NA
9	AUD_HPOL	HPO_L	Headphone output Left channel	Input	10	AUD_HP_JD	GPIO3	Headphone or Jack detection	Input

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to Audio Panel Header. Input is from Audio Panel Header. Bidir is for Bidirectional signals.

2.10 JTAG Header

The Jetson carrier board has a 10-pin (2x5, 1.27mm pitch) JTAG header (J502).

Figure 12. JTAG Header Connections

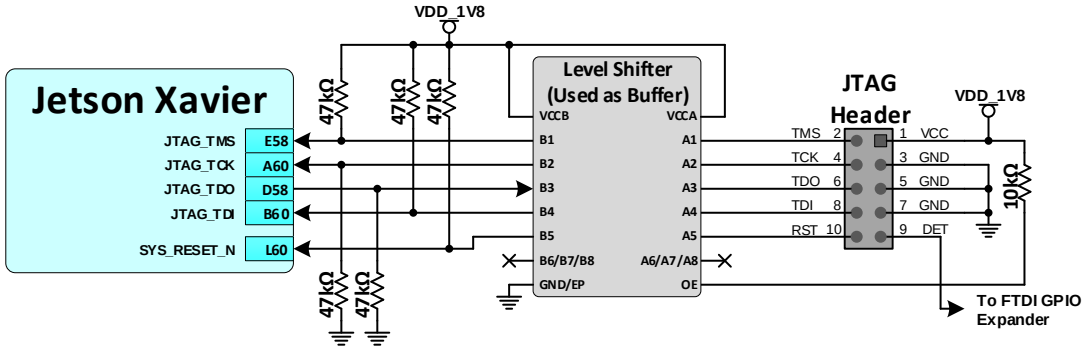


Table 15. JTAG Header Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
2	JTAG_AP_TMS	JTAG_TMS	JTAG Test Mode Select	Input	1	VDD_1V8	–	Main 1.8V Supply	Power
4	JTAG_AP_TCK	JTAG_TCK	JTAG Test Clock	Input	3	GND	–	Ground	Ground
6	JTAG_AP_TDO	JTAG_TDO	JTAG Test Data Out	Output	5	GND			
8	JTAG_AP_TDI	JTAG_TDI	JTAG Test Data In	Input	7	GND			
10	SYS_RST_IN*	SYS_RESET_N	Main carrier board reset	Input	9	J502_DET	–	Detect presence of JTAG debugger connection.	Input

Legend

Ground	Power	Reserved

Notes: In the Type/Dir column, Output is to JTAG header. Input is from JTAG header. Bidir is for Bidirectional signals.

3.0 CARRIER BOARD CUSTOM EXPANSION CONNECTIONS

The Jetson carrier board supports several custom expansion headers:

- Jetson Xavier Connector, 65x11
- Camera Expansion Header, 2x60, 0.5mm pitch
- Expansion Header, 2x20, 2.54mm pitch
- Audio Panel Header, 2x5, 2.54mm pitch
- Fan Header, 4-pin, 1.25mm pitch
- DC Power Jack

The Routing Guidelines for the interfaces supported on the expansion connectors can be found in the Jetson Xavier OEM Product Design Guide. Those guidelines cover the PCB routing from the Jetson Xavier to the peripheral device or actual device connector. When designing modules for one of the Jetson Xavier expansion connectors, the routing on the carrier board must be accounted for. Tables are provided for the critical interfaces that provide the PCB delays on the carrier board. These delays are subtracted from the delays allowed in the Jetson Xavier OEM Product Design Guide routing guidelines. The tables also include the max trace guidelines and remaining max trace delay allowed on the peripheral modules. See the Jetson Xavier OEM Product Design Guide for other requirements (Impedance, trace spacing, skews between signals, etc.).

3.1 Module Connector

The carrier board interfaces to Jetson Xavier using a 699-pin (65x11) connector (J3). The part number for the connector used on the carrier board can be found in the Jetson Xavier Supported Component List (SCL) document. This interfaces with the module. See the Jetson Xavier Module Data Sheet for the connector used on the module. The connector pinout can be found in the Jetson Xavier OEM Product Design Guide.

3.2 Camera Expansion Header

The Jetson Xavier carrier board includes a 120-pin (2x60, 0.5mm pitch) Camera Expansion Connector (J509). The connector used on the carrier board is a Samtec QSH-060-01-H-D-A. The mating connector is a Samtec QTH-060-01-H-D-A. The expansion connector includes interface options for multiple cameras as well as some for audio (I2S & DMIC):

- CSI up to 6x2 lane
- CAM_I2C, Clock & Control GPIOs for the Cameras
- I2C

Table 16. Camera Expansion Connector Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
1	CSI_0_D0_P	CSI0_D0_P	CSI 0 Data 0+	Input	2	CSI1_D0_P	CSI1_D0_P	CSI 1 Data 0+	Input
3	CSI_0_D0_N	CSI0_D0_N	CSI 0 Data 0-	Input	4	CSI1_D0_N	CSI1_D0_N	CSI 1 Data 0-	Input
5	GND	–	Ground	Ground	6	GND	–	Ground	Ground
7	CSI_0_D0_P	CSI0_D0_P	CSI 0 Clock+	Input	8	CSI1_CLK_P	CSI1_CLK_P	CSI 1 Clock+	Input
9	CSI_0_D0_N	CSI0_D0_N	CSI 0 Clock-	Input	10	CSI1_CLK_N	CSI1_CLK_N	CSI 1 Clock-	Input
11	GND	–	Ground	Ground	12	GND	–	Ground	Ground
13	CSI0_D1_P	CSI0_D1_P	CSI 0 Data 1+	Input	14	CSI1_D1_P	CSI1_D1_P	CSI 1 Data 1+	Input
15	CSI0_D1_N	CSI0_D1_N	CSI 0 Data 1-	Input	16	CSI1_D1_N	CSI1_D1_N	CSI 1 Data 1-	Input
17	GND	–	Ground	Ground	18	GND	–	Ground	Ground
19	CSI2_D0_P	CSI2_D0_P	CSI 2 Data 0+	Input	20	CSI3_D0_P	CSI3_D0_P	CSI 3 Data 0+	Input
21	CSI2_D0_N	CSI2_D0_N	CSI 2 Data 0-	Input	22	CSI3_D0_N	CSI3_D0_N	CSI 3 Data 0-	Input
23	GND	–	Ground	Ground	24	GND	–	Ground	Ground
25	CSI2_CLK_P	CSI2_CLK_P	CSI 2 Clock+	Input	26	CSI3_CLK_P	CSI3_CLK_P	CSI 3 Clock+	Input
27	CSI2_CLK_N	CSI2_CLK_N	CSI 2 Clock-	Input	28	CSI3_CLK_N	CSI3_CLK_N	CSI 3 Clock-	Input
29	GND	–	Ground	Ground	30	GND	–	Ground	Ground
31	CSI2_D1_P	CSI2_D1_P	CSI 2 Data 1+	Input	32	CSI3_D1_P	CSI3_D1_P	CSI 3 Data 1+	Input
33	CSI2_D1_N	CSI2_D1_N	CSI 2 Data 1-	Input	34	CSI3_D1_N	CSI3_D1_N	CSI 3 Data 1-	Input
35	GND	–	Ground	Ground	36	GND	–	Ground	Ground
37	CSI4_D0_P	CSI4_D0_P	CSI 4 Data 0+	Input	38	CSI6_D0_P	CSI6_D0_P	CSI 6 Data 0+	Input

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
39	CSI4_D0_N	CSI4_D0_N	CSI 4 Data 0-	Input	40	CSI6_D0_N	CSI6_D0_N	CSI 6 Data 0-	Input
41	GND	–	Ground	Ground	42	GND	–	Ground	Ground
43	CSI4_CLK_P	CSI4_CLK_P	CSI 4 Clock+	Input	44	CSI6_CLK_P	CSI6_CLK_P	CSI 6 Clock+	Input
45	CSI4_CLK_N	CSI4_CLK_N	CSI 4 Clock-	Input	46	CSI6_CLK_N	CSI6_CLK_N	CSI 6 Clock-	Input
47	GND	–	Ground	Ground	48	GND	–	Ground	Ground
49	CSI4_D1_P	CSI4_D1_P	CSI 4 Data 1+	Input	50	CSI6_D1_P	CSI6_D1_P	CSI 6 Data 1+	Input
51	CSI4_D1_N	CSI4_D1_N	CSI 4 Data 1-	Input	52	CSI6_D1_N	CSI6_D1_N	CSI 6 Data 1-	Input
53	GND	–	Ground	Ground	54	GND	–	Ground	Ground
55	DVDD_CAM_LV	–	Reserved for Low Voltage Digital Supply	Power	56	DVDD_CAM_LV	–	Reserved for Low Voltage Digital Supply	Power
57	DVDD_CAM_LV				58	DVDD_CAM_LV			
59	CSI5_D0_P	CSI5_D0_P	CSI 5 Data 0+	Input	60	CSI7_D0_P	CSI7_D0_P	CSI 7 Data 0+	Input
61	CSI5_D0_N	CSI5_D0_N	CSI 5 Data 0-	Input	62	CSI7_D0_N	CSI7_D0_N	CSI 7 Data 0-	Input
63	GND	–	Ground	Ground	64	GND	–	Ground	Ground
65	CSI5_CLK_P	CSI5_CLK_P	CSI 5 Clock+	Input	66	CSI7_CLK_P	CSI7_CLK_P	CSI 7 Clock+	Input
67	CSI5_CLK_N	CSI5_CLK_N	CSI 5 Clock-	Input	68	CSI7_CLK_N	CSI7_CLK_N	CSI 7 Clock-	Input
69	GND	–	Ground	Ground	70	GND	–	Ground	Ground
71	CSI5_D1_P	CSI5_D1_P	CSI 5 Data 1+	Input	72	CSI7_D1_P	CSI7_D1_P	CSI 7 Data 1+	Input
73	CSI5_D1_N	CSI5_D1_N	CSI 5 Data 1-	Input	74	CSI7_D1_N	CSI7_D1_N	CSI 7 Data 1-	Input
75	I2C_GP3_CLK	I2C_GP3_CLK	Camera I2C clock	Bidir	76	NC	–	Unused	Unused
77	I2C_GP3_DAT	I2C_GP3_DAT	Camera I2C data	Bidir	78	NC			
79	GND	–	Ground	Ground	80	GND	–	Ground	Ground
81	AVDD_CAM	–	2.8V Camera supply (LDO)	Power	82	AVDD_CAM_2V8	–	2.8V Analog Camera supply	Power
83	AVDD_CAM				84	NC	–	Unused	Unused
85	NC	–	Unused	Unused	86	NC			
87	I2C_GP2_CLK	I2C_GP2_CLK	General Purpose I2C #2 Clock	Bidir/OD	88	CAM1_MCLK03	CAM1_MCLK03	Camera #1 Master Clock	Output
89	I2C_GP2_DAT	I2C_GP2_DAT	General Purpose I2C #2 Data	Bidir/OD	90	GPIO15_CAM1_PWDN	GPIO15	Camera #1 Powerdown	Output
91	CAM0_MCLK02	CAM0_MCLK02	Camera #0 Master Clock	Output	92	GPIO16_CAM1_RST	GPIO16	Camera #1 Reset	Output
93	CAM0_PWDN	UART4_CTS	Camera #0 Powerdown	Output	94	CAM2_MCLK04	CAM2_MCLK04	Camera #2 Master Clock	Output
95	CAM0_RST	UART4_TX	Camera #0 Reset	Output	96	NC	–	Unused	Unused
97	NC	–	Unused	Unused	98	NC			
99	GND	–	Ground	Ground	100	GND	–	Ground	Ground
101	DVDD_CAM_IO_1V2	–	1.2V digital Camera supply	Power	102	VDD_1V8	–	1.8V Camera supply.	Power
103	NC	–	Unused	Unused	104	NC	–	Unused	Unused
105	I2C_GP4_CLK	I2C_GP4_CLK	General I2C #4 Clock	Bidir/OD	106	NC			
107	I2C_GP4_DAT	I2C_GP4_DAT	General I2C #4 Data	Bidir/OD	108	VDD_3V3	–	3.3V supply	Power
109	NC	–	Unused	Unused	110	VDD_3V3			
111	NC				112	NC	–	Unused	Unused
113	NC				114	NC			
115	GND	–	Ground	Ground	116	GND	–	Ground	Ground
117	NC	–	Unused	Unused	118	VDD_3V3	–	3.3V supply	Power
119	GPIO25_VDD_SYS_EN	GPIO25	System power enable	Output	120	VDD_3V3			

Legend

Ground	Power	Reserved

Notes: In the Type/Dir column, Output is to Camera Module. Input is from Camera Module. Bidir is for Bidirectional signals.

Figure 13: Camera CSI Connections (C-PHY)

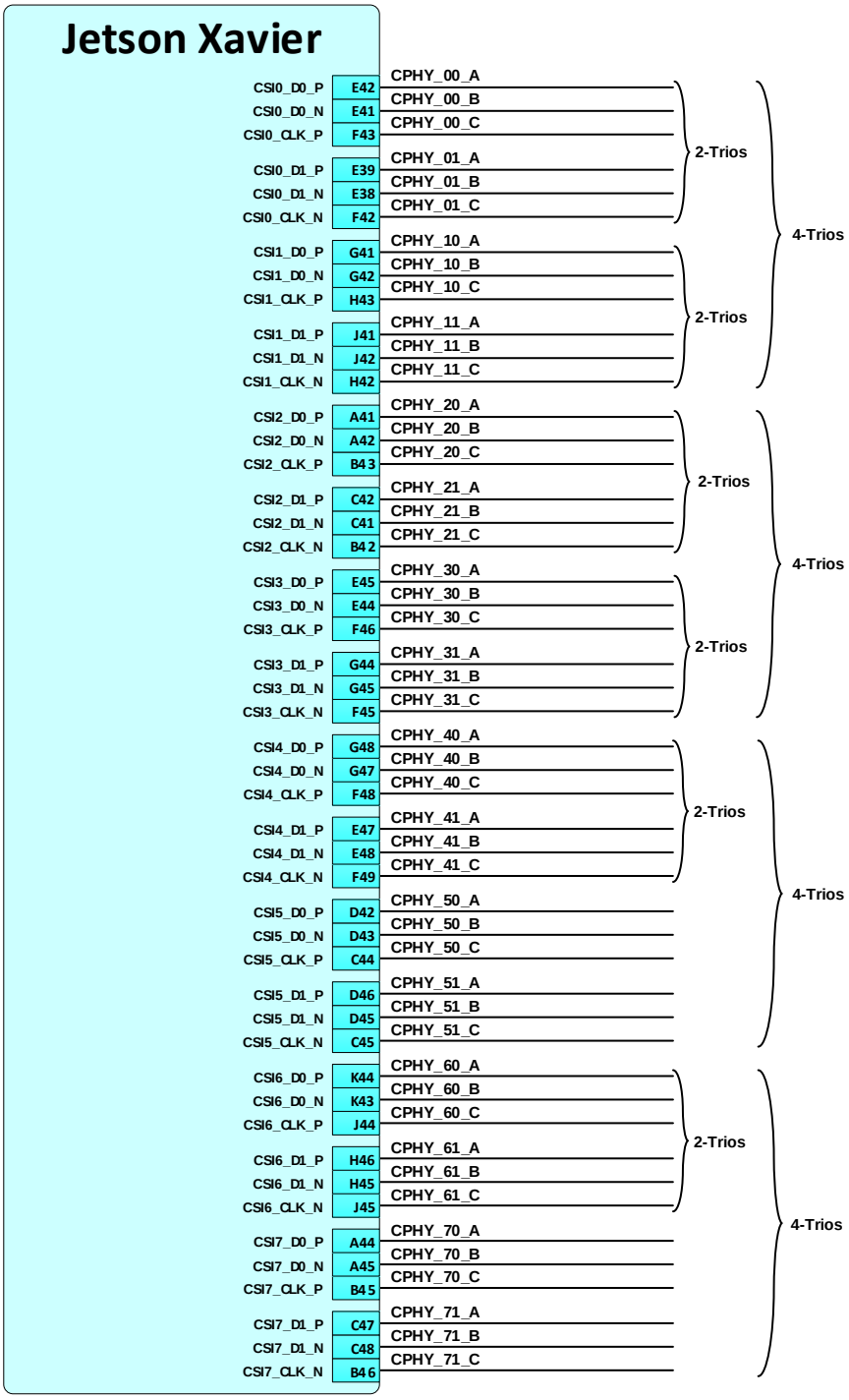
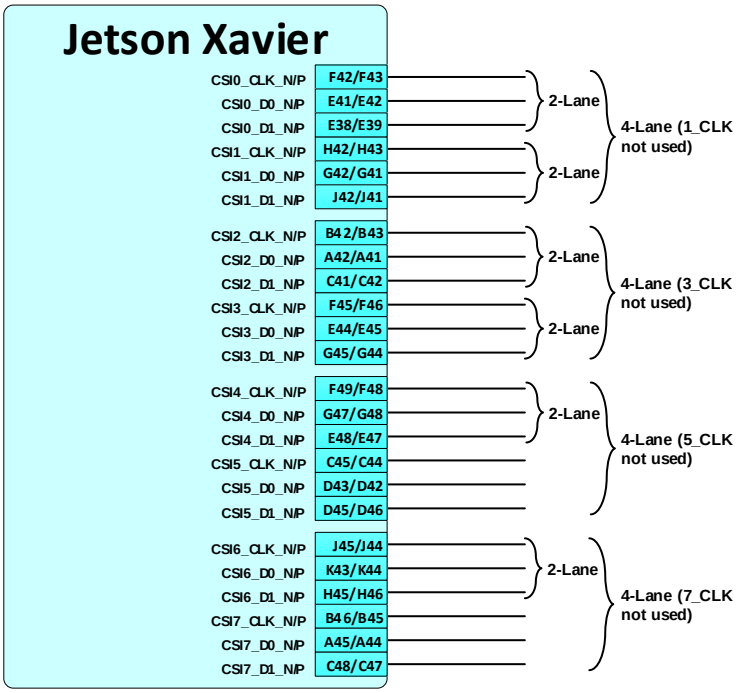


Figure 14: Camera CSI Connections (D-PHY)



See the Jetson Xavier OEM Product Design Guide for Routing Guidelines. Include the carrier board PCB trace delays in the following table when calculating max trace length & for skew matching.

Table 17. Camera Expansion Connector Related Carrier Board PCB Trace Delays (D-PHY only)

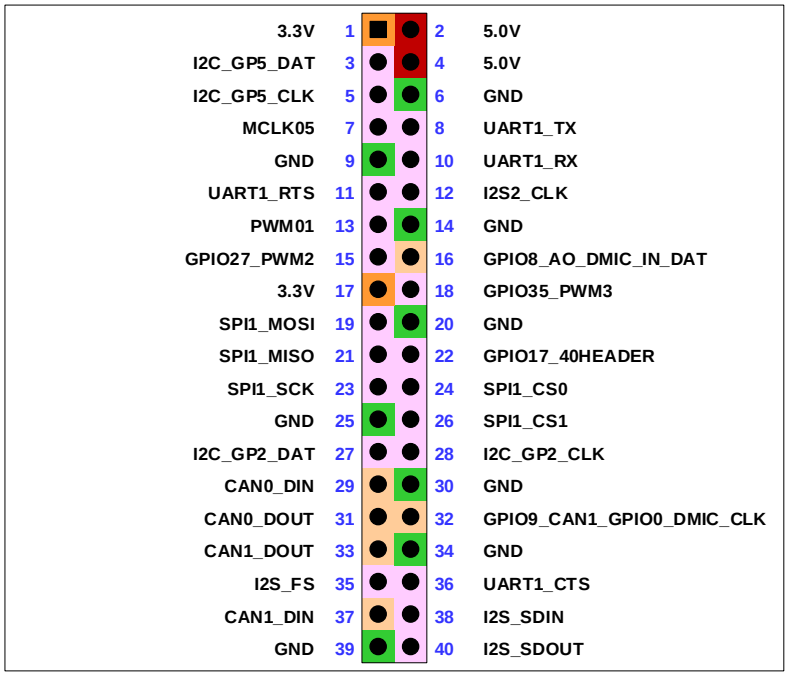
Jetson Xavier Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for Camera Module (ps)			Jetson Xavier Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for Camera Module (ps)	
		1Gbps	1.5Gbps	1Gbps	1.5Gbps				1Gbps	1.5Gbps	1Gbps	1.5Gbps
CSI_0_CLK_N	349.73	1100	800	750.27	450.27		CSI_4_CLK_N	242.98	1100	800	857.02	557.02
CSI_0_CLK_P	350.38	1100	800	749.62	449.62		CSI_4_CLK_P	242.49	1100	800	857.51	557.51
CSI_0_D0_N	352.56	1100	800	747.44	447.44		CSI_4_D0_N	245.51	1100	800	854.49	554.49
CSI_0_D0_P	353.30	1100	800	746.70	446.70		CSI_4_D0_P	246.49	1100	800	853.51	553.51
CSI_0_D1_N	346.33	1100	800	753.67	453.67		CSI_4_D1_N	241.41	1100	800	858.59	558.59
CSI_0_D1_P	346.84	1100	800	753.16	453.16		CSI_4_D1_P	241.46	1100	800	858.54	558.54
CSI_1_CLK_N	351.26	1100	800	748.74	448.74		CSI_5_CLK_N	233.20	1100	800	866.80	566.80
CSI_1_CLK_P	351.32	1100	800	748.68	448.68		CSI_5_CLK_P	234.03	1100	800	865.97	565.97
CSI_1_D0_N	350.70	1100	800	749.30	449.30		CSI_5_D0_N	234.52	1100	800	865.48	565.48
CSI_1_D0_P	350.02	1100	800	749.98	449.98		CSI_5_D0_P	234.62	1100	800	865.38	565.38
CSI_1_D1_N	357.20	1100	800	742.80	442.80		CSI_5_D1_N	234.55	1100	800	865.45	565.45
CSI_1_D1_P	357.20	1100	800	742.80	442.80		CSI_5_D1_P	233.91	1100	800	866.09	566.09
CSI_2_CLK_N	275.30	1100	800	824.70	524.70		CSI_6_CLK_N	271.92	1100	800	828.08	528.08
CSI_2_CLK_P	275.72	1100	800	824.28	524.28		CSI_6_CLK_P	271.82	1100	800	828.18	528.18
CSI_2_D0_N	275.17	1100	800	824.83	524.83		CSI_6_D0_N	276.35	1100	800	823.65	523.65
CSI_2_D0_P	274.47	1100	800	825.53	525.53		CSI_6_D0_P	277.12	1100	800	822.88	522.88
CSI_2_D1_N	269.56	1100	800	830.44	530.44		CSI_6_D1_N	275.54	1100	800	824.46	524.46
CSI_2_D1_P	270.10	1100	800	829.90	529.90		CSI_6_D1_P	276.30	1100	800	823.70	523.70
CSI_3_CLK_N	282.77	1100	800	817.23	517.23		CSI_7_CLK_N	262.58	1100	800	837.42	537.42
CSI_3_CLK_P	282.75	1100	800	817.25	517.25		CSI_7_CLK_P	263.07	1100	800	836.93	536.93
CSI_3_D0_N	284.73	1100	800	815.27	515.27		CSI_7_D0_N	262.84	1100	800	837.16	537.16
CSI_3_D0_P	285.66	1100	800	814.34	514.34		CSI_7_D0_P	263.65	1100	800	836.35	536.35
CSI_3_D1_N	282.24	1100	800	817.76	517.76		CSI_7_D1_N	262.00	1100	800	838.00	538.00
CSI_3_D1_P	281.24	1100	800	818.76	518.76		CSI_7_D1_P	262.82	1100	800	837.18	537.18

Notes: Max Trace Delay Allowed for SPI assumes a single load case. If two loads are implemented, See the Jetson Xavier OEM Product Design Guide for details.

3.3 Expansion Header

The Jetson Xavier carrier board includes a 40-pin (2x20, 2.54mm pitch) Expansion Header (J30). The connector used on the carrier board is a Samtec TSM-120-01-S-DV-TR.

Figure 15. Expansion Header (Top View)



Legend	Ground	5.0V Power Rail	3.3V Power Rail	1.8V/3.3V Selectable by J514	3.3V only

Note: ***Caution must be taken when using the CAN[1:0]_DIN, CAN[1:0]_DOUT pins (Exp. Conn. pins 37, 29, 33 & 31). These are pulled to 3.3V when system is powered on due to internal 3.3V pull-ups in the SoC enabled by default. If used, they should only be connected to 3.3V tolerant device pins. The voltage rail can be switched by SW after boot to 1.8V, & the internal pull-ups can be disabled, but the initial power-on state of these pins is pulled to 3.3V.***

The expansion connector includes various audio & control interfaces including:

- I2S(See Note)
- Audio Clock/Control
- Digital Microphone IF
- I2C (x2) (See Note)
- SPI (See Note)
- UART (See Note)

Table 18. Expansion Header Pin Descriptions

Pin #	Signal Name	Associated Jetson Xavier Pin Name	Usage/Description	Type/ Direction	Signal Voltage Level at Header	GPIO Max Drive (I_{OL}/I_{OH}) or Power Pin Current Capability	Notes
1	VDD_3V3	–	Main 3.3V Supply	Power	–	1A	1
2	VDD_5V	–	Main 5.0V Supply	Power	–	1A	1
3	I2C_GP5_DAT_3V3	I2C_GP5_DAT	General I2C #5 Data	Bidir/OD	1.8/3.3V	1mA / -1mA	2
4	VDD_5V		Main 5.0V Supply	Power	–	1A	1
5	I2C_GP5_CLK_3V3	I2C_GP5_CLK	General I2C #5 Clock	Bidir/OD	1.8/3.3V	1mA / -1mA	2
6	GND	–	Ground	Ground	–	–	–
7	MCLK05_3V3	AUDIO_MCLK	Audio Master Clock	Bidir	1.8/3.3V	20uA / -20uA	3
8	UART1_TX_3V3	UART1_TX	UART #1 Transmit	Output	3.3V	24mA / -24mA	4
9	GND	–	Ground	Ground	–	–	–
10	UART1_RXD_3V3	UART1_RX	UART #1 Receive	Input	1.8/3.3V	–	4
11	UART1_RTS_3V3	UART1_RTS	UART #1 Request to Send	Output	1.8/3.3V	24mA / -24mA	4
12	I2S2_CLK_3V3	I2S2_CLK	Audio I2S #2 Clock	Bidir	1.8/3.3V	20uA / -20uA	3
13	PWM01_3V3	GPIO32	Pulse Width Modulation #1	Bidir	1.8/3.3V	20uA / -20uA	3
14	GND	–	Ground	Ground	–	–	–
15	GPIO27_PWM2_3V3	GPIO27	GPIO/Pulse Width Modulation #2	Bidir	1.8/3.3V	20uA / -20uA	3
16	GPIO8_AO_DMIC_IN_DAT	GPIO8	Digital Mic Input Data	Input	3.3V	1mA / -1mA	5
17	VDD_3V3	–	Main 3.3V Supply	Power	–	1A	1
18	GPIO35_PWM3_3V3	GPIO35	GPIO/Pulse Width Modulation #2	Input	1.8/3.3V	20uA / -20uA	3, 7
19	SPI1_MOSI_3V3	SPI1_MOSI	SPI #1 Master Out/Slave In	Bidir	1.8/3.3V	20uA / -20uA	3
20	GND	–	Ground	Ground	–	–	–
21	SPI1_MISO_3V3	SPI1_MISO	SPI #1 Master In/Slave Out	Bidir	1.8/3.3V	20uA / -20uA	3
22	GPIO17_40HEADER_3V3	GPIO17	GPIO	Bidir	1.8/3.3V	20uA / -20uA	3
23	SPI1_SCK_3V3	SPI1_CLK	SPI #1 Shift Clock	Bidir	1.8/3.3V	20uA / -20uA	3
24	SPI1_CS0_3V3	SPI1_CS0#	SPI #1 Chip Select #0	Bidir	1.8/3.3V	20uA / -20uA	3
25	GND	–	Ground	Ground	–	–	–
26	SPI1_CS1_3V3	SPI1_CS1#	SPI #1 Chip Select #1	Bidir	1.8/3.3V	20uA / -20uA	3
27	I2C_GP2_DAT_3V3	I2C_GP2_DAT	General I2C #2 Data	Bidir/OD	1.8/3.3V	1mA / -1mA	2
28	I2C_GP2_CLK_3V3	I2C_GP2_CLK	General I2C #2 Clock	Bidir/OD	1.8/3.3V	1mA / -1mA	2
29	CAN0_DIN	CAN0_DIN	CAN #0 Data In	Input	3.3V	1mA / -1mA	5
30	GND	–	Ground	Ground	–	–	–
31	CAN0_DOUT	CAN0_DOUT	CAN #0 Data Out	Output	3.3V	1mA / -1mA	5
32	GPIO9_CAN1_GPIO0_DMIC_CLK	GPIO9	Digital Mic Input Clock	Bidir	3.3V	1mA / -1mA	5
33	CAN1_DOUT	CAN1_DOUT	CAN #1 Data Out	Output	3.3V	1mA / -1mA	5
34	GND	–	Ground	Ground	–	–	–
35	I2S2_FS_3V3	I2S2_FS	AUDIO I2S #2 Left/Right Clock	Bidir	1.8/3.3V	20uA / -20uA	3
36	UART1_CTS_3V3	UART1_CTS	UART #1 Clear to Send	Input	1.8/3.3V	–	4
37	CAN1_DIN	CAN1_DIN	CAN #1 Data In	Input	3.3V	1mA / -1mA	5
38	I2S2_SDIN_3V3	I2S2_SDIN	Audio I2S #2 Data in	Input	1.8/3.3V	20uA / -20uA	3, 7
39	GND	–	Ground	Ground	–	–	–
40	I2S2_SDOUT_3V3	I2S2_SDOUT	Audio I2S #2 Data Out	Output	1.8/3.3V	20uA / -20uA	3, 7

Legend

Ground	5.0V Power Rail	3.3V Power Rail	1.8V/3.3V Selectable by J514	Signals, 3.3V only

Notes:

1. This is current capability per power pin.
2. These pins connect to the SoC through an I2C (FXMA2102L8X) level shifter. They are open-drain (either pulled up, or driven low by the SoC when configured as outputs). The voltage level at the header pins can be selected by J514 to be 1.8V (2-3) or 3.3V (1-2). The max drive that meets the Data Sheet V_{OL} is 1mA.
3. These pins connect to TI TXB0108 level translators. The voltage level at the header pins is selectable (see note #2). Due to the design of these devices, the output drivers are very weak so they can be overdriven by another connected device output for bidirectional support.
4. These pins connect to a SN74LVC4T245 buffer. The voltage level at the header pins is selectable (see note #2).
5. These pins are directly connected to the SoC. The max drive that meets full Data Sheet V_{OL}/V_{OH} is 1mA.
6. In the Type/Dir column, Output is to Exp. Module. Input is from Exp. Module. Bidir is for Bidirectional signals.
7. The direction indicated matches that indicated in the reference design schematics. These signals can be bidirectional.

Table 19. Jetson Xavier Expansion Header Signal Details

Pin #	Signal Name	SoC Ball Name	SoC GPIO Port.#	Power-on Default State	Pin State after Pinmux Config.	External PU/PD on module	External PU/PD on carrier board (kΩ	Pinmux SFIO Functions Supported	Notes
3	I2C_GP5_DAT_3V3	DP_AUX_CH3_N	–	Z		1KΩ to 1.8V	2.2KΩ to 1.8V/3.3V	I2C9_DAT	3
5	I2C_GP5_CLK_3V3	DP_AUX_CH3_P	–	Z		1KΩ to 1.8V	2.2KΩ to 1.8V/3.3V	I2C9_CLK	3
7	MCLK05_3V3	SOC_GPIO42	Q.06	PD		–	1MΩ to GND	EXTPERIPH4_CLK	4
8	UART1_TX_3V3	UART1_TX	R.02	PD		100KΩ to GND	1MΩ to GND	UART1_TXD	4
10	UART1_RXD_3V3	UART1_RX	R.03	Z		–	1MΩ to GND	UART1_RXD	4
11	UART1_RTS_3V3	UART1_RTS	R.04	PD		–	1MΩ to GND	UART1_RTS	4
12	I2S2_CLK_3V3	DAP2_SCLK	H.07	PD		–	1MΩ to GND	I2S2_SCLK	4
13	PWM01_3V3	SOC_GPIO44	R.00	PD		–	1MΩ to GND	GP_PWM8	4
15	GPIO27_PWM2_3V3	SOC_GPIO54	N.01	PD		–	1MΩ to GND	GP_PWM1	4
16	GPIO8_AO_DMIC_IN_DAT	CAN1_STB	BB.00	PD		–	–	DMIC3_DAT	
18	GPIO35_PWM3_3V3	SOC_GPIO12	H.00	Z		–	1MΩ to GND	GP_PWM5	4
19	SPI1_MOSI_3V3	SPI1_MOSI	Z.05	PU		–	1MΩ to GND	SPI1_DOUT	4
21	SPI1_MISO_3V3	SPI1_MISO	Z.04	PU		–	1MΩ to GND	SPI1_DIN	4
22	GPIO17_40HEADER_3V3	SOC_GPIO21	Q.01	PD		–	1MΩ to GND	–	4
23	SPI1_SCK_3V3	SPI1_SCK	Z.03	PD		–	1MΩ to GND	SPI1_SCK	4
24	SPI1_CS0_3V3	SPI1_CS0	Z.06	PU		–	1MΩ to GND	SPI1_CS0	4
26	SPI1_CS1_3V3	SPI1_CS1	Z.07	PU		–	1MΩ to GND	SPI1_CS1	4
27	I2C_GP2_DAT_3V3	GEN2_I2C_SDA	DD.00	Z		1KΩ to 1.8V	2.2KΩ to 1.8V/3.3V	I2C2_DAT	3
28	I2C_GP2_CLK_3V3	GEN2_I2C_SCL	CC.07	Z		1KΩ to 1.8V	2.2KΩ to 1.8V/3.3V	I2C2_CLK	3
29	CAN0_DIN	CAN0_DIN	AA.03	PU		–	–	CAN0_DIN	
31	CAN0_DOUT	CAN0_DOUT	AA.02	PU		–	–	CAN0_DOUT	
32	GPIO9_CAN1_GPIO0_DMIC_CLK	CAN1_EN	BB.01	Z		–	–	DMIC3_CLK	
33	CAN1_DOUT	CAN1_DOUT	AA.00	PU		–	–	CAN1_DOUT	
35	I2S2_FS_3V3	DAP2_FS	I.02	PD		–	1MΩ to GND	I2S2_LRCK	4
36	UART1_CTS_3V3	UART1_CTS	R.05	PU		–	1MΩ to GND	UART1_CTS	4
37	CAN1_DIN	CAN1_DIN	AA.01	PU		–	–	CAN1_DIN	
38	I2S2_SDIN_3V3	DAP2_DIN	I.01	PD		–	1MΩ to GND	I2S2_SDATA_IN	4
40	I2S2_SDOUT_3V3	DAP2_DOUT	I.00	PD		–	1MΩ to GND	I2S2_SDATA_OUT	4

Notes:
1. Non-signal pins and those without functionality on Jetson Xavier are not included in table.
2. PD = SoC Internal Pull-down, PU - SoC Internal Pull-up, Z – Tristate
3. These pins are pulled up to the selectable (1.8V/3.3V) on the connector side of the level shifters.
4. Pull-down on the carrier board are on the connector side of the level shifters.

Expansion Header Interface Guidelines

See the Jetson Xavier OEM Product Design Guide for Routing Guidelines. Include the carrier board PCB trace delays in the following table when calculating max trace length & for skew matching.

Table 20. Expansion Header Related Carrier PCB Trace Delays

Jetson Xavier Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Expansion Module (ps)		Jetson Xavier Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Expansion Module (ps)
I2S					**SPI**			
I2S2_CLK_3V3	240.32	3600	3359.68		SPI1_SCK_3V3	190.26	1228	1037.74
I2S2_FS_3V3	89.46	3600	3510.54		SPI1_MOSI_3V3	191.32	1228	1036.68
I2S2_SDOUT_3V3	148.74	3600	3451.26		SPI1_MISO_3V3	186.70	1228	1041.30
I2S2_SDIN_3V3	145.98	3600	3454.02		SPI1_CS0_3V3	179.06	1228	1048.94
					SPI1_CS1_3V3	178.24	1228	1049.76

1036.68

Notes: Max Trace Delay Allowed for SPI assumes a single load case. If two loads are implemented, See the Jetson Xavier OEM Product Design Guide for details.

3.4 Fan Connector

The Jetson carrier board includes a 4-pin Fan Header (J9).

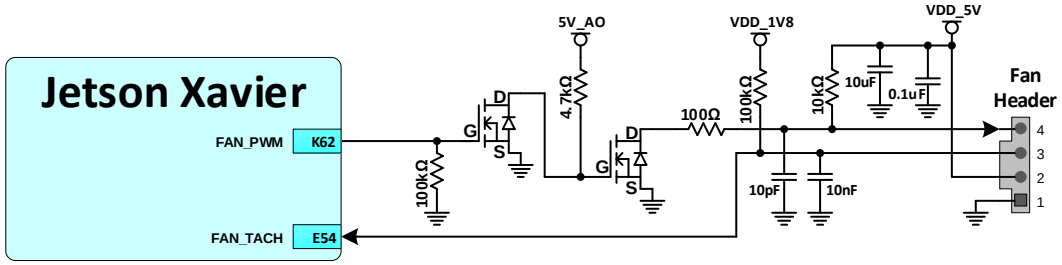


Table 21. Fan Connector Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
1	GND	–	Ground	Ground
2	VDD_5V	–	Gated version of Main 5.0V Supply (Enabled by VDD_3V3_SLP)	Power
3	FAN_TACH_CON	FAN_TACH	Fan Tachometer signal	Input
4	FAN_PWM_Q*	FAN_PWM	Fan Pulse Width Modulation signal	Output

Legend	Ground	Power	Reserved

Notes: In the Type/Dir column, Output is to Fan Connector. Input is from Fan Connector. Bidir is for Bidirectional signals.

3.5 Automation Header

The Jetson carrier board includes an 8-pin Header (J508) that makes accessible several critical system control signals.

Table 22. Automation Header Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
1	GND	–	Ground	Ground
2	FORCE_RECOVERY*	FORCE_RECOVERY_N	Force Recovery Strap	Input
3	SYS_RST_IN*	–	System Reset – Connected to Reset Button on carrier board	Input
4	BUTTON_POWER_ON*	–	Power Button – Connected to Power Button on carrier board	Input
5	CCG4_LED	–	See note	Output
6	ACOK	–	AC (USB Type C or DC Jack) power OK	Input
7	CVB_STBY	–	Reserved	RSVD
8	SYSTEM_OC_N	SYSTEM_OC_N	System Overcurrent indicator	Input

Legend	Ground	Power	Reserved

Notes:
- Auto-Power-On is enabled when pins 5 & 6 are tied together
- In the Type/Dir column, Output is to Header. Input is from Header. Bidir is for Bidirectional signals.

3.6 DC Power Jack

The Jetson carrier board uses a DC power jack (J2) to bring in the power from the included DC power supply. The jack used on the Carrier board is a Singatron Enterprise 2DC-G213-B73F.

Table 23. DC Jack Pin Descriptions

Pin #	Signal Name	Jetson Xavier Pin Name	Usage/Description	Type/Dir Default
1	VCC_DCIN	–	Option for Main DC input supplying SYS_VIN_HV (Typc C VBUS1 or VBUS2 are other options).	Power
2	GND	–	Ground	Ground
3	GND	–	Ground	Ground
4	GND	–	Ground	Ground
5	GND	–	Ground	Ground
6	GND	–	Ground	Ground

4.0 MISCELLANEOUS

4.1 Buttons, Jumpers & Indicators

Table 24. Buttons (switches)

Button	Description	Usage
S501	Power button	Used to power system up if off, or power down if on. If held for >10 seconds, will shut down the system.
S502	Reset button	Used to force a full system reset.
S503	Recovery button	Used to enter Force Recovery Mode. Button is held down while either system is first powered on, or by pressing & releasing reset button while Recovery button is pressed.

Table 25. Jumpers

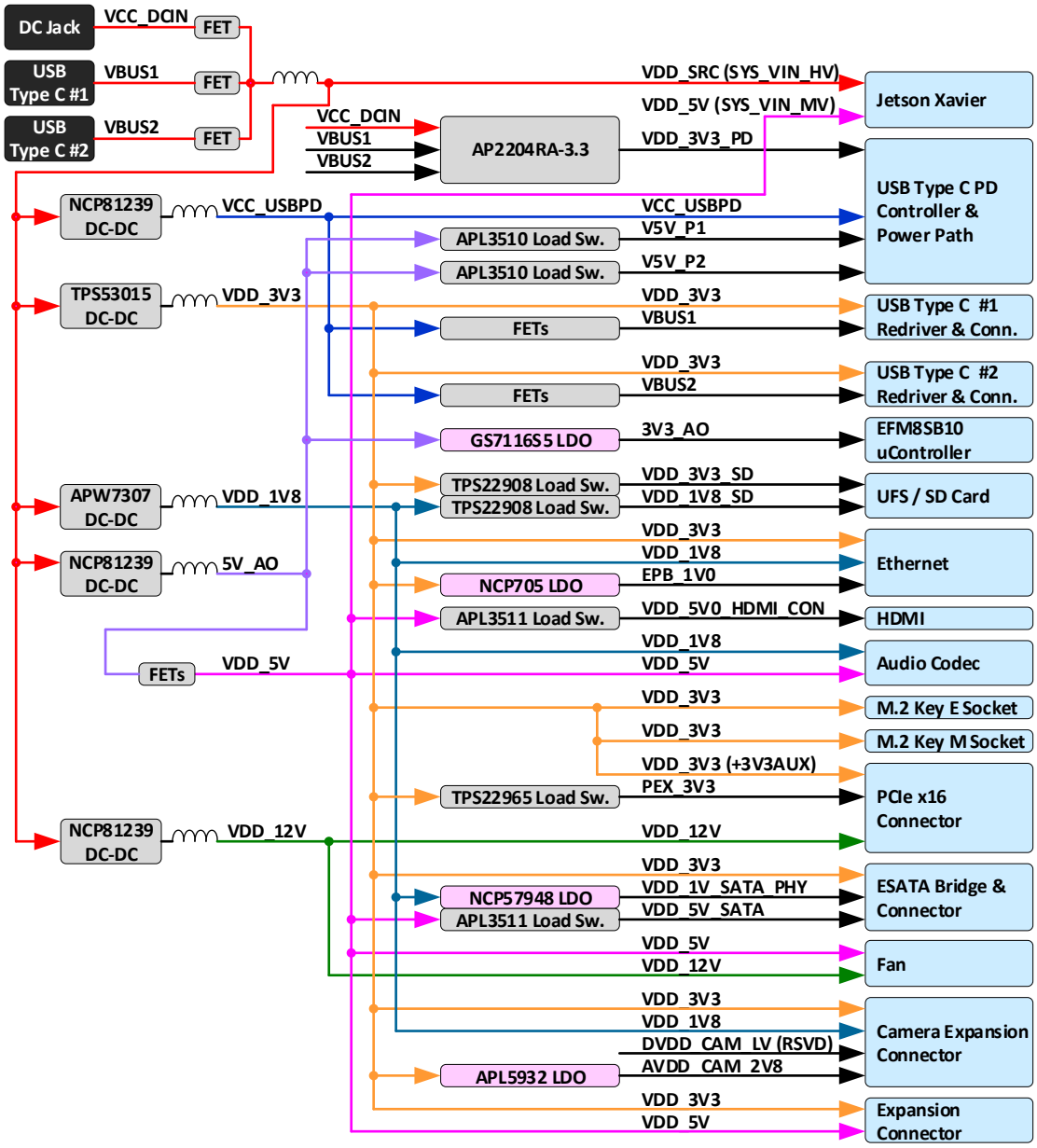
Jumper	Description	Usage
J514	Voltage select header	Selects the level shifter voltage on the non-Jetson Xavier side of the level shifters for the signals listed below. When a jumper is on pins 1-2, 3.3V level is selected. When on pins 2-3, 1.8V level is selected. - Audio MCLK05, I2S2 - PWM[3:1] - SPI1 - UART1 - I2C_GP[5,2]

Table 26. Indicators (LEDs)

LEDs	Description	Usage
DS2	SOC Regulator Power LED (Green)	Indicates when the main 5.0V (VDD_5V) supply is enabled

5.0 INTERFACE POWER

Figure 16. Interface Connector Power Diagram



The tables below show the allocation of supplies to the connectors on the Jetson carrier board and current capabilities.

Table 27 Interface Power Supply Allocation

Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable
VCC_SRC	Main power input from DC Adapter or USB type C VBUS[2:1]	9-20	FETs	**DC Adapter or Type C USB**	
VCC_USBPD		5-20	NCP81239 Regulator	**VCC_SRC**	
VDD_3V3_PD		3.3	AP2204RA-3.3 DC-DC	**VCC_DCIN or VBUS[2:1]**	VCC_DCIN, VBUS1 or VBUS2
5V_AO	Always-on 5V supply	5.0	NCP81239 DC-DC	**VCC_SRC**	CARRIER_PWR_ON
VDD_5V	Main 5V supply	5.0	FETs	**5V_AO**	VIN_PWR_ON
VDD_3V3	Main 3.3V supply	3.3	TPS53015 DC-DC	**VCC_SRC**	CARRIER_PWR_ON
VDD_1V8	Main 1.8V supply	1.8	APW7307 DC-DC	**VCC_SRC**	CARRIER_PWR_ON
VDD_12V	12V rail for PCIe, Fan	12.0	NCP81239 DC-DC	**VCC_SRC**	12V_SYS_EN (From module GPIO05)
VBUS[2:1]	VBUS pin from USB Type C connectors – main option for powering system. (alternative is DC Jack)	5-20	FETs	**VCC_USBPD**	PD Controller
PEX_3V3	PCIe x16 connector +3V3 rail supply	3.3	TPS22965 Load Switch	**VDD_3V3**	Module GPIO23
VDD_3V3_SD	SD Card & UFS VCC power rail	3.3	TPS22908 Load Switch	**VDD_3V3**	Module GPIO21
VDD_1V8_SD	UFS VCCQ2 power rail		TPS22908 Load Switch	**VDD_1V8**	Module GPIO21
EPB_1V0	Ethernet PHY DVDD power rail	1.0	NCP705 LDO	**VDD_3V3**	VDD_3V3
VDD_5V0_HDMI_CON	5V rail for HDMI connector	5.0	APL3511 Power Switch	**VDD_5V0**	Module GPIO20
VDD_1V_SATA_PHY	PCIe to eSATA bridge VDD power rail	1.0	NCP57948 LDO	**VDD_1V8**	VDD_1V8
VDD_5V_SATA	VBUS for USB portion of Hybrid eSATA connector.	5.0	APL3511 Load Switch	**VDD_5V**	Module GPIO22
DVDD_CAM_LV	Reserved for potential use as Camera Digital power rail	NA	NA	NA	NA
AVDD_CAM_2V8	Camera Analog power rail	2.8	APL5932 LDO	**VDD_3V3**	Module GPIO36

Table 28 Interface Supply Current Capabilities

Power Rails	Usage	(V)	Max Current (A)
VCC_SRC	Main power input from USB Type C connectors or DC Jack	9-20	5.0
VDD_5V	Main system 5V supply	5.0	9.5
VDD_3V3	Main system 3.3V supply	3.3	10.5
VDD_1V8	Main system 1.8V supply	1.8	2.8
VDD_12V	12V rail for PCIe connector & optionally for Fan	12	5.5
AVDD_CAM_2V8	Analog Camera rail	2.8	3.0

Notes:
1. The values shown in the "Max Current" column indicate the total power available on the expansion connectors minus the current used on the platform (not per connector pin).
2. If a given voltage rail cannot provide enough current, a possible solution is for the user to use a regulator from VDD_5V, VDD_3V3 or VDD_1V8 to generate the desired rail.

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