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S2000 Spectrometer Data Sheet

Description

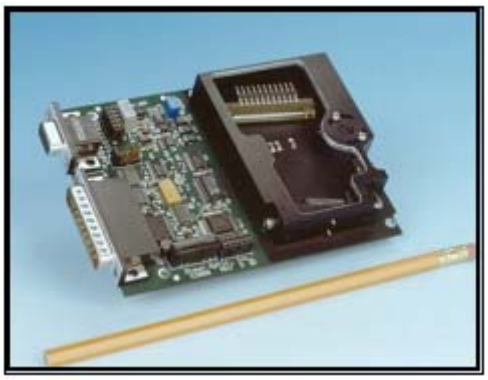
The Ocean Optics OEM S2000 Spectrometer includes the linear CCD-array optical bench, plus the circuits necessary for spectrometer operation. The result is a compact, flexible system with no moving parts that's easily integrated as an OEM component.

The S2000 Spectrometer is a unique combination of technologies providing users with both an unusually high spectral response and good optical resolution in a single package. The electronics have been designed for considerable flexibility in connecting to various S2000 Series modules as well as external interfaces. The S2000 can be directly coupled to as many as 7 "slave" spectrometer channels of various designs. The S2000 also can be supplied in a CE-certified enclosure. The information included in this guide provides detailed instructions on the connection and operation of the S2000.

The detector used in the S2000 Spectrometer is a high-sensitivity 2048-element CCD array from Sony (product number ILX511). (For complete details on this detector, visit Sony's web site at http://www.sel.sony.com/semi/PDF/ILX511.pdf.) However, Ocean Optics applies a coating to all ILX511 detectors, so the optical sensitivity could vary from that specified in the Sony datasheet.

The S2000 operates from a single +5VDC supply and two clock signals. One clock sets the detector's integration time and the other clock sets the A/D frequency. Having separate clock signals allows the user to integrate for long periods of time yet clock the data out of the spectrometer quickly. These two clocks are not required to be synchronous except in the situation where a light source strobes multiple times during an integration period (see Synchronizing Strobe Events on page 10).

The S2000 generates two signals for triggering light sources and external hardware and supports four different trigger modes. Details of these functions are provided in later sections.



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Features

Listed below are the design specifications for the USB A/D card:

- High sensitivity of up to 90 photons/counts
- An optical resolution of 3 pixels (FWHM)
- A wide variety of optics available
  - 14 gratings
  - 6 slit widths
  - 3 detector coatings
  - 6 optical filters
- Integration times from 2 to >30000 milliseconds
- Low power of only 650 mW
- Modular design allows up to 7 slave spectrometer channels to operate from one master channel
- 2 MHz maximum CCD frequency
- 4 triggering modes
- 2 strobe signals for triggering other devices
- CE Certification

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Mechanical Diagrams

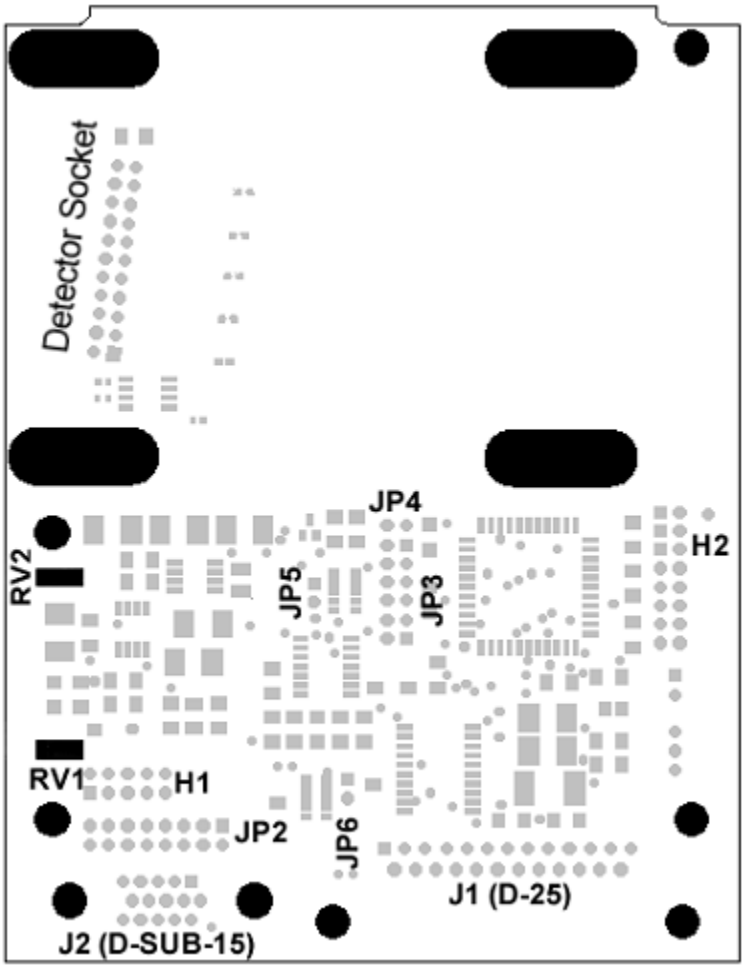


Figure 1: Board Diagram – Layout

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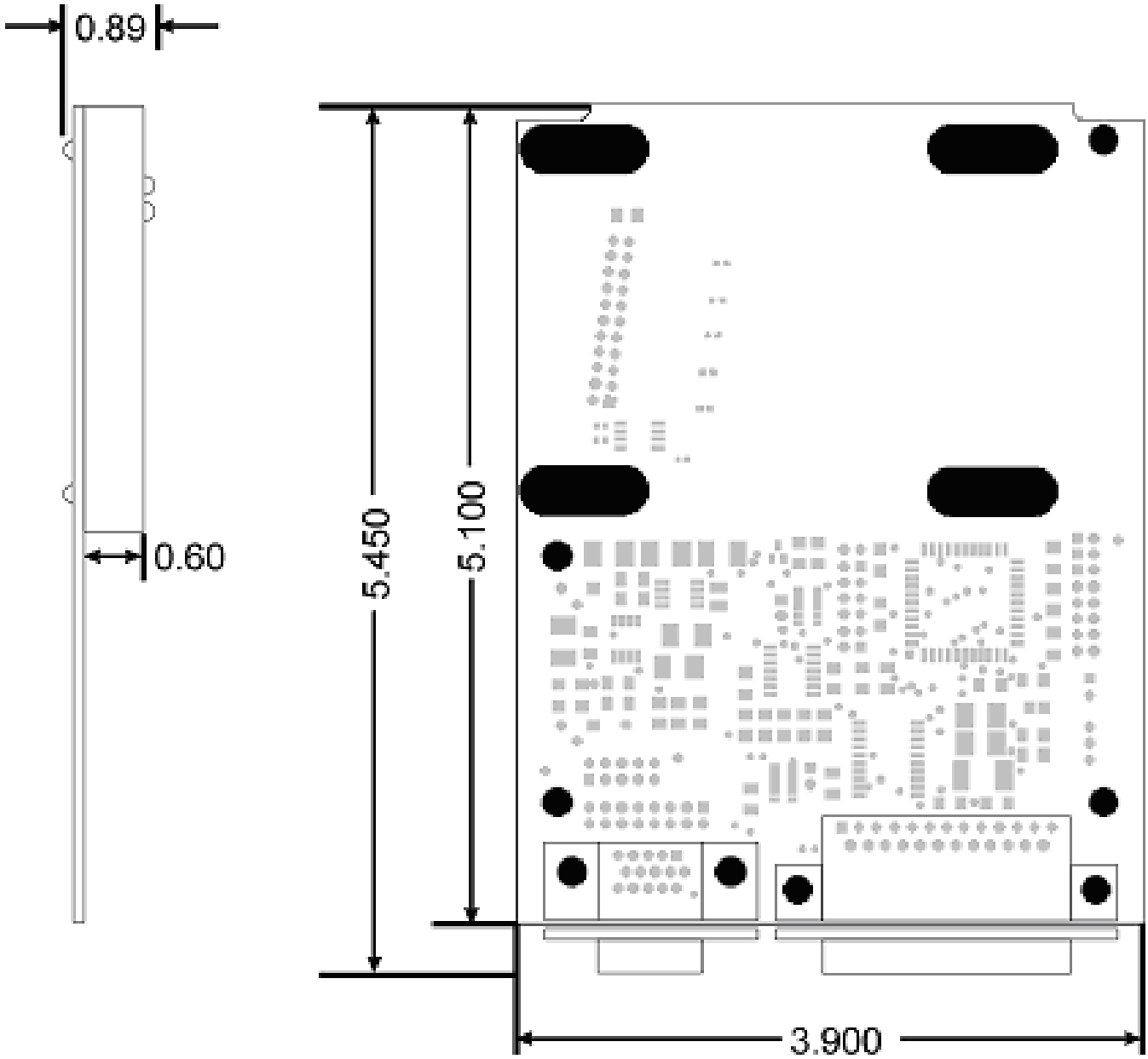


Figure 2: Board Diagram Overall – Dimensions

Notes:

- All dimensions are in inches.
- PCB thickness is 0.062” nominal.
- User must provide sufficient clearance on the bottom of the PCB to prevent electrical short-circuiting of leads. An additional 0.25” is recommended.

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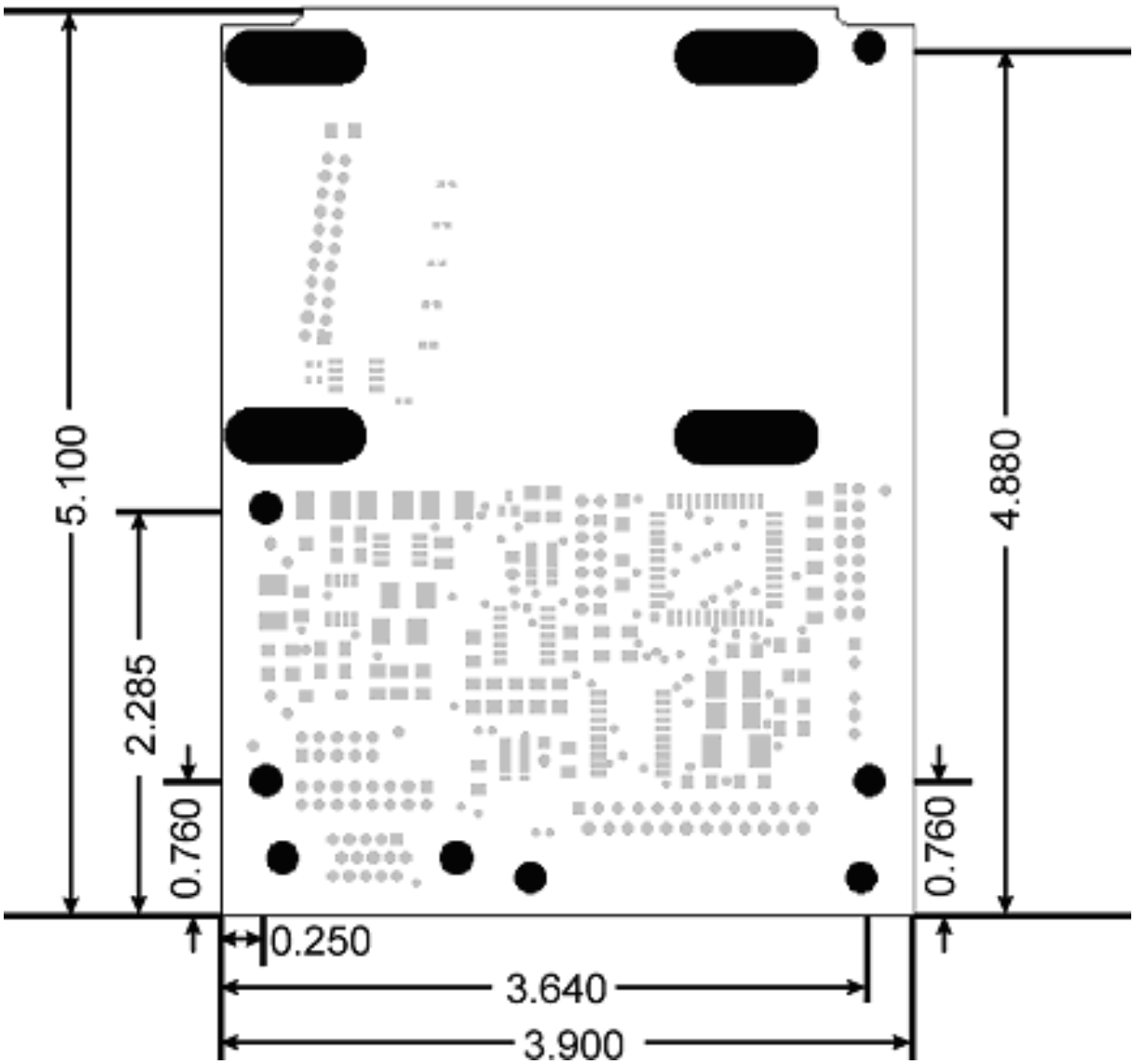


Figure 3: Board Diagram – Mounting Holes

Notes:

- All dimensions are in inches.
- Electrical and optical components are not shown for clarity. Maximum electrical component height is 0.40”. Maximum optical component height is 0.71”.
- All mounting holes are connected to ground.
- All mounting holes are 0.125” ID, designed for a 4-40 screw.
- PCB thickness is 0.062” nominal.

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Specifications

Specifications	Criteria
Absolute Maximum Ratings:	
V_{CC}	+ 5.5 VDC
Voltage on any pin	Vcc + 0.2 VDC
Physical Specifications:	
Physical Dimensions (no enclosure)	5.45 (length) x 3.90 (width) x 0.90 (height) inches (master only)
Physical Dimensions (enclosure)	5.46 (length) x 4.14 (width) x 1.60 (height) inches (master only)
Weight	200 g (master only, no enclosure)
Power:	
Power requirement (master)	130 mA at +5 VDC
Power requirement (slave)	70 mA at +5 VDC
Supply voltage	4.5 – 5.5 V
Power-up time	3 msec
Spectrometer:	
Design	Asymmetric crossed Czerny-Turner
Focal length (input)	42 mm
Focal length (output)	68 mm (75, 83 and 90 mm focal lengths are also available)
Input Fiber Connector	SMA 905
Gratings	14 different gratings
Entrance Slit	5, 10, 25, 50, 100, or 200 µm slits. (Slits are optional. In the absence of a slit, the fiber acts as the entrance slit.)
Detector	Sony ILX511 CCD
Filters	2nd order rejection, long pass (optional)
Spectroscopic:	
Integration Time	3 – >30,000 msec
Dynamic Range	2 x 10^8
Signal-to-Noise	250:1 single acquisition
Readout Noise (single dark spectrum)	3.5 counts RMS, 20 counts peak-to-peak
Resolution (FWHM)	0.03 – 10.0 nm varies by configuration (see www.Oceanoptics.com for configuration options)
Stray Light	<0.05% at 600 nm; <0.10% at 435 nm
Spectrometer Channels	8 (master plus up to 7 slaves)
Environmental Conditions:	
Temperature	-30° to +70° C Storage & -10° to +60° C Operation
Humidity	0% - 90% noncondensing

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Electrical Pinouts

J1 (D-25) Master to A/D Connectors

Pin	Function
1	Analog Channel 0
2	Analog Channel 1
3	Analog Channel 2
4	Analog Channel 3
5	Analog GND
6	Reserved
7	N/C
8	N/C
9	Digital GND
10	A/D Trigger
11	Master Clock
12	Digital GND
13	+5VDC
14	Analog Channel 4
15	Analog Channel 5
16	Analog Channel 6
17	Analog Channel 7
18	Analog GND
19	N/C
20	Continuous Strobe In
21	External Software Trigger Out (D3)
22	Spectrometer Mode Input S1
23	Integration Time Clock In
24	S0
25	Enable Read In

J2 (D-SUB-15) Accessory Connectors

Pin	Function
1	Single Strobe
2	Continuous Strobe
3	+5VDC
4	External Hardware Trigger
5	External Synchronization Trigger
6	Analog Channel 7 Input
7	Analog Channel 6 Input
8	External Software Trigger (D3)
9	Analog Channel 1 input
10	GND
11	Analog Channel 4 input
12	Analog Channel 5 input
13	S0
14	Analog Channel 3 input
15	Analog Channel 2 input

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H1 Header Pins (Analog)

1	Analog Channel 0
2	Analog Channel 1
3	Analog Channel 2
4	Analog Channel 3
5	Analog Channel 4
6	GND
7	Reserved
8	Analog Channel 7
9	Analog Channel 6
10	Analog Channel 5

H2 Header Pins (Digital)

D	N/C
C	A/D Trigger
B	D3 (Digital In 3)
A	S1
1	GND
2	+5 VDC
3	Phi A/D Clock
4	Phi Readout Gate
5	Reserved
6	Temperature (optional)
7	Read Enable
8	S0
9	Single Strobe
10	Continuous Strobe
11	Integration Clock
12	Master Clock

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Pin Function Description

Function	Description
Analog Channel 0 - 7	The analog signals that correspond to the output from the 8 spectrometer channels. Inputs for channels 1-7 are available on J1.
V_{CC}	The positive supply voltage +5VDC.
GND	The ground (supply voltage return) or case ground.
Integration Clock	The free-running TTL clock signal that determines the integration (exposure) time.
Master Clock	The free-running TTL clock signal that is 2x the desired A/D frequency.
Read Enable	The active high TTL input signal. Driving this line high generates the A/D Trigger pulses at the start of the next integration period. Driving this line LOW disables the trigger signals.
A/D Trigger	TTL output signal used for triggering an A/D converter. The analog signals should be latched onto the rising edge of this signal.
S0 & S1	TTL Inputs used to determine the triggering mode. **S1** **S0** **Mode** L X Normal or Continuous Scan L X External Software Trigger H L External Synchronization Trigger H H External Hardware Trigger X = does not matter In the first 2 modes, S0 is also used to enable/disable light sources.
D3	Active high TTL input signal used to trigger the acquisition system in the External Software Trigger mode. The input from J1: pin 8 is passed unbuffered to this line.
Single Strobe	TTL output signal used to pulse a strobe that is high at the start of each integration period.
Continuous Strobe	TTL output signal used to pulse a strobe that is divided down from the Master Clock signal.
External Hardware Trigger	TTL trigger signal (rising edge trigger input) used in the External Hardware Trigger mode.
External Synchronization Trigger	TTL signal used to define the integration time (time between rising edges) when using the External Synchronization Trigger mode.
F Clock	Clock signal used to drive the slave spectrometers.
F Read	TTL timing signal used to drive the slave spectrometers.

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Interface Information

Pixel Definition

A series of pixels in the beginning of the scan have been covered with an opaque material to compensate for thermal induced drift of the baseline signal. As the S2000 warms up, the baseline signal will shift slowly downward a few counts depending on the external environment. (Temperature-regulated units do not exhibit this shift.) The baseline signal is set between 50 and 100 counts at the time of manufacture. If the baseline signal is manually adjusted, it should be left high enough to allow for system drift. The following is a description of all of the pixels:

Pixel	Description
0 – 1	Not usable
2 – 24	Optical black pixels
24 – 25	Transition pixels
26 – 2074	Optical active pixels

It is important to note that Ocean Optics A/D products only digitize the first 2048 pixels, as they all have a 2048 x 16 FIFO buffer.

Analog Section

The S2000 is capable of supporting the output of up to 8 spectrometer channels (master channel plus 7 slave channels). Each spectrometer generates an analog signal (0-10V factory default), which corresponds to the input spectra. The analog circuitry performs an inversion and a level shift of the signal. The level shift is capable of adjusting the output range ±10V. The bandwidth of this signal is ~2MHz. The analog and digital sections share the same ground.

Channel Selection

JP2 determines the analog channel to which the spectrometer's signal will be routed. There are 8 possible jumper positions that correspond to the 8 spectrometer channels.

Timing Requirements

Spectral Acquisition

The detector's signal is being shifted out and converted for each integration period, thus it is the function of the A/D card to decide when to capture spectral data. To acquire a spectrum, the user drives the Read Enable signal HIGH.

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The A/D Trigger signal is then generated starting with pixel 0 of the next integration period. The trigger signal appears as a pulse train in which the analog signal is valid on the rising edge of each pulse (see the Timing Diagram on p. 12). This pulse train continues until the Read Enable signal is driven LOW. It is the responsibility of the A/D converter to acquire the desired number of pixels and then reset the Read Enable signal. All Ocean Optics A/D products convert the first 2048 pixel values, drive Read Enable LOW, and ignore the remaining 26 pixels.

Operating the S2000 with the Read Enable HIGH all of the time leaves the A/D converter to decide when to digitize the pixel values. We don't recommended operating the system in this manner, as the timing between the start of an integration period and the first pixel is not identical for all S2000 revisions.

Master Clock

The Master Clock cannot exceed 4 MHz, which equates to a CCD array limit of 2 MHz (meaning that the maximum A/D Trigger frequency is 2 MHz). Due to the readout electronics in the spectrometer, the analog signal increases as the Master Clock frequency decreases. A recommended minimum frequency is 100 kHz.

Integration Clock

The period for the integration time clock should be longer than 2048 trigger events in order to read the entire array. If necessary, asymmetrical pulse trains can be used for the integration time clock, but the HIGH level should exceed 4 master clock ticks. It is recommended, but not required, that the integration time clock be synchronous with the master clock. However, if the continuous strobe output is used, the integration time clock and the master clock **must** be synchronous.

A/D Trigger Signal

The Read Enable line should be driven HIGH when a train of A/D Triggers is required (i.e., 2048 pixels). The analog signal for all spectrometers is valid on the rising edge of the A/D Trigger signal. This rising edge is spaced in time at the mid-point for a given pixel. Pixel 0 is about 40 master clock cycles after the start of an integration period.

Strobe Signals

Single Strobe

The Single Strobe signal is a TTL HIGH pulse that occurs at the start of each integration period. This pulse occurs 2 master clock cycles (32 for Rev D Boards) after the start of the integration period. The pulse is not generated unless S0 is HIGH.

Continuous Strobe

The Continuous Strobe signal is a pulse-train (50% duty cycle) whose frequency is determined by the JP3 jumper setting. The master clock frequency is divided by 2 and then further divided by the JP3 jumper setting as shown in the following table. Position 1 of JP3 connects the Strobe In signal (DB25: Pin 20) to the Continuous Strobe output, thereby allowing the user to supply the strobe signal.

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JP3 Position	÷ by	Output Frequency	
		1 MHz Master Clock Freq.	2 MHz Master Clock Freq.
5	2^{10}	488 Hz	977 Hz
4	2^{12}	122 Hz	244 Hz
3	2^{14}	30.5 Hz	62 Hz
2	2^{16}	7.6 Hz	15.3 Hz
1	N/A	User Set	User Set

Synchronizing Strobe Events

For some applications it is necessary to view pulsed sources. If the application requires more than one pulse per integration period, exercise care to insure a stable signal. In these cases, the master clock and integration clock **must** be synchronous. The integration time must be set so that an equal number of strobe events occurs during any given integration period. This synchronization only occurs when the integration period is a multiple of a power of 2, since the strobe signal is the master clock divided by a power of 2.

Triggering Modes

The S2000 supports four triggering modes, which are defined by the state of the S0 and S1 signals. Depending on the triggering mode chosen, the source for the integration clock could come from the A/D converter or from an external source. Each triggering mode is detailed below.

Normal (S1:S0 = 0:X)

In this mode, the S2000 uses the user-supplied integration clock (DB25: Pin 23) and continuously scans the CCD array.

External Software Trigger (S1:S0 = 0:X)

In this mode, the S2000 uses the user-supplied integration clock (DB25: Pin 23); however, the A/D converter is required to wait until the D3 line (DB15: Pin 8) goes HIGH before it drives the Read Enable line HIGH. The amount of delay between the trigger pulse and when a spectrum is acquired is indeterminate because the delay is dependent upon (1) how fast the software polls the D3 line and recognizes it is HIGH and (2) the amount of time until the start of the next integration period. The integration time is under user control in this mode. This mode must be implemented in the software that controls the data acquisition. All Ocean Optics software drivers enable this triggering mode.

External Synchronization (S1:S0 = 1:0)

In this mode, the effective integration time is the time between rising edges of the signal applied to the External Synchronization pin (DB15: Pin 5). This mode is useful for synchronizing the integration time to an external clock source.

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External Hardware Trigger (S1:S0 = 1:1)

In this mode, the S2000 uses an internally generated integration clock that is triggered by the rising edge of the External Hardware Trigger signal (DB15: Pin 4). On the rising edge of this signal, the internal logic resets the CCD array, integrates for a period of time determined by the position of JP4, and then clocks out the array. The following table illustrates how the integration time is dependent upon the master clock frequency.

JP4 1-2	JP4 3-4	Integration Time Equation	Integration Time	
			1 MHz Master Clock Frequency	2 MHz Master Clock Frequency
out	out	$8.8/F_m$	8.8 ms	4.4 ms
out	in	$27.5/F_m$	27.5	13.3
in	out	$55/F_m$	55	27.5
in	in	$137.5/F_m$	137.5	67.5
F_m = the master clock frequency in MHz				

CCD Detector

The detector used for the S2000 is a charge transfer device (CCD) that has a fixed well depth (capacitor) associated with each photodetector (pixel).

Charge transfer, reset and readout initiation begin with the integration time clock going HIGH. At this point, the remaining charge in the detector wells is transferred to a shift register for serial transfer. This process is how the array is read.

The reset function recharges the photodetector wells to their full potential and allows for nearly continuous integration of the light energy during the integration time, while the data is read out through serial shift registers. At the end of an integration period, the process is repeated.

When a well is fully depleted by leakage through the back-biased photodetector, the detector is considered saturated and provides the maximum output level. The CCD is a depletion device and thus the output signal is inversely proportional to the input photons. The electronics in the S2000 invert and amplify this electrical signal.

CCD Detector Reset Operation

At the start of each integration period, the detector transfers the signal from each pixel to the readout registers and resets the pixels. The total amount of time required to perform this operation is ~20 µs. The user needs to account for this time delay when the pixels are optically inactive, especially in the external triggering modes.

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CCD Detector Temperature

Also available is an optional temperature sensor, which when included is located directly under the detector. The output of this signal is fed to H2: pin 6. The typical uncalibrated error of the sensor is ± 0.5°C around 25°C. The output is calibrated directly in °C with a scale factor of 10 mV/°C.

If slave spectrometer channels with temperature sensors are stacked with a master unit, avoid shorting the signal between them by cutting the pin (H2: pin 6) between the boards.

CCD Well Depth

We strive for a large signal-to-noise (S:N) in optical measurements so that small signal variations can be observed and a large dynamic range is available. The S:N in photon noise-limited systems is defined and measured as the square root of the number of photons it takes to fill a well to saturation. In the S2000, the well depth of the CCD pixels is about 160,000 photons, providing a S:N of 400:1 (S:N can also be measured as the saturation voltage divided by near-saturation RMS noise). There is also a fixed readout noise component to all samples. The result is a system with a S:N of ~275:1.

There are two ways to achieve a large S:N (e.g., 6000:1) in CCD detectors where photon noise is predominant.

1. Use a large-well device that integrates to saturation over a long period of time until the photon noise is averaged out by the root of *n* multiples of a defined short Δt.
2. Use a small-well device that integrates to saturation at one short Δt and then signal average mathematically *n* times.

Theoretically, both approaches achieve the same results, though there are large differences in actual operation. Traditional spectroscopic instruments use large-well devices and 16-bit ADCs to achieve the defined S:N. The S2000 uses a small-well device and utilizes signal averaging to achieve the same S:N. A brief comparison of large and small-well devices is shown in the table below.

Well Depth Comparison

Large-well CCDs	Small-well CCDs
Low photon noise	Medium photon noise that can be averaged out
Low optical sensitivity	High optical sensitivity
High power consumption	Low power consumption
>10 MHz operating speeds	Moderate operating speeds (~2 MHz)

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Signal Averaging

Signal averaging is an important tool in the measurement of spectral structures. It increases the S:N and the amplitude resolution of a set of samples. The types of signal averaging available in our software are time-based and spatial-based.

When using the time-base type of signal averaging, the S:N increases by the square root of the number of samples. Signal averaging by summing is used when spectra are fairly stable over the sample period. Thus, a S:N of 2500:1 is readily achieved by averaging 100 spectra.

Spatial averaging or boxcar averaging can be used to improve S:N when observed spectral structures are broad. The traditional boxcar algorithm averages *n* pixel values side by side and replaces the center value with an averaged value.

Time-based and spatial-based algorithms are not correlated, so therefore the improvement in S:N is the product of the two processes.

In review, large-well devices are far less sensitive than small-well devices and thus, require a longer integration time for the same output. Large-well devices achieve a good S:N because they integrate out photon noise. Small-well devices must use mathematical signal averaging to achieve the same results as large-well devices, but small-well devices can achieve the results in the *same period of time*. This kind of signal averaging was not possible in the past because analog-to-digital converters and computers were too slow.

Large-well devices consume large amounts of power, resulting in the need to build thermoelectric coolers to control temperature and reduce electronic noise. Then, even more power is required for the temperature stabilization hardware. But small-well devices only need to utilize signal averaging to achieve the same results as large-well devices, and have the advantages of remaining cool and less noisy.

A/D Converter

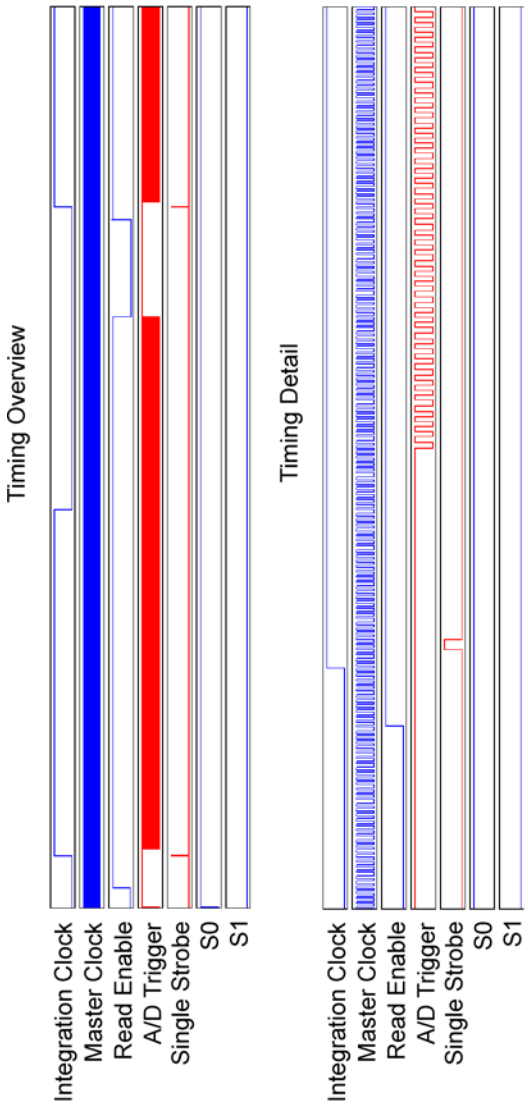
Its important to realize that the detector's signal is being shifted out and converted for every integration period. It is the function of the A/D converter to decide when to capture spectral data. An integration period is defined as the timebetween rising edges of the integration clock. To ensure reproducible measurements, it is extremely important that this period be consistent from cycle to cycle.

In order for an A/D converter to digitize the output analog signal, it needs to know where the start of the spectra is and when each pixel is "valid." The A/D Trigger signal serves this function. Once the user drives the Read Enable signal HIGH, the A/D Trigger signal will be generated starting with pixel 0 of the next integration period. The trigger signal will appear as a pulse train in which the analog signal is valid on the rising edge of each pulse (see *Timing Diagram*).

This pulse train will continue until the Read Enable signal is driven LOW. Thus it is the responsibility of the A/D converter to count the number of pixels being digitized and "turn off" the Read Enable pulse once the desired number is reached.

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Timing Diagram



Notes:

- The user must drop the Read Enable line LOW after receiving the desired number of A/D triggers (pixels).
- Spectral data (signal from the CCD detector) runs parallel with the A/D Trigger pulses. All spectrometer channels are read out simultaneously. It is the responsibility of the A/D converter to know which analog signal to digitize.

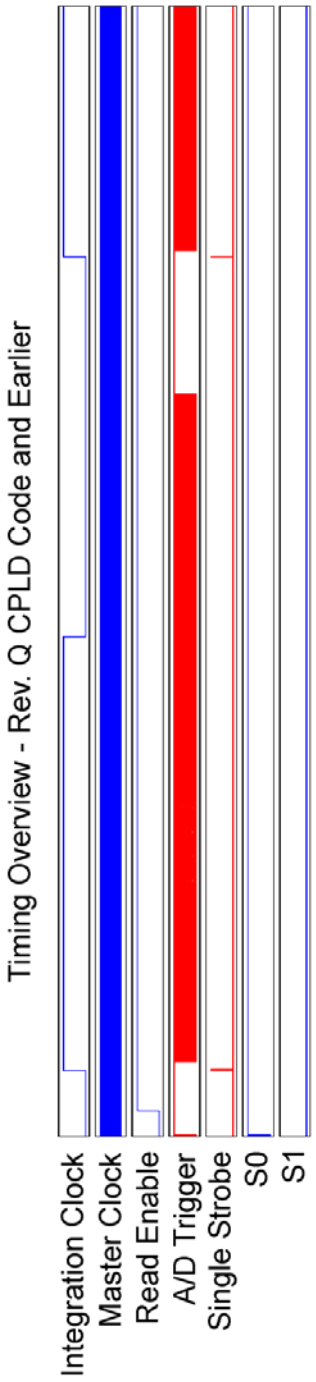
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Errata 1

This Errata Sheet applies to all S2000 and PC2000 spectrometers that are programmed with the Rev Q or earlier CPLD code. These units can be identified by the letter “Q” (or earlier) on the 44-pin PZ5064 chip, which is designated as U3 on the S2000 Rev J, and U35 on the PC2000 Rev D.

Problem:

As described in the S2000 OEM Guide, the A/D Trigger signal presents trigger events until the Read Enable signal is driven LOW. On the affected units, the A/D Trigger signal presents trigger events for the first 2048 pixels only. If Read Enable remains HIGH after this time, additional trigger events will be generated at the start of the next integration period (see figure at right). In other words, the A/D Trigger signal is “active” for just the first 2048 pixels of any integration period. If the Read Enable signal is driven LOW while it is pulsing, the A/D Trigger signal will return to the “inactive” state.



Implications:

Since Ocean Optics A/D converters only digitize the first 2048 pixels, this functionality does not interfere with the normal operation of the system. This functionality only presents a problem in systems which (1) capture the entire 2074 pixels or, (2) set Read Enable HIGH continuously.

Solution:

When using an Ocean Optics A/D converter, the system will function normally and no repair is required. For use in other systems, the user can simply ensure that the Read Enable line is driven LOW after 2048 A/D triggers have been received. Contact Ocean Optics to return the S2000 for chip reprogramming.

Note:

The Read Enable line is kept HIGH, and A/D triggers are sent by the spectrometer at the beginning of each integration period. This behavior is present only in Rev. Q or earlier of the CPLD code, and will not be continued.

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