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COMET™

VMEbus I/O BOARD
Multi-Channel Analog Digitizer
REFERENCE MANUAL

February 1994

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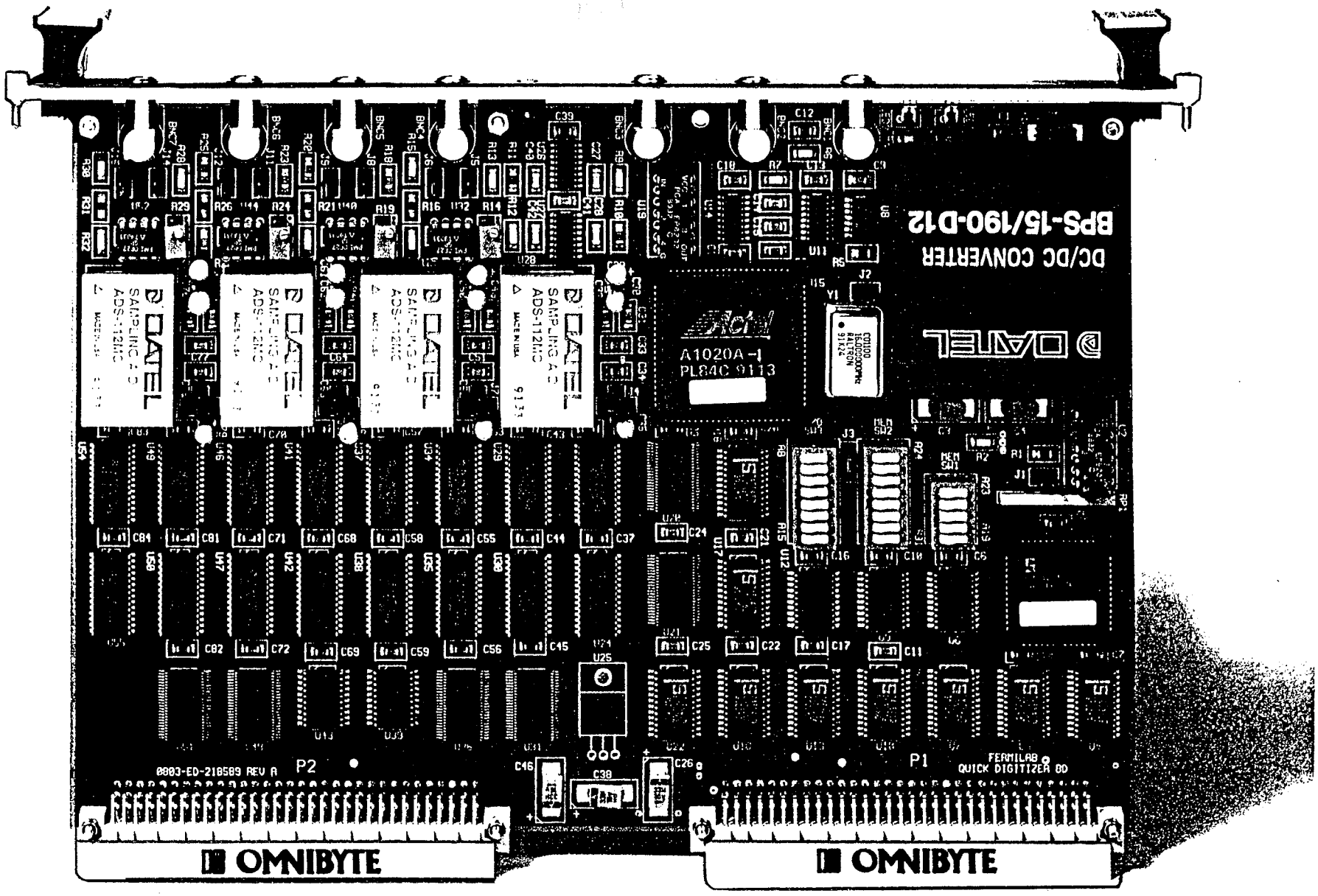
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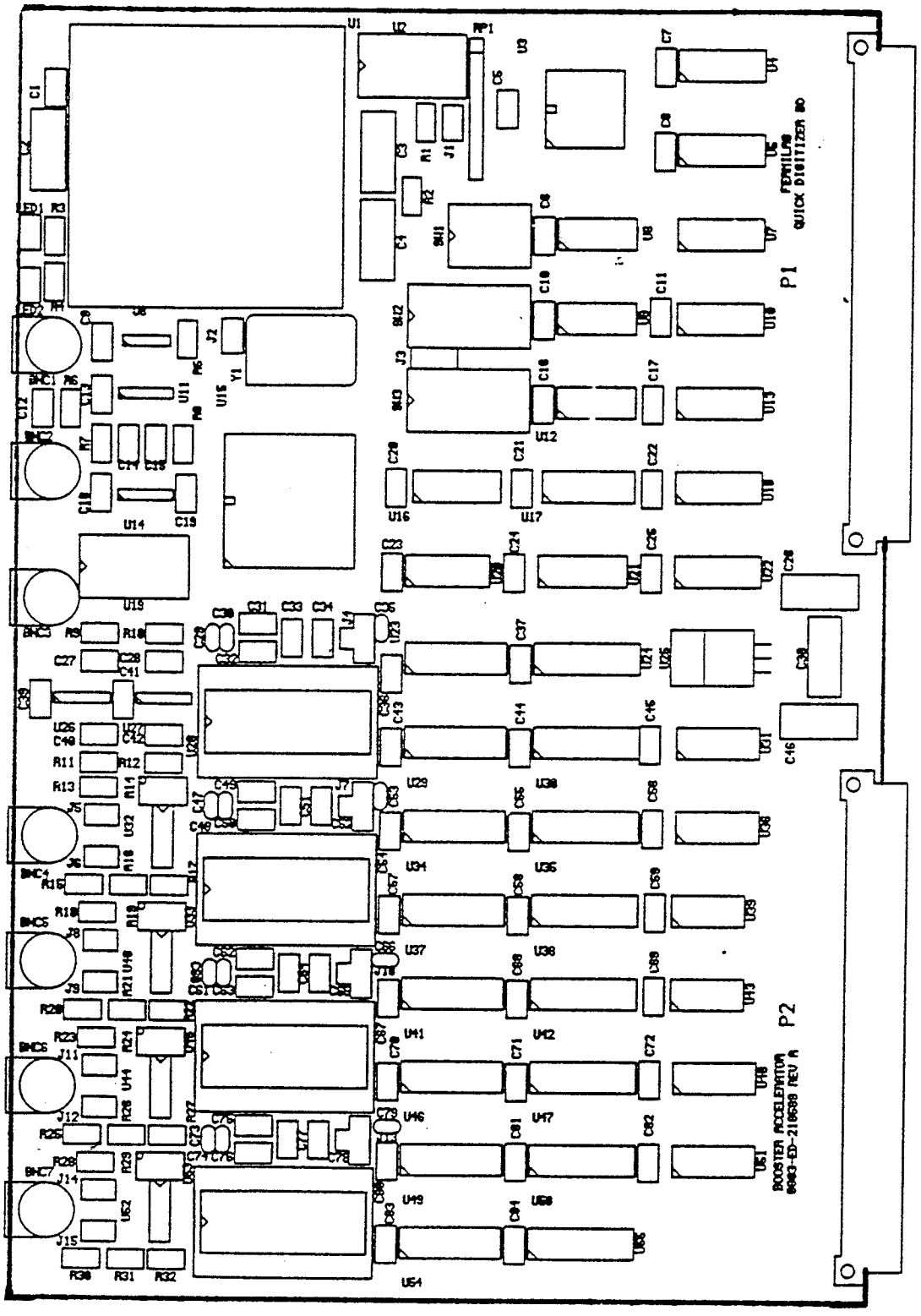


FIGURE 1.1 COMET PARTS LOCATION DIAGRAM

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1.0 INTRODUCTION/INSTALLATION

1.1 Introduction

This chapter provides the unpacking and inspection instructions for the VMEbus COMET Board.

1.2 Unpacking and Inspection

When handling the COMET board, observe Electrostatic Discharge (ESD) procedures to protect the board from damage. Omnibyte strongly recommends that the board be kept in the anti-static foam (pink plastic) when not in use.

"NOTE"

IF THE SHIPPING CARTON IS DAMAGED UPON RECEIPT, REQUEST THAT CARRIER'S AGENT BE PRESENT WHILE THE ITEMS ARE BEING UNPACKED AND INSPECTED.

Unpack the COMET VMEbus I/O board from its shipping carton. Save the packing material for storing and reshipping the items in case this becomes necessary. The COMET VMEbus I/O board should be inspected upon receipt for broken, damaged, or missing parts, and for physical damage to the printed circuit board or connectors.

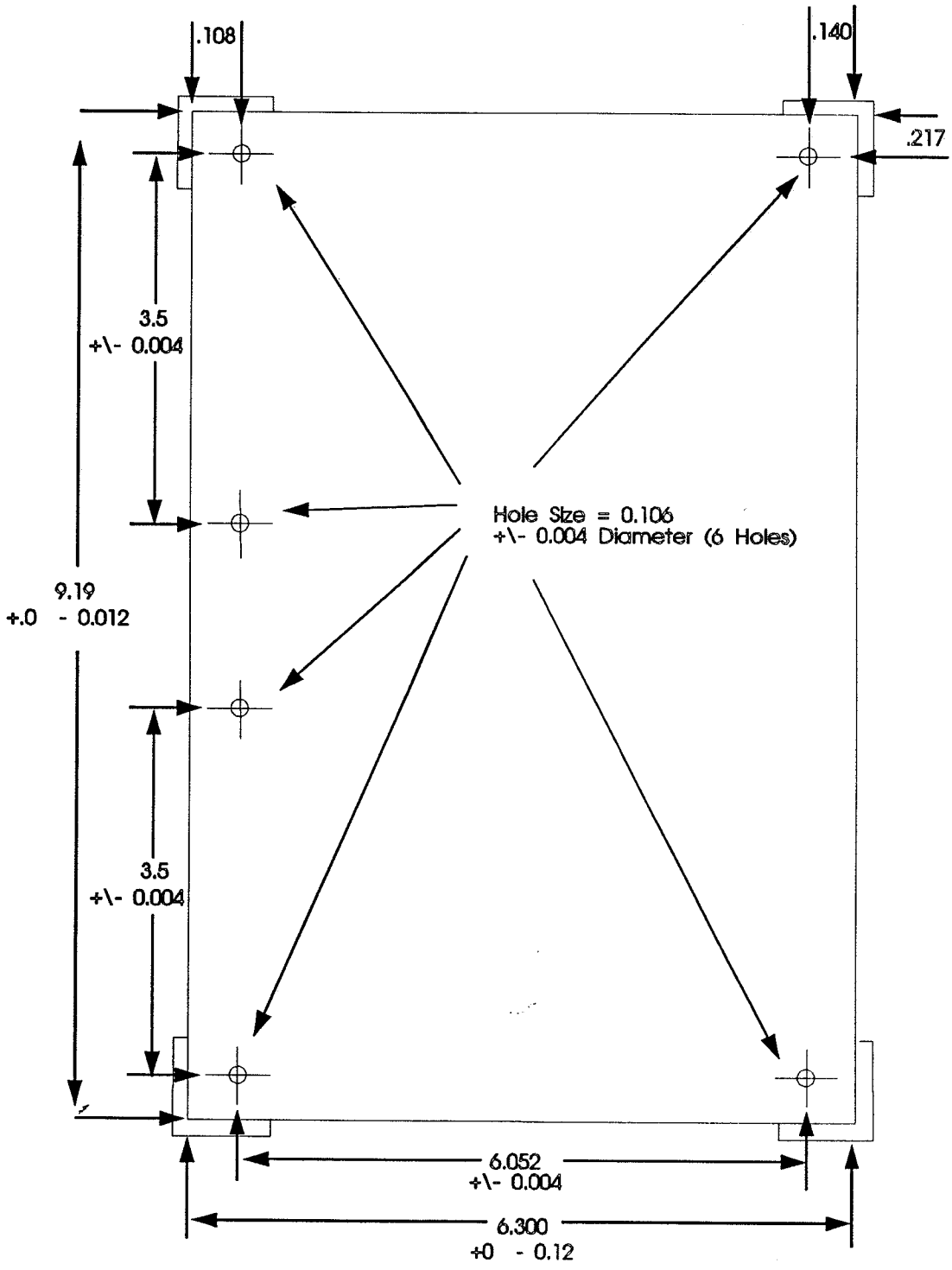
1.3 Factory Standard Configuration

The COMET board may be used in several configurations. Prior to inserting the COMET in a system, care should be taken to install the proper jumper options on the COMET board. Refer to Figure 4.3 for physical locations of the jumper options on the COMET. See Section 4.3 for the Factory Standard Configuration of the COMET.

1.4 Specifications

Listed below are the specifications for compliance, environment, power and dimensions for the COMET Multi-Channel Analog Digitizer Board.

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All board dimensions are in inches.

FIGURE 1.4 COMET BOARD DIMENSIONS

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1.4.1 VMEbus Compliance

This section lists the VMEbus compliance and options for the COMET board.

Slave Data Transfer Options:

Extended Addressing: A32:D16
Standard Addressing: A24:D16
Short Addressing: A16:D16

1.4.2 Environmental

Temperature:	0 to 65 degrees C (operating) -15 to +85 degrees C (storage)
Humidity:	0 to 90% (non-condensing)

1.4.3 Power Requirements

The board receives its power through the VMEbus Backplane. Power requirements are as follows:

+5 VDC ± 5%	2.4 Amps. Max (2.0 A. Typ.)
+12 VDC ± 5%	.7 A Typ. using four ADS-117 devices .4 A Typ. using four ADS-118 devices
-12 VDC ± 5%	0.09 A Typ. using four ADS-117 devices .5 A Typ. using four ADS-118 devices

1.4.4 Physical

The COMET is a NEXP (Non-Expandable Data Bus, Double Height (6U) VMEbus printed circuit board. See Figure 1.4 for dimensions of the board.

Dimensions: 9.19 in (234 mm) X 6.30 in (16 mm) X 0.062in (0.16mm)

PC Board: FR4 material, Multilayer - Solder mask on both sides.

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1.5 OVERVIEW OF THE I/O BOARD

This section describes the major features of the COMET. A block diagram of this I/O board is shown in Figure 1.5.

1.5.1 Summary of Features

The COMET board provides the following features:

- Four independent 12 bit, low power sampling A/D converters with true sampling rates of 2 or 5 MHz.
- 512KB of SRAM buffer memory (128KB per channel).
- Storage of up to 64,000 samples per channel.
- Four single-ended inputs.
- Dual-ported data buffers which appear as VMEbus memory to host CPU.
- Continuous or synchronous sequencing.
- Independent or multi-board synchronizing.
- Delayed triggering capability.
- Inputs routed fromboth front panel and VME P2 connectors.
- Jumper selectable input ranges:

  2 MHz. = 0-10 Volts, or +/- 5 Volts.
  5 MHz. = +/- 1 Volt

- Jumper selectable 50 Ohm terminators for each input.

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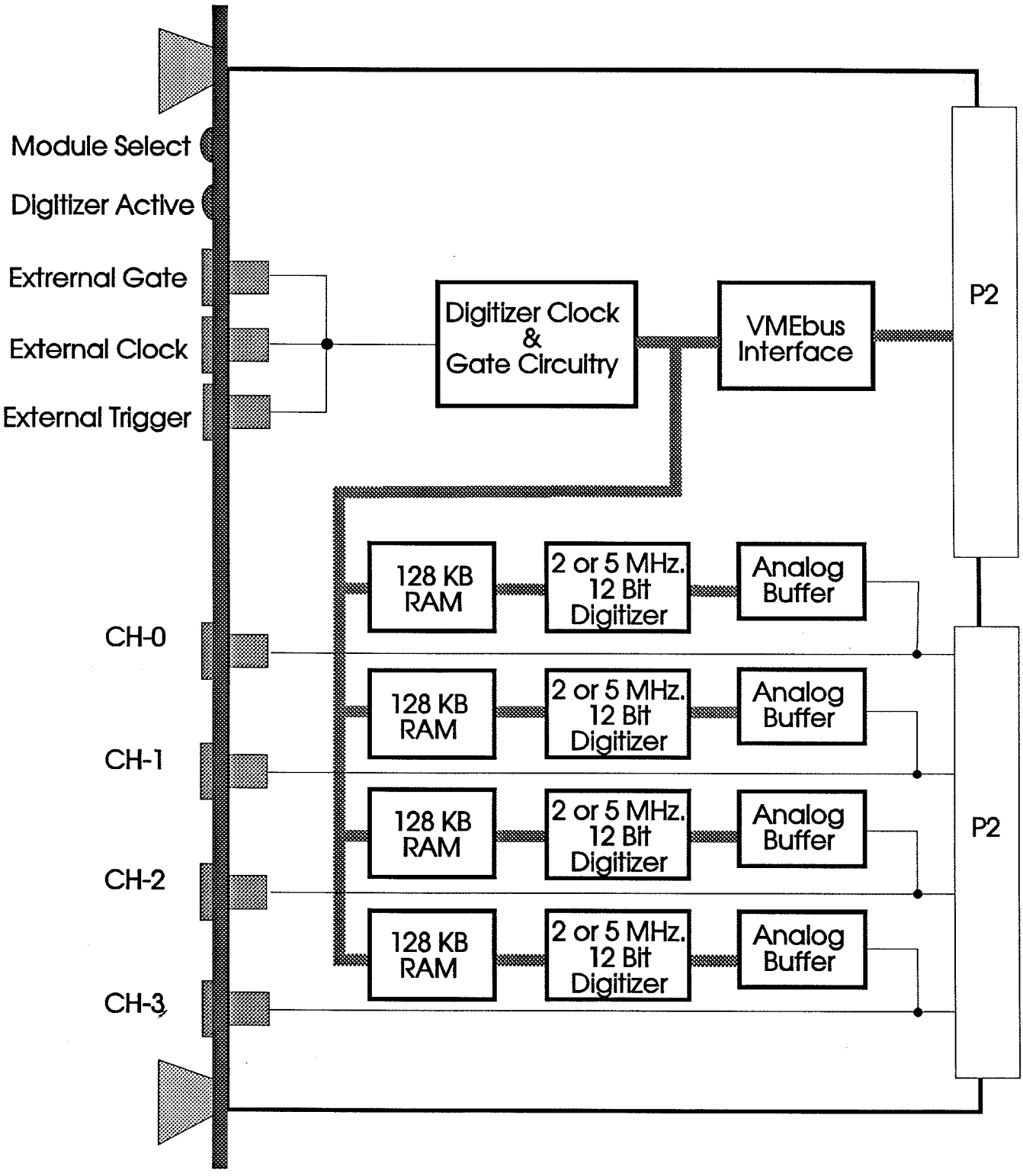


FIGURE 1.5 BLOCK DIAGRAM OF THE COMET ANALOG DIGITIZER

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2.0 GENERAL DESCRIPTION OF THE COMET

The Comet is an intermediate speed, 4-channel waveform digitizer designed to fill the niche between kilocycle data acquisition devices, and powerful sampling oscilloscopes.

The Comet conforms to the VMEbus (IEEE 1014) Specification (REVISION C.1). The Comet can digitize and store analog signals up to 5 Mega-samples per second. Three Modes of operation are available on the Comet, they are:

1. Trigger Mode: A preset number of Memory locations are filled after each input trigger.
2. Circular Mode: Continuous wrap-around filling of Memory with samples.
3. One-Shot Mode: First trigger starts the digitizing, additional triggers ignored.

Each of the Modes of Operation may utilize the deskewing mechanism which provide the input signals time to stabilize before the sample is taken.

The Comet is a dual-ported VMEbus Slave Board that occupies 512KB of VMEbus Memory Space, and 256 bytes of VMEbus Short I/O Space. The Comet utilizes four cost-effective Datel 12 bit, low power A/D Converters (ADS-117 = 2 MHz, ADS-118 = 5 MHz). Each of the Comet's four channels has a 128KB deep Memory (for a total of 512KB). The 16-Bit samples from each of the four channels can be stored in either overwrite, sequential or circular buffer mode, for optimal flexibility. The number of parallel channels sampled can also be easily and cost effectively increased by linking several Comets to a common external trigger and/or Clock.

The Comet can be used in any VMEbus system for applications that require an intermediate speed waveform digitizer. The Comet can also be used for any application that requires a correlation of events to one another in real time, across a number of channels. Examples include transient, vibration or other general purpose waveform analysis as used in industrial instrumentation, or more specialized medical instrumentation and high speed data acquisition systems.

A clarification of terms is as follows:

Bandwidth: The range of frequencies able to pass through the input buffers without undue distortion or loss of signal strength.

Sample Rate: How many samples are taken per second of the input signal. Events may be over-sampled or under-sampled.

Examples: An input signal may have a bandwidth of 1000 Hz. and is sampled at 10,000 samples per second (over-sampling of event). An input signal may have a bandwidth of 5 MHz. and be sampled at 2 MHz (under-sampling event).

Control Registers: The COMET has eight Control Register that configure the functions of the digitizer.

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Gate Duration Counter Register: A register that contains the number of Memory Locations that are filled per trigger event.

Location Counter Register: A register that contains a value that when multiplied by two, is the Address of the next Memory Location to be filled by the digitizer (ie: LCR value * 2 = next Memory Address in COMET RAM to be filled with data). This register is not alterable once the COMET is armed.

Auto-Reset Function: A function that Resets the Location Counter each time a Trigger is received (overwrite storage).

Overwrite Storage: Each time the Comet is triggered to start digitizing, the Location Counter is Reset to its start value. This results in each event (trigger) overwriting the previous event.

Sequential Storage: The storage address is incremented for each sample taken. This refers to per Channel Memory area and not the whole Comet Memory. For example, Channel 0, 1, 2 and 3 each start at Memory location $0, $20000, $40000 and $60000 respectively. This is where the first sample would be stored. In the sequential storage mode, the next sample would be stored in the sequential address location of each Channel (ie: at $2, $20002, $40002 and $60002 respectively).

Truncated Event: This non-standard function occurs if a trigger has started a digitizing event (current event), but has not yet finished (ie: the Gate Duration Counter has not timed out) and another trigger is delivered. The current digitizing event will stop (abort) and a new digitizing event will start.

Trigger Mode: In this Mode digitizing begins at the External Clock Rate or at the Selected Internal Rate following a trigger and fills a number of Memory locations specified by the user. Events may be sequentially stored, but once Memory has been filled, digitizing will stop. Section 2.2.2 will give details regarding this function.

Circular Buffer Storage Mode: This is a continuous storage Mode where the storage address is incremented for each sample taken until a Trigger is received. When the end of Memory is reached, the Location Counter will Reset and storage will continue at the start of Memory again - overwriting any previous digitized data (as opposed to the Trigger Mode where once Memory has been filled, digitizing will stop). Section 2.1.3 will give details regarding this function.

One-Shot Mode: In this Mode only the first trigger received will start a digitization, subsequent triggers are ignored (as opposed to the Trigger Mode which will re-trigger and digitize again and again with each additional trigger received). Section 2.1.2 will give details regarding this function.

Deskewing Mode: This feature delays the start of sampling for some time after the trigger is received to allow for input signal stabilization. See section 2.2 for details.

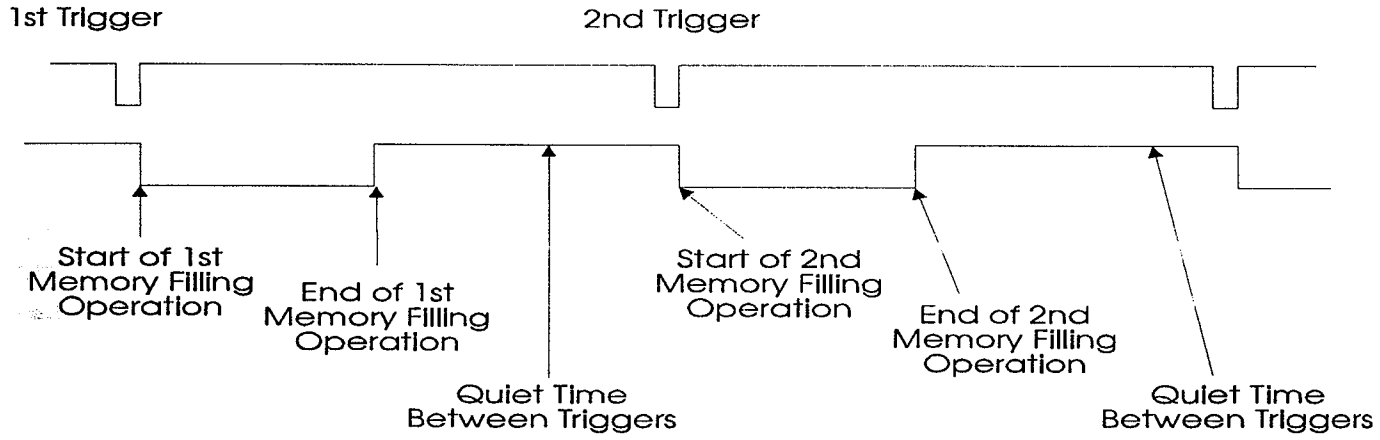
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2.1 Modes of Operation

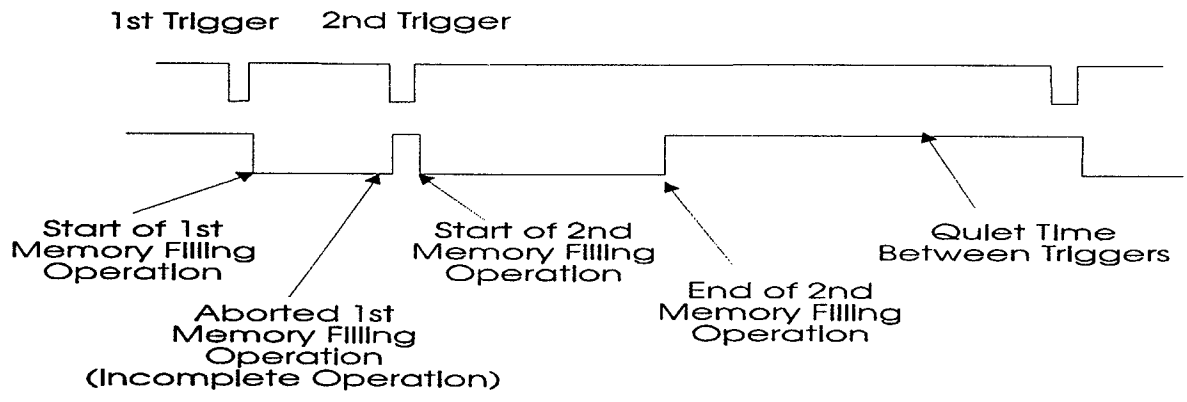
Several operating modes are possible with the Comet. Each of them is defined by configuring the Control Registers as per section 3.4. The Trigger Mode of Operation is described first followed by a description of the One-Shot Mode followed by a description of the Circular Mode of Operation.

2.1.1 Trigger Mode:

In the Trigger Mode, digitizing begins at the External Clock Rate or at the Selected Internal Rate following a trigger and fills a number of Memory locations. Each of the four Input Channels operates simultaneously, but digitizes its own input (ie: a common trigger signal is used to start the four Channels digitizing at the same time). The Location Counter Register sets the starting address where the data is stored in Memory and the Gate Duration Register controls the number of samples to be stored per trigger. Standard operation of the Trigger Mode would be to set the Gate Duration Counter for the number of samples to be stored per trigger event with each trigger input timed so that each trigger event completely fills this amount of Memory (see diagram below).



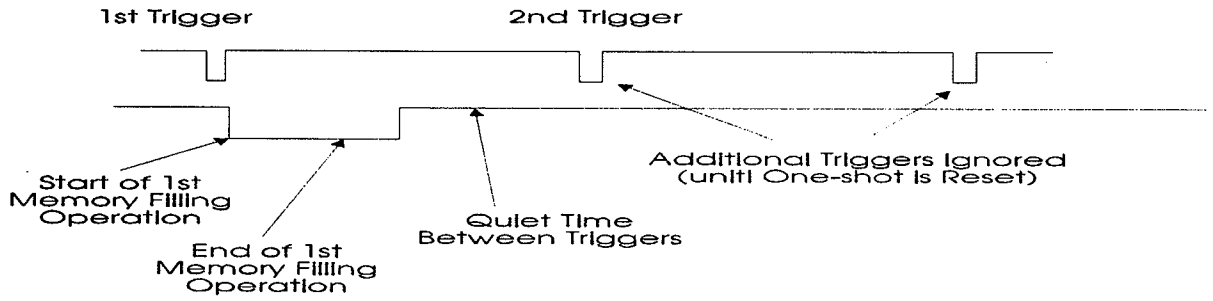
A "Non-Standard Operation" of the Trigger Mode would be if the Gate Duration Counter was set for a number of samples to be stored per trigger event, but a another trigger input arrives before the previous trigger event completely filled the amount of Memory set by the Gate Duration Counter. The 2nd trigger will abort (truncate) the previous trigger operations and start immediately with its own operation (see diagram below).



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2.1.2 One-Shot Mode:

The One-Shot Mode is similar to the Trigger Mode of operation where digitizing begins at the External Clock Rate or at the Selected Internal Rate following a trigger and fills the number of Memory locations (setup by the Gate Duration Register). The One-Shot Mode, however, will trigger and digitize once and only once when the first trigger signal is received, whereas the Trigger Mode will re-trigger and digitize again and again with each additional trigger received. To re-arm the One-Shot requires re-setting the control registers. The Auxiliary Control Register is used to select the One-Shot Mode, Location Counter Register determines where the data is stored sequentially in Memory and the Gate Duration Register controls the number of Memory locations to be filled.

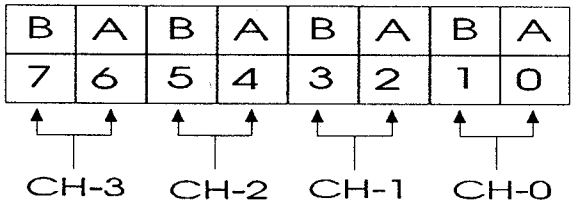


2.1.3 Circular Buffer Mode:

This Mode starts the digitizer continuously fill Memory until it is stopped by a trigger. The number of conversions after the trigger is received is controlled via the Gate Duration Register. This Mode allows the capture of data both before and after a trigger, and the trigger may be located at any point within the captured data set. When operating in the Circular Buffer Mode, the Wrap-Around function bit must be set in the Control Status Register (CSR-H). Conversions start as soon as this Mode is enabled. The user can first set the starting Memory location with a known pattern and can then verify if a total wrap has occurred (ie: This insures the users that all the data prior to the Trigger is in fact new data and not left over data from a previous conversion).

2.2 Deskewing Option

Some operations require no delay and the four Channels can all be triggered at Internal Digitize Clock time where the four channels will trigger simultaneously. Requiring all four channels to convert each time keeps digital noise from one channel from affecting the conversion of other channels. If skewing is required, the Channel Delay Register (CDR) can be employed to set each Input Channel to a delay period. (from 0 to 4 delay periods). Shown below is the bit assignment and example usage of the CDR.



CH-0	CH-1	CH-2	CH-3
D0 = A	D2 = A	D4 = A	D6 = A
D1 = B	D3 = B	D5 = B	D7 = B

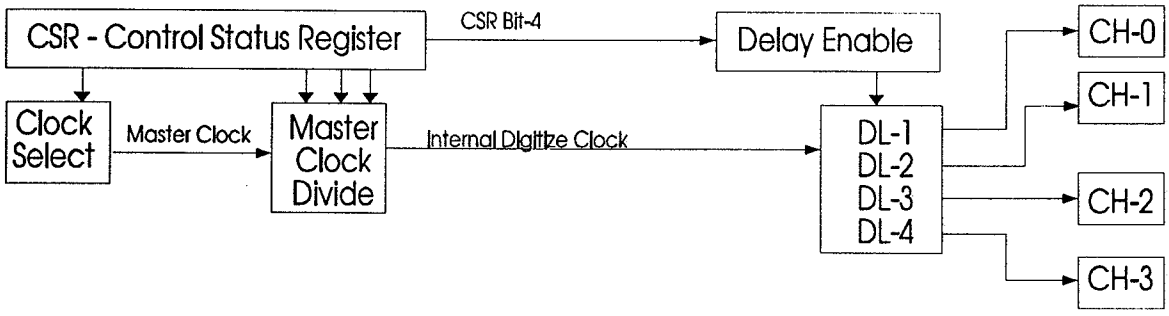
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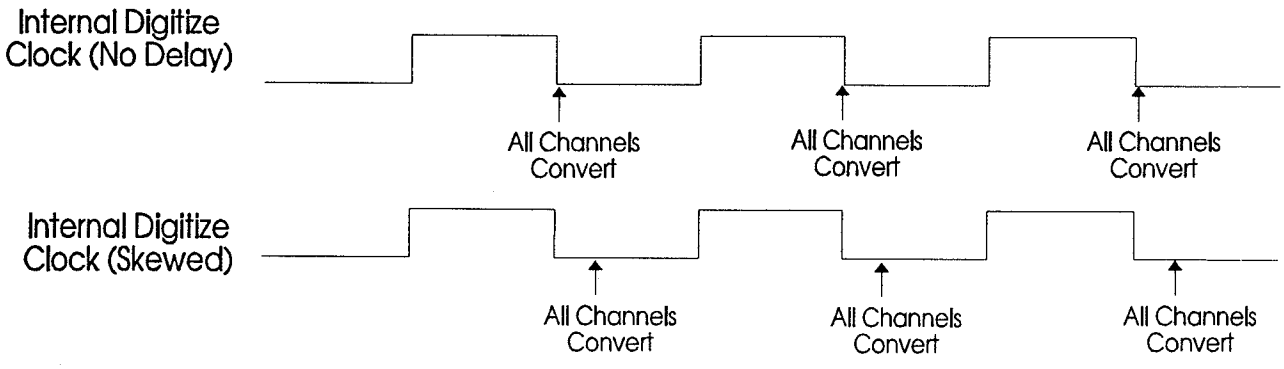
Four Channels Skewed Digitizer Type Selection		
Rate	Digitizer P/N	Sampling Period (Skewed Timing)
2 MHz	ADS-117	0.125 us.
5 MHz	ADS-118	0.050 us.

Channel Delay Register		
B	A	Delay Periods
0	0	1
0	1	2
1	0	3
1	1	4

Example of non staggered (ie: same delay for each Input Channel) delay operation: (Assume Short I/O Base Address is $A000.)

```
Move.b #$E4,$A006 ; A VMEbus Master Writes to the CDR.
                  ; Ch-0 = 1 Delay Period.
                  ; Ch-1 = 2 Delay Period.
                  ; Ch-2 = 3 Delay Period.
                  ; Ch-3 = 4 Delay Period.
```

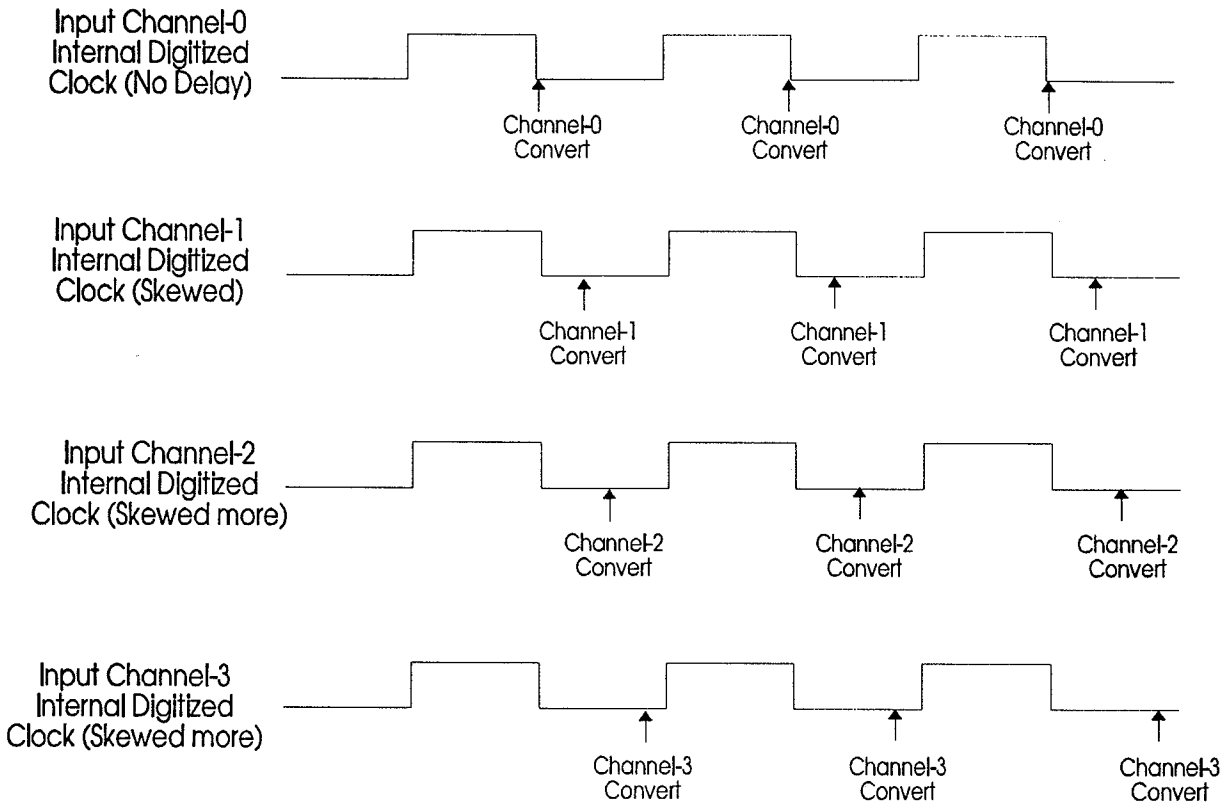


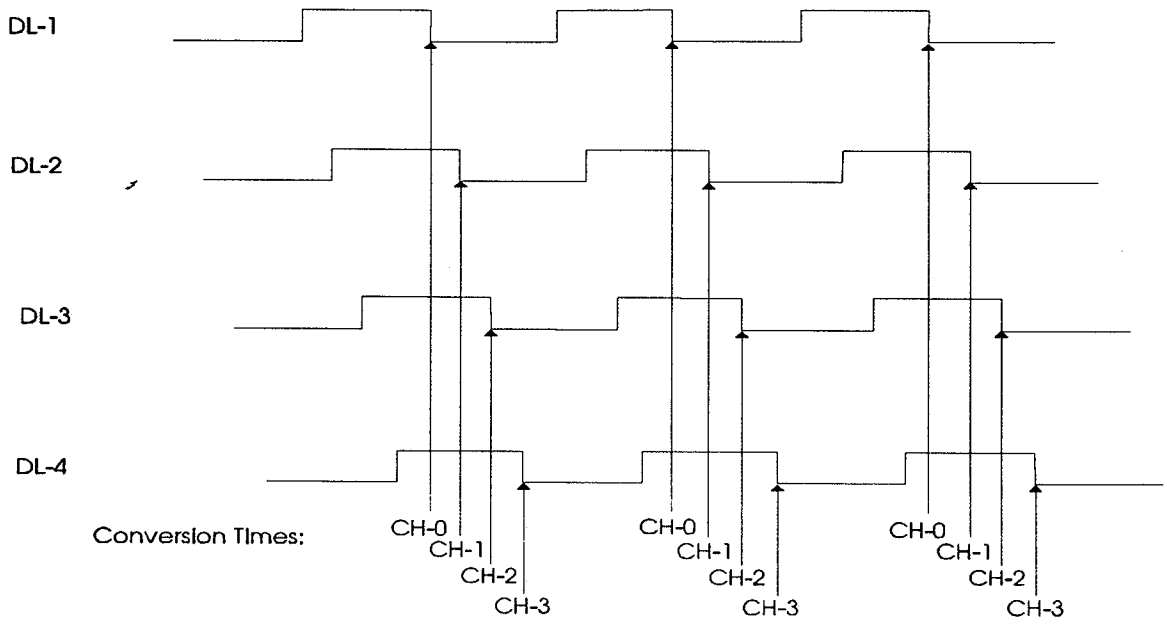


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Example of staggered (ie: different delays for each Input Channel) delay operation:
(Assume Short I/O Base Address is $A000.)

```
Move.b #$FF,$A006        ; A VMEbus Master Writes to the CDR
```

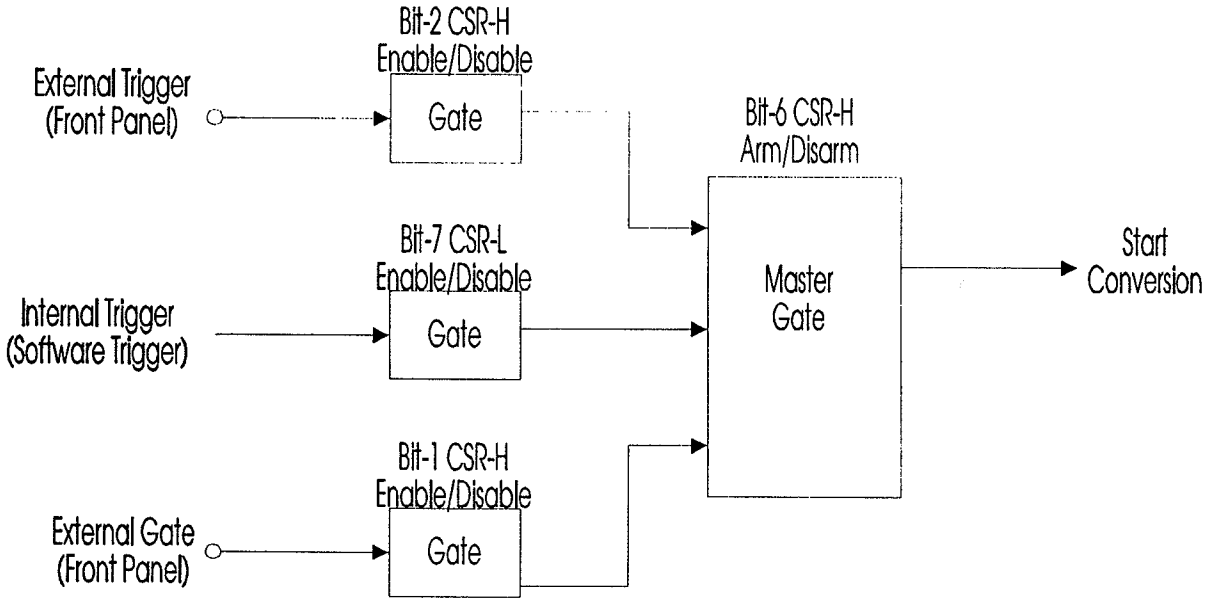




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2.3 Trigger & Gate Inputs:

The Front Panel has two inputs that are used to control starting and stopping the COMET Digitizer. The Trigger signal can be either an Internal Trigger (a software generated trigger) or an External Trigger (via the Front Panel connector). The External Gate signal is supplied to the COMET via Front Panel Connector. Section 2.3.1 details the Internal Trigger function; Section 2.3.2 details the External Trigger; Section 2.3.3 details the External Gate signal. As shown below, the source selected to start the conversion is accomplished by enabling/disabling gates via the CSRs (Control/Status Registers).



2.3.1 Internal Trigger (Software generated):

The Internal Trigger starts a digitizing event when Bit-7 of the CSR-L (Control & Status Register) is set to a "1". The Comet must be Armed and the External Trigger disabled (via the CSR-H Register) for the Internal trigger to be active. For example in the Trigger Mode, the digitizing sequence will stop when the Gate Duration Counter counts down to zero (ie: the Gate Duration Counter is configured for the number of samples per trigger event the user desires). The Circular Buffer Mode starts digitzing when selected and can be Triggered to stop via this Internal Trigger. The Trigger Mode, the One-Shot Mode, the Non-Standard Mode and the Circular Buffer Mode are supported. Basically, the Internal Trigger (Software Trigger) has the same function as the External Trigger (Front Panel).

```
Example:    Move.b #$40,$Base_Address      ; Arm Digitizer, External Trigger Disabled.
            Move.b #$82,$Base_Address+1    ; Will trigger a conversion with sample rate
                                           ;   of 1 MHz.
```

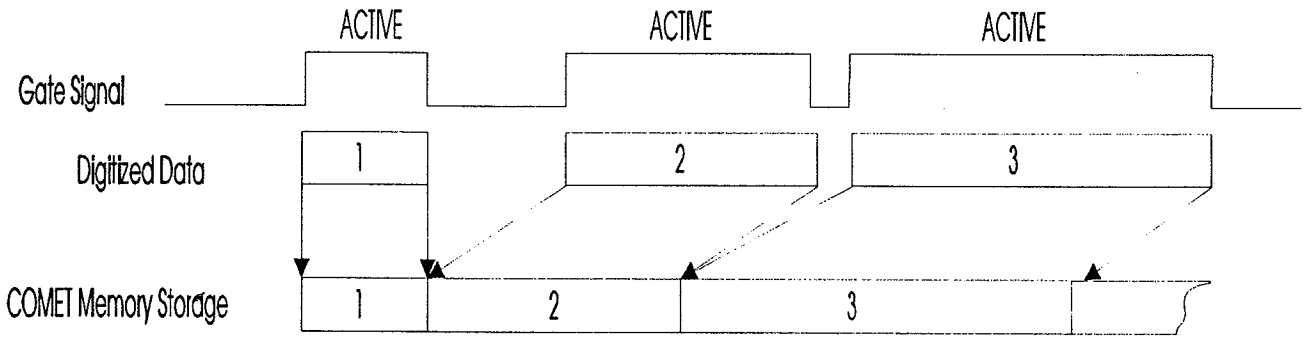

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2.3.2 External Trigger (Front Panel Connector):

The External Trigger starts a digitizing event when Bit-2 of the CSR-H (Control & Status Register) is set to a "1" and the rising edge of a trigger pulse is supplied to the Front Panel Connector. The Comet must be Armed and the Software Trigger disabled (via the CSR-L Register) for the External trigger to be active. For example in the Trigger Mode, the digitizing sequence will stop when the Gate Duration Counter counts down to zero (ie: the Gate Duration Counter is configured for the number of samples per trigger event the user desires). The Circular Buffer Mode starts digitzing when selected and can be Triggered to stop via this External Trigger. The Trigger Mode, the One-Shot Mode, the Non-Standard Mode and the Circular Buffer Mode are supported. Basically, the External Trigger has the same function as the Software (Internal) Trigger.

2.3.3 External Gate (Front Panel Connector):

The External Gate signal acts as both a trigger for starting the conversions and as the duration timer (ie: the External Gate signal acts like the External Trigger (see above section) and also acts as the Gate Duration Counter that stops the conversions). This provides a mechanism where the digitizing event can be of variable length via a control signal as shown below. The digitized data is sequentially added to Memory with each new Gate assertion the new digitized data is appended to the previous events data. If Auto-Reset is employed, only the first Auto-Reset will work (ie: the Location Counter will re-zero only the first time the Auto-Reset is asserted; subsequent resets will be ignored and digitized data will be sequentially stored (appended) in Memory.



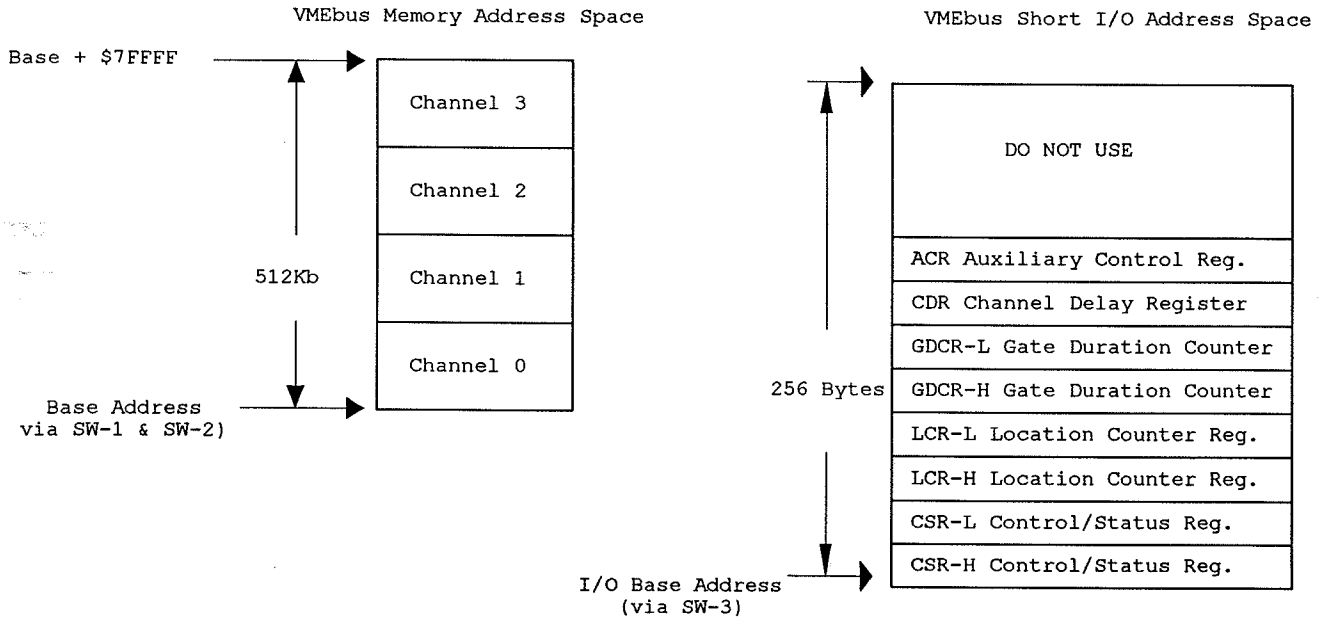
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3.0 COMET DIGITIZER MEMORY MAPPING

This section describes the VMEbus Addressing, the On-Board RAM Memory Addressing and the On-Board Control/Status Registers of the COMET Board.

3.1 COMET Digitizer VMEbus Memory Map

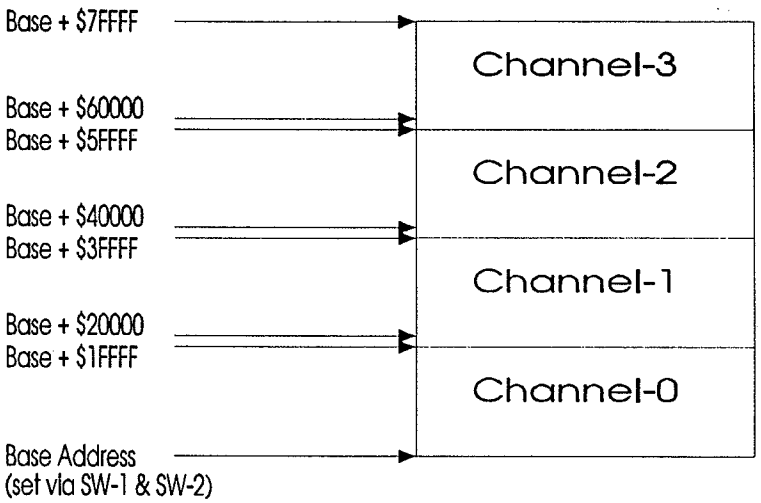
The Comet Digitizer Board takes up 512KB of VMEbus Memory Address Space and 256 Bytes of VMEbus Short I/O Address Space. The VMEbus Memory Address Space occupied by the Comet Board consist of four blocks of Read/Write RAM Memory. The Control Registers of the Comet Board reside in the VMEbus Short I/O Address Space and occupy eight consecutive Bytes of Memory (the remaining space is not used). The following section will discuss the RAM Memory. Next a detailed look at the Control Registers will be presented. Figure 1.5 shows a Block Diagram of the Comet Board. Below is a diagram of the Memory Map of the Comet Digitizer Board. See section 4.1 for configuration of VMEbus Base Address.



3.2 Comet RAM Memory Mapping

Each of the four A/D Converters is allocated 128K Bytes of RAM Memory. With the Start of Conversion, each A/D device loads the converted values into it's own bank of RAM. After conversion is completed, the RAM can be Read by any VMEbus Master as a contiguous block of 512K Bytes of VMEbus Memory. Both Byte and Word accesses from the VMEbus are supported with the VMEbus Memory Space Address set by DIP Switches SW-1 & SW-2 (see section 4.1 for switch set-up). The data Read by the VMEbus is with Channel 0 starting at the Base Address and ending 128K Bytes ($1FFFF hex) later. Channel 1 starts at Base Address plus $20000 and ends 128K Bytes later at Base Address plus $3FFFF. Channel 2 starts at Base Address plus $40000 and ends 128K Bytes later at Base Address plus $5FFFF. Channel 3 starts at Base Address plus $60000 and ends 128K Bytes later at Base Address plus $7FFFF.

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```
Example: To test Comet RAM Block via a VMEbus Master.

       Move.l #$Base_Address,A0          ; Load the Address of the Comet Board.
       Move.l #$Base_Address+$7FFFF,A1   ; End of Comet RAM.
Test   Move.b #$55,(A0)+                       ; Move test pattern to Comet RAM.
       Cmp.l  A0,A1                      ; Test for End of Comet RAM.
       BNE    Test                             ; Not done ?

       Move.l #$Base_Address,A0          ; Reload the Address of the Comet Bd.
Check Move.b (A0)+,D0                          ; Read Comet RAM.
       Cmp.l A0,A1                             ; Done with testing ?
       BEQ   Done                              ; Jump to Done if finished.
       Cmp.b  #$55,D0                          ; Check value read.
       BEQ   Check                             ; Value ok ?
       BNE   ERROR                             ; Jumper to Error if value is bad.


Example: To test Channel-2 RAM block via a VMEbus Master.

       Move.l #$Base_Address+40000,A0    ; Load the Base Address of the Channel-2.
       Move.l #$Base_Address+$5FFFF,A1   ; End of Channel-2 RAM Block.
Test   Move.b #$55,(A0)+                       ; Move test pattern to Comet RAM.
       Cmp.l  A0,A1                      ; Test for End of Comet RAM.
       BNE    Test                             ; Not done ?

       Move.l #$Base_Address+40000,A0    ; Reload Address of Channel-2 RAM Block.
Check Move.b (A0)+,D0                          ; Read Channel-2 RAM Block.
       Cmp.l A0,A1                             ; Done with testing ?
       BEQ   Done                              ; Jump to Done if finished.
       Cmp.b  #$55,D0                          ; Check value read.
       BEQ   Check                             ; Value ok ?
       BNE   ERROR                             ; Jumper to Error if value is bad.
```

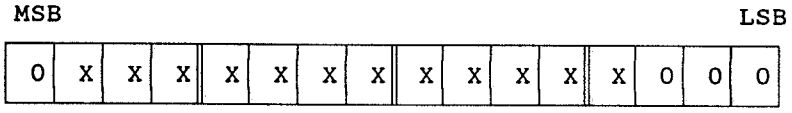
NOTE: When digitizing, sequential storage is utilized. The storage address for each Channel is incremented for each sample taken. This refers to per Channel Memory area and not the whole Comet Memory. For example, Channel 0, 1, 2 and 3 each start at Memory location $0, $20000, $40000 and $60000 respectively. This is where the first sample would be stored. The next sample would be stored in the sequential address location of each Channel (ie: at $2, $20002, $40002 and $60002 respectively).

The Comet Memory is from Base Address + 0 to Base Address + $7FFFF. Reading from Base Address + 0 to Base Address + $40000 is not reading Half the samples, but rather only reading the samples from Channel-0 & Channel-1 Memory (see above diagram and note the addresses for the Channels).

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3.3 COMET Digitizer Data Format

The following figure shows the data format when Reading the digitized data where 0 is a constant value and X is the digitized value (the Datel A/D devices are 12 Bit devices):



3.4 COMET Control Register Mapping

The eight Control Registers are detailed in the following sections.

CSR-L (8-Bits)	= Control & Status Register - Low	Section 3.4.1
CSR-H (8-Bits)	= Control & Status Register - High	Section 3.4.1
ACR (8-Bits)	= Auxiliary Control Register	Section 3.4.2
CDR (8-Bits)	= Channel Delay Register	Section 3.4.3
LCR-L (8-Bits)	= Location Counter Register - Low	Section 3.4.4
LCR-H (8-Bits)	= Location Counter Register - High	Section 3.4.4
GDCR-L (8-Bits)	= Gate Duration Counter Register - Low	Section 3.4.5
GDCR-H (8-Bits)	= Gate Duration Counter Register - High	Section 3.4.5

These registers are accessed by VMEbus Masters at the VMEbus I/O Space Address set by the 8-bit DIP Switch (SW-3, see section 4.1.1 for switch set-up). All Control Registers are accessed in the Byte Mode (Word Mode not supported for Control Register accesses). CSR-L and CSR-H are bit-significant registers that select the operating characteristics of the board. CDR is a register that is used to allow for skewing of the input signal samples. LCR-L and LCR-H are pointers to the next data sample location to be filled with the digitizer data. GDCR-L and GDCR-H hold the number of conversions to be performed following a Trigger event. The ACR is a bit-significant register that selects some modes of operation. The COMET registers and their Address offsets are:

CSR-H	= Control & Status Register - High Byte	= I/O Base Address + $0
CSR-L	= Control & Status Register - Low Byte	= I/O Base Address + $1
LCR-H	= Location Counter Register - High Byte	= I/O Base Address + $2
LCR-L	= Location Counter Register - Low Byte	= I/O Base Address + $3
GDCR-H	= Gate Duration Counter Register - High Byte	= I/O Base Address + $4
GDCR-L	= Gate Duration Counter Register - Low Byte	= I/O Base Address + $5
CDR	= Channel Delay Register	= I/O Base Address + $6
ACR	= Auxiliary Control Register	= I/0 Base Address + $7

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ACR = Auxiliary Control Register	Byte	(7)	Base Address + 7
CDR = Channel Delay Register	Byte	(6)	Base Address + 6
GDCR-L = Gate Duration Counter Register	LOW Byte	(5)	Base Address + 5
GDCR-H = Gate Duration Counter Register	HIGH Byte	(4)	Base Address + 4
LCR-L = Location Counter Register	LOW Byte	(3)	Base Address + 3
LCR-H = Location Counter Register	HIGH Byte	(2)	Base Address + 2
CSR-L = Control & Status Register	LOW Byte	(1)	Base Address + 1
CSR-H = Control & Status Register	HIGH Byte	(0)	Base Address + 0

3.4.1 Control & Status Registers (CSR-L CSR-H)

The Control-Status Registers (CSR-L & CSR-H) can be accessed from the VMEbus as a D8 (Byte) Module. The contents of these bit-significant Registers select the operating characteristics of the board, as defined below:

CSR-H = Control & Status Register - High Byte ; I/O Base Address (Byte Access)
CSR-L = Control & Status Register - Low Byte ; I/O Base Address + $1 (Byte Access)

CSR-H

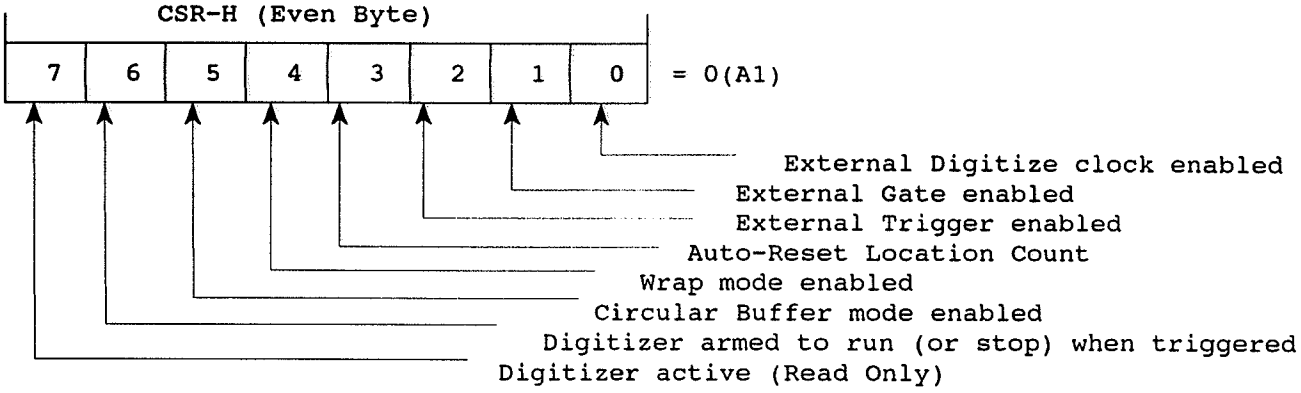
```
Bit 7:  1 = Digitizer active (Status)     0 = Inactive (Status Indicator)
Bit 6:  1 = Digitizer armed to run        0 = Stop when Triggered
Bit 5:  1 = Circular Buffer enabled       0 = Circular Buffer disabled
Bit 4:  1 = Wrap mode enabled             0 = Wrap mode disabled
Bit 3:  1 = Auto-Reset Location Count     0 = Auto-Reset Counter disabled
Bit 2:  1 = External Trigger enabled      0 = External Trigger disabled
Bit 1:  1 = External Gate enabled         0 = External Gate disabled
Bit 0:  1 = External Clock enabled        0 = External Clock disabled
```

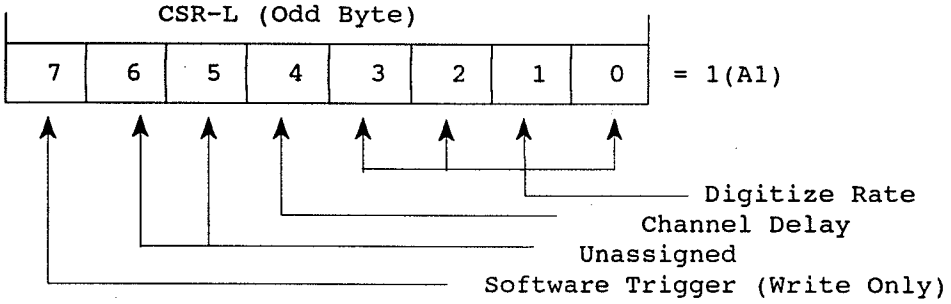
CSR-L

```
Bit 7:   Software Trigger (Writing a '1' causes a Trigger)
Bit 6-5: Unassigned
Bit 4:   1 = Channel Delay Enable          0 = Channel Delay Disabled
Bit 3-0: Digitize Rate Selector
```

D7	D6	D5	D4	D3	D2	D1	D0	CSR-H
D7	D6	D5	D4	D3	D2	D1	D0	CSR-L

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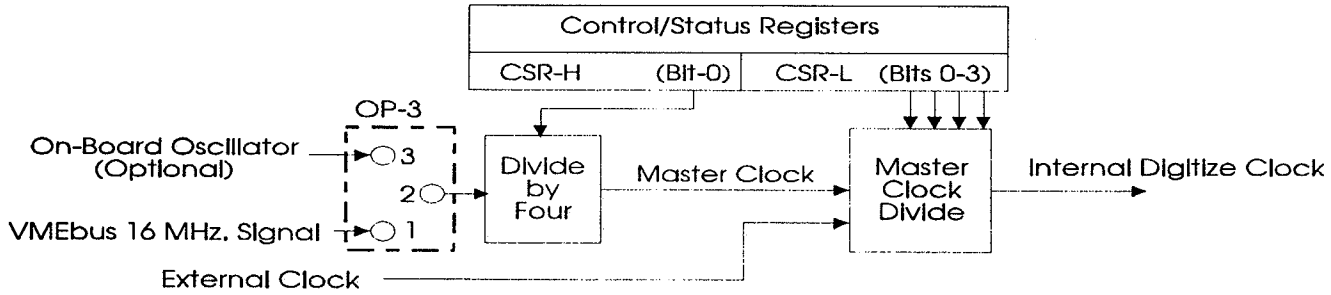



```
Example: (Assume Short I/O Base Address is $A000.)

   Move.b #$7F,$A000 ; A VMEbus Master Writes a $7F to the CSR-H
                     ; (High Byte Access).
   Move.b #$1F,$A001 ; A VMEbus Master Writes a $1F to the CSR-L (Low Byte Access).
```

CSR-L Bit Assignments:

Bits 0 - 3: These four bits are used to divide the Master Clock down to derive the *Internal Digitize Clock*. The Master Clock is either from On-Board sources selected by Option OP-3 (ie: the VMEbus 16 MHz Bus Clock or an Optional On-Board 20 MHz. Oscillator) or from an External source (the External Clock signal via a front panel connector). The On-Board sources are first sent to a divide by four circuit before being sent to the Master Clock Divide circuit. Bit-0 of the CSR-H selects the Master Clock source while Bits 0 thru 3 of the CSR-L control the 16-bit divider. Any one of the sixteen binary related frequencies can be selected as the digitize rate.



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DIGITIZE RATE FOR ADS-117 DEVICE (0.5 us Sampling Period)			
Bits 0 - 3	Digitize Rate	Bits 0 - 3	Digitize Rate
0000 ($0)	----------	1000 ($8)	15.625 KHz.
0001 ($1)	2 MHz.	1001 ($9)	7.813 KHz.
0010 ($2)	1 MHz.	1010 ($A)	3.906 KHz.
0011 ($3)	500 KHz.	1011 ($B)	1.953 KHz.
0100 ($4)	250 KHz.	1100 ($C)	976.563 Hz.
0101 ($5)	125 KHz.	1101 ($D)	488.281 Hz.
0110 ($6)	62.6 KHz.	1110 ($E)	244.414 Hz.
0111 ($7)	31.25 KHz.	1111 ($F)	122.070 Hz.

DIGITIZE RATE FOR ADS-118 DEVICE (0.2 us Sampling Period)			
Bits 0 - 3	Digitize Rate	Bits 0 - 3	Digitize Rate
0000 ($0)	----------	1000 ($8)	15.625 KHz.
0001 ($1)	2 MHz.	1001 ($9)	7.813 KHz.
0010 ($2)	1 MHz.	1010 ($A)	3.906 KHz.
0011 ($3)	500 KHz.	1011 ($B)	1.953 KHz.
0100 ($4)	250 KHz.	1100 ($C)	976.563 Hz.
0101 ($5)	125 KHz.	1101 ($D)	488.281 Hz.
0110 ($6)	62.6 KHz.	1110 ($E)	244.414 Hz.
0111 ($7)	31.25 KHz.	1111 ($F)	122.070 Hz.

(Above Tables assumes the 16 MHz. VMEbus Clock is used.)

```
Examples:   Move.b #$02,$Base_Address + 1 ; Configure CSR-L for 1 MHz. sample
                                          ; rate (Byte Access).

            Move.b #$03,$Base_Address + 1 ; Configure CSR-L for 500 KHz. sample
                                          ; rate (Byte Access).
```

Bit 4: This bit enables or disables the *Deskewing Option*. It is assumed that all four Channels will be digitized at each Clock event. When enabled by writing a "1" to Bit-4, the Clock Pulses to each Channel can be delayed to accommodate skew in the input signals. When disable by writing a "0", no delay will be introduced. See section 2.2 for usage of the Deskewing Function.

Bits 5 - 6: These bits are unassigned at this point.

Bit 7: Writing a "1" to Bit-7 of the CSR-L will issue a *software generated "trigger"* signal. The Comet must be Armed (Bit-14) and the External Trigger (Bit-10) disabled for this trigger to be asserted.

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```
Example:    Move.b #$40,$Base_Address      ; Arm Digitizer, External Trigger Disabled.

            Move.b #$92,$Base_Address+1    ; Will trigger a conversion with sample rate
                                           ; of 1 MHz.
```

CSR-H Bit Assignments:

Bit 0: This bit selects the *Source for the Master Clock* from either the External Clock Input (via the Front Panel) or the On-Board Clock Inputs (16 MHz. from VMEbus/On-Board 20 MHz. Oscillator). This Master Clock is divided down (via Bits 0 thru 3 of CSR-L) and becomes the Internal Digitizing Clock. If no delays are needed to skew the input signals, the four Channels can all be triggered at the Internal Digitize Clock time. If delay is required to allow for skewing then see section 2.2 for details regarding the CDR (Channel Delay Register).

Bit 1: When this bit is a "1", it enables the use of a "continuous trigger mode" (as opposed to a pulsed start-conversion trigger) where the Comet will continuously sample the input for as long as the input Gate Signal is asserted. The *Gate Trigger* is asserted via the Front Panel connector.

Bit 2: When this bit is a "1", it enables the use of the Front Panel "pulsed trigger" (as opposed to a gate trigger) where the Comet will start sampling the input until terminated either by another trigger (Circular Buffer Mode) or the Gate Duration Counter Register (Trigger Mode). The *External Trigger* is asserted from the Front Panel connector. When this bit is a "0", the External Trigger is disabled.

Bit 3: This bit enables/disables the *Auto-Reset Location Count*. When this bit is a "1", the Auto-Reset Location Count is enabled which Resets the Location Counter Register each time another trigger is received, over writing any previous data collected. Clearing this bit to a "0" will disable the Auto-Reset Location Count and each new trigger will store it's data sequentially in Memory. The Wrap Bit (Bit-12) determines if successive triggers will "wrap around" from the end of Memory to the beginning again or stop sampling, ignoring any further triggers. LCR-L and LCR-H should not be written to in this mode.

Bit 4: This bit enables/disables the *Wrap-Around* function. When in the Trigger Mode with the Auto-Reset disabled (ie: the data from each new trigger is stored sequentially in each Channels' Memory Space), the user has the option to stop collecting data when Memory is full and ignore any further triggers or Wrap-Around to the beginning of Memory Space and continue to store data. Writing a "1" to this bit enables the Wrap-Around function. Writing a "0" disables the Wrap-Around function.

Notes:

The Memory Space is 128 Kbytes for each Channel. Each Channel Wraps-Around only to it's own beginning address.

In the Circular Buffer Mode, this bit allows the LCR's (Location Counter Registers) to Wrap around (ie: to reset back to zero and continue to count up with each sample). If not enabled, the LCR's will count up to $FFFF and stop. This does not stop the Circular Buffer function (ie: the samples are still taken and routed to the correct Memory space), but only stops the LCR's from Wrapping back to zero and keeping staying in count with the samples.

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Bit 5: This bit enables the *Circular Buffer Mode*. A "1" will select the Circular Mode of operation. A "0" will select the Trigger Mode of operation.

Standard Operaton: Standard Operation is where digitizing begins at the external or the selected rate following a unique trigger and fills the number of Memory locations given by the Gate Duration Register. The Auto Reset bit (Bit-3 of the CSR-H) determines whether the Location Counter is Reset by a trigger event. The Wrap bit (Bit-4 of the CSR-H) determines if the digitizer stops at the end of Memory or wraps around and begins to fill Memory at channel location zero.

Circular Buffer Operation: In this Mode, the digitizer continuously fills Memory and is stopped by a trigger. As in the Standard Operation, the number of conversions that follow the trigger is given by the value stored in the Gate Duration Register. This allows the capture of data both before and after a trigger, and the trigger may be located at any point within the captured data set. Before activating the Circular Mode via setting Bit-5 to a "1", Bit 6 of CSR-H must be set to a "1" to arm the digitizer.

NOTES: *The Circular Buffer Mode must be temporarily stopped if a large block of COMET RAM is to be transferred over the VMEbus. Once the transfer is completed the Circular Buffer Mode can be enabled again with the Location Counter Register starting where it had been stopped.*

A $60 Written to this CSR-H register enables the Circular Buffer Mode, but prevents the LCR's Wrap around function (see Bit-4 Notes). A $70 enables both the Circular Mode and Wrap around for the LCR"s. Values of $20 and $40 will not function properly.

Bit 6: This bit *arms the Digitizer*. When Bit-6 is set to "1", the Comet will be armed and ready to start to digitize. When this bit is cleared to a "0" or disarmed, the Comet will stop digitizing. Once armed, writing to the Location Counter Register is disabled.

Bit 7: This bit is a *Status Indicator* (Read Only) and indicates the state of the DIG. ACT LED on the Front Panel. When the Comet is digitizing, Status Bit-7 will be a "1" and the Front Panel LED will be on. When the Comet is inactive, Status Bit-7 will be a "0" and the Front Panel LED will be off.

```
Example:

   Move.l  #$FFFFA000,A2    ; Assume I/O Base Address of Comet = $A000
   Move.b  #$48,$A000 ; Load CSR-H:
                                Bit-7  = 0 ; Status Bit - Read-Only.
                                Bit-6  = 1 ; Digitizer active.
                                Bit-5  = 0 ; Trigger Mode of Operation.
                                Bit-4  = 0 ; Wrap-Around disabled.

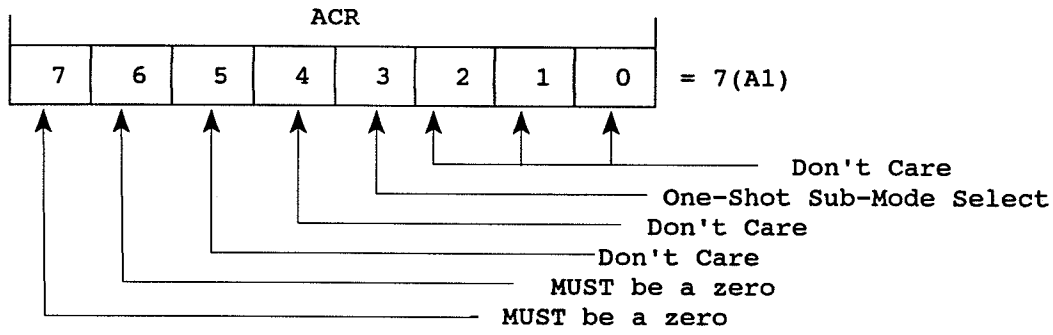
                                Bit-3  = 1 ; Auto-Reset enabled.
                                Bit-2  = 0 ; External Trigger disabled.
                                Bit-1  = 0 ; External Gate disabled.
                                Bit-0  = 0 ; External Clock Disabled.

   Move.b  #$12,$A001 ; Load CSR-L:
                                Bit-7 = 0  ; No Software Trigger.
                                Bit-6 = 0  ; Unassigned.
                                Bit-5 = 0  ; Unassigned.
                                Bit-4 = 1  ; Channel Delay enabled.
                                Bits 3 thru 0 = 0010  ; 1 MHz. Digitize Rate.
```


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The Auxiliary Control Register can be accessed from the VMEbus as a D8 (Byte) Module. The contents of this bit-significant Register selects the operating Modes of the COMET Board, as defined below:

```
CSR-H ─┐ Bit 7:  1 = 0 ; MUST be a zero
       │ Bit 6:  1 = 0 ; MUST be a zero
       │ Bit 5:  don't care
       │ Bit 4:  1 = One-Shot Mode Select     0 = Trigger Mode
       │ Bit 3:  don't care
       │ Bit 2:  don't care
       │ Bit 1:  don't care
       └ Bit 0:  don't care
```

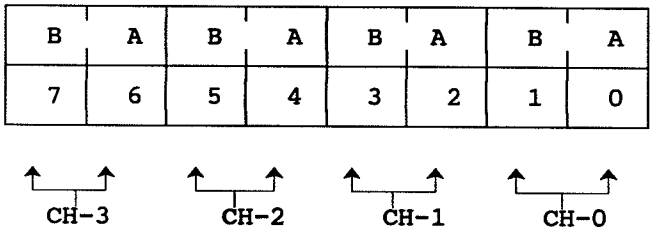


Bit-3 for the One-Shot Mode must be Cleared and Reset before another trigger/sample can be digitized.

3.4.3 Channel Delay Register (CDR)

To allow input signal sampling skewing, Bit-4 of the CSR-L must be set to a "1" and configuration of the CDR - Channel Delay Register - will be required. If no delays are needed, the four Channels can all be triggered at Internal Digitize Clock time where the four channels will trigger simultaneously. Requiring all four channels to convert each time keeps digital noise from one channel from affecting the conversion of other channels.

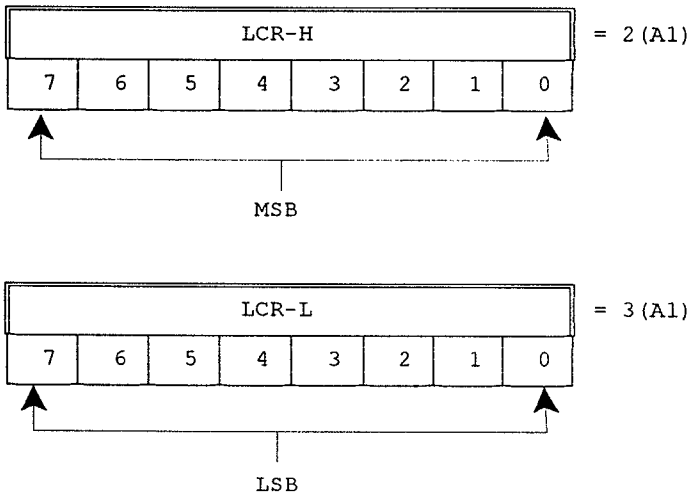
The Channel Delay Register (CDR) is a Byte wide (D8) register. Each Channel can be have it's delay individually set from 0 to 4 delay periods. The standard mode of operation is to have each of the four Channels simultaneously digitize its own input at the same skewed time during each Internal Digitize Clock event. The CDR can also support a staggered mode where each Channel digitizes at a different delay period. The Register is located $6 off the Base I/O Address set via SW-3 (see section 4.1 for details). See section 2.2 for further details. Shown below is the bit assignment of the CDR.



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3.4.4 Location Counter Registers (LCR-L & LCR-H)

These Registers pointer to the next data sample location to be filled with the digitizer data. LCR-H is the MSB (Most Significant Byte of the Pointer) and LCR-L is the LSB (Least Significant Byte of the Pointer). The Registers are accessed in the Byte mode (D8). The LCR-H Register is located $2 off the Base I/O Address and LCR-L is $3 of the Base I/O Address (set via SW-3, see section 3.1.1 for details). If CSR-H bit 3 is a "1" (enabling Auto-Reset Count) then LCR-L and LCR-H should not be written to (however, they may be read). Once armed, writing to the LCR registers is prohibited.




```
Example: (Assume Short I/O Base Address is $A000.)

      Move.b $A002,D0          ; A VMEbus Master Reads LCR-H into
                               ; D0 (High Byte Access).

      Move.b $A003,D1          ; A VMEbus Master Reads LCR-L into
                               ; D1 (Low Byte Access).

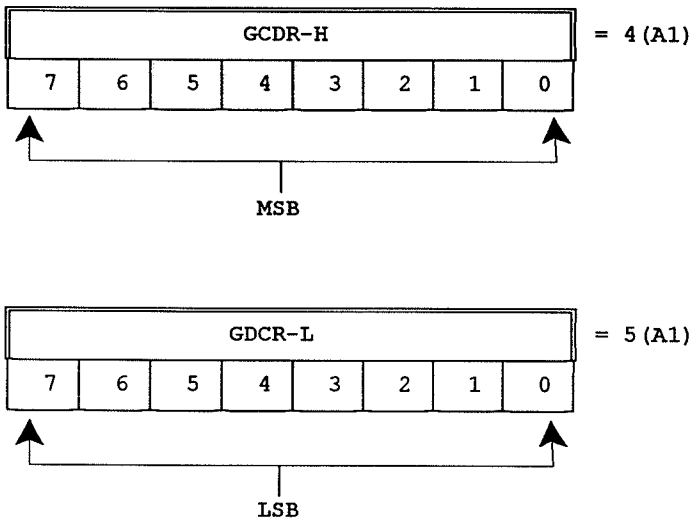
      Move.b #$00,$A002        ; A VMEbus Master Writes to
                               ; LCR-H  (High Byte Access).

      Move.b #$00,$A003        ; A VMEbus Master Writes to
                               ; LCR-L  (Low Byte Access).
```

3.4.5 Gate Duration Counter Registers (GDCR-L & GDCR-H)

The Gate Duration Counter is employed in both the Trigger Mode and the Circular Buffer Mode of Operation. The value contained in the GDCR is the number of conversions stored following a trigger. It is possible to capture data before and after a trigger when used in the Circular Buffer Mode of Operation. GDCR-H being the MSB (Most Significant Byte of the Data) and GDCR-L being the LSB (Least Significant Byte of the Data). These Registers are accessed only in either in the Byte mode (D8). The GDCR-L Register is located $4 off the Base I/O Address and GDCR-H is located $5 off the Base I/O Address (set via SW-3 - see section 4.1 for details).

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```
Example: (Assume Short I/O Base Address is $A000.)

      Move.b #$FF,$A004        ; A VMEbus Master Writes to GDCR-H  (High Byte Access).
      Move.b #$FF,$A005        ; A VMEbus Master Writes to GDCR-L  (Low Byte Access).
```

3.4.6 Initializing the Comet A/D Converters

Upon cold power-up, the Datel A/D Converters internal counters are not synchronized to the outside world. After power-up, the COMET Board should first be initialized with the following routine:

```
INIT  Move.b #$48,CSR-H      ; 0(A1)
      Move.b #$02,CSR-L      ; 1(A1)
      Move.b #$00,LCR-H      ; 2(A1)
      Move.b #$00,LCR-L      ; 3(A1)
      Move.b #$00,GDCR-H     ; 4(A1)
      Move.b #$01,GDCR-L     ; 5(A1)
      Move.b #$00,CDR        ; 6(A1)
```

This routine needs to be executed after a cold power-up condition. Resets issued, either hardware or software, after power-up, will not initialize the Datel devices. However, once initialized, the COMET Board does not have to be re-initialized after Resets (ie: initialization is only required when first powering up the COMET Board).

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4.0 HARDWARE DESCRIPTION

The Comet includes four digitizer-memory channels, the programmable trigger and digitizer clock logic, and the VMEbus interface. This design uses the 12-bit 2 or 5-MHz Datel digitizers with 128KB (64k samples) of memory for each of the four channels. The Comet appears to the bus as a 512KB RAM card with Registers in VMEbus I/O Space for trigger, digitizer clock and gate control. Comet Memory may be accessed from the VMEbus in either Byte or Word modes. Comet Registers may be accessed from the VMEbus in Byte mode only. Provisions are made for using either internal or external triggers, digitizer clocks and gate signals. Connectors on the front panel are provided for the external versions of these inputs.

Analog inputs may be brought onto the board through either the front panel connectors or the rear VMEbus P2 Connector. Jumpers are provided to select termination for each of the input signals. The analog input range is jumper selectable with 2 MHz. devices for 0-10V or +/-5V ranges and the 5 MHz. device for +/- 1 volt range.

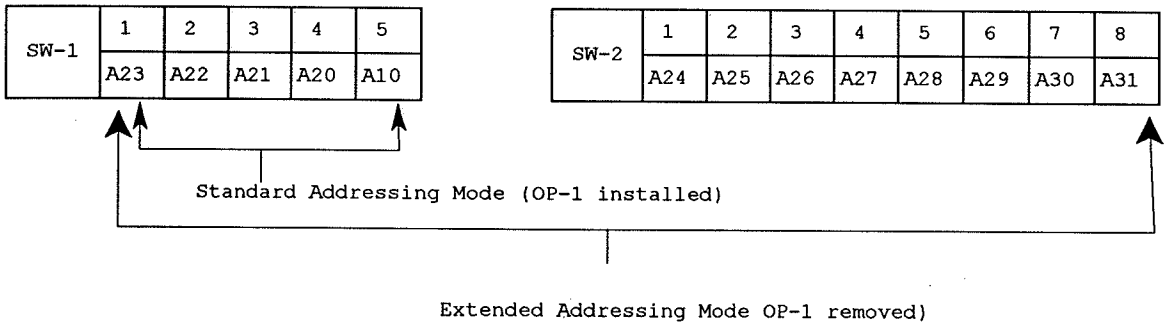
The following sections describe the COMET's hardware and Option jumpers:

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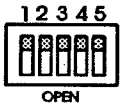
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4.1 Configuring VMEbus Base Address (SW-1, SW-2 & SW-3)

The Comet's 512 KB of RAM is accessed via the VMEbus Memory Address Space via SW-1 and SW-2 as either an A32 or A24 module. Selection between A32 (Extended Addressing) and A24 (Standard Addressing) is accomplilshed via Option OP-1 (see section 3.3.1). If OP-1 is installed, then the A24 Addressing Mode is selected and only SW-1 is active (SW-2 becomes a don't care switch). With OP-1 removed then the A32 Addressing Mode is selected and both SW-1 and SW-2 are active. SW-1 controls the Address Lines A19 thru A23 while SW-2 Controls A24 thru A31.

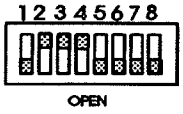


Open = 1 = ON
Closed = 0 = OFF

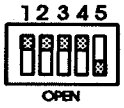


MEM SW-1

= Extended Address of $F100 0000
(Option OP-1 = Removed)

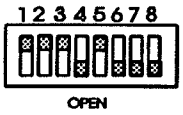


MEM SW-2

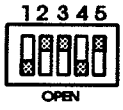


MEM SW-1

= Extended Address of $E808 0000
(Option OP-1 = Removed)

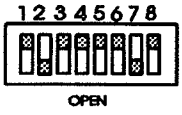


MEM SW-2



MEM SW-1

= Standard Address of $900 000
(Opton OP-1 = Installed)
(SW-2 is a don't care)



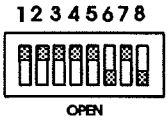
MEM SW-2

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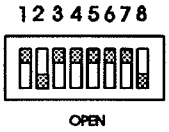
The Comet's Control Registers are accessed via the VMEbus Short Address Space via SW-3 as an A16 module. SW-3 Controls A8 thru A15.

SW-3	1	2	3	4	5	6	7	8
	A8	A9	A10	A11	A12	A13	A14	A15

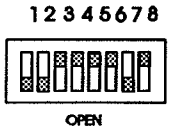
Open = 1 = ON
Closed = 0 = OFF



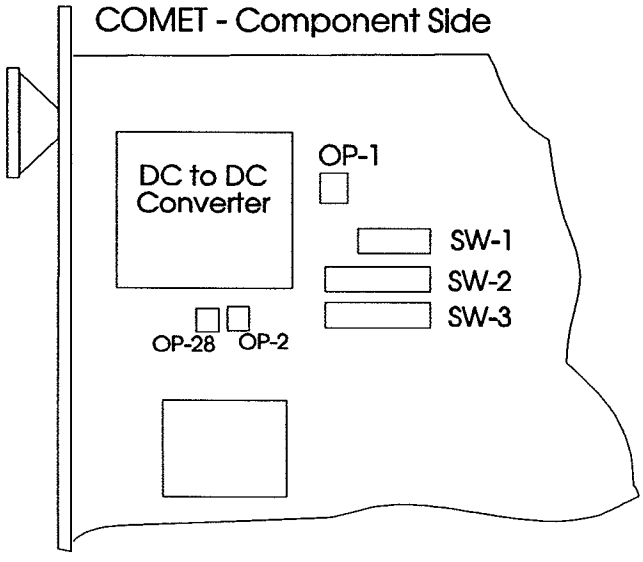
I/O SW-3 = Short I/O Address of $A000



I/O SW-3 = Short I/O Address of $8200



I/O SW-3 = Short I/O Address of $4300



SW-1, SW-2 & SW-3 Location Diagram

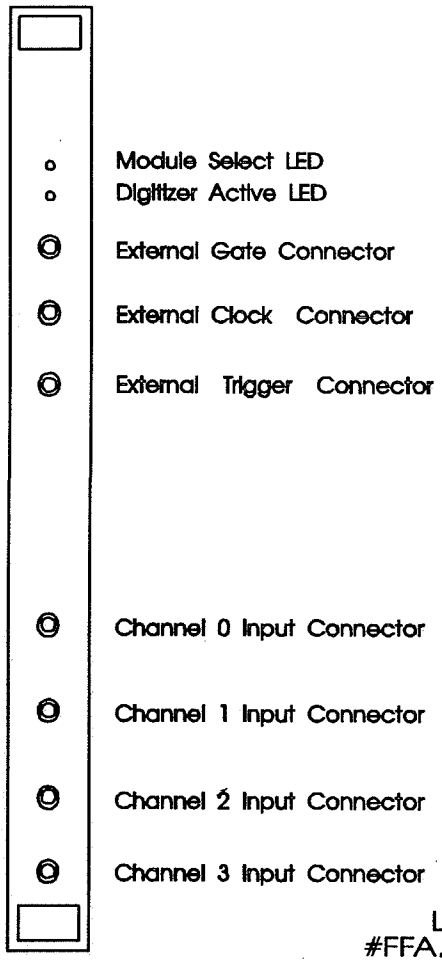
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4.2 Front Panel Connectors and LEDs.

The Front Panel of the Comet Digitizer Board has two LED indicators, 3 Control Input Connectors and 4 Input Signal Connectors.

The Module Select LED is active (on) when the Comet Board is being accessed by a VMEbus Master. The Digitizer Active LED is asserted (on) when the Comet Board is in the process of digitizing the input signals.

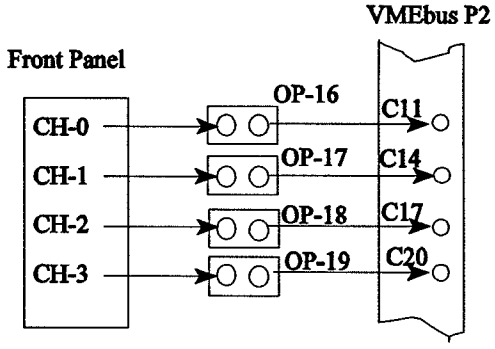
The three Control Input Connectors - External Gate, External Clock and External Trigger are explained in sections 2.2 & 3.3.1. The user may make a Lemo/BNC cable as shown below or an adapter can be purchased.

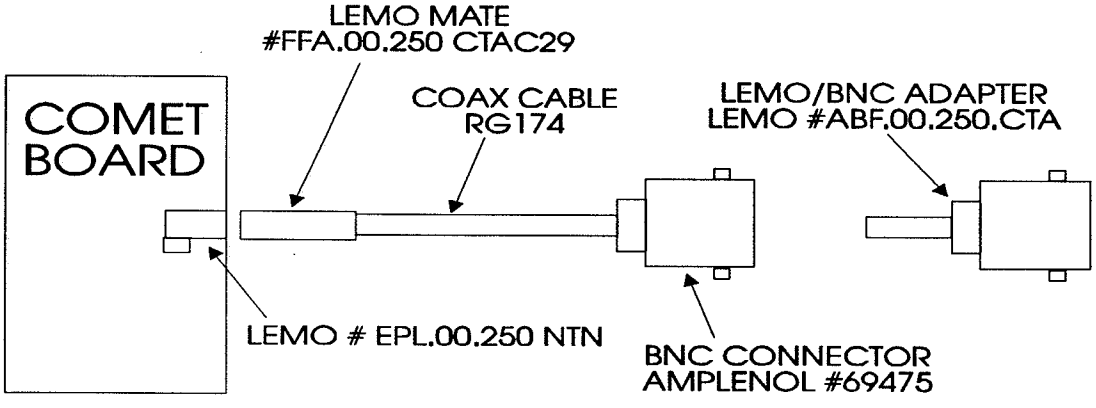


Front Panel Input Connectors	
Pins	Part No.
2	EPL.00.250 NTN

LEMO USA c/o Raines & Assoc. 708-498-0890

NOTE: Front Panel Input Connectors are also directly routed to the VMEbus P2 Connector via OPtion Jumpers as shown below.





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4.3 User Definable Options

The Table 4.3 describes the Options and Switches found on the COMET board. Factory standard is indicated, but does not preclude the user from reconfiguring the Board for their particular application. The locations of these Options are shown in Figure 4.3.

OPTION NO:	CONFIGURATION:	FUNCTION:
OP-1	Out	Addressing Mode (A32 selected)
OP-2	In	ACT1020 Active (Must be installed)
OP-3	2-3	Clock Source (On-Board 16 MHz. Oscillator)
OP-4	2-4 = CH-0	Input Operaton (0 - 10 Volts)
OP-5	Out "	50 Ohm Termination (Not selected)
OP-6	In "	1K Ohm Termination (Selected)
OP-7	2-4 = CH-1	Input Operaton (0 - 10 Volts)
OP-8	Out "	50 Ohm Termination (Not selected)
OP-9	In "	1K Ohm Termination (Selected)
OP-10	2-4 = CH-2	Input Operaton (0 - 10 Volts)
OP-11	Out "	50 Ohm Termination (Not selected)
OP-12	In "	1K Ohm Termination (Selected)
OP-13	2-4 = CH-3	Input Operaton (0 - 10 Volts)
OP-14	Out "	50 Ohm Termination (Not selected)
OP-15	In "	1K Ohm Termination (Selected)
OP-16	Out = CH-0	Analog Input via VMEbus P2
OP-17	Out = CH-1	Analog Input via VMEbus P2
OP-18	Out = CH-2	Analog Input via VMEbus P2
OP-19	Out = CH-3	Analog Input via VMEbus P2
OP-20	In = CH-1	A/D Device Type (for ADS-118) (Out for ADS-117)
OP-21	2-3 = CH-1	A/D Device Type (for ADS-118) (1-2 for ADS-117)
OP-22	In = CH-2	A/D Device Type (for ADS-118) (Out for ADS-117)
OP-23	2-3 = CH-2	A/D Device Type (for ADS-118) (1-2 for ADS-117)
OP-24	In = CH-3	A/D Device Type (for ADS-118) (Out for ADS-117)
OP-25	2-3 = CH-3	A/D Device Type (for ADS-118) (1-2 for ADS-117)
OP-26	In = CH-0	A/D Device Type (for ADS-118) (Out for ADS-117)
OP-27	2-3 = CH-0	A/D Device Type (for ADS-118) (1-2 for ADS-117)
OP-28	In	On-Board 16 MHz. Clock Enable (Selected)
SW-1	All Closed	Extended Addressing (used with SW-2)
SW-2	2,3,4 Closed	Extended Addressing = $F100 0000
SW-3	6,8 Open	Short I/O Addressing = $A000

TABLE 4.3 OPTIONS & FACTORY STANDARD CONFIGURATION

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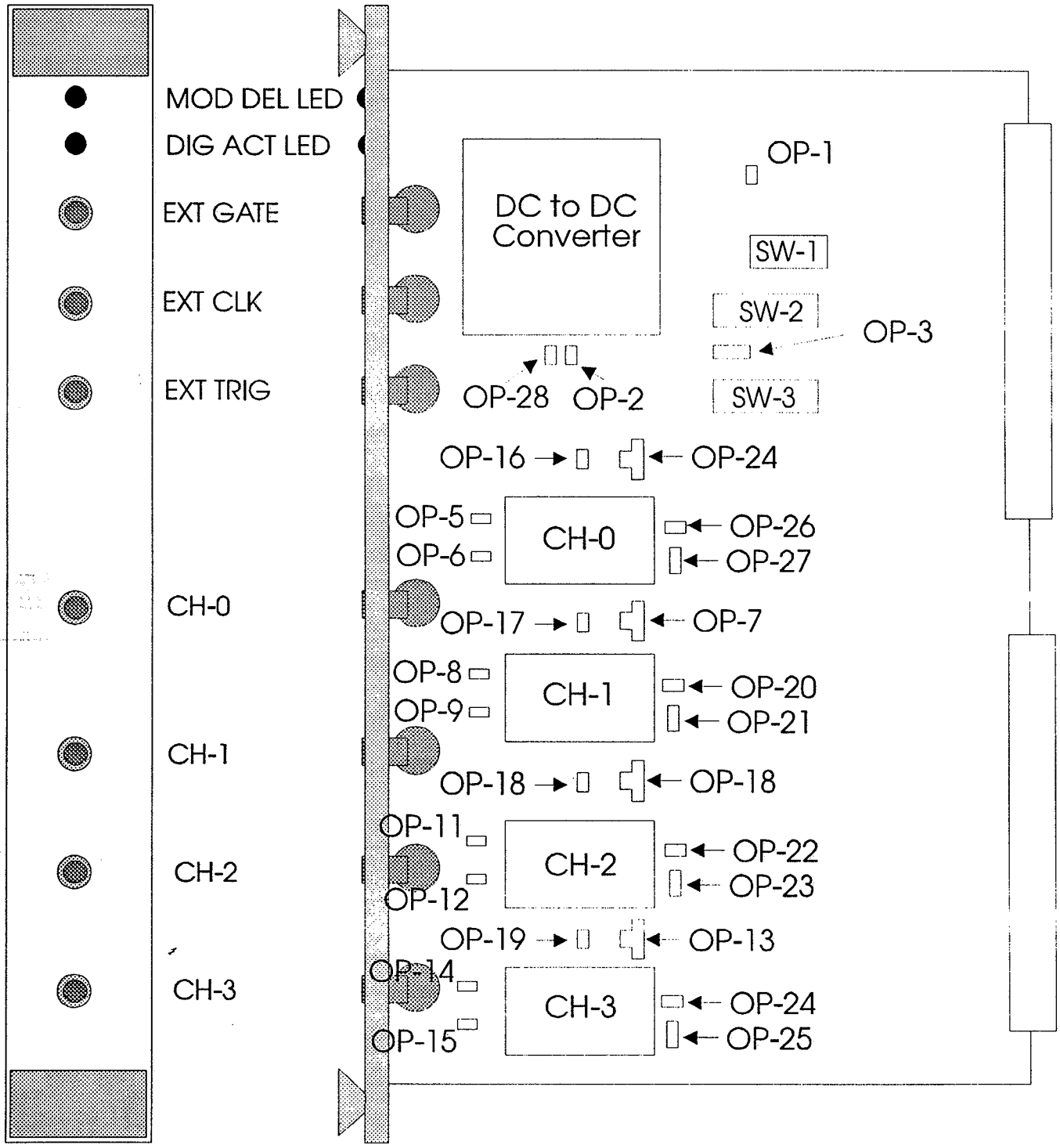


FIGURE 4.3 LOCATIONS OF OPTIONS AND SWITCHES

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4.3.1 Comet Board Addressing Mode (Option OP-1)

Option OP-1 selects between the Extended (32-Bit Addressing) and Standard (24-Bit Addressing) VMEbus Access Modes. See section 3.1.1 for setting Address Switches SW-1 and SW-2.

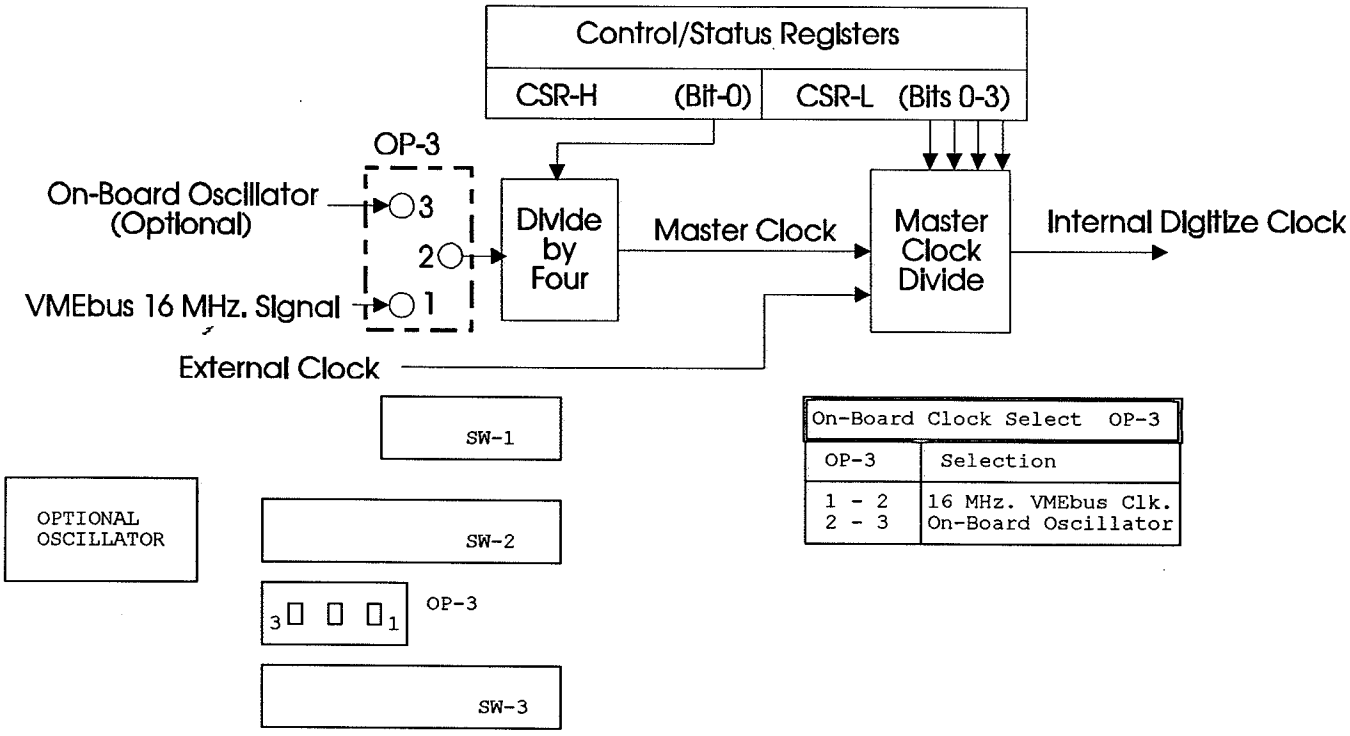
VMEbus Addressing Mode		
Access Mode	Option OP-1	Active Switches
Standard Addressing Mode (A24)	Installed	SW-1 only
Extended Addresssing Mode (A32)	Removed	SW-1 & SW-2

4.3.2 Gate Array ACT1020 Enable (Option OP-2)

Option OP-2 must be installed for the Comet Digitizer Board to function. It is a factory installed option and never should be removed by the user.

4.3.3 On-Board Clock Select (Option OP-3)

If Bit-0 of the CSR-H is set to a "0", then the Master Clock is selected from the On-Board sources (ie: the VMEbus 16 MHz Bus Clock or an Optional On-Board Oscillator - see section 3.1.3.1 - Bit 0 for details on the CSR-H). When the On-Board sources are to be used, OP-3 selects between the two sources available. If OP-3 is jumpered from pins 1 to 2 the VMEbus Backplane SYSCLK 16 MHz. Clock signal will be selected. If OP-3 is jumpered from pins 2 to 3 an Optional On-Board Oscillator (U8) Clock signal will be selected. The On-Board sources are both sent to a divide by four circuit before being sent to the Master Clock Divide circuit.



On-Board Clock Select OP-3	
OP-3	Selection
1 - 2	16 MHz. VMEbus Clk.
2 - 3	On-Board Oscillator

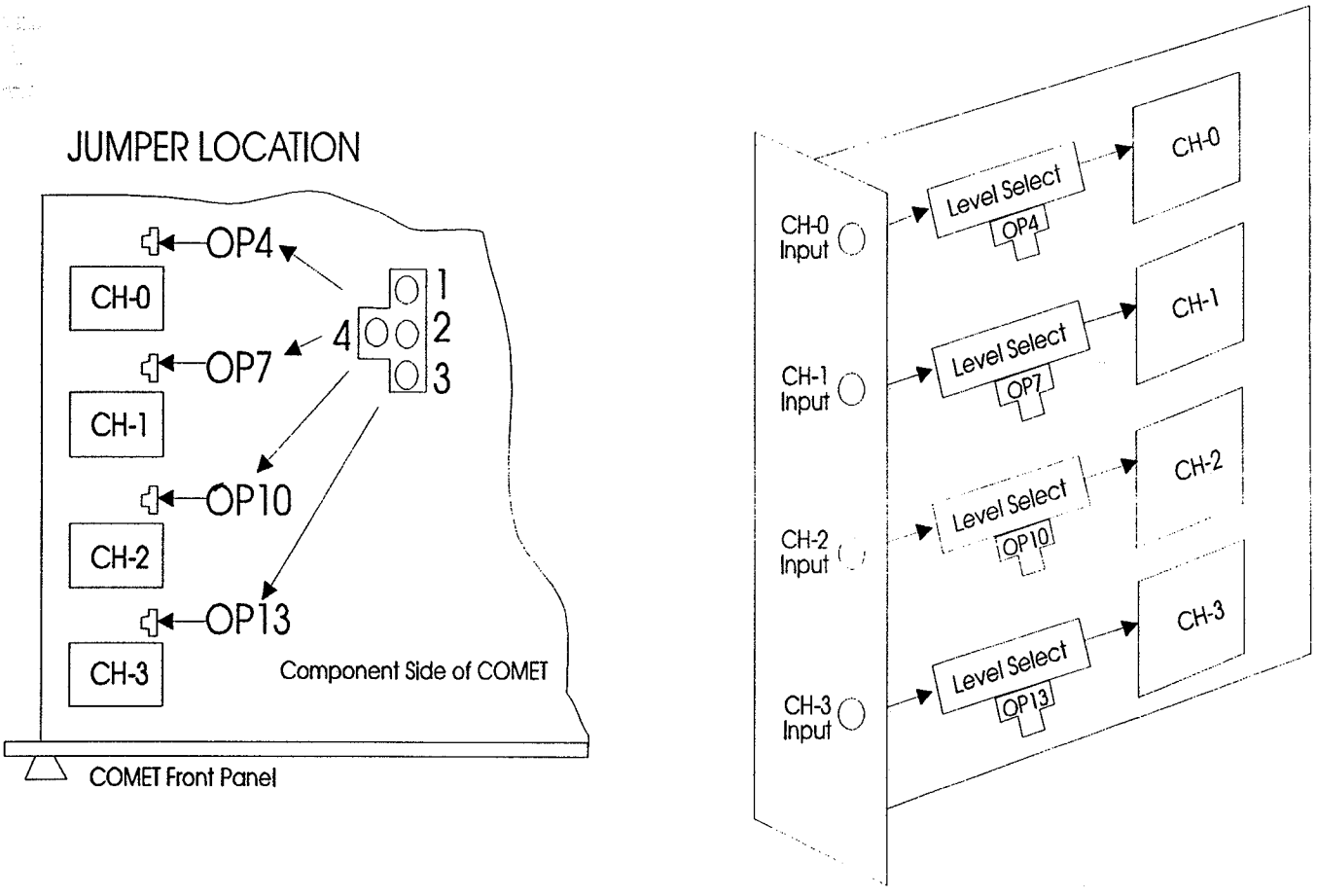
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4.3.4 Input Signal Voltage Levels (Op -4, -7, -10, & -13)

The Comet Digitizer Board can operate using two different input signal levels. Option Jumpers OP-4, OP-7, OP-10 and OP-13 select the type of operation for Channels CH-0, CH-1, CH-2 and CH-3 respectively. The two input levels for 2 MHz. Devices are supported; 0 thru 10 Volts and Plus/Minus 5 Volts. For 5 MHz. Devices, only +/- 1 Volt operation is supported. The Table below shows the jumper configuration and the figure below shows the jumper locations and a pictorial diagram.

0 - 10 Volt Range 2 MHz. Devices		+/- 5 Volt Bipolar Range 2 MHz. Devices)	+/- 1 Volt Range (5 MHz. Device)
CHANNEL	OPTIONS	OPTIONS	OPTIONS
CH-0	OP-4 = 1-2	OP-4 = 2-3	OP-4 = 4-2
CH-1	OP-7 = 1-2	OP-7 = 2-3	OP-7 = 4-2
CH-2	OP-10 = 1-2	OP-10 = 2-3	OP-10 = 4-2
CH-3	OP-13 = 1-2	OP-13 = 2-3	OP-13 = 4-2

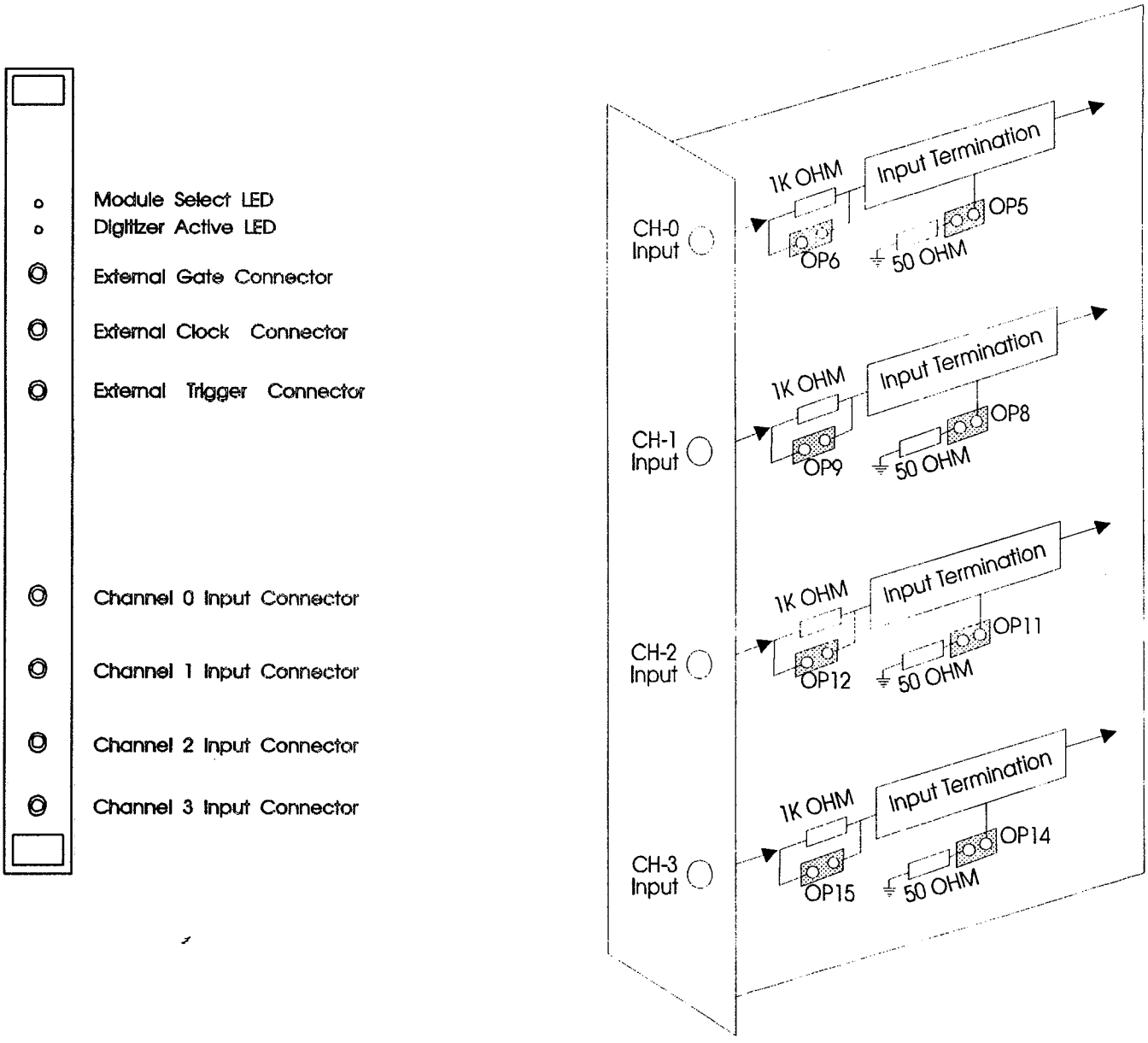
TABLE 4.3.4 INPUT VOLTAGE OPERATION



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4.3.5 Input Signal Termination (OP-5, -6, -8, -9, -11, -12, -14 & -15)

The four Channel Input Connectors on the Front Panel bring into the Comet Board the analog signals to be digitized. Input termination is selectable for 50 ohms, 1000 ohms, or a split termination network (ie: voltage divider) of 1000/50 ohms. Options OP-5 & OP-6 are associated with CH-0, OP-8 & OP-9 are associated with CH-1, OP-11 & OP-12 are associated with CH-2, OP-14 & OP-15 are associated with CH-3.



50 OHM TERMINATION		1K OHM TERMINATION	
CHANNEL	OPTIONS	CHANNEL	OPTIONS
CH-0	OP-5 = IN, OP-6 = IN	CH-0	OP-5 = IN, OP-6 = OUT
CH-1	OP-8 = IN, OP-9 = IN	CH-1	OP-8 = IN, OP-9 = OUT
CH-2	OP-11 = IN, OP-12 = IN	CH-2	OP-11 = IN, OP-12 = OUT
CH-3	OP-14 = IN, OP-15 = IN	CH-3	OP-14 = IN, OP-15 = OUT

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4.4 Connector Pinouts

4.4.1 VMEbus P1 Connector

The P1 connector is pinned out according to the VMEbus specifications given in Table 7.0.

Pin Number	Row A Signal	Row B Signal	Row C Signal
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

(1) See VMEbus Specification (Rev. C.1) for further information on these signals.
*Indicates Low Active

TABLE 4.4.1 VMEbus P1 CONNECTOR PINOUT

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4.4.2 VMEbus P2 Connector

Row B of the P2 connector is defined for address and data lines needed for 32-bit systems. Row C is pinned out according to the following Table.

Pin Number	Row A	Row B	Row C
1		+5V	GND
2		GND	EXT-TRIG
3		RESERVED	GND
4		A24	GND
5		A25	EXT-GATE
6		A26	GND
7		A27	GND
8		A28	EXT-CLK
9		A29	GND
10		A30	GND
11		A31	CH-0 INPUT
12		GND	GND
13		+5V	GND
14		D16	CH-1 INPUT
15		D17	GND
16		D18	GND
17		D19	CH-2 INPUT
18		D20	GND
19		D21	GND
20		D22	CH-3 INPUT
21		D23	GND
22		GND	
23		D24	
24		D25	
25		D26	
26		D27	
27		D28	
28		D29	
29		D30	
30		D31	
31		GND	
32		+5V	

TABLE 4.4.2 P2 CONNECTOR PINOUT

Front Panel Input Connectors	
Pins	Part No.
2	FFA.00.250.CTAC29
See Section 4.2	

LEMO USA c/o Raines & Assoc. 708-498-0890

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5.0 WARRANTY INFORMATION

All items manufactured and sold by Omnibyte Corporation are warranted against defects in materials or workmanship and are guaranteed to meet specifications in effect at the time of manufacture for a period of (2) years from the date of delivery, to the original purchaser only.

Omnibyte's responsibility under this warranty is limited to repair or replacement of any item (at our option) returned to the factory during the warranty period, freight prepaid. Omnibyte shall either repair or replace the item, provided the failure of the item, in our opinion, was not due to abuse, modification, or acts of God. **EXCEPT AS OTHERWISE INDICATED, THERE ARE NO OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.** Omnibyte's liability shall be limited to the purchase price of the item or items, and Omnibyte shall not be responsible or liable for any lost profits or consequential damages, or for any claim against the purchaser by any party.

"NOTE"

ALL BOARDS RETURNED TO OMNIBYTE CORPORATION FOR REPAIR MUST BE ACCOMPANIED WITH AN RMA NUMBER (RETURN MATERIAL AUTHORIZATION). THIS NUMBER WILL BE ISSUED TO YOU BY OMNIBYTE WHEN REQUESTING AUTHORIZATION TO RETURN YOUR BOARD. ALSO, AN EXPLANATION OF THE PROBLEM AND THE NAME AND PHONE NUMBER OF THE PERSON USING THE BOARD WHEN THE PROBLEM OCCURRED SHOULD BE ENCLOSED WITH THE RETURNED BOARD. THIS PROCEDURE WILL EXPEDITE THE REPAIR AND RETURN OF YOUR BOARD.

ANY BOARDS RECEIVED BY OMNIBYTE CORPORATION WITHOUT AN RMA NUMBER WILL BE RETURNED TO SENDER, UNTIL AN RMA NUMBER HAS BEEN PROCURED.

6.0 ORDERING INFORMATION

Order numbers for the Omnibyte COMET board are as follows Comet-Z where:

Z=0,	No A/D converter modules	
Z=2-1	(1) ADS-117MC	2MHz A/D module
Z=2-2	(2) ADS-117MC	2MHz A/D modules
Z=2-3	(3) ADS-117MC	2MHz A/D modules
Z=2-4	(4) ADS-117MC	2MHz A/D modules
Z=5-1	(1) ADS-118MC	5MHz A/D module
Z=5-2	(2) ADS-118MC	5MHz A/D modules
Z=5-3	(3) ADS-118MC	5MHz A/D modules
Z=5-4	(4) ADS-118MC	5MHz A/D modules

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7.0 PARTS LISTING FOR THE COMET DIGITIZER BOARD

The parts list for the Comet Digitizer Board is shown in the Table below:

PART NUMBER:	DESCRIPTION:	QTY:	PLACEMENT:
CCN04293	1 PIN STRIP	4	OP-4,-7,-0,-3
CCN04291	1 X 2 PIN STRIP	10	OP-1,-2,-5,-6,-8,-9,-11, OP-12,-14,-15
CCN04289	1 X 3 PIN STRIP	5	OP-3,-4,-7,-10,-13
CCN01160	96 PIN RT DIN	2	P1,P2
CCN04279	RT ANG LEMO CONNECTOR	7	BNC1 -BNC7
CCPO4272	22PF CHIP CAP	5	C14,C27,C28,C40,C42
CCPO4275	0.01 UF CHIP CAP	42	C5-C11,C13,C16-C25, C36,C37,C39,C41,C43-C45,C54-C59,C67-C72, C80-C84
CCP04278	0.1UF CHIP CAP	19	C1,C12,C15,C31-C34,C49 C52,C62-C65,C75-C78
CCP04282	4.7UF TANT	12	C29,C30,C35,C47,C48,C53, C60,C61,C66,C73,C74,C79
CCPO4286	33UF CHIP CAP	6	C2-C4,C26,C38,C46
CHWO1187	2-56 X 1/2 MACH SCW	4	P1,P1,P2,P2
CHWO3530	2-56 NUT	4	P1,P1,P2,P2
CIC03776	74S38D	1	U8
CIC03860	74F543D	9	U4,U5,U7,U10,U13,U16,U17, U18,U22
CIC04009	74LS244DW	2	U39,U43
CIC04073	74ACT16245DL	6	U20,U21,U31,U36,U48,U51
CIC04271	74ALS520DW	3	U6,U9,U12
CIC04277	HM62832JP-35	16	U23,U24,U29,U30,U34,U35, U37,U38,U41,U42,U46,U47, U49,U50,U54,U55
CIC04280	74LS423DW	4	U11,U14,U26,U27
CLE04285	RED LED	2	LED1, LED2
CMI01940	10X12 ANTISTATIC BAG1SHIPPING	1	SHIPPING
CPT04276	3266W-1-103	4	R14,R19,R24,R29
CRE03724	4.7K OHM CHIP RES	5	R1,R9,R10,R11,R12
CRE03957	10K OHM CHIP RES	1	R7
CRE04064	1K OHM CHIP RES	4	R15,R20,R25,R30
CRE04269	470 OHM CHIP RES	3	R3,R4,R5
CRE04274	22K OHM CHIP RES	2	R6,R8
CRE-0428	51 OHM CHIP RES	4	R13,R18,R23,R28
CRE04294	0 OHM CHIP RES	3	R2,R17,R22,R27,R32
CSK00378	8 PIN DIP SKT	4	U32,U40,U44,U52
CSK00379	14 PIN DIP SKT	2	U2,U19
CSK00384	24 PIN MACH SC SKT	4	U28,U33,U45,U53
CSK04290	84 PIN PLCC SKT	1	U15
CSK04292	52 PIN PLCC SKT	1	U3
CSK04295	1 X 3 SKT STRIP	4	U1 (X4)
CSK04296	1 PIN SOCKET	2	U1 (X2)
CSPOO064	4310R-101-472	1	RP1
CSWO0161	8 POS DIP SWITCH	2	SW2,SW3
CSWO4270	5 POS DIP SWITCH	1	SW1
CXT01151	16MHZ OSCILLATOR	1	Y1

NOTE: U25,R16,R21,R26,R31 HAVE NO COMPONENTS INSTALLED.

TABLE 7.0 PARTS LIST FOR THE COMET DIGITIZER BOARD

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8.0 APPENDICES

The Appendix in this manual contain information pertinent to the operation of the COMET Digitizer Board.

Appendix A (Reliability Prediction)

Appendix A contains reliability informaton regarding the Comet Board.

Appendix B (Schematic Diagrams)

Electrical schematic diagrams for the COMET Digitizer Board are given in this secton.

"NOTE"

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Appendix C (Data Sheets)

Appendix C contains excerpts from the data sheets for the Datel ADS-117 2.0 MHz. and Datel ADS-118 5.0 MHz. devices. Familarity with the operating characteristics of these devices will be necessary for proper operation and is included for that purpose. The data sheets has been reprinted courtesy of DATEL, Inc.

The reprints contained herein are the most current available at the time of printing and may be updated by the manufacturer without notice at any time. Omnibyte assumes no liability for notifying purchasers of this manual of these updates.

ADS-117 A/D CONVERTER
ADS-118 A/D CONVERTER

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APPENDIX-A

RELIABILITY PREDICTION
for the
CTS04708 COMET

The CTS04708 COMET (with up to 4 5MHz. Modules) has the following predicted reliability based on the MIL-HDBK-217 (Revision F, notice 1) Appendix A Parts Count Reliability Prediction Model:

Failure Rate for COMET w/ no Module
= 15.96312 Failures/10^6 hours
= 62,644 hours MTBF
= 7.1512 years MTBF

Failure Rate for COMET w/ 1 5MHz Module
= 27.66312 Failures/10^6 hours
= 36,149 hours MTBF
= 4.1266 years MTBF

Failure Rate for COMET w/ 2 5MHz Modules = 39.36312 Failures/10^6 hours
= 25,404 hours MTBF
= 2.9001 years MTBF

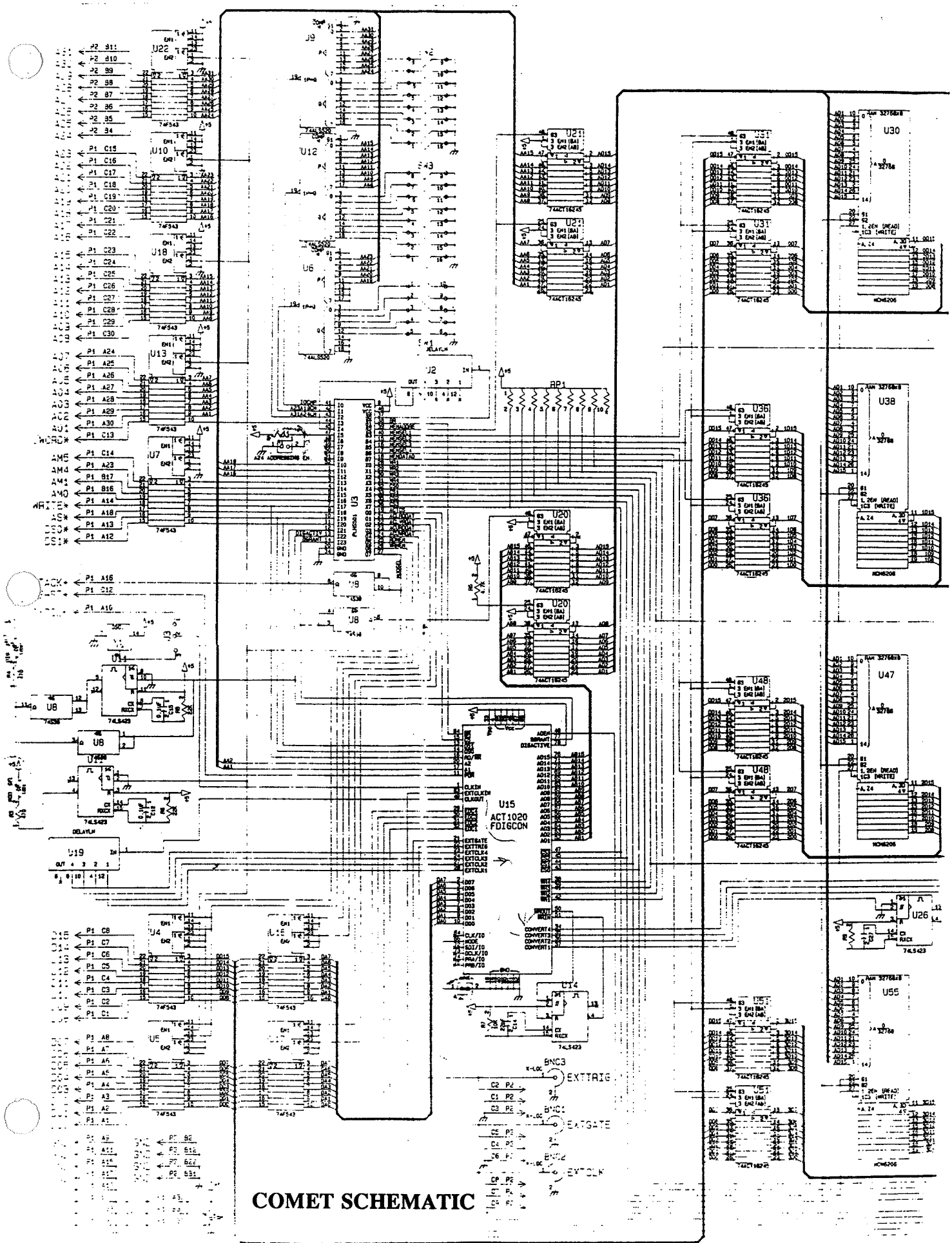
Failure Rate for COMET w/ 3 5MHz Modules = 51.06312 Failures/10^6 hours
= 19,584 hours MTBF
= 2.2356 years MTBF

Failure Rate for COMET w/ 4 5MHz Modules
= 62.76312 Failures/10^6 hours
= 15,933 hours MTBF
= 1.8188 years MTBF

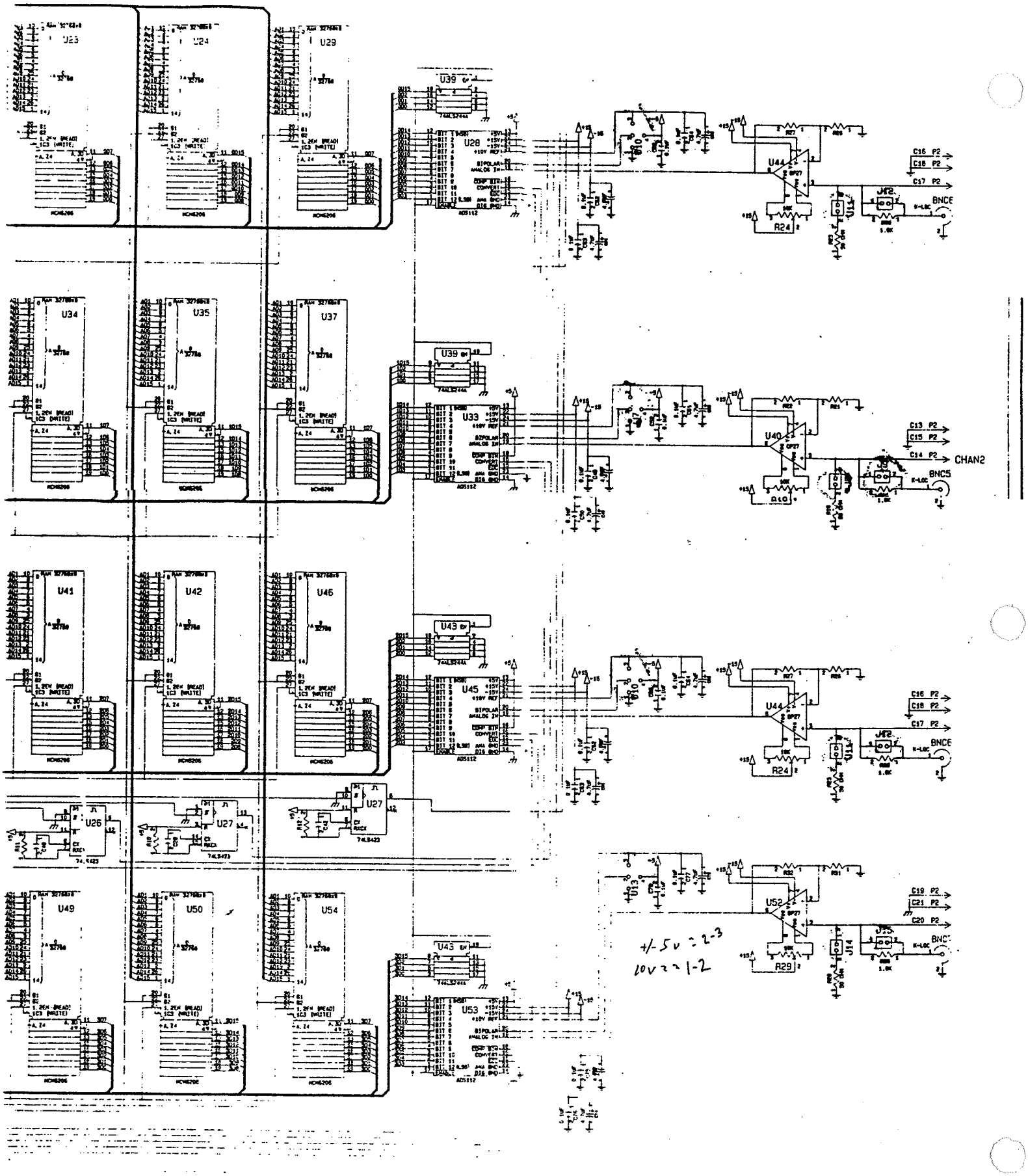
All individual failure rates were calculated using the Appendix A default values for commercial devices operating continuously in a Ground Benign environment, ivith the exception of the Datel ADS118MC Sampling A/D Device (Omnibyte P/N CIC04705). (Please refer to MIL-HDBK-217, Appendix A for a complete listing of these default values.) The individual failure rate for the ADS118MC was calculated by Datel, and is based on a commercial device operating continuously in a Ground Benign environment at 50° C.

Please note that in general, use of the MIL-HDBK-217 Parts Count Reliability Prediction Method will result in a more conservative estimate (i.e. higher failure rate) of system reliability than the MIL-HDBK-217 Part Stress Method. Remember also that the figures produced by either method are only an estimate of system reliability. Actual reliability will depend upon many factors, including (but not limited to) duty cycle of the equipment, the operating environment, the supplied voltages, and other operating conditions specific to each application.

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COMET SCHEMATIC

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DATEL

DATEL, Inc.

11 Cabot Boulevard, Mansfield, MA 02048

DATEL
ADS-117

12-Bit A/D Converter

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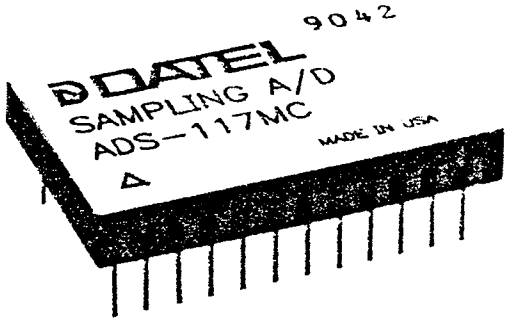
ADS-117

12-Bit, 2.0 MHz, Low-Power Sampling A/D Converter

PRELIMINARY PRODUCT DATA

FEATURES

- 12-Bit resolution
- Internal Sample/Hold
- 2.0 MHz minimum throughput
- Functionally complete
- Small 24-pin DIP
- Low-power, 1.4 Watts
- Three-state output buffers
- Samples to Nyquist

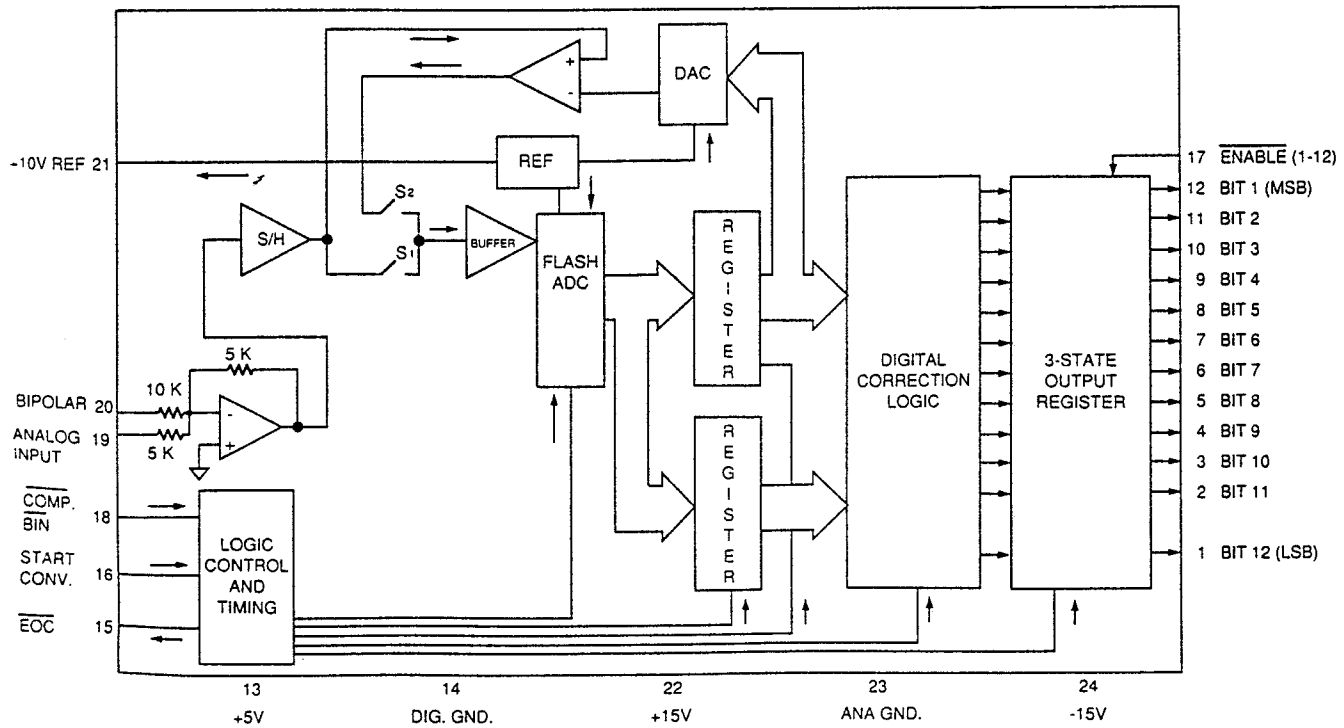


GENERAL DESCRIPTION

DATEL's ADS-117 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin ceramic DIP. A minimum throughput rate of 2.0 MHz is achieved while only dissipating 1.4 Watts. The ADS-117 digitizes signals up to Nyquist.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	13	+5V
2	BIT 11 OUT	14	DIGITAL GROUND
3	BIT 10 OUT	15	$\overline{EOC}$
4	BIT 9 OUT	16	START CONVERT
5	BIT 8 OUT	17	$\overline{ENABLE}$ (1-12)
6	BIT 7 OUT	18	$\overline{COMP}$ BIN
7	BIT 6 OUT	19	ANALOG INPUT
8	BIT 5 OUT	20	BIPOLAR
9	BIT 4 OUT	21	+10V REF
10	BIT 3 OUT	22	+15V
11	BIT 2 OUT	23	ANALOG GROUND
12	BIT 1 OUT (MSB)	24	-15V



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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply (Pin 13)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 16, 17, 18)	-0.3 to +6.0	Volts dc
Analog Input (Pin 19)	-15 to +15	Volts dc
Lead Temp. (10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-117	–	±5	–	Volts dc
(See Table 2 also)	–	0 to +10	–	Volts dc
Input Impedance	4.5	5.0	–	K Ohms
Input Capacitance	–	6	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5	µA
Logic Loading "0"	–	–	-200	µA
PERFORMANCE				
No Missing Codes (12 Bits; fin=1.0 MHz)	Over the Operating Temp. Range.			
Integral non-Linearity				
+25 °C	–	±1/4	±3/4	LSB
0 °C to +70 °C	–	±1/4	±3/4	LSB
-55 C to +125 °C	–	–	±2	LSB
Differential Non-Linearity				
+25 °C	–	–	±3/4	LSB
0 °C to +70 °C	–	–	±3/4	LSB
-55 C to +125 °C	–	–	±1.5	LSB
Full Scale Absolute Accuracy (see Tech Note 1)				
+25 °C	–	±0.13	±0.25	% FSR
0 °C to +70 °C	–	±0.15	±0.44	% FSR
-55 C to +125 °C	–	±0.25	±0.78	% FSR
Unipolar Zero Error, +25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Unipolar Zero Tempco.	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Bipolar Zero Tempco	–	±5	±8	ppm/ °C
Bipolar Offset Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Gain Tempco	–	±20	±40	ppm/ °C
OUTPUTS				
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift.	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Resolution	12 Bits			
Output Coding (Pin 18 Hi) (Pin 18 Low)	Straight bin./offset bin. Comp. bin./Comp. offset bin.			
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA

OUTPUT CONT.	MIN.	TYP.	MAX.	UNITS
DYNAMIC PERFORMANCE				
In-Band Harmonics (-0.5 dB)				
DC to 100 KHz	-75	-81	–	FS -dB
100 KHz to 500 KHz	-70	-75	–	FS -dB
500 KHz to 1 MHz	-67	-70	–	FS -dB
Total Harm. Distort. (-0.5 dB)				
DC to 100 KHz	-75	-78	–	FS -dB
100 KHz to 500 KHz	-68	-73	–	FS -dB
500 KHz to 100 MHz	-66	-71	–	FS -dB
Signal-to-Noise Ratio (w o distort., -0.5 dB)				
DC to 100 KHz	-68	-72	–	FS -dB
100KHz to 500 KHz	-67	-71	–	FS -dB
500 KHz to 1 MHz	-66	-71	–	FS -dB
Signal-to-Noise Ratio & distort., -0.5 dB				
DC to 100 KHz	-66	-70	–	FS -dB
100 KHz to 500 KHz	-66	-70	–	FS -dB
500 KHz to 1 MHz	-65	-70	–	FS -dB
Effective Bits, -0.5 dB				
DC to 100 KHz	11.0	11.4	–	bits
100 KHz to 500 KHz	10.6	11.25	–	bits
500 KHz to 1 MHz	10.5	11.0	–	bits
Two-Tone Intermodulation Distort. (fin = 75 KHz, 105 KHz, Fs = 1 MHz, -7 dB	-80	-88	–	FS -dB
Two-Tone Intermodulation Distort. (fin = 970 KHz, 990 KHz, Fs = 2 MHz, -0.5 dB)	-65	-68	–	FS -dB
Input Bandwidth				
Small Signal (-20 dB input)	8	10	–	MHz
Full Power (0 dB input)	5	7	–	MHz
Feedthrough (1 MHz)	-72	-74	–	dB
Slew Rate	–	210	–	V/µSec.
Aperture Delay Time	–	–	20	nSec.
Effect. Aperture Delay Time	–	–	16	nSec.
Aperture Uncertainty (Jitter)				
(RMS)	–	±5	±15	pSec.
(peak)	–	–	±40	pSec.
Overvoltage Recovery Time	–	–	1000	nSec.
S/H Acquisition Time to 0.01%FS				
+ 25 °C	–	–	150	nSec.
0 °C to +70 °C	–	–	165	nSec
-55 C to +125 °C	–	–	170	nSec
Conversion Rate -55 C to +125 °C	2.0	–	–	MHz
POWER REQUIREMENTS				
Power Supply Range ①				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+35	+46	mA
-15V dc Supply	–	-40	-50	mA
+5V dc Supply ②	–	+60	+75	mA
Power Dissipation	–	1.4	1.8	Watts
Power Supply Rejection	–	–	0.07	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range, case				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	24-pin hermetic sealed, ceramic DIP			
Weight	0.42 ounces (12 grams)			

① For ±12V, +5V operation, contact DATEL
② +5V power usage at 1 TTL logic loading per data output bit.

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TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-117 to zero using the optional external circuitry shown in Figure 4. The external adjustment circuit has no affect on the throughput rate.

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 18) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 18 to ground. The pin 18 signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect ENABLE (pin 17) to a logic "0" (low). To disable, connect pin 17 to a logic "1" (high).

6. To meet the guaranteed conversion rate. a maximum start convert pulse is specified. A wider start convert pulse will result in slower conversion rates.

   Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, Figure 4, and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 150 nanoseconds to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 1. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the pin 18 tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the pin 18 tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 18 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 18 tied low (complementary offset binary).

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 1. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 18 tied high or between 0000 0000 0001 and 0000 0000 0000 for pin 18 tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

Table 1. Zero and Gain Adjust

FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV dc	+9.9963V dc
±5V dc	+1.22mV dc	+4.9963V dc

Table 2. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	K Ohms
0 to +5V, ±2.5V	2	6	K Ohms
0 to +2.5V, ±1.25V	2	14	K Ohms

Table 3. Output Coding

		STRAIGHT BIN.	COMP. BINARY		
UNIPOLAR SCALE	INPUT RANGES, V dc 0 to +10V	OUTPUT CODING MSB LSB	MSB LSB	INPUT RANGE ±5V dc	BIPOLAR SCALE
+FS -1 LSB	+9.9976V	1111 1111 1111	0000 0000 0000	+4.9976V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000	0001 1111 1111	+3.7500V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000	0011 1111 1111	+2.5000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000	0111 1111 1111	0.0000V	0
1/4 FS	2.5000V	0100 0000 0000	1011 1111 1111	-2.5000V	-1/2 FS
1/8 FS	1.2500V	0010 0000 0000	1101 1111 1111	-3.7500V	-3/4 FS
1 LSB	0.0024V	0000 0000 0001	1111 1111 1110	-4.9976V	-FS +1 LSB
0	0.0000V	0000 0000 0000	1111 1111 1111	-5.0000V	-FS
		OFF. BINARY	COMP. OFF. BIN.		

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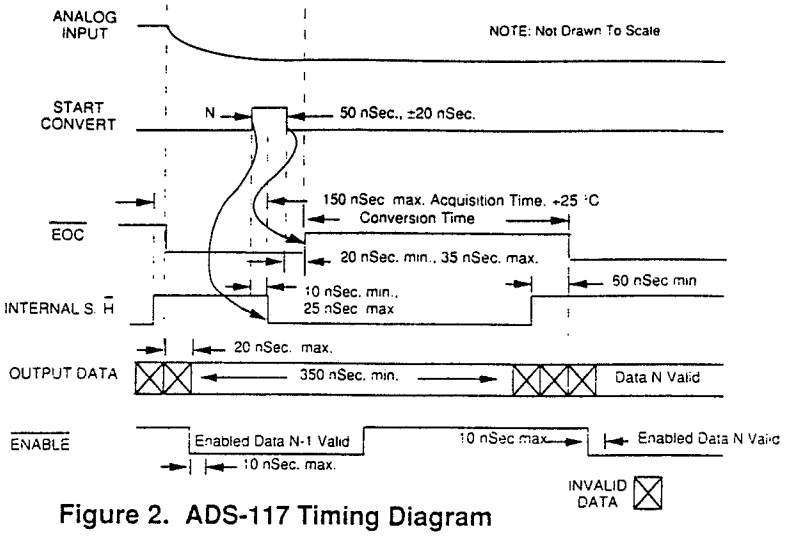


Figure 2. ADS-117 Timing Diagram

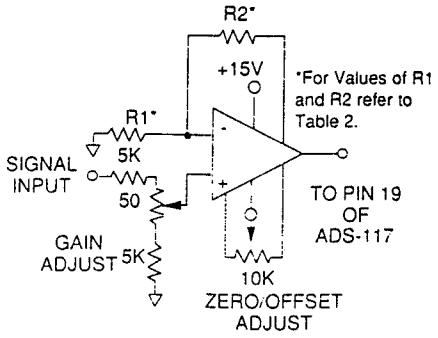


Figure 4. Optional Calibration Circuit

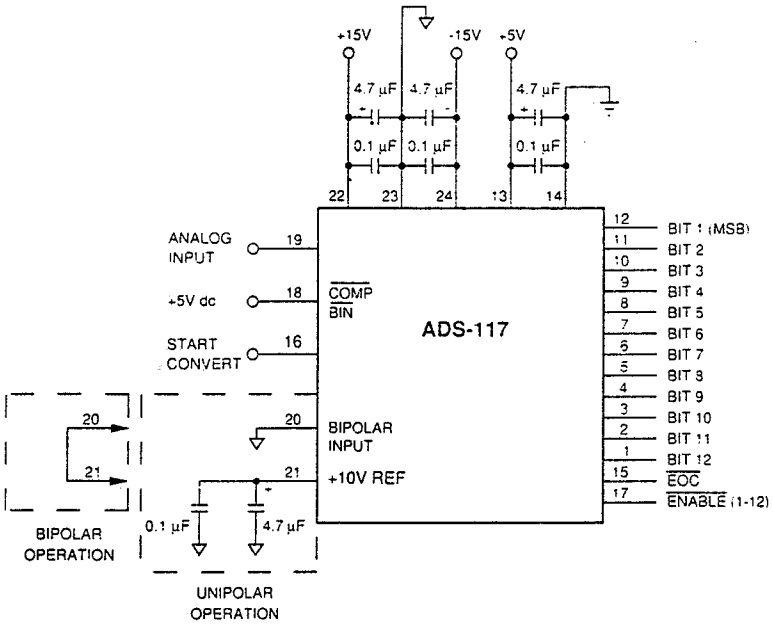


Figure 3. Typical ADS-117 Connection Diagram

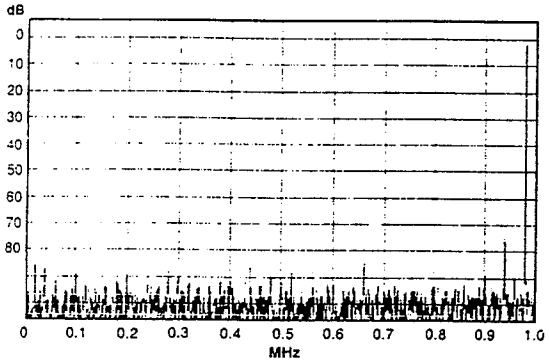
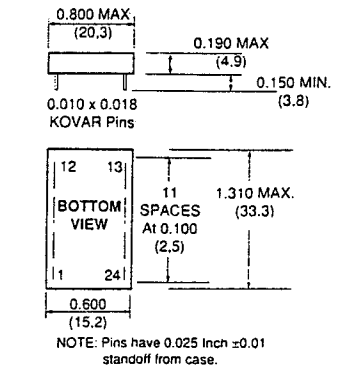


Figure 5. FFT Analysis of ADS-117

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Pins have 0.025 Inch ±0.01 standoff from case.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-117MC	0 °C to +70 °C	Hermetic
ADS-117MM	-55 °C to +125 °C	Hermetic
ADS-EVAL1	Evaluation board (without ADS-117)	

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For availability of MIL-STD-883 versions of the ADS-117, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

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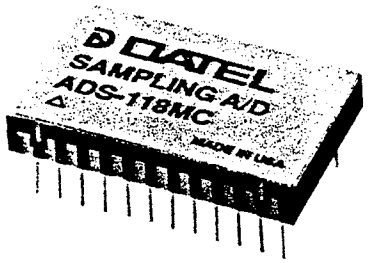
PRELIMINARY PRODUCT DATA

ADS-118, ADS-118A

12-Bit, 5.0 MHz, Low-Power Sampling A/D Converter

FEATURES

- **12-Bit resolution**
- **Internal Sample/Hold**
- **5.0 MHz minimum throughput**
- **On-board reference and clock**
- **Small 24-pin DDIP**
- **Low-power, 1.9 Watts**
- **Samples to Nyquist**
- **Three-state output buffers on ADS-118**
- **Direct offset and gain adjust on ADS-118A**
- **Effective bits: 11 bits**



GENERAL DESCRIPTION

DATEL's ADS-118 and ADS-118A are 12-bit, 5.0 MHz, sampling A/D converters packaged in a space-saving 24-pin DDIP. The ADS-118 offers an input range of ±1V and has three-state outputs. The ADS-118A has an input range of ±1.25V and features direct adjustment of offset and gain errors.

These low-power devices (1.9 watts) contain an internal fast-settling sample/hold amplifier, a 12-bit subranging A/D converter, and a precision reference. All timing and control logic operates from a single start convert pulse.

Other features include a differential non-linearity of ±1/2 LSB and a spurious free dynamic range of −77 dB. These functionally complete devices are ideally suited for both time and frequency domain applications.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	13	+5V DIGITAL SUPPLY
2	BIT 11 OUT	14	DIGITAL GROUND
3	BIT 10 OUT	15	EOC
4	BIT 9 OUT	16	START CONVERT
5	BIT 8 OUT	17 *	ENABLE (1-12)/OFFSET
6	BIT 7 OUT	18	ANALOG GROUND
7	BIT 6 OUT	19	ANALOG INPUT
8	BIT 5 OUT	20	−5V
9	BIT 4 OUT	21	+5V ANALOG SUPPLY
10	BIT 3 OUT	22	+15V
11	BIT 2 OUT	23	ANALOG GROUND
12	BIT 1 OUT (MSB)	24	−15V

* ADS-118A, Pin 17 is OFFSET
ADS-118, Pin 17 is ENABLE (1-12)

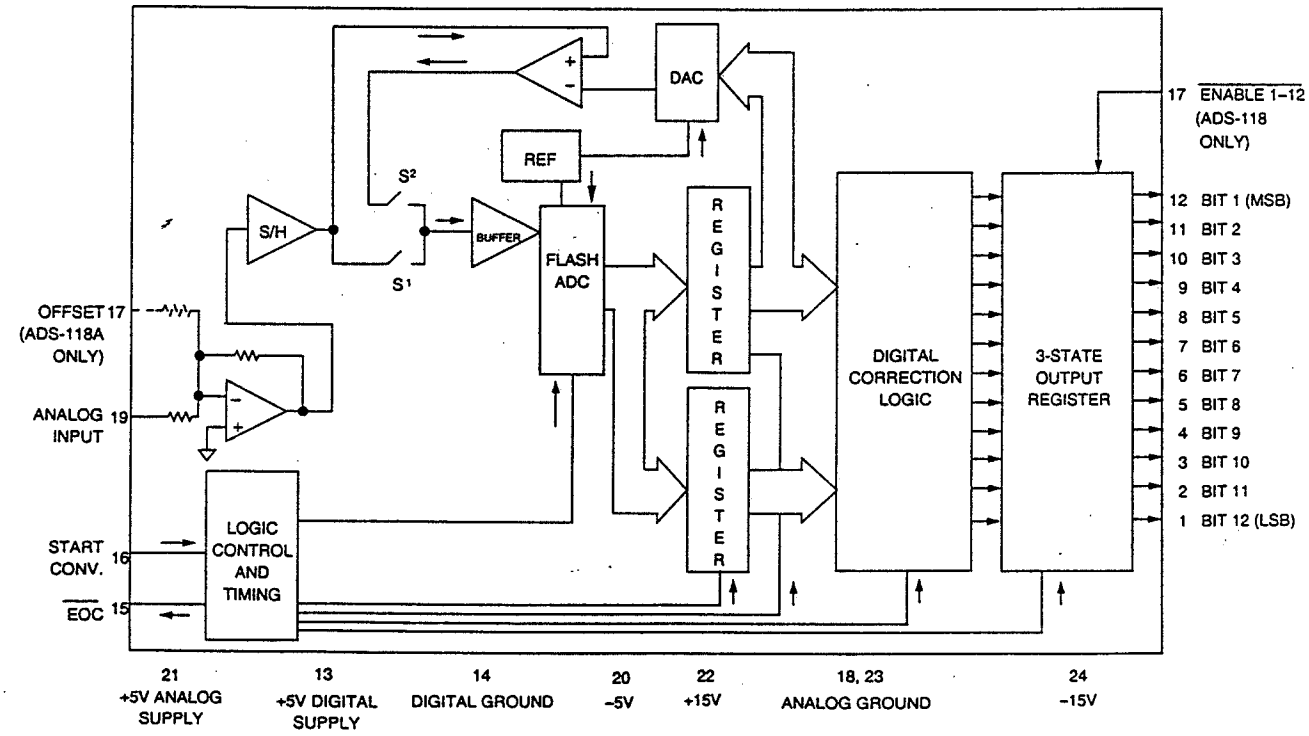


Figure 1. ADS-118 Simplified Block Diagram

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
–15V Supply (Pin 24)	0 to –18	Volts dc
+5V Supply (Pin 13, 21)	–0.5 to +7.0	Volts dc
–5V Supply (Pin 20)	+0.5 to –7.0	Volts dc
Digital Inputs (Pins 16, 17)	–0.3 to VDD +0.3	Volts dc
Analog Input (Pin 19)	–15 to +15	Volts dc
Lead Temp. (10 Sec.)	300	°C max .

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and ±5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS–118 (See Table 2 also)	—	±1	—	Volts dc
ADS-118A	—	±1.25	—	Volts dc
Input Impedance	475	500	—	Ohms
Input Capacitance	—	6	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	—	—	Volts dc
Logic "0"	—	—	0.8	Volts dc
Logic "1" Loading	—	—	5	µA
Logic "0" Loading	—	—	–200	µA
PERFORMANCE				
No Missing Codes (12 Bits; ƒIN = 2.5 MHz)	Over the Operating Temp. Range.			
Integral Non–Linearity				
+25 °C	—	±1/4	±1	LSB
0 to +70 °C	—	±1/2	±1	LSB
Diff.Non–Linearity				
+25 °C	—	±1/2	±3/4	LSB
0 to +70 °C	–0.99	±1/2	±1.25	LSB
Full Scale Absolute Accuracy (See Technical Note 1)				
+25 °C	—	±0.13	±0.25	% FSR
0 to +70 °C	—	±0.15	±0.44	% FSR
Bipolar Zero Error, 0 to +70 °C (See Tech Note 1)	—	±0.2	±0.4	% FSR
Bipolar Offset Error, 0 to +70 °C (See Tech Note 1)	—	±0.2	±0.4	% FSR
Gain Error, 0 to +70 °C (See Tech Note 1)	—	±0.2	±0.4	%FSR
OUTPUTS				
Logic Levls				
Logic "1"	2.4	—	—	Volts dc
Logic "0"	—	—	0.4	Volts dc
Logic "1" Loading	—	—	–160	µA
Logic "0" Loading	—	—	6.4	mA
Resolution	12 Bits			
Output Coding	Offset binary			

DYNAMIC PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Peak Harmonic (–0.5 dB)				
DC to 500 kHz	—	–77	–72	FS –dB
500 kHz to 1.0 MHz	—	–72	–67	FS –dB
1.0 MHz to 2.5 MHz	—	–67	–65	FS –dB
Total Harm. Distort. (–0.5 dB)				
DC to 500 kHz	—	–80	–75	FS –dB
500 kHz to 1.0 MHz	—	–78	–77	FS –dB
1.0 MHz to 2.5 MHz	—	–76	–68	FS –dB
Signal–to–Noise Ratio (w/o distort., –0.5 dB)				
DC to 500 kHz	68	70	—	FS –dB
500 kHz to 1.0 MHz	66	69	—	FS –dB
1.0 MHz to 2.5 MHz	64	68	—	FS –dB
Signal–to–Noise Ratio ③ (with distortion, –0.5 dB)				
DC to 500 kHz	66	68	—	FS –dB
500 kHz to 1.0 MHz	64	67	—	FS –dB
1.0 MHz to 2.5 MHz	62	66	—	FS –dB
Two–Tone Intermodulation Distort. (ƒIN = 75 kHz, 105 kHz, Fs = 5 MHz, –7 dB	—	–83	–76	FS –dB
Two–Tone Intermodulation Distort. (ƒIN = 2.3 kHz, 2.5 MHz, Fs = 5 MHz, –0.5 dB)	—	–65	–63	FS –dB
Input Bandwidth				
Small Signal (–20 dB input)	50	65	—	MHz
Full Power (0 dB input)	30	40	—	MHz
Slew Rate	—	250	—	V/µSec..
Aperture Delay Time	—	—	10	nSec.
Effect. Aperture Delay Time	—	—	8	nSec.
Aperture Uncertainty (Jitter)				
(rms)	—	—	±10	pSec.
(peak)	—	—	±25	pSec.
Overvoltage Recovery Time	—	—	1000	nSec.
S/H Acquisition Time to 0.01% (Transient Recovery Time)	—	—	50	nSec.
Conversion Rate	5.0	—	—	MHz
POWER REQUIREMENTS				
Power Supply Range ①				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
–15V dc Supply	–14.25	–15.0	–15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
–5V dc Supply	–4.75	–5.0	–5.25	Volts dc
Power Supply Current				
+15V dc Supply	—	+32	+40	mA
–15V dc Supply	—	–4	–6	mA
+5V dc Supply ②	—	+170	+200	mA
–5 V dc Supply	—	–100	–120	mA
Power Dissipation	—	1.9	2.3	Watts
Power Supply Rejection	—	—	0.07	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range –MC	0	—	+70	°C
Thermal Impedance				
θ JC	—	TBD	—	°C/Watt
θ CA	—	TBD	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24–pin DIP			
Weight	0.42 ounces (12 grams)			

① For ±12V, +5V operation, contact DATEL
② +5V power usage at 1 TTL logic loading per data output bit.
③ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

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TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-118/ADS-118A to zero using the optional external circuitry shown in Figures 4a and 4b. The external adjustment circuit has no affect on the throughput rate.

2. Always connect the analog and digital grounds to a ground plane beneath the converter for best performance. The analog and digital grounds are not connected internally.

3. Bypass the analog and digital supplies to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor.

4. Users should use a single +5V supply for both analog +5V and digital +5V. Should users have separate supplies, the difference between the analog and digital supply should be within ±100 mV to avoid performance degradation.

5. To enable the ADS-118's three-state outputs, connect ENABLE 1–12 (pin 17) to a logic "0" (low). To disable them, connect pin 17 to a logic "1" (high). The three-state outputs are permanently enabled in the ADS-118A.

6. Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

7. Re-initiating the START CONVERT (pin 16) while $\overline{EOC}$ is a logic "1" (high) will result in a new conversion sequence.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Figure 4 for the appropriate full-scale range (FSR). Apply a pulse of 45 nanoseconds to the START CONVERT input (pin 16) at a rate of 250 kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 1 for bipolar zero adjustment (zero +1/2 LSB).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 1 for the bipolar gain adjustment (+FS -1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 2.

Table 1. Zero and Gain Adjust, Bipolar Operation

BIPOLAR FSR	ZERO ADJUST 0 + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB	PRODUCT
±1V dc ±1.25V	±244 µV dc ±305 µV	+0.99926V ±1.249075V	ADS-118 ADS-118A

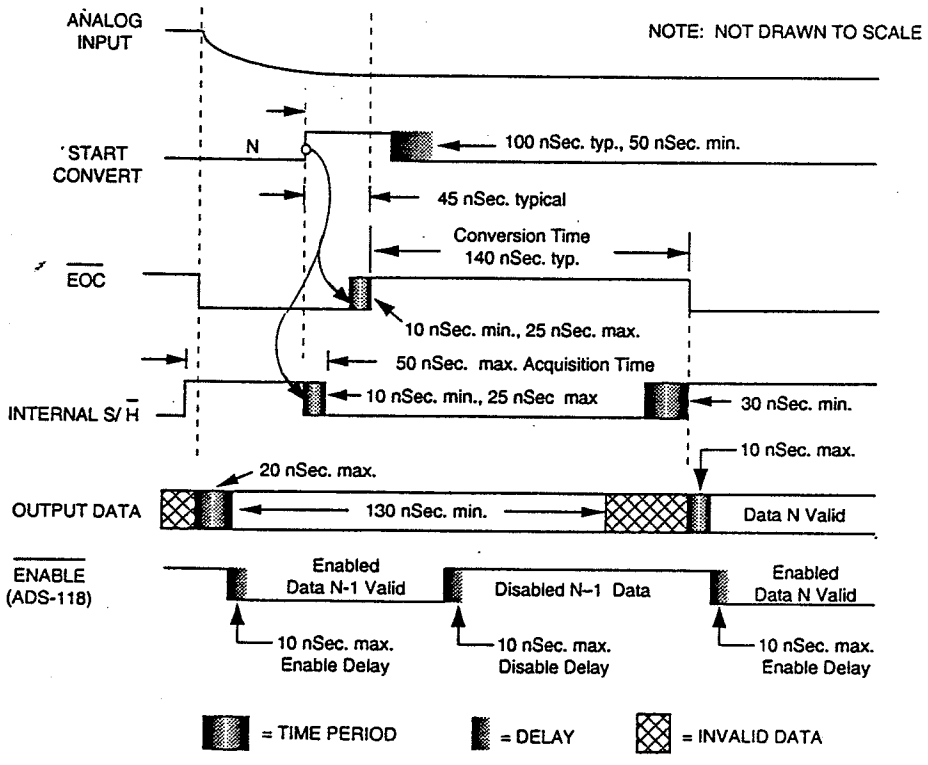


Figure 2. ADS-118 Timing Diagram

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Table 2. Output Coding for Bipolar Operation

BIPOLAR SCALE	ADS-118 INPUT RANGE (Volts dc) ±1V	OUTPUT CODING OFFSET BINARY MSB LSB	ADS-118A INPUT RANGE (Volts dc) ±1.25V
+FS –1 LSB	+0.99952V	1111 1111 1111	+1.2494V
+3/4 FS	+0.7500V	1110 0000 0000	+0.9375V
+1/2 FS	+0.5000V	1100 0000 0000	+0.6250V
0	0.0000V	1000 0000 0000	0.0000V
–1/2 FS	–0.5000V	0100 0000 0000	–0.6250V
–3/4 FS	–0.7500V	0010 0000 0000	–0.9375V
–FS +1 LSB	–0.99952V	0000 0000 0001	–1.2494V
–FS	–1.0000V	0000 0000 0000	–1.2500V

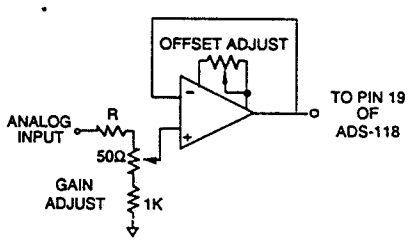


Figure 4a.
Optional Bipolar Calibration Circuit, ADS-118

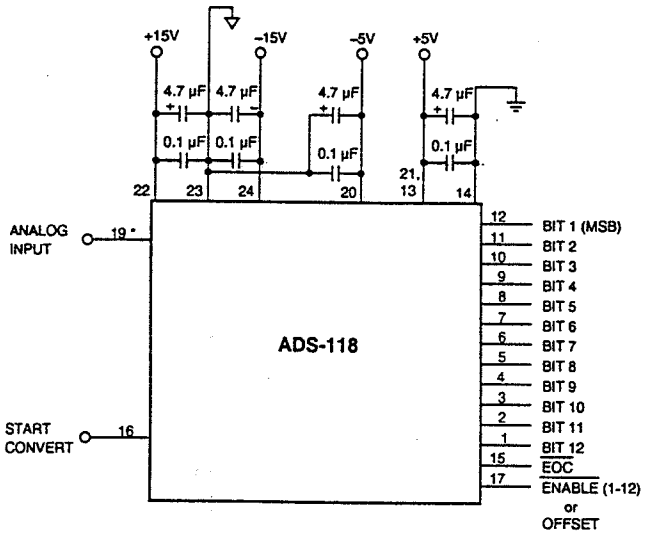


Figure 3. Typical ADS-118 Connection Diagram

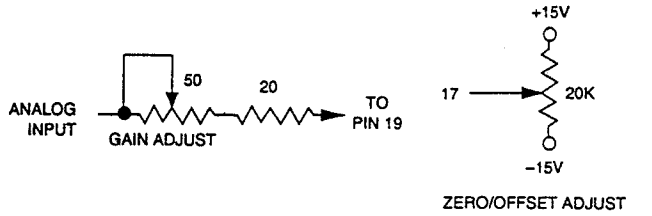


Figure 4b.
Optional Gain and Offset Adjust Circuits, ADS-118A

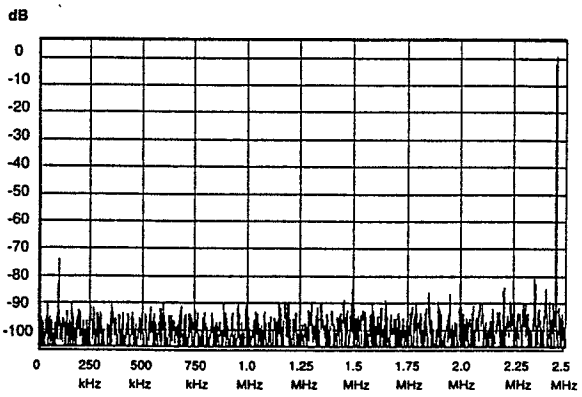
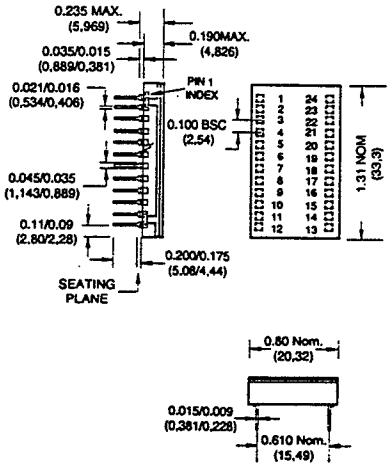


Figure 5. FFT Analysis of ADS-118

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-118MC	0 to +70 °C
ADS-118AMC	0 to +70 °C
ADS-EVAL2	Evaluation Board (without ADS-118)

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For availability of extended temperature range and MIL-STD-883 versions, contact DATEL.

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