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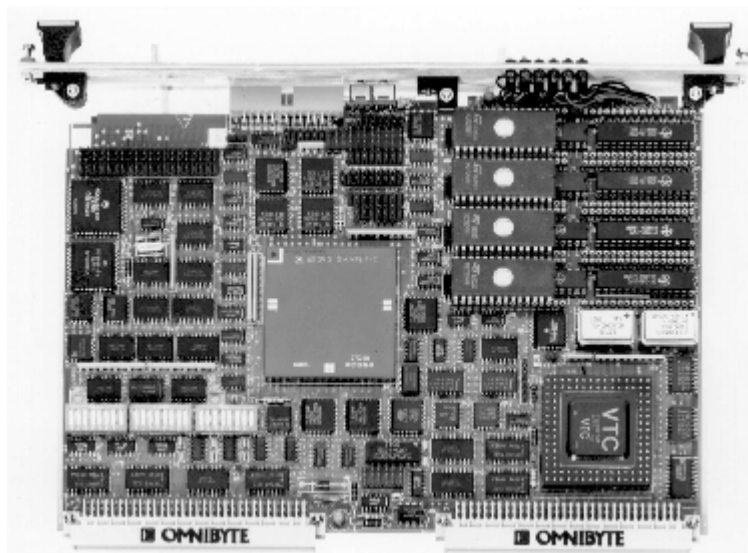
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Omnibyte's *OB68K/VME40** Motorola 68040 based VMEbus Single Board Computer



General Description

The Omnibyte OB68K/VME40 is a high performance single board computer featuring the 32-bit 68040, a large amount of static RAM and ROM and I/O flexibility through the use of [Omnimodules*](#).

It is ideal for embedded control or robotics applications where simplicity, computational speed and low cost are essential.

Features Include:

- Motorola 68040, 25 or 33MHz., 32-bit CPU.
- (8) 28 pin sockets for dual access, 32-bit wide static RAM (up to 256KB included).
- (8) 32 pin sockets for 32-bit wide ROM (4 sockets can be configured for EEPROM).
- (2) RS232C serial ports utilizing one 68681 DUART.
- (2) 8-bit or (1) 16-bit parallel port utilizing one 68230 PI/T.
- (1) 12-bit timer/counter (in 68681).
- (1) 24-bit timer/counter (in 68230).
- (1) Omnimodule* I/O module socket, capable of supporting a wide variety of standard or custom Omnimodules, (Standard Omnimodules do not violate VME above board height specifications).
- VIC068 VME interface controller, providing:
 - Mailbox interrupt.
 - 4 level bus arbiter.
 - Bus interrupter.
 - Unaligned transfer (UAT) support.
 - Multi-master bus arbitration.
- VMEbus (IEEE 1014) Rev. C.1 compatibility.
- VME40bug* terminal monitor/debugger and power-up diagnostic firmware program included.
- Two year limited warranty.

Specifications

Board Dimensions:

6.30in. (160mm) x 9.19in. (234mm) 0.062in.(1.6mm) (multilayer) FR4 printed circuit board

Master Data Transfer Options:

A32:A24:A16 D32:D16:D08 (EO) UAT (DYN)

Slave Data Transfer Options:

RAM-A32:A24 D32:D16:D08 (EO) (DYN)

Mailbox Interrupt:

A16 D32:D16:D08 (EO) (DYN)

Tout 4us, 16us, 32us, 64us, 128us, 256us, 480us and Disabled (DYN)

Address Modifier Options:

Any one of 29, 2D 39, 3A, 3D, 3E, 09, OA, OD, OE (DYN)

Arbiter Options:

PRI Fixed Priority, RRS Round Robin Select, 4 Level (STAT)

Requester Options:

Any R(0-3) (DYN) Any one of ROR (Release on Request) RWD (Release when Done) (STAT) Fair requestor mode

Interrupt Handler Options:

Any of IH (1-7) (DYN)

Interrupter Options:

Any of I (I -7) (DYN)

Environmental Options:

Operating temperature: 0 to 65 degrees C.

Operating humidity: 0-90% (non-condensing)

Power Options:

5.8A (typ) at +5VDC +/-5%

20mA (typ) at +12VDC +/-5%

15mA (typ) at -12VDC +/-5%

without Omnimodule

Physical Configuration Options:

EXP Expanded Bus, Double VMEbus Board

MC68040 Processor

The MC68040 is Motorola's third generation of MC68000-user object code compatible, high performance, 32-bit microprocessors. The MC68040 is a virtual memory microprocessor employing multiple, concurrent execution units and a highly integrated architecture to provide very high performance in a monolithic HCMOS device. The MC68040 integrates an MC68030-compatible integer unit, an MC68882-compatible floating-point unit (FPU), dual independent demand paged memory management units (MMUs) for instruction and data stream accesses, and independent 4K-byte instruction and data caches. A high degree of instruction execution parallelism is achieved through the use of multiple independent execution pipelines, multiple internal buses, and a full internal Harvard architecture, including the separate physical caches for both instruction and data accesses. Cache functionality is enhanced by the inclusion of on-chip bus snooping logic to directly support cache coherency in multimaster applications.

Instruction execution is pipelined in both the integer unit and FPU, which interface to fully independent data and instruction memory units. Each memory unit consists of an MMU, an address translation cache (ATC), a main cache, and a snoop controller. The ATCs decrease logical-to-physical address translation overhead by storing recently-used translations, while the bus snooper circuit ensures cache coherency in multimaster applications. External memory requests from each cache are prioritized by the bus controller, which executes bus transfers on the external bus.

Memory

The RAM of the OB68K/VME40 has been designed for fast access "Skinny Dip" static RAM. This will allow the board to attain zero-wait-state operation at currently available processor speeds. The static RAM is arranged in 2 banks of four sockets yielding a maximum RAM configuration of 256KB, 32-bit wide RAM. The RAM is dual-access from the processor and the VMEbus. The board comes standard with 256KB of RAM.

ROM is also arranged as (2) banks of (4) 32 pin sockets. One bank can be configured as EEPROM using 8k x 8 parts or larger. The ROM sockets will accept 27256, 27512, 271024, 272048, 274096 and 278192 parts.

VIC068

The VME Interface Controller (VIC068) is a single chip designed to minimize the cost and board area requirements and to maximize performance of the VMEbus interface of a VMEbus master/slave module. The VIC068 was designed using VTC's high-performance standard cells on an advanced 1 micron CMOS process. The VIC068 provide all VMEbus system controller functions. The VIC068 utilizes output buffers based on VTC's patented and military approved ACL product family. These CMOS high drive buffers provide direct connection to the address and data lines.

In addition to these signals, the VIC068 connects directly to the arbitration, interrupt, address modifier, utility and strobe lines. Signals are provided which control data direction and latch functions needed for a 32-bit implementation.

The VIC068 was developed through the joint efforts of both VTC and a consortium of board vendors, under the auspices of the VMEbus International Trade Association (VITA). The VIC068 thus offers an implementation that provides inputs from a wide array of users which maximizes the number of applications. This also ensures compatibility between boards designed by different manufacturers.

I/O

Both serial and parallel I/O are provided on the OB68K/VME40. Two RS232C buffered serial ports are implemented using a 68681 DUART. One port is brought out to the front panel using a 26-pin connector. Both serial ports are also brought out to the P2 connector. A software controlled baud rate generator permits the selection of 1 of 18 standard baud rates (50-38.4K baud) and has independent baud rate selection for each port.

The 68230 parallel interface/timer (PIT) provides 16-bits of undedicated binary I/O and 4 hand shake lines. The PIT is organized as two 8-bit ports with two control lines each or one 16 bit port with four control lines. The parallel I/O is brought out to the P2 connector only.

Additional I/O functions on the OB68K/VME40 can be implemented through Omnimodule I/O module daughter boards. The Omnimodule plugs into the socket on the OB68K/VME40. The modules have a low profile and do not violate the VMEbus above board height specification, allowing the OB68K/VME40 with I/O module to fit into just one slot. I/O lines are brought out to the front panel and the P2 connector. A wide variety of I/O can be implemented using the following available Omnimodules:

- OM/2SA2 - (2) RS232C asynchronous I/O ports using one 68681 DUART with baud rates up to 38.4K baud.
- OM/20PUB - (20) lines of unbuffered parallel I/O using one 68230 PUT.
- OM/KLUGE - Blank wire-wrap kluge board.

- OM/SCSI - SCSI controller.
- OM/2SAS2 - (2) RS232C asynchronous/synchronous I/O ports using one 68564 with baud rates up to 1000K baud.
- OM/2SA4 - (2) RS422 asynchronous I/O ports using one 68681 DUART.
- OM/488 - IEEE 488 GPIB controller.
- OM/8SA2 - (8) RS232C asynchronous I/O ports using one SCC2698A.
- OM/CPI - Centronics printer interface.
- OM/AD-DA1 - Analog to digital, digital to analog I/O.
- And more...

Ordering Information

OB68K/VME40-XXX-ZZ

Where:

XXX is RAM size (256=256KB (standard))

ZZ is processor speed (25=25MHz, 33=33MHz)

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