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USER MANUAL

Accessory 5E

UMAC MACRO and I/O

3Ax-603437-xUxx

September 30, 2009

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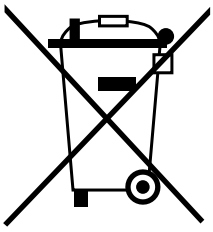
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REVISION HISTORY				
REV.	**DESCRIPTION**	**DATE**	**CHG**	**APPVD**
1	CORRECTIONS TO JIO PLC	08/02/06	CP	S.FIERRO, S.SATTARI
2	CORRECTIONS FOR PFM OUTPUT SETUP	09/21/06	CP	S.SATTARI
3	ADDED UL SEAL TO MANUAL COVER UPDATED AGENCY APPROVAL/SAFETY ENTRY	09/30/09	CP	S.FIERRO

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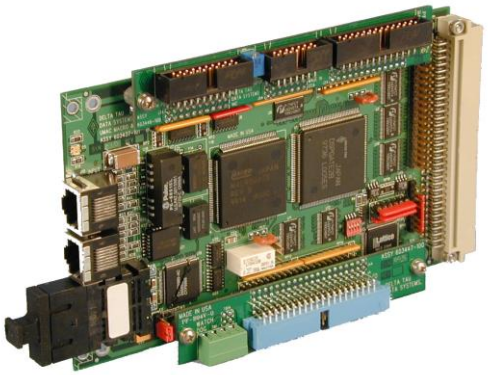
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INTRODUCTION

Delta Tau's Universal Motion and Automation Controller (UMAC) combines the power of the PMAC controller with an integrated packaging and connectivity strategy that gives the user revolutionary flexibility and ease of use. The UMAC consists of a set of 3U format Euro-cards (100 x 160 mm) that can be assembled in a variety of different strategies.

The Acc-5E UMAC MACRO and I/O accessory (P/N 300-603437-10X) provides the interface capabilities for the LCD Display port, handwheel port, general purpose I/O port, thumbwheel port, and MACRO in both fiber and wire formats.

Acc-5E Board Options



Acc-5E: UMAC I/O and MACRO Accessory
(Shown w/OPT2 & OPTB installed)

This 3U-size rack-mounted board provides four general-purpose (non-servo) I/O ports for the UMAC:

1. The JDISP display port
2. The JTHW multiplexor port
3. The JIO general-purpose I/O port
4. The JHW handwheel port

These are the same ports that are present along the top of a PC-bus PMAC2 or out the front of a VME-bus PMAC2. Optionally, it can also provide a 16-node or 32-node MACRO-ring interface. It connects to the CPU board through the UBUS backplane expansion port. It is intended for Pack use only.

- **Option A:** 16-node MACRO Interface with SC-style fiber-optic transceiver
- **Option B:** 16-node MACRO interface with SC-style fiber-optic transceiver and RJ-45 electrical connector
- **Option C:** 16-node MACRO interface with RJ-45 electrical connectors
- **Option 2:** Additional 16 nodes of MACRO interface (32 nodes total). Requires Option A, B, or C.

Note:

To use with RJ45 option, the user must write a one to location X:$78F10,6 at power-on.

Acc-5E Port Summary

JIO Port – 32-bit IO

The JIO port has 32 bits of inputs and outputs that can be software configured as inputs or outputs on a byte-by-byte basis. The following table lists the possible input/out schemes possible with the Acc-5E JIO port.

The user can configure the system to have:

- 32 inputs and no outputs
- 24 inputs and 8 outputs
- 16 inputs and 16 outputs
- 8 inputs and 24 outputs
- 0 inputs and 32 outputs

Since the 40-pin connector for this port is not an industry standard, the Acc-21A was created to give the user the capability to use Acc-5E's JIO port with OPTO 22 or Grayhill style I/O module racks. The Acc-21A can be used with the 8, 16, 24, or 32 module boards from these manufacturers.

JHW Port – Handwheel Port

The handwheel port can be used to bring in two quadrature encoders, pulse and direction encoders, or MLDT feedback devices. The encoders have a maximum input frequency of up to 40 MHz (the default is 10 MHz). These encoders can be processed in the encoder conversion table of the UMAC Turbo and used as either extra feedback devices or as the name implies for handwheels. The only limitation we have for the encoder inputs on the JHW port is that we do not provide an input for the index pulse of the encoder

Another function of the handwheel port is that it gives the user access to two auxiliary pulse and direction outputs. These outputs could be used for standard pulse and direction encoders, general-purpose pulse outputs, or as the main frequency output for MLDT feedback devices.

JDIS – Display Port

For many applications a 40×2 character display might be needed to display text messages about the machine process or to display axis position. The JDIS connector allows connection of the Acc-12 or Acc-12A liquid crystal displays, or of the Acc-12C vacuum fluorescent display. Both text and variable values may be shown on these displays through the use of the **`DISPLAY`** command, executing in either motion or PLC programs.

JTHW – Multiplexer Port

The JTHW multiplexer port has 16 discrete digital I/O lines for general purpose use. The lines are configurable by byte for input or output (on the DSPGATE2 I/O IC, the lines are individually configurable for input or output, but the buffer ICs are only byte-configurable), and individually configurable for inverting or non-inverting format.

The multiplexer port allows us to multiplex data from up to 32 different cards into one port. The cards designed for this port are used for retrieving absolute position data from R/D converters or Yaskawa Absolute encoders and general purpose IO from the Acc-34xx family of IO cards.

TB1 – Watchdog Relay Connector

The TB1 connector allows the user to send an output from the UMAC system to the machine if a watchdog condition has occurred at the UMAC. This is an important safety feature because the UMAC is effectively disabled when it is in a watchdog condition and this will allow the other machine hardware/logic to bring the machine to a safe condition.

Note

Accessory Boards from Revision -104 and higher have logic which causes the watchdog relay to appear tripped when either a watchdog condition occurs or power is removed from the UMAC rack.

This causes the relay to operate in the opposite condition from the earlier revisions of this board.

MACRO Communication Port Connections

The MACRO IO connections allow the user to control up to 16 motors/actuators and service up to 864 bits of IO using the Delta Tau MACRO protocol. MACRO allows the user to service motors and IO at locations up to 1 km away from the UMAC Turbo CPU.

SPECIFICATIONS

Environmental Specifications

Description	Specification	Notes
Operating Temperature	0°C to 45°C,	
Storage Temperature	-25°C to 70°C	
Humidity	10% to 95 % non-condensing	

Physical Specifications

Description	Specification	Notes
Dimensions	Length: 16.256 cm (6.4 in.) Height: 10 cm (3.94 in.) Width: 2.03 cm (0.8 in.)	
Weight (max)	192 g	With Option 2
Terminal Block Connectors	FRONT-MC1,5/3-ST3,81	Terminal Blocks from Phoenix Contact. UL-94V0
IDC Connectors	16-pin box header connector 20-pin box header connector 26-pin box header connector 40-pin box header connector	Thermoplastic, UL-94V0
The width is the width of the front plate. The length and height are the dimensions of the PCB.		

Electrical Specifications

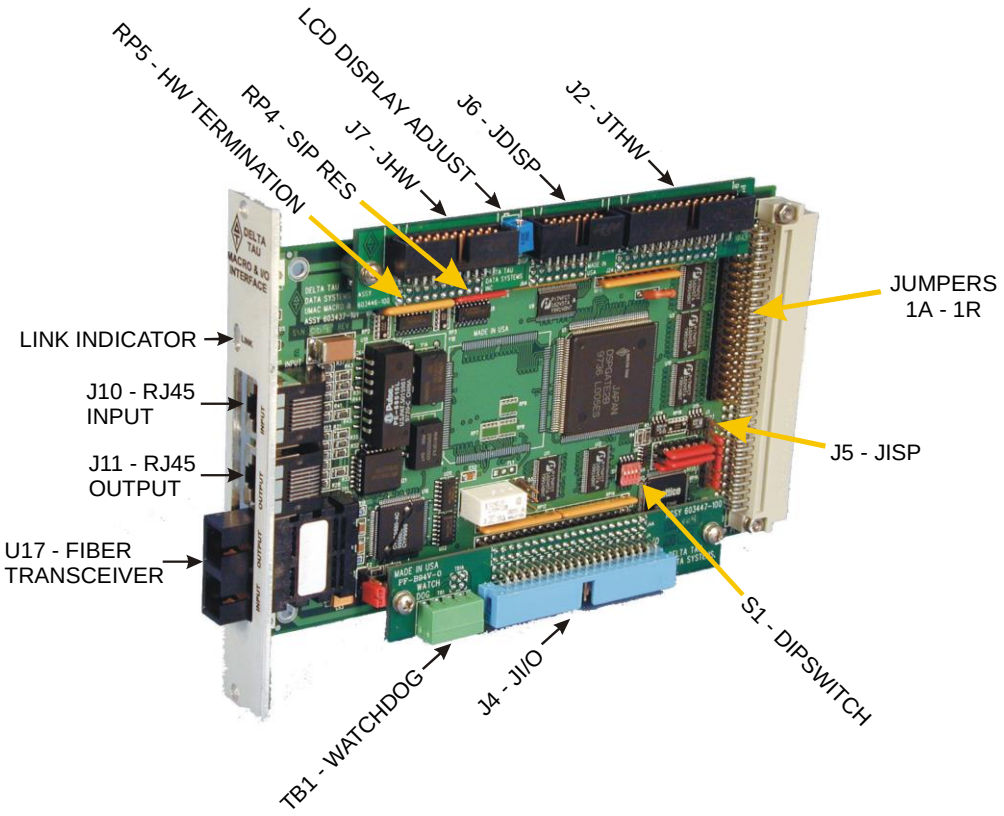
Description	Specification	Notes
ACC-5E	5V @ 0.92A (±10%)	
ACC-5E with Option 2	5V @ 1.20A (±10%)	

Agency Approval and Safety

Item	Description
CE Mark	Full Compliance
EMC	EN55011 Class A EN61000-3-2 EN61000-3-3 EN61000-4-2 EN61000-4-3 EN61000-4-4 EN61000-4-5 EN61000-4-6 EN61000-4-11
Safety	EN 61010-1
UL	UL 61010-1 File E314517
cUL	CAN/CSA C22.2 No. 1010.1-92 File E314517
Flammability Class	UL 94V-0

ACC-5E HARDWARE SETTINGS AND PORT SELECTION

The picture below shows the location of jumpers, resistor packs, dipswitch, and connectors:



MACRO & I/O Card Layout
(Shown w/OPTB installed)

Note:

The Acc-5E accessory shown here is not the exact revision of the circuit board that is currently distributed. However, all the components represented here exist on current revisions.

Jumper J1 MLT-3 Select

Use this jumper to select MLT-3 encoding for MACRO with wired RJ45 connectors. Many of the newer wired MACRO interfaces require that this jumper be selected for MLT-3 protocol transmission.

J1 when jumpered from position 1-2 deselects the MLT-3 PHY layer protocol.

J1 when jumpered from position 2-3 selects the MLT-3 PHY layer protocol.

Jumpers E1A - E1R Backplane Thumbwheel Port Connection

Install these 16 shorting bars when the backplane is used for thumbwheel port functions.

The UBUS Specification does not require these lines to be connected and these backplane lines may actually be used for other purposes.

Normally these jumpers are not installed.

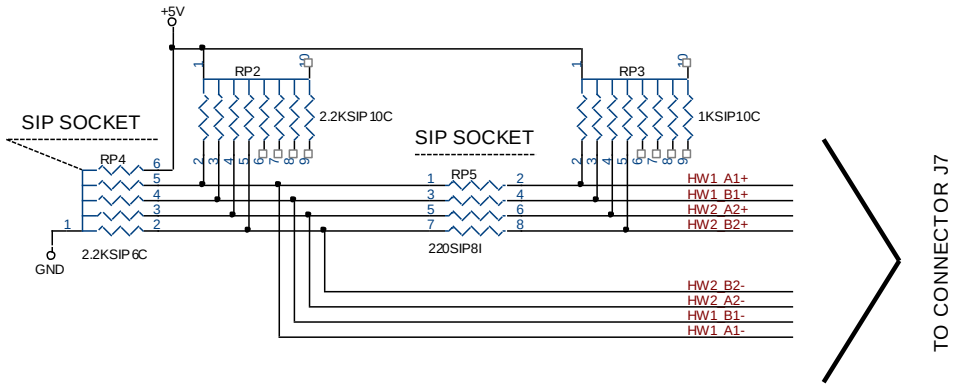
RP4: SIP Resistor

This common bussed 6-pin resistor pack is used to select between single-ended and differential handwheel encoder inputs.

When placed with pin 1 of the resistor pack at pin 1 of the SIP socket, this resistor pack biases the negative side of the differential handwheel encoder inputs to 2.5Vdc. This is the configuration for single-ended encoders.

When placed with pin 1 of the resistor pack at pin 6 of the SIP socket, this resistor pack biases the negative side of the differential handwheel encoder inputs to 5Vdc. This is the configuration for differential encoders.

Refer to the schematic below for the handwheel encoder input circuit:



RP5: SIP Resistor

This 8-pin resistor pack has four individual resistors that are used to apply a termination resistance between differential handwheel encoder inputs.

Remove this resistor pack when using single-ended encoders to reduce a threshold shift that occurs when there is no negative side input.

Refer to the schematic above for the application of RP5 in the handwheel encoder circuit.

S1: Dipswitch UBUS MACRO IC Base Address

This 4-position dipswitch is used to select the UBUS address for the Acc-5E.

Acc-5E Mapping Table {CS4 Mappings}							
MACRO & I/O SW1 Settings				Turbo PMAC MACRO IC # (m)	Base Channel Address	2nd Gate Array Base Address (OPT2)	Config. Ident. Address
4	3	2	1				
on	on	on	on	0	$78400	$79400	$78F10
on	on	on	off	1	$79400	$7A400	$79F10
on	on	off	on	2	$7A400	$7B400	$7AF10
on	on	off	off	3	$7B400	$78500	$7BF10
on	off	on	on	4	$78500	$79500	$78F14
on	off	on	off	5	$79500	$7A500	$79F14
on	off	off	on	6	$7A500	$7B500	$7AF14
on	off	off	off	7	$7B500	$78600	$7BF14
off	on	on	on	8	$78600	$79600	$78F18
off	on	on	off	9	$79600	$7A600	$79F18
off	on	off	on	10	$7A600	$7B600	$7AF18
off	on	off	off	11	$7B600	$78700	$7BF18
off	off	on	on	12	$78700	$79700	$78F1C
off	off	on	off	13	$79700	$7A700	$79F1C
off	off	off	on	14	$7A700	$7B700	$7AF1C
off	off	off	off	15	$7B700	Not Available	$7BF1C

The memory mapping for the UBUS MACRO and I/O accessory allows 16 channels to be selected. The dipswitch selects between any of the 16 banks of memory. This allows for up to 16 Acc-5Es to be logically configured.

Note:

The Acc-5E defines the mapping for its memory depending upon whether it is a single gate array or dual gate array device. The dual gate option for the Acc-5E is OPT-2.

The second gate array base addresses are shown in the last column of the table.

Therefore, although there are 16 slots to place the Acc-5E into, these same slots may be occupied by MACRO accessory cards that have OPT2 installed. When this occurs, the accessory card occupies the equivalent of two slots and, therefore there may be fewer slots available for addressing. Be careful to allow for OPT2 addressing when more than one Acc-5E card is used.

Note:

The Acc-5E with OPT-2 installed occupies two slots of address space. However, there is only one CS16-identification register for the accessory card even when OPT-2 is installed.

MACRO Communications Port Selection

By default, the Acc-5E is setup to communicate via the Fiber Optic (option A) ports. The Acc-5E does not have any hardware jumpers to allow the user to select the Fiber Optic or RJ45 MACRO communications. To switch from Fiber Optic mode to RJ45 mode the user must write to a memory location at power up and this location is found at X:$78F10,6 (if Acc-5E base address is $78400). Again, by default, this location is set to 0 so most Fiber Optic MACRO users will not have to worry about this location.

For RJ45 Communications Option:

```
M4000->X:$78F10,6              ;Acc-5e Communications Port Selection Bit
M4000=1                        ;Set to 1 for RJ45 communications
```

For Fiber Optics Communications Option (redundant because this is the default value):

```
M4000->X:$78F10,6              ;Acc-5e Communications Port Selection Bit
M4000=0                        ;Set to 0 for Fiber Optics communications.
                               ;Default power-on value
```

Example Power-on PLC for RJ45 communications

```
OPEN PLC1 CLEAR
M4000=1                        ;set to 1 for RJ45 communications
DIS PLC1
CLEAR
```

Communications Port Configuration Table

Acc-5E Base Address	Port Config Register
$78400	X:$78F10,6
$79400	X:$79F10,6
$7A400	X:$7AF10,6
$7B400	X:$7BF10,6
$78500	X:$78F14,6
$79500	X:$79F14,6
$7A500	X:$7AF14,6
$7B500	X:$7BF14,6
$78600	X:$78F18,6
$79600	X:$79F18,6
$7A600	X:$7AF18,6
$7B600	X:$7BF18,6
$78700	X:$78F1C,6
$79700	X:$79F1C,6
$7A700	X:$7AF1C,6
$7B700	X:$7BF1C,6

I/O CONFIGURATION

Two ports on the Accessory 5E may be used for general purpose I/O, the JIO (J4) port and the JTHW (J2) port. Although their setup is similar to setting them up for a PMAC2 PC, there are some addressing differences which need to be made clear.

Multiplexer Port JTHW (J2) Setup

The JTHW multiplexer port has 16 discrete digital I/O lines for general-purpose use. The lines are configurable by byte for input or output (on the DSPGATE2 I/O IC, the lines are individually configurable for input or output, but the buffer ICs are only byte-configurable), and individually configurable for inverting or non-inverting format.

Hardware Characteristics

When configured as an output, each line has a 5V CMOS totem-pole driver. This driver can sink or source up to 20 mA. There is a 10 κ pull-up resistor to 5V on each line for input purposes, but the driver IC can hold the line high or low despite this resistor. When configured as an input, the buffer IC presents a high-impedance input either sinking or sourcing; no significant current will flow. The pull-up resistor on the line will bias the line high in the absence of anything actively pulling the line low at significantly lower impedance.

Suggested M-Variables

The 16 I/O lines are memory-mapped into PMAC's address space in register Y:$C082. Typically, these lines are used as a unit with specially designed multiplexing I/O accessories and appropriate multiplexing M-variables (TWB, TWD, TWR, and TWS formats), in which case PMAC2 handles the direct control of these I/O lines automatically. However, these lines can also be accessed individually with M-variables. Following is a suggested set of M-variable definitions to use these data lines:

```
M40->Y:$078402,8              ; SEL0 Line; J2 Pin 4
M41->Y:$078402,9              ; SEL1 Line; J2 Pin 6
M42->Y:$078402,10             ; SEL2 Line; J2 Pin 8
M43->Y:$078402,11             ; SEL3 Line; J2 Pin 10
M44->Y:$078402,12             ; SEL4 Line; J2 Pin 12
M45->Y:$078402,13             ; SEL5 Line; J2 Pin 14
M46->Y:$078402,14             ; SEL6 Line; J2 Pin 16
M47->Y:$078402,15             ; SEL7 Line; J2 Pin 18
M48->Y:$078402,8,8,U          ; SEL0-7 Lines treated as a byte
M50->Y:$078402,0              ; DAT0 Line; J2 Pin 3
M51->Y:$078402,1              ; DAT0 Line; J2 Pin 5
M52->Y:$078402,2              ; DAT0 Line; J2 Pin 7
M53->Y:$078402,3              ; DAT0 Line; J2 Pin 9
M54->Y:$078402,4              ; DAT0 Line; J2 Pin 11
M55->Y:$078402,5              ; DAT0 Line; J2 Pin 13
M56->Y:$078402,6              ; DAT0 Line; J2 Pin 15
M57->Y:$078402,7              ; DAT0 Line; J2 Pin 17
M58->Y:$078402,0,8,U          ; DAT0-7 Lines treated as a byte
```

Direction Control

In the default configuration set automatically at power-up/reset, DAT0 to DAT7 are set up as non-inverting inputs; SEL0 to SEL7 are set up as non-inverting outputs with a zero (low voltage) value. If any of the multiplexer port accessories are to be used, this configuration must not be changed.

The direction control bit for each of these I/O bits is located in the corresponding bit in the matching X register. For example, the direction control bit for DAT3 is located at X:$78402,3; the direction control bit for SEL6 is located at X:$78402,14.

Because the buffer ICs can only be switched by byte, it is best to define 8-bit M-variables for the direction control. Suggested definitions are:

```
M60->X:$078402,0,8            ; Direction control for DAT0 to DAT7
M62->X:$078400,8,8            ; Direction control for SEL0 to SEL7
```

These M-variables should take values of 0 or 255 ($FF) only; 0 sets the byte to input, 255 sets the byte to output.

In addition, the bi-directional buffer IC for each byte has a direction control line accessible as a software control bit. These control lines and bits must match the ASIC direction bits. In the UMAC version of the Turbo PMAC2, the buffer direction control bits are at UMAC address Y:$78F10,11 and Y:$78411,8. These address are based off the Configuration Identification Address chosen by the dip switch S1 setting. A bit value of 0 specifies input; 1 specifies output.

Suggested M-variable definitions are:

```
M61->Y:$78F10,11              ; Buffer direction control for DAT0 to DAT7
M63->Y:$78F11,8               ; Buffer direction control for SEL0 to SEL7
```

If it is desired to change either of these I/O bytes, it must be done by user programs (usually this is done in PLC 1 acting as a reset PLC, scanning through once on power-up/reset, then disabling itself).

Inversion Control

Each line on the JTHW port is individually controllable as to whether it is an inverting I/O point (0=+5V; 1=0V) or a non-inverting I/O point (0=0V; 1=+5V).

Register X:$78406 contains the inversion control bits:

X:$78406 bits 0 to 7 control DAT0 to DAT7, respectively
X:$78406 bits 8 to 15 control SEL0 to SEL7, respectively

A value of 0 in the control bit sets the corresponding I/O point as non-inverting. A value of 1 in the control bits sets the corresponding I/O point as inverting. At power-up/reset, PMAC automatically sets all of the I/O points on the JTHW port as non-inverting. To use any of the multiplexed I/O accessory boards on the JTHW port, all I/O points on the port must be left non-inverting.

Alternate Uses

Because of the byte-wide direction-control buffer ICs, it is not possible to use all of the I/O points on the JTHW in their alternate uses.

Each general-purpose I/O point on the JTHW port has an alternate use as a supplemental fixed-use I/O point on a supplemental machine interface channel (1* or 2*). The points are individually controllable as to general-purpose use or fixed use by control register Y:$78406. Refer to this register in the memory-I/O map to see the alternate uses of each point. At power-up/reset, UMAC sets up all of the I/O points on the port for general-purpose use automatically.

JIO (J4) Setup

The JIO port has 32 discrete digital I/O lines for general-purpose use. The lines are configurable by byte for input or output (on the DSPGATE2 I/O IC, the lines are individually configurable for input or output, but the buffer ICs are only byte-configurable), and individually configurable for inverting or non-inverting format.

Hardware Characteristics

Because all of these lines default to inputs at power-up/ reset, any lines used as outputs will pull to +5V at power-up/reset until software configures them as outputs.

When configured as an output, each line has a 5V CMOS totem-pole driver. This driver can sink or source up to 20 mA. There is a 10 κ pull-up resistor to 5V on each line for input purposes, but the driver IC can hold the line high or low despite this resistor. When configured as an input, the buffer IC presents a high-impedance sinking input; no significant current will flow. The pull-up resistor on the line will bias the line high in the absence of anything actively pulling the line low at significantly lower impedance.

Suggested M-Variables

The 32 I/O lines are memory-mapped into UMAC's address space in the registers Base Address and Base Address+1, depending on SW2 settings. Typically these I/O lines are accessed individually with M-variables. Following is a suggested set of M-variable definitions to use these data lines with a base address of $78400:

```
M0->Y:$78400,0                ; I/O00 Data Line; J3 Pin 1
M1->Y:$78400,1                ; I/O01 Data Line; J3 Pin 2
M2->Y:$78400,2                ; I/O02 Data Line; J3 Pin 3
M3->Y:$78400,3                ; I/O03 Data Line; J3 Pin 4
M4->Y:$78400,4                ; I/O04 Data Line; J3 Pin 5
M5->Y:$78400,5                ; I/O05 Data Line; J3 Pin 6
M6->Y:$78400,6                ; I/O06 Data Line; J3 Pin 7
M7->Y:$78400,7                ; I/O07 Data Line; J3 Pin 8
M8->Y:$78400,8                ; I/O08 Data Line; J3 Pin 9
M9->Y:$78400,9                ; I/O09 Data Line; J3 Pin 10
M10->Y:$78400,10              ; I/O10 Data Line; J3 Pin 11
M11->Y:$78400,11              ; I/O11 Data Line; J3 Pin 12
M12->Y:$78400,12              ; I/O12 Data Line; J3 Pin 13
M13->Y:$78400,13              ; I/O13 Data Line; J3 Pin 14
M14->Y:$78400,14              ; I/O14 Data Line; J3 Pin 15
M15->Y:$78400,15              ; I/O15 Data Line; J3 Pin 16
M16->Y:$78400,16              ; I/O16 Data Line; J3 Pin 17
M17->Y:$78400,17              ; I/O17 Data Line; J3 Pin 18
M18->Y:$78400,18              ; I/O18 Data Line; J3 Pin 19
M19->Y:$78400,19              ; I/O19 Data Line; J3 Pin 20
M20->Y:$78400,20              ; I/O20 Data Line; J3 Pin 21
M21->Y:$78400,21              ; I/O21 Data Line; J3 Pin 22
M22->Y:$78400,22              ; I/O22 Data Line; J3 Pin 23
M23->Y:$78400,23              ; I/O23 Data Line; J3 Pin 24
M24->Y:$78401,0               ; I/O24 Data Line; J3 Pin 25
M25->Y:$78401,1               ; I/O25 Data Line; J3 Pin 26
M26->Y:$78401,2               ; I/O26 Data Line; J3 Pin 27
M27->Y:$78401,3               ; I/O27 Data Line; J3 Pin 28
M28->Y:$78401,4               ; I/O28 Data Line; J3 Pin 29
M29->Y:$78401,5               ; I/O29 Data Line; J3 Pin 30
M30->Y:$78401,6               ; I/O30 Data Line; J3 Pin 31
M31->Y:$78401,7               ; I/O31 Data Line; J3 Pin 32
```

Direction Control

The direction control bit for each of these I/O bits is located in the corresponding bit in the matching X register. For example, with the base address set at $78400 the direction control bit for I/O03 is located at X:$78400,3; the direction control bit for I/O30 is located at X:$78401,6. Because the buffer ICs can only be switched by byte, it is best to define 8-bit M-variables for the direction control. Suggested definitions are:

```
M32->X:$78400,0,8             ; Direction control for I/O00 to I/O07
M34->X:$78400,8,8             ; Direction control for I/O08 to I/O15
M36->X:$78400,16,8            ; Direction control for I/O16 to I/O23
M38->X:$78401,0,8             ; Direction control for I/O24 to I/O31
```

These M-variables should take values of 0 or 255 ($FF) only; 0 sets the byte to input, 255 sets the byte to output. The default values are zero for all of the above registers.

In addition, the bidirectional buffer IC for each byte has a direction control line accessible as a software control bit. These control lines and bits must match the ASIC direction bits. The buffer direction control bits are at the UMAC Configuration Identification Address (depends on SW2), with bits 7 to 10 controlling the four bytes of the JIO port. A bit value of 0 specifies input; 1 specifies output. With base address of $78400, the suggested M-variable definitions are:

```
M33->Y:$78F10,7               ; Buffer direction control for I/O00 to I/O07
M35->Y:$78F10,8               ; Buffer direction control for I/O08 to I/O15
M37->Y:$78F10,9               ; Buffer direction control for I/O16 to I/O23
M39->Y:$78F10,10              ; Buffer direction control for I/O24 to I/O31
```

In the default configuration automatically set at power-up/reset, I/O00 to I/O31 are set up as inputs (M32 through M39 = 0). This is done for maximum safety; no lines can be forced into an undesirable high or low state. Any of these lines that are to be used as outputs must be changed to outputs by user programs (usually this is done in PLC 1 acting as a reset PLC, scanning through once on power-up/reset, then disabling itself).

Inversion Control

Each line on the JIO port is individually controllable as to whether it is an inverting I/O point (0=+5V; 1=0V) or a non-inverting I/O point (0=0V; 1=+5V). For base address $78400, registers X:$78404 and X:$78405 contain the inversion control bits:

```
X:$78404 bits 0 to 23 control I/O00 to I/O23, respectively
X:$78405 bits 0 to 7 control I/O24 to I/O31, respectively
```

Suggested M-Variable definitions

```
m41->x:$78404,0,8
m42->x:$78404,8,8
m43->x:$78404,16,8
m44->x:$78405,0,8
m45->x:$78404,0,24
```

A value of 0 in the control bit sets the corresponding I/O point as inverting. A value of 1 in the control bits sets the corresponding I/O point as non-inverting. At power-up/reset, UMAC sets all of the I/O points on the JIO port as inverting automatically. On power up, all of the inputs are at zero and pulled up to 5V.

Alternate Uses

The direction-control of the buffer ICs must be set properly for the alternate uses of the I/O points, just as for the general-purpose I/O uses. These lines must be set properly at power up.

Each general-purpose I/O point on the JIO port has an alternate use as a supplemental fixed-use I/O point on a supplemental machine interface channel (1* or 2*). The default setting of configures this port for the general purpose I/O. To use the supplemental channel registers, then set these bits to 0 at power up to use each line as a general-purpose I/O point**.** The points are controlled individually for general-purpose use or fixed use by control registers Y:$78404 and Y:$78405, when base address is at $78400. Refer to these registers in the memory-I/O map to see the alternate uses of each point. At power-up/ reset, UMAC sets up all of the I/O points on the port for general-purpose use automatically.

Suggested M-Variable Definitions

```
M46->Y:$78404,0,24            ;setup for IO0-23
M47->Y:$78405,0,8             ;setup for IO24-32
```

Example Setup of JIO

If the above definitions were made, set these variables to their proper values in an initialization PLC. This example sets up the first two bytes as outputs and the second two bytes as inputs, all set to non-inverting. The following technique can be used for an initialization PLC:

```
#define DIR_CONTROL_1          m32
#define BUFF_CONTROL_1         m33
#define DIR_CONTROL_2          m34
#define BUFF_CONTROL_2         m35
#define DIR_CONTROL_3          m36
#define BUFF_CONTROL_3         m37
#define DIR_CONTROL_4          m38
#define BUFF_CONTROL_4         m39
#define INV_CTRL_0_23          m45
#define INV_CTRL_24_31         m44
#define Alt_use_0_23           m46
#define Alt_use_24_31          m47

OPEN PLC 6 CLEAR
DIR_CONTROL_1 = 255            ;set as output
BUFF_CONTROL_1 = 1             ;set as output
DIR_CONTROL_2 = 255            ;set as output
BUFF_CONTROL_2 = 1             ;set as output
DIR_CONTROL_3 = 0              ;set as input
BUFF_CONTROL_3 = 0             ;set as input
DIR_CONTROL_4 = 0              ;set as input
BUFF_CONTROL_4 = 0             ;set as input
INV_CTRL_0_23 = $FFFF          ;set as non-inverting
INV_CTRL_24_31 =$FF            ;set as non-inverting
Alt_use_0_23 = $FFFFFF
Alt_use_24_31 = $FF

;place other initialization variables here
while (1<2)
;PLC in here (perhaps E_STOP routine)
.
.
endwhile
CLOSE
```

Display Port - JDISP (J6) Setup

The JDISP connector (J6) allows connection of the Acc-12 or Acc-12A liquid crystal displays, or of the Acc-12C vacuum fluorescent display. Both text and variable values may be shown on these displays using the **DISPLAY** command, executing in either motion or PLC programs.

Handwheel Port – JHW (J7) Setup

The Handwheel port on the Acc-5E is a convenient and cheap tool to use for an extra two encoder inputs and two PFM outputs. The encoder input lines do not provide a method for inputting an index pulse, but quadrature encoder input is available. The two PFM outputs can used be used in many different applications including driving stepper motors or laser outputs.

Channel-Specific MACRO IC I-Variables

(For MACRO IC Channel n*, where n* = 1 to 2) I-Variables in the I6810s, I6820s, I6910s, and I6920s control the hardware aspects of the MACRO IC DSPGATE2 ASIC that provides the machine interface for supplemental channels 1 and 2. Note that normally few of these functions are used on the Turbo PMAC2s. By default, only the two encoder inputs and the two C-channel PWM/PFM outputs are used. These I-variables are not active if the MACRO IC is not present, or is a MACROGATE IC.

Encoder Input Setup

To set up a supplemental encoder channel through the thumbwheel port, there is very little software setup involved. One parameter that must be changed is the encoder decode. This UMAC I variable is I68n0 or I69n0, where is the supplemental channel. There is firmware support for a system with four Acc5Es addressed to Macro IC #0-3 (based on the settings of S1) and then access to eight supplemental encoder channels with I-variable pointers. Since it is possible to connect up to 16 Acc-5Es into a system, there are methods available to set up additional supplemental encoders through M-Variable pointers. Consult Technical Support to bring in more than eight supplemental encoder channels.

I68n0/I69n0

I68*n*0 and I69n0 control how the encoder input signal for Channel *n* (n** = 1 to 2) on a "DSPGATE2" MACRO IC is decoded into counts. For MACRO ICs 0 and 2, *n* = *n**; for MACRO ICs 1 and 3, *n* = *n** + 5 (i.e. I6810 controls MACRO IC 0 Channel 1; I6970 controls MACRO IC 3 Channel 2). As such, this defines the sign and magnitude of a count. The following settings may be used to decode an input signal.

I68n0/I69n0 = 0: Pulse and direction CW
I68n0/I69n0 = 1: x1 quadrature decode CW
I68n0/I69n0 = 2: x2 quadrature decode CW
I68n0/I69n0 = 3: x4 quadrature decode CW
I68n0/I69n0 = 4: Pulse and direction CCW
I68n0/I69n0 = 5: x1 quadrature decode CCW
I68n0/I69n0 = 6: x2 quadrature decode CCW
I68n0/I69n0 = 7: x4 quadrature decode CCW
I68n0/I69n0 = 8: Internal pulse and direction
I68n0/I69n0 = 9: Not used
I68n0/I69n0 = 10: Not used
I68n0/I69n0 = 11: x6 hall format decode CW*
I68n0/I69n0 = 12: MLDT pulse timer control (Internal pulse resets timer; external pulse latches timer)
I68n0/I69n0 = 13: Not used
I68n0/I69n0 = 14: Not used
I68n0/I69n0 = 15: x6 hall format decode CCW*
*Requires version B or newer of the DSPGATE2 MACRO IC.

After setting up the decode properties, process the data in the encoder conversion table. The encoder counter data for the first encoder will be located at the BaseAddress+11 from your SW1 setting. The second channel of encoder data will be at BaseAddress+19. The following is an example for the encoder conversion table settings for an Acc-5E with two encoders wired into the Handwheel port and switch settings for a base address of $78400.

```
I6810=7                         ;x4 quadrature decode CCW
I6820=7                         ;x4 quadrature decode CCW
I8008=$78410                    ;1/T interpolation where data is at $78411 at
                                ; 9th entry of ECT
I8009=$78418                    ;1/T interpolation where data is at $78419 at
                                ;10th entry of ECT
I903=$3509                      ;Motor 9 position is now set up for position
                                ;feedback through the handwheel port
I904=$3509                      ;Motor 9 position is now set up for velocity
                                ;feedback through the handwheel port
I1003=$350a                     ;Motor 10 position is now set up for position
                                ;feedback through the handwheel port
I1004=$350a                     ;Motor 10 position is now set up for velocity
                                ;feedback through the handwheel port
```

Alternatively, use the data from the following M-Variables:

```
M901->X:$78411,0,24           ;encoder counter for handwheel encoder 1
M991->X:$3509,0,24            ;output from the encoder conversion table with
                              ;1/T interpolation
M1001->X:$78419,0,24          ;encoder counter for handwheel encoder 1
M1091->X:$350a,0,24           ;output from the encoder conversion table with
                              ;1/T interpolation
```

I68n2/I69n2 and I68n3/I69n3 are used to setup the encoder capture characteristics (see Turbo Software Reference Manual). If using the encoder capture function, the captured data will be located at X:$BaseAddress+3,0,24.

PFM Output Setup

There is little setup needed when configuring the two PFM output signals on the Handwheel port of the 5E. Variables I68n6/I69n6 through I68n8/I69n8 are the variables provided through firmware. Look in the Turbo Software Reference Manual for details on all of these variables.

I68n6/I69n6

I68n6/I69n6 = 0: Outputs A and B are PWM; Output C is PWM
I68n6/I69n6 = 1: Outputs A and B are DAC; Output C is PWM
I68n6/I69n6 = 2: Outputs A and B are PWM; Output C is PFM
I68n6/I69n6 = 3: Outputs A and B are DAC; Output C is PFM

Since PFM outputs are needed, select a value of 2 or 3 for this variable. The output register will then be located at address $BaseAddress+4,8,16,s for the first PFM output and $BaseAddress+12,8,16,s for the second PFM channel.

Example for Base Address of $78400:

```
I6816=3                       ;first supplemental channel output mode
I6826=3                       ;second supplemental channel output mode
M902->Y:$78414,0,24,S         ;first supplemental output channel PFM address
M1002->Y:$7841C,0,24,S        ;second supplemental output channel PFM address
```

Now, by setting M902 or M1002 to a value, the PFM output will be located on pins 11-18 on the handwheel port. The maximum value of M902 or M1002 is 16777215 will correspond to a PFM value ½ the PFM clock set by I6803. The pulse width is configured through I6804 for all of the channels at the same base address. See the Turbo Software Reference Manual for all of the details of this setup.

UMAC MACRO AND I/O BOARD CONNECTOR SUMMARY

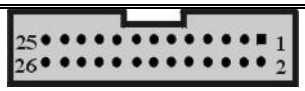
J2:	JTHW	-	Thumbwheel port connector: 26-pin box header connector
J3:	JIO	-	I/O interface connector (32 I/O lines): 40-pin box header connector
J5:	JTAG	-	Programming header (Factory use only)
J6:	JDISP	-	Alphanumeric display connector: 14-pin box header
J7:	JHW	-	Handwheel port, pulse and direction output combined: 20-pin box header
J9:	WD	-	Watchdog relay connector: 4-pin mini-combicon connector
J10:	RJ45IN	-	MACRO wire-based input: 8-pin RJ45 connector (OPTB or OPTC only)
J11:	RJ45OUT	-	MACRO wire-based output: 8-pin RJ45 connector (OPTB or OPTC only)
P1:	JEXP	-	UBUS Interface (96-pin DIN connector)
U17:	OPTO-XCVR	-	MACRO Fiber optic interface: 2- SC style optical connectors (OPTA or OPTB only)

UMAC MACRO AND I/O CONNECTOR PINOUTS

The schematic circuits shown in this section are for interface reference only. Subtle differences may exist between the circuits shown here and the actual hardware used.

J2: JTHW – Thumbwheel Port

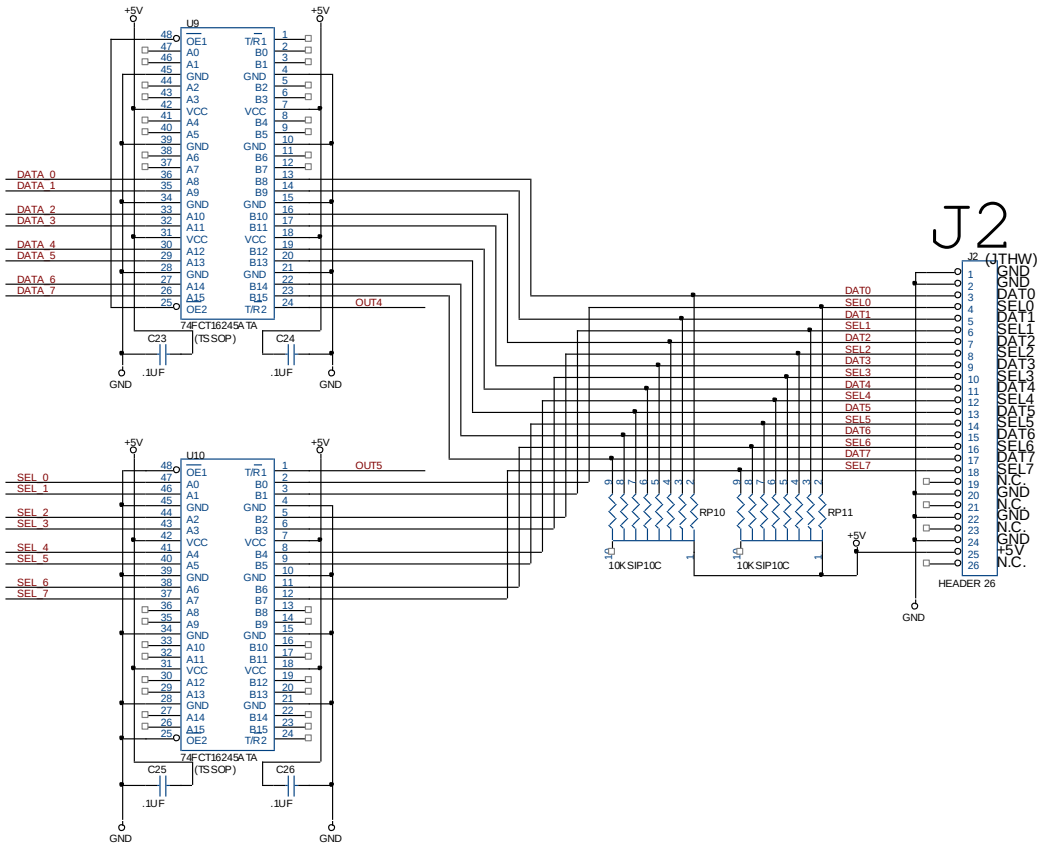
(26-pin Header)



Front View

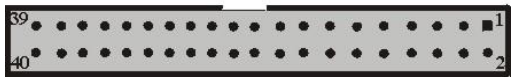
Pin #	Symbol	Function	Description	Notes
1	GND	Common	Power Supply Return	
2	GND	Common	Power Supply Return	
3	DAT0	Bidirect	Thumbwheel Data Line 0	
4	SEL0	Bidirect	Thumbwheel Select Line 0	
5	DAT1	Bidirect	Thumbwheel Data Line 1	
6	SEL1	Bidirect	Thumbwheel Select Line 1	
7	DAT2	Bidirect	Thumbwheel Data Line 2	
8	SEL2	Bidirect	Thumbwheel Select Line 2	
9	DAT3	Bidirect	Thumbwheel Data Line 3	
10	SEL3	Bidirect	Thumbwheel Select Line 3	
11	DAT4	Bidirect	Thumbwheel Data Line 4	
12	SEL4	Bidirect	Thumbwheel Select Line 4	
13	DAT5	Bidirect	Thumbwheel Data Line 5	
14	SEL5	Bidirect	Thumbwheel Select Line 5	
15	DAT6	Bidirect	Thumbwheel Data Line 6	
16	SEL6	Bidirect	Thumbwheel Select Line 6	
17	DAT7	Bidirect	Thumbwheel Data Line 7	
18	SEL7	Bidirect	Thumbwheel Select Line 7	
19	n.c.		Not Connected	
20	GND	Common	Power Supply Return	
21	n.c.		Not Connected	
22	GND	Common	Power Supply Return	
23	n.c.		Not Connected	
24	GND	Common	Power Supply Return	
25	+5V	Vcc	Power Supply	Pwr supply output from UBUS backplane
26	n.c.		Not Connected	

The JTHW connector provides the UMAC system with the ability to communicate either by using the thumbwheel port protocol or by a user-created parallel means.



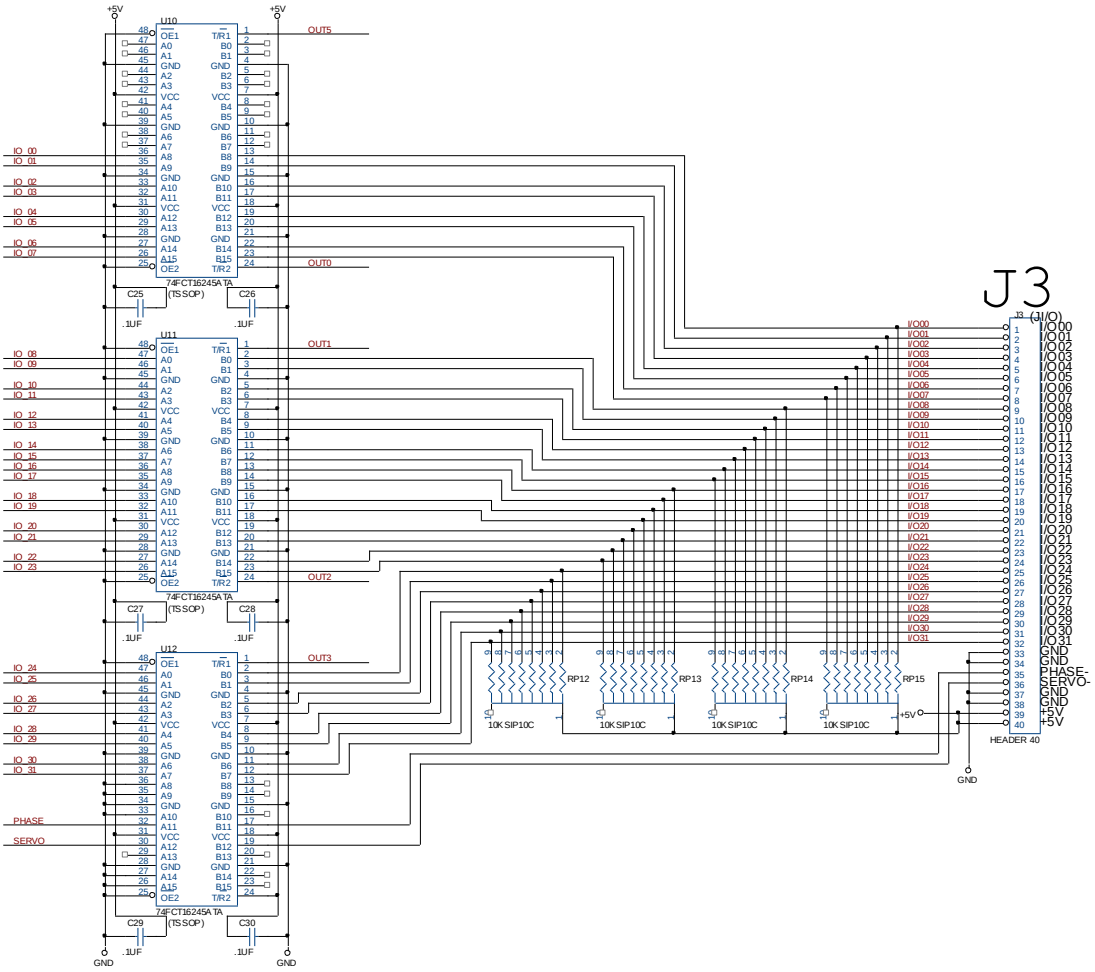
Circuitry for J2 JTHW Interface

J4: JI/O - General Purpose I/O Port
(40-pin Header)



Front View

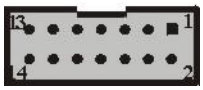
Pin #	Symbol	Function	Description	Notes
1	I/O00	Bidirect	Input or Output #00	
2	I/O01	Bidirect	Input or Output #01	
3	I/O02	Bidirect	Input or Output #02	
4	I/O03	Bidirect	Input or Output #03	
5	I/O04	Bidirect	Input or Output #04	
6	I/O05	Bidirect	Input or Output #05	
7	I/O06	Bidirect	Input or Output #06	
8	I/O07	Bidirect	Input or Output #07	
9	I/O08	Bidirect	Input or Output #08	
10	I/O09	Bidirect	Input or Output #09	
11	I/O10	Bidirect	Input or Output #10	
12	I/O11	Bidirect	Input or Output #11	
13	I/O12	Bidirect	Input or Output #12	
14	I/O13	Bidirect	Input or Output #13	
15	I/O14	Bidirect	Input or Output #14	
16	I/O15	Bidirect	Input or Output #15	
17	I/O16	Bidirect	Input or Output #16	
18	I/O17	Bidirect	Input or Output #17	
19	I/O18	Bidirect	Input or Output #18	
20	I/O19	Bidirect	Input or Output #19	
21	I/O20	Bidirect	Input or Output #20	
22	I/O21	Bidirect	Input or Output #21	
23	I/O22	Bidirect	Input or Output #22	
24	I/O23	Bidirect	Input or Output #23	
25	I/O24	Bidirect	Input or Output #24	
26	I/O25	Bidirect	Input or Output #25	
27	I/O26	Bidirect	Input or Output #26	
28	I/O27	Bidirect	Input or Output #27	
29	I/O28	Bidirect	Input or Output #28	
30	I/O29	Bidirect	Input or Output #29	
31	I/O30	Bidirect	Input or Output #30	
32	I/O31	Bidirect	Input or Output #31	
33	GND	Common	Power Supply Return	
34	GND	Common	Power Supply Return	
35	PHASE	Output	Phase Clock Output	
36	SERVO	Output	Servo Clock Output	
37	GND	Common	Power Supply Return	
38	GND	Common	Power Supply Return	
39	+5V	Vcc	Power Supply	Pwr supply output from UBUS backplane
40	+5V	Vcc	Power Supply	Pwr supply output from UBUS backplane



Circuitry For J3 JI/O Interface

J6: JDISP - Display Port Connector

(14-pin Header)



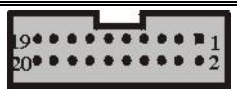
Front View

Pin #	Symbol	Function	Description	Notes
1	+5V	Vcc	Power Supply	Pwr supply output from UBUS backplane
2	GND	Common	Power Supply Return	
3	RS	Output	Read Select	Connected to OUT8-
4	Vee	Output	LCD Display Intensity	Pot adjusts between 5V and GND
5	E	Output	LCD Display Enable	Connected to OUT7-
6	R/W-	Output	Read/write- Signal	Connected to OUT6-
7	DB1	Bidirect	Data Bit 1	
8	DB0	Bidirect	Data Bit 0	
9	DB3	Bidirect	Data Bit 3	
10	DB2	Bidirect	Data Bit 2	
11	DB5	Bidirect	Data Bit 5	
12	DB4	Bidirect	Data Bit 4	
13	DB7	Bidirect	Data Bit 7	
14	DB6	Bidirect	Data Bit 6	

Note 1: Upon a clear-reset power-up, this port will automatically output data to the LCD device.
Note 2: This port is designed to operate with the Acc-12 display products from Delta Tau Data Systems Inc.
Note 3: This port is capable of being used as an 8-bit parallel input or output.
Note 4: The value of Y:$10D0 (for Turbo UMAC) is set to $80 for Acc-12A (LCD Display). Set this register to $16 for Acc-12C (Vacuum Fluorescent Display) or basic parallel output from the display buffer register. Set this register to 00 if the JDISP connector is to be used as an 8-bit parallel port.

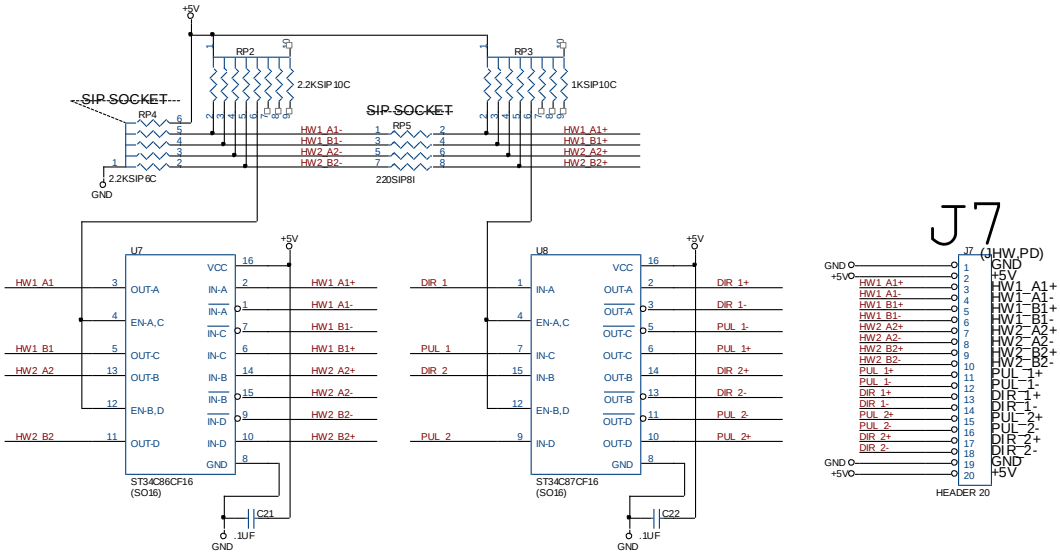
J7: JHW - Handwheel Port, Pulse and Direction Output Connector

(20-pin Header)



Front View

Pin #	Symbol	Function	Description	Notes
1	GND	Common	Power Supply Return	
2	+5V	Vcc	Power Supply	Pwr supply output from UBUS backplane
3	HW1_A+	Input	Handwheel #1 'A+' Input	
4	HW1_A-	Input	Handwheel #1 'A-' Input	
5	HW1_B+	Input	Handwheel #1 'B+' Input	
6	HW1_B-	Input	Handwheel #1 'B-' Input	
7	HW2_A+	Input	Handwheel #2 'A+' Input	
8	HW2_A-	Input	Handwheel #2 'A-' Input	
9	HW2_B+	Input	Handwheel #2 'B+' Input	
10	HW2_B-	Input	Handwheel #2 'B-' Input	
11	PUL1+	Output	Pulse Output #1+	
12	PUL1-	Output	Pulse Output #1-	
13	DIR1+	Output	Direction Output #1+	
14	DIR1-	Output	Direction Output #1-	
15	PUL2+	Output	Pulse Output #2+	
16	PUL2-	Output	Pulse Output #2-	
17	DIR2+	Output	Direction Output #2+	
18	DIR2-	Output	Direction Output #2-	
19	GND	Common	Power Supply Return	
20	+5V	Vcc	Power Supply	Pwr supply output from UBUS backplane



Circuitry For J7 JHW Interface

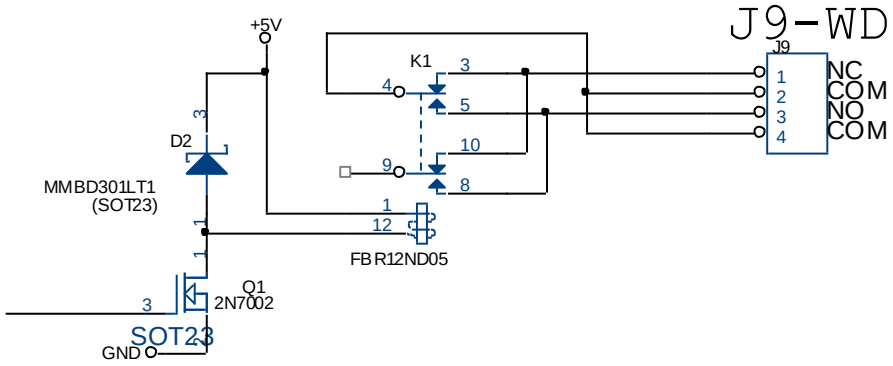
TB1: Watchdog Relay Connector

(4 pin Mini-Combicon)



Front View

Pin #	Symbol	Function	Description	Notes
1	NC	Relay Contact	Normally closed contact	This Pin is connected to J9-2 and J9-4 when the watchdog is tripped.
2	COM	Relay Contact	Watchdog Common	Connected to pin 4.
3	NO	Relay Contact	Normally open contact	This pin is connected to J9-2 and J9-4 when the system is functioning normally. This pin is disconnected when the Watchdog circuit trips (error condition).
4	COM	Relay Contact	Watchdog Common	Connected to pin 2.



Watchdog Relay Circuit

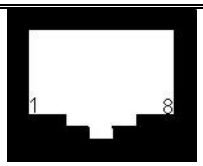
Note

Accessory Boards from Revision -104 and higher have logic which causes the watchdog relay to appear tripped when either a watchdog condition occurs or power is removed from the UMAC rack.

This causes the relay to operate in the opposite condition from the earlier revisions of this board.

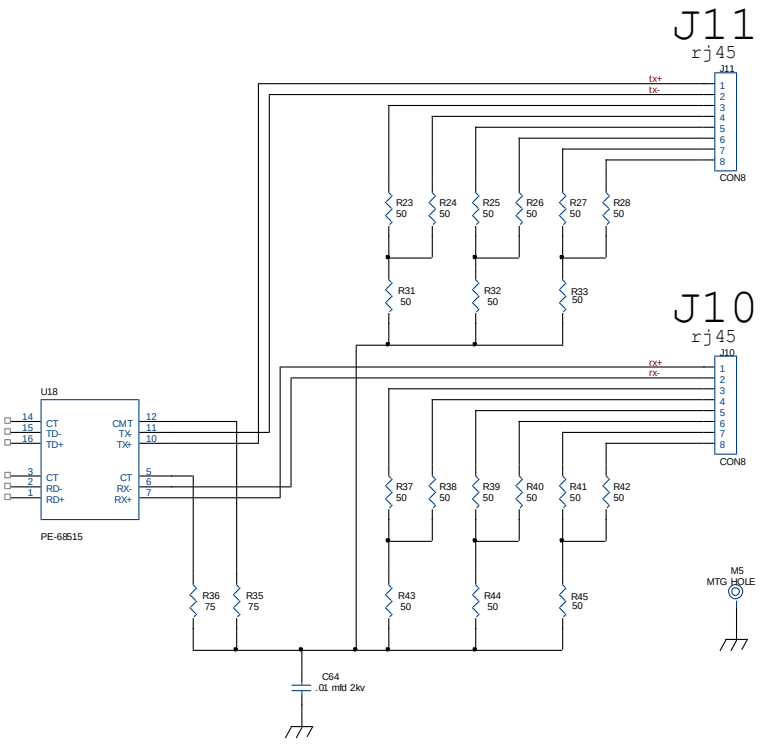
J10,J11: MACRO I/O (Opt. B, C)

(8 pin RJ45)



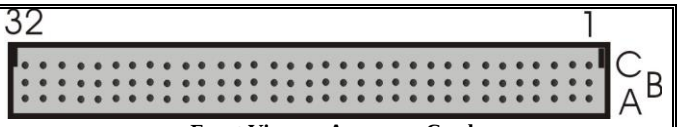
Front View

Pin #	Symbol	Function	Description	Notes
1	DATA+	Data +	Differential MACRO Signal.	J10: DATA+ input. J11: DATA+ output.
2	DATA-	Data -	Differential MACRO Signal	J10: DATA- input. J11: DATA- output.
3	Unused		Unused terminated pin	See schematic below.
4	Unused		Unused terminated pin	See schematic below.
5	Unused		Unused terminated pin	See schematic below.
6	Unused		Unused terminated pin	See schematic below.
7	Unused		Unused terminated pin	See schematic below.
8	Unused		Unused terminated pin	See schematic below.
The cable used for MACRO wired connections is CAT5 verified straight-through 8 conductor.				



P1: UBUS Interface Connector

(96 pin EURO-Connector)



Front View on Accessory Card

Pin #	Row A	Row B	Row C
1	+5Vdc	+5Vdc	+5Vdc
2	GND	GND	GND
3	BD01	DAT0	BD00
4	BD03	SEL0	BD02
5	BD05	DAT1	BD04
6	BD07	SEL1	BD06
7	BD09	DAT2	BD08
8	BD11	SEL2	BD10
9	BD13	DAT3	BD12
10	BD15	SEL3	BD14
11	BD17	DAT4	BD16
12	BD19	SEL4	BD18
13	BD21	DAT5	BD20
14	BD23	SEL5	BD22
15	BS1	DAT6	BS0
16	BA01	SEL6	BA00
17	BA03	DAT7	BA02
18	BX/Y	SEL7	BA04
19	N.C.	BA06	N.C.
20	BA05	BA07	CS4-
21	N.C.	BA08	N.C.
22	CS16-	BA09	N.C.
23	BA13	BA10	BA12
24	BRD-	BA11	BWR-
25	BS3	MEMCS0-	BS2
26		MEMCS1-	RESET
27	PHASE+	IREQ1-	SERVO+
28	PHASE-	IREQ2-	SERVO-
29	N.C.	IREQ3-	N.C.
30	-15Vdc	N.C.	+15Vdc
31	GND	GND	GND
32	+5Vdc	+5Vdc	+5Vdc

1. Refer to the UBUS Specification for detailed signal descriptions.
2. Items shown in gray boxes represent optional UBUS backplane operation. Jumpers must be installed to use these signals.

U17: MACRO Fiber Optic Connector (OPT A, B)

(2 Socket SC-Style)



Front View

Pin #	Symbol	Function	Description	Notes
1	RX	Fiber Input	MACRO Ring Receiver	
2	TX	Fiber Output	MACRO Ring Transmitter	

1. The fiber optic version of MACRO uses 62.5/125 multi-mode glass fiber optic cable terminated in an SC-style connector. The optical wavelength is 1,300nm.
2. It is possible to "adapt" wire to fiber operation when using OPT B.

UMAC MACRO AND I/O MEMORY MAPS

The diagrams below shows the mapping of the registers used in the Acc-5E.

There are two maps shown here: They represent the layout for the CS16- identification registers and the CS4- Gate Array Select registers.

Identification and Configuration Register Map

Identification Register (CS16-) TABLE

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BANK 0													OUT4	OUT3	OUT2	OUT1	OUT0	W/F	VLTN	SCLK	VENDOR CODE				BASE
													OUT8	OUT7	OUT6	OUT5	BIST	DLB	LTCOMP	BANK					+1
																			LINK FAULT-	OPTION CODE					+2
																									+3
BANK 1													OUT4	OUT3	OUT2	OUT1	OUT0	W/F	VLTN	SCLK	REVISION				BASE
													OUT8	OUT7	OUT6	OUT5	BIST	DLB	LTCOMP	BANK	CARD TYPE				+1
																			LINK FAULT-						+2
																									+3

SCLK: (Read/Write)
0 = Servo and phase clock input mode (Source is supplied from UBUS)
1 = Servo and phase clock source (power-up default)

VLTN: (Violation Status) (Read Only)
0 = No violation
1 = Violation

W/F: (Wire/Fiber) (Read/Write)
0 = Fiber (Power-up default)
1 = Wire

BANK: (Bank Select) (Read/Write)
0 = Bank 0
1 = Bank 1

DLB: (Data Loop Back) (Read/Write)
0 = Disabled (power-up default)
1 = Enabled

BIST: (Built In Self Test) (Read/Write)
0 = Disabled (power-up default)
1 = Enabled

OUT0 - OUT8: (Read/Write)
These are registered bits that operate hardware located on the circuit board (i.e. JDISP). The user must take care not to change these bits when changing other configuration bits.

LINK FAULT-: (Link Fault Interrupt) (Read Only)
0 = ERROR- Input signal that is selected by W/F has no activity.
1 = NORMAL- Input signal is present.

Vendor Codes: (Read Only Least sig. four bits in two adjacent registers)
Vendor codes are assigned by board manufacturer per the UBUS Specification.
This board has a vendor code of 0000 0001 (the code for Delta Tau Data Systems Inc.).

Option Codes: (Read Only Least sig. five bits in two adjacent registers)
Located in CS16- register base address + 2, these bits are set as follows:
00000 0wxyz
w : O3 strap
x : O2 strap
y : O1 strap - MACRO is installed
z : O0 - 1 = Dual gate array 0 = Single gate array

Revision Codes: (Read Only Least sig. four bits in base address of bank 1)
This register is located in the CS16- register base address, bank one, these bits are set as follows:
00000 0wxyz

Card Type Code: (Read Only 14 bits in three adjacent registers of bank 1)

Located starting in CS16-register base address + 1, these bits are set by the board manufacturer to indicate which board this is.

Delta Tau Data Systems Inc. assigns the board number into this space as converted to hexadecimal. Since the number of this board is 60**3437** the value of these registers is set to $3437_{10}=0D6D_{16}$.

MACRO IC Base Address and Register Map

Refer to the Turbo PMAC Software Reference for a detailed description of each register used in the gate arrays on the Acc-5E accessory card.

The table described in S1: Dipswitch UBUS MACRO IC Base Address section above shows the base addresses available for the Acc-5E.

UMAC Turbo systems may have up to 16 MACRO ICs, although only four at any given time can support automatic firmware functions by designation as MACRO ICs 0 – 3 (configured by I20 – I23). The 16 possible base addresses are $07xy00, where 'x' can be 8, 9, A, or B, and 'y' can be 4, 5, 6, or 7.

This section assumes that MACRO ICs 0 – 3 have the default base addresses of $078400, $078500, $078600, and $078700.

Here are some practices that should be followed to simplify the operation of the device ports (i.e. JDISP, JTHW) on the Acc-5E accessory card:

1. Always start the first Acc-5E card at the base address of $78400. This is the first address available for a MACRO IC (CS4-) based device and has reference examples that directly refer to this address in the software reference manual.
2. If multiple Acc-5E accessory cards are used in the UMAC system, plan to use the device ports on the first (lowest addressed) Acc-5E.

DECLARATION OF CONFORMITY

Application of Council Directive: 89/336/EEC, 72/23/EEC

Manufacturers Name: Delta Tau Data Systems, Inc.

Manufacturers Address: 21314 Lassen Street
Chatsworth, CA 91311
USA

We, Delta Tau Data Systems, Inc. hereby declare that the product
Product Name: Accessory 5E
Model Number: 603437
And all of its options conforms to the following standards:

EN61326: 1997	Electrical equipment for measurement, control, and laboratory use- EMC requirements
EN55011: 1998	Limits and methods of measurements of radio disturbance characteristics of information technology equipment
EN61010-1	Electrical equipment for measurement, control, and laboratory use- Safety requirements
EN61000-3-2 :1995 A14:1998	Limits for harmonic current emissions. Criteria A
EN61000-3-3: 1995	Limitation of voltage fluctuations and flicker in low-voltage supply systems for equipment with rated current ≤ 16A. Criteria B.
EN61000-4-2:1995 A1: 1998	Electro Static Discharge immunity test. Criteria B
EN61000-4-3: 1995 A1: 1998	Radiated, radio-frequency, electromagnetic field immunity test. Criteria A
EN61000-4-4: 1995	Electrical fast transients/burst immunity test. Criteria B
EN61000-4-5: 1995	Surge Test. Criteria B
EN61000-4-6: 1996	Conducted immunity test. Criteria A
EN61000-4-11: 1994	Voltage dips test. Criteria B and C

Date Issued: 11 May 2006
Place Issued: Chatsworth, California USA

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