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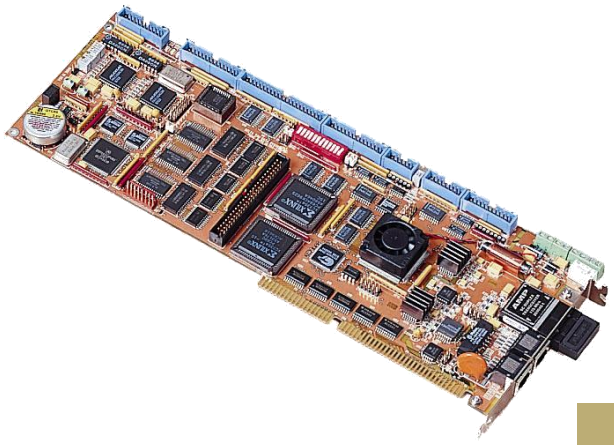
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HARDWARE REFERENCE MANUAL

PMAC2 PC Ultralite



Programmable Multi-Axis Controller

3Ax-602415-xHxx

June 7, 2004

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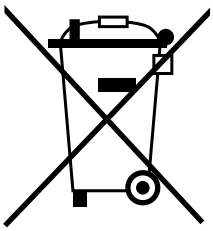
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INTRODUCTION

The PMAC2 PC Ultralite control board is a member of the PMAC2 family of controllers that replaces the local axis interface circuitry with the MACRO ring network interface. The Ultralite name is used because of the lack of any direct on-board axis interface circuitry. In other words, the interface hardware for channels 1 through 8 is missing on the Ultralite.

Features

Input/Output

The Ultralite board does retain the local general purpose I/O of the PMAC family, including:

- JDISP Display Port
- JTHW Multiplexer Port
- JIO General I/O Port
- JHW Handwheel Port
- JRS232 Serial Port
- JRS422 Serial Port

The Ultralite board's MACRO interface is available in 1 of 3 forms; 1 of the 3 must be ordered:

- SC optical fiber interface
- BNC coaxial cable interface
- RJ-45 phone jack interface

The following ports are not available on the PMAC2 PC Ultralite:

- JANA Analog Input Port
- JEQU Position Compare Output Port
- JMACHn Axis Interface Ports

Firmware

The firmware for the Ultralite functions identically to that of other members of the PMAC2 family, which is very similar to the firmware for the original PMAC family. Because of the hardware differences, there are some differences in the use of the firmware.

Variables I910 to I989, which control the setup of machine interface channels 1-8, are useless, because these machine interface channels are not present on the Ultralite. In an Ultralite system, equivalent functions are implemented on the remote drives.

Variables I900 to I909, which control the overall hardware setup on non-Ultralite boards, are useless on the Ultralite boards because they require some of the missing hardware. On a PMAC2 Ultralite, these functions are implemented by variables in the I990s. The comparison is given in the table 1-1.

The values of the motor I-variables that specify the addresses of the outputs and inputs for that motor, and the setup of the encoder conversion table that pre-processes the position feedback will be different on the PMAC2 Ultralite.

Function	Non-Ultralite Variable	Ultralite Variable
MaxPhase/PWM Freq	I900, I906	I992
Phase Clock Freq	I901	I997
Servo Clock Freq	I902	I998
Hardware Clock Freq	I903	I993
Deadtime/Pulse Width	I904	I994

DSPGATE2 I/O ASIC

Delta Tau has designed its own custom application-specific integrated circuits (ASICs) for the PMAC2 PC Ultralite using the latest sub-micron gate-array technology. Each ASIC contains 45,000 active logic gates. These ASICs contain all of the digital interface circuitry to tie the DSP to the machine; the rest of the circuitry on the board is buffer circuitry. The DSPGATE2 ASIC has three parts:

- General-purpose digital I/O: 56 I/O points for JIO, JTHW, and JDISP ports
- Servo interface circuitry for 2 supplemental channels with clock generation
- MACRO ring interface circuitry

The general-purpose I/O and the servo interface circuitry on the DSPGATE2 generally share pins, except for two 2-channel encoder inputs and two PWM/PFM output sub-channels. On a PMAC2 PC Ultralite board, the shared pins are usually used for general-purpose I/O instead of extra servo interface circuitry, but this is up to the individual user.

Basic Specifications

Physical Specifications

Size: 33.5cm x 9.9cm x 3.8cm (13.2" x 3.9" x 1.4")

Weight: ¾ lb.

Temperature

Operating: 0°C to 60°C (32°)F to 140°F)

Storage: 12°C to 82°C (10°F to 180°F)

Humidity: 10% to 95%, non-condensing

Electrical Specifications

Power: 1.8A @ +5V (±5%)
0.1A @ -12 to –15V
Pertains to 8-channel configuration, with a typical load of encoders

Battery 3.0V Lithium Cell, 1200 mAh, 2/3 A-size, no tabs, or 3.6V Lithium Cell, 1000 mAh, 1.00" can
Expected battery life: 10 years (standard), 6-9 months (Opt. 5).
Recommended replacement: 24 months (standard), 3-6 months (Opt. 5)

CONNECTORS AND JUMPERS

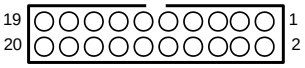
Connector Summary

The following paragraphs provide a brief description of each connector on the PMAC2 PC Ultralite, its use, and individual pinout information. See the layout diagram for connector locations.

The JANA connector provides the inputs for the 8 or 16 optional analog inputs on the PMAC2.

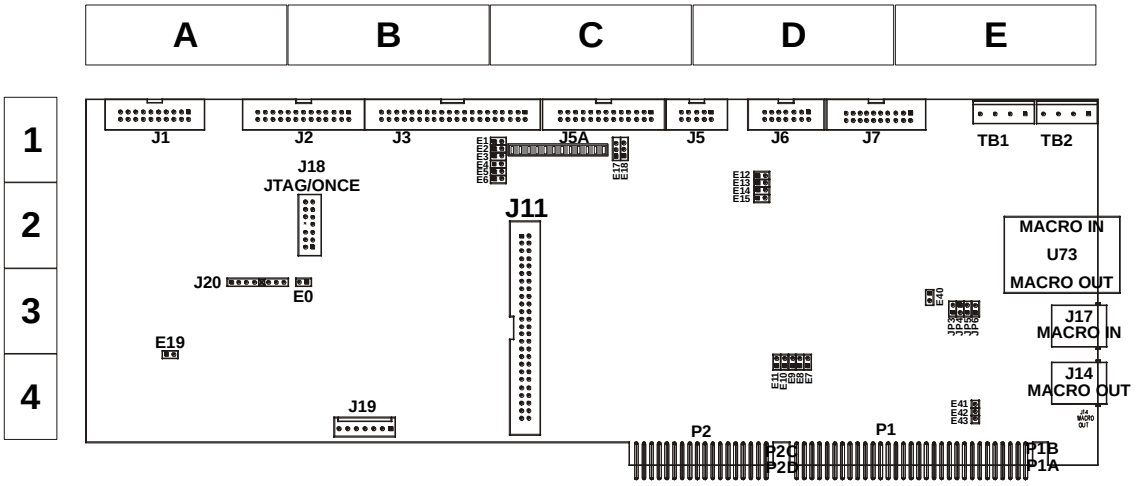
J1/JANA (20-Pin Header)

(Present only if Option 12 ordered)



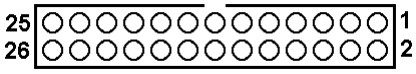
Front View

Pin #	Symbol	Function	Description	Notes
1	ANAI00	Input	Analog Input 0	0-5V or +/-2.5V range
2	ANAI01	Input	Analog Input 1	0-5V or +/-2.5V range
3	ANAI02	Input	Analog Input 2	0-5V or +/-2.5V range
4	ANAI03	Input	Analog Input 3	0-5V or +/-2.5V range
5	ANAI04	Input	Analog Input 4	0-5V or +/-2.5V range
6	ANAI05	Input	Analog Input 5	0-5V or +/-2.5V range
7	ANAI06	Input	Analog Input 6	0-5V or +/-2.5V range
8	ANAI07	Input	Analog Input 7	0-5V or +/-2.5V range
9	ANAI08	Input	Analog Input 8	0-5V or +/-2.5V range
10	ANAI09	Input	Analog Input 9	0-5V or +/-2.5V range
11	ANAI10	Input	Analog Input 10	0-5V or +/-2.5V range
12	ANAI11	Input	Analog Input 11	0-5V or +/-2.5V range
13	ANAI12	Input	Analog Input 12	0-5V or +/-2.5V range
14	ANAI13	Input	Analog Input 13	0-5V or +/-2.5V range
15	ANAI14	Input	Analog Input 14	0-5V or +/-2.5V range
16	ANAI15	Input	Analog Input 15	0-5V or +/-2.5V range
17	GND	Common	PMAC Common	Not isolated from digital
18	+12V	Output	Pos. Supply Volt.	To power external circuitry
19	GND	Common	PMAC Common	Not isolated from digital
20	-12V	Output	Neg. Supply Volt	To power external circuitry



Ref Des	Connector Name	Loc	Ref Des	Connector Name	Loc
J1	JANA Analog Input Connector (Option 12 only): 20-pin IDC header	A1	**J17**	MACRO Electrical Output Connector: 8-pin RJ-45 socket	E3
J2	JTHW Multiplexer Port Connector: 26-pin IDC header	A1	**J18**	JTAG/OnCE (for factory use only): 10-pin IDC header	B2
J3	JIO General Purpose Input/Output Connector: 40-pin IDC header	B1	**J19**	JSIO (for factory use only): 8-pin SIP connector	B4
J5	JRS232 Serial Port Connector: 10-pin IDC header	C1	**J20**	JISP (for factory use only): 8-pin SIP connector	A3
J5A	JRS422 Serial Port Connector: 26-pin IDC header	C1	**P1**	ISA Bus Connector: 64-pin card-edge connector	D4
J6	JDISP Display Port Connector: 14-pin IDC header	D1	**P2**	ISA Bus Connector: 36-pin card-edge connector	C4
J7	JHW Handwheel Encoder Connector: 20-pin IDC header	D1	**TB1**	JPWR Power Supply Connector: 4-point terminal block	E1
J11	JEXP Expansion Port Connector: 50-pin IDC header	C2	**TB2**	WD Watchdog Output Connector: 4-point terminal block	E1
J14	MACRO Electrical Input Connector: 8-pin RJ-45 socket	E4	**U73**	MACRO Fiber Optic Transceiver: Double SC fiber-optic socket	E2

J2/JTHW (26-Pin Header)

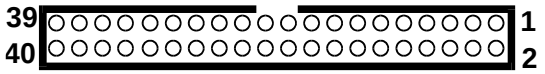


Front View

Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Input	Data-0 Input	Data input from mux port accessories
4	SEL0	Output	Select-0 Output	Address/data output for mux port accessories
5	DAT1	Input	Data-1 Input	Data input from mux port accessories
6	SEL1	Output	Select-1 Output	Address/data output for mux port accessories
7	DAT2	Input	Data-2 Input	Data input from mux port accessories
8	SEL2	Output	Select-2 Output	Address/data output for mux port accessories
9	DAT3	Input	Data-3 Input	Data input from mux port accessories
10	SEL3	Output	Select-3 Output	Address/data output for mux port accessories
11	DAT4	Input	Data-4 Input	Data input from mux port accessories
12	SEL4	Output	Select-4 Output	Address/data output for mux port accessories
13	DAT5	Input	Data-5 Input	Data input from mux port accessories
14	SEL5	Output	Select-5 Output	Address/data output for mux port accessories
15	DAT6	Input	Data-6 Input	Data input from mux port accessories
16	SEL6	Output	Select-6 Output	Address/data output for mux port accessories
17	DAT7	Input	Data-7 Input	Data input from mux port accessories
18	SEL7	Output	Select-7 Output	Address/data output for mux port accessories
19	N.C.	N.C.	No Connection	
20	GND	Common	PMAC Common	
21	BRLD/	Output	Buffer Request	Low is buffer request
22	GND	Common	PMAC Common	
23	IPLD/	Output	In Position	Low is in position
24	GND	Common	PMAC Common	
25	+5V	Output	+5Vdc Supply	Power supply out
26	INIT/	Input	PMAC Reset	Low is reset

The JTHW connector provides eight inputs and eight outputs at TTL levels; typically, these are used to create multiplexed I/O with accessory boards such as Acc-18 (Thumbwheel) and Acc-34 (Discrete I/O). The port I/O may also be used directly, as non-multiplexed I/O.

J3/JIO (40-Pin Header)

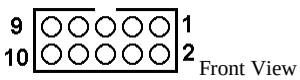


Front View

Pin #	Symbol	Function	Description	Notes
1	I/O00	In/Out	Digital I/O 0	Software direction ctrl.
2	I/O01	In/Out	Digital I/O 1	Software direction ctrl.
3	I/O02	In/Out	Digital I/O 2	Software direction ctrl.
4	I/O03	In/Out	Digital I/O 3	Software direction ctrl.
5	I/O04	In/Out	Digital I/O 4	Software direction ctrl.
6	I/O05	In/Out	Digital I/O 5	Software direction ctrl.
7	I/O06	In/Out	Digital I/O 6	Software direction ctrl.
8	I/O07	In/Out	Digital I/O 7	Software direction ctrl.
9	I/O08	In/Out	Digital I/O 8	Software direction ctrl.
10	I/O09	In/Out	Digital I/O 9	Software direction ctrl.
11	I/O10	In/Out	Digital I/O 10	Software direction ctrl.
12	I/O11	In/Out	Digital I/O 11	Software direction ctrl.
13	I/O12	In/Out	Digital I/O 12	Software direction ctrl.
14	I/O13	In/Out	Digital I/O 13	Software direction ctrl.
15	I/O14	In/Out	Digital I/O 14	Software direction ctrl.
16	I/O15	In/Out	Digital I/O 15	Software direction ctrl.
17	I/O16	In/Out	Digital I/O 16	Software direction ctrl.
18	I/O17	In/Out	Digital I/O 17	Software direction ctrl.
19	I/O18	In/Out	Digital I/O 18	Software direction ctrl.
20	I/O19	In/Out	Digital I/O 19	Software direction ctrl.
21	I/O20	In/Out	Digital I/O 20	Software direction ctrl.
22	I/O21	In/Out	Digital I/O 21	Software direction ctrl.
23	I/O22	In/Out	Digital I/O 22	Software direction ctrl.
24	I/O23	In/Out	Digital I/O 23	Software direction ctrl.
25	I/O24	In/Out	Digital I/O 24	Software direction ctrl.
26	I/O25	In/Out	Digital I/O 25	Software direction ctrl.
27	I/O26	In/Out	Digital I/O 26	Software direction ctrl.
28	I/O27	In/Out	Digital I/O 27	Software direction ctrl.
29	I/O28	In/Out	Digital I/O 28	Software direction ctrl.
30	I/O29	In/Out	Digital I/O 29	Software direction ctrl.
31	I/O30	In/Out	Digital I/O 30	Software direction ctrl.
32	I/O31	In/Out	Digital I/O 31	Software direction ctrl.
33	GND	Common	Reference Voltage	
34	GND	Common	Reference Voltage	
35	PHASE/	Output	Phase Clock	For latching data
36	SERVO/	Output	Servo Clock	For latching data
37	GND	Common	Reference Voltage	
38	GND	Common	Reference Voltage	
39	+5V	Output	Supply Voltage	To power ext. circuitry
40	+5V	Output	Supply Voltage	To power ext. circuitry

The JI/O connector provides 32 input/output pins at TTL levels. Direction can be controlled in byte-wide groups.

J5/JRS232 (10-Pin Header)



Front View

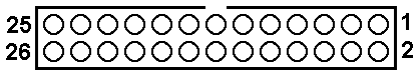
Pin #	Symbol	Function	Description	Notes
1	PHASE	In/Out	Phasing Clock	See Notes 1, 2
2	DTR	Bidirect	Data Term Rdy	Tied to DSR
3	TXD/	Input	Receive Data	Host transmit data
4	CTS	Input	Clear To Send	Host ready bit
5	RXD/	Output	Send Data	Host receive data
6	RTS	Output	Req. To Send	PMAC ready bit
7	DSR	Bidirect	Data Set Ready	Tied to DTR
8	SERVO	In/Out	Servo Clock	See Note 2
9	GND	Common	PMAC Common	
10	+5V	Output	+5Vdc Supply	Power supply out

The JRS232 connector provides the PMAC2 PC with the ability to communicate serially with an RS232 port. This connector cannot be used for daisy chain communication interconnection of multiple PMACs, although it can be used to share servo and phase clocks for synchronicity. The J5A RS-422 interface is required for daisy chain communication. Jumpers E17 and E18 must connect pins 1 and 2 to use this port for serial communications.

Note 1: If communicating to PMAC2 over this connector with a modem style terminal emulator such as Microsoft Windows Terminal, line 1 should not be connected.

Note 2: Servo and Phase are outputs if jumper E1 is OFF; they are inputs if jumper E1 is on.

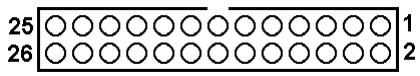
J5A/JRS422 (26-Pin Header)



Front View

Pin #	Symbol	Function	Description	Notes
1	CHASSI	Common	PMAC Common	
2	S+5V	Output	+5Vdc Supply	Deactivated by E8
3	RD-	Input	Receive Data	Diff I/O low true **
4	RD+	Input	Receive Data	Diff I/O high true *
5	SD-	Output	Send Data	Diff I/O low true **
6	SD+	Output	Send Data	Diff I/O high true *
7	CS+	Input	Clear to Send	Diff I/O high true **
8	CS-	Input	Clear to Send	Diff I/O low true *
9	RS+	Output	Req. to Send	Diff I/O high true **
10	RS-	Output	Req. to Send	Diff I/O low true *
11	DTR	Bidirect	Data Term Read	Tied to DSR
12	INIT/	Input	PMAC Reset	Low is reset
13	GND	Common	PMAC Common	**
14	DSR	Bidirect	Data Set Ready	Tied to DTR
15	SDIO-	Bidirect	Special Data	Diff I/O low true
16	SDIO+	Bidirect	Special Data	Diff I/O high true
17	SCIO-	Bidirect	Special Ctrl.	Diff I/O low true
18	SCIO+	Bidirect	Special Ctrl.	Diff I/O high true
19	SCK-	Bidirect	Special Clock	Diff I/O low true
20	SCK+	Bidirect	Special Clock	Diff I/O high true
21	SERVO-	Bidirect	Servo Clock	Diff I/O low true ***
22	SERVO+	Bidirect	Servo Clock	Diff I/O high true ***

J5A/JRS422 (26-Pin Header) Continued



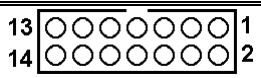
Front View

Pin #	Symbol	Function	Description	Notes
23	PHASE-	Bidirect	Phase Clock	Diff I/O low true ***
24	PHASE+	Bidirect	Phase Clock	Diff I/O high true***
25	GND	Common	PMAC Common	
26	+5V	Output	+5Vdc Supply	Power supply out

The JRS422 connector provides the PMAC with the ability to communicate in both RS422 and RS232. In addition, this connector is used to daisy chain interconnect multiple PMACs for synchronized operation.

Jumpers E17 and E18 must connect pins 2 and 3 to use this port for serial communications.

J6/JDISP (14-Pin Header)

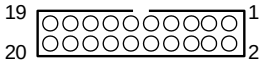


Front View

Pin #	Symbol	Function	Description	Notes
1	VDD	Output	+5V Power	Power supply out
2	VSS	Common	PMAC Common	
3	RS	Output	Read Strobe	TTL signal out
4	VEE	Output	Contrast Adjust Vee	0 to +5Vdc *
5	E	Output	Display Enable	High is enable
6	R/W	Output	Read Or Write	TTL signal out
7	DB1	Output	Display Data1	
8	DB0	Output	Display Data0	
9	DB3	Output	Display Data3	
10	DB2	Output	Display Data2	
11	DB5	Output	Display Data5	
12	DB4	Output	Display Data4	
13	DB7	Output	Display Data7	
14	DB6	Output	Display Data6	

The JDISP connector is used to drive the 2-line x 24-character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (Acc 12C) display unit. The **DISPLAY** command may be used to send messages and values to the display.

J7/JHW (20-Pin Header)

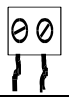


Front View

Pin #	Symbol	Function	Description	Notes
1	GND	Common	Ref. Voltage	
2	+5V	Output	Supply Voltage	To power external circuitry
3	HWA1+	Input	HW Pos A Chan.	Also pulse input
4	HWA1-	Input	HW Neg A Chan.	Also pulse input
5	HWB1+	Input	HW Pos B Chan.	Also direction input
6	HWB1-	Input	HW Neg B Chan.	Also direction input
7	HWA2+	Input	HW Pos A Chan.	Also pulse input
8	HWA2-	Input	HW Neg A Chan.	Also pulse input
9	HWB2+	Input	HW Pos B Chan.	Also direction input
10	HWB2-	Input	HW Neg B Chan.	Also direction input
11	PUL1+	Output	PFM Pos Pulse	Also PWM output
12	PUL1-	Output	PFM Neg Pulse	Also PWM output
13	DIR1+	Output	PFM Pos Dir. Out	Also PWM output
14	DIR1-	Output	PFM Neg Dir Out	Also PWM output
15	PUL2+	Output	PFM Pos Pulse	Also PWM output
16	PUL2-	Output	PFM Neg Pulse	Also PWM output
17	DIR2+	Output	PFM Pos Dir. Out	Also PWM output
18	DIR2-	Output	PFM Neg Dir Out	Also PWM output
19	GND	Common	Ref. Voltage	
20	+5V	Output	Supply Voltage	To power external circuitry

This connector provides the interface for two quadrature encoders, typically to be used as handwheel or time base master encoders.

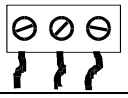
TB1 (2-Pin Terminal Block)



Pin#	Symbol	Function	Description	Notes
1	GND	Common	Reference Voltage	
2	+5V	Input	Positive Supply Voltage	Supplies all PMAC digital circuits

This terminal block can be used to provide the input for the power supply for the circuits on the PMAC2 board when it is not in a bus configuration. When the PMAC2 is in a bus configuration, these supplies automatically come through the bus connector from the bus power supply; in this case, this terminal block should not be used.

TB2 (3-Pin Terminal Block)



Pin#	Symbol	Function	Description	Notes
1	WD_NC	Output	Watchdog Relay Out	Normally closed
2	Com	Input	Watchdog Return	+V or 0V
3	WD_No	Output	Watchdog Relay Out	Normally open

This terminal block provides the output for PMAC2's watchdog timer relay, both normally open and normally closed contacts. The normally open relay contact is closed while PMAC2 is operating properly, and open when PMAC2 is not operating properly.

Note: The normally closed relay contact is open while PMAC2 is operating properly (it has power and the watchdog timer is not tripped), and closed when the PMAC2 is not operating properly (either it has lost power or the watchdog timer has tripped).

MACRO Interface Connectors

Version 1: Fiber Optic Transceiver

Lower port - Transmit Optical Data
Upper port - Receive Optical Data

Version 2: Coaxial Cable Connectors

J12 - Receive Main Data
J13 - Receive Complementary Data
J15 - Transmit Complementary Data
J16 - Transmit Main Data

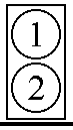
Version 3: RJ-45 Phone Jack Connectors

J14 - Receive Data
J17 - Transmit Data

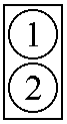
Jumper Summary

The following paragraphs provide the physical layout, location, and default setting of the jumpers on the PMAC2 PC Ultralite. Refer to the PMAC2 PC Ultralite layout diagram for jumper locations.

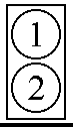
E0: External Boot Enable

E Point and Physical Layout	Location	Description	Default
E0 	B3	Remove jumper to boot card in normal fashion, with firmware from on-board flash IC. Jump pins 1 to 2 to boot card with external firmware.	No jumper installed

E1: Card 0 Select

E Point and Physical Layout	Location	Description	Default
E1 	C1	Remove jumper to specify that this PMAC is Card 0, which generates its own phase and servo clock (default). Jump pins 1 to 2 to specify that this PMAC is not Card 0, but Card 1 to F (15), which requires external phase and servo clock signals from the serial port to operate.	No jumper installed

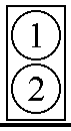
E2: 40MHZ/60MHZ CPU Operation

E Point and Physical Layout	Location	Description	Default
E2 	C1	Remove jumper to specify 40 MHz operation of the PMAC CPU (2 x crystal frequency). Jump pins 1 to 2 to specify 60 MHz operation of the PMAC CPU (3 x crystal frequency).	No jumper installed (standard) 1-2 jumper installed (Option 5B)

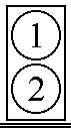
E3: Re-Initialization on Reset Control

E Point and Physical Layout	Location	Description	Default
E3 	C1	Remove jumper for normal reset mode (default). Jump pins 1 to 2 for re-initialization on reset.	No jumper installed

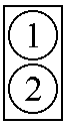
E4: 80 MHz CPU Operation

E Point and Physical Layout	Location	Description	Default
E4 	C1	Remove jumper for 40 or 60 MHz operation (see E2). Jump pins 1-2 for 80 MHz operation (with E2 OFF).	No jumper installed

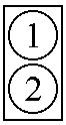
E4-E6: (Reserved for Future Use)

E Point and Physical Layout	Location	Description	Default
E4-E6 	C1		No jumper installed

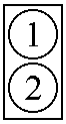
E7: IRQ10 PC Interrupt Select

E Point and Physical Layout	Location	Description	Default
E7 	D4	Jump E7 pin 1 to 2 to permit PMAC2 PC Ultralite to interrupt PC on ISA bus interrupt line IRQ10. Remove E7 jumper to inhibit interrupt capability on this line.	No jumper installed

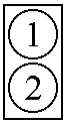
E8: IRQ11 PC Interrupt Select

E Point and Physical Layout	Location	Description	Default
E8 	D4	Jump E8 pin 1 to 2 to permit PMAC2 PC Ultralite to interrupt PC on ISA bus interrupt line IRQ11. Remove E8 jumper to inhibit interrupt capability on this line.	No jumper installed

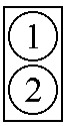
E9: IRQ12 PC Interrupt Select

E Point and Physical Layout	Location	Description	Default
E9 	D3	Jump E9 pin 1 to 2 to permit PMAC2 PC Ultralite to interrupt PC on ISA bus interrupt line IRQ12. Remove E9 jumper to inhibit interrupt capability on this line	No jumper installed

E10: IRQ14 PC Interrupt Select

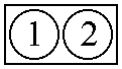
E Point and Physical Layout	Location	Description	Default
E10 	D3	Jump E10 pin 1 to 2 to permit PMAC2 PC Ultralite to interrupt PC on ISA bus interrupt line IRQ14. Remove E10 jumper to inhibit interrupt capability on this line.	No jumper installed

E11: IRQ15 PC Interrupt Select

E Point and Physical Layout	Location	Description	Default
E11 	D3	Jump E11 pin 1 to 2 to permit PMAC2 PC Ultralite to interrupt PC on ISA bus interrupt line IRQ15. Remove E11 jumper to inhibit interrupt capability on this line.	No jumper installed

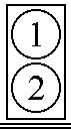
E12-E15: Reserved for Future Use

E19: Watchdog Control Jumper

E Point and Physical Layout	Location	Description	Default
E19 	A3	Jump pin 1 to 2 to disable Watchdog timer (for test purposes only). Remove jumper to enable Watchdog timer.	No jumper installed

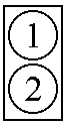
E20: Battery-Backed RAM Enable

E40: Electrical/Optical MACRO Input Select

E Point and Physical Layout	Location	Description	Default
E40 	E3	Jump E40 pin 1 to 2 to select MACRO input from fiber optic receiver. Remove E40 jumper to select MACRO input from electrical RJ45 receiver.	Jumper installed (Option A) No jumper installed (Option C)

E41: MACRO Signal Test Points

JP3: Internal/External MACRO Electrical Select

E Point and Physical Layout	Location	Description	Default
JP3 	E3	Jump JP3 pin 1 to 2 to disable internal loopback MACRO communications and permit true electrical MACRO communications. Remove JP3 jumper to select internal loopback MACRO communications (for test purposes only).	Jumper installed

JP4-JP6: Reserved for Future Use

Dip Switch Block S1: PC Bus Base Address

The 12 dip switches on block S1 set the base address of the PMAC2 on the PC bus. Together they form a binary number. Each switch, if in the closed position, sets its bit to 0; if in the open position, sets its bit to 1. The possible base addresses are all multiples of 16, so switch 1 sets a bit value of 16, switch 2 sets a bit value of 32, and so on.

Switch #	Location	Bit Value	Default	Default Value	Your Value
1	C1	16 (10h)	Open (X1)	16 (10h)	
2	C1	32 (20h)	Closed (X0)	0	
3	C1	64 (40h)	Closed (X0)	0	
4	C1	128 (80h)	Closed (X0)	0	
5	C1	256 (100h)	Closed (X0)	0	
6	C1	512 (200h)	Open (X1)	512 (200h)	
7	C1	1024 (400h)	Closed (X0)	0	
8	C1	2048 (800h)	Closed (X0)	0	
9	C1	4096 (1000h)	Closed (X0)	0	
10	C1	8192 (2000h)	Closed (X0)	0	
11	C1	16384 (4000h)	Closed (X0)	0	
12	C1	32768 (8000h)	Closed (X0)	0	
Total				528 (210h)	

To set the board to a different bus address, it is best to specify that address in hexadecimal form, because each hex digit corresponds to four switches. The last hex digit of the base address is always zero.

For example, to set the base address on the PC bus to 992 decimal, or 03E0 hex. The first 0 corresponds to switches 9 through 12. All of these should be closed to set their bits to 0. The 3 corresponds to switches 5 through 8. Switches 8 and 7 should be closed, and switches 6 and 5 should be open to define the 3. The E corresponds to switches 1 through 4. Switches 4, 3, and 2 should be open, and switch 1 should be closed to define the E.

Switch #	12	11	10	9	8	7	6	5	4	3	2	1	-	-	-	-
Hex				0				3				E				0
Binary	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
Setting	cl	cl	cl	cl	cl	cl	op	op	op	op	op	cl	-	-	-	-
cl = Closed; op = Open																

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