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HARDWARE REFERENCE MANUAL

Universal PMAC Lite

Programmable Multi-Axis Controller

3Ax-602402-UHxx

October 2001



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INTRODUCTION

Overview



The PMAC Lite is a member of the PMAC1 family of boards optimized for interface to traditional servo drives with single analog inputs representing velocity or torque commands. Its software is capable of eight axes of control. It has four channels of on-board axis interface circuitry. It can also support up to eight channels of off-board axis interface circuitry through its expansion port, connected to an Acc-24P board.

The PMAC Lite is a full-sized ISA-bus expansion board. While the PMAC Lite is capable of ISA bus communications, with or without the optional dual-ported RAM, it does not need to be inserted into an ISA expansion slot. Communications can be done through an RS-232 or RS-422 serial port; standalone operation is possible.

The new Universal PMAC Lite board replaces the previous PMAC Lite board with battery-backed RAM and the PMAC 1.5 Lite board with flash-backed RAM. The Universal PMAC Lite can be built to use either type of memory.

Board Configuration

Base Version

The base version of the PMAC Lite provides a 1-slot board with:

- 20 MHz DSP56002
- 128k x 24 SRAM active memory
- Battery-backup circuitry for SRAM (PMAC Lite)
- 128k x 8 EPROM for firmware (PMAC Lite)
- 512k x 8 flash memory for SRAM backup and firmware (PMAC1.5-Lite)
- Latest released firmware version
- RS-232/422 serial interface, ISA (PC) bus interface
- Four channels axis interface circuitry, each including:
  - 16-bit +/-10V analog output
  - 3-channel differential/single-ended encoder input
  - Four input flags, two output flags
  - Interface to external 16-bit serial ADC
- Display, control panel, muxed I/O, direct I/O interface ports
- PID/notch/feedforward servo algorithms
- 1-year warranty from date of shipment
- One CD manual per set of one to four PMACs in shipment
  (Cables, mounting plates, mating connectors not included)

If the PMAC1 Lite version (battery-backed memory) of the board is ordered, the standard configuration will have SRAM ICs in U6, U9, and U15, filling the full footprint, and a battery in BT1. There will be no SRAM ICs in U7, U10, and U16. There will be an EPROM IC in the U5 socket.

If the PMAC 1.5 Lite version (flash-backed memory) of the board is ordered, the standard configuration will have SRAM ICs in U7, U10, and U16. There will be a flash-memory IC in the U5 socket. There will be no SRAM ICs in U6, U9, and U15, and no battery in BT1, unless Option 16 is ordered.

Option 2: Dual Ported RAM

Dual-ported RAM provides a high-speed communications path for bus communications with the host computer through a bank of shared memory. DPRAM is advised if more than about 100 data items per second are to be passed between the controller and the host computer in either direction.

- Option 2 provides an on-board 8k x 16 bank of dual-ported RAM. The key component on the board is U46. (Note that for previous versions of the PMAC Lite, this was a separate board.)

Option 5: CPU and Memory Configurations

If the 20 MHz CPU that comes standard does not have sufficient computational power, faster versions are available as options. These options provide faster CPU ICs in U13 and faster SRAM ICs in U7, U10, and U16. They are available only with flash-memory backup of the SRAM.

- Option 5A provides a 40 MHz CPU with zero-wait-state SRAM active memory and flash backup.
- Option 5B provides a 60 MHz CPU with zero-wait-state SRAM active memory and flash backup.
- Option 5C provides an 80 MHz CPU with zero-wait-state SRAM active memory and flash backup.

Option 6: Extended Servo Algorithm

The standard PID servo algorithm with feedforward and notch filter is suitable for most applications. Systems with difficult dynamics, especially with significant flexibility, may require a more powerful servo algorithm, such as the Extended Servo Algorithm (ESA).

- Option 6 provides firmware in the PMAC Lite that replaces the standard PID servo algorithm with the Extended Servo Algorithm. This option provides different firmware in the U5 flash-memory/ EPROM IC. If loaded at the factory, this IC will have a 1 suffix on the labeled and reported version number (e.g. V1.16D1).

Option 7: Plate Mounting

If the PMAC Lite is used as an ISA bus expansion board, the standard hardware provides for proper mounting of the board in the bus. However, if it is not installed in an ISA expansion slot, other provisions must be made for mounting.

- Option 7 provides a mounting plate connected to the PMAC Lite with standoffs. It is used to install the PMAC Lite in standalone applications.

Option 8: High-Accuracy Clock Crystal

The PMAC Lite has a clock crystal (component Y1) of nominal frequency 19.6608 MHz (~20 MHz). The standard crystal's accuracy specification is +/-100 ppm. Long-term velocity accuracy is limited by the accuracy of the crystal, unless an external time base is used.

- Option 8A provides a nominal 19.6608 MHz crystal with a +/-15 ppm accuracy specification.

Option 9: RS-422 Interface (Obsolete)

The RS-422 interface now comes standard with the PMAC Lite in addition to the RS-232 interface. There is no need to order Option 9L as before.

Option 10: Firmware Version Specification

Normally the PMAC Lite is provided with the newest released firmware version. A label on the U5 flash-memory/EPROM IC shows the firmware version loaded at the factory.

- Option 10 provides for a user-specified firmware version.

Option 14: Replacement of Flag Opto-Isolators with Socketed Shunts

Normally, the flag inputs on all servo channels have opto-isolator circuits that require 12 to 24V inputs to turn on. When the Acc-8D Option 8 Analog Encoder Interpolator is used on a pair of channels, it uses the flag inputs on the second (even-numbered) channel to provide sub-count information at 5V levels referenced to digital ground.

- Option 14 for the replacement of the opto-isolators on the even-numbered channels of PMAC Lite with socketed shunts that permit the input of 5V non-isolated signals from the ACC-8D Option 8 board.

Option 15: V-to-F Converter for Analog Input

The JPAN control panel port on the PMAC Lite has an optional analog input called Wiper (because it is often tied to a potentiometer's wiper pin). PMAC Lite can digitize this signal by passing it through an optional voltage-to-frequency converter, using E-point jumpers to feed this into the Encoder 4 circuitry (no other use is then permitted), and executing frequency calculations using the time base feature of the encoder conversion table.

- Option 15 provides a voltage-to-frequency converter that permits the use of the Wiper input on the control panel port.

Option 16: Battery-Backed Parameter Memory

The contents of the main flash-backed memory (components U7, U10, and U16) of the PMAC 1.5 Lite are not retained through a power-down or reset unless they have been saved to flash memory first. Option 16 provides supplemental battery-backed RAM for real-time parameter storage that is ideal for holding machine state parameters in case of an unexpected power-down. It can only be ordered if the main memory is flash-backed.

- Option 16 provides a 16k x 24 bank of battery-backed parameter RAM in components U6, U9, U15 (smaller than the full footprint, with the battery in BT1.

PMAC Connectors and Indicators

J1 - Display Port Outputs (JDISP Port)

The JDISP connector allows connection of the ACC-12 or ACC-12A liquid crystal displays, or of the ACC-12C vacuum fluorescent display. Both text and variable values may be shown on these displays through the use of the **`DISPLAY`** command, executing in either motion or PLC programs.

J2 - Control-Panel Port I/O (JPAN Port)

The JPAN connector is a 26-pin connector with dedicated control inputs, dedicated indicator outputs, a quadrature encoder input, and an analog input (requires PMAC Option 15). The control inputs are low true with internal pull-up resistors. They have predefined functions unless the control-panel-disable I-variable (I2) has been set to 1. If this is the case, they may be used as general-purpose inputs by assigning M-variable to their corresponding memory-map locations (bits of Y address $FFC0).

J3 - Thumbwheel Multiplexer Port I/O (JTHW Port)

The Thumbwheel Multiplexer Port, or Multiplexer Port, on the JTHW connector has eight input lines and eight output lines. The output lines can be used to multiplex large numbers of inputs and outputs on the port, and Delta Tau provides accessory boards and software structures (special M-variable definitions) to capitalize on this feature. Up to 32 of the multiplexed I/O boards may be daisy-chained on the port, in any combination.

J4 – RS-232 Serial Port Connection (JRS232 Port)

Both RS-232 and RS-422 ports are always provided, and jumpers must be set correctly to use the port of your choice. Jumpers E107 and E108 must connect pins 1 and 2 to use the RS-232 port on the J4 connector. J4 and J4A cannot be used at the same time.

J4A – RS-422 Serial Port Connection (JRS422 Port)

Both RS-232 and RS-422 ports are always provided, and jumpers must be set correctly to use the port of your choice. Jumpers E107 and E108 must connect pins 2 and 3 to use the RS-422 port on the J4A connector. J4 and J4A cannot be used at the same time.

J5 - General-Purpose Digital Inputs and Outputs (JOPTO Port)

PMAC's JOPTO connector provides eight general-purpose digital inputs and eight general-purpose digital outputs. Each input and each output has its own corresponding ground pin in the opposite row. The 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules. Acc-21F is a six-foot cable for this purpose.

J6 - Auxiliary I/O Port Connector (JXIO Port)

This connector is used for miscellaneous I/O functions related to expansion cards that are used with PMAC.

J7 - A/D Port Connector (JS1 Port)

This connector is used for bringing the signals from an Acc-28A or an Acc-28B analog to digital converter accessory board.

J8 - Position-Compare Connector (JEQU Port)

This connector provides the position-compare outputs and the amplifier enable outputs for the four servo interface channels. The PMAC position-compare feature changes an external signal when the associated encoder counter reaches a programmable position. In this way, events can be triggered to happen on the actual position of the system. Because the triggering is a pure hardware function (although setup is software), it is very fast and accurate. The signal can be used to trigger an action in the host computer, in the plant, or in PMAC itself.

J11 - Machine Connector (JMACH Connector)

Since the PMAC Lite is limited to four on-board axes, it has only one JMACH machine interface connector, which is labeled J11. This connector contains the pins for four channels of machine I/O: analog outputs, incremental encoder inputs, and associated input and output flags, plus power-supply connections.

TB1 – Power Supply Terminal Block

This terminal block can be used to provide the input for the power supply for the circuits on the PMAC Lite board when it is not in a bus configuration.

LED Indicators

The PMAC Lite has three LED indicators: red, yellow, and green. When the green LED is lit, this indicates that power is applied to the +5V input; when the red LED is lit; this indicates that the watchdog timer has tripped and shut down the PMAC.

The yellow LED located beside the red and green LEDs, when lit, indicates that the phase-locked loop that multiplies the CPU clock frequency from the crystal frequency on the Option CPU is operational and stable. This indicator is for diagnostic purposes only; it may not be present on your board.

Fuse

The 5V output through the J5 JOPTO connector is protected by F1, a 2-Amp fuse.

PMAC System Configuration Incompatibilities

In general, PMAC, its options, and its accessories can be mixed and matched at will. However, some combinations are not permissible. These combinations are listed below.

JEXP Expansion Port Accessories

Acc-24P/V and Acc-29P/V may not be used on the same PMAC due to addressing conflicts. To interface with MLDT feedback devices the PMAC2 controller is recommended instead of the PMAC1 and Acc-29P/V combination. The PMAC can interface with two off-board DSPGATEs. The Acc-24P/V can have either only one DSPGATE or a second DSPGATE when Acc-24P/V Option 1 is ordered. The Acc-51P can have only one DSPGATE.

Due to bus drive limitations, a limit of four with an absolute maximum of six expansion port (JEXP) accessories is recommended on any PMAC. In addition, the address spaces for Acc-14D/V and Acc-36P/V boards on the JEXP expansion port are limited to six. One Acc-14D/V occupies a full address space; four Acc-36P/V boards occupy one address space.

JTHW Thumbwheel Multiplexer Port Accessories

A total of 32 boards can be plugged into the thumbwheel multiplexer port (JTHW).

The Acc-27 Opto-Isolated I/O board cannot be used with any other accessory that connects through the thumbwheel multiplexer port (JTHW): the Acc-8D Opt 7 R/D converter (if absolute power-on position is desired); the Acc-8D Opt 9 Yaskawa Encoder Interface, the ACC-18 thumbwheel board, or any of the Acc-34 family of serial I/O boards. This is because the Acc-27 uses the port in non-multiplexed fashion.

There is a limit of 256 addresses for multiplexed accessories on the JTHW thumbwheel multiplexer port: the Acc-8D Opt 7 R/D converter (if absolute power-on position is desired); the Acc-8D Opt 9 Yaskawa Encoder Interface, the Acc-18 thumbwheel board, or any of the ACC-34 family of serial I/O boards.

An Acc-8D Opt 7 board occupies one address.
An Acc-8D Opt 9 board occupies one address.
An Acc-18 board occupies eight consecutive addresses, starting with an address divisible by 8.
An Acc-34 type board occupies eight consecutive addresses, starting with an address divisible by 8.

There are no known cases of anyone using all of these address spaces.

JPAN Control Panel Port Accessories

The Acc-16D control panel and the Acc-39 handwheel encoder converter cannot be used on the same PMAC because both use the entire JPAN control panel port.

JDISP Display Port Accessories

Only one display can be connected to the JDISP display port. This includes any of the Acc-12 family of displays, and the built-in display in the Acc-16D control panel.

JSx Port Accessories

Each Acc-28 A/D converter board must interface to a separate DSPGATE gate array IC on PMAC or Acc-24P/V through its JSx connector. Therefore, the limitations on numbers of Acc-28s for a PMAC are as follows:

PMAC Lite; no ACC-24P/V	1 ACC-28
PMAC Lite; ACC-24P, no Opt 1	2 ACC-28s
PMAC Lite; ACC-24P with Opt 1	3 ACC-28s

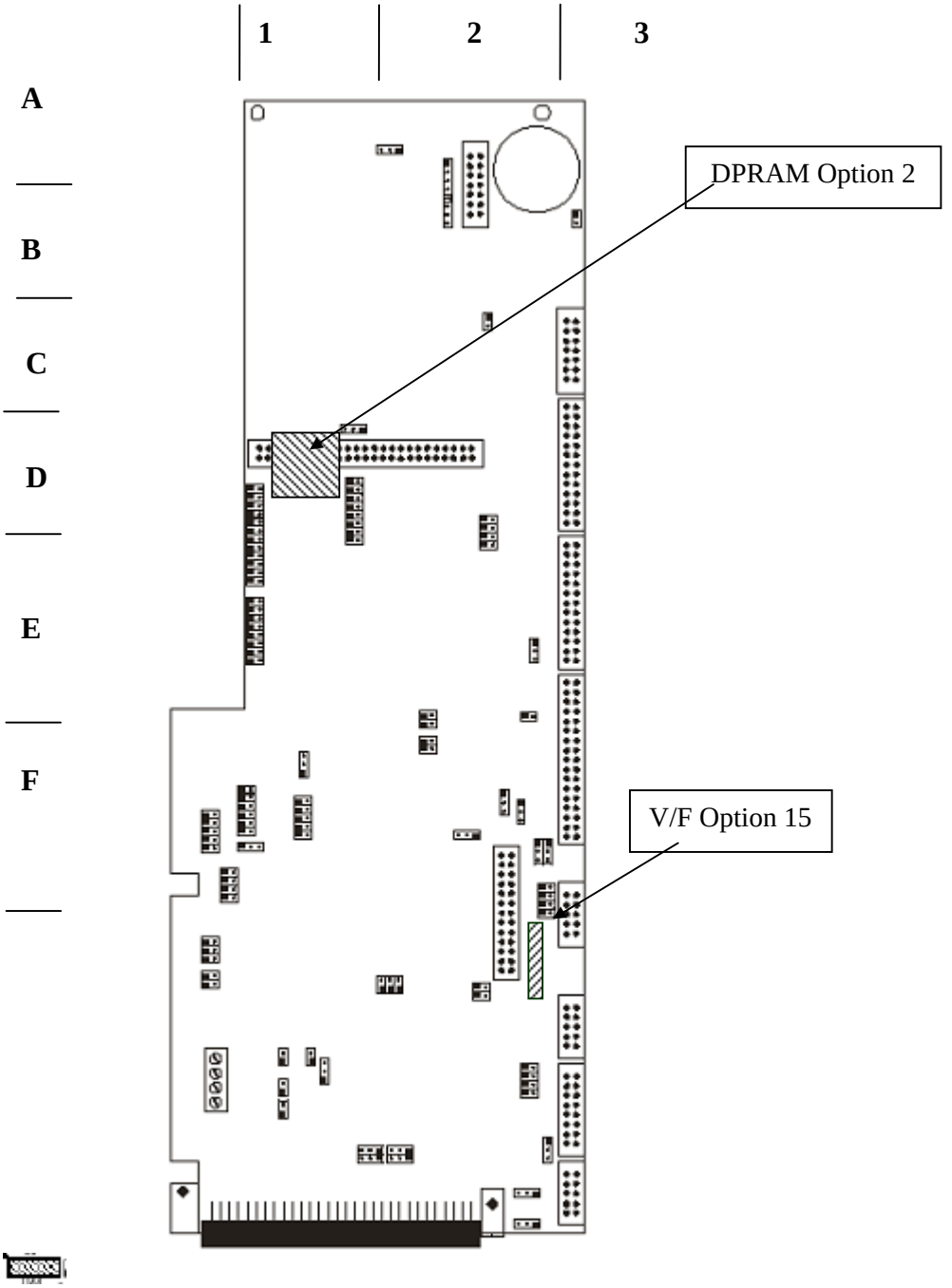
Resistor Pack Configuration

Termination Resistors

The PMAC Lite provides sockets for termination resistors on differential input pairs coming into the board. As shipped, there are no resistor packs in these sockets. If these signals are brought long distances into the PMAC Lite board and ringing at signal transitions is a problem, SIP resistor packs may be mounted in these sockets to reduce or eliminate the ringing. All termination resistor packs are the type that has independent resistors (no common connection) with each resistor using two adjacent pins. The following table shows which packs are used to terminate each input device:

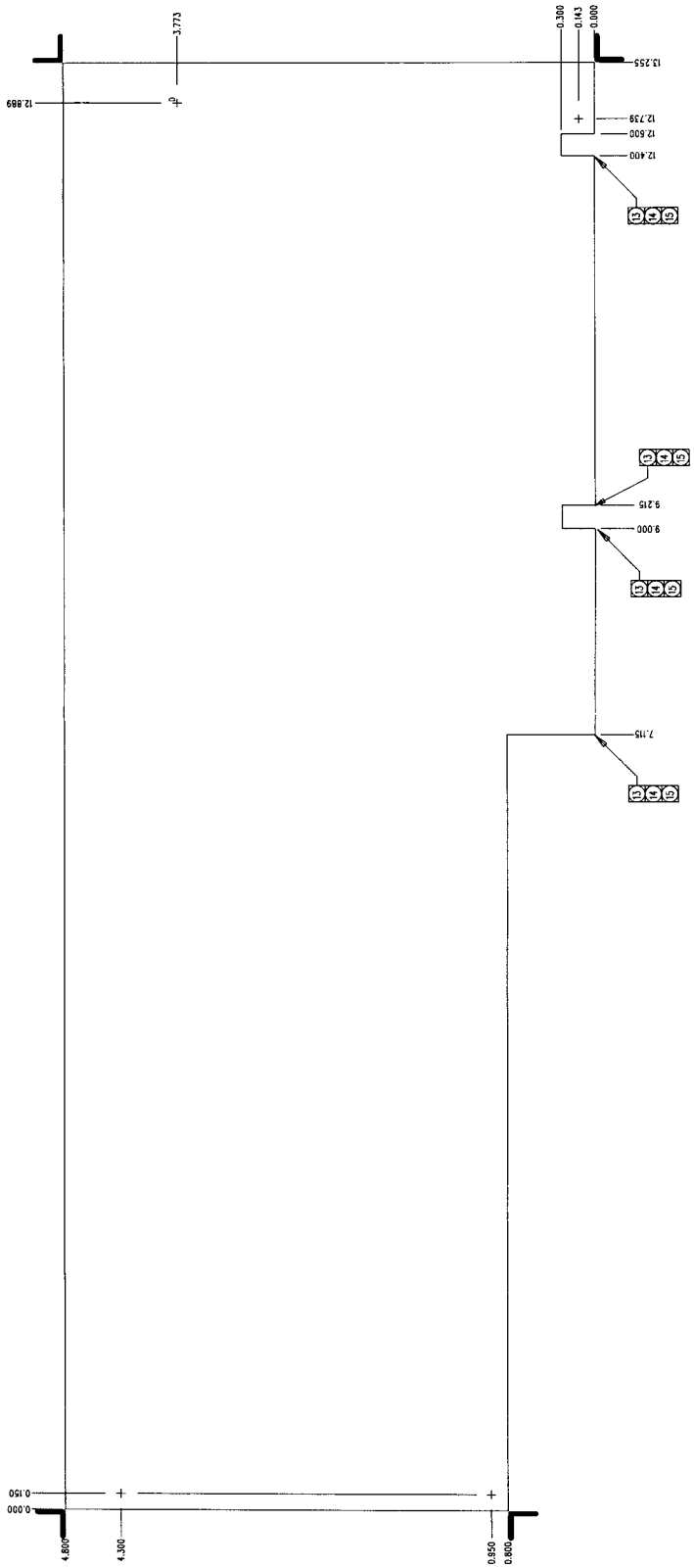
Device	Resistor Pack	Device	Resistor Pack
Encoder 1	RP51	Encoder 3	RP53
Encoder 2	RP52	Encoder 4	RP54

Universal PMAC Lite Jumpers and Connectors Layout P/N 602402



E0	E1	**E13**	F1	**E26**	H2	**E35**	E3	**E45**	C2	**E58**	C3	**E70**	D3	**E80**	F3	**E90**	G2	**E106**	A2
E1	E1	**E14**	F1	**E27**	H2	**E36**	F3	**E46**	D2	**E59**	C3	**E71**	D3	**E81**	F3	**E91**	D3	**E107**	F1
E2	E1	**E17A**	G1	**E28**	E3	**E37**	F3	**E47**	D2	**E61**	D3	**E72**	E2	**E82**	F3	**E92**	D3	**E108**	F1
E3	F3	**E17B**	G1	**E29**	F3	**E38**	F3	**E48**	D1	**E62**	D3	**E73**	E2	**E83**	G3	**E93**	C3	**E109**	B1
E4	F3	**E17C**	G1	**E30**	F3	**E39**	D3	**E49**	D1	**E63**	D3	**E74**	E2	**E84**	G3	**E94**	C3	**E110**	C2
E5	F3	**E17D**	G1	**E31**	F3	**E40**	C2	**E50**	C1	**E65**	D3	**E75**	E2	**E85**	G3	**E98**	F3	**D1**	B1
E6	F3	**E22**	G1	**E32**	E3	**E41**	C2	**E51**	C1	**E66**	D3	**E76**	F3	**E86**	G3	**E100**	H1	**D2**	B1
E7	D1	**E23**	G1	**E33**	E3	**E42**	C2	**E54**	C3	**E67**	D3	**E77**	F3	**E87**	G3	**E101**	H1	**D3**	B1
E9	F1	**E24**	H2	**E34A**	E3	**E43**	C2	**E55**	C3	**E68**	D3	**E78**	F3	**E88**	H3	**E102**	H1	**D21**	G1
E10	F1	**E25**	H2	**E34**	E3	**E44**	C2	**E57**	C3	**E69**	D3	**E79**	F3	**E89**	G2	**E103**	A1	**F1**	F1

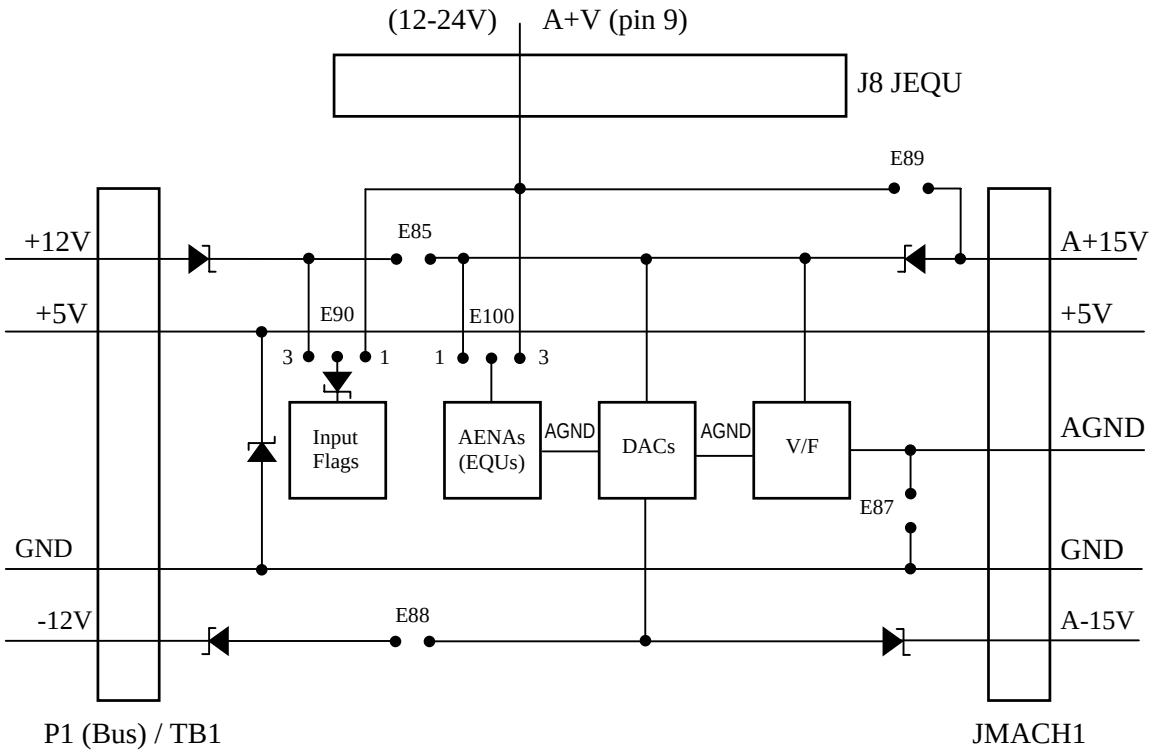
Universal PMAC Lite Dimensions Part Number 602402



JUMPERS SETUP SUMMARY

On the PMAC Lite, there are many jumpers (pairs of metal prongs) called E-points. Some have been shorted together; others have been left open. These jumpers customize the hardware features of the board for a given application and must be setup appropriately. The following is an overview of the several PMAC jumpers grouped in appropriate categories. For a complete description of the jumper setup configuration, refer to the PMAC Lite Jumpers Descriptions section of this manual.

Power-Supply Configuration Jumpers



E85, E87, E88: Analog Circuit Isolation Control – These jumpers control whether the analog circuitry on the PMAC Lite is isolated from the digital circuitry, or electrically tied to it. In the default configuration, these jumpers are off, keeping the circuits isolated from each other (provided separate isolated supplies are used).

Putting E87 ON ties the digital GND reference signal to the analog AGND reference signal, defeating the isolation between the circuits. Putting E85 ON ties the digital +12V supply line to the analog A+15V supply line. Putting E88 ON ties the digital –12V supply line to the analog A-15V supply line. Putting these jumpers on permits the bus +/-12V supply to power PMAC's analog circuits.

E89-E90: Input Flag Supply Control – If E90 connects pins 1 and 2 and E89 is ON, the input flags (+LIMn, -LIMn, HMFLn, and FAULTn) are supplied from the analog A+15V supply, which can be isolated from the digital circuitry. If E90 connects pins 1 and 2 and E89 is OFF, the input flags are supplied from a separate A+V supply brought in on pin 9 of the J8 JEQU connector. This supply can be in the +12V to +24V range, and can be kept isolated from the digital circuitry. If E90 connects pins 2 and 3, the input flags are supplied from the digital +12V supply, and isolation from the digital circuitry is defeated.

Clock Configuration Jumpers

E98: DAC/ADC Clock Frequency Control – Leave E98 in its default setting of 1-2, which creates a 2.45 MHz DCLK signal, unless you are connecting an Acc-28 A/D-converter board. In this case, move the jumper to connect pins 2 and 3, which creates a 1.22 MHz DCLK signal.

E29-E33: Phase Clock Frequency Control – Only one of the jumpers E29 – E33A, which select the phase-clock frequency, may be on in any configuration. The default setting of E31 ON, which selects a 9 kHz phase-clock frequency, is seldom changed.

E48: Option CPU Clock Frequency Control – When PMAC is ordered with Option 5B, E48 setup the CPU clock frequency to either 40 MHz or 60 MHz.

E3-E6: Servo Clock Frequency Control – The jumpers E3 – E6 determine the servo-clock frequency by controlling how many times it is divided down from the phase-frequency. The default setting of E3 and E4 OFF, E5 and E6 ON divides the phase-clock frequency by 4, creating a 2.25 kHz servo-clock frequency. This setting is seldom changed.

E34A-E38: Encoder Sample Clock – Only one of the jumpers E34A – E38, which select the encoder sample clock frequency, may be on in any configuration. The frequency must be high enough to accept the maximum true count rate (no more than one count in any clock period), but a lower frequency can filter out longer noise spikes. The anti-noise digital delay filter can eliminate noise spikes up to 1 sample-clock cycle wide.

E40-E43: Servo and Phase Clock Direction Control – Jumpers E40-E43 control the software address of the card, for serial addressing and for sharing the servo and phase clock over the serial connector. Card @0 sends the clocks and cards @1-@F receive the clocks. If any of these jumpers is removed, PMAC PC will expect to receive external servo and phase clock signals on the J4 serial port – if these signals are not provide in this configuration, the watchdog timer will immediately trip.

Encoder Configuration Jumpers

E24-E27: Encoder Complementary Line Control– These jumpers, one per encoder, control the voltage to which the complementary channels A/, B/, and C/ are pulled. The default setting for each jumper, connecting pins 1 and 2, ties the complementary lines to 2.5V. This setting is required for single-ended encoders, and is best if the channel is left unconnected. If encoders with differential line drivers are used, the setting of these jumpers does not matter. Changing the jumpers to connect pins 2 and 3 ties the complementary lines to 5V. This setting is used for (now obsolete) complementary open-collector encoders, or if external exclusive-or loss-of-encoder circuitry is used.

The following table shows which jumper affects which encoder channel:

ENC1	E27	**ENC2**	E26	**ENC3**	E25	**ENC4**	E24

E22-E23: Control-Panel Handwheel Enable – Putting these jumpers ON ties the handwheel-encoder inputs on the JPAN control-panel port to the Channel 2 encoder circuitry. Since these inputs are single-ended, jumper E26 must connect pins 1-2. If the handwheel inputs are connected to Channel 2, no encoder should be connected to Channel 2 through the JMACH1 connector.

E72-E73: Control Panel Analog Input Enable – Putting these jumpers ON ties the output of the Option 10 voltage-to-frequency converter that can process the Wiper analog input on the JPAN control panel port to the Channel 4 encoder circuitry. If the frequency signal is connected to Channel 4, no encoder should be connected to Channel 4 through the JMACH1 connector.

E74-E75: Encoder Sample Clock Output – Putting these jumpers ON ties the encoder sample-clock signal to the CHC4 and CHC4/ lines on the JMACH1 port. This permits the clock signal to be used to synchronize external encoder-processing devices like the ACC-8D Option 8 interpolator board. With these jumpers ON, no encoder input signal should be connected to these pins.

Board Reset/Save Jumpers

E39: Reset-From-Bus Enable – Putting this jumper ON ties the ISA-bus reset line to the PMAC Lite reset line so that a bus reset will automatically reset the PMAC. However, if this jumper is ON and the PMAC Lite is not installed in an ISA bus, the PMAC will be held permanently in its reset state and will not operate.

E50: Flash-Save Enable/Disable Control – If E50 is ON (default), the active software configuration of the PMAC can be stored to non-volatile flash memory with the **SAVE** command. If the jumper on E50 is removed, this **SAVE** function is disabled, and the contents of the flash memory cannot be changed.

E51: Re-Initialization on Reset Control – If E51 is OFF (default), PMAC executes a normal reset, loading active memory from the last saved configuration in non-volatile flash memory. If E51 is ON, PMAC re-initializes on reset, loading active memory with the factory default values.

E93-E94: Reset from Bus by Software Enable – These jumpers permits hardware resets of the PMAC (which work even if the watchdog timer has tripped) through software operations from the PC. If E93 is ON, the PMAC PC powers up locked in the reset state. It can be put in the operational state by the PC writing a value of 40hex to {base address + 12}; it can be put back in the reset state by the PC writing a value of 40hex to {base address + 10}. If E94 is ON, the PMAC PC powers up in operational mode. It can be put in reset mode by the PC writing a value of 40hex to {base address + 12}; it can be put back in operational mode by the PC writing a value of 40hex to {base address + 10}.

E103: Watchdog Timer Disable – If E103 is installed the watchdog safety function will be disabled. This jumper is for testing purposes only.

E106: Power-Up/Reset Load Source – If E106 is installed when the PMAC Lite executes its reset cycle, PMAC enters a special re-initialization mode that permits the downloading of new firmware through either the serial port or the bus port. In this bootstrap mode, there are very few command options. PMAC will respond to any of the status-bit query commands (**?**, **??**, or **???**) with the response Bootstrap PROM. This permits the host to know whether PMAC is in this mode or not. PMAC will respond to the VERSION query command with the number of the bootstrap firmware (e.g. 1.01), which will probably be different than the operational firmware version. To bypass the download operation in this mode, send a <CONTROL-R> character to PMAC. This puts PMAC in the normal operational mode with the existing firmware. Factory default values for I-variables, conversion table settings, and bus addresses for DPRAM are copied from the firmware section of flash memory into active memory. The saved values of these values are not used, but they are still kept in the user section of flash memory.

Note:

Before attempting to upgrade PMAC operational firmware, make sure all of PMAC's configuration has been stored to disk. If the new firmware provides a different user memory map, PMAC will clear memory on power-up after new firmware has been loaded. Even if this is not the case, the easiest way to establish a new firmware checksum reference value is to send the $$$*** command, which clears the buffers. For any change in the operational firmware, the compiled PLCs will have to be re-compiled with the List Link file for the new firmware version. It is important to delete all compiled PLCs (Delete PLCC n) before attempting to change the operational firmware version. Compiled PLC programs running under a firmware version other than that which they were compiled for can have unpredictable consequences.

Communication Jumpers

E9-E10, E13-E14: Serial Interface Configuration Control – The E9, E10, E13, and E14 jumpers control whether the RS-232 serial port will be in DCE or DTE format. The default configuration permits straight-across connection to a PC DB-9 serial port.

E44-E47: Serial Baud Rate Selection –The configuration of these jumpers and the particular CPU Option ordered will determine the baud rate at which PMAC will communicate through its J4 serial port. For example, when PMAC is ordered with no CPU Options and only the jumpers E45 and E46 are installed, the baud rate will be set at 9600 baud.

E49: Serial Communications Parity Control – Jump pin 1 to 2 for NO serial parity; remove jumper for ODD serial parity.

E66-E71, E91-E92: ISA Bus Base Address Control – Jumpers E91, E92, E66, E67, E68, E69, E70, and E71 on the PMAC Lite determine the base address of the card in the I/O space of the host PC's expansion bus (consult the Host PC-at I/O Address Map in this manual for details on selecting the appropriate base address). Together, they form a binary number that specifies the 16 consecutive addresses on the bus where the card can be found. The jumpers form the base address in the following fashion:

Jumper	E91	E92	E66	E67	E68	E69	E70	E71
Bit #	11	10	9	8	7	6	5	4
Dec Value	2048	1024	512	256	128	64	32	16
Hex Value	800	400	200	100	80	40	20	10

If a jumper is ON, the value it contributes to the base address is ZERO.

If a jumper is OFF, the value it contributes to the base address is given in the table above.

On the PMAC Lite, the jumpers are arranged physically in the same order they are presented in the above table.

From Jumper Configuration to Address

To determine the address specified by a given jumper configuration, use the following formula:

(Decimal)
Address = 2048*E91 + 1024*E92 + 512*E66 + 256*E67 + 128*E68 + 64*E69 + 32*E70 + 16*E71
(Hexadecimal)
Address = $800*E91 + $400*E92 + $200*E66 + $100*E67 + $80*E68 + $40*E69 + $20*E70 + $10*E71

In each case, Exx = 1 if the jumper is OFF; Exx = 0 if the jumper is ON.

Example: On a PMAC card, the jumpers are in the following configuration:

E91	E92	E66	E67	E68	E69	E70	E71
ON	ON	OFF	OFF	ON	ON	ON	ON

The address can be computed as:
Decimal Address = 0 + 0 + 512 + 256 + 0 + 0 + 0 + 0 = 768
Hex Address = 0 + 0 + $200 + $100 + 0 + 0 + 0 + 0 = $300

From Address to Jumper Configuration

Once an I/O address on the PC expansion port has been selected, the following procedure can be used for setting the address jumpers.

1. Convert the address to a 3-digital hexadecimal value ($000 to $FFF, representing 0 to 4095). If the value does not fit in this range, you will not be able to set PMAC for this address. Make sure the last digit is 0; only addresses divisible by 16 are permitted as PMAC base addresses.
2. Take the first hex digit and convert it to binary. The binary digits represent bits 11 through 8 of the base address. Assign each binary digit to jumpers as follows:

Bit #	11(MSB)	10	9	8(LSB)
Jumper	E91	E92	E66	E67
Digit Value	8	4	2	1
Setting for 1	OFF	OFF	OFF	OFF
Setting for 0	ON	ON	ON	ON

3. Take the second hex digit and convert it to binary. The binary digits represent bits 7 through 4 of the base address. Assign each binary digit to jumpers as follows:

Bit #	7(MSB)	6	5	4(LSB)
Jumper	E68	E69	E70	E71
Digit Value	8	4	2	1
Setting for 1	OFF	OFF	OFF	OFF
Setting for 0	ON	ON	ON	ON

Example 1: To set up the card to be at base address 992 decimal on the PC expansion bus.

1. 992 decimal is equal to 3E0 hexadecimal.
2. The first digit of 3 is binary 0011. This sets E91 ON, E92 ON, E66 OFF, and E67 OFF.
3. The second digit of E is binary 1110. This sets E68 OFF, E69 OFF, E70 OFF, and E71 ON.

Example 2: To set up the card to be at base address 528 decimal on the PC expansion bus.

1. 528 decimal is equal to 210 hexadecimal.
2. The first digit of 2 is binary 0010. This sets E91 ON, E92 ON, E66 OFF, and E67 ON.
3. The second digit of E is binary 0001. This sets E68 ON, E69 ON, E70 ON, and E71 OFF.

Example 3: To set up the card to be at base address 544 decimal on the PC expansion bus.

1. 544 decimal is equal to 220 hexadecimal.
2. The first digit of 2 is binary 0010. This sets E91 ON, E92 ON, E66 OFF, and E67 ON.
3. The second digit of E is binary 0010. This sets E68 ON, E69 ON, E70 OFF, and E71 ON.

E54-E55, E57-E59, E61-63, E65: Interrupt Source Control – These jumpers control which signals are tied to interrupt lines IR5, IR6 and IR7 on PMAC's programmable interrupt controller (PIC), as shown in the interrupt diagram. Only one signal may be tied into each of these lines.

E76-E84, E86: Host Interrupt Signal Select – This bank of jumpers determines which ISA bus interrupt line can be used by the PMAC PC, as shown in the interrupt diagram. Only one of these sets of jumpers should be on in any configuration.

E107-E108: Serial Port Configure – Both RS-232 and RS-422 ports are always provided, and jumpers must be set correctly to use the port of your choice. Jumpers E107 and E108 must connect pins 1 and 2 to use the RS-232 port on the J4 connector; jumpers E107 and E108 must connect pins 2 and 3 to use the RS-422 port on the J4A connector.

I/O Configuration Jumpers

E1-E2: Machine Output Supply Configure – With the default sinking output driver IC (ULN2803A or equivalent) in U30 for the J5 JOPTO port outputs, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly. A wrong setting of these jumpers will damage the associated output IC.

E7: Machine Input Source/Sink Control – With this jumper connecting pins 1 and 2 (default) the machine input lines on the J5 JOPTO port are pulled up to +5V or the externally provided supply voltage for the port. This configuration is suitable for sinking drivers. If the jumper is changes to connect pins 2 and 3, these lines are pulled down to GND – this configuration is suitable for sourcing drivers.

E17A - E17D: Amplifier-Enable Polarity Control – Jumpers E17A through E17D control the polarity of the amplifier enable signal for the corresponding motor 1 to 4. When the jumper is ON (default), the amplifier-enable line for the corresponding motor is low true so the enable state is low-voltage output and sinking current, and the disable state is not conducting current. With the default ULN2803A sinking driver used by the PMAC Lite, this is the fail-safe option, allowing the circuit to fail in the disable state. With this jumper OFF, the amplifier-enable line is high true so the enable state is not conducting current, and the disable state is low-voltage output and sinking current. Generally, this setting is not recommended.

E28: Following Error/Watchdog Timer Signal Control – Jump pin 1 to 2 to allow warning following error (Ix12) for the selected coordinate system to control FEFCO/ on J8-57. Jump pin 2 to 3 to cause Watchdog timer output to control FEFCO/. Low TRUE output in either case.

E100: Auxiliary Signals Supply Control – The U50 driver IC controls the AENA, EQU, PULSE, DIR and FEFCO signals on the J8 JEQU connector. If E100 connects pins 1 and 2, U50 will be supplied from the analog A+15V supply, which can be isolated from the digital circuitry. If E100 connects pins 2 and 3, U50 will be supplied from a separate A+V supply brought in on pin 9 of the J8 JEQU connector. This supply can be in the +12V to +24V range, and can be kept isolated from the digital circuitry.

E101-E102: Auxiliary Signals Output voltage configure – The U50 driver IC controls the AENA, EQU, PULSE, DIR and FEFCO signals on the J8 JEQU connector. With the default sinking output driver IC (ULN2803A or equivalent) in U50 for the J8 JEQU port outputs, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly. A wrong setting of these jumpers will damage the associated output IC.

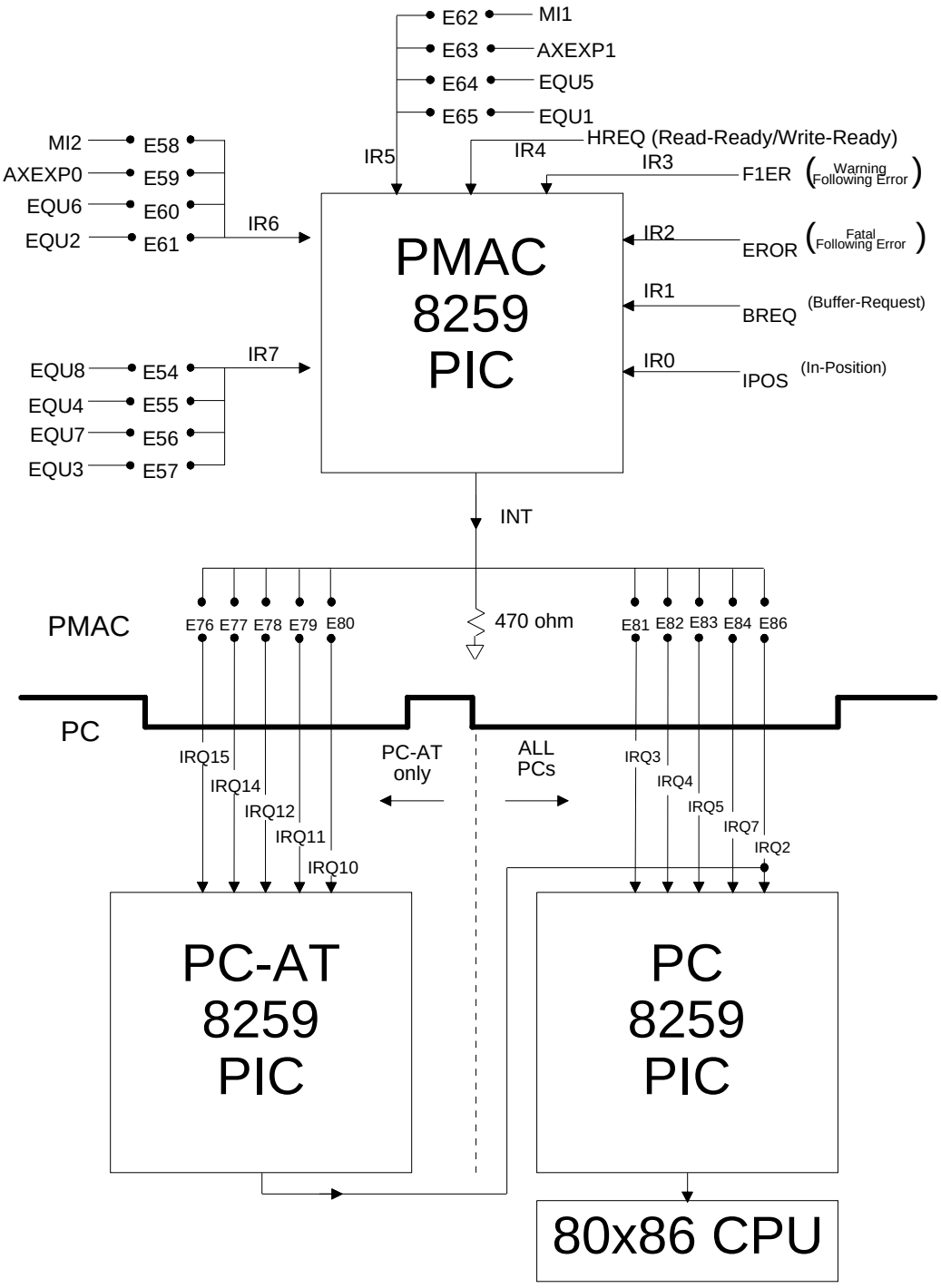
E109: Display Port Configuration – Remove jumper to use standard display driving. Jump pins 1 to 2 to use alternate display driving (to be implemented).

E110: Expansion Port Configuration – Jump pin 1 to 2 to bring address line BA04 to JEXP pin 31 to support interface to ACC-24P2 board. Jumper pin 2 to 3 to bring chip select line CS02/ to JEXP pin 31, which is required when not using the ACC-24P2 board.

Reserved Configuration Jumpers

E0: Reserved for future use

PMAC-PC INTERRUPT STRUCTURE



PMAC-LITE E-POINT DESCRIPTIONS

E1 - E2: Machine Output Supply Voltage Configure

E Point and Physical Layout	Location	Description	Default
E1 	E1	**CAUTION:** The jumper setting must match the type of driver IC or damage to the IC will result. Jump pin 1 to 2 to apply +V (+5V to 24V) to pin 11 of U26 (should be ULN2803A for sink output configuration) JOPTO Machine outputs M01-M08. Jump pin 2 to 3 to apply GND to pin 11 of U26 (should be UDN2981A for source output configuration).	1-2 Jumper installed
E2 	E1	**CAUTION** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply GND to pin 10 of U26 (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply +V (+5V to 24V) to pin 10 of U26 (should be UDN2981A for source output configuration).	1-2 Jumper installed

E3 - E6: Servo Clock Frequency Control

The servo clock (which determines how often the servo loop is closed) is derived from the phase clock (see E98, E29 - E33) through a divide-by-N counter. Jumpers E3 through E6 control this dividing function.

E3	E4	E5	E6	Servo Clock = Phase Clock Divided by N	Default and Physical Layout E3 E4 E5 E6  LOCATION F3 F3 F3 F3
ON	ON	ON	ON	N = Divided by 1	
OFF	ON	ON	ON	N = Divided by 2	
ON	OFF	ON	ON	N = Divided by 3	
OFF	OFF	ON	ON	N = Divided by 4	Only E5 and E6 ON
ON	OFF	ON	ON	N = Divided by 5	
OFF	ON	OFF	ON	N = Divided by 6	
ON	OFF	OFF	ON	N = Divided by 7	
OFF	OFF	OFF	ON	N = Divided by 8	
ON	ON	ON	OFF	N = Divided by 9	
OFF	ON	ON	OFF	N = Divided by 10	
ON	OFF	ON	OFF	N = Divided by 11	
OFF	OFF	ON	OFF	N = Divided by 12	
ON	ON	OFF	OFF	N = Divided by 13	
OFF	ON	OFF	OFF	N = Divided by 14	
ON	OFF	OFF	OFF	N = Divided by 15	
OFF	OFF	OFF	OFF	N = Divided by 16	

Notes:

The setting of I-variable I10 should be adjusted to match the servo interrupt cycle time set by E98, E29 -- E33, and E3 -- E6. I10 holds the length of a servo interrupt cycle, scaled so that 8,388,608 equals one millisecond. Since I10 has a maximum value of 8,388,607, the servo interrupt cycle time should always be less than a millisecond (unless you want to make your basic unit of time on PMAC something other than a millisecond). If you wish a servo sample time greater than one millisecond, the sampling may be slowed in software with variable Ixx60.

Frequency can be checked on J4 pins 21 and 22. It can also be checked from software by typing RX:0 in the PMAC terminal at 10-second intervals and dividing the difference of successive responses by 10000. The resulting number is the approximate Servo Clock frequency kHz.

If E40-E43 are not all ON, the phase clock is received from an external source through the J4 serial-port connector, and the settings of E3 – E6 are not relevant.

E7: Machine Input Source/Sink Control

E Point and Physical Layout	Location	Description	Default
E7 	D1	Jump pin 1 to 2 to apply +5V to input reference resistor sip pack; this will bias MI1 to MI8 inputs to +5V for OFF state; input must then be grounded for ON state. Jump pin 2 to 3 to apply GND to input reference resistor sip pack; this will bias MI1 to MI8 inputs to GND for OFF state; input must then be pulled up for ON state (+5V to +24V).	1-2 Jumper installed

E9, E10, E13, E14: Serial Interface Direction Control

The E9, E10, E13, and E14 jumpers control whether the RS-232 serial port will be in DCE or DTE format. The default configuration permits straight-across connection to a PC DB-9 serial port.

E Point & Physical Layout	Location	Description	Default
E9 E10 	F1	Jump, E9-1 to E9-2 to allow RXD/ to be input on J4-3. Jump E10-1 to E10-2 to allow TXD/ to be output on J4-5. Jump E9-1 to E10-1 to allow TXD/ to be output on J4-3. Jump E9-2 to E10-2 to allow RXD/ to be input on J4-5.	1-2 Jumpers installed
E13 E14 	F1	Jump E13-1 to E13-2 to allow RTS to be input on J4-7. Jump E14-1 to E14-2 to allow CTS to be output on J4-9. Jump E13-1 to E14-1 to allow CTS to be output on J4-7. Jump E13-2 to E14-2 to allow RTS to be input on J4-9.	1-2 Jumpers installed

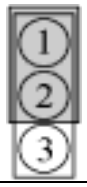
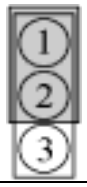
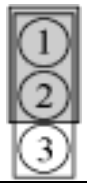
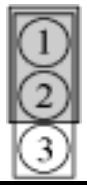
E17A-D: Amplifier Enable/Direction Polarity Control

E Point and Physical Layout	Location	Description	Default
E17A 	G1	Jump 1-2 for high-true AENA1. Remove jumper for low-true AENA1.	No jumper installed
E17B 	G1	Jump 1-2 for high-true AENA2. Remove jumper for low-true AENA2.	No jumper installed
E17C 	G1	Jump 1-2 for high-true AENA3. Remove jumper for low-true AENA3.	No jumper installed
E17D 	G1	Jump 1-2 for high-true AENA4. Remove jumper for low-true AENA4.	No jumper installed
Note: Low-true enable is the fail-safe option because of the sinking (open-collector) ULN2803A output driver IC.			

E22 - E23: Control Panel Handwheel Enable

E Point and Physical Layout	Location	Description	Default
E22 	G1	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-16 for CHB2 (ENC2-B).	No jumper
E23 	G1	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-22 for CHA2 (ENC2-A).	No jumper
Note: With these jumpers ON, no encoder should be wired into ENC2 on JMACH1. Jumper E26 must connect pins 1-2, because these are single-ended inputs. This function is unrelated to the encoder brought in through ACC-39 on J2.			

E24 - E27: Encoder Single-Ended/Differential Control

E Point and Physical Layout	Location	Description	Default
E24 	H2	ENC 4 through 1: Jump pin 1 to 2 to tie complementary encoder inputs to 2.5V.	1-2 Jumper installed for E24 - E27.
E25 	H2	Jump pin 2 to 3 to tie complementary encoder inputs to 5V. For no encoder connection: Jump pin 1 to 2.	E24: ENC 4 E25: ENC 3 E26: ENC 2 E27: ENC 1
E26 	H2	For single-ended encoders: Jump pin 1 to 2. For differential line-driver encoders: Do not care.	
E27 	H2	For complementary open-collector encoders: Jump pin 2 to 3.	

E28: Following Error/Watchdog Timer Signal Control

E Point and Physical Layout	Location	Description	Default
E28 	E3	Jump pin 1 to 2 to allow warning following error (Ix12) for the selected coordinate system to control FEFCO/ on J8-57. Jump pin 2 to 3 to cause Watchdog timer output to control FEFCO/. Low True output in either case.	2-3 Jumper installed

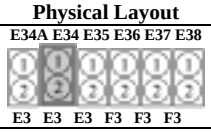
E29 - E33: Phase Clock Frequency Control

Jumpers E29 through E33 control the speed of the phase clock, and, indirectly, the servo clock, which is divided down from the phase clock (see E3 - E6). No more than one of these five jumpers may be on at a time.

					Phase Clock Frequency		Default and Physical Layout	
E29	**E30**	**E31**	**E32**	**E33**	**E98 Connects Pins 1 and 2**	**E98 Connects Pins 2 And 3**		**LOC**
ON	OFF	OFF	OFF	OFF	2.26 kHz	1.13 kHz	 **E29**	F3
OFF	ON	OFF	OFF	OFF	4.52 kHz	2.26 kHz	 **E30**	F3
OFF	OFF	ON	OFF	OFF	9.04 kHz	4.52 kHz	 **E31**	F3
OFF	OFF	OFF	ON	OFF	18.07 kHz	9.04 kHz	 **E32**	E3
OFF	OFF	OFF	OFF	ON	36.14 kHz	18.07 kHz	 **E33**	E3
Note: If E40-E43 are not all ON, the phase clock is received from an external source through the J4 serial-port connector, and the settings of E29 – E33 are not relevant.								

E34 - E38: Encoder Sampling Clock Frequency Control

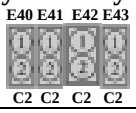
Jumpers E34 - E38 control the encoder-sampling clock (SCLK) used by the gate array ICs. No more than one of these six jumpers may be on at a time.

E34A	**E34**	**E35**	**E36**	**E37**	**E38**	**SCLK Clock Frequency**	**Default and Physical Layout** 
ON	OFF	OFF	OFF	OFF	OFF	19.6608 MHz	
OFF	ON	OFF	ON	OFF	OFF	9.8304 MHz	E34 ON
OFF	OFF	ON	OFF	OFF	OFF	4.9152 MHz	
OFF	OFF	OFF	ON	OFF	OFF	2.4576 MHz	
OFF	OFF	OFF	OFF	ON	OFF	1.2288 MHz	
OFF	OFF	OFF	OFF	OFF	ON	External clock 1 to 30 MHz maximum input on CHC4 and CHC4/	

E39: Reset-From-Bus Enable

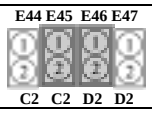
E Point and Physical Layout	**Location**	**Description**	**Default**
E39 	D3	Jump pin 1 to 2 to allow PMAC to derive its reset from the PC backplane. Remove jumper to allow PMAC to power up in normal way; PC bus hardware reset will not reset PMAC; must be removed for standalone operation. Only one of E39, E93, and E94 should be on at once. See also E93 and E94	No jumper

E40 - E43: Servo and Phase Clock Direction Control

E40	E41	E42	E43	Card Address	Servo and Phase Clock Direction	Default and Physical Layout 
ON	ON	ON	ON	@0	Output	(All on)
OFF	ON	ON	ON	@1	Input	
ON	OFF	ON	ON	@2	Input	
OFF	OFF	ON	ON	@3	Input	
ON	ON	OFF	ON	@4	Input	
OFF	ON	OFF	ON	@5	Input	
ON	OFF	OFF	ON	@6	Input	
OFF	OFF	OFF	ON	@7	Input	
ON	ON	ON	OFF	@8	Input	
OFF	ON	ON	OFF	@9	Input	
ON	OFF	ON	OFF	@A	Input	
OFF	OFF	ON	OFF	@B	Input	
ON	ON	OFF	OFF	@C	Input	
OFF	ON	OFF	OFF	@D	Input	
ON	OFF	OFF	OFF	@E	Input	
OFF	OFF	OFF	OFF	@F	Input	
Note: If any jumper E40 – E43 is removed and the servo and phase clocks are not brought in on the J4A serial port, the watchdog timer will trip immediately.						

E44 - E47: Serial Baud Rate Control

Jumpers E44 - E47 control what baud rate to use for serial communications. Any character received over the bus causes PMAC to use the bus for its standard communications. The serial port is disabled if E44-E47 are all on.

Baud Rate Control "E" Points				Baud Rate				Default and Physical Layout
E44	**E45**	**E46**	**E47**	**20 MHz Flash CPU (OPT 4A)**	**Battery CPU, 40 MHz Flash CPU (Opt 5A)**	**60 MHz Flash CPU (Opt 5B)**	**80 MHz Flash CPU (Opt 5C)**	
ON	ON	ON	ON	Disabled	Disabled	Disabled	Disabled	
OFF	ON	ON	ON	300	600	900	1200	
ON	OFF	ON	ON	400*	800*	1200	1600*	
OFF	OFF	ON	ON	600	1200	1800	2400	
ON	ON	OFF	ON	800*	1600*	2400	3200*	
OFF	ON	OFF	ON	1200	2400	3600	4800	
ON	OFF	OFF	ON	1600*	3200*	4800	6400*	
OFF	OFF	OFF	ON	2400	4800	7200	9600	Opt 5C
ON	ON	ON	OFF	3200*	6400*	9600	12800*	Opt 5B
OFF	ON	ON	OFF	4800	9600	14400	19200	Standard, Opt 5A
ON	OFF	ON	OFF	6400*	12800*	19200	25600*	
OFF	OFF	ON	OFF	9600	19200	28800	38400	Opt 4A (1.5-Lite)
ON	ON	OFF	OFF	12800*	25600*	38400	51200*	
OFF	ON	OFF	OFF	19200	38400	57600	76800	
ON	OFF	OFF	OFF	25600*	51200*	76800	102400*	
OFF	OFF	OFF	OFF	38400	76800	115200	153600	

* Non-standard baud rate

Note: These jumpers are only read at power-up/reset to set the baud rate at that time.

E48: CPU Clock Frequency Control

E Point and Physical Layout	Location	Description	Default
E48 	D1	Jump pins 1 and 2 to multiply crystal frequency by 3 inside CPU for 60 MHz operation. Remove jumper to multiply crystal frequency by 2 inside CPU for 40 MHz operation. Do not care for 20 MHz CPU versions. For 80 MHz operation, set jumper for 40 MHz, then increase speed in software (WX$FFFD,$750003).	No jumper installed (20, 40 and 80 MHz versions) Jumper installed (60 MHz version)

Note: It may be possible to operate a board at a frequency higher than that for which its components are rated. However, this uses the components outside of their specified operating range, and proper execution of the PMAC under these conditions is not guaranteed. PMAC software failure is possible, even probable, under these conditions, and this can lead to very dangerous machine failure. Operation in this mode is done completely at the user's own risk; Delta Tau can accept no responsibility for the operation of the PMAC or the machine under these conditions.

E49: Serial Communications Parity Control

E Point and Physical Layout	Location	Description	Default
E49 	D1	Jump pin 1 to 2 for NO serial parity; remove jumper for ODD serial parity.	Jumper installed

E50: Non-Volatile Memory Save Control

E Point and Physical Layout	Location	Description	Default
E50 	C1	Jump pin 1 to 2 to enable save to EAROM or flash memory; Remove jumper to disable save to EAROM or flash memory	Jumper installed

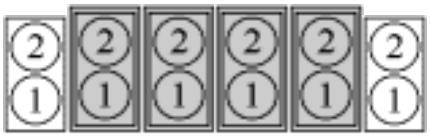
E51: Normal/Re-Initializing Power-Up

E Point and Physical Layout	Location	Description	Default
E51 	C1	Jump pin 1 to 2 to re-initialize on power-up/reset, loading factory default parameters; Remove jumper for normal power-up/reset, loading last saved parameters.	No jumper installed
Note: On the Universal PMAC Lite, the board is put in bootstrap mode for the loading of new firmware by connecting pins 2 and 3 of E106. E51 is for re-initialization of parameters only.			

E54 - E65: Host Interrupt Signal Select

E Point and Physical Layout	Location	Description	Default
 **E54**	C3	Jump pin 1 to 2 to allow WDO (watchdog output) to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
 **E55**	C3	Jump pin 1 to 2 to allow EQU4 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
 **E57**	C3	Jump pin 1 to 2 to allow EQU3 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
 **E58**	C3	Jump pin 1 to 2 to allow MI2 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
 **E59**	C3	Jump pin 1 to 2 to allow Axis Expansion Int-0 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
 **E61**	D3	Jump pin 1 to 2 to allow EQU2 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
 **E62**	D3	Jump pin 1 to 2 to allow MI1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed
 **E63**	D3	Jump pin 1 to 2 to allow Axis Expansion Int-1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed
 **E65**	D3	Jump pin 1 to 2 to allow EQU1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed

E66 - E71: Bus Base Hardware Address (Low Bits)

E Point and Physical Layout	Location	Description	Default
E66 E67 E68 E69 E70 E71 	D3	E66 - Bit 9 PC bus base address E67 - Bit 8 PC bus base address E68 - Bit 7 PC bus base address E69 - Bit 6 PC bus base address E70 - Bit 5 PC bus base address E71 - Bit 4 PC bus base address ON = 0; OFF = 1 for calculating bus address	E67-E70 installed
These jumpers work with E91 and E92 to set the base address of PMAC Lite on the PC bus. See PMAC Lite Jumpers Summary section for details on how to set these jumpers.			

E72 - E73: Panel Analog Time Base Signal Enable

E Point and Physical Layout	Location	Description	Default
E72 	E2	Jump pin 1 to 2 to allow V to F converter FOUT derived from Wiper input on J2 to connect to CHA4.	No jumper installed
E73 	E2	Jump pin 1 to 2 to allow V to F converter sign out derived from Wiper input on J2 to connect to CHB4.	No jumper installed
Note: With these jumpers ON, no encoder should be wired into ENC4 on JMACH1. E27 must connect pins 1 to 2 because these are single-ended inputs. Variable I915 should be set to 4 to create a positive voltage (frequency) number in PMAC.			

E74 - E75: Clock Output Control for Ext. Interpolation

E Point and Physical Layout	Location	Description	Default
E74 	E2	Jump pin 1 to 2 to allow SCLK/ to output on CHC4/.	No jumper installed
E75 	E2	Jump pin 1 to 2 to allow SCLK to output on CHC4.	No jumper installed
Note: SCLK out permits synchronous latching of analog encoder interpolators such as Acc-8D Opt 8.			

E76 - E84: Host Interrupt Signal Select

E Point and Physical Layout	Location	Description	Default
E76 	F3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ14.	No jumper installed
E77 	F3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ15.	No jumper installed
E78 	F3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ12.	No jumper installed
E79 	F3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ11.	No jumper installed
E80 	F3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ10.	No jumper installed
E81 	F3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ3.	No jumper installed
E82 	F3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ4.	No jumper installed
E83 	G3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ5.	No jumper installed
E84 	G3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ7.	No jumper installed
Only one of the jumpers from E76 to E84, and E86, should be ON at one time.			

E85: Host-Supplied Analog Power Source Enable

E Point and Physical Layout	Location	Description	Default
E85 	G3	Jump pin 1 to pin 2 to allow A+14V to come from PC bus (ties amplifier and PMAC Lite power supply together. Defeats OPTO coupling.). Note that if E85 is changed, E88 and E87 must also be changed. Also, see E90.	No jumper

E86: Host Interrupt Signal Select

E Point and Physical Layout	Location	Description	Default
E86 	G3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ2.	No jumper

E87 - E88: Host-Supplied Analog Power Source Enable

E Point and Physical Layout	Location	Description	Default
E87 	G3	Jump pin 1 to pin 2 to allow AGND to come from PC bus (ties amplifier and PMAC Lite GND together. Defeats OPTO coupling.) Note that if E87 is changed, E85 and E88 must also be changed. Also, see E90.	No jumper
E88 	H3	Jump pin 1 to pin 2 to allow A-14V to come from PC bus (ties amplifier and PMAC Lite power supply together. Defeats OPTO coupling.). Note that if E88 is changed, E87 and E85 must also be changed. Also, see E90.	No jumper

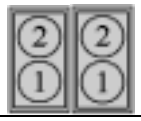
E89: Amplifier-Supplied Switch Pull-Up Enable

E Point and Physical Layout	Location	Description	Default
E89 	G2	Jump pin 1 to 2 to use A+15V on J8 (JMACH1) pin 59 as supply for input flags. Remove jumper to use A+15V/OPT+V from J7 pin 59 as supply for input flags.	Jumper installed
Note: This jumper setting is only relevant if E90 connects pin 1 to 2.			

E90: Host-Supplied Switch Pull-Up Enable

E Point and Physical Layout	Location	Description	Default
E90 	G2	Jump pin 1 to 2 to use A+15V from J8 pin 59 as supply for input flags (E89 ON) {flags should be tied to AGND} or A+15V/OPT+V from J8 pin 11 as supply for input flags (E89 OFF) {flags should be tied to separate 0V reference}. Jump pin 2 to 3 to use +12V from PC bus connector P1-pin B09 as supply for input flags {flags should be tied to GND}. See also E85, E87, E88 and PMAC Opto-isolation diagram	1-2 Jumper installed

E91 - E92: Bus Base Address Select (High Bits)

E Point and Physical Layout	Location	Description	Default
E91 E92 	D3	E91 - Bit 11 PC bus base address E92 - Bit 10 PC bus base address ON = 0 OFF = 1	Jumper installed
These jumpers work with E66 - E71 to set the base address of PMAC Lite on the PC bus. See PMAC Lite Jumpers Summary section for details on how to set these jumpers.			

E93 - E94: Reset from Bus by Software Enable

E Point and Physical Layout	Location	Description	Default
E93 	C3	Jump 1-2 to provide hardware Reset of PMAC Lite under the software control of the host-PC. PMAC Lite will power up and stay in the Reset state until PC software writes 40 HEX to Base +12. PMAC Lite can be put in Reset state by PC writing 40 HEX to Base +10. Remove jumper to disable this function. Only one of E39, E93, E94 should be ON at the same time.	No jumper
E94 	C3	Jump 1-2 to provide hardware Reset of PMAC Lite under the software control of the host-PC. PMAC Lite will power up in Normal mode. PMAC Lite can be put in Reset state by PC writing 40 HEX to Base+12. PMAC Lite can be released from Reset state by PC writing 40 HEX to Base +10. Remove jumper to disable this function. Only one of E39, E93, E94 should be ON at the same time.	No jumper

E98: DAC/ADC Clock Frequency Control

E Point and Physical Layout	Location	Description	Default
E98 	F3	Jump 1-2 to provide a 2.45 MHz DCLK signal to DACs and ADCs. Jump 2-3 to provide a 1.22 MHz DCLK signal to DACs and ADCs. Important for high accuracy A/D conversion on Acc-28. **Note**: This also divides the phase and servo clock frequencies in half. See E29-E33, E3-E6, I10	1-2 Jumper installed

E100: Output Flag Supply Select

E Point and Physical Layout	Location	Description	Default
E100 	H1	Jump pin 1 to 2 to apply analog supply voltage A+15V to U54 flag output driver IC. Jump pin 2 to 3 to apply flag supply voltage OPT+V to U54 flag output driver IC.	1-2 Jumper installed

E101 – E102: Output Flag Supply Voltage Configure

E Point and Physical Layout	Location	Description	Default
E101 	H1	**CAUTION:** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply +V (12V to 24V) to pin 10 of U54 (should be ULN2803A for sink output configuration) for AENA1-4 and EQU1-4 flag outputs. Jump pin 2 to 3 to apply AGND to pin 10 of U54 (should be UDN2981A for source output configuration) for AENA1-4 and EQU1-4 flag outputs.	1-2 Jumper installed
E102 	H1	**CAUTION:** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to AGND to pin 9 of U54 (should be ULN2803A for sink output configuration) for AENA1-4 and EQU1-4 flag outputs. Jump pin 2 to 3 to apply +V (12V to 24V) to pin 9 of U54 (should be UDN2981A for source output configuration) for AENA1-4 and EQU1-4 flag outputs.	1-2 Jumper installed

E103: Watchdog Disable Jumper

E Point and Physical Layout	Location	Description	Default
E103 	A1	Jump pin 1 to 2 to disable Watchdog timer (for test purposes only.). Remove jumper to enable Watchdog timer.	No jumper installed
Note: E104 and E105 on earlier designs permitted connecting address lines A04 and A05 onto pins 41 and 42, respectively, of the J9 expansion port. On the Universal PMAC Lite, these signals are always connected to these pins, and the jumpers are not present.			

E106: Firmware Reload Enable

E Point and Physical Layout	Location	Description	Default
E106 	A2	Remove jumper for normal operation. Jump pin 1 to 2 to lock card in reset state for programming of on-board logic (for factory use only). Jump pin 2 to 3 to reload firmware through serial or bus port on power-up/reset.	No jumper installed

E107 – E108: Serial Port Select

E Point and Physical Layout	Location	Description	Default
E107 	F1	Jump pin 1 to 2 to select RS-232 port on J4 for serial communications. Jump pin 2 to 3 to select RS-422 port on J4A for serial communications	No jumper installed
E108 	F1	Jump pin 1 to 2 to select RS-232 port on J4 for serial communications. Jump pin 2 to 3 to select RS-422 port on J4A for serial communications	No jumper installed

E109: Display Port Configuration

E Point and Physical Layout	Location	Description	Default
E109 	B1	Remove jumper to use standard display driving. Jump pins 1 to 2 to use alternate display driving (to be implemented).	No jumper installed

E110: Expansion Port Configuration

E Point and Physical Layout	Location	Description	Default
E110 	C2	Jump pin 1 to 2 to bring address line BA04 to JEXP pin 31 to support interface to ACC-24P2 board. Jumper pin 2 to 3 to bring chip select line CS02/ to JEXP pin 31.	1-2 jumper installed

MACHINE CONNECTIONS

Typically, the user connections are actually made to a terminal block that is attached to the JMACH connector by a flat cable (Acc-8D or 8P). The pinout numbers on the terminal block are the same as those on the JMACH connector. The possible choices for breakout boards are the following:

Board	Mounting	Breakout Style	Breakout Connector	Notes
ACC-8P	DIN – Rail	Monolithic	Terminal Block	Simple Phoenix contact board
ACC-8D	DIN – Rail	Monolithic	Terminal Block	Headers for connection to option boards
ACC-8DCE	DIN – Rail	Modular	D-sub connector	Fully shielded for easy CE mark compliance
ACC-8DP	Panel	Modular	D-sub connector	Used in the PC-pack product

Power Supplies

Digital Power Supply

1.75 A @ +5V (+/-5%) (8.75 W)
(Four-channel configuration, with a typical load of encoders)

- The host computer provides the 5V power supply in the case PMAC is installed in its internal bus.
- With the board plugged into the bus, it will automatically pull +5V power from the bus and it cannot be disconnected. In this case, there must be no external +5V supply, or the two supplies will fight each other, possibly causing damage. This voltage could be measured between pins 1 and 3 of the terminal block.
- In a stand-alone configuration, when PMAC is not plugged in a computer bus, it will need an external five-volt supply to power its digital circuits. The +5V line from the supply should be connected to pin 1 or 2 of the JMACH connector (usually through the terminal block), and the digital ground to pin 3 or 4. Acc-1x provides different options for the 5V power supply.

Analog Power Supply

0.3A @ +12 to +15V (4.5W)
0.25A @ -12 to -15V (3.8W)
(Eight-channel configuration)

The analog output circuitry on PMAC is optically isolated from the digital computation circuitry, and so requires a separate power supply. This is brought in on the JMACH connector. The positive supply -- +12 to +15V -- should be brought in on the A+15V line on pin 59. The negative supply -- -12 to -15V -- should be brought in on the A-15V line on pin 60. The analog common should be brought in on the AGND line on pin 58.

Typically, this supply can come from the servo amplifier; many commercial amplifiers provide such a supply. If this is not the case, an external supply may be used. Acc-2x provides different options for the ± 15V power supply. Even with an external supply, the AGND line should be tied to the amplifier common. It is possible to get the power for the analog circuits from the bus, but doing so defeats optical isolation. In this case, no new connections need to be made. However, you should be sure jumpers E85, E87, E88, E89, and E90 are set up for this circumstance. (The card is not shipped from the factory in this configuration.)

Flags Power Supply (Optional)

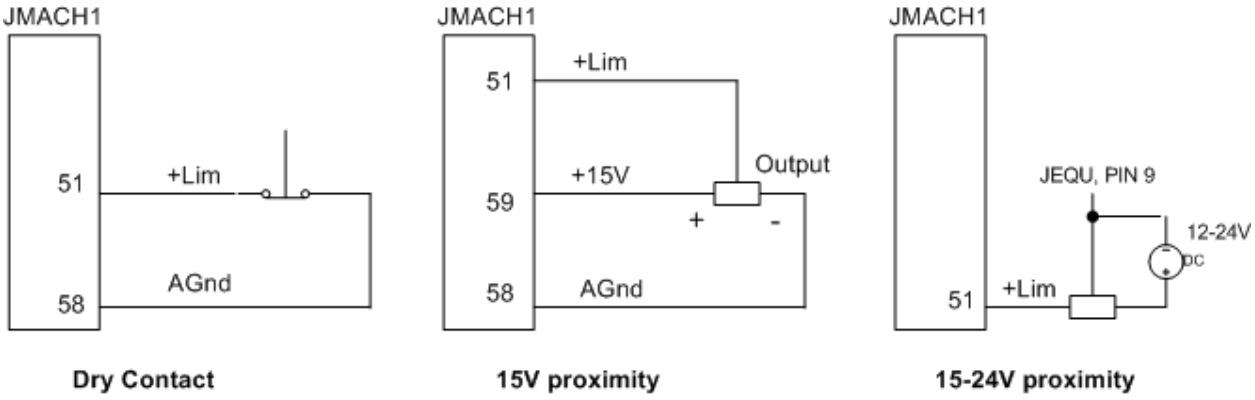
Each channel of PMAC has four dedicated digital inputs on the machine connector: +LIMn, -LIMn (overtravel limits), HMFLn (home flag), and FAULTn (amplifier fault). If the PMAC is ordered with Option-1 (8-axis PMAC), these inputs can be kept isolated from other circuits. A power supply from 12 to 24V connected on pin 9 of J8 could be used to power the corresponding opto-isolators. In this case, jumper E89 must be removed and jumper E90 must connect pins 1-2.

Overtravel Limits and Home Switches

When assigned for the dedicated uses, these signals provide important safety and accuracy functions. +LIMn and -LIMn are direction-sensitive overtravel limits, which must be actively held low (sourcing current from the pins to ground) to permit motion in their direction. The direction sense of +LIMn and -LIMn is as follows: +LIMn should be placed at the negative end of travel, and -LIMn should be placed at the positive end of travel.

Types of Overtravel Limits

PMAC expects a closed-to-ground connection for the limits to not be considered on fault. This arrangement provides a failsafe condition and therefore it cannot be reconfigured differently in PMAC. Usually a passive normally close switch is used. If a proximity switch is needed instead, use a 15V normally closed to ground NPN sinking type sensor.



Dry Contact **15V proximity** **15-24V proximity**

Jumper E89 and E90 must be set appropriately for the type of sensor used.

Home Switches

While normally closed-to-ground switches are required for the overtravel limits inputs, the home switches could be either normally close or normally open types. The polarity is determined by the home sequence setup, through the I-variables I902, I907, ... I977. However, for the following reasons, the same type of switches used for overtravel limits are recommended:

- Normally closed switches are proven to have greater electrical noise rejection than normally open types.
- Using the same type of switches for every input flag simplifies maintenance stock and replacements.

Motor Signals Connections

Incremental Encoder Connection

Each JMACH connector provides two +5V outputs and two logic grounds for powering encoders and other devices. The +5V outputs are on pins 1 and 2; the grounds are on pins 3 and 4. The encoder signal pins are grouped by number: all those numbered 1 (CHA1, CHA1/, CHB1, CHC1, etc.) belong to encoder #1. The encoder number does not have to match the motor number, but usually does. If you do not have your PMAC plugged into a bus and drawing its +5V and GND from the bus, use these pins to bring in +5V and GND from your power supply. Connect the A and B (quadrature) encoder channels to the appropriate terminal block pins. For encoder 1, the CHA1 is pin 25, CHB1 is pin 21. If you have a single-ended signal, leave the complementary signal pins floating -- do not ground them. However, if single-ended encoders are used, please check the settings of the jumpers E18 to E21 and E24 to E27. For a differential encoder, connect the complementary signal lines -- CHA1/ is pin 27, and CHB1/ is pin 23. The third channel (index pulse) is optional; for encoder 1, CHC1 is pin 17, and CHC1/ is pin 19.

Example: differential quadrature encoder connected to channel #1:



DAC Output Signals

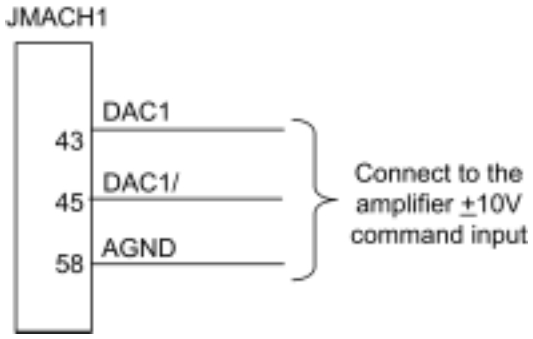
If PMAC is not performing the commutation for the motor, only one analog output channel is required to command the motor. This output channel can be either single-ended or differential, depending on what the amplifier is expecting. For a single-ended command using PMAC channel 1, connect DAC1 (pin 43) to the command input on the amplifier. Connect the amplifier's command signal return line to PMAC's AGND line (pin 58). In this setup, leave the DAC1/ pin floating; do not ground it.

For a differential command using PMAC channel 1, connect DAC1 (pin 43) to the plus command input on the amplifier. Connect DAC1/ (pin 45) to the minus-command input on the amplifier. PMAC's AGND should still be connected to the amplifier common. If the amplifier is expecting separate sign and magnitude signals, connect DAC1 (pin 43) to the magnitude input. Connect AENA1/DIR1 (pin 47) to the sign (direction input). Amplifier signal returns should be connected to AGND (pin 58). This format requires some parameter changes on PMAC; (see Ix25. Jumper E17 controls the polarity of the direction output; this may have to be changed during the polarity test. This magnitude-and-direction mode is suited for driving servo amplifiers that expect this type of input, and for driving voltage-to-frequency (V/F) converters, such as PMAC's ACC-8D Option 2 board, for running stepper motor drivers.

If using PMAC to commutate the motor, use two analog output channels for the motor. Each output may be single-ended or differential, just as for the DC motor. The two channels must be consecutively numbered, with the lower-numbered channel having an odd number (e.g. use DAC1 and DAC2 for a motor, or DAC3 and DAC4, but not DAC2 and DAC3, or DAC2 and DAC4). For the motor #1 example, connect DAC1 (pin 43) and DAC2 (pin 45) to the analog inputs of the amplifier. If using the complements as well, connect DAC1/ (pin 45) and DAC2/ (pin 46) the minus-command inputs; otherwise leave the complementary signal outputs floating. Tto limit the range of each signal to +/- 5V, use parameter Ix69.

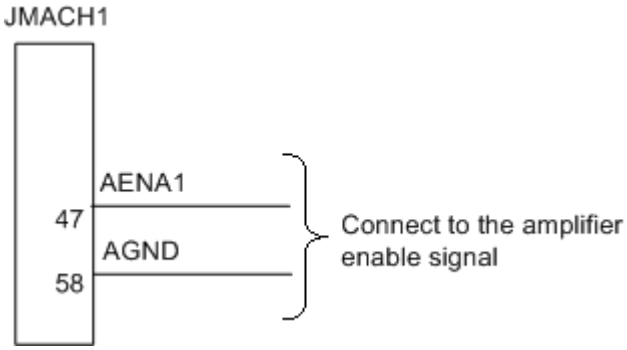
Any analog output not used for dedicated servo purposes may be utilized as a general-purpose analog output. Usually, this is done by defining an M-variable to the digital-to-analog-converter register (suggested M-variable definitions M102, M202, etc.), then writing values to the M-variable. The analog outputs are intended to drive high-impedance inputs with no significant current draw. The 220Ω output resistors will keep the current draw lower than 50 mA in all cases and prevent damage to the output circuitry, but any current draw above 10 mA can result in noticeable signal distortion.

Example:



Amplifier Enable Signal (AENAx/DIRn)

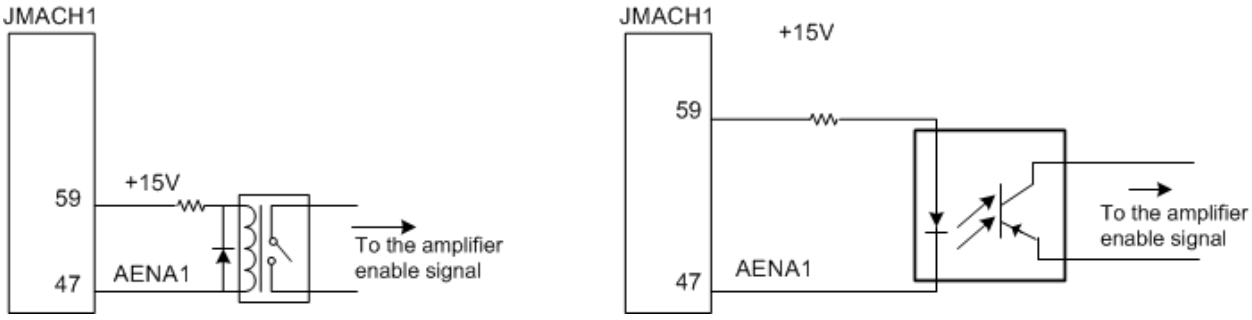
Most amplifiers have an enable/disable input that permits complete shutdown of the amplifier regardless of the voltage of the command signal. PMAC's AENA line is meant for this purpose. If not using a direction and magnitude amplifier or voltage-to-frequency converter, use this pin to enable and disable the amplifier (wired to the enable line). AENA1/DIR1 is pin 47. The polarity of the signal is controlled by jumper E17 and the default is conducting enable.



The amplifier enable signals are controlled by chip U50. If jumper E100 connects pins 1 and 2, U50 will be supplied from the analog A+15V supply, which can be isolated from the digital circuitry. If E100 connects pins 2 and 3, U50 will be supplied from a separate A+V supply brought in on pin 9 of the J8 JEQU connector. This supply can be in the +12V to +24V range, and can be kept isolated from the digital circuitry.

By default, the PMAC Lite is provided with a sinking output driver IC (ULN2803A or equivalent) in U50. In this configuration, jumpers E101 and E102 must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), E101 and E102 must be changed to connect pins 2 and 3 to supply the new IC correctly. A wrong setting of these jumpers will damage the associated output IC.

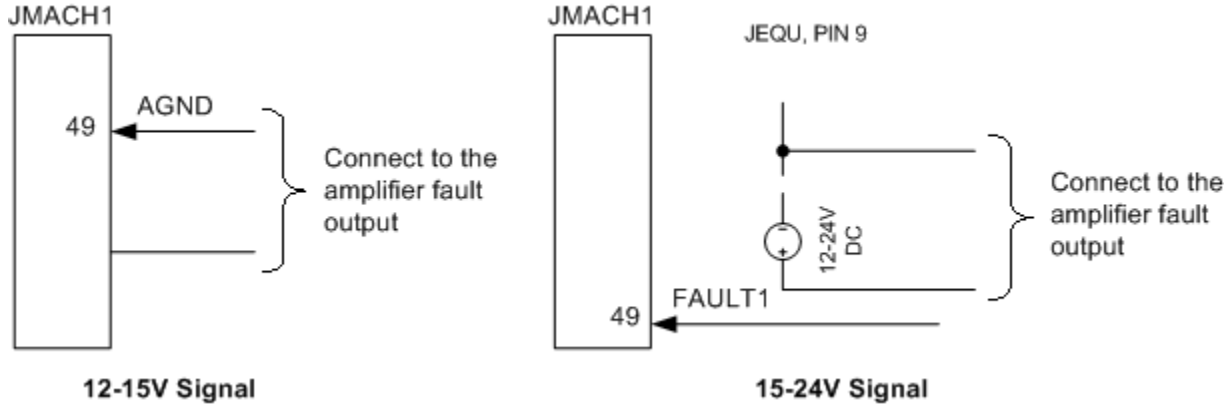
For any other kind of amplifier enable signal, like a 24V signal, a dry contact of a relay or a solid-state relay could be used:



To test the amplifier enable signal of motor x set Ix00=0 and properly define the related Mx14 variable. Then, setting Mx14=1 or Mx14=0 will change the state of the motor x amplifier enable signal to either enable or disable.

Amplifier Fault Signal (FAULTn)

This input can take a signal from the amplifier so PMAC knows when the amplifier is having problems and can shut down action. The polarity is programmable with I-variable Ix25 (I125 for motor #1) and the return signal is analog ground (AGND). FAULT1 is pin 49. With the default setup, this signal must actively be pulled low for a fault condition. In this setup, if nothing is wired into this input, PMAC will consider the motor not to be in a fault condition. The amplifier fault signal could be monitored using the properly defined Mx23 variable.



Jumper E89 and E90 must be set appropriately for the type of signal used. Some amplifiers share the amplifier fault output with the amplifier enable\disable status output. In this case, a special PLC code must be written with the following sequence: disable the amplifier fault input (see Ix25), enable the motor (J/ command), wait for the amplifier fault input to be false (monitor Mx23), re-enable the amplifier fault input (see Ix25).

General-Purpose Digital Inputs and Outputs (JOPTO Port)

PMAC's J5 or JOPTO connector provides eight general-purpose digital inputs and eight general-purpose digital outputs. Each input and each output has its own corresponding ground pin in the opposite row. The 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules. Acc-21F is a six-foot cable for this purpose. Characteristics of the JOPTO port on the PMAC-PC:

- 16 I/O points. 100 mA per channel, up to 24V
- Hardware selectable between sinking and sourcing in groups of eight; default is all sinking (inputs can be changed simply by moving a jumper; sourcing outputs must be special-ordered or field-configured)
- Eight inputs, eight outputs only; no changes. Parallel (fast) communications to PMAC CPU
- Not opto-isolated; easily connected to Opto-22 (PB16) or similar modules through ACC-21F cable

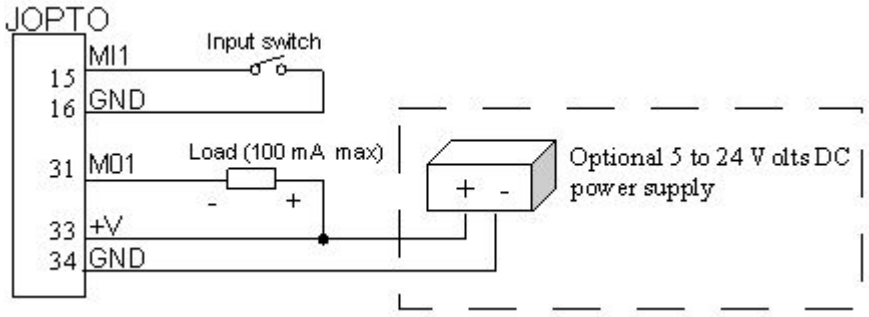
Jumper E7 controls the configuration of the eight inputs. If it connects pins 1 and 2 (the default setting), the inputs are biased to +5V for the OFF state, and they must be pulled low for the ON state. If E7 connects pins 2 and 3, the inputs are biased to ground for the OFF state, and must be pulled high for the ON state. In either case, a high voltage is interpreted as a 0 by the PMAC software, and a low voltage is interpreted as a 1.

CAUTION:

Having Jumpers E1 and E2 set wrong can damage the IC.

PMAC is shipped standard with a ULN2803A sinking (open-collector) output IC for the eight outputs. These outputs can sink up to 100 mA, but must have a pull-up resistor to go high. Do not connect these outputs directly to the supply voltage, or damage to the PMAC will result from excessive current draw. The user can provide a high-side voltage (+5 to +24V) into Pin 33 of the JOPTO connector, and allow this to pull up the outputs by connecting pins 1 and 2 of Jumper E1. Jumper E2 must also connect pins 1 and 2 for a ULN2803A sinking output. It is possible for these outputs to be sourcing drivers by substituting a UDN2981A IC for the ULN2803A. This U3 IC is socketed, and so may easily be replaced. For this driver, pull-down resistors should be used. With a UDN2981A driver IC, Jumper E1 must connect pins 2 and 3, and Jumper E2 must connect pins 2 and 3.

Example: Standard configuration using the ULN2803A sinking (open-collector) output IC



Control-Panel Port I/O (JPAN Port)

The J2 or JPAN connector is a 26-pin connector with dedicated control inputs, dedicated indicator outputs, a quadrature encoder input, and an analog input. The control inputs are low true with internal pull-up resistors. They have predefined functions unless the control-panel-disable I-variable (I2) has been set to 1. If this is the case, they may be used as general-purpose inputs by assigning M-variable to their corresponding memory-map locations (bits of Y address $FFC0). There are five dedicated low-true outputs on the JPAN connector, usually used to light LEDs. They are BRLD/ (buffer-request LED), IPLD/ (in-position LED), EROR/ (Error condition LED), F1LD/ (1st -- warning -- following error LED), and F2LD/ (which goes true when the watchdog timer trips). If I2=0, they refer to the panel-selected coordinate system (by FDPn/). If I2=1, they refer to the host-selected coordinate system (&n). If I2=0 but no coordinate system is selected (all FPDn/ inputs are floating or pulled high), these lines can be used as general-purpose outputs, addressed as bits 20-23 of Y:$FFC2.

Thumbwheel Multiplexer Port (JTHW Port)

The Thumbwheel Multiplexer Port, or Multiplexer Port, on the JTHW (J3) connector has eight input lines and eight output lines. The output lines can be used to multiplex large numbers of inputs and outputs on the port, and Delta Tau provides accessory boards and software structures (special M-variable definitions) to capitalize on this feature. Up to 32 of the multiplexed I/O boards may be daisy-chained on the port in any combination.

The Acc-18 Thumbwheel Multiplexer board provides up to 16 BCD thumbwheel digits or 64 discrete TTL inputs per board. The TWD and TWB forms of M-variables are used for this board. The Acc-34x family Serial I/O Multiplexer boards provides 64 I/O point per board, optically isolated from PMAC. The TWS form of M-variables is used for these boards. The Acc-8D Option 7 Resolver-to-Digital Converter board provides up to 4 resolver channels whose absolute positions can be read through the thumbwheel port. The TWR form of M-variables is used for this board. The Acc-8D Option 9 Yaskawa™ Absolute Encoder Interface board can connect to up to four of these encoders. The absolute position is read serially through the multiplexer port on power up.

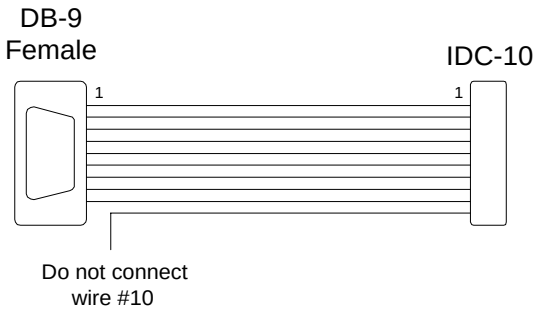
If none of these accessory boards is used, the inputs and outputs on this port may be used as discrete, non-multiplexed I/O. They map into PMAC's processor space at Y address $FFC1. The suggested M-variable definitions for this use are M40 to M47 for the eight outputs and M50 to M57 for the eight inputs. The ACC-27 Optically Isolated I/O board buffers the I/O in this non-multiplexed form, with each point rated to 24V and 100 mA.

Serial Connections

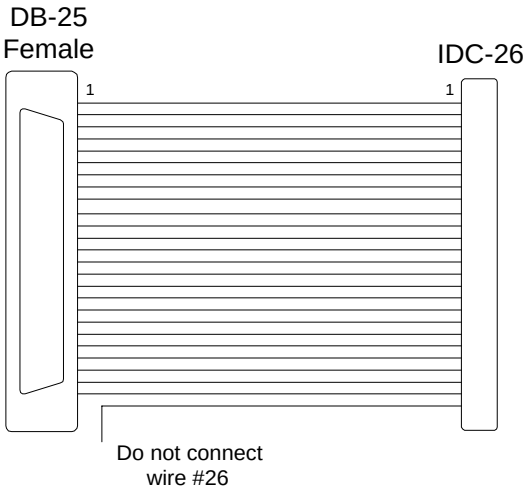
The PMAC Lite is provided with both RS232 and RS422 serial ports. To use the RS232 port on the 10-pin J4 connector jumpers E107 and E108 must connect pins 1 and 2. To use the RS422 port on the 26-pin J4A connector jumpers E107 and E108 must connect pins 2 and 3. Connectors J4 and J4A cannot be used at the same time.

Delta Tau provides cables for connecting PMAC with a host computer. Acc-3D connects J4A to a DB-25 connector; Acc-3L connects J4 to a DB-9 connector. Standard DB-9-to-DB-25 or DB-25-to-DB-9 adapters may be needed for a particular setup.

If a cable needs to be made, the easiest approach is to use a flat cable prepared with flat-cable type connectors as indicated in the following diagrams:

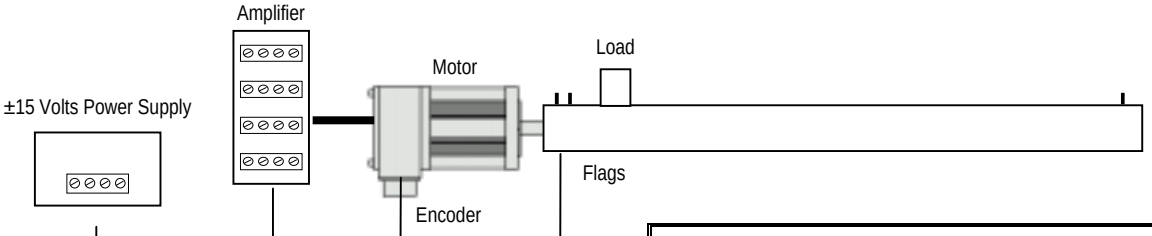


PMAC (IDC-10)	PC (DB-9)
1	1
2	6 (DSR)
3	2 (RXD)
4	7 (RTS)
5	3 (TXD)
6	8 (CTS)
7	4 (DTR)
8	9

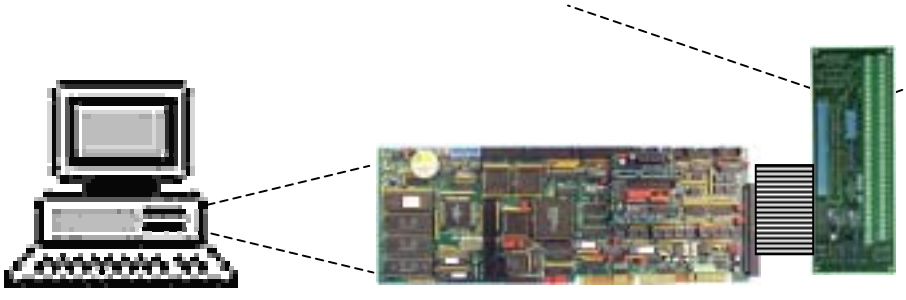


PMAC (IDC-26)	PC (DB-25)
1	1
2	14
3	2 (TXD)
4	15
5	3 (RXD)
6	16
7	4 (RTS)
8	17
9	5 (CTS)
10	18
11	6 (DSR)
12	19
13	7 (Gnd)
14	20 (DTR)
15	8
16	21
17	9
18	22
19	10
20	23
21	11
22	24
23	12
24	25
25	13
26	No connect

Machine Connections Example



ACC-8D or ACC-8P				
#1 Pin #	**#2 Pin #**	**#3 Pin #**	**#4 Pin #**	**SYMBOL**
53	54	39	40	-LIMn
55	56	41	42	HMFLn
51	52	37	38	+LIMn
58	58	58	58	AGND
1	2	1	2	+5V
3	4	3	4	GND
17	18	5	6	CHCn
19	20	7	8	CHCn/
21	22	9	10	CHBn
23	24	11	12	CHBn/
25	26	13	14	CHAn
27	28	15	16	CHAn/
43	44	29	30	DACn
45	46	31	32	DACn/
47	48	33	34	AENAn/DIRn
49	50	35	36	FAULTn
58	58	58	58	AGND
58				AGND
59				A+15V/OPT+V
60				A-15V



PMAC installed in a desktop PC

ACC-8D

For this configuration, jumpers E85, E87, E88, E89, and E90 are left at the default settings.

HOST PC-AT I/O ADDRESS MAP

Hex Range	Dec Range	Usage
000-01F	0-31	DMA Controller 1 8237A-5
020-03F	32-63	Interrupt Controller 1 8259A
040-05F	64-67	Timer 8254-2
060-06F	96-111	8042 (Keyboard)
070-07F	112-127	Real-time clock, NMI mask
080-09F	128-159	DMA Page Registers
0A0-0BF	160-191	Interrupt Controller 2 8259A
0C0-0DF	192-223	DMA Controller 2 8237A-5
0F0-0FF	240-255	Math CO processor
1F0-1F8	496-504	Fixed Disk
200-20F	512-527	Game Control
210-217	528-535	Expansion Unit (usually open)
278-27F	632-639	Parallel Printer: LPT2
2B0-2DF	688-735	Alternate EGA
2F8-2FF	760-767	Asynchronous Common: COM2
300-31F	768-799	Prototype Card (usually open)
360-36F	864-879	PC Network
378-37F	888-895	Parallel Printer: LPT1
380-38F	896-911	SDLC Communications 2
390-393	912-915	Cluster
3A0-3A9	928-937	SDLC Communications 1
3B0-3BF	944-959	IBM Monochrome Display/Printer
3C0-3CF	960-975	Enhanced Graphics Adapter
3D0-3DF	976-991	Color/Graphics
3F0-3F7	1000-1015	Diskette Controller
3F8-3FF	1016-1023	Asynchronous Common: COM1
x2E1		GPIB Adapter
x390-x393		Cluster Adapter

*__Note__: It is highly recommended that the addresses marked below with * not be used by PMAC PC. See above chart for possible contention with existing I/O. If a contention occurs, try a new unused address.

Contention is exhibited by:

1) Total Malfunction.
2) Partial Function, Input O.K., Output bad or vice versa.
3) Intermittent operation.

PMAC-LITE MATING CONNECTORS

This section lists several options for each connector. Choose an appropriate one for an application. (See attached PMAC mating connector sketch for typical connection.)

J1 (JDISP)/Display Port

1. Two 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0 T&B Ansley P/N 609-1441
2. 171-14 T&B Ansley standard flat cable stranded 14-wire
3. Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1

J2 (JPAN)/Control Panel Port

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
2. 171.26.T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J3 (JTHW)/Multiplexer Port

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J4 (JRS232)/RS232 Serial Communications

1. Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0 T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J4A (JRS422)/RS422 Serial Communications

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J5 (JOPT)/General Purpose I/O

1. Two 34-pin female flat cable connector Delta Tau P/N 014-R00F34-0k0 T&B Ansley P/N 609-3441
2. 171-34 T&B Ansley standard flat cable stranded 34-wire
3. Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J6 (JXIO)/Auxiliary Port

1. Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0 T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J7 (JS1)/A-D Inputs

1. Two 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0 T&B Ansley P/N 609-1641
2. 171-16 T&B Ansley standard flat cable stranded 16-wire
3. Phoenix varioface module type FLKM 16 (male pins) P/N 22 81 03 4

J8 (JEQU)/Position Compare

1. Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0 T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J9 (JEXP)/Expansion Port

1. Two 50-pin female flat cable connector Delta Tau P/N 014-R00F50-0K0 T&B Ansley P/N 609-5041
2. 171-50 T&B Ansley standard flat cable stranded 50-wire
3. Phoenix varioface module type FLKM 50 (male pins) P/N 22 81 08 9 used for daisy chaining Acc-14 I/0, -23 A and D connectors -24 expansion

J11 (JMACH1)/1st Machine Connector

1. Two 60-pin female flat cable connector Delta Tau P/N 014-R00F60-0K0 T&B Ansley P/N 609-6041 available as Acc 8P or 8D
2. 171-60 T&B Ansley standard flat cable stranded 60-wire
3. Phoenix varioface module type FLKM 60 (male pins) P/N 22 81 09 2

Note

Normally, J11 is used with accessory 8P or 8D with Option P, which provides complete terminal strip fan-out of all connections.

P1 (PC Bus)

One 62-pin card edge connector with solder pierced eyelets Delta Tau P/N 014-000F62-SCO Viking P/N 3KH 31/9 JN12 card edge connector. Pierced solder eyelets.

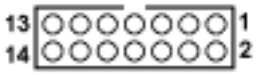
P2 (AT Bus)

One 36-pin card edge connector with solder pierced eyelets Delta Tau P/N 014-000 F36-SCO Viking P/N 3KH 18/9 JN12 card edge connector. Pierced solder eyelets.

PMAC LITE CONNECTOR PINOUTS

J1 (JDISP): Display Port Connector

(14-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	VDD	Output	+5V Power	Power supply out
2	VSS	Common	PMAC Common	
3	RS	Output	Read Strobe	TTL signal out
4	VEE	Output	Contrast Adjust VEE	0 to +5Vdc *
5	E	Output	Display Enable	High is enable
6	R/W	Output	Read or Write	TTL signal out
7	DB1	Output	Display Data1	
8	DB0	Output	Display Data0	
9	DB3	Output	Display Data3	
10	DB2	Output	Display Data2	
11	DB5	Output	Display Data5	
12	DB4	Output	Display Data4	
13	DB7	Output	Display Data7	
14	DB6	Output	Display Data6	

***** Controlled by potentiometer R1

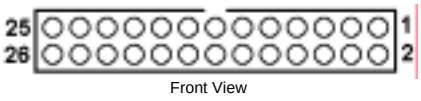
The JDISP connector is used to drive the 2-line x 24-character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (Acc 12C) display unit. The **DISPLAY** command may be used to send messages and values to the display.

See Also:

Program Commands: Display
Accessories; ACC-12, 12A, 12C, ACC16D
Memory Map: Y:$0780 - $07D1

J2 (JPAN): Control Panel Port Connector

(26-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	+5V	Output	+5V Power	For remote panel
2	GND	Common	PMAC Common	
3	FPD0/	Input	Motor/C.S. Select Bit 0	Low is True
4	JOG-/	Input	Jog IN - DIR.	Low is JOG -
5	FPD1/	Input	Motor/C.S. Select 1	Low is Low is
6	JOG+/	Input	Jog IN + DIR.	Low is JOG +
7	PREJ/	Input	Return to Prejog Position	Low is Return Equivalent to J= CMD
8	STRT/	Input	Start Program Run	Low is Start Equivalent to R CMD
9	STEP/	Input	Step Through Program	Low is Step Equivalent to S or Q
10	STOP/	Input	Stop Program Run	Low is Stop Equivalent to A
11	HOME/	Input	Home Search Command	Low is Go Home Equivalent to HM
12	HOLD/	Input	Hold Motor	Low is Hold Equivalent to H
13	FPD2/	Input	Motor/C.S. Select 2	Low is True
14	FPD3/	Input	Motor/C.S. Select 3	Low is True
15	INIT/	Input	Reset PMAC	Low is Reset Equivalent to $$$
16	HWCA	Input	Handwheel Encoder A Channel	5V TTL SQ. pulse Must use E23 (CHA2)
17	IPLD/	Output	In Position Ind. (C.S.)	Low lights LED
18	BRLD/	Output	Buffer Request Ind.	Low lights LED
19	ERLD/	Output	Fatal Follow Err (C.S.)	Low lights LED
20	WIPER	Input	Feed Pot Wiper	0 TO +10V input. Must use E72, E73 (CHA4)
21	(SPARE)	N.C.		
22	HWCB	Input	Handwheel Encoder B Channel	5V TTL SQ. pulse. Must use E22 (CHB2)
23	F1LD/	Output	Warn Follow Err (C.S.)	Low Lights LED
24	F2LD/	Output	Watchdog Timer	Low Lights LED
25	+5V	Output	+5V Power	For remote panel
26	GND	Common	PMAC Common	

The JPAN connector can be used to connect the Acc-16 (Control Panel), or customer-provided I/O, to the PMAC, providing manual control of PMAC functions via simple toggle switches. If the automatic control panel input functions are disabled (I2=1), the inputs become general-purpose TTL inputs, and the coordinate system (C.S.) specific outputs pertain to the *host*-addressed coordinate system.

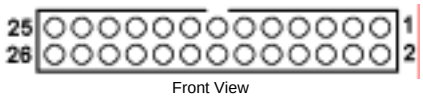
See Also:

Control panel inputs, Accessories: Acc-16, Acc-39

I-variables: I2, Ixx06

J3 (JTHW): Multiplexer Port Connector

(26-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Input	Data-0 Input	Data input from multiplexed accessory
4	SEL0	Output	Select-0 Output	Multiplexer select output
5	DAT1	Input	Data -1 Input	Data input from multiplexed accessory
6	SEL1	Output	Select -1 Output	Multiplexer select output
7	DAT2	Input	Data -2 Input	Data input from multiplexed accessory
8	SEL2	Output	Select -2 Output	Multiplexer select output
9	DAT3	Input	Data -3 Input	Data input from multiplexed accessory
10	SEL3	Output	Select -3 Output	Multiplexer select output
11	DAT4	Input	Data -4 Input	Data input from multiplexed accessory
12	SEL4	Output	Select -4 Output	Multiplexer select output
13	DAT5	Input	Data -5 Input	Data input from multiplexed accessory
14	SEL5	Output	Select -5 Output	Multiplexer select output
15	DAT6	Input	Data -6 Input	Data input from multiplexed accessory
16	SEL6	Output	Select -6 Output	Multiplexer select output
17	DAT7	Input	Data -7 Input	Data input from multiplexed accessory
18	SEL7	Output	Select -7 Output	Multiplexer select output
19	N.C.	N.C.	No Connection	
20	GND	Common	PMAC Common	
21	BRLD/	Output	Buffer Request	Low is Buffer Request
22	GND	Common	PMAC Common	
23	IPLD/	Output	In Position	Low is In Position
24	GND	Common	PMAC Common	
25	+5V	Output	+5Vdc Supply	Power supply out
26	INIT/	Input	PMAC Reset	Low is "Reset"

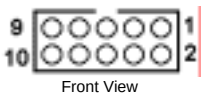
The JTHW multiplexer port provides 8 inputs and 8 outputs at TTL levels. While these I/O can be used in un-multiplexed form for 16 discrete I/O points, most users will utilize PMAC software and accessories to use this port in multiplexed form to greatly multiply the number of I/O that can be accessed on this port. In multiplexed form, some of the SELn outputs are used to select which of the multiplexed I/O are to be accessed.

See also:

I/O and Memory Map Y:$FFC1
Suggested M-variables M40 - M58
M-variable formats TWB, TWD, TWR, and TWS
Acc-8d Opt 7, Acc-8d Opt 9, Acc-18, Acc-34x, NC Control Panel

J4 (JRS232) Serial Port Connector

(10-Port Connector)



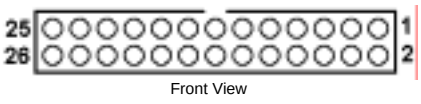
Front View

Pin #	Symbol	Function	Description	Notes
1	PHASE	Output	Phasing Clock	
2	DTR	Bidirectional	Data Terminal Ready	Tied to DSR
3	TXD/	Input	Receive Data	Host transmit data
4	CTS	Input	Clear to Send	Host ready bit
5	RXD/	Output	Send Data	Host receive data
6	RTS	Output	Request to Send	PMAC ready bit
7	DSR	Bidirectional	Data Set Ready	Tied to DTR
8	SERVO	Output	Servo Clock	
9	GND	Common	PMAC Common	
10	+5V	Output	+5Vdc Supply	Power supply out

The JRS232 connector provides the PMAC2 PC with the ability to communicate serially with an RS232 port. E107 and E108 must connect pins 1 and 2 to use this connector. This connector cannot be used for daisy chain interconnection of multiple PMACs – the J4A RS422 connector must be used for daisy chaining.

J4A (JRS422): Serial Port Connector

(26-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	CHASSI	Common	PMAC Common	
2	S+5V	Output	+5Vdc Supply	Deactivated by E8
3	RD-	Input	Receive Data	Diff. I/O low True **
4	RD+	Input	Receive Data	Diff. I/O high True *
5	SD-	Output	Send Data	Diff. I/O low True **
6	SD+	Output	Send Data	Diff. I/O high True *
7	CS+	Input	Clear to Send	Diff. I/O high True **
8	CS-	Input	Clear to Send	Diff. I/O low True *
9	RS+	Output	Request to Send	Diff. I/O high True **
10	RS-	Output	Request to Send	Diff. I/O low True *
11	DTR	Bidirectional	Data Terminal Ready	Tied to DSR
12	INIT/	Input	PMAC Reset	Low is Reset
13	GND	Common	PMAC Common	**
14	DSR	Bidirectional	Data Set Ready	Tied to DTR
15	SDIO-	Bidirectional	Special Data	Diff. I/O low True
16	SDIO+	Bidirectional	Special Data	Diff. I/O high True
17	SCIO-	Bidirectional	Special CTRL.	Diff. I/O low True
18	SCIO+	Bidirectional	Special CTRL.	Diff. I/O high True
19	SCK-	Bidirectional	Special Clock	Diff. I/O low True
20	SCK+	Bidirectional	Special Clock	Diff. I/O high True
21	SERVO-	Bidirectional	Servo Clock	Diff. I/O low True ***
22	SERVO+	Bidirectional	Servo Clock	Diff. I/O high True ***
23	PHASE-	Bidirectional	Phase Clock	Diff. I/O low True ***
24	PHASE+	Bidirectional	Phase Clock	Diff. I/O high True ***
25	GND	Common	PMAC Common	
26	+5V	Output	+5Vdc Supply	Power supply out

The JRS422 connector provides the PMAC with the ability to communicate both in RS422 and RS232. In addition, this connector is used to daisy chain interconnect multiple PMACs for synchronized operation. Jumpers E107 and E108 must connect pins 2 and 3 to use this port.

* **Note:** Required for communications to an RS-422 host port

** **Note:** Required for communications to an RS-422 or RS-232 host port

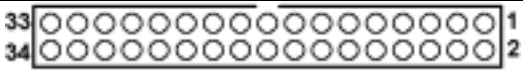
*** **Note:** Output on card @0; input on other cards. These pins are for synchronizing multiple PMACs together by sharing their phasing and servo clocks. The PMAC designated as card 0 (@0) by its jumpers E40-E43 outputs its clock signals. Other PMACs designated as cards 1-15 (@1-@F) by their jumpers E40-E43 take these signals as inputs. If synchronization is desired, these lines should be connected even if serial communications is not used.

See Also:

Serial Communications
Synchronizing PMAC to other PMACs

J5 (JOPTO): I/O Port Connector

(34-Pin Connector)

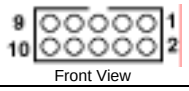


Front View

Pin #	Symbol	Function	Description	Notes
1	MI8	Input	Machine Input 8	Low is True
2	GND	Common	PMAC Common	
3	MI7	Input	Machine Input 7	Low is True
4	GND	Common	PMAC Common	
5	MI6	Input	Machine Input 6	Low is True
6	GND	Common	PMAC Common	
7	MI5	Input	Machine Input 5	Low is True
8	GND	Common	PMAC Common	
9	MI4	Input	Machine Input 4	Low is True
10	GND	Common	PMAC Common	
11	MI3	Input	Machine Input 3	Low is True
12	GND	Common	PMAC Common	
13	MI2	Input	Machine Input 2	Low is True
14	GND	Common	PMAC Common	
15	MI1	Input	Machine Input 1	Low is True
16	GND	Common	PMAC Common	
17	MO8	Output	Machine Output 8	Low- True (sinking); High- True (sourcing)
18	GND	Common	PMAC Common	
19	MO7	Output	Machine Output 7	" "
20	GND	Common	PMAC Common	
21	MO6	Output	Machine Output 6	" "
22	GND	Common	PMAC Common	
23	MO5	Output	Machine Output 5	" "
24	GND	Common	PMAC Common	
25	MO4	Output	Machine Output 4	" "
26	GND	Common	PMAC Common	
27	MO3	Output	Machine Output 3	" "
28	GND	Common	PMAC Common	
29	MO2	Output	Machine Output 2	" "
30	GND	Common	PMAC Common	
31	MO1	Output	Machine Output 1	" "
32	GND	Common	PMAC Common	
33	+V	Input/Output	+V Power I/O	+V = +5V to +24V +5V out from PMAC, +5 to +24V in from external source, diode isolation from PMAC
34	GND	Common	PMAC Common	

This connector provides means for eight general-purpose inputs and eight general-purpose outputs. Inputs and outputs may be configured to accept or provide either +5V or +24V signals. Outputs can be made sourcing with an IC (U11 to UDN2981) and jumper (E1 and E2) change. E7 controls whether the inputs are pulled up or down internally. Outputs are rated at 100mA per channel.

J6 (JXIO): Auxiliary I/O Port Connector
(10-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	CHA1	Input	Encoder A Ch. Pos.	From Acc-14 board
2	CHB1	Input	Encoder B Ch. Pos.	From Acc-14 board
3	CHC1	Input	Encoder C Ch. Pos.	From Acc-14 board
4	CHA3	Input	Encoder A Ch. Pos.	From Acc-14 board
5	CHB3	Input	Encoder B Ch. Pos.	From Acc-14 board
6	CHC3	Input	Encoder C Ch. Pos.	From Acc-14 board
7	E63	Input	Interrupt IR4	From Acc-14 board
8	E59	Input	Interrupt IR5	From Acc-14 board
9	SCLK	Output	Encoder Clock	To Acc-24, Acc-8D OPT 8 boards
10	DCLK	Output	D to A, A to D Clock	To Acc-24 board
This connector is used for miscellaneous I/O functions related to expansion cards that are used with PMAC.				

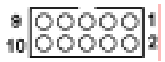
J7 (JS1): A/D Port Connector
(16-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for Channel 1, 2, 3, 4
2	BDATA1	Output	D to A Data	DAC data for Channel 1, 2, 3, 4
3	ASEL0/	Output	Chan. Select bit 0	Select for Channel 1, 2, 3, 4
4	ASEL1/	Output	Chan. Select 1	Select for Channel 1, 2, 3, 4
5	CNVRT01	Output	A to D Convert	ADC convert signal Channel 1, 2, 3, 4
6	ADCIN1	Input	A to D Data	ADC data for Channel 1, 2, 3, 4
7	OUT1/	Output	Amplifier Enable/Dir	Amp enable/dir for Channel 1
8	OUT2/	Output	Amplifier Enable/Dir	Amp enable/dir for Channel 2
9	OUT3/	Output	Amplifier Enable/Dir	Amp enable/dir for Channel 3
10	OUT4/	Output	Amplifier Enable/Dir	Amp enable/dir for Channel 4
11	HF41	Input	Amplifier Fault	Amp fault input for Channel 1
12	HF42	Input	Amplifier Fault	Amp fault input for Channel 2
13	HF43	Input	Amplifier Fault	Amp fault input for Channel 3
14	HF44	Input	Amplifier Fault	Amp fault input for Channel 4
15	+5V	Output	+5V Supply	Power supply out
16	GND	Common	PMAC Common	
Acc-28A/B connection; digital amplifier connection.				

J8 (JEQU): Position-Compare Connector
(10-Pin Connector)

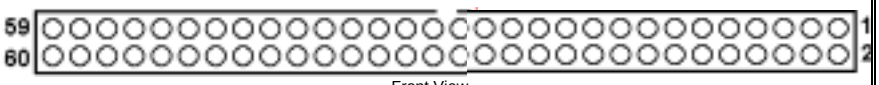


Front View

Pin #	Symbol	Function	Description	Notes
1	EQU1/	Output	Encoder 1 Comp-Eq	Low is True
2	EQU2/	Output	Encoder 2 Comp - Eq	Low is True
3	EQU3/	Output	Encoder 3 Comp - Eq	Low is True
4	EQU4/	Output	Encoder 4 Comp - Eq	Low is True
5	AENA1/	Output	Amplifier Enable 1	Low is True
6	AENA2/	Output	Amplifier Enable 2	Low is True
7	AENA3/	Output	Amplifier Enable 3	Low is True
8	AENA4/	Output	Amplifier Enable 4	Low is True
9	A+V	Supply	Positive Supply	+5V to +24V
10	AGND	Common	Analog Ground	

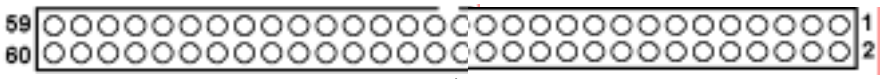
This connector provides the position-compare outputs and the amplifier enable outputs for the four servo interface channels. The board is shipped by default with a ULN2803A or equivalent open-collector driver IC. It may be replaced with UDN2891A or equivalent open-emitter driver (E11 and E12 must be changed.), or a 74ACT563 or equivalent 5V CMOS driver.

J11 (JMACH1): Machine Port Connector
(60-Pin Header)



Front View

Pin #	Symbol	Function	Description	Notes
1	+5V	Output	+5V Power	For encoders, 1
2	+5V	Output	+5V Power	For encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC3	Input	Encoder C Ch. Pos.	2
6	CHC4	Input	Encoder C Ch. Pos.	2
7	CHC3/	Input	Encoder C Ch. Neg.	2,3
8	CHC4/	Input	Encoder C Ch. Neg.	2,3
9	CHB3	Input	Encoder B Ch. Pos.	2
10	CHB4	Input	Encoder B Ch. Pos.	2
11	CHB3/	Input	Encoder B Ch. Neg.	2,3
12	CHB4/	Input	Encoder B Ch. Neg.	2,3
13	CHA3	Input	Encoder A Ch. Pos.	2
14	CHA4	Input	Encoder A Ch. Pos.	2
15	CHA3/	Input	Encoder A Ch. Neg.	2,3
16	CHA4/	Input	Encoder A Ch. Neg.	2,3
17	CHC1	Input	Encoder C Ch. Pos.	2
18	CHC2	Input	Encoder C Ch. Pos.	2
19	CHC1/	Input	Encoder C Ch. Neg.	2,3
20	CHC2/	Input	Encoder C Ch. Neg.	2,3
21	CHB1	Input	Encoder B Ch. Pos.	2
22	CHB2	Input	Encoder B Ch. Pos.	2
23	CHB1/	Input	Encoder B Ch. Neg.	2,3
24	CHB2/	Input	Encoder B Ch. Neg.	2,3
25	CHA1	Input	Encoder A Ch. Pos.	2
26	CHA2	Input	Encoder A Ch. Pos.	2
27	CHA1/	Input	Encoder A Ch. Neg.	2,3
28	CHA2/	Input	Encoder A Ch. Neg.	2,3
29	DAC3	Output	Analog Out Pos.. 3	4

J11 JMACH1 60-Pin Header (Continued)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
30	DAC4	Output	Analog Out Pos.. 4	4
31	DAC3/	Output	Analog Out Neg.. 3	4,5
32	DAC4/	Output	Analog Out Neg.. 4	4,5
33	AENA3/DIR3	Output	Amp-Ena/Dir. 3	6
34	AENA4/DIR4	Output	Amp-Ena/Dir. 4	6
35	FAULT3	Input	Amp-Fault 3	7
36	FAULT4	Input	Amp-Fault 4	7
37	+LIM3	Input	Neg. End Limit 3	8,9
38	+LIM4	Input	Neg. End Limit 4	8,9
39	-LIM3	Input	Pos. End Limit 3	8,9
49	FAULT1	Input	Amp. Fault 1	7
50	FAULT2	Input	Amp. Fault 2	7
51	+LIM1	Input	Neg. End Limit 1	8,9
52	+LIM2	Input	Neg. End Limit 2	8,9
53	-LIM1	Input	Pos. End Limit 1	8,9
54	-LIM2	Input	Pos. End Limit 2	8,9
55	HMFL1	Input	Home-Flag 1	10
56	HMFL2	Input	Home-Flag 2	10
57	FEFCO/	Output	FE/Watchdog Out	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15V Supply	
60	A-15V	Input	Analog -15V Supply	

The J8 connector is used to connect PMAC to the first 4 channels (Channels 1, 2, 3, and 4) of servo amps, flags, and encoders.

Note 1: In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on your version of PMAC, it is preferable to bring the +5V power in through the terminal block.

Note 2: Referenced to digital common (GND). Maximum of + 12V permitted between this signal and its complement.

Note 3: Leave this input floating if not used (i.e. digital single-ended encoders). In this case, jumper (E18 - 21, E24 - 27) for channel should hold input at 2.5V.

Note 4: + 10V, 10mA max, referenced to analog common (AGND).

Note 5: Leave floating if not used; do not tie to AGND. In this case AGND is the return line.

Note 6: Functional polarity controlled by jumper(s) E17. Choice between AENA and DIR use controlled by Ix02 and Ix25.

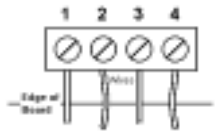
Note 7: Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software. Automatic fault function can be disabled with Ix25.

Note 8: Pins marked *-LIMn* should be connected to switches at the *positive* end of travel. Pins marked *+LIMn* should be connected to switches at the *negative* end of travel.

Note 9: Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

Note 10: Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software.

TB1 (JPWR): Power Supply
(4-Pin Terminal Block)



Top View

Pin #	Symbol	Function	Description	Notes
1	GND	Common	Reference Voltage	
2	+5V	Input	Positive Supply Voltage	Supplies all PMAC digital circuits
3	+12V	Input	Positive Supply Voltage	Ref to digital GND
4	-12V	Input	Negative Supply Voltage	Ref to Digital GND

This terminal block can be used to provide the input for the power supply for the circuits on the PMAC board when it is not in a bus configuration. When the PMAC Lite is in a bus configuration, these supplies automatically come through the bus connector from the bus power supply; in this case, this terminal block should not be used.

To keep the optical isolation between the digital and analog circuits on PMAC, provide analog power (+/-12V to +/-15V and AGND) through the JMACH connector, instead of the bus connector or this terminal block.

PMAC-PC SOFTWARE SETUP

PMAC has a large set of Initialization parameters (I-variables) that determine the personality of the card for a specific application. Many of these are used to configure a motor properly. Once set up, these variables may be stored in non-volatile EAROM memory (using the **SAVE** command) so the card is always configured properly (PMAC loads the EAROM I-variable values into RAM on power-up).

The easiest way to program, setup and troubleshoot PMAC is by using the PMAC Executive Program PEWIN and its related add-on packages P1Setup and PMACPlot. These software packages are available from Delta Tau, ordered through the Acc-9WN accessory.
The programming features and configuration variables for the PMAC PC are fully described in the PMAC User and Software manuals.

Configuring PMAC with Option-5C for 80 MHz Operation

On the PMAC Lite 1.5 (a board with flash-backed main memory), jumper E48 controls the frequency of operation of the DSP. It can only directly set 40 MHz and 60 MHz DSP operation. On power-up/reset, the DSP, operating at the crystal frequency of 20 MHz, reads the frequency jumper E48 and writes into its own PLL multiplier register at X:$FFFD. Bits 0-3 of this word contain a value one less than the multiplier value (if the frequency is being multiplied by 3, these bits contain a value of 2).

To check the value of the multiplier, use the on-line command **RHX:$FFFD** and look at the last hexadecimal digit. The actual multiplier is one greater than the value in this last digit. Alternately, an M-variable such as M99->X:$FFFD,0,4 can be defined and then read from or write to these bits with the M-variable.

E48	X:$FFFD; 0-3	True Multiplier	DSP Frequency
OFF	1	x2	40 MHz
ON	2	x3	60 MHz

When PMAC is ordered with the CPU Option 5C it is capable to run at 80 MHz frequency. To operate the CPU at 80 MHz, set the multiplier value in user software. In this case, usually E48 will be set to OFF, so the CPU comes up at 40 MHz. The usual way to set the multiplier value for 80 MHz is to use a reset PLC, one that executes automatically on power-up/reset, then disables itself. Typically, this is PLC 1, the first to execute after power-up/reset (see below).

If using serial communications on an 80 MHz PMAC(1), also change the baud rate divider register in the CPU. On power-up/reset, the firmware reads jumpers E44-E47 and sets the baud rate divider register in the CPU (at X:$FFF2 bits 0 to 11) to set the serial baud rate. Since the baud rate clock is derived from the CPU frequency, a change in the CPU frequency will change the baud rate.

To counteract this change, when the CPU frequency is changed, change the baud rate divider register in the CPU. If the CPU frequency is doubled, also double the divider value and add 1. This should also be done in the reset PLC.

This operation can be done with the following code segment. This baud divider algorithm is valid only if the PMAC has been jumpered for 40-MHz operation (E48 OFF).

```
M98->X:$FFF2,0,12
M99->X:$FFFD,0,4
OPEN PLC 1 CLEAR
M99=3                          ; Set x4 frequency multiplication (80 MHz)
M98=2*M98+1                    ; Increase baud divider to maintain rate
                               ; (Only needed for serial communications)
...                            ; More of reset PLC
DISABLE PLC 1                  ; So PLC 1 will not repeat
CLOSE
```

To make the change in CPU frequency and baud rate over the serial port with on-line commands, make sure that the two commands are on the same command line. If they are on separate command lines, the second command will not be accepted because the baud rate has changed. For example, with the same setup as the above example, use the command line

```
M99=3 M98=2*M98+1
```

to change the CPU frequency and baud rate divider (to keep the baud rate constant) together.

Option 16 Supplemental Memory

If the Option 16 supplemental battery-backed parameter memory is ordered, an extra bank of memory with battery backup circuitry is provided. This option can only be ordered if the main memory is flash backed (Option 4A, 5A, 5B, or 5C). This memory is for user parameter storage only. From PMAC programs, it can be accessed with M-variables only (L-variables also in compiled PLCs). The on-line direct-memory read and write commands can be used from the host computer as well.

With M-variable access, arrays can be created with indirect addressing techniques by pointing a second M-variable to the definition of a first M-variable that points into this memory area. For example, with the M-variable definitions:

```
M0->L:$A000                    ; 1st long word of Opt. 16 RAM; floating point
M10->Y:$BC000,0,16             ; Low 16 bits of M0 def., with pointer address
```

the following code segment could load a sine table into the first 360 words of the Option 16 RAM:

```
P1=0
WHILE (P1<360)
  M10=$A000+P1                 ; Sets address that M0 points to
  M0=SIN(P1)                   ; Puts value in register that M0 points to
  P1=P1+1
ENDWHILE
```

Note that this technique is not possible with L-variables in compiled PLCs (but it is possible with M-variables in compiled PLCs).

Physically, the Option 16 memory is a 16k x 24 bank of battery-backed static RAM. It maps into the PMAC and PMAC2 at addresses $A000 to $BFFF, on both the X and Y data buses, an 8k x 48 block of address space. Addresses Y:$BC00 to Y:$BFFF are double mapped with the main flash-backed RAM for the M-variable definitions, and should not be used for user parameter storage.

Any value written into the Option 16 memory will be retained automatically through a power-down or reset; no **SAVE** operation is required. Typically, the power draw on the battery is low enough that battery life will be limited only by the quoted 10-year life of the battery.

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