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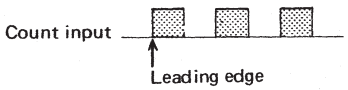
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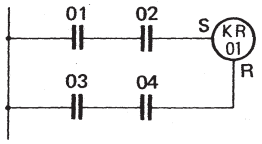
- At the leading edge (i.e., from OFF to ON) of a count input signal, the counter decrements the count value by 1.



- When both a count input and a reset input are applied simultaneously, the reset input takes precedence over the count input. The counter performs counting operation again after the reset input is removed.
- **The present value of the counter is retained in memory during a power failure**
  If a power failure occurs, the counter is not reset and the present value (i.e., count remaining) of the counter is retained in the memory.
  Accordingly, to reset the count value of the counter when power is applied, use the contact of special auxiliary relay MR59 to generate a reset input. (Refer to paragraph 5.2.4, Applied Programs.)

■ LATCHING RELAY (KR) INSTRUCTION

The KR instruction can be used as a latching relay in the same manner as a relay circuit.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND		02
002	LD		03
003	AND		04
004	OUT*	KR/3	01

Contents of Registers

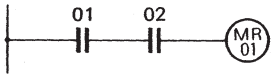
R	S
01	—
01 02	—
03	01 02
03 04	01 02
03 04	01 02

NOTE: * A latching relay program must be entered in the order of a set input circuit, a reset input circuit and a latching relay coil. Use the OUT instruction to program a latching relay coil.

- **Operation of each register**
  The latching relay operates when the content of the R register is logical 0 and the content of the S register is logical 1. The relay releases when the content of the R register is logical 1.
- When both a set input and a reset input are applied simultaneously, the reset input takes precedence over the set input.
- The content of the latching relay is retained in the memory during a power failure. It continues to be retained until application of a reset input.

■ INTERNAL AUXILIARY (MR) INSTRUCTION

This instruction is used when an internal auxiliary relay is employed.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND		02
002	OUT*	MR/2	01

Contents of Registers

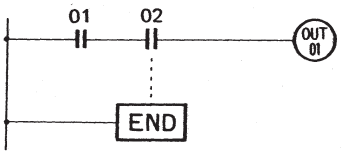
R	S
01	—
01 02	—
01 02	—

NOTE: * The OUT instruction is used to program an internal auxiliary relay coil.

- Internal auxiliary relays have no relation whatsoever to input/output relays. However, the internal auxiliary relay contacts cannot be used as external outputs.
- The number of contacts is not limited for use.

■ END INSTRUCTION

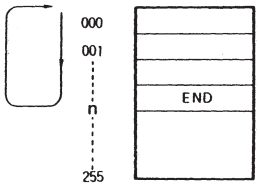
Insert this instruction at the end of a program.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND		02
002	OUT		01
003			
004			
⋮	⋮	⋮	⋮
n	END		

- The program memory of the SYSMAC-P0R is provided with addresses 000 to 255. The CPU scans program data from address 000 to address with an END instruction according to the ladder diagram.



- When performing a test run, insert an END instruction at each end of a sequence circuit and then delete the END instruction after confirming each circuit. In this manner, the test run can be executed smoothly.
- When the mode selector switch is set to the RUN mode without an END instruction being inserted at the end of a program, the RUN indicator illuminates. In this case, however, error message " ☒ " appears in the Sub OP code display, and the program cannot be executed.

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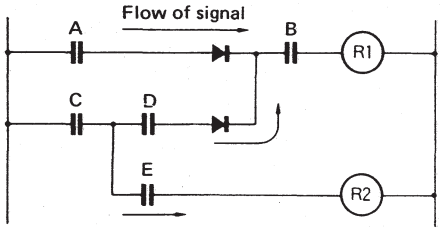
5. Programming

5.1 How to Program

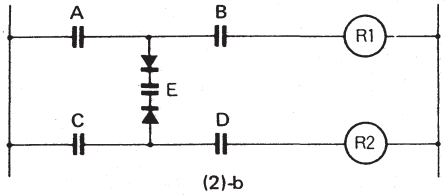
With the SYSMAC-P0R, a ladder circuit is controlled according to the sequence of the instructions stored in the CPU memory. Therefore, it is neccessary to observe the hints on correct programming and programming order.

5.1.1 Hints on correct programming

1. Since the number of contacts is not limited for input/output relays, internal auxiliary relays, timers, etc., it can be said that the best way to design a ladder circuit is to configure a simple, clear circuit, rather than a complicated circuit created by reducing the number of contacts.
2. In the SYSMAC-P0R, signals will flow from the left to the right. In other words, signals will flow as if diodes are inserted in the circuit as shown in (2)-a or (2)-b. To operate a circuit without diodes in the same manner as the circuit configured with general control relays, it is necessary to rewrite the circuit.

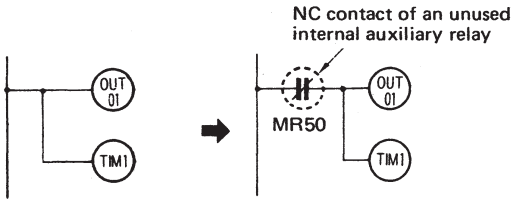


(2)-a

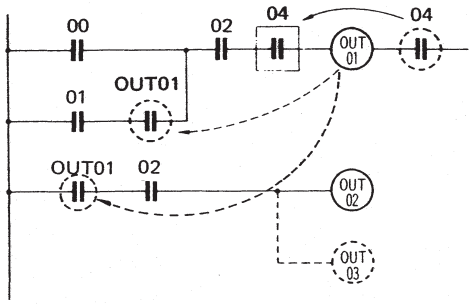


(2)-b

3. In a series-parallel circuit, the number of contacts that can be connected in series is not limited, as well as the number of contacts that can be connected in parallel.
4. No output relay can be connected directly from the bus bar. If necessary, connect it through the NC contact of an unused internal auxiliary relay.



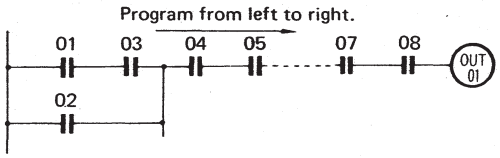
5. All output relays are provided with auxiliary contacts that can be used on a circuit, in addition to the output signal contacts to drive loads actually. The number of contacts that can be used per output relay is not limited.



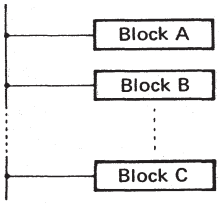
6. No relay contact can be inserted next to an output coil. If necessary, insert it before the output coil.
7. Two or more output coils can be connected in parallel. In this case, however, note that a circuit error message will appear in the display.
8. For contact and coil numbers on the circuit, use the I/O relay numbers described in Chapter 3.
9. Output coil numbers (including those for timers and counters) cannot be used in duplication.

5.1.2 Programming order

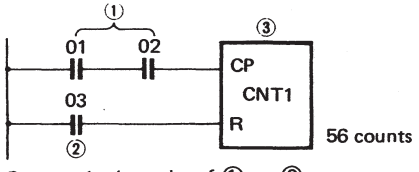
1. Program a circuit from its left to right.



2. Assume the circuit elements located from the bus bar to an output relay as one block. If a number of blocks are in line, programming can be started from any block. However, pay attention in case of circuits utilizing scan time or timing such as differentiator, shift register, etc.



3. When composite instructions such as counter, latching relay, etc. are used, their order of programming is predetermined. Be sure to perform the programming according to the predetermined order.



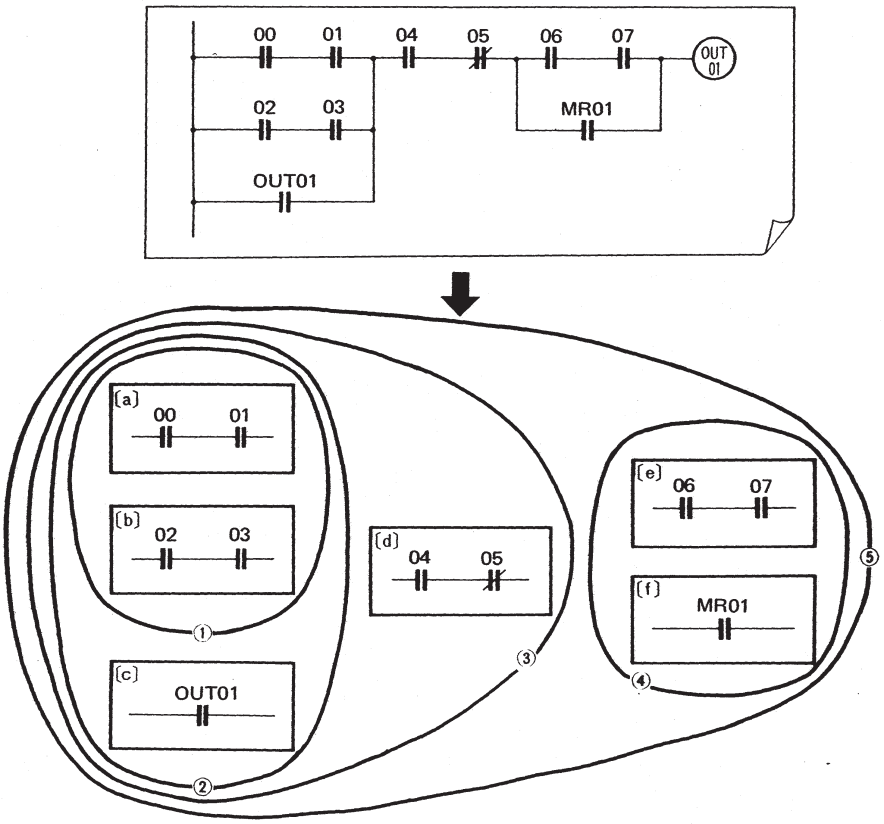
Program in the order of ① → ③.

⋮	⋮		⋮
n	LD		01
n + 1	AND		02
n + 2	LD		03
n + 3	CNT	1	56
⋮	⋮	⋮	⋮

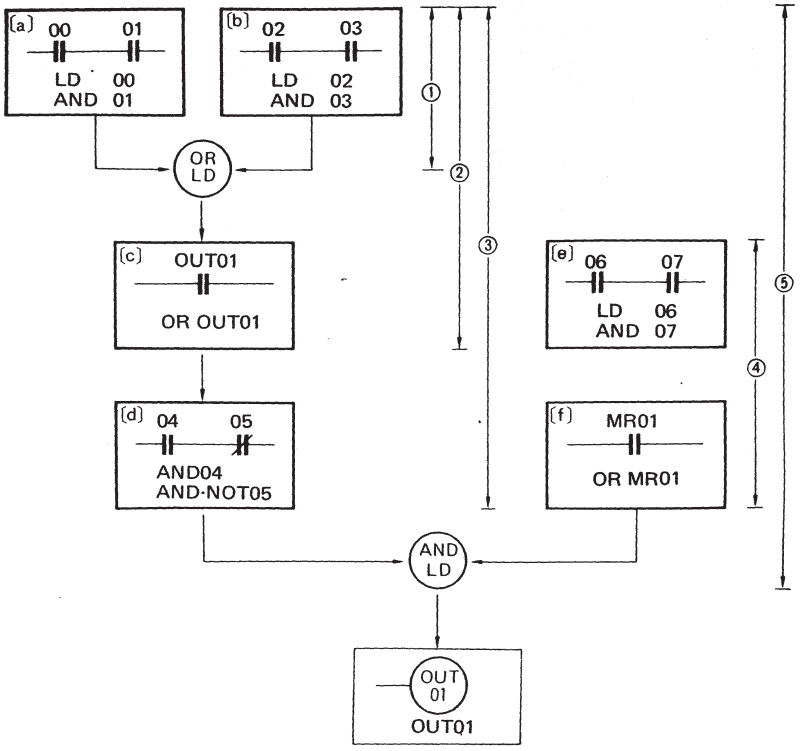
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4. Be sure to insert an END instruction at the end of each program.
5. A ladder diagram such as the one shown below can be divided into small blocks as shown below, to program each block in the order of ① to ⑤. Eventually, the circuit will be programmed as one large block such as ⑤.

- **Ladder diagram**



- **Programming procedure**

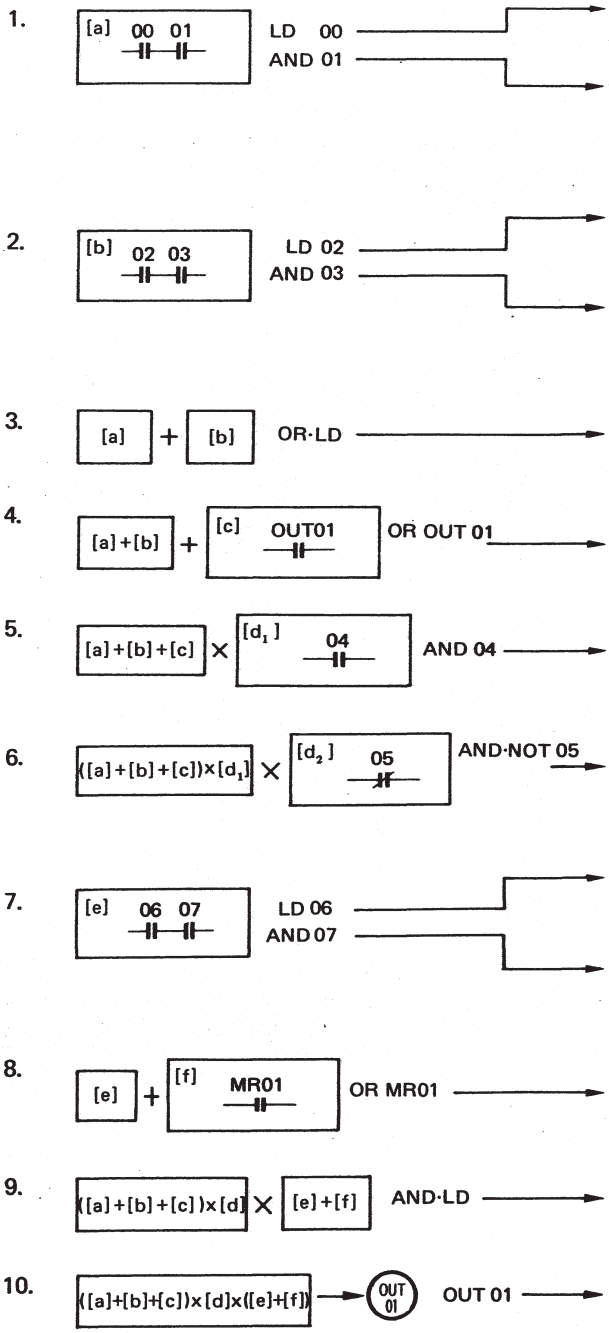


- **Coding**

Address	OP	Sub OP	Data
000	LD		00
001	AND		01
002	LD		02
003	AND		03
004	OR·LD		
005	OR	OUT/1	01
006	AND		04
007	AND·NOT		05
008	LD		06
009	AND		07
010	OR	MR/2	01
011	AND·LD		
012	OUT		01
⋮	⋮		⋮
n	END		

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● Operations of R and S registers



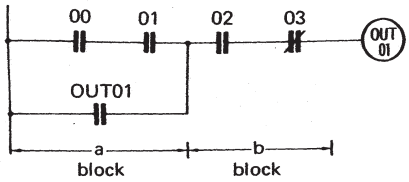
Content of register	R register	S register
The content ("1" or "0") of 00 is stored in R register.	00	Vacant
The content of R register is ANDed with the content of 01 and the result of operation is stored in R register.	Result of 00 01 = [a]	Vacant
The previous content of R register is transferred to S register and the content of 02 is newly stored in R register.	02	[a]
The content of R register is ANDed with the content of 03, and the result of operation is stored in R register.	Result of 02 03 = [b]	[a]
The content of R register (result [b]) is ORed with the content of S register (result [a]), and the result of operation is stored in R register.	Result of ORing [a] with [b] = [a]+[b]	Vacant
The content of OUT 01 is ORed with the content of R register, and the result of operation is stored in R register.	Result of ORing [a]+[b] with [c] = [a]+[b]+[c]	Vacant
The content of 04 is ANDed with the content of R register, and the result of operation is stored in R register.	Result of ANDing [a]+[b]+[c] with $[d_1]$ = [a]+[b]+[c] × $[d_1]$	Vacant
The content of 05 is ANDed with the content of R register and the result of operation is stored in R register.	Result of ANDing [a]+[b]+[c] × $[d_1]$ with $[d_2]$ = ([a]+[b]+[c]) +$[d_2]$	Vacant
The previous content of R register is transferred to S register, and the content of 06 is stored in R register.	06	[a] [b] [c] [d]
The content of R register is ANDed with the content of 07, and the result of operation is stored in R register.	Result of 06 07 = [e]	[a] [b] [c] [d]
The content of R register is ORed with the content of MR01, and the result of operation is stored in R register.	Result of ORing [e] with [f] = [e]+[f]	[a] [b] [c] [d]
The content of R register is ANDed with the content of S register, and the result of operation is stored in R register.	([a]+[b]+[c]) × [d] × [e]+[f]	Vacant
The result of R register is output to output relay OUT01.	([a]+[b]+[c]) × [d] × ([e]+[f])	Vacant

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5.2 Applied Programs

5.2.1 When LD/OR/AND/NOT instructions are used

1. An example of parallel-series circuit

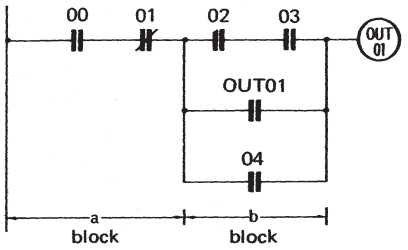


Coding

OP	Sub OP	Data	
LD		00	a
AND		01	
OR	OUT/1	01	
AND		02	b
AND-NOT		03	
OUT		01	
⋮	⋮	⋮	
END			

- Process block "b" after programming block "a" (parallel circuit).
- For coding, enter I/O relay numbers in the data field.

2. An example of series-parallel circuit

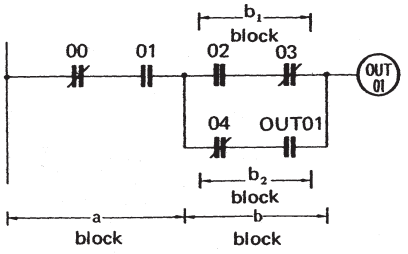


Coding

OP	Sub OP	Data	
LD		00	a
AND-NOT		01	
LD		02	b
AND		03	
OR	OUT/1	01	
OR		04	
AND-LD			
OUT		01	
⋮	⋮	⋮	
END			

- Divide the circuit into blocks "a" and "b" and program each block.
- Then combine blocks "a" and "b" by AND-LD instruction.

3. An example of series-parallel circuit

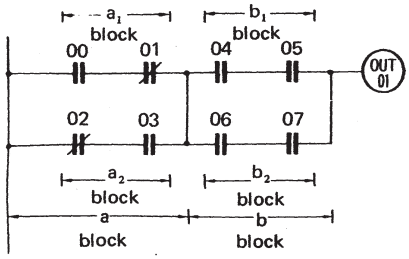


Coding

OP	Sub OP	Data	
LD-NOT		00	a
AND		01	
LD		02	b_1
AND-NOT		03	
LD-NOT		04	b_2
AND	OUT/1	01	
OR-LD			b_1+b_2
AND-LD			a·b
OUT		01	
⋮	⋮	⋮	
END			

- Program block "a".
- Program block "b_1" and then block "b_2".
- Combine blocks "b_1" and "b_2" using OR-LD instruction.
- Combine blocks "a" and "b" using AND-LD instruction.

4. An example of connecting parallel circuits in series



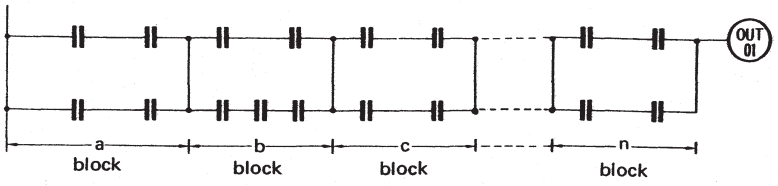
Coding

OP	Sub OP	Data	
LD		00	a_1
AND-NOT		01	
LD-NOT		02	a_2
AND		03	
OR-LD			a_1+a_2
LD		04	b_1
AND		05	
LD		06	b_2
AND		07	
OR-LD			b_1+b_2
AND-LD			a·b
OUT		01	
⋮	⋮	⋮	
END			

- Program block "a_1" and then block "a_2" and combine both blocks using OR-LD instruction.
- Program blocks "b_1" and "b_2" in the same manner as above.
- Combine blocks "a" and "b" using AND-LD instruction.

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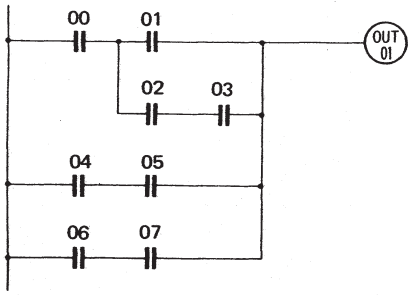
5. An example of connecting parallel circuits in series



- When a number of blocks continue from block number "a" to "n," the programming procedure is the same as paragraph 4 above. Namely, program the circuit the following sequence.

① block a → ② block b → ③ blocks a·b → ④ block c → ⑤ blocks a·b·c → ⑥ · · · ·

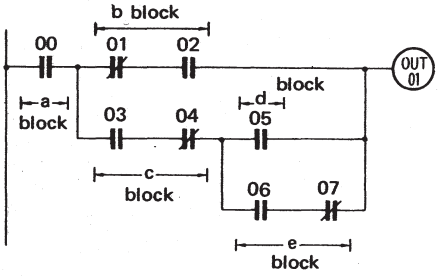
6. An example of complicated parallel circuit



Coding

OP	Sub OP	Data
LD		00
LD		01
LD		02
AND		03
OR·LD		
AND·LD		
LD		04
AND		05
OR·LD		
LD		06
AND		07
OR·LD		
OUT		01
⋮	⋮	⋮
END		

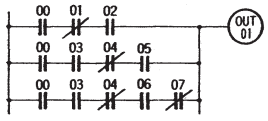
7. An example of complicated circuit



Coding

OP	Sub OP	Data	
LD		00	a
LD·NOT		01	b
AND		02	
LD		03	c
AND·NOT		04	
LD		05	d
LD		06	e
AND·NOT		07	
OR·LD			d+e
AND·LD			(d+e)·c
OR·LD			(d+e)·c+b
AND·LD			[(d+e)·c+b]·a
OUT		01	
⋮	⋮	⋮	
END			

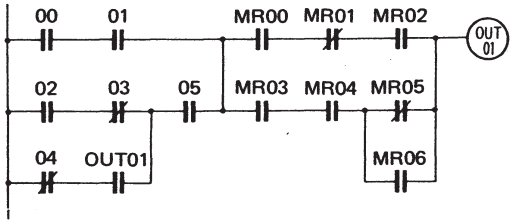
- The circuit shown on the left may be rewritten as follows.



Coding

LD		00
AND·NOT		01
AND		02
LD		00
AND		03
AND·NOT		04
AND		05
OR·LD		
LD		00
AND		03
AND·NOT		04
AND		06
AND·NOT		07
OR·LD		
OUT		01
⋮	⋮	⋮
END		

8. An example of complicated circuit

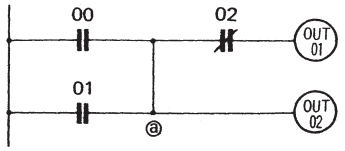


Coding

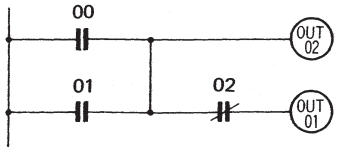
LD		00
AND		01
LD		02
AND·NOT		03
LD·NOT		04
AND	OUT/1	01
OR·LD		
AND		05
OR·LD		
LD	MR/2	00
AND·NOT	MR/2	01
AND	MR/2	02
LD	MR/2	03
AND	MR/2	04
LD·NOT	MR/2	05
OR	MR/2	06
AND·LD		
OR·LD		
AND·LD		
OUT		01
⋮	⋮	⋮
END		

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9. An example of circuit requiring caution

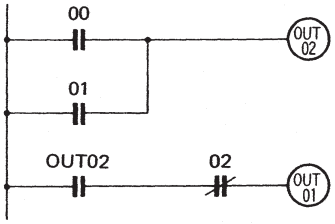


- In such a case as shown above, program relay contact 02 after programming output relay OUT02. This action is necessary for the following reason. Even if an output is sent to OUT02, the content of the R register at point @ will remain unchanged. However, if 02 is programmed before OUT02, the content of the R register at point @ will change and differ from the content sent to OUT02.



- In the case of the above circuit diagram, the circuit operation is possible, but note that this circuit configuration is regarded as a program error during the program check.

or



* This circuit configuration is not regarded as a program error.

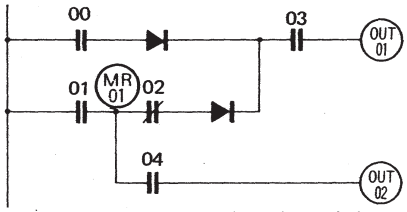
Coding

OP	Sub OP	Data
LD		00
OR		01
OUT		02
AND·NOT		02
OUT		01
⋮	⋮	⋮
END		

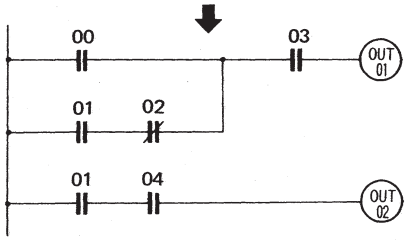
Coding

OP	Sub OP	Data
LD		00
OR		01
OUT		02
LD	OUT/1	02
AND·NOT		02
OUT		01
⋮	⋮	⋮
END		

10. An example of circuit requiring caution



- Separate the above circuit as shown below.



Coding

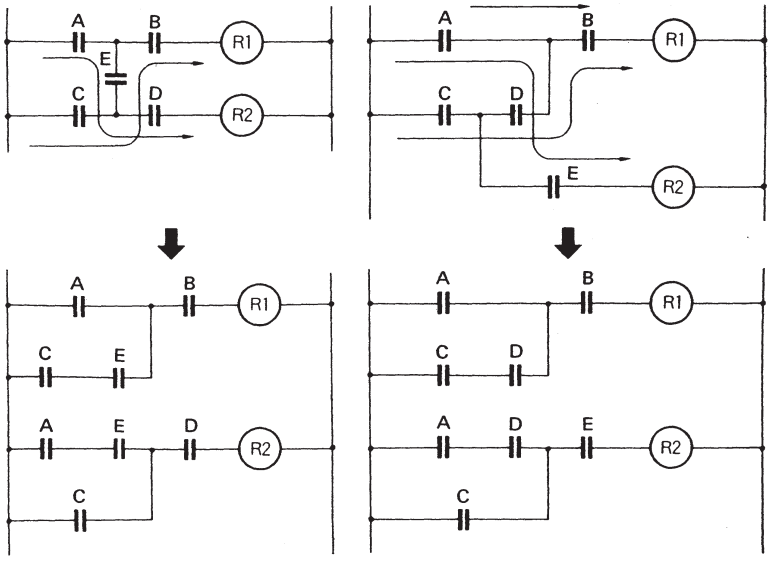
OP	Sub OP	Data
LD		00
LD		01
AND·NOT		02
OR·LD		
AND		03
OUT		01
LD		01
AND		04
OUT		02
⋮	⋮	⋮
END		

- If the circuit is to be programmed without separating it, program an unused internal auxiliary relay after relay contact 01
The following table shows an example of programming MR 01 after 01

Coding

OP	Sub OP	Data
LD		00
LD		01
OUT	MR/2	01
AND·NOT		02
OR·LD		
AND		03
OUT		01
LD	MR/2	01
AND		04
OUT		02
⋮	⋮	⋮
END		

11. Examples of circuit requiring rewrite



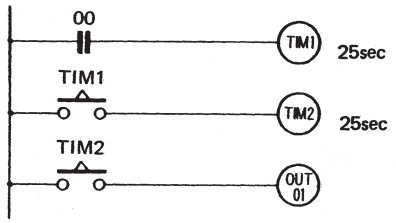
- Such circuits as the two upper circuits shown on the left cannot be programmed and must therefore be rewritten as shown directly below.
- Since the two upper circuits are respectively configured with control relays, the circuits operate even by the flows of signals shown by the arrows. To permit the similar circuit operation with the SYSMAC-P0R, the two upper circuits must be rewritten into the corresponding circuits shown below.

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5.2.2 When TIM/CNT instructions are used

1. Long-time timer (25.5sec or more)

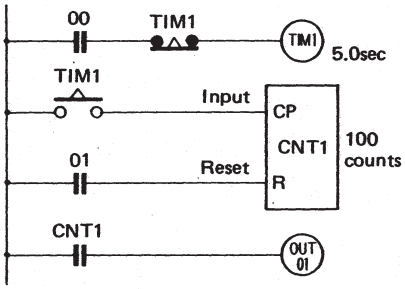
a. Series connection of TIM instructions



Coding

OP	Sub-OP	Data
LD		00
TIM	1	250
LD	TIM/4	1
TIM	2	250
LD	TIM/4	2
OUT		01
⋮	⋮	⋮
END		

b. Use of CNT instruction

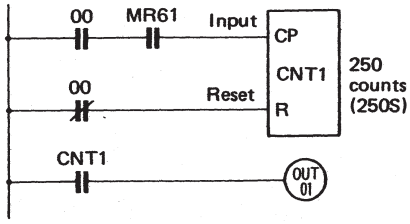


Coding

OP	Sub-OP	Data
LD		00
AND-NOT	TIM/4	1
TIM	1	050
LD	TIM/4	1
LD		01
CNT	1	100
LD	CNT/5	1
OUT		01
⋮	⋮	⋮
END		

- In this circuit, a pulse is generated every 5 seconds by timer TIM1 and then pulses at intervals of 5 seconds are counted by counter CNT1. The example shown here is a 500 sec timer. The setting time of the timer is (timer + scan time) x number of counts.
- The present count value of the counter is retained in memory even if the power switch of the SYSMAC-P0R is turned off.

c. Use of internal clock pulse



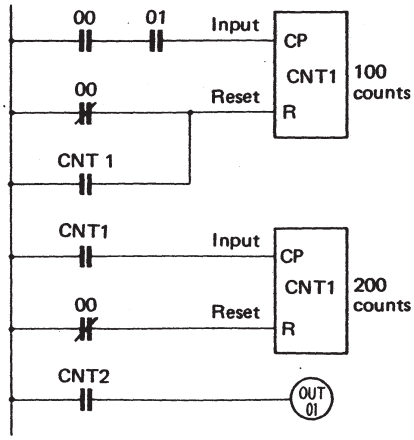
Coding

OP	Sub-OP	Data
LD		00
AND	MR/2	61
LD-NOT		00
CNT	1	250
LD	CNT/5	1
OUT		01
⋮	⋮	⋮
END		

- The SYSMAC-P0R has two internal clock pulses (1.0sec pulse: MR61, 0.1sec pulse: MR60). By counting either of the pulses with a counter, a long-time timer can be developed.
- As CNT instruction is employed, the present count value is retained in memory even after the power is turned off.

2. Multi-digit counter (255 counts or more)

e.g., 20,000 counts

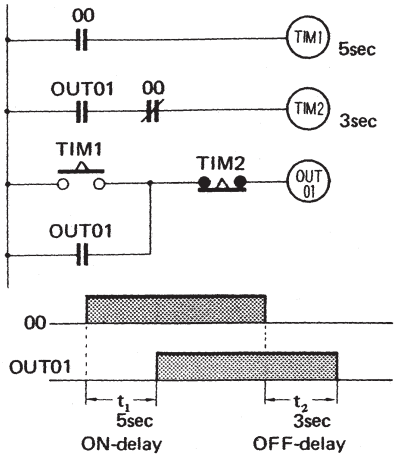


Coding

LD		00
AND		01
LD-NOT		00
OR	CNT/5	1
CNT	1	100
LD	CNT/5	1
LD-NOT		00
CNT	2	200
LD	CNT/5	2
OUT		01
⋮	⋮	⋮
END		

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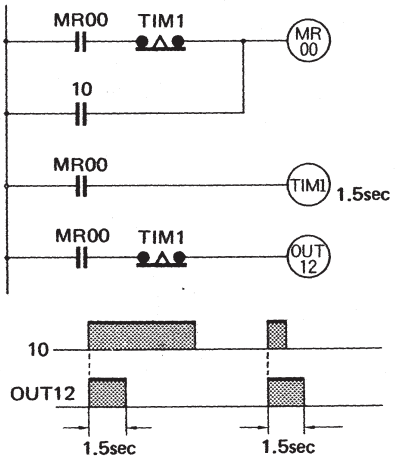
3. An example of ON/OFF-delay timer circuit



Coding

OP	Sub OP	Data
LD		00
TIM	1	050
LD	OUT/1	01
AND-NOT		00
TIM	2	030
LD	TIM/4	1
OR	OUT/1	01
AND-NOT	TIM/4	2
OUT		01
⋮	⋮	⋮
END		

4. An example of one shot timer circuit



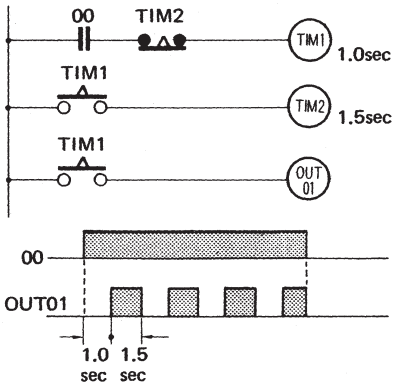
Coding

OP	Sub OP	Data
LD	MR/2	00
AND-NOT	TIM/4	1
OR		10
OUT	MR/2	00
LD	MR/2	00
TIM	1	015
LD	MR/2	00
AND-NOT	TIM/4	1
OUT		12
⋮	⋮	⋮
END		

- One shot output is produced for only the set time of TIM1 after an input signal is applied.

5. Examples of flicker circuit

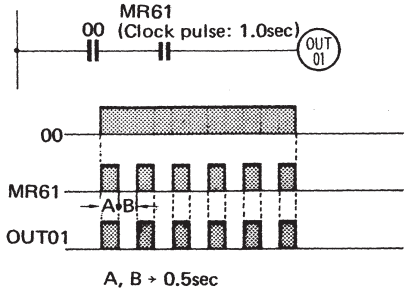
a. With 2 timers used



Coding

OP	Sub OP	Data
LD		00
AND-NOT	TIM/4	2
TIM	1	010
LD	TIM/4	1
TIM	2	015
LD	TIM/4	1
OUT		01
⋮	⋮	⋮
END		

b. With clock pulses



Coding

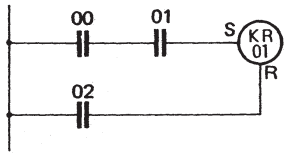
OP	Sub OP	Data
LD		00
AND	MR/2	61
OUT		01
⋮	⋮	⋮
END		

- Using an internal clock pulse (0.1sec or 1.0sec), a flicker circuit can be processed easily. In this case, however, the flickering time is available only in the following 2 types.
  Special auxiliary relay number MR61: 1.0sec clock pulse
  Special auxiliary relay number MR60: 0.1sec clock pulse

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5.2.3 When latching relay is used

1. Basic circuit

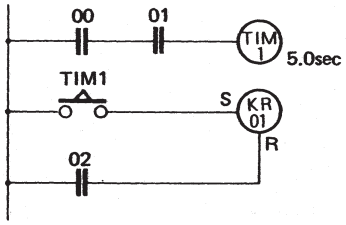


Coding

OP	SUB	No.
LD		00
AND		01
LD		02
OUT	KR/3	01
⋮	⋮	⋮
END		

- In the event of a power failure, the ON/OFF state before power failure can be retained in memory, using a latching relay. SYSMAC-P0R has 47 latching relays with relay numbers KR00 ~ KR46.
- Memory retention time after a power failure is about 2 years just the same as that of the program memory.

2. A circuit to keep the time-up state

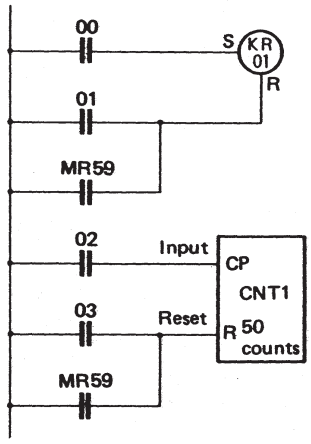


Coding

OP	SUB	No.
LD		00
AND		01
TIM	1	050
LD	TIM/4	1
LD		02
OUT	KR/3	01
⋮	⋮	⋮
END		

5.2.4 When Special Auxiliary Relay MR59 is used

1. A circuit to initialize a counter and a latching relay when power is applied



Coding

OP	SUB	No.
LD		00
LD		01
OR	MR/2	59
OUT	KR/3	01
LD		02
LD		03
OR	MR/2	59
CNT	1	050
⋮	⋮	⋮
END		

- Special auxiliary relay MR59 is turned on for 1 scan time when power is applied in the RUN mode or when the mode selector switch is changed from "STOP" to "RUN" position.

5.2.5 When Special Auxiliary Relay MR62 is used

1. A circuit to transmit a battery fault signal to an output terminal



Coding

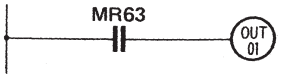
OP	SUB	No.
LD	MR/2	62
OUT		01
⋮	⋮	⋮
END		

- Relay MR62 is turned on when the battery voltage drops or when the battery voltage drops or when the battery is not loaded.
- If a buzzer is connected to the terminal of output relay OUT01, MR62 can be used to issue alarm.
- When the battery is restored to normal, MR62 is turned off.

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5.2.6 When Special Auxiliary Relay MR63 is used

1. A circuit to transmit a memory fault signal to an output terminal



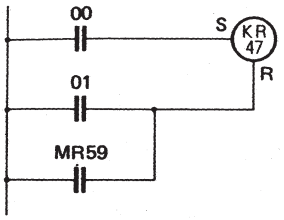
Coding

OP	Sub-OP	Data
LD	MR/2	63
OUT		01
⋮	⋮	⋮
END		

- Special auxiliary relay MR63 is turned on when a memory failure occurs and the ERROR indicator flashes on and off.
- MR63 is turned off when a power failure occurs or when the mode selector switch position is changed.
- If a buzzer is connected to the terminal of OUT01, MR63 can be used to issue alarm.

5.2.7 When Special Latching Relay KR47 is used

1. A circuit to inhibit all outputs



Coding

OP	Sub-OP	Data
LD		00
LD		01
OR	MR/2	59
OUT	KR/3	47
⋮	⋮	⋮
END		

- When special latching relay KR47 is turned on, all outputs are inhibited, causing all output relays to release. At this time, all the OUTPUT indicators go out and the RUN indicator flashes on and off.
- When special latching relay KR47 is turned off, all the outputs are released from the inhibited state.

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6. Operating Procedure

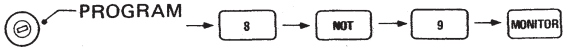
6.1 Basic Functions

Items of Operation	Description
All program clear	Since the CPU retains previously stored data in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.
Address setting	Address setting is required to designate an address in such operations as program read, program write, etc.
Program write	This operation is to store a program in the specified memory address.
Program read	This operation is to confirm whether or not data has been programmed properly in the specified memory address.
Program check	This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the predetermined rules (syntax).
RUN	This operation is to place the SYSMAC-P0R in the RUN (Program Execution) state.
Monitor	This operation is to display the operating state of each relay, or the present value of each timer or counter during the execution of a program.
Trace (continuity) check	When a circuit operation is to be checked in a program simulation or test run, this operation allows the operating state of each relay number to be displayed while tracing the programming sequence of the circuit.
Instruction search	When a circuit change is to be made in a program simulation or test run, this operation allows an address where an instruction has been written in a program to be searched.
Contact (coil) number change	This operation is to change the contact (or coil) number in a program due to a circuit modification.
Contact (coil) addition	This operation is employed when the contact (or coil) number is to be added due to a circuit modification.
Contact (coil) deletion	This operation is to delete the contact (or coil) number from a program due to a circuit modification.
EPROM write	This operation is to transfer the contents of the RAM to the specified EPROM bank.
EPROM read	This operation is to transfer the contents of the specified EPROM bank to the RAM.
EPROM verify	This operation is to verify the contents of the specified EPROM bank against the contents of the RAM.
Tape write	This operation is to record the contents of the RAM (program memory) on a cassette tape.
Tape read	This operation is to transfer the program data recorded on the cassette tape into the RAM.
Tape verify	This operation is to verify the contents of the RAM against the programmed data recorded on a cassette tape.

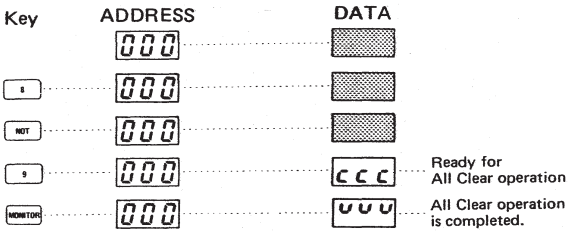
6.2 All Program Clear Operation

Since the CPU retains previously stored data in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.

- **Operating procedure**



- **Display**



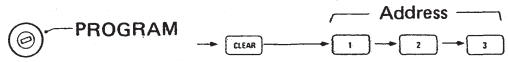
NOTES:
1. By the All Clear operation, all the programs (I/O relays, internal auxiliary relays, latching relays, timers and counters) stored in addresses 000 ~ 255 are cleared.
2. Before the key operation, change the mode selector switch position from other mode to "PROGRAM."
3. In the All Clear operation, a beep sound is generated at the depression of each key.

CAUTION:
After the PROGRAM mode selection, depression of CLEAR key or any key other than the four keys shown above will not allow All Clear operation to be executed. In this case, repeat the operation starting from the mode selection. For example, if the PROGRAM mode was originally changed from the RUN mode, do not set the mode selector to the RUN mode again. First set it to the STOP mode and then to the PROGRAM mode to repeat the operation.

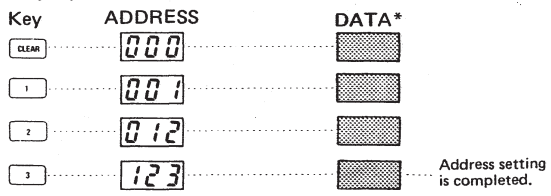
6.3 Address Setting Operation

Address setting is required to designate an address in such operations as program read, program write.

- **Operating procedure**

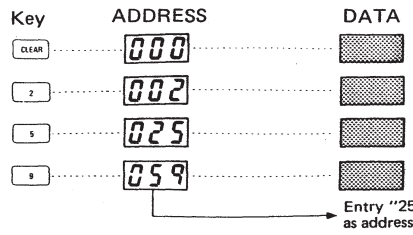


- **Display**



NOTES:
1. Each address is set in 3 digits using numeric 000 ~ 255. To set address "000," no numeric entry is required. To set address "003," depress only numeric key 3 and to set address "023," depress only numeric keys 2 and 3. Preceding zero(es) may be omitted from key entry.
2. * The data entered will not be displayed by the address setting operation alone. To display the data entered, [ ] [ ] keys must be depressed.
3. In address setting, when numeric data entered as an address exceeds 255, the first digit of the 3-digit address is automatically processed as "0." Since the CPU does not recognize this as an error, the only way to identify this error is through confirmation by the operator.
For example, if address 259 is entered, it will be set as follows.

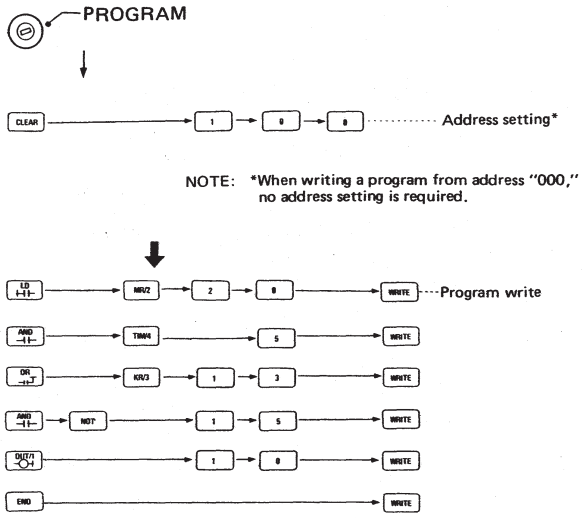
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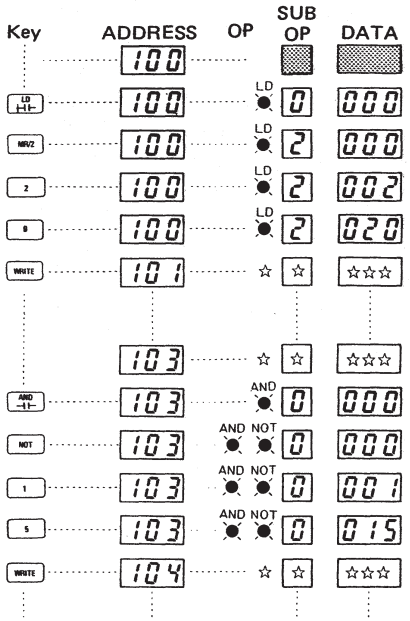
6.4 Program Write Operation

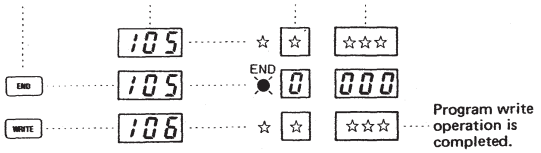
This operation is to store a program in the specified memory address.

- **Operating procedure**

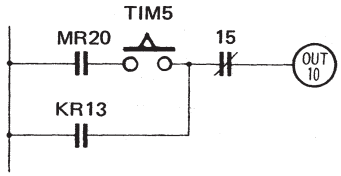


- **Display**





- **Circuit for exercise and programming example**



Coding

Address	OP	Sub OP	DATA
100	LD	MR/2	20
101	AND	TIM/4	5
102	OR	KR/3	13
103	AND-NOT		15
104	OUT		10
105	END		
106	⋮	⋮	⋮

NOTES:

1. In the left-hand figure, ☆☆☆ indicates that the content of the memory at the displayed address will appear in the DATA display. Accordingly, after the All Clear operation, nothing will appear in the OP display and zeroes will appear in the SUB OP and DATA displays, respectively.
2. Depression of the WRITE key causes the contents appearing in the OP, SUB OP and DATA displays to be stored into the memory address specified by the ADDRESS display and at the same time causes the memory address to be incremented by one.

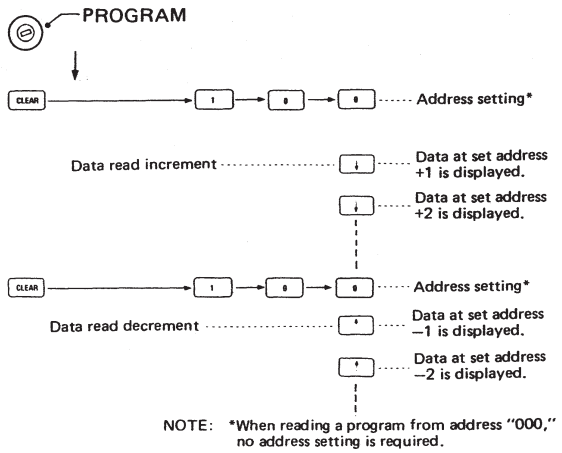
Correction Procedures when an error occurs in program write

1. If an error in programming is noticed before depressing the WRITE key, depress the CLEAR DISPLAY key and the re-entry operation from OP code becomes effective.
2. If an error is programming is discovered after depressing the WRITE key, repeat the operation from the address setting, or return to the address in which the error exists by depressing the ↑ key and then depress the CLEAR DISPLAY key and the re-entry operation from OP code becomes effective.

6.5 Program Read Operation

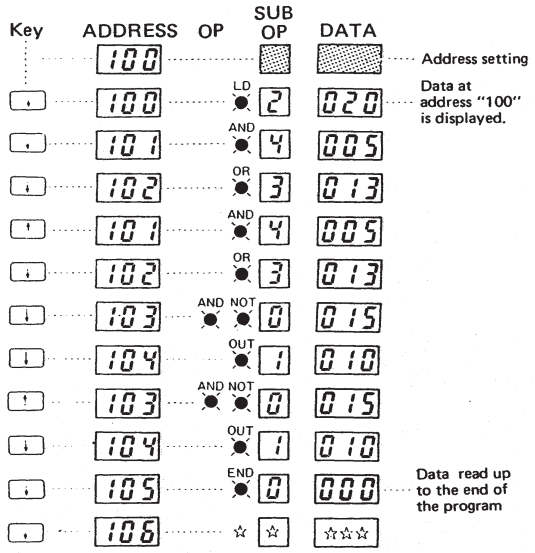
This operation is to confirm whether or not the data has been programmed properly in the specified memory address.

- **Operating procedure**

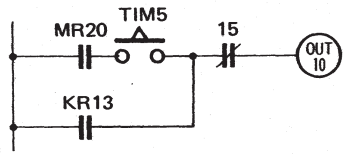


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- **Display**



- **Circuit for exercise and programming example**



Coding

Address	OP	Sub OP	Data
100	LD	MR/2	20
101	AND	TIM/4	5
102	OR	KR/3	13
103	AND-NOT		15
104	OUT		10
105	END		
106	⋮		⋮

NOTES:
1. At each depression of the ↓ key, the data at the set address +1 is displayed (i.e., data read increment).
2. At each depression of the ↑ key, the data at the set address −1 is displayed (i.e., data read decrement).

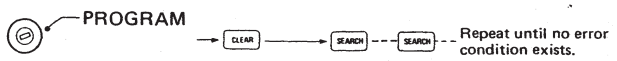
6.6 Program Check Operation

This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the predetermined rules (syntax).

Items subject to program check are as follows.

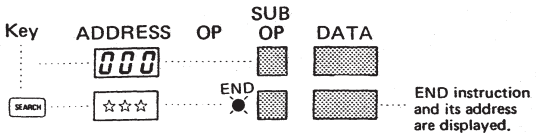
- Coil duplication error
- Circuit error
- END instruction missing error

- **Operating procedure**

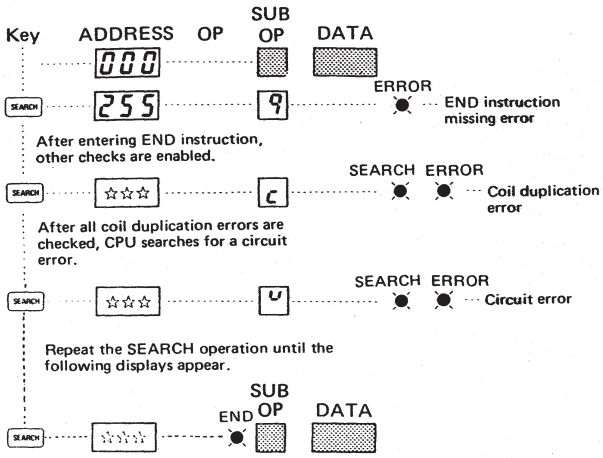


- **Display**

When a program error does not exist



When a program error exists



- **Error conditions**

1. END instruction missing error
   In the absence of an END instruction at the last address of a program, error message " 9 " appears in the SUB OP display. If this error occurs, the CPU cannot perform other item checks. After entering an END instruction, the CPU is enabled to perform other item checks.
2. Coil duplication error
   If a program contains OUT, OUT MR/2, OUT KR/3, TIM or CNT instructions of the same number, error message " c " appears in the SUB OP display. After all the coil duplication errors have been checked, the CPU performs circuit error check.
3. Circuit error
   This check is intended to manage the R and S registers. As a method, the difference between the number of logical start instructions (LD, LD-NOT, etc.) and the number of inter-block logic instructions (AND-LD, OR-LD) is computed, and if the difference is abnormal when the results of the operation (OUT, OUT MR/2, OUT KR/3, TIM and CNT) are executed, this condition is regarded as a circuit error.

NOTES:
1. Priority in program check is as follows: END instruction missing error > coil duplication error > circuit error.
2. If any programming error is discovered, correct the erroneous program in accordance with the program write procedure.

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6.7 RUN Operation

This operation is to place the SYSMAC-P0R in the RUN (Program Execution) condition.

- **Operating procedure**



NOTES:

1. In the RUN mode, sum check, watchdog timer check and battery check are automatically performed. If any error occurs in the respective checks, the status indicators and the state of program execution by CPU become as shown below. (See paragraph 8.5, Troubleshooting for details.)

	ERR/ALM indicator	RUN indicator	BAT indicator	State of program execution by CPU
Sum check	●	◐		Continues
Watchdog timer	●	○		Stops
Battery failure		●	●	Continues

○ mark indicates the indicator goes out.
● mark indicates the indicator lights.
◐ mark indicates the indicator flashes ON and OFF.

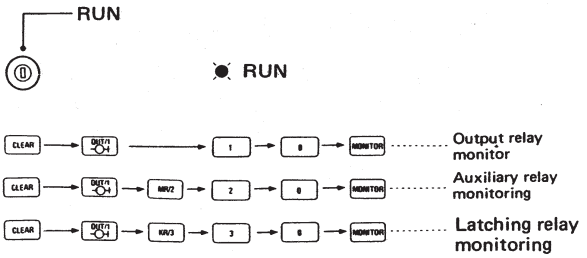
2. In other than the RUN mode, all external outputs are turned off. When the mode selector switch position is changed from "STOP" to "RUN," the SYSMAC-P0R is placed in the same state when power is applied.

6.8 Monitor Operation

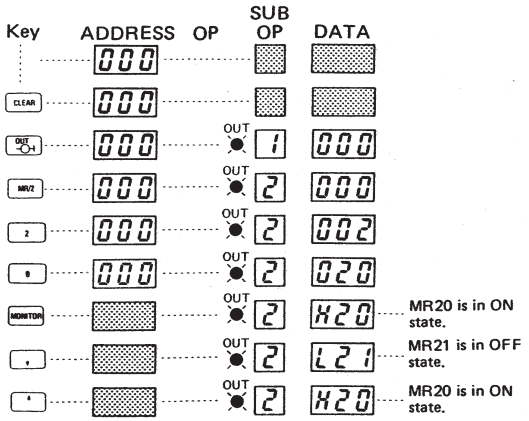
This operation is to display the operating state of each relay, or the present value of each timer or counter during the execution of a program.

■ MONITORING OF THE OPERATING STATE OF AN OUTPUT RELAY, INTERNAL AUXILIARY RELAY OR LATCHING RELAY

- **Operating procedure**

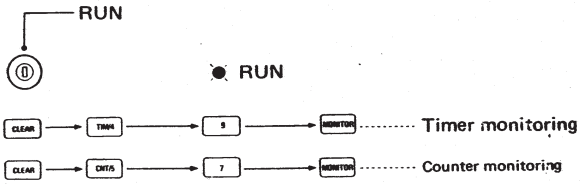


- **Display**

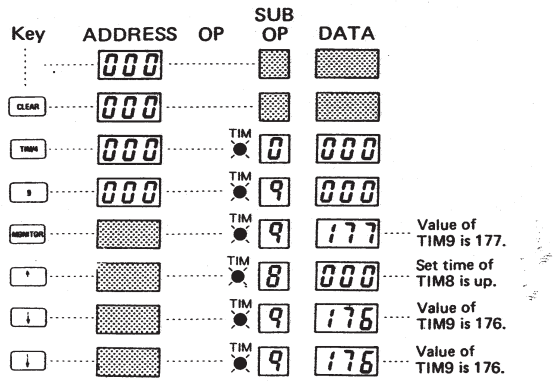


■ MONITORING OF THE CURRENT VALUE OF A TIMER, OR COUNTER

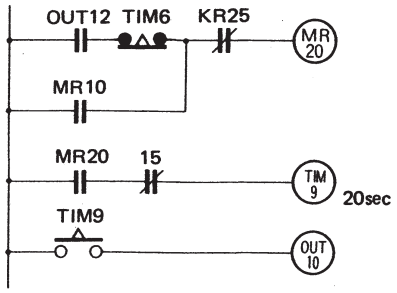
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



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Coding

Address	OP	Sub OP	Data
100	LD	OUT/1	12
101	AND-NOT	TIM/4	6
102	OR	MR/2	10
103	AND-NOT	KR/3	25
104	OUT	MR/2	20
105	LD	MR/2	20
106	AND-NOT		15
107	TIM	9	200
108	LD	TIM/4	9
109	OUT		10
110	END		

NOTES:

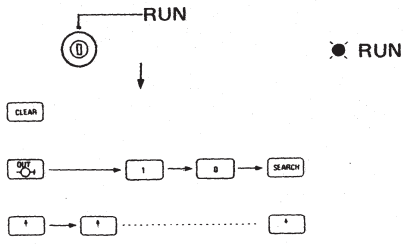
1. As the operating state of each output relay, auxiliary relay, or latching relay, "H" or "L" is displayed at the MSD position of the DATA display.
   "H" (High level) is displayed when the state of the set relay number is ON.
   "L" (Low level) is displayed when the state of the set relay number is OFF.
2. As the present value of each timer or counter, 3-digit data is displayed in the ADDRESS display. When the set time of the set timer number is up (or the set value of the set counter number is counted out), "000" will appear in the 3-digit positions of the DATA display.
3. At each depression of the [↑] or [↓] key following the MONITOR key, the relay number, timer number or counter number is incremented or decremented respectively by 1. Thus, the state of each relay, timer, or counter can be monitored in succession.

6.9 Trace (Continuity) Check Operation

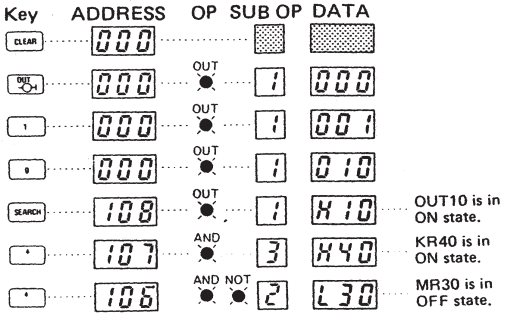
When a circuit operation is to be checked in a program simulation or test run, this operation allows the operating state of each relay number to be displayed while tracing the programming sequence of the circuit.

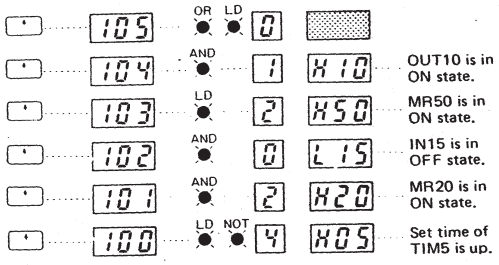
- **Operating procedure**

  In the circuit for exercise shown on the right, the procedure to check the operating states of respective relays from (OUT 10) to (TIM5) in the programming sequence is shown below.

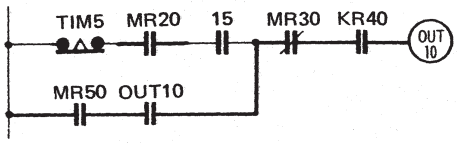


- **Display**





- **Circuit for exercise and programming example**



Coding

Address	OP	Sub OP	Data
100	LD-NOT	TIM/4	5
101	AND	MR/2	20
102	AND		15
103	LD	MR/2	50
104	AND	OUT/1	10
105	OR-LD		
106	AND-NOT	MR/2	30
107	AND	KR/3	40
108	OUT		10
109	END		
110			

NOTES:

1. The following two methods of trace check are available.
   - Check starting from address 000

     [CLEAR] → [↑] → [↑] ····· [↑]

   - Check starting from an OUT instruction (OUT, OUT MR/2, OUT KR/3, TIM, or CNT).

     [CLEAR] → [OUT] → [MR/2] → [5] → [0] → [SEARCH] → [1] → [↑]
2. In the RUN mode, the SEARCH operation is possible for OUT, OUT MR/2, OUT KR/3, TIM and CNT instructions only.
3. In the RUN mode, a beep sound is generated when the output instruction has been searched.
4. When the relay number represented by the low-order 2 digits of the DATA display is in the ON state, "H" will appear in the MSD position of the DATA display. When the relay number is in the OFF state, "L" will appear in the MSD position of the DATA display. This indicates the ON/OFF state of the relay number without relation to the presence or absence of a NOT instruction. In other words, if "L" appears when a NOT instruction is entered, it indicates that the relay is in the energized state.
5. Search of timer or counter.
   When a timer or counter is searched in the RUN mode, the present value of the timer or counter is not displayed. "H" is displayed when the set time (or set count) is up, while "L" is displayed when the set time (or set count) is remaining.

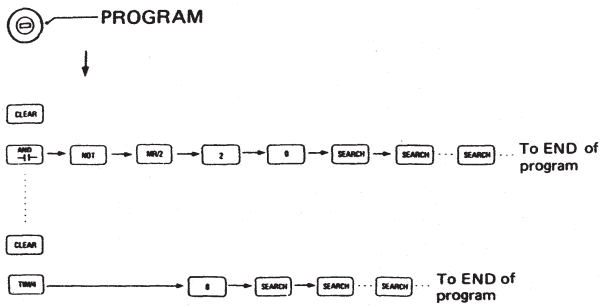
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6.10 Instruction Search Operation

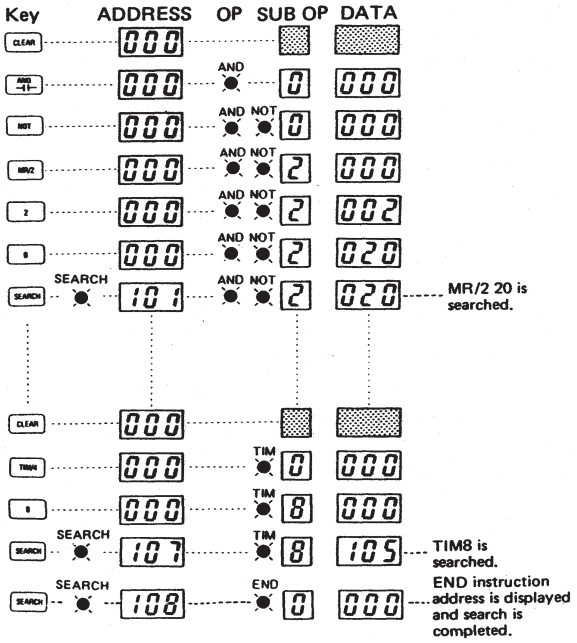
When a circuit change is to be made in a program simulation or test run, this operation allows an address where an instruction has been written in a program to be searched.

- **Operating procedure**

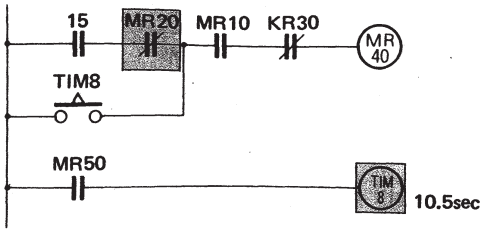
  Referring to the circuit for exercise and programming example shown below, an example of searching MR02 and (TIM 8) instructions is explained here.



- **Display**



- **Circuit for exercise and programming example**



shows the instruction to be searched.

Coding

Address	OP	Sub OP	Data
100	LD		15
101	AND-NOT	MR/2	20
102	OR	TIM/4	8
103	AND	MR/2	10
104	AND-NOT	KR/3	30
105	OUT	MR/2	40
106	LD	MR/2	50
107	TIM	8	105
108	END		
109			
110			

NOTES:

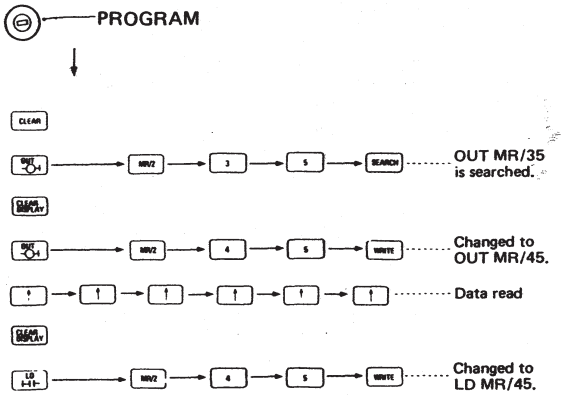
1. When the SEARCH key is depressed after entering an instruction, the first address where the instruction is stored is displayed. Continued depression of the SEARCH key causes all the addresses containing this instruction to be searched until the END instruction is encountered.
2. If the program has no END instruction, the CPU cannot perform the search operation. This condition is indicated as "END instruction missing error" on the SUB OP display and the ERROR indicator will be illuminated if such a condition occurs.
3. If the instruction entered is not contained in the program, depression of the SEARCH key causes the END address to be displayed.
4. When a TIM or CNT instruction is to be searched, it is unnecessary to enter the setting value of the timer or counter.
5. A search operation is completed when the CLEAR or CLEAR DISPLAY key is depressed or after the search of an END instruction in a program. Upon completion of the search operation, the SEARCH indicator will go out.

6.11 Contact (Coil) Number Change Operation

This operation is to change the contact (or coil) number in a program due to a circuit modification.

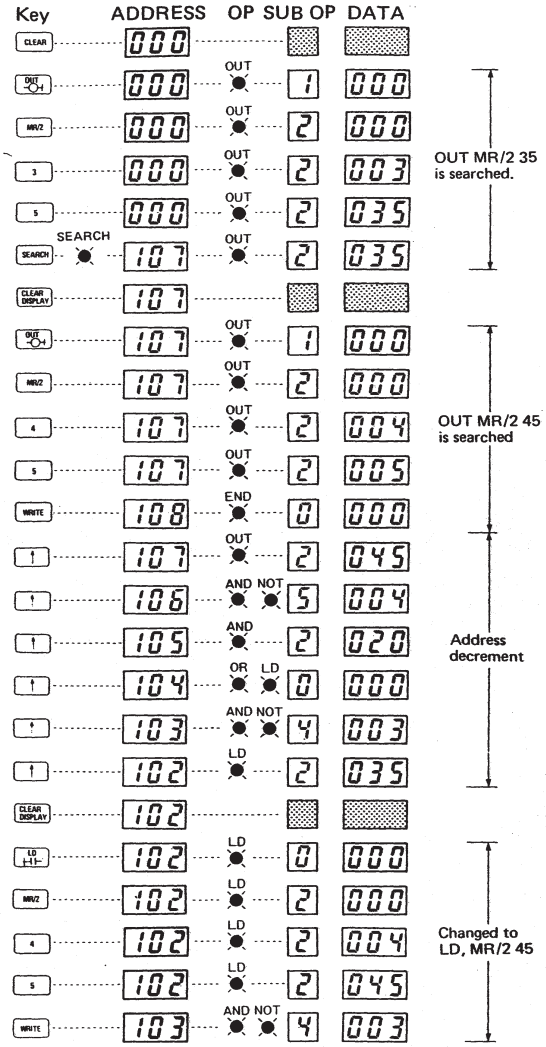
- **Operating procedure**

  Refer to the circuit for exercise and programming example shown on the right.

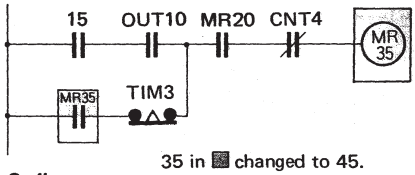


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- **Display**



- **Circuit for exercise and programming example**



35 in ■ changed to 45.

Coding

Address	OP	Sub OP	Data
100	LD		15
101	AND	OUT/1	10
102	LD	MR/2	35
103	AND-NOT	TIM/4	3
104	OR-LD		
105	AND	MR/2	20
106	AND-NOT	CNT/5	4
107	OUT	MR/2	35
108	END		
109			
110			

NOTES:

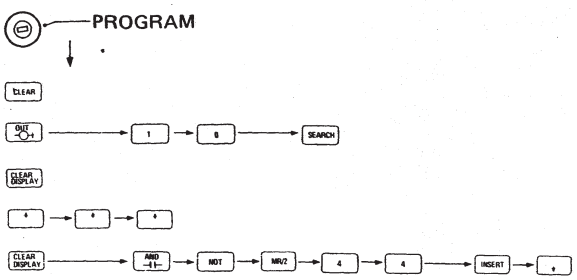
1. After an OUT instruction has been searched, depress the [↑] or [↓] key continuously to decrement the address number until the address where the contact (coil) number is to be changed. The instruction to be changed at an intended address may be searched directly. However, the same instruction may in some cases be stored in other memory addresses of the same program. Therefore, it is necessary to check instructions before and after the intended address. Since no two OUT instructions with an identical relay number exist in one program, the instruction to be changed can be found easily and quickly by first searching the OUT instruction and then searching before and after the OUT instruction.
2. When the contact (coil) number of an OUT, TIM, or CNT instruction is to be changed, confirm the circuit related to the instruction.
3. After the contact (coil) number has been changed, be sure to perform the Program Check operation ([CLEAR] → [SEARCH]) to confirm that the program is free from any programming error.

6.12 Contact (Coil) Addition Operation

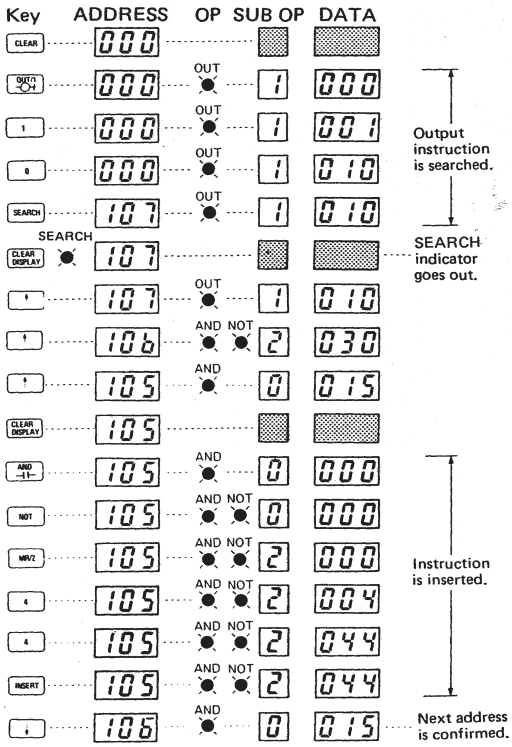
This operation is employed when the contact (or coil) number is to be added due to a circuit modification.

- **Operating procedure**

In the following, the procedure of adding MR44 before 15 is shown.

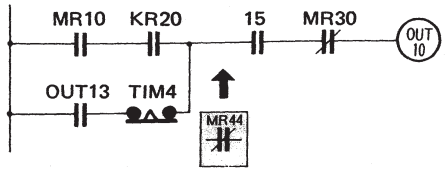


- **Display**



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- **Circuit for exercise and programming example**



Coding

Address	OP	Sub OP	Data
100	LD	MR/2	10
101	AND	KR/3	20
102	LD	OUT/1	13
103	AND-NOT	TIM/4	4
104	OR-LD		
105	AND		15
106	AND-NOT	MR/2	30
107	OUT		10
108	END		
109			
110			

Coding

100	LD	MR/2	10
101	AND	KR/3	20
102	LD	OUT/1	13
103	AND-NOT	TIM/4	4
104	OR-LD		
105	AND-NOT	MR/2	44
106	AND		15
107	AND-NOT	MR/2	30
108	OUT		10
109	END		
110			

NOTES:

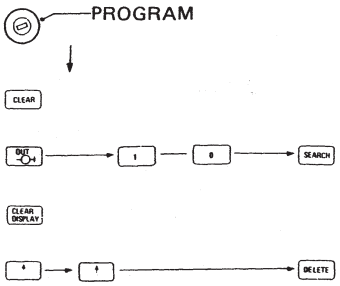
1. When an instruction entered for addition is in excess of the program capacity, the INSERT key input will not be accepted and thus the instruction cannot be inserted.
2. After the instruction to be inserted has been entered, depression of the INSERT key two or more times in succession will be ignored and no instruction can be entered.
3. After the insertion of the instruction, confirm instructions before and after the inserted address.
4. After the contact (coil) has been inserted, be sure to perform the Program Check operation (CLEAR → SEARCH) to confirm that the program is free from any programming error.

6.13 Contact (Coil) Deletion Operation

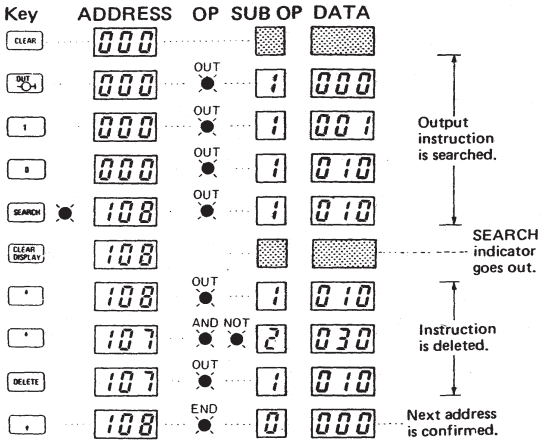
This operation is to delete the contact (or coil) number from a program due to a circuit modification.

- **Operating procedure**

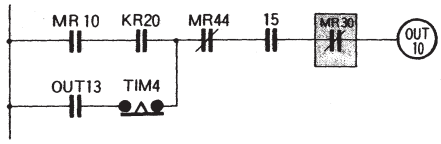
  Referring to the circuit for exercise shown below, an example of deleting MR30 is explained.



- **Display**



- **Circuit for exercise and programming example**



☐ indicates the instruction to be deleted.

Coding

100	LD	MR/2	10
101	AND	KR/3	20
102	LD	OUT/1	13
103	AND-NOT	TIM/4	4
104	OR-LD		
105	AND-NOT	MR/2	44
106	AND		15
107	AND-NOT	MR/2	30
108	OUT		10
109	END		
110			

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Coding

Address	OP	SUB OP	Data
100	LD	MR/2	10
101	AND	KR/3	20
102	LD	OUT/1	13
103	AND-NOT	TIM/4	4
104	OR-LD		
105	AND-NOT	MR/2	44
106	AND		15
107	OUT		10
108	END		
109			
110			

NOTES:
1. After the instruction has been deleted, confirm instructions before and after the deleted address.
2. After the deletion of the instruction, be sure to execute the Program Check operation (CLEAR → SEARCH). Particularly, the program check is mandatory when such an instruction as LD, OUT, TIM, or CNT is deleted.
3. Note that each depression of the DELETE key causes each instruction being displayed to be deleted successively.

6.14 EPROM Handling

The Type SCYP0R-CPU20 is an EPROM self-contained type CPU. Since the CPU executes programs by reading the contents of the RAM, this type of CPU permits data read, write and verify operations between the RAM and the EPROM when various programs are in use, or for program storage.

■ AVAILABLE TYPE OF EPROM

Type ROM-F (equivalent to 2716)

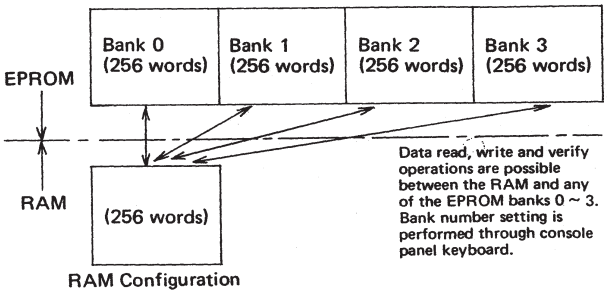
■ MEMORY CAPACITY

4 kinds of user programs (256 RAM addresses x 4) can be stored per EPROM chip.

■ ADDRESS SETTING

The EPROM address area is divided into 4 which are referred to as Bank 0, 1, 2 and 3, respectively. The capacity of one RAM corresponds to one EPROM bank (i.e., 256 words).

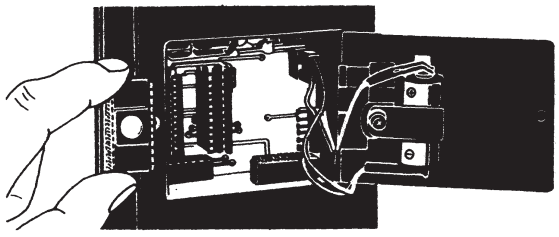
EPROM Bank Configuration



RAM Configuration

■ MOUNTING EPROM CHIP

Be sure to insert the EPROM chip onto the EPROM socket with its dip facing upwards.

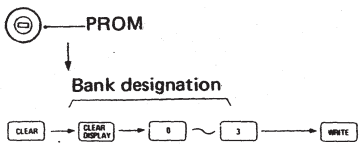


NOTES:
1. Completely erase the EPROM and then write data into the EPROM. The contents of the EPROM are erased by irradiating ultraviolet rays on the EPROM surface through the erase window. The EPROM cannot be erased completely if the irradiation of ultraviolet rays is insufficient. Therefore, be sure to observe the specified erase time. Whether or not the EPROM has been erased completely can be confirmed by the EPROM Verify operation. (Refer to paragraph 6.18, Errors in PROM Mode.)
2. Erase time
   Completely erase the EPROM according to the specifications of the eraser to be used.
3. Frequency of re-programming
   Limit the frequency of re-programming the EPROM to 7 times. If the EPROM is reprogrammed more than 7 times, the EPROM may malfunction.
4. Program protection
   To sustain the reliability of the EPROM, place the EPROM in a protective case or wrap it in aluminum foil if it is not to be used for an extended period.
5. Handling EPROM
   The EPROM is susceptible to static electricity being carried in the human body. When handling the EPROM, avoid touching its pins as much as possible.
6. Removal of EPROM
   The EPROM can be inserted or removed while power is being applied to the SYSMAC-P0R. However, never remove the EPROM chip during the EPROM write, read, or verify operation.
7. After the program debugging, be sure to attach a light-shielding seal to the erase window in order to maintain the reliability of the EPROM chip.

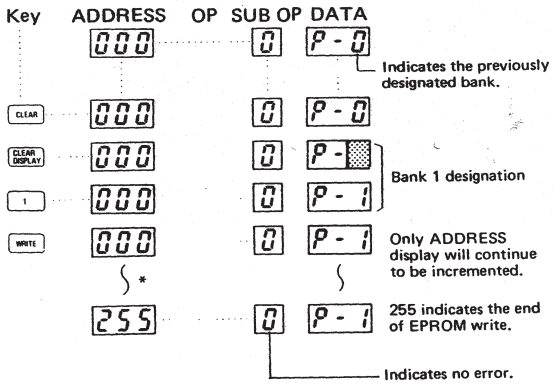
6.15 EPROM Write Operation

This operation is to transfer the contents of the RAM to the specified EPROM bank.

- **Operating procedure**



- **Display**



NOTES:
1. Bank designation is not required if the same bank as that previously set is to be used. Therefore, the only required key operation in this case is as follows.
   CLEAR → WRITE
2. * Upon depression of the WRITE key, only the ADDRESS display will continue to be incremented. When the display shows 255, it indicates that the EPROM write operation has been completed.
3. During the EPROM write operation, if the power is turned off, or the EPROM chip is removed, the EPROM write will be interrupted. In such a case, retry the EPROM write operation from the beginning after erasing the EPROM chip, or use other EPROM.
4. During the EPROM write operation, no PROGRAM key input will be accepted.

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