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OMRON USER'S MANUAL

Programmable Controller

Model SYSMAC-P0R

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INTRODUCTION

"OMRON SYSMAC" is the trade name of OMRON's programmable controllers unparalleled in reliability and versatility.

Programmable controllers, which were initially developed to meet the demands by equipment manufacturing industries and large-scale plants for their production facilities, now answer the needs of industries from every field and have become original equipment for installation at factories.

The above trend has induced original equipment manufacturers to design the incorporation of programmable controllers in their machinery and equipment, and thus the demand for availability of the programmable controllers that can be handled as easily as components has been increasing. Accordingly, OMRON has sought to develop programmable controllers which are: a. small and economical, b. easy to handle by merely connecting a load and power and c. easy to operate by anyone at site, in addition to possessing flexibility that permits adapting to changes to the controlled systems or control parameters with simple keyboard operation and high reliability which can be materialized only by electronic control.

OMRON now offers with confidence the OMRON SYSMAC-P0R Package Type Programmable Controller, a first-class programmable controller with "CPU function" and "techniques responding adequately to the needs at every site." Programming with the SYSMAC-P0R can be performed easily and directly from ladder diagrams using the program console incorporated in the programmable controller.

The OMRON SYSMAC-P0 Step Advance Type Sequence Controller which employs the timing chart programming method is also recommended.

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OMRON SYSMAC-P0R Coding Sheet

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1. Features

Compact, slim styled programmable controller with abundant checking functions and cassette tape adapter.

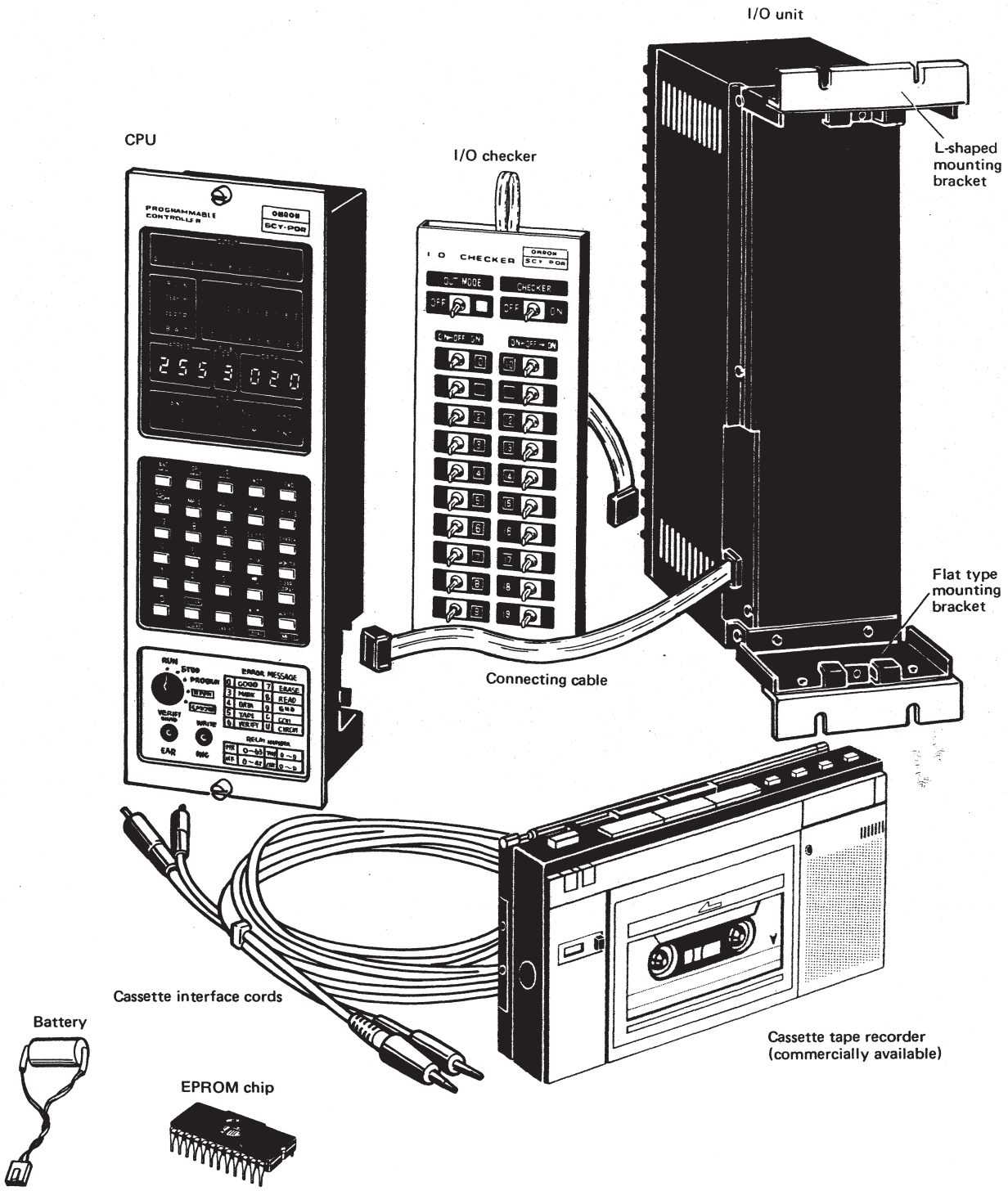
- **Integrated program console**
  The central processing unit (CPU) incorporates a program console which is provided with an abundance of operational check functions in addition to programming. From the keyboard of this program console, ladder diagrams can be programmed directly with ease and speed.
- **Continuity checking is possible according to the sequence of ladder diagram**
  The SYSMAC-P0R is capable of retrieving an instruction word (output instruction) during the program execution to check the circuit block concerned for electrical continuity according to the sequence of the ladder diagram. Furthermore, it monitors the present value of each timer or counter, thus facilitating the program simulation and maintenance operations of the controller.
- **RAM and RAM & ROM types for free selection**
  Normally, the RAM type programmable controller is supplied. However, the RAM & ROM type programmable controller is available for selection to meet the specifications of the equipment to be controlled. With the RAM & ROM type, a maximum of four program patterns can be written into the EPROM in units of 256 words per pattern. After the program writing, a user program can be selected for execution by operating the program console.
- **Flexible mounting style**
  Since the SYSMAC-P0R consists of a CPU and an I/O unit, the two units can be mounted either as an integrated unit or as separated units and wiring is also possible from either front or rear panel.
- **Built-in PROM writer function**
  The PROM writer function is incorporated only in the RAM & ROM type CPU to permit writing of a debugged program into the EPROM.
- **Programs can be recorded on cassette tape**
  By connection of the exclusive interface cords, programs in the CPU memory may be dumped onto a commercially available cassette tape.
- **Program address control is not required**
  Since direct programming from ladder diagrams is possible, the contents of the program memory are readily known through retrieval of instructions during program change, simulation, or maintenance. Therefore, it is not necessary to control the use of program addresses by coding sheets.

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2. System Configuration and Specifications

2.1 Available Types

The SYSMAC-P0R consists of a central processing unit (CPU) and an I/O unit. As an optional accessory, an I/O checker for manual input is available for use in program debugging. A PROM writer and a cassette interface are contained in the CPU.



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■ STANDARD TYPES

Classification	Components	Type
RAM type	RAM type CPU, I/O unit, Connecting cable (20cm), Battery, Mounting brackets (L-shaped/Flat type)	SCY-P0R10E
RAM & ROM type	RAM & ROM type CPU, I/O unit, Connecting cable (20cm), Battery, EPROM, Mounting brackets (L-shaped/Flat type)	SCY-P0R20E

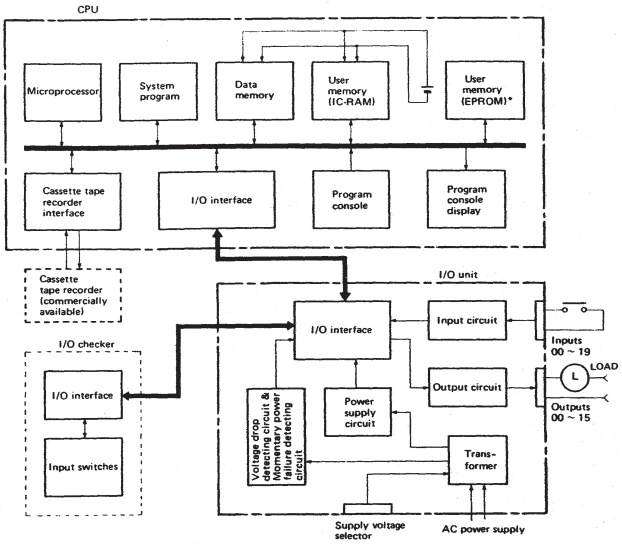
■ COMPONENTS AND OPTIONS (FOR SUPPLY INDIVIDUALLY)

Classification	Specification	Type
CPU	Program memory: IC-RAM with battery Weight: Approx. 1kg max.	SCYP0R-CPU10E
CPU	Program memory: IC-RAM with battery Weight: Approx. 1kg max. EPROM Weight: Approx. 1kg max.	SCYP0R-CPU20E
I/O unit	Weight: Approx. 4.6kg max.	SCYP0R-I/O01E
Connecting cable	For connection between CPU and I/O unit: 20cm Weight: Approx. 10g	SCYP0R-CN020
Connecting cable	For connection between CPU and I/O unit: 300cm Weight: Approx. 65g	SCYP0R-CN300
I/O checker	For program debugging Weight: Approx. 500g	SCYP0R-CHK01
Cassette interface cord	For connection between CPU and cassette tape recorder Weight: Approx. 50g	SCYP0R-PLG01
L-shaped mounting bracket	A pair of brackets supplied as a set Weight: Approx. 55g	SCYP0R-PAT01
Flat type mounting bracket	A pair of brackets supplied as a set Weight: Approx. 140g	SCYP0R-PAT02
EPROM chip*	Weight: Approx. 10g	ROM-F
Battery	3V lithium battery with connector Weight: Approx. 18g	SCY-BAT01

NOTE: * OMRON offers Type ROM-F (equivalent to 2716) developed under strict quality control as the EPROM (1K) chip for OMRON Programmable Controller series. Be sure to use this EPROM chip for the OMRON Programmable Controllers.

2.2 System Configuration

The system block diagram of the Type SCY-P0R20E (RAM & ROM type) is shown below.



NOTE: * Type SCY-P0R10E (RAM type) is not provided with a user memory (EPROM).

2.3 Specifications

■ RATINGS

Supply voltage	AC 110, 120, 220, or 240V, 50/60Hz*
Operating voltage	85 to 110% of rated voltage**
Power consumption	55VA max.
Insulation resistance	20MΩ min. at DC 500V (between external terminal and outer casing)
Dielectric strength	AC 1,500V, 50/60Hz for 1 minute (between external terminal and outer casing)
Noise immunity	1,000Vp-p Rise time: 1nsec; Pulse width: 2μsec
Vibration	16.7Hz, 3-mm double amplitude for 2 hrs.
Shock	10G's (in X, Y, Z directions, respectively 3 times)
Ambient temperature	Operating: 0 to +50°C Storage: −10 to +70°C
Humidity	30 to 90% RH (without condensation)
Atmosphere	Must be free from corrosive gases
Structure	Package type (CPU and I/O unit are separable)
Colorings	CPU sides: Dark gray CPU front: Aluminum hairline process I/O unit: Dark gray
Weight	CPU: 1.1kg max. I/O unit: 4.6kg max.

NOTE: * Set the voltage selector socket to the required voltage.
** A momentary power failure of less than ½ cycle is ignored by the programmable controller. If a momentary power failure of ½ to 1 cycles occurs, the power failure condition may or may not be detected by the programmable controller since it is in an unstable area. If a power failure of more than 1 cycle occurs, the programmable controller detects the power failure.

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■ CHARACTERISTICS

Control system	Stored program system
Main control element	LSI, TTL, C-MOS
Programming system	Ladder diagram
Instruction word length	16 bits/word
Number of instructions	13 kinds
Scan time	21msec max./256 words
Programming capacity	RAM: 256 words EPROM: 256 words x 4
Number of input points	20 points (Relay Nos. 00 ~ 19)
Number of output points	16 points (Relay Nos. 00 ~ 15)
Number of internal auxiliary relays	59 points (Relay Nos. 00 ~ 58)
Number of special auxiliary relays	5 points (Relay Nos. 59 ~ 63) • 59: Turns ON for 1 scan time when power is applied • 60: 0.1sec clock • 61: 1sec clock • 62: Turns ON when the battery is abnormal • 63: Turns ON when the memory is abnormal
Number of latching relays	47 points (Relay Nos. 00 ~ 46)
Number of temporary relays	1 point (Relay No. 47) When relay No. 47 is set, all outputs are inhibited and the output display goes out.
Number of timers and counters	10 points (Relay Nos. 0 ~ 9) respectively Timer: 0.1 ~ 25.5sec Counter: 1 ~ 255 counts
Timer accuracy	(Set value x ±1%) + (±50msec)
Counter response speed	10Hz max.
Memory protection function during power failure	Status data of respective latching relays and counters before the power failure are retained in the memory.
Diagnostic functions	Memory failure (Sum check) CPU failure (Watchdog timer) Battery failure (Battery not loaded, battery voltage drop) Program check • Coil duplication check • END instruction check • Circuit error check (syntax check)

■ INPUT

Input type	No-voltage contact input (photocoupler isolation)
Input voltage	DC 20V (built-in power supply)
Input current	10mA
Input operation level	ON: 5mA min. OFF: 2mA max.
Input response speed	7 to 14msec
Input impedance	1.8kΩ
Input common configuration	10 points/common (terminal block connector)
Operation indicators	LED's on the front panel of the CPU (The corresponding LED illuminates when the input is ON.)

■ OUTPUT

Output type	Relay (SPST-NO) contact output (no-voltage)
Model	OMRON Type MY2*
Rated load	DC 30V/AC 250V 2A, resistive load DC 30V/AC 250V 0.8A, inductive load
Output common configuration	4 points/common (terminal block connector)**
Operation indicators	LED's on the front panel of the CPU (The corresponding LED illuminates when the output is ON.)

NOTES: * Interchangeable with OMRON Model G3F solid-state relay.
** 7A max. per common terminal.

■ DIAGNOSTIC FUNCTIONS

As the diagnostic functions of the SYSMAC-P0R, checks on the items listed in the following tables are performed in the PROGRAM and RUN modes, respectively.

• PROGRAM mode

Diagnostic function: Item	Title	Function	Error indication	Error location
Program check	Coil duplication check	Checks coil numbers for duplication.	ON	C
	END instruction check	Checks the presence of END instruction at the end of the program.	ON	9
	Circuit error check	Checks the ladder diagram for proper configuration.	ON	U
	Program over check	Checks if the number of program instructions exceeds the memory capacity (i.e., 256 words) in Insert operation.	–	–

NOTE: In the "Program Over" condition, entries by the Insert key will be ignored.

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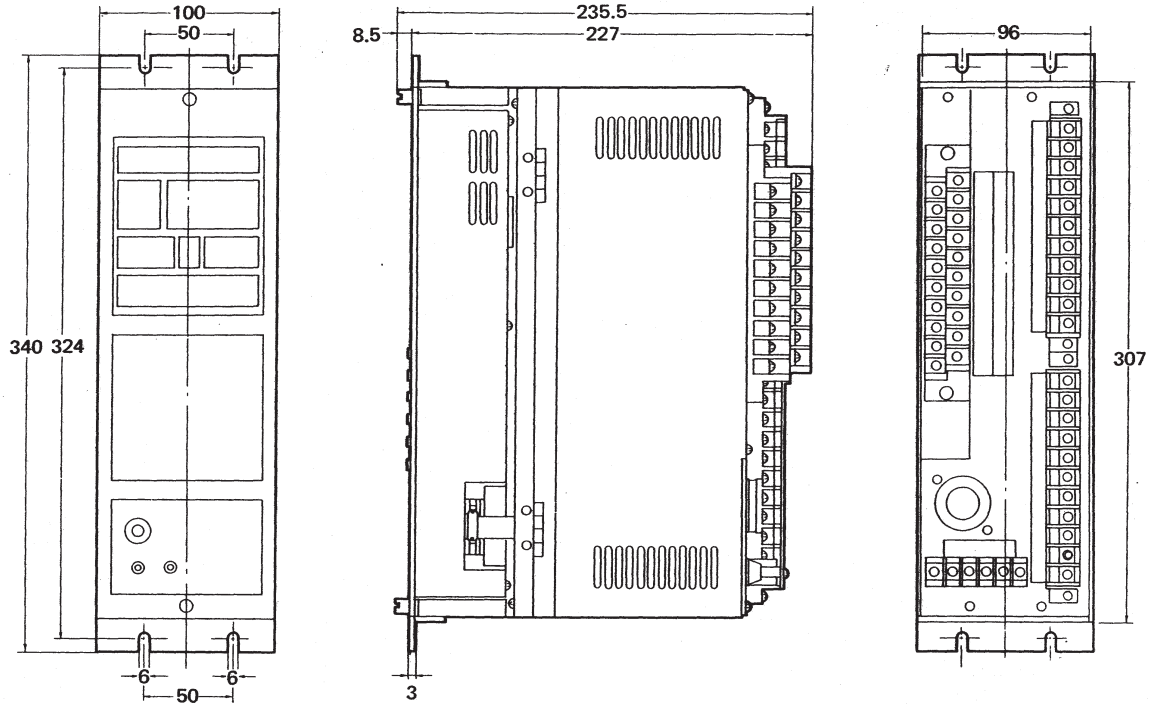
- **RUN mode**

Item	Diagnostic function	Error detection	Indication		Status of program execution	Special internal auxiliary relay
			RUN indicator	BAT indicator		
Program memory	Sum check	ON	Flashes ON/OFF	–	Continue	MR63: ON
Lithium battery*	Rated voltage check Battery loading check	–	ON	ON	Continue	MR62: ON
CPU failure	Watchdog timer	ON	OFF	–	Stop (all outputs will be turned OFF)	–

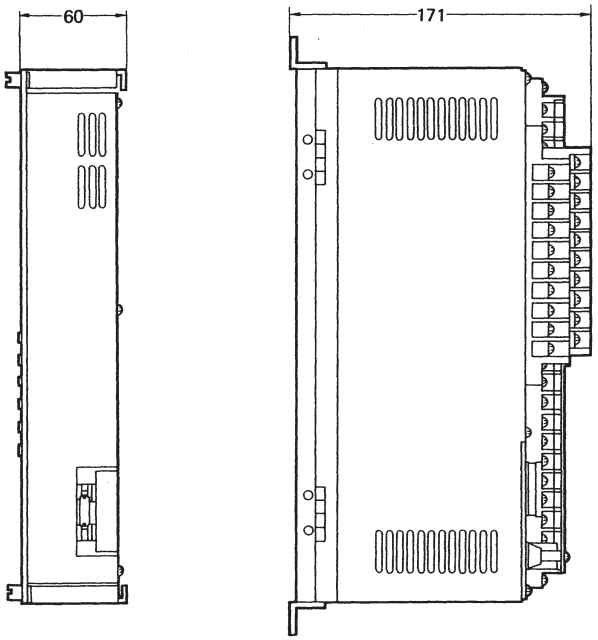
NOTE: * The lithium battery checks are performed in all the modes. After the BAT indicator illuminates, be sure to replace the battery within a week, or the contents of the program memory will be destroyed.

2.4 Dimensions

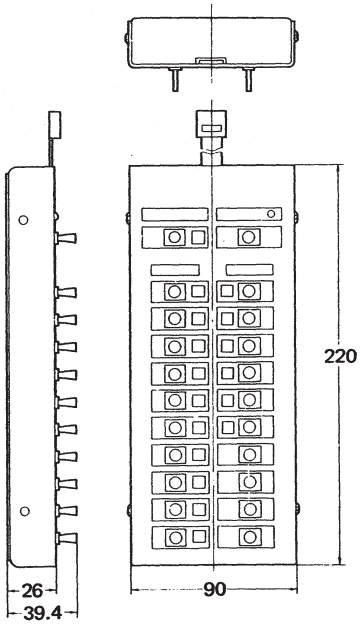
- **Programmable controller (with CPU and I/O unit integrated)**



- **Programmable controller (with CPU and I/O separated)**



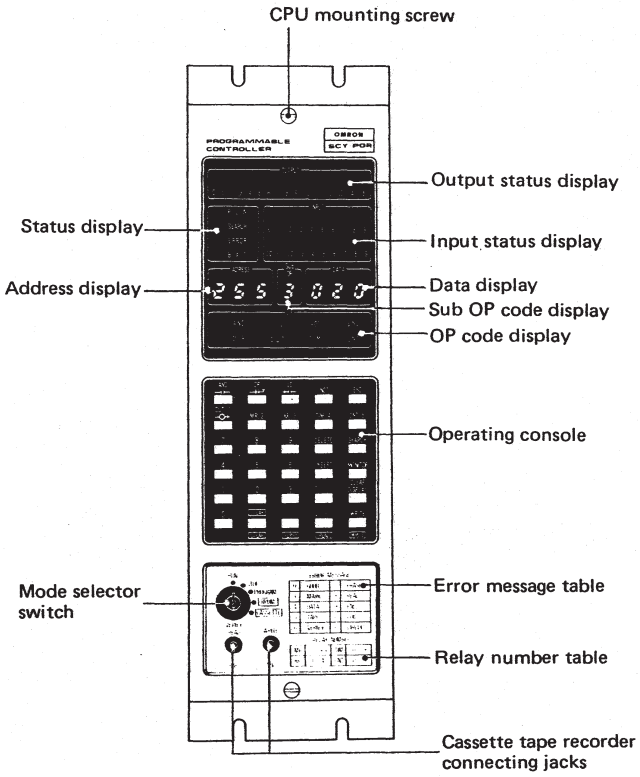
- **I/O checker**



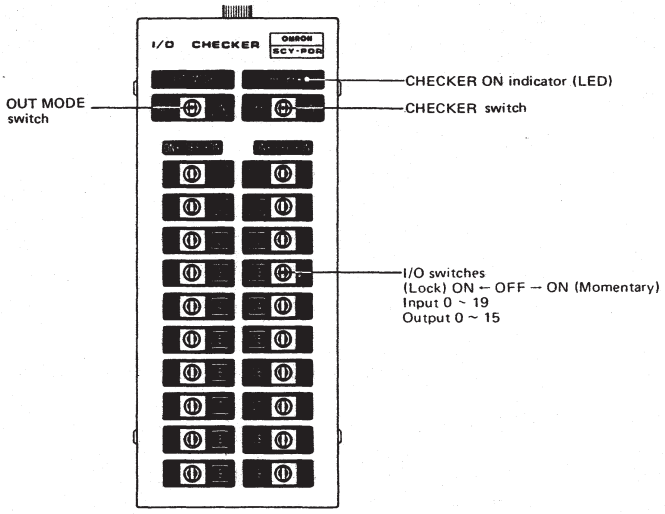
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2.5 Names of Respective Parts

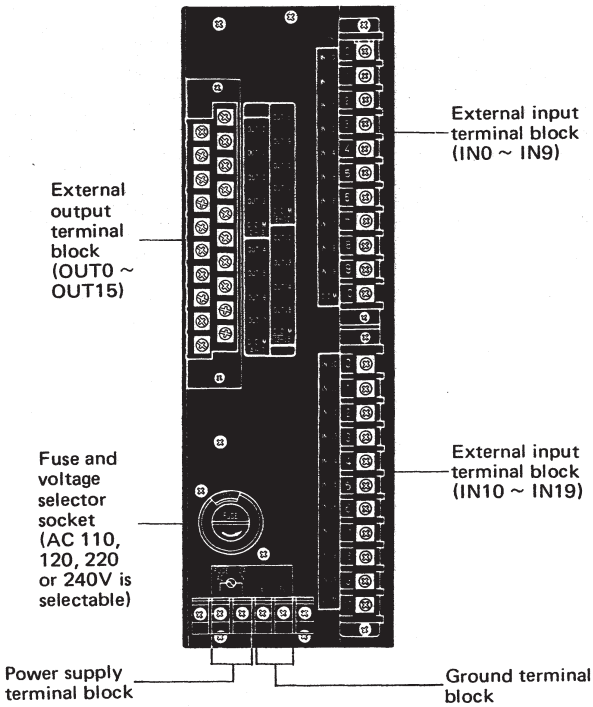
- **Front panel of CPU**



- **I/O checker**



- **Rear panel of I/O unit**



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3. Assignment of Relay Numbers

Relay numbers correspond to the data memory areas and the operation (ON/OFF state) of each relay is stored in the corresponding memory area.
The method of assigning relay numbers used for the SYSMAC-P0R is as follows.

3.1 List of Relay Numbers

Name	No. of points	Relay number									
Input relay	20	00	01	02	03	04	05	06	07	08	09
		10	11	12	13	14	15	16	17	18	19
Output relay	16	00	01	02	03	04	05	06	07	08	09
		10	11	12	13	14	15				
Internal auxiliary relay	59	00	01	02	03	04	05	06	07	08	09
		10	11	12	13	14	15	16	17	18	19
		20	21	22	23	24	25	26	27	28	29
		30	31	32	33	34	35	36	37	38	39
		40	41	42	43	44	45	46	47	48	49
		50	51	52	53	54	55	56	57	58	
Latching relay	40	00	01	02	03	04	05	06	07	08	09
		10	11	12	13	14	15	16	17	18	19
		20	21	22	23	24	25	26	27	28	29
		30	31	32	33	34	35	36	37	38	39
		40	41	42	43	44	45	46			
Timer	10	0	1	2	3	4	5	6	7	8	9
Counter	10	0	1	2	3	4	5	6	7	8	9

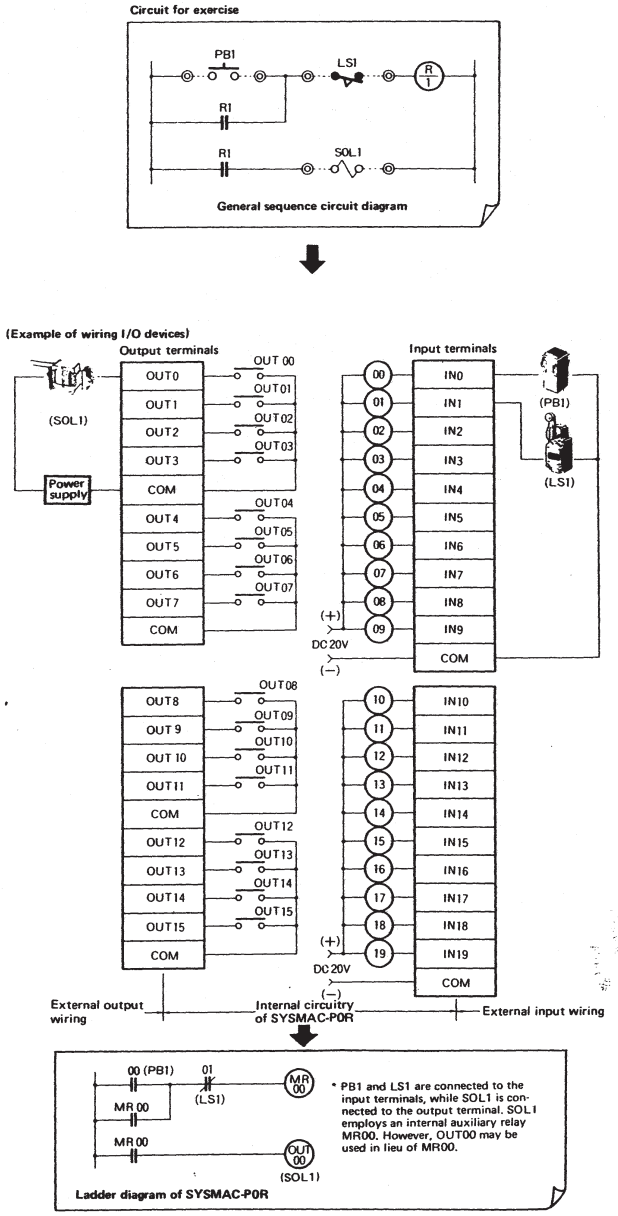
Name	No. of points	Relay number	Description
Special auxiliary relay	7	59	This relay operates for 1 scan time when power is applied.
		60	This relay is used for 0.1sec clock.
		61	This relay is used for 1sec clock.
		62	This relay operates when a battery failure occurs.
		63	This relay operates when a memory failure occurs.
Special latching relay	1	47	When this relay operates, all output are inhibited and all output indicators go out.

- With the SYSMAC-P0R, relay numbers other than above cannot be used. For setting the timer and counter values, values higher than 255 cannot be used.

3.2 Determination of I/O Relay Numbers

1. In a sequence circuit diagram which is generally known, a sequence circuit is drawn with input/output devices included and I/O device symbols and relay numbers are arbitrarily determined. However, since the SYSMAC-P0R cannot recognize such arbitrary I/O device symbols and relay numbers, it is necessary to determine the I/O terminals to which I/O devices are to be connected.

2. The ladder diagrams of the SYSMAC-P0R require the relay numbers corresponding to the I/O devices. The relay numbers are determined by the locations (I/O terminals) of I/O terminal blocks to which the I/O devices are connected. Each of these relay numbers must be used for ladder diagrams and programming.



3.3 Determination of Internal Auxiliary Relay Numbers

The SYSMAC-P0R has 59 internal auxiliary relays which are used for internal data transfer. They are independent of I/O devices in sequence. Since the internal auxiliary relays are the data memories incorporated in the CPU, no wiring to the I/O terminals is required. (In other words, they cannot be used as contact outputs.)

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- **Internal auxiliary relay numbers**

00	01	02	03	04	05	06	07	08	09
10	11	12	13	14	15	16	17	18	19
20	21	22	23	24	25	26	27	28	29
30	31	32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47	48	49
50	51	52	53	54	55	56	57	58	

NOTES: 1. Relay numbers 00 ~ 58 may not necessarily be assigned consecutively.
2. When using an internal auxiliary relay, the letters "MR" must be prefixed to the relay number (e.g. MR00).
3. Relay coil number cannot be used in duplication. However, the number of relay contacts is not limited for use.
4. If more than 59 internal auxiliary relays are required, output relay numbers of the output terminals to which output devices are not connected may be used as internal auxiliary relay numbers.

3.4 Determination of Special Auxiliary Relay Numbers

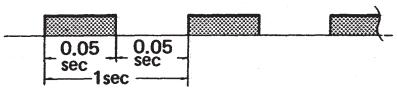
5 special auxiliary relays are provided. These relays are sort of internal auxiliary relays which operate and release according to the internal conditions controlled by hardware and are independent of the I/O devices in sequence.

- **Special auxiliary relay numbers**

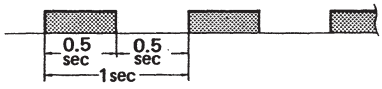
59	60	61	62	63

59: This relay operates for 1 scan time when the mode selector switch is changed from STOP to RUN after power application in the RUN mode. Use of this relay is recommended to generate a signal to reset latching relays, counters, etc. upon power application.

60: This relay is used to generate 0.1sec clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure. The relay output can also be used as a flicker signal.



61: This relay is used to generate 1sec clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure. The relay output can also be used as a flicker signal.



62: This relay operates when a battery failure occurs and releases when the battery is returned to normal. When this relay operates, the BAT indicator on the front panel of the CPU illuminates. These relay outputs cannot be transmitted directly to an output terminal. If any of the relay outputs is desired to be transmitted externally, prepare and program a circuit so that the relay output is transmitted externally through an output relay. (Refer to paragraph 5.2.5, Applied Programs.)

63: This relay operates when a memory failure occurs. To release this relay, change the mode selector switch position or turn off the power. These relay outputs cannot be transmitted directly to an output terminal. If any of the relay outputs is desired to be transmitted externally, prepare and program a circuit so that the relay output is transmitted externally through an output relay. (Refer to paragraph 5.2.6, Applied Programs.)

NOTES: 1. When using any special auxiliary relay, the letters "MR" must be prefixed to the relay number (e.g., MR59).
2. Special auxiliary relays cannot be used as output relays. However, the number of these relay contacts is not limited for use.

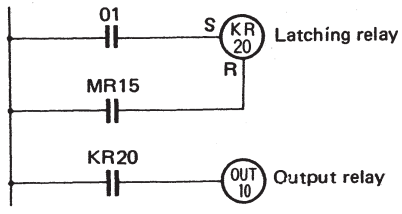
3.5 Determination of Latching Relay Numbers

The SYSMAC-P0R has 47 latching relays whose operating states before a power failure can be retained in the memory. Since the operating states of these relays are stored in the memory, all their outputs at the time of the power failure are turned off, but the relays will return to the state before the power failure when power is applied again. Memory retention time after a power failure is about 2 years just the same as that of the program memory.

- **Latching relay numbers**

00	01	02	03	04	05	06	07	08	09
10	11	12	13	14	15	16	17	18	19
20	21	22	23	24	25	26	27	28	29
30	31	32	33	34	35	36	37	38	39
40	41	42	43	44	45	46			

NOTES: 1. Relay numbers 00 ~ 46 may not necessarily be assigned consecutively.
2. When using a latching relay, the letters "KR" must be prefixed to the relay number.
3. Relay coil numbers cannot be used in duplication. However, the number of relay contacts is not limited for use.
4. When set and reset input signals are applied simultaneously, the reset input signal takes precedence over the set input signal.
5. These relay outputs cannot be transmitted directly to an output terminal. If any of the relay outputs is desired to be transmitted externally, prepare and program a circuit so that the relay output is transmitted externally through an output relay.



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3.6 Determination of Special Latching Relay Number

The SYSMAC-P0R has only one special latching relay whose relay number is KR47. When the KR47 operates, all output relays are disabled, causing their outputs to turn off and all the operation indicators of the output relays to be extinguished. At this time, the RUN indicator flashes. When the KR47 releases, the output relays are put in the ON or OFF state depending on the program conditions at that time, causing the operation indicators of the output relays to be illuminated or extinguished accordingly. At this time, the RUN indicator changes from the flashing state to the illuminated state.

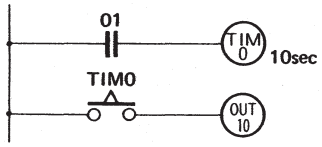
3.7 Determination of Timer Numbers

The SYSMAC-P0R has 10 timers which are used for timer numbers in programming.

- **Timer numbers**

0	1	2	3	4	5	6	7	8	9

NOTES:
1. Timer numbers 0 ~ 9 may not necessarily be assigned consecutively.
2. When using a timer, the letters "TIM" must be prefixed to the timer number (e.g., TIM0).
3. Timer coil numbers cannot be used in duplication. However, the number of timer contacts is not limited for use.



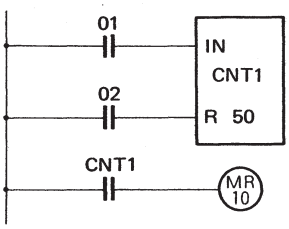
3.8 Determination of Counter Numbers

The SYSMAC-P0R has 10 counters which are used as counter numbers in programming.

- **Counter numbers**

0	1	2	3	4	5	6	7	8	9

NOTES:
1. Counter numbers 0 ~ 9 may not necessarily be assigned consecutively.
2. When using a counter, the letters "CNT" must be prefixed to the counter number (e.g., CNT1).
3. Counter coil numbers cannot be used in duplication. However, the number of counter contacts is not limited for use..



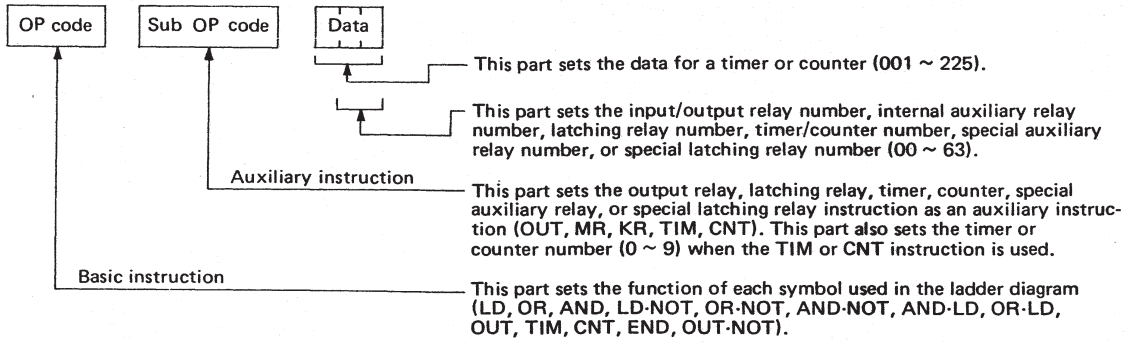
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4. Instruction Words

A sequence circuit is programmed according to the ladder diagram instruction words provided for the SYSMAC-P0R. In this chapter, usages of ladder diagrams and ladder diagram instruction words are described.

4.1 Configuration of Instruction Words

Each instruction word used in the SYSMAC-P0R consists of the following 3 blocks.



4.2 List of Instructions

- **Basic instructions (OP codes)**

No.	Instruction	Symbol	Function	Data
1	LOAD	LD	Logical start operation.	Input relays 00 ~ 19 Output relays 00 ~ 15 Internal auxiliary relays 00 ~ 58 Latching relays 00 ~ 46 Timers 0 ~ 9 Counters 0 ~ 9 Special auxiliary relays 59 ~ 63 Special latching relay 47
2	LOAD NOT	LD NOT	Logical NOT start operation.	
3	AND	AND	Logical AND operation.	
4	AND NOT	AND NOT	Logical AND NOT operation.	
5	OR	OR	Logical OR operation.	
6	OR NOT	OR NOT	Logical OR NOT operation.	
7	AND LOAD	AND LD	Logical AND operation with the condition of the preceding block.	——
8	OR LOAD	OR LD	Logical OR operation with the condition of the preceding block.	
9	OUT	OUT/1	Outputs the result of a logical operation to the specified output relay, internal auxiliary relay, or latching relay.	Output relays 00 ~ 15 Internal auxiliary relays 00 ~ 58 Latching relays 00 ~ 46
10	OUT NOT	OUT/1 NOT	Inverts the results of a logical operation and then outputs them to the specified output relay, internal auxiliary relay or latching relay.	
11	TIMER	TIM/4	On-delay timer operation.	Timer Nos. 0 ~ 9 Counter Nos. 0 ~ 9 Setting value 001 ~ 255
12	COUNTER	CNT/5	Down counter operation.	
13	END	END	The end of a program.	——

- **Auxiliary instructions (Sub OP codes)**

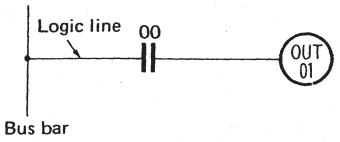
No.	Instructions	Symbol	Function	Data
1	Internal auxiliary relay	MR/2	Indicates an internal auxiliary relay.	Internal auxiliary relays 00 ~ 58
2	Latching relay	KR/3	Indicates a latching relay	Latching relays 00 ~ 46

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4.3 Explanation of Instruction Words

■ LOAD (LD) & OUTPUT (OUT) INSTRUCTIONS

If each logic line starts with an NO contact, use the LD instruction. Use the OUT instruction for a relay coil.



Coding

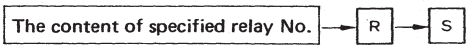
Address	OP	Sub OP	Data
000	LD		00
001	OUT		01

Contents of Registers

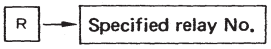
R	S
00	—
00	—

- **Operation of each register**

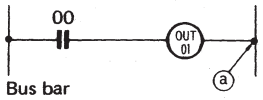
The LD instruction causes the content (ON or OFF state) of the specified relay number to be stored into the RESULT REGISTER (hereafter referred to as "R register"). It also causes the previous result in the R register to be transferred to the STACK REGISTER (hereafter referred to as "S register").



The OUT instruction causes the content of the R register to be output to the specified relay number. In this case, the content of the R register will remain unchanged.



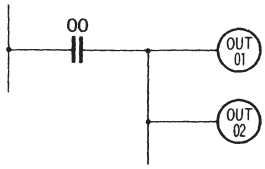
- Bus bar of a different phase is not required to be programmed.



Connection to the bus bar of a different phase (part ⓐ) is accomplished automatically by programming an OUT instruction.

- **Consecutive OUT instructions**

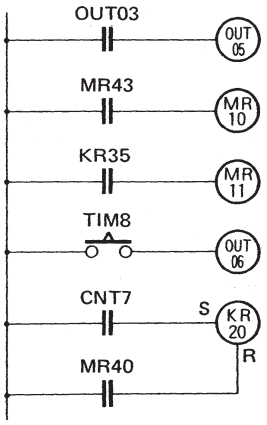
If the OUT instruction is followed by another OUT instruction, this condition is regarded as a circuit error during the program check. However, each output relay operates normally.



Coding

OP	Sub OP	Data
LD		00
OUT		01
OUT		02
⋮		⋮

- The LD instruction is used for any NO contact at the start of each logic line.



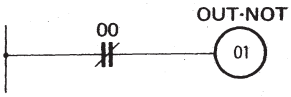
Coding

OP	Sub OP	Data
LD	OUT/1	03
OUT		05
LD	MR/2	43
OUT	MR/2	10
LD	KR/3	35
OUT	MR/2	11
LD	TIM/4	8
OUT		06
LD	CNT/5	7
LD	MR/2	40
OUT	KR/3	20
⋮	⋮	⋮

- The OUT instruction is used when an output relay, internal auxiliary relay, or latching relay is employed.

■ LOAD NOT (LD·NOT) & OUTPUT NOT (OUT·NOT) INSTRUCTIONS

If each logic line starts with an NC contact, use the LD·NOT instruction in lieu of the LD instruction. Use the OUT·NOT instruction to invert the output condition.



Coding

Address	OP	Sub OP	Data
000	LD·NOT		00
001	OUT·NOT		01

Contents of Registers

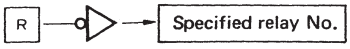
R	S
00	—
00	—

- **Operation of each register**

The LD·NOT instruction causes the content of the specified relay number to be inverted and then stored into the R register.

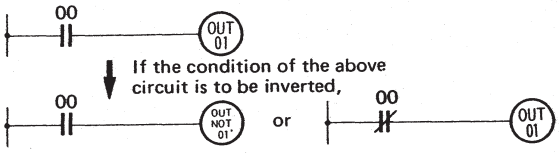


The OUT·NOT instruction causes the content of the R register to be inverted and then output to the specified relay number. In this case, the content of the R register will remain unchanged.



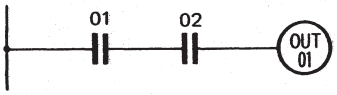
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- The LD·NOT instruction is used for any NC contact at the start of each logic line.
- The OUT·NOT instruction may be used when an output relay, internal auxiliary relay, or latching relay is employed.
- Normally, the OUT·NOT instruction is not used. However, the instruction may be applied in the following case.



■ AND INSTRUCTION

NO contacts in series are processed by the AND instruction.



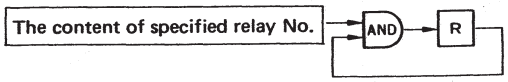
Coding

000	LD		01
001	AND		02
002	OUT		01

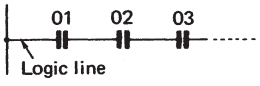
Contents of Registers

01	—
01 02	—
01 02	—

- **Operation of each register**
  The AND instruction causes the logical AND operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical AND operation will be newly stored in the R register.



- **Number of contacts**
  The number of contacts is not limited for use on a logic line. As many NO contacts as required can be connected by means of the [AND] key.

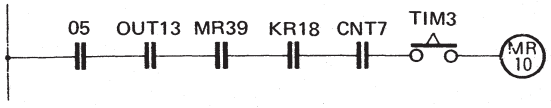


Coding

LD		01
AND		02
AND		03
⋮	⋮	⋮

In this case, the contact of the first relay number 01 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD01."

- The AND instruction is a series connection instruction and is used when all the contacts to be connected in series are NO contacts.

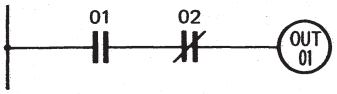


Coding

OP	Sub OP	Data
LD		05
AND	OUT/1	13
AND	MR/2	39
AND	KR/3	18
AND	CNT/5	7
AND	TIM/4	3
OUT	MR/2	10

■ AND NOT INSTRUCTION

If an NC contact is connected in series, use the AND·NOT instruction in lieu of the AND instruction.



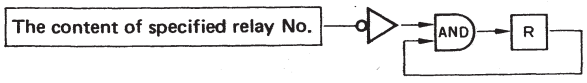
Coding

000	LD		01
001	AND·NOT		02
002	OUT		01

Contents of Registers

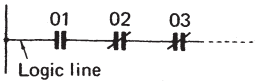
01	—
01 02	—
01 02	—

- **Operation of each register**
  The AND·NOT instruction causes the content of the specified relay number to be inverted and then ANDed with the content of the R register. The result of the logical AND operation will be newly stored in the R register.



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- **Number of contacts**
  The number of contacts is not limited for use on a logic line. As many NC contacts as required can be connected in series by means of [AND] [NOT] keys.



Coding

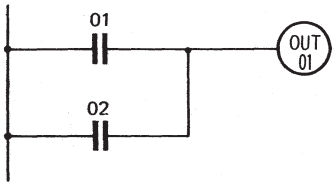
LD		01
AND·NOT		02
AND·NOT		03
⋮		⋮

In this case, the contact of the first relay number 01 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD01."

- The AND·NOT instruction is a series connection instruction and is used when all the contacts to be connected in series are NC contacts.

■ OR INSTRUCTION

NO contacts in parallel are processed by the OR instruction.



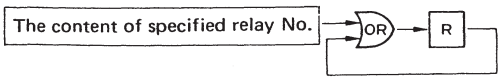
Coding

000	LD		01
001	OR		02
002	OUT		01

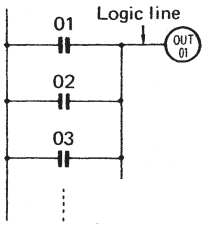
Contents of Registers

01	—
01 02	—
01 02	—

- **Operation of each register**
  The OR instruction causes the logical OR operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical OR operation will be newly stored in the R register.



- **Number of contacts**
  The number of contacts is not limited for use on a logic line. As many NO contacts as required can be connected by means of [OR] key.



Coding

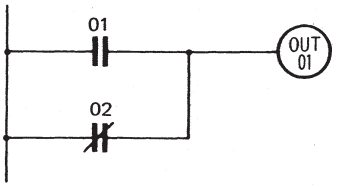
LD		01
OR		02
OR		03
⋮		⋮
OUT		01

In this case, the contact of the first relay number 01 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD01."

- The OR instruction is a parallel connection instruction and is used when all the contacts to be connected in parallel are NO contacts.

■ OR·NOT INSTRUCTION

If an NC contact is to be connected in parallel, use the OR·NOT instruction in lieu of the OR instruction.



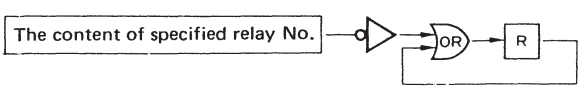
Coding

000	LD		01
001	OR·NOT		02
002	OUT		01

Contents of Registers

01	—
01 02	—
01 02	—

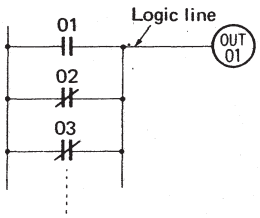
- **Operation of each register**
  The OR·NOT instruction causes the content of the specified relay number to be inverted and then ORed with the content of the R register. The result of the logical OR operation will be newly stored in the R register.



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- **Number of contacts**

  The number of contacts is not limited for use on a logic line. As many NC contacts as required can be connected by means of [OR] [NOT] keys.



Coding

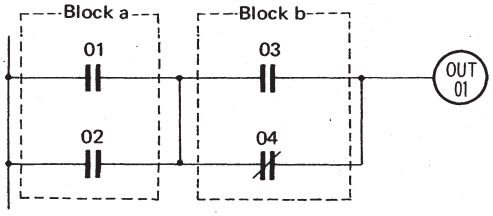
OP	Sub OP	Data
LD		01
OR·NOT		02
OR·NOT		03
⋮		⋮
OUT		01

  In this case, the contact of the first relay number 01 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD01."

- The OR·NOT instruction is a parallel connection instruction and is used when all the contacts to be connected in parallel are NC contacts.

■ AND·LOAD (AND·LD) INSTRUCTION

For inter-block AND operation between two or more blocks, use the AND·LD instruction.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	OR		02
002	LD*		03
003	OR·NOT		04
004	AND·LD**		
005	OUT		01

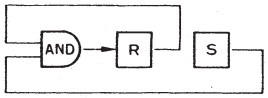
Contents of Registers

R	S
01	—
01 02	—
03	01 02
03 04	01 02
01 03 02 04	—
01 03 02 04	—

NOTES: * Use this instruction as the first instruction for the next block to be ANDed with the preceding block.
** Use the AND·LD instruction for series connection of two blocks (blocks "a" and "b").

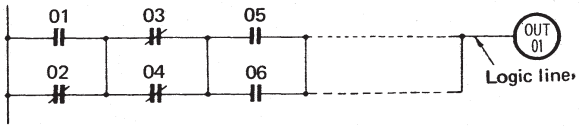
- **Operation of each register**

  1. By the LD01 and OR02 instructions, the result of the logical OR operation in block "a" is stored into the R register.
  2. By the LD03 instruction in block "b", the result of the operation in block "a" is transferred into the S register, while the result of the logical operation by instructions LD03 and OR·NOT04 in block "b" is stored into the R register.
  3. AND·LD instruction causes the logical AND operation to be performed between the R register and the S register. The result of the logical AND operation will be newly stored in the R register.



- **Number of blocks**

  The number of blocks is not limited for AND·LD operation on a logic line. As many blocks as required can be continued for series connection by means of [LD] ~ [AND] [LD] keys.



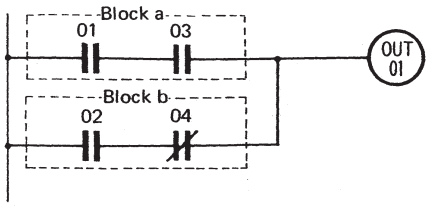
Coding

OP	Sub OP	Data
LD		01
OR·NOT		02
LD·NOT		03
OR·NOT		04
AND·LD		—
LD		05
OR		06
AND·LD		—
⋮		⋮
OUT		01

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■ OR-LOAD (OR-LD) INSTRUCTION

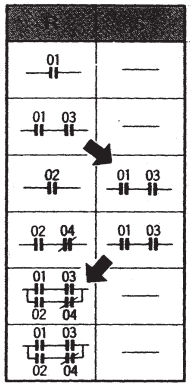
For inter-block OR operation between two or more blocks, use the OR-LOAD instruction.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND		03
002	LD*		02
003	AND-NOT		04
004	OR-LD**		
005	OUT		01

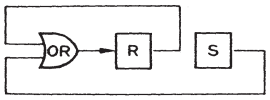
Contents of Registers



NOTES: * Use this LD instruction as the first instruction of the next block to be ORed with the preceding block.
** Use the OR-NOT instruction for parallel connection of two blocks (blocks "a" and "b").

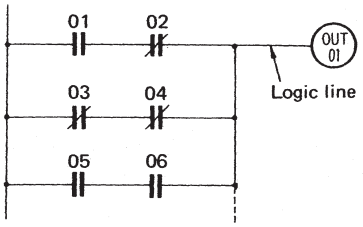
- **Operation of each register**

1. By the LD01 and AND03 instructions, the result of the logicla AND operation in block "a" is stored into the R register.
2. By the LD02 instruction in block "b", the result of the operation in block "a" is transferred into the S register, while the result of the logical operation by instructions LD02 and AND-NOT04 in block "b" is stored into the R register.
3. The OR-LD instruction causes the logical OR operation to be performed between the R register and the S register. The result of the logical OR operation will be newly stored into the R register.



- **Number of blocks**

The number of blocks is not limited for OR-LD operation on a logic line. As many blocks as required can be continued for parallel connection by means of LD ~ OR, LD keys.

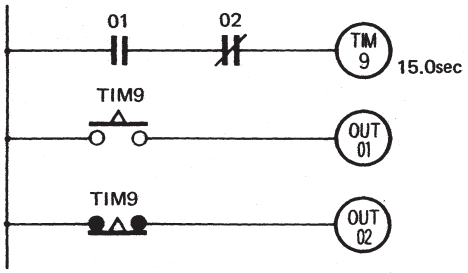


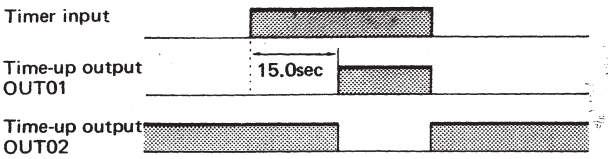
Coding

OP	Sub OP	Data
LD		01
AND-NOT		02
LD-NOT		03
AND-NOT		04
OR-LD		—
LD		05
AND		06
OR-LD		—
⋮		⋮
OUT		01

■ TIMER (TIM) INSTRUCTION

The TIM instruction can be used as an ON-delay timer in the same manner as a relay circuit.





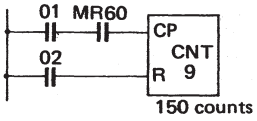
Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND-NOT		02
002	TIM	9*	150**
003	LD	TIM/4	9
004	OUT		01
005	LD-NOT	TIM/4	9
006	OUT		02

NOTES: * Timer number 0 ~ 9.
** Time setting value 001 ~ 255 x 0.1sec

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- **Operation of each register**
  The timer starts when the content of the R register is logical 1 and resets when the content of the R register is logical 0.
- **Number of contacts**
  A time-up contact designates the timer number itself. Both NO and NC contacts can be used in the required quantity.
- **Timer is of decrementing type**
  The timer is of a decrementing type which produces an output when the present value (time remaining) becomes "000." When the timer input is turned off, the present value of the timer returns to the preset value. The timer output is transmitted externally through an output relay as shown in the above circuit example.
- **Timer is reset at the time of a power failure**
  If a power failure occurs, the timer is reset and the present value returns to the preset value. Therefore, if it is required to retain the present value of the timer in the memory, a memory retentive type timer circuit as shown below must be used for programming.
- **Memory retentive type timer**
  A circuit to memorize the present value of the timer during a power failure is configured using a combination of clock instruction and counter (CNT) instruction.

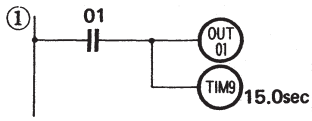


Coding

LD		01
AND	MR/2	60
LD		02
CNT	9	150

NOTE: Timer contact MR60 is for 0.1sec clock. (Use timer contact MR61 for 1sec clock.)

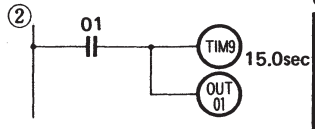
- **Consecutive OUT instruction and TIM instruction**
  If the OUT instruction is followed by the TIM instruction, this condition is regarded as a circuit error during the program check. However, they operate as follows.



Coding

LD		01
OUT		01
TIM	9	150

When the NO contact 01 turns ON, output relay 01 is energized and at the same time timer 9 starts operating.



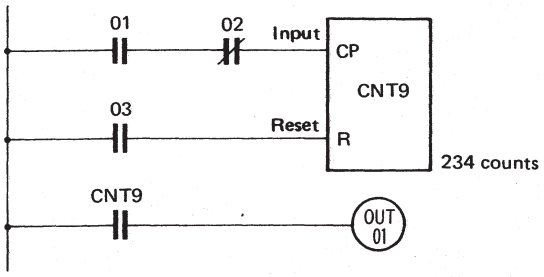
Coding

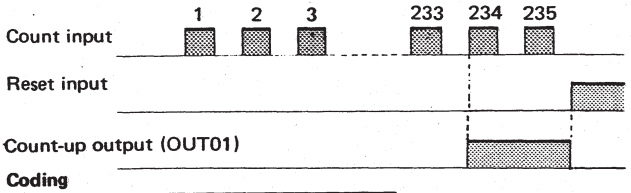
LD		01
TIM	9	150
OUT		01

When the NO contact 01 turns ON, timer 9 starts operating and at the same time, output relay 01 is energized.

■ COUNTER (CNT) INSTRUCTION

The CNT instruction can be used as a preset counter in the same manner as a relay circuit.





Coding

000	LD		01
001	AND-NOT		02
002	LD		03
003	CNT	9*	234**
004	LD	CNT/5	9
005	OUT		01

NOTES: 1. A counter program must be entered in the order of a count input circuit, a reset input circuit and a counter coil.
2. Counter number 0 ~ 9.
3. Counter setting value 001 ~ 255.

- **Operation of each register**
  The counter resets when the content of the R register is logical 1 and is enabled to count when the content of the R register is logical 0. A count input is provided from the S register.
- **Number of contacts**
  A count-up contact designates the counter number itself. Both NO and NC contacts can be used in the required quantity.
- **Counter is of decrementing type**
  The counter is of a decrementing type which produces an output when the count value becomes "000." The present value of the counter returns to the preset value when a reset input is applied. The counter output is transmitted externally through an output relay as shown in the above circuit example.
- After the preset count is up, subsequent count inputs are ignored.

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