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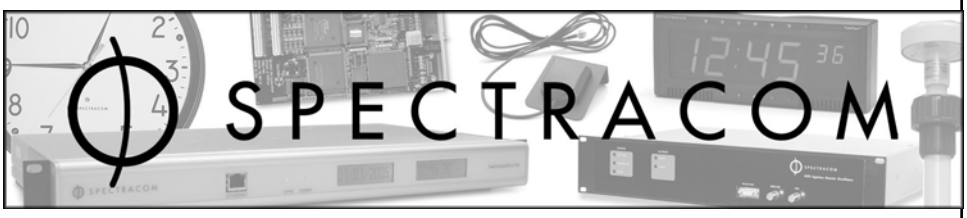
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TPRO/TSAT PCI-U-2/-66U
SYNCHRONIZABLE TIMECODE GENERATOR with UNIVERSAL PCI BUS INTERFACE

User Manual

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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1 Overview

This manual provides comprehensive information on the system architecture, specifications, and operation of the Spectracom TPRO and TSAT Synchronizable Time Code Generators with Universal PCI Bus Interface.

The TPRO is a precision clock that synchronizes automatically to standardized timecode signals (or, for the TSAT configuration, to the GPS satellite system) and can be read from the PC host computer.

Inputs to the TPRO are modulated timecode (or, for the TSAT, GPS receiver signals), host commands, and time tags.

Outputs are modulated IRIG-B timecode, programmable start/stop time, and a programmable "heartbeat" pulse rate.

The board can generate interrupts on the universal PCI bus (if enabled). Interrupt sources include the heartbeat, time tag, FIFO data available, and at the programmable start time.

The clock automatically synchronizes to specified timecode signals. A status bit advises the host of synchronization status. In the absence of timecode input or GPS, the board starts counting at 000 days, 00 hours, 00 minutes, 00 seconds at power-on. The clock time can also be set by user command.

1.1 General Information about GPS

NOTE: GPS applies only to the TSAT board. The TPRO is not equipped for GPS.

The United States government operates a set of approximately 32 satellites, collectively known as the "GPS Constellation" or "GPS Satellites." Each satellite has an internal atomic clock and transmits a signal specifying the time and satellite position. On the ground, the GPS receiver determines its position (longitude, latitude, and elevation) and the time by decoding the signals simultaneously from at least four of the GPS satellites.

The satellite orbits are circular, inclined approximately 56 degrees from the equator, orbiting the Earth once every 11 hours. There are several different orbital planes, providing continuous coverage to all places on Earth. The GPS receiver uses an omni-directional antenna; the satellites move slowly across the sky (they are not at fixed locations).

Each satellite transmits a spread-spectrum signal, centered at 1575.42 MHz. When power is first applied, the GPS receiver begins searching for the satellites. It does this by searching for each satellite individually, listening for each satellite's distinct spread-spectrum hopping sequence. This process can take a few minutes, as the receiver iteratively locates satellites, refines its position, and determines for which satellites to search.

The GPS receiver retains the last known position when the power is switched off. This results in faster satellite acquisition the next time it is switched on. If the antenna has been moved more than a few miles, however, acquisition time will be slightly longer because it must first re-compute the position.

1.2 Your Spectracom GPS Receiver

Your board's GPS receiver is built into the antenna housing and communicates to the board via a serial (RS-422) interface. Power (+12V) is supplied from the board. The unit comes with a 100-foot cable. Extension cables are available in 100-foot lengths. The maximum total length is 500 feet. The connectors on the extension cables are not weatherproof; only the first 100-feet can be outdoors. The cable consists of several twisted pairs (not coaxial cable) and a foil shield.

NOTE: Spectracom recommends applying an appropriate silcon grease to the cable connection at the GPS antenna in order to protect the connection from moisture. An additional weatherproofing kit (P/N 221213) containing butyl rubber and plastic tape is also available from Andrews Corporation, US 800.255.1479.

1.3 Distinguishing Between TPRO & TSAT Boards – Software

Examine the Subsystem Product ID number that is detailed in the "*Specifications*" section.

1.4 Inventory

Before installing the board, please verify that all material ordered has been received. The TSAT is delivered with a 100-foot cable with pre-installed connectors, a GPS receiver/antenna (housed together in a single enclosure), and a user manual. The TPRO is delivered with mating connector (15-pin) and a user manual. If there is a discrepancy, please contact Spectracom Customer Service at US 585.321.5800.

1.5 Inspection and Support

Unpack the equipment and inspect it for damage. If any equipment has been damaged in transit, please contact Spectracom Customer Service at US 585.321.5800.

If any problems occur during installation and configuration of your Spectracom product, please contact Spectracom Technical Support at US 585.321.5823 or US 585.321.5824.

CAUTION:  *Electronic equipment is sensitive to Electrostatic Discharge (ESD). Observe all ESD precautions and safeguards when handling the timecode generator.*

NOTE: If equipment is returned to Spectracom, it must be shipped in its original packing material. Save all packaging material for this purpose.

2 Specifications

NOTE: In this manual, the prefix "0x" indicates that the number is in hexadecimal (Base 16) format.

2.1 TPRO (Board Only)

Table 2.1—Time Code Input Specifications	
Code Format (autodetect)	IRIG-A (A132)*, IRIG-B (B122), NASA36
Amplitude	1.2 Vp-p min, 8.0 Vp-p max
Polarity	Detected automatically
Modulation Ratio	2:1 min, 3:1 typical, 4:1 max
Input Impedance	>10 K ohms
Timing Accuracy	Better than 100 ppm (not suitable for tape playback)
Common Mode Voltage	Differential input, ±100 V max

**Not supported with Option -M.*

Table 2.2—IRIG-B Output Specifications	
Code Format	IRIG-B (B122)
Amplitude (mark)	3.5 Vp-p (type)
Modulation Ratio	3:1
Output Impedance	600 ohms

Table 2.3—Time Tag Input Specifications	
Input Voltage	-0.5V min, +0.8V max for logic 0 +2.0V min, +5.5 max for logic 1 Tags rising edge
Input Current	<5 µA for logic 0 <5 µA for logic 1
Rise/Fall Time	500 nS max
Repetition Rate	1000 events per second max
Timing Resolution	1 µS

Table 2.4—1 PPS Sync Input Specifications (Option -M Only)	
Input Voltage	2.4 V min, 16.0 V max (high) (500 µA max at 5 Vin, 12 mA max at 16 Vin)
Rise/Fall Time	500 nS max
Trigger Edge	Rising
1PPS [H] Accuracy	Must be 100 ppm or better

[H] One pulse-per-second

Table 2.5—Match Output Specifications	
Output Voltage	3.8 V min at 6 mA (high) 0.4 V max at -6 mA (low)
Setability	1 µS

Table 2.6—On-board Clock Specifications	
Resolution	1 µS
Range	366:23:59:59.999999
Date Format	Integer (001-366)
Synchronization Time	<8 seconds
Stability	Disciplined to timecode: $1x10^{-6}$ Undisciplined: $2x10^{-7}$

Table 2.7—PCI Interface Specifications		
Model	**PCI-U-2**	**PCI-66U**
Interface	PCI Spec. 2.2 compliant	
Bus Speed	33MHz	33/66MHz
I/O	64 bytes	
DMA Transfers	None	
General	Occupies 32 consecutive 16-bit I/O and memory addresses (64 bytes)	
Chipset Vendor ID	0x10b5	0x1AD7
Chipset Product ID	0x9030	0x9100
Subsystem Vendor ID	0x1347	0x1AD7
Subsystem Product ID		
TPRO-PCI	0x9050 (standard)	0x9150 (standard)
TPRO-PCI-M	0x9051	0x9151
TPRO-PCI-HB1PPS	0x9052	0x9152
TPRO-PCI-FXB	0x9052	0x9152
TPRO-PCI-LOR1	0x9052	0x9152
TPRO-PCI-M-HB1PPS	0x9053	0x9153
TPRO-PCI-DCLOBNC	0x9050	0x9150
TSAT-PCI	0x9070 (standard)	0x9170 (standard)
TSAT-PCI-HB1PPS	0x9072	0x9172
TSAT-PCI-FXA	0x9072	0x9172
TSAT-PCI-DCLOBNC	0x9072	0x9172

Table 2.8—General Specifications	
Size	H 106.7 mm, L 174.6 mm (H 4.2”, L 6.875”)
Power (from PCI bus)	+5 VDC @ 425 mA max, +12 VDC @ 225 mA max, -12 VDC @ 50 mA max
Operating Temperature	-30 to +70 C (-22 to +158 F)
Storage Temperature	-40 to +80 C (-40 to +176 F)
Connectors	BNCs for timecode input and output; DB15 (socket) for timecode input, output, heartbeat output, match output, time-tag input, and 1 PPS input.

Table 2.9—Heartbeat Output Specifications	
Output Voltage	3.8 V min at 6 mA (high) 0.4 V max at -6 mA (low)
Wave Shape	Pulse or Square Wave (programmable)
Pulse Width	150 nS min, 450 nS max
Pulse Polarity	Negative
Square Wave	45% - 55%
Timing	Falling edge on-time (pulse or square wave)
Range	1.000 µS-21.845 mS in 1 µS steps (1 MHz - 45.7771 Hz)
Power-on default rate	100 PPS (pulse)

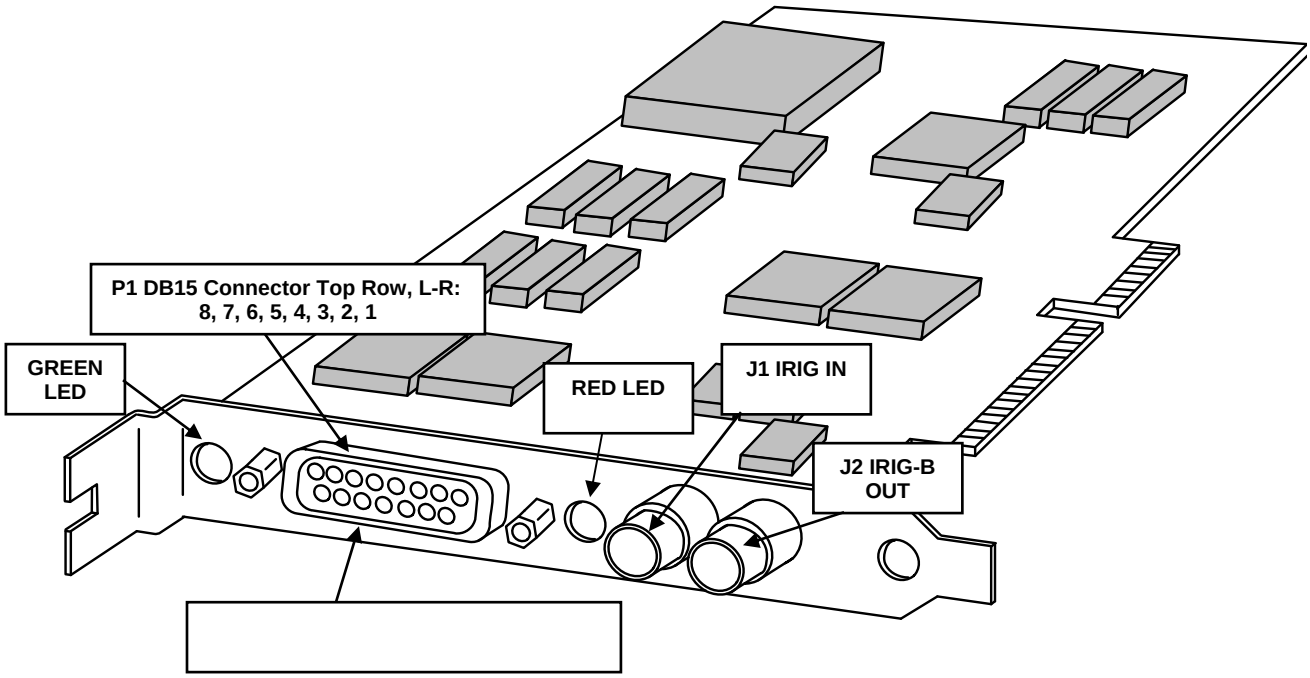
2.2 TSAT (GPS Receiver Only)

NOTE: When both IRIG and GPS synchronization sources are connected simultaneously, the unit will default to IRIG decoding.

Table 2.10—GPS Receiver/Antenna Specifications	
Number of Satellites	6
Acquisition Time (cold start)	1 minutes typical
Re-acquisition Time	<1 minute
Frequency	L1 frequency, C/A code (SPS), continuous tracking receiver, static overdetermined clock mode (default)
Sync to UTC	Within 15 nanoseconds (static)
Accuracy Horizontal Position	<6 meters (50%) <9 meters (90%)
Accuracy Altitude Position	<11 meters (50%) <18 meters (90%)
Altitude	0 m to +18,000 m (0 to +59,055 feet)
Size	3.74" D, 2.85" H (95mm x 72.5mm)
Weight	5.4 oz (154 g)
Pole Mount	1"-14 straight thread or 3/4" pipe thread
Operating Temp	–40° to +85° C (-40 to +185 °F)
Storage Temp	–55° to +105° C (-67 to +221 °F)
Operating Humidity	95% RH, non-condensing @ 60 °F

3 Pinouts

The accompanying figure illustrates pinouts for both the TSAT-PCI and the TPRO-PCI:



3.1 Connector Pinout (TSAT Only)

The GPS receiver/antenna cable plugs into the 15-pin P1 connector. In addition, some pins may interface to the user's equipment. It is the user's responsibility to modify the antenna cable connector, if necessary, to access the "User Connection" pins. A description of the pinout for the supplied cable is shown in Table 3.1. Refer to the figure on the following page.

Table 3.1—TSAT, P1 Connector Pinout

P1 Pin	Antenna Pin	Antenna Connection	Wire Color	User Connection
1	—	—	—	Do not connect
2	—	—	—	Do not connect
3	1	+12 Volts	Red	—
4	—	—	—	Time Tag input
5	9	Ground	Black	Ground
6	—	—	—	Heartbeat output
7	—	Ground	Shield	—
8	—	—	—	Match time output
9	11	1PPS+	Orange/White	—
10	5	RXD+	Yellow	—
11	4	RXD–	Brown	—
12	3	TXD+	Orange	—
13	2	TXD–	Violet	—
14	12	1PPS–	Black/White	—
15	8	Battery	Green	—

The antenna cable wires are twisted pairs as follows:

Red with Black ..... (Pins 3 and 5)
Orange with Violet..... (Pins 12 and 13)
Yellow with Brown..... (Pins 10 and 11)
Green with Blue ..... (Pins 15 and None)
Orange/White with Black/White ..... (Pins 9 and 14)

NOTE: The following antenna cable wires are connected at the antenna end, but NOT at P1:

Antenna	Pin Color
6	White
7	Gray
10	Blue

The pigtail on the 15-pin end of the cable is used for custom options (if any).

3.2 P1 Connector Pinout (TPRO Only)

The timecode input can be applied either to Pins 1 and 2 of P1 or to the J1 BNC connector (this is the connector closest to P1). The timecode input is a differential signal (i.e., timecode input is isolated from ground). It is acceptable to connect timecode input to ground.

The IRIG-B output can be taken either from Pin 9 of P1 or from the J2 BNC connector (this is the connector farthest from P1). The IRIG-B output is a single-ended signal (i.e., it is referenced to ground).

Table 3.2—TPRO, P1 Connector Pinout

P1 Pin	User Connection	Other Options	
1	IRIG IN +	——	
2	IRIG IN -	——	
3	Do not use	——	
4	Time Tag input	——	
5	Ground	——	
6	Heartbeat output	FXB + / HB1PPS+ / HDRV +	*
7	Ground	——	
8	Match time output	FXB - / HDRV -	*
9	IRIG B Output	DCLOBNC	*
10	——	——	
11	——	——	
12	——	——	
13	——	——	
14	——	——	
15	10 MHz output	Option M	*

** Refer to Section 9,* Options and Accessories*, for more information.*

3.3 Time Code Input BNC Connector (J1)

The timecode input BNC connector is located nearest the 15-pin D-type connector.

3.4 IRIG-B Output BNC Connector (J2)

The IRIG-B output BNC connector is located farthest from the 15-pin D-type connector.

4 Configuration

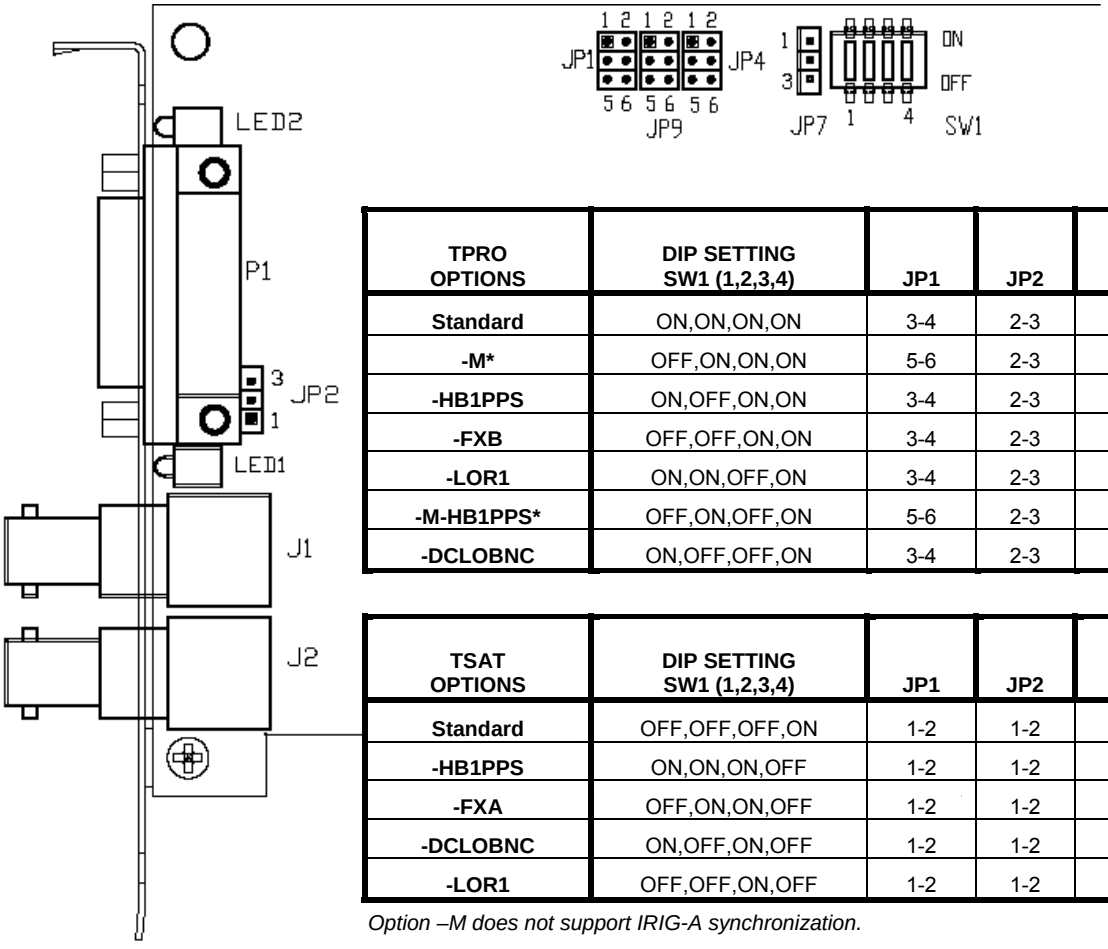
4.1 Base Address

The host computer's PCI BIOS software configures the base address.

4.2 Interrupt Request Level

The host computer's PCI BIOS software configures the interrupt request (IRQ) level.

4.3 PCI-U-2/66MHz Jumper Configuration



TPRO OPTIONS	DIP SETTING SW1 (1,2,3,4)	JP1	JP2	JP4	JP9
Standard	ON,ON,ON,ON	3-4	2-3	1-3, 2-4	1-3, 2-4
-M*	OFF,ON,ON,ON	5-6	2-3	1-3, 2-4	1-3, 2-4
-HB1PPS	ON,OFF,ON,ON	3-4	2-3	1-3, 2-4	1-3, 2-4
-FXB	OFF,OFF,ON,ON	3-4	2-3	1-3, 2-4	3-5, 4-6
-LOR1	ON,ON,OFF,ON	3-4	2-3	1-3, 2-4	1-3, 2-4
-M-HB1PPS*	OFF,ON,OFF,ON	5-6	2-3	1-3, 2-4	1-3, 2-4
-DCLOBNC	ON,OFF,OFF,ON	3-4	2-3	3-5, 4-6	2-4, 3-5

TSAT OPTIONS	DIP SETTING SW1 (1,2,3,4)	JP1	JP2	JP4	JP9
Standard	OFF,OFF,OFF,ON	1-2	1-2	1-3, 2-4	1-3, 2-4
-HB1PPS	ON,ON,ON,OFF	1-2	1-2	1-3, 2,4	1-3, 2-4
-FXA	OFF,ON,ON,OFF	1-2	1-2	1-3, 2-4	3-5, 4-6
-DCLOBNC	ON,OFF,ON,OFF	1-2	1-2	3-5, 4-6	2-4, 3-5
-LOR1	OFF,OFF,ON,OFF	1-2	1-2	1-3, 2-4	1-3, 2-4

Option –M does not support IRIG-A synchronization.

5 Installation

5.1 GPS Receiver/Antenna (TSAT Only)

The mounting location should be free of objects that could obstruct satellite visibility from straight overhead to within 20 degrees of the horizon in all directions. Obstructions that block a significant portion of the sky result in degraded performance. Specifically, the GPS receiver can track fewer than four satellites, which would prevent it from obtaining time synchronization. To optimize timing accuracy, the GPS receiver attempts to track satellites that are spread out as far as possible across the sky. The GPS receiver/antenna must be mounted with the connector side pointing down and must be spaced at least 39 inches (1 meter) away from other GPS antennas.

Mount the antenna at the desired location. Connect the round end of the supplied cable to the antenna. Take appropriate lightning precautions as necessary.

NOTE: Spectracom recommends applying an appropriate silcon grease to the cable connection at the GPS antenna in order to protect the connection from moisture. An additional weatherproofing kit (P/N 221213) containing butyl rubber and plastic tape is also available from Andrews Corporation, US 800.255.1479.

5.2 Installing the Board in the Computer

Shut the computer down, then turn its power switch off and unplug the line cord.

Open the computer and install the board in any unused PCI slot.

CAUTION:  *Observe all ESD procedures when handling the board and the computer. Before installing the board, discharge static buildup by touching the metal frame of the computer with one hand and the protective bag containing the board with the other hand. Open the protective bag only after static buildup has been safely discharged.*

Remove the metal plate at the desired location on the rear panel, then plug the board in. Attach the top of the mounting bracket with the screw from the metal plate.

Close the computer, plug in the line cord, start the computer. Depending on which operating system being used, a message that identifies new hardware may appear; this message may indicate that the hardware is of "unknown type." This is normal. Exit the "Found New Hardware" dialogue box. **DO NOT click on "Have Disk."**

The TPRO and TSAT operate automatically as soon as the host computer system performs the power-on reset. To change the operating parameters or read data, consult Chapter Seven.

An on-board LED (LED1) flashes a status pattern to assist in diagnosing installation errors. The pattern is a sequence of short and long flashes. To enable the status pattern to repeat more frequently, trailing short flashes are deleted.

Table 5.1—LED Flash Patterns

Flash Position	Meaning of Short (Cleared) Flash	Meaning of Long (Set) Flash
1	GPS satellite receiver being used for time reference	Modulated timecode input being used for time reference
2	Synchronization to better than 5µs verified with last 5 seconds	Synchronization to better than 5µs not verified within last 5 seconds
3	1PPS pulse from GPS satellite receiver is OK	1 PPS pulse from GPS satellite receiver is bad. In applications with modulated timecode inputs only, this status bit will always be set.
4	GPS satellite receiver serial data being received OK	No serial data being received from GPS satellite receiver. In applications with modulated timecode inputs only, this status bit will always be set.
5	GPS satellite receiver is tracking enough satellites for accurate UTC time.	GPS satellite receiver is not tracking enough satellites for accurate UTC time. In applications with modulated timecode inputs only, this status bit will always be set.
6	Timecode input being decoded	Timecode input not decodable. In applications without modulated timecode inputs, this status bit will always be set.
7	If using 1PPS, set NEXT 1PPS TIME command sequence has been performed. (Used for Option –M only)	Waiting for “SET NEXT 1PPS TIME” command. (Used for Option –M only)

6 Board Operation

6.1 TSAT

The TSAT acquires time from the GPS satellites, synchronizes its on-board clock to this time, and provides an IRIG-B output from the on-board clock.

NOTE: When IRIG and GPS are connected simultaneously, the unit defaults to IRIG synchronization.

GPS consists of a set ("constellation") of approximately 30. These satellites are in relatively high, circular orbits, are inclined about 55 degrees relative to the equator, and circle the Earth approximately once every 12 hours. Consequently, several satellites are above the horizon at all times anywhere on Earth. The receiver must track at least four satellites simultaneously in order to determine time and position. Best accuracy is achieved when the satellites that are being tracked are scattered widely across the sky; the receiver automatically attempts to choose satellites based on maximum apparent separation. Therefore, it is important that the antenna have a clear view of as much sky as possible (and, for the same reason, be mounted with the connector pointed down). The satellites do not remain at a fixed location in the sky.

Occasionally, the receiver stops tracking a satellite and begins searching for another one; this causes fluctuations in the number of satellites tracked (between five and eight).

The most common complaint among new GPS users is that the time needed to begin tracking satellites varies each time the unit is turned on, or that it seems to take a long time to begin tracking. Refer to the section entitled *"Specifications"* in Chapter Two for typical and maximum times, and note that significant variations around the "typical" time are normal. If the receiver has not established synchronization after the maximum time specified, the most probable reason is that the antenna does not have an unobstructed view of the sky—try re-locating the antenna. Note that the GPS receiver is built into the antenna housing; additional filtering cannot be installed.

When power is applied, the GPS receiver automatically begins to search for GPS satellite signals. After the receiver has been operating for a few minutes and has calculated the position (longitude, latitude, and altitude), it saves the position in memory. A saved position results in faster re-acquisition the next time power is applied. A large capacitor on the board provides voltage to the receiver's memory; if the cable between the board and the receiver is disconnected, or if the computer has not been turned on in approximately the past 10 days, the receiver's position memory is lost. Therefore, a slightly longer acquisition time is required the next time that power is applied.

The time obtained is in Coordinated Universal Time (UTC) format. This means the same time (and date) is received in all parts of the world, regardless of local time zone. UTC is 5 hours ahead of Eastern Standard Time (EST) in the United States in winter, and 4 hours ahead of Eastern Daylight Time (EDT) in summer. UTC is not adjusted for Daylight Saving time; for example, 10:00 p.m. in New York City on July 3rd is 02:00 a.m. July 4th UTC.
A Gregorian date consists of the year, month, and day in the format YYYY-MM-DD; for example, "2003-09-19" for September 19, 2003. The Gregorian date can be read from the board; however, the Gregorian date is not transmitted in the IRIG-B output. Instead, the IRIG-B

output transmits the Julian date (an integer from 001-366 that represents the day number in the year). This limitation is due to the standard definition of the IRIG-B code format.

The on-board clock continues to increment time ("freewheel") while not tracking satellites. When power is first applied, time begins freewheeling from 000:00:00:00, then jumps to the correct time when synchronization is established.

6.2 TPRO

The TPRO acquires time from the timecode input, synchronizes its on-board clock to this time, and provides an IRIG-B output from its on-board clock. The timecode input consists of an amplitude-modulated sine wave (carrier frequency is 1 kHz for IRIG-B or NASA36, or 10 kHz for IRIG-A). The code format is detected automatically.

The board does not significantly load the timecode input, and, since it is a very low frequency, cable impedance mismatches do not significantly degrade the signal either. Thus, a single timecode source can drive at least 10 inputs. Cable termination is not necessary, cable length can be up to several hundred feet, and a variety of cable types can be used. Usually, coaxial cable (RG-58 or RG-59 type) with BNC connectors is used. Multiple boards can be driven by placing a BNC "T" connector at each board, and connecting the timecode input in a daisy-chain configuration.

For another approach, take the IRIG-B output from one board to the timecode input of the next board (i.e., a loop-through configuration). The advantage of the loop-through configuration is that if the signal is lost at some point, all boards downstream of the break continue to have the same time (driven by the first board's freewheeling clock). Also, it eliminates the need for BNC "T" connectors.

The board synchronizes to the incoming timecode automatically. An on-board 10 MHz crystal oscillator is phase-locked to the timecode carrier frequency. This results in timing resolution down to 1μS, despite the fact that the input carrier is only 1 kHz (or 10 kHz for IRIG-A). Also, this precludes using timecode from sources with unstable time bases (e.g., playback from tape or digital storage).

By definition, the timecode format standard (IRIG-B, NASA36, or IRIG-A) specifies that the format for transmitting the date be an integer (001-366). This is referred to as the Julian date. Note that the date is not in year/month/day as in Gregorian format.

NOTE: Although the user's software can convert from a Julian date to a Gregorian date, be careful. First, the user's software must distinguish whether or not the current year is a leap year. Second, the user's software must account for the fact that, when freewheeling before synchronizing, the board will report an invalid Julian date (000).

7 Programming for TPRO/TSAT-U-2

7.1 General Information

From a programming standpoint, the board appears to be a PCI-to-ISA bridge device. This means that the universal PCI bus "sees" the board as a device that has thirty-two consecutive 16-bit memory locations (64 bytes) and thirty-two consecutive 16-bit I/O locations (64 bytes). During startup, the PCI BIOS (part of the host computer) mapped these locations somewhere in the absolute address space.

The thirty-two memory locations and the thirty-two I/O locations serve exactly the same functions. In actual use, only one of these (either memory or I/O) is used; the other is ignored. On host computers with Intel CPUs (e.g., Pentium, 486, etc.) use the I/O locations. On host computers with Motorola CPUs (e.g., the 68000 family) use the memory locations (since Motorola does not have "I/O" instructions).

The locations of the board's registers are specified as "Base + Offset". The offsets are constants, as described in the next section. The "Base" is chosen by the PCI BIOS during startup. There is a separate "Base" for the memory and I/O locations.

Time is read as four 16-bit words, and is in binary-coded decimal format. Status is read as a single 16-bit word. Time tags and, for the TSAT, GPS information (longitude, latitude, altitude, and Gregorian date), are read by first sending a command to the board, then reading ten 16-bit words from a first-in-first-out (FIFO) register.

The user's software must wait a short amount of time after sending each command. This admittedly cumbersome requirement is necessary because the on-board processor places a higher priority on maintaining the time than on processing commands. The actual amount of time needed to process a command depends on when the command was received relative to the on-board time. Entries in Chapter Six specify the amount of time needed to assure that the command was received. There is no restriction on reading from the board.

Each 16-bit word is located on an even address. Although many of the registers use only eight bits, always read and write registers as 16-bit entities. **Do not attempt an 8-bit access on an odd address location.**

7.2 Register Locations

NOTE: In this manual, the prefix "0x" indicates that the number is in hexadecimal (Base 16) format.

Table 7.1—Register Locations for PRO/TSAT-U-2

Location	Read Usage	Write Usage	Register Function
Base + 0x00	FIFO	Interrupt Control Port	R - Returns response data from the board W - Interrupt control register
Base + 0x02	Status Register	Command Port	R - Returns status information for the board W - Issues commands to the board
Base + 0x04	H	De-assert Reset	Releases the board from reset
Base + 0x06	H	Assert Reset	Places the board into reset
Base + 0x08	Clock: Days	H	Returns portion of latched time
Base + 0x0a	Clock: Hours, Minutes	H	Returns portion of latched time
Base + 0x0c	Clock: Seconds through 10 mS	H	Returns portion of latched time
Base + 0x0e	Clock: 1 mS through 1 uS	H	Latches a snapshot of the present time and returns the lower portion of time
Base + 0x10	H	Clear Flags	Clears interrupt flags
Base + 0x12	H	Simulate Time Tag	Simulates a time tag occurrence
Base + 0x14	H	H	
Base + 0x16	H	H	
(H = Reserved for future use.)			

7.3 Using the FIFO

The board uses a FIFO register to provide multi-word responses. Each of these responses consists of ten 16-bit words, of which only the lower 8-bits are actually used. A bit in the Status Register indicates whether data is ready in the FIFO. The user's software must check that status bit before reading *each* word from the FIFO.

There can be a delay of up to 200 μS before all ten words are written into the FIFO. This is due to the fact that although the on-board CPU writes this data, it also maintains the time (days through milliseconds) in software, and places a higher priority on maintaining the time than on filling the FIFO. Thus, it is not uncommon that, for example, only three of the ten words are written into the FIFO, then, following a substantial delay, the remaining seven words are written. The user's software must allow for such operation (i.e., it must not “give up” just because it has not read all ten words before the status indicates that the FIFO is empty. Either wait 200 μS before beginning to read, or allow for enough retries if FIFO empty status is detected prematurely.)

To check the FIFO Ready flag, read the Status Register (at Base + 0x02). If the least significant bit is a zero, there is data in the FIFO. If this bit is a one, the FIFO is empty.

The FIFO holds 512 words (i.e., 51 responses). Letting these responses stack up in the FIFO is acceptable, but the user's software is responsible for knowing what each of the responses is.

During initialization, the user's software must flush the FIFO. Do this by reading the FIFO until the “FIFO Ready” flag is a one. This could take up to 512 reads, maximum.

Responses to user commands echo the command in the first two words from the FIFO. This can be useful in sorting out multiple responses that are stacked up in the FIFO.

7.4 Reading Clock Time

The current ("clock") time is read as four 16-bit words. Reading the first word latches all four words, thus the latency time between reading them does not affect the accuracy. This also means that it is important to read the least significant word first, as this causes the other words to be latched. It is not necessary to read all four words if the application does not need the complete clock time.

NOTE: These locations are read-only. A different sequence is used to set the time. Refer to the sections on setting the clock time.

It is also necessary to examine the status register to determine if the time is valid.

The Julian date (not the Gregorian date) is reported.

The value range for Days is 000-366. Be sure the variable that stores Days can accommodate this range. Assigning Days to an 8-bit integer (with a range of 000-255) produces an unpleasant surprise in mid-September!

Within each 16-bit word there are four "nibbles" (groupings of 4 bits each). Each nibble is decoded separately, representing a single binary-coded-decimal (Base 10) digit.

Table 7.2—Clock Time Data				
Location	**Most Significant Nibble**	**Nibble**	**Nibble**	**Lease Significant Nibble**
Base + 0x0e	10^0 mS	10^2 µS	10^1 µS	10^0 µS
Base + 0x0c	10^1 Seconds	10^0 Seconds	10^2 mS	10^1 mS
Base + 0x0a	10^1 Hours	10^0 Hours	10^1 Minutes	10^0 Minutes
Base + 0x08	(Reserved)	10^2 Days	10^1 Days	10^0 Days

For example, if the time is day 123, hour 11, minute 58, second 17.654321, the time is read as follows:

Location	**Contents**	
Base + 0x0e	0x4321	
Base + 0x0c	0x1765	
Base + 0x0a	0x1158	
Base + 0x08	0xU123	(U = Unknown)

7.5 Sending Commands

Writing to the Command Port at Base + 0x02, sends commands to the board. A small delay is required after sending each word. Note that there is no way to “read back” a command once it has been sent.

Commands consist of one or more 16-bit words, of which only the lower 8-bits are actually used. These lower 8 bits are further divided into two 4-bit "nibbles". For some commands, the high nibble is a constant, and the low nibble contains the data. For other commands both the high and low nibbles are constant.

It is necessary to wait at least 100 µS after sending each command word before sending anything else to the command port.

Table 7.3—Command Functions	
Function	**Command**
Reset Firmware	0x004f
Enable Sync	0x004d
Disable Sync	0x004e
Report Firmware Version in FIFO	0x00e9
Report Number of GPS Satellites in FIFO (TSAT only)	0x005c
Report Altitude & Gregorian Date in FIFO	0x005d
Report Longitude in FIFO (TSAT only)	0x005e
Report Latitude in FIFO (TSAT only)	0x005f
Clear Holding Register	0x00f0
Put 10^2 Days in Holding Register	0x0050–53
Put 10^1 Days in Holding Register	0x0060–69
Put 10^0 Days in Holding Register	0x0070–79
Put 10^1 Hours or 10^{-1} Seconds in Holding Register	0x0080–89
Put 10^0 Hours or 10^{-2} Seconds in Holding Register	0x0090–99
Put 10^1 Minutes, 10^{-3} Seconds, or 16^3 Heartbeat in Holding Register	0x00a0–af
Put 10^0 Minutes, 10^{-4} Seconds, or 16^2 Heartbeat in Holding Register	0x00b0–bf
Put 10^1 Seconds, 10^{-5} Seconds, or 16^1 Heartbeat in Holding Register	0x00c0–cf
Put 10^0 Seconds, 10^{-6} Seconds, or 16^0 Heartbeat in Holding Register	0x00d0–df
Put Propagation Delay 10^3 µS in Holding Register	0x0030–39
Put Propagation Delay 10^2 µS in Holding Register	0x0020–29
Put Propagation Delay 10^1 µS in Holding Register	0x0010–19
Put Propagation Delay 10^0 µS in Holding Register	0x0000–09
Copy Holding Register to Clock Time or Propagation Time	0x00e0
Copy Holding Register to Start/Stop Time (Days-Seconds)	0x00e1
Copy Holding Register to Start Time (10^{-1} to 10^{-6} Seconds)	0x00e2
Copy Holding Register to Stop Time (10^{-1} to 10^{-6} Seconds)	0x00e3
Copy Holding Register to Clock Time on next 1PPS (Option –M only)	0x004c
Copy Holding Register to Heartbeat, Pulse Mode, at next period	0x00e5
Copy Holding Register to Heartbeat, Pulse Mode, immediately	0x00e6
Copy Holding Register to Heartbeat, Square wave Mode, at next period	0x00e7
Copy Holding Register to Heartbeat, Square wave Mode, immediately	0x00e8
Copy Holding Register to Year	0x00ea

7.6 Setting the Clock Time (Not Applicable to Option -M)

Set the clock time by commanding the days, hours, minutes, and seconds. The milliseconds and microseconds cannot be commanded; they are reset to 000000 when the command is sent.

It is necessary to load the time into the Holding Register. First, send a command to clear the Holding Register. Then, one at a time, write each digit (hundreds of days down to ones of seconds) into the Holding Register.

There is a separate command for loading each of these digits. The upper 4 bits of the command identify which digit is being loaded, the lower 4 bits contain the actual data to load. Once all the digits have been loaded, a command is sent to set the time (the board does this by copying the Holding Register into the clock).

For example, to set the clock to day 123, hour 11, minute 58, second 17, send the following sequence of commands to the Command Port:

```
0x00f0                              ; Clear the Holding Register
0x0051     0x0062     0x0073        ; Day 123
0x0081     0x0091                   ; Hour 11
0x00a5     0x00b8                   ; Minute 58
0x00c1     0x00d7                   ; Second 17
0x00e0                              ; Set Clock Time
```

NOTE: If no timecode input is present (TPRO), or the GPS receiver is not tracking satellites (TSAT), the board will accept the time set sequence described above and continue to increment time ("freewheel").

However, when a valid timecode (TPRO) is input, or when the GPS receiver begins tracking satellites (TSAT), the clock's time will jump to the decoded time, unless the above sequence was preceded with a Disable Sync command (described later in this chapter).

While freewheeling, the In-Sync status bit will be false.

The user's software must ensure that the commanded values are in the appropriate ranges. The board does not error-check the data before loading the clock. Commanding invalid values (e.g., 39 hours) causes erratic operation.

7.7 Setting the Clock Time (TPRO Option -M Only)

Set the clock time by commanding the days, hours, minutes, and seconds. The milliseconds and microseconds cannot be commanded; they are reset to 000000 when the *next* 1PPS occurs. The clock time of the *next* 1PPS is commanded to the board.

It is necessary to load the time into the Holding Register. First, send a command to clear the Holding Register. Then, one at a time, write each digit (hundreds of days down to ones of seconds) into the Holding Register.

There is a separate command for loading each of these digits. The upper 4 bits of the command identify which digit is being loaded, the lower 4 bits contain the actual data to load. Once all the digits have been loaded, a command is sent to arm the clock.

For example, to set the clock to day 123, hour 11, minute 58, second 17, send the following sequence of commands to the Command Port:

```
0x00f0                              ; Clear the Holding Register
0x0051      0x0062      0x0073      ; Day 123
0x0081      0x0091                  ; Hour 11
0x00a5      0x00b8                  ; Minute 58
0x00c1      0x00d7                  ; Second 17
0x004c                              ; Arm the clock for next 1PPS
```

After sending the 0x004c command, the board sets the milliseconds and microseconds to 000000 when the first 1PPS occurs (the seconds do not increment). Then, on the second 1PPS pulse, the time (seconds) begins to increment.

CAUTION:



The board expects the 1PPS input to be continuous. If the 1PPS signal stops pulsing after the board establishes initial sync, the board will continue to increment time ("freewheel"). However, if the 1PPS signal resumes after a period of freewheeling, the board may reset the clock time to 000:00:00:00.000000. This is because the 1PPS occurs outside of a narrow window in which the board expects it, either because the 1PPS has moved or because the board's time has drifted during freewheeling.

The arm command (0x004c) must be sent no sooner than 50 mS after the previous 1PPS occurred, and no later than 50 mS before the next (arming) 1PPS occurs.

NOTE: If both 1PPS and Timecode inputs are present, the board will sync to the incoming timecode and ignore the 1PPS.

Commands 0x004d and 0x004e (Enable/Disable Sync) apply both to the 1PPS and the timecode input. Commands 0x00e0 (set clock) and 0x00ea (set year) are not applicable to boards with Option –M.
The user's software must ensure that the commanded values are in the appropriate ranges. The board does not error-check the data before loading the clock. Commanding invalid values (e.g., 39 hours) will cause erratic operation.

7.8 Setting the Year (Not Applicable to Option -M)

Whether the IRIG-B output is synchronized to GPS or timecode, or is freewheeling, it counts from day 365 to day 001, unless the year is set to a leap year. Once set to a leap year, the IRIG-B output counts from 365 to 366, then to 001.

The TSAT acquires the year from the GPS satellites. The year can also be set by command (if the GPS receiver is not connected).

To function properly, the TPRO requires that the year be set by command at the end of a leap year. The board will increment the year when the day rolls over to 001. Also, setting the year enables the board (TPRO and TSAT) to compute the Gregorian date using the year and Julian date.

Set the year by sending the command sequence "0x006n 0x007n 0x008n 0x009n 0x00ea" to the command port. For example, to set the year to 2003, send "0x0062 0x0070 0x0080 0x0093 0x00ea".

The year is reset to 0000 when power is first applied, or when any of the following occur: system reset, firmware reset (command 0x004f), or writing to the "Assert Reset" or "De-assert Reset" addresses.

7.9 Reading the Year, Gregorian Date and Altitude (Not Applicable to Option -M)

The GPS receiver's computations for the altitude (TSAT only) and Gregorian date (TSAT and TPRO) are reported in the FIFO in response to the 0x005d command. Altitude is in units of meters relative to mean sea level.

Word	Bits 7– 4	Bits 3 – 0
0 (first)	5	D
1	5	D
2	10^1 Day	10^0 Day
3	10^5 meters	10^4 meters
4	10^3 meters	10^2 meters
5	10^1 meters	10^0 meters
6	10^{-1} meters	0
7	10^1 Year	10^0 Year
8	10^3 Year	10^2 Year
9 (last)	10^1 Month	10^0 Month

The board increments the Gregorian date approximately one second after time rolls over from 23:59:59 to 00:00:00 (HH:MM:SS). This occurs on every date in every year. Consequently, the Gregorian date should not be used during minutes 59 and 00—this will avoid rollover problems.

7.10 Report Longitude (TSAT Only)

The GPS receiver's computation for longitude is put into the FIFO in response to the 0x005e command. The units are degrees, minutes, and fractions of minutes. The response is in the following format:

Word	Bits 7–4	Bits 3–0
0 (first)	5	e
1	5	e
2	0	10^2 Degrees
3	10^1 Degrees	10^0 Degrees
4	10^1 Minutes	10^0 Minutes
5	10^{-1} Minutes	10^{-2} Minutes
6	10^{-3} Minutes	10^{-4} Minutes
7	Reserved	Reserved
8	Reserved	Reserved
9 (last)	Reserved	Reserved

NOTE: If the reported value is less than 180 degrees, the longitude is East (for Europe, Africa, Asia, etc.). If the reported value is greater than or equal to 180 degrees, subtract 180 degrees to obtain west longitude (for USA, Canada, Central & South America, etc.). For example, the reported value for Los Angeles, CA, USA, will be approximately 298 degrees. Since this is greater than 180, subtract 180 to get the correct value, i.e., 118 degrees West. Be sure to convert minutes to decimal degrees before comparing to 180 degrees.

7.11 Report Latitude (TSAT Only)

The GPS receiver's computation for latitude is put into the FIFO in response to the 0x005f command.

The units are degrees, minutes, and fractional minutes. Latitudes north of the equator are reported as 0–90 degrees, latitudes south of the equator are reported as 180+ degrees South—i.e., if the reported value is greater than or equal to 180, subtract 180 degrees and change the sign to negative (south). It is important to convert minutes to decimal degrees before comparing to 180 degrees. The response is in the format shown here:

Word	Bits 7–4	Bits 3– 0
0 (first)	5	f
1	5	f
2	0	10^2 Degrees
3	10^1 Degrees	10^0 Degrees
4	10^1 Minutes	10^0 Minutes
5	10^{-1} Minutes	10^{-2} Minutes
6	10^{-3} Minutes	10^{-4} Minutes
7	Reserved	Reserved
8	Reserved	Reserved
9 (last)	Reserved	Reserved

7.12 Report Number of GPS Satellites Being Tracked (TSAT Only)

The GPS receiver determines automatically which satellites to track. The number (quantity) of satellites being tracked is reported in the FIFO in response to sending command 0x005c to the command port. The response is of the form shown here:

Word	Bits 7–4	Bits 3 – 0
0 (first)	5	c
1	5	c
2	Reserved	Reserved
3	Reserved	Reserved
4	Reserved	Reserved
5	Reserved	Reserved
6	Reserved	Reserved
7	0	# of Satellites
8	Reserved	Reserved
9 (last)	Reserved	Reserved

NOTE: The number of satellites tracked is for diagnostic purposes only. The number of satellites ranges from 0 to 8, inclusive. Valid time and position require that at least four satellites be tracked. The In-Sync flag in the Status Register must be used to actually determine whether the board is synchronized and providing valid position.

There is no difference in timing accuracy when 5, 6, 7, or 8 satellites are being tracked. It is normal for the number to fluctuate between 5 and 8, given that the GPS receiver picks different satellites to optimize the timing.

It is normal for the number of satellites to be between 0 and 3 during acquisition and re-acquisition.

7.13 Enable/Disable Sync

The board can be forced to freewheel by sending the "Disable Sync" command. Sending this command causes the board to ignore the timecode input, the 1PPS input (Option –M only), and the GPS input (TSAT only).

To restore normal operation, send the "Enable Sync" command.

To send the Disable Sync command, write 0x004e to the command port. To send the Enable Sync command, write 0x004d to the command port.

The power-on default is to Enable Sync.

7.14 Reading the Status Register

The Status Register consists of one 16-bit word, of which only the lower 8 bits are used. The Status Register is read from location Base + 0x02, and is formatted as shown in Table 7.4.

Table 7.4—Status Register Format

Bit	Name	Meaning When "0"	Meaning When "1"
0 (LSB)	FIFO Ready Flag	FIFO Ready (data available)	FIFO empty
1	Timecode Present	Timecode Input has no detectable signal	Timecode input has a signal present
2	In-sync Flag	Clock is freewheeling GPS position is invalid	Clock is synced to timecode or GPS and GPS position is valid
3	Match Flag	Start time has not occurred	Start time has occurred
4	Heartbeat Flag	Heartbeat has not occurred	Heartbeat has occurred
5	Heartbeat Int. Mask	PCI bus interrupt disabled for heartbeat	PCI bus interrupt occurs on each heartbeat
6	Match Int. Mask	PCI bus interrupt disabled for start time	PCI bus interrupt occurs at the start time
7	FIFO Ready Int. Mask	PCI bus interrupt disabled for FIFO data available	PCI bus interrupt occurs when FIFO data available
8–15	(Reserved)	(Reserved)	(Reserved)

NOTE: Bit 2 (In-Sync Flag) is the only bit to examine when determining the validity of the time (and position for TSAT).

Bit 1 (Timecode Present) is for diagnostic purposes only. It indicates only that the amplitude of the timecode input is adequate for detection. It does not indicate whether the input is valid. For TSAT, this bit will always be zero.

Bits 5, 6, and 7 provide a means for reading back the corresponding bits in the Interrupt Control Port.

Bits 3 and 4 may be true ("1") when power is first applied. The user's software must clear bits 3 and 4 before using them.

7.15 Interrupt Control Port

The board can generate interrupts when the FIFO has data, when each heartbeat occurs, and/or when the commanded Start Time occurs. Each of these is enabled separately via the Interrupt Control Port, and any, all, or none can be enabled simultaneously.

The Interrupt Control Port is a single 16-bit word, of which only 3 bits are actually used. It is located at Base + 0x00, and is write-only. The bits in the Interrupt Control Port are defined as shown in Table 7.5.

Table 7.5—Interrupt Control Port Bit Definitions

Bit	Name	Writing "0" Action	Writing "1" Action
0–4	(Reserved)	(Reserved)	(Reserved)
5	Heartbeat Interrupt Mask	No PCI interrupt on heartbeat	Heartbeat causes PCI interrupt
6	Match Interrupt Mask	No PCI interrupt at start time	Start time causes PCI interrupt
7	FIFO Ready Int. Mask	No PCI interrupt when data is available in FIFO	PCI interrupt when data is available in FIFO
8–15	(Reserved)	(Reserved)	(Reserved)

The board generates the same interrupt regardless of whether it was caused by heartbeat, start time, or FIFO data available. After an interrupt, the user's software must interrogate the board to determine which of these was the cause.

The power-on default is to have all interrupts disabled. Also, sending the "Assert Reset" command disables all interrupts.

CAUTION:



The "FIFO Ready" interrupt occurs each time the FIFO changes from being empty to containing data. If the user's software detects quickly that the first word has been written into the FIFO and reads it out, it is possible that the FIFO will be empty for a moment. Thus, when the second word is put into the FIFO, it generates another interrupt.

The solution is to disable the FIFO Ready interrupt until all 10 words have been read from the FIFO, then re-enable the interrupt.

7.16 Setting the Propagation Delay Correction

This command is used to correct for delays that are due to cable length (timecode or GPS cables). Most applications do not need to compensate for cable delays because the delay is on the order of a hundred nanoseconds, while the clock's resolution is 1 microsecond. However, introducing a deliberate (large) offset can be helpful in situations in which the board is used to trigger an instrument slightly *before* a particular time.

The range of the propagation correction is –1000 μS to +8999 μS. The power-on default is zero.

To specify the propagation delay, first clear the Holding Register, then write four words (representing each of the digits in the delay value), then send the "Set Clock Time/Propagation Time" command. A special number sequence is used to specify negative delays. To specify delays from –1000 μS to – 1 μS send values of 9000 to 9999, respectively. For example, to specify a correction of +4567 μS, send the following sequence of commands to the command port:

```
0x00f0                                          ; Clear the Holding Register
0x0034     0x0025     0x0016     0x0007        ; Specifies +4567 μS
0x00e0                                          ; set propagation correction
```

7.17 Setting the Start/Stop ("Match") Times (Not Applicable to Options -FXA, -FXB, or –HDRV)

The **match output** (P1 Pin 8) goes high at the Start time and low at the Stop time. The **match interrupt** occurs at the Start time (not at the Stop time). The **match flag** (in the Status Register) goes true at the Start time and remains true until the user clears it with a software command.

To specify the Start and Stop times, first clear the Holding Register, then command the days-through-seconds portion of the time, send a set command, next send the milliseconds through microseconds, finally, send another set command.

For example, to command a Start time of day 123, hour 11, minute 58, second 17.456789, send the following sequence to the command port:

```
0x00f0                                  ; Clear Holding Register
0x0051      0x0062      0x0073          ; Day 123
0x0081      0x0091                      ; Hour 11
0x00a5      0x00b8                      ; Minute 58
0x00c1      0x00d7                      ; Second 17
0x00e1                                  ; send days-seconds
0x0084      0x0095      0x00a6          ; xx.456xxx seconds
0x00b7      0x00c8      0x00d9          ; xx.xxx789 seconds
0x00e2                                  ; send Start time
```

To specify the Stop time, the sequence is the same, but the final command is 0x00e3 (instead of 0x00e2). The sequence must be completed at least 50 mS before the commanded time occurs. The match output and interrupt (if enabled) operates regardless of whether the board is in-sync or freewheeling.

7.18 Programming the Heartbeat Output (Not Applicable to -HB1PPS, -FXA, -FXB, -LOR1 Options)

The heartbeat output (P1 Pin 6) can be programmed to be either a pulse or a square wave. The specified rate must be an exact multiple of 1.000 μS. The range of programmable rates is:

Minimum Rate *(lowest frequency)* .....21.845 mS (45.7771 Hz)
Maximum Rate *(highest frequency)* .....1.000 μS (1.000 MHz)
Pulse Width *(time low, pulse mode only)*..... 150 nS min, 450 nS max (negative polarity)

To specify the rate (or frequency), compute the divide number N as follows. Note that N must be exactly divisible by 3, meaning that the specified period must be an exact multiple of 1.000 μS.

To specify a period for a pulse or square wave, compute N as:
$N = 3t/10^{-6}$ t is the period in seconds

To specify a frequency for a pulse or square wave, compute N as:
$N = 3 * 10^{6}/F$ F is the frequency in Hertz

Not all values of N are acceptable. Verify that the computed value is evenly divisible by 3 and that it is in the range of 3 to 65,535, inclusive.

Convert N into hexadecimal (Base 16) notation. For example, if the desired output frequency is 10 kHz, N=300 (Base 10), converted to hexadecimal notation yields N=0x012c. Send the hexadecimal number to the board by outputting the following sequence to the command register.

```
0x00f0                                          ; Clear the Holding Register
0x00a0      0x00b1      0x00c2      0x00dc      ; specifies N = 0x012c
```

The heartbeat output can be programmed for a square wave or a pulse, and can be programmed either to start immediately, or at the beginning of the next cycle. Send one of the following commands to command port:

```
0x00e5          ; Pulse mode, starts at beginning of next cycle
0x00e6          ; Pulse mode, starts immediately
0x00e7          ; Square wave, starts at beginning of next cycle
0x00e8          ; Square wave, starts immediately
```

The heartbeat output is present whether the board is in-sync or is freewheeling.

The power-on default is 100 PPS, pulse mode.

7.19 Programming the Heartbeat Output (For Options -HB1PPS, -FXA, -FXB, and -LOR1 Only)

The heartbeat output (P1 Pin 6) can be programmed to be either a pulse or a square wave. The specified rate must be an exact multiple of 1.000 mS. The range of programmable rates is:

```
Minimum Rate (lowest frequency):            65.534 Seconds (0.0152593 Hz)
Maximum Rate (highest frequency):           2 mS (500 Hz)
Pulse Width (time low, pulse mode only):    1 mS (typical)
Programming Resolution:                     1 mS
```

To specify the rate (or frequency), compute the divide number N as follows.

To specify a period for a pulse or square wave, compute N as follows:

N = t/.001 t is the period in seconds

To specify a frequency for a pulse or square wave, compute N as follows:

N = 1000/F F is the frequency in Hertz

Verify that the computed value is in the range of 2 to 65,534, inclusive.

Convert N into hexadecimal (Base 16) notation. For example, if the desired output period is once every 25 seconds, N=25,000 (Base 10), converted to hexadecimal notation yields N=0x61a8. Send the hexadecimal number to the board by outputting the following sequence to the command register.

```
0x00f0                                          ; Clear the Holding Register
0x00a6     0x00b1     0x00ca     0x00d8        ; specifies N = 0x61a8
```

The heartbeat output can be programmed for a square wave or a pulse, and can be programmed to start immediately or at the beginning of the next cycle. Send one of the following commands to command port:

```
0x00e5          ; Pulse mode, starts at beginning of next cycle
0x00e6          ; Pulse mode, starts immediately
0x00e7          ; Square wave, starts at beginning of next cycle
0x00e8          ; Square wave, starts immediately
```

The heartbeat output is present regardless of whether the board is in-sync or freewheeling.

The power-on default is 1PPS, pulse mode.

7.20 Using the Time Tag Input

When the rising edge of the Time Tag Input (P1 Pin 4) occurs, the clock time is latched into a temporary register, and this register is then loaded into the FIFO. An interrupt on the PCI bus is generated, if enabled. The user's software establishes that a time tag has occurred in one of two ways: either by examining the least significant bit of the Status Register (FIFO Ready flag) to determine if it is a zero, or by waiting for an interrupt. Since the clock time is latched when

the rising edge occurs, the Time Tag data will be correct regardless of how long it takes to read the FIFO.

For test purposes, a time tag event can be simulated by writing (any value) to Base + 0x12. The result is indistinguishable from a time tag event on P1 Pin 4.

The FIFO response to either of these events is shown here:

Word	Bits 7–4	Bits 3–0
0 (first)	0	0
1	0	0
2	0	10^2 Days
3	10^1 Days	10^0 Days
4	10^1 Hours	10^0 Hours
5	10^1 Minutes	10^0 Minutes
6	10^1 Seconds	10^0 Seconds
7	10^{-1} Seconds	10^{-2} Seconds
8	1^{-3} Seconds	10^{-4} Seconds
9 (last)	1^{-5} Seconds	10^{-6} Seconds

For example, if the time tag occurs at day 123, hour 11, minute 58, second 17.456789, the contents read from the FIFO will be:

```
Word        Contents
0 (first)   0xUU00      U = Unknown)
1           0xUU00
2           0xUU01
3           0xUU23
4           0xUU11
5           0xUU58
6           0xUU17
7           0xUU45
8           0xUU67
9 (last)    0xUU89
```

NOTE: The Julian date (not the Gregorian date) is reported.

Erratic operation may result if the rate of the time tags exceeds 1000 per second.

There may be a delay of up to 200 µS before time tag data is available in the FIFO.

Some older boards repeated words 2 and 3 in bytes 0 and 1, respectively.

7.21 Report Firmware Version

The version of the embedded firmware is reported in the FIFO in response to the 0x00e9 command. For example, firmware version 7A104221 is reported as shown below.

Word	Bits 7–4	Bits 3– 0
0 (first)	E	9
1	E	9
2	7	A
3	1	0
4	4	2
5	2	1
6	Unknown	Unknown
7	Unknown	Unknown
8	Unknown	Unknown
9 (last)	Unknown	Unknown

NOTE: The Firmware version is for diagnostic purposes only. It is not possible to determine which options are present, or which version is more recent, by examining the version number.

The firmware version is also printed on the label on device U19.

Some older boards ignore the 0x00e9 command.

7.22 Clear Flags Port

Once the Match and/or Heartbeat flag(s) get set, it is necessary to clear the flag by writing a “1” to the appropriate bit of this register at location Base + 0x10.

Table 7.6—Interrupt Control Port Bit Definitions

Bit	Name	Writing “0” Action	Writing “1” Action
0–2	(Reserved)	(Reserved)	(Reserved)
3	Clear Match	Match flag does not change	Clear match flag to zero
4	Clear Heartbeat	Heartbeat flag does not change	Clear heartbeat flag to zero
5–15	(Reserved)	(Reserved)	(Reserved)

NOTE: If used as an interrupt, the user's software must clear the Match Flag each time the Start time occurs. Failure to do so will result in missed interrupts (if enabled) until the flag is cleared.

If used as an interrupt, the user's software must be fast enough to clear the Heartbeat Flag each time a heartbeat occurs. Failure to do so will result in missed interrupts (if enabled) until the flag is cleared.

7.23 Reset Firmware

CAUTION:  *This command is for diagnostic purposes only. It should not be used during normal operation.*

Writing 0x004f to the command port causes the embedded firmware to reset. This command does not reset the hardware or the PCI bus interface. Wait at least eight seconds after sending this command before commanding or interrogating the board.

7.24 Assert/De-assert Reset

These commands are for diagnostic purposes only. Sending the Assert Reset command holds the hardware reset signal on the board in the asserted state. This stops the on-board CPU and clears the interrupt masks and Match and Heartbeat Flags. The only command that the board will respond to in this state is the De-assert Reset command. The PCI bus interface is not affected.

Send the Assert Reset command by writing any data value to location Base + 0x06. Send the De-assert Reset command by writing any data value to location Base + 0x04. Wait at least eight seconds after sending the De-assert Reset command before commanding or interrogating the board.

NOTE: After the Assert Reset command is sent, the diagnostic light on the rear panel stops flashing (it may be either lit or not lit). This can be used as an indication to determine if the user's software is capable of writing to the board (i.e., that the PCI bus addressing is working correctly).

Sending the De-assert Reset command without first sending an Assert Reset command will also reset the board.

8 Programming the TPRO/TSAT-66U

8.1 General Information

The universal PCI bus "sees" the board as a device that has 64 consecutive 32-bit memory locations (64 bytes) and 64 consecutive 32-bit I/O locations (64 bytes). During startup, the PCI BIOS (part of the host computer) mapped these locations somewhere in the absolute address space.

Two Base Address Registers (BAR's) are provided which permit the operating system (OS) driver to map the register space as both Memory and I/O on the PCI bus. BAR0 provides memory space mapping, while BAR1 maps as I/O. Both BARs are configured to request 64 bytes of space from the OS, corresponding to sixteen 32-bit registers.

The 64 memory locations and the 64 I/O locations serve exactly the same functions. In actual use, only one of these (either memory or I/O) is used; the other is ignored. On host computers with Intel CPUs (e.g., Pentium, 486, etc.) use the I/O locations. On host computers with Motorola CPUs (e.g., the 68000 family) use the memory locations (since Motorola does not have "I/O" instructions).

The locations of the board's registers are specified as "Base + Offset". The offsets are constants, as described in the next section. The "Base" is chosen by the PCI BIOS during startup. There is a separate "Base" for the memory and I/O locations.

Time is read as two 32-bit words, and is in binary-coded decimal format. Status is read as a single 32-bit word. Time tags and, for the TSAT, GPS information (longitude, latitude, altitude, and Gregorian date), are read by first sending a command to the board, then reading ten 32-bit words from a first-in-first-out (FIFO) register.

The user's software must wait a short amount of time after sending each command. This admittedly cumbersome requirement is necessary because the on-board processor places a higher priority on maintaining the time than on processing commands. The actual amount of time needed to process a command depends on when the command was received relative to the on-board time. Entries in Chapter Six specify the amount of time needed to assure that the command was received. There is no restriction on reading from the board.

Each 32-bit word is located on an even address. Although many of the registers use only eight bits, always read and write registers as 32-bit entities. **Do not attempt an 8-bit access on an odd address location.**

8.2 Register Locations

NOTE: In this manual, the prefix "0x" indicates that the number is in hexadecimal (Base 16) format.

Table 8.1—Register Locations for TPRO/TSAT-66U

Location	Read Usage	Write Usage	Register Function
Base + 0x00	FIFO	Interrupt Control Port	R - Returns response data from the board W - Interrupt control register
Base + 0x04	Status Register	Command Port	R - Returns status information for the board W - Issues commands to the board
Base + 0x08	H	De-assert Reset	Releases the board from reset
Base + 0x0c	H	Assert Reset	Places the board into reset
Base + 0x10	TIME_REG_LOW	H	Latches a snapshot of the present time and returns the lower portion of time
Base + 0x14	TIME_REG_HIGH	H	Returns upper portion of latched time and Status info
Base + 0x18	H	Clear Flags	Clears interrupt flags
Base + 0x1c	H	Simulate Time Tag	Simulates a time tag occurrence
Base + 0x20	FPGA_REV	H	Returns FPGA revision
Base + 0x24	H	H	
(H = Reserved for future use.)			

8.3 Using the FIFO

The board uses a FIFO register to provide multi-word responses. Each of these responses consists of ten 32-bit words, of which only the lower 8-bits are actually used. A bit in the Status Register indicates whether data is ready in the FIFO. The user's software must check that status bit before reading *each* word from the FIFO.

There can be a delay of up to 200 μS before all ten words are written into the FIFO. This is due to the fact that although the on-board CPU writes this data, it also maintains the time (days through milliseconds) in software, and places a higher priority on maintaining the time than on filling the FIFO. Thus, it is not uncommon that, for example, only three of the ten words are written into the FIFO, then, following a substantial delay, the remaining seven words are written. The user's software must allow for such operation (i.e., it must not “give up” just because it has not read all ten words before the status indicates that the FIFO is empty. Either wait 200 μS before beginning to read, or allow for enough retries if FIFO empty status is detected prematurely.)

To check the FIFO Ready flag, read the Status Register (at Base + 0x04). If the least significant bit is a zero, there is data in the FIFO. If this bit is a one, the FIFO is empty.

The FIFO holds 512 words (i.e., 51 responses). Letting these responses stack up in the FIFO is acceptable, but the user's software is responsible for knowing what each of the responses is.

During initialization, the user's software must flush the FIFO. Do this by reading the FIFO until the “FIFO Ready” flag is a one. This could take up to 512 reads, maximum.

Responses to user commands echo the command in the first two words from the FIFO. This can be useful in sorting out multiple responses that are stacked up in the FIFO.

8.4 Reading Clock Time

The current ("clock") time is read as two 32-bit words, TIME_REG_LOW and TIME_REG_HIGH. Reading the TIME_REG_LOW word latches both words, thus the latency time between reading them does not affect the accuracy. This also means that it is important to read TIME_REG_LOW first, as this causes the other word to be latched. It is not necessary to read both words if the application does not need the complete clock time.

NOTE: These locations are read-only. A different sequence is used to set the time. Refer to the sections on setting the clock time.

Reading TIME_REG_HIGH also returns 2 status flags, SYNC & TCODE. All the status flags can also be read from the status register which requires an additional register read.

The Julian date (not the Gregorian date) is reported.

The value range for Days is 000-366. Be sure the variable that stores Days can accommodate this range. Assigning Days to an 8-bit integer (with a range of 000-255) produces an unpleasant surprise in mid-September!

Within each 32-bit word there are eight "nibbles" (groupings of 8 bits each). Each nibble is decoded separately, representing a single binary-coded-decimal (Base 10) digit.

Table 8.2—Clock Time Data

Location	Nibble	Nibble	Nibble	Nibble
Base + 0x10	Seconds_Tens[31:28]	Seconds_Ones[27:24]	Msec_Hundreds[23:20]	Msec_Tens[19:16]
	Msec_Ones[15:12]	Usec_Hundreds[11:8]	Usec_Tens[7:4]	Usec_Ones[3:0]
Base + 0x14	0 **SYNC** **TCODE** 0	Days_Hundreds[27:24]	Days_Tens[23:20]	Days_Ones[19:16]
	Hours_Tens[15:12]	Hours_Ones[11:8]	Minutes_Tens[7:4]	Minutes_Ones[3:0]

SYNC – Set if clock is synced to Timecode or GPS and GPS positions is valid
TCODE – Set if Timecode input has a signal present

For example:

The time is day 123, hour 11, minute 58, second 17.654321
SYNC = 1
TCODE = 1

The time is read as follows:

Location	**Contents**
Base + 0x10 (TIME_REG_LOW)	0x17654321
Base + 0x14 (TIME_REG_HIGH)	0x 61231158

8.5 Sending Commands

Writing to the Command Port at Base + 0x04, sends commands to the board. A small delay is required after sending each word. Note that there is no way to “read back” a command once it has been sent.

Commands consist of one or more 32-bit words, of which only the lower 8-bits are actually used. These lower 8 bits are further divided into two 4-bit "nibbles". For some commands, the high nibble is a constant, and the low nibble contains the data. For other commands both the high and low nibbles are constant.

It is necessary to wait at least 100 μS after sending each command word before sending anything else to the command port.

Table 8.3—Command Functions	
Function	**Command**
Reset Firmware	0x0000004f
Enable Sync	0x0000004d
Disable Sync	0x0000004e
Report Firmware Version in FIFO	0x000000e9
Report Number of GPS Satellites in FIFO (TSAT only)	0x0000005c
Report Altitude & Gregorian Date in FIFO	0x0000005d
Report Longitude in FIFO (TSAT only)	0x0000005e
Report Latitude in FIFO (TSAT only)	0x0000005f
Clear Holding Register	0x000000f0
Put 10^2 Days in Holding Register	0x00000050–53
Put 10^1 Days in Holding Register	0x00000060–69
Put 10^0 Days in Holding Register	0x00000070–79
Put 10^1 Hours or 10^{-1} Seconds in Holding Register	0x00000080–89
Put 10^0 Hours or 10^{-2} Seconds in Holding Register	0x00000090–99
Put 10^1 Minutes, 10^{-3} Seconds, or 16^3 Heartbeat in Holding Register	0x000000a0–af
Put 10^0 Minutes, 10^{-4} Seconds, or 16^2 Heartbeat in Holding Register	0x000000b0–bf
Put 10^1 Seconds, 10^{-5} Seconds, or 16^1 Heartbeat in Holding Register	0x000000c0–cf
Put 10^0 Seconds, 10^{-6} Seconds, or 16^0 Heartbeat in Holding Register	0x000000d0–df
Put Propagation Delay 10^3 µS in Holding Register	0x00000030–39
Put Propagation Delay 10^2 µS in Holding Register	0x00000020–29
Put Propagation Delay 10^1 µS in Holding Register	0x00000010–19
Put Propagation Delay 10^0 µS in Holding Register	0x00000000–09
Copy Holding Register to Clock Time or Propagation Time	0x000000e0
Copy Holding Register to Start/Stop Time (Days-Seconds)	0x000000e1
Copy Holding Register to Start Time (10^{-1} to 10^{-6} Seconds)	0x000000e2
Copy Holding Register to Stop Time (10^{-1} to 10^{-6} Seconds)	0x000000e3
Copy Holding Register to Clock Time on next 1PPS (Option –M only)	0x0000004c
Copy Holding Register to Heartbeat, Pulse Mode, at next period	0x000000e5
Copy Holding Register to Heartbeat, Pulse Mode, immediately	0x000000e6
Copy Holding Register to Heartbeat, Square wave Mode, at next period	0x000000e7
Copy Holding Register to Heartbeat, Square wave Mode, immediately	0x000000e8
Copy Holding Register to Year	0x000000ea

8.6 Setting the Clock Time (Not Applicable to Option -M)

Set the clock time by commanding the days, hours, minutes, and seconds. The milliseconds and microseconds cannot be commanded; they are reset to 000000 when the command is sent.

It is necessary to load the time into the Holding Register. First, send a command to clear the Holding Register. Then, one at a time, write each digit (hundreds of days down to ones of seconds) into the Holding Register.

There is a separate command for loading each of these digits. The upper 4 bits of the command identify which digit is being loaded, the lower 4 bits contain the actual data to load. Once all the digits have been loaded, a command is sent to set the time (the board does this by copying the Holding Register into the clock).

For example, to set the clock to day 123, hour 11, minute 58, second 17, send the following sequence of commands to the Command Port:

```
0x000000f0                                  ; Clear the Holding Register
0x00000051    0x00000062    0x00000073      ; Day 123
0x00000081    0x00000091                    ; Hour 11
0x000000a5    0x000000b8                    ; Minute 58
0x000000c1    0x000000d7                    ; Second 17
0x000000e0                                  ; Set Clock Time
```

NOTE: If no timecode input is present (TPRO), or the GPS receiver is not tracking satellites (TSAT), the board will accept the time set sequence described above and continue to increment time ("freewheel").

However, when a valid timecode (TPRO) is input, or when the GPS receiver begins tracking satellites (TSAT), the clock's time will jump to the decoded time, unless the above sequence was preceded with a Disable Sync command (described later in this chapter).

While freewheeling, the In-Sync status bit will be false.

The user's software must ensure that the commanded values are in the appropriate ranges. The board does not error-check the data before loading the clock. Commanding invalid values (e.g., 39 hours) causes erratic operation.

8.7 Setting the Clock Time (TPRO Option -M Only)

Set the clock time by commanding the days, hours, minutes, and seconds. The milliseconds and microseconds cannot be commanded; they are reset to 000000 when the *next* 1PPS occurs. The clock time of the *next* 1PPS is commanded to the board.

It is necessary to load the time into the Holding Register. First, send a command to clear the Holding Register. Then, one at a time, write each digit (hundreds of days down to ones of seconds) into the Holding Register.

There is a separate command for loading each of these digits. The upper 4 bits of the command identify which digit is being loaded, the lower 4 bits contain the actual data to load. Once all the digits have been loaded, a command is sent to arm the clock.

For example, to set the clock to day 123, hour 11, minute 58, second 17, send the following sequence of commands to the Command Port:

```
0x000000f0                                  ; Clear the Holding Register
0x00000051    0x00000062   0x00000073       ; Day 123
0x00000081    0x00000091                    ; Hour 11
0x000000a5    0x000000b8                    ; Minute 58
0x000000c1    0x000000d7                    ; Second 17
0x0000004c                                  ; Arm the clock for next 1PPS
```

After sending the 0x0000004c command, the board sets the milliseconds and microseconds to 000000 when the first 1PPS occurs (the seconds do not increment). Then, on the second 1PPS pulse, the time (seconds) begins to increment.

CAUTION:



The board expects the 1PPS input to be continuous. If the 1PPS signal stops pulsing after the board establishes initial sync, the board will continue to increment time ("freewheel"). However, if the 1PPS signal resumes after a period of freewheeling, the board may reset the clock time to 000:00:00:00.000000. This is because the 1PPS occurs outside of a narrow window in which the board expects it, either because the 1PPS has moved or because the board's time has drifted during freewheeling.

The arm command (0x0000004c) must be sent no sooner than 50 mS after the previous 1PPS occurred, and no later than 50 mS before the next (arming) 1PPS occurs.

NOTE: If both 1PPS and Timecode inputs are present, the board will sync to the incoming timecode and ignore the 1PPS. IRIG-A is not supported when this option is enabled.

Commands 0x0000004d and 0x0000004e (Enable/Disable Sync) apply both to the 1PPS and the timecode input. Commands 0x000000e0 (set clock) and 0x000000ea (set year) are not applicable to boards with Option –M.

The user's software must ensure that the commanded values are in the appropriate ranges. The board does not error-check the data before loading the clock. Commanding invalid values (e.g., 39 hours) will cause erratic operation.

8.8 Setting the Year (Not Applicable to Option -M)

Whether the IRIG-B output is synchronized to GPS or timecode, or is freewheeling, it counts from day 365 to day 001, unless the year is set to a leap year. Once set to a leap year, the IRIG-B output counts from 365 to 366, then to 001.

The TSAT acquires the year from the GPS satellites. The year can also be set by command (if the GPS receiver is not connected).

To function properly, the TPRO requires that the year be set by command at the end of a leap year. The board will increment the year when the day rolls over to 001. Also, setting the year enables the board (TPRO and TSAT) to compute the Gregorian date using the year and Julian date.

Set the year by sending the command sequence "0x0000006n 0x0000007n 0x0000008n 0x0000009n 0x000000ea" to the command port. For example, to set the year to 2003, send "0x00000062 0x00000070 0x00000080 0x00000093 0x000000ea".

The year is reset to 0000 when power is first applied, or when any of the following occur: system reset, firmware reset (command 0x0000004f), or writing to the "Assert Reset" or "De-assert Reset" addresses.

8.9 Reading the Year, Gregorian Date and Altitude (Not Applicable to Option -M)

The GPS receiver's computations for the altitude (TSAT only) and Gregorian date (TSAT and TPRO) are reported in the FIFO in response to the 0x0000005d command. Altitude is in units of meters relative to mean sea level.

Word	Bits 7– 4	Bits 3 – 0
0 (first)	5	D
1	5	D
2	10^1 Day	10^0 Day
3	10^5 meters	10^4 meters
4	10^3 meters	10^2 meters
5	10^1 meters	10^0 meters
6	10^{-1} meters	0
7	10^1 Year	10^0 Year
8	10^3 Year	10^2 Year

9 (last)	10^1 Month	10^0 Month

The board increments the Gregorian date approximately one second after time rolls over from 23:59:59 to 00:00:00 (HH:MM:SS). This occurs on every date in every year. Consequently, the Gregorian date should not be used during minutes 59 and 00—this will avoid rollover problems.

8.10 Report Longitude (TSAT Only)

The GPS receiver's computation for longitude is put into the FIFO in response to the 0x005e command. The units are degrees, minutes, and fractions of minutes. The response is in the following format:

Word	Bits 7–4	Bits 3–0
0 (first)	5	e
1	5	e
2	0	10^2 Degrees
3	10^1 Degrees	10^0 Degrees
4	10^1 Minutes	10^0 Minutes
5	10^{-1} Minutes	10^{-2} Minutes
6	10^{-3} Minutes	10^{-4} Minutes
7	Reserved	Reserved
8	Reserved	Reserved
9 (last)	Reserved	Reserved

NOTE: If the reported value is less than 180 degrees, the longitude is East (for Europe, Africa, Asia, etc.). If the reported value is greater than or equal to 180 degrees, subtract 180 degrees to obtain west longitude (for USA, Canada, Central & South America, etc.). For example, the reported value for Los Angeles, CA, USA, will be approximately 298 degrees. Since this is greater than 180, subtract 180 to get the correct value, i.e., 118 degrees West. Be sure to convert minutes to decimal degrees before comparing to 180 degrees.

8.11 Report Latitude (TSAT Only)

The GPS receiver's computation for latitude is put into the FIFO in response to the 0x005f command.

The units are degrees, minutes, and fractional minutes. Latitudes north of the equator are reported as 0–90 degrees, latitudes south of the equator are reported as 180+ degrees South—i.e., if the reported value is greater than or equal to 180, subtract 180 degrees and change the sign to negative (south). It is important to convert minutes to decimal degrees before comparing to 180 degrees. The response is in the format shown here:

Word	Bits 7–4	Bits 3– 0
0 (first)	5	f
1	5	f
2	0	10^2 Degrees
3	10^1 Degrees	10^0 Degrees
4	10^1 Minutes	10^0 Minutes
5	10^{-1} Minutes	10^{-2} Minutes
6	10^{-3} Minutes	10^{-4} Minutes
7	Reserved	Reserved
8	Reserved	Reserved
9 (last)	Reserved	Reserved

8.12

8.13 Report Number of GPS Satellites Being Tracked (TSAT Only)

The GPS receiver determines automatically which satellites to track. The number (quantity) of satellites being tracked is reported in the FIFO in response to sending command 0x005c to the command port. The response is of the form shown here:

Word	Bits 7–4	Bits 3 – 0
0 (first)	5	c
1	5	c
2	Reserved	Reserved
3	Reserved	Reserved
4	Reserved	Reserved
5	Reserved	Reserved
6	Reserved	Reserved
7	0	# of Satellites
8	Reserved	Reserved
9 (last)	Reserved	Reserved

NOTE: The number of satellites tracked is for diagnostic purposes only. The number of satellites ranges from 0 to 8, inclusive. Valid time and position require that at least four satellites be tracked. The In-Sync flag in the Status Register must be used to actually determine whether the board is synchronized and providing valid position.

There is no difference in timing accuracy when 5, 6, 7, or 8 satellites are being tracked. It is normal for the number to fluctuate between 5 and 8, given that the GPS receiver picks different satellites to optimize the timing.

It is normal for the number of satellites to be between 0 and 3 during acquisition and re-acquisition.

8.14 Enable/Disable Sync

The board can be forced to freewheel by sending the "Disable Sync" command. Sending this command causes the board to ignore the timecode input, the 1PPS input (Option –M only), and the GPS input (TSAT only).

To restore normal operation, send the "Enable Sync" command.

To send the Disable Sync command, write 0x0000004e to the command port. To send the Enable Sync command, write 0x0000004d to the command port.

The power-on default is to Enable Sync.

8.15 Reading the Status Register

The Status Register consists of one 32-bit word, of which only the lower 8 bits are used. The Status Register is read from location Base + 0x04, and is formatted as shown in Table 8.4.

Table 8.4—Status Register Format

Bit	Name	Meaning When "0"	Meaning When "1"
0 (LSB)	FIFO Ready Flag	FIFO Ready (data available)	FIFO empty
1	Timecode Present	Timecode Input has no detectable signal	Timecode input has a signal present
2	In-sync Flag	Clock is freewheeling GPS position is invalid	Clock is synced to timecode or GPS and GPS position is valid
3	Match Flag	Start time has not occurred	Start time has occurred
4	Heartbeat Flag	Heartbeat has not occurred	Heartbeat has occurred
5	Heartbeat Int. Mask	PCI bus interrupt disabled for heartbeat	PCI bus interrupt occurs on each heartbeat
6	Match Int. Mask	PCI bus interrupt disabled for start time	PCI bus interrupt occurs at the start time
7	FIFO Ready Int. Mask	PCI bus interrupt disabled for FIFO data available	PCI bus interrupt occurs when FIFO data available
8–31	(Reserved)	(Reserved)	(Reserved)

NOTE: Bit 2 (In-Sync Flag) is the only bit to examine when determining the validity of the time (and position for TSAT).

Bit 1 (Timecode Present) is for diagnostic purposes only. It indicates only that the amplitude of the timecode input is adequate for detection. It does not indicate whether the input is valid. For TSAT, this bit will always be zero.

Bits 5, 6, and 7 provide a means for reading back the corresponding bits in the Interrupt Control Port.

Bits 3 and 4 may be true ("1") when power is first applied. The user's software must clear bits 3 and 4 before using them.

8.16 Interrupt Control Port

The board can generate interrupts when the FIFO has data, when each heartbeat occurs, and/or when the commanded Start Time occurs. Each of these is enabled separately via the Interrupt Control Port, and any, all, or none can be enabled simultaneously.

The Interrupt Control Port is a single 32-bit word, of which only 3 bits are actually used. It is located at Base + 0x00, and is write-only. The bits in the Interrupt Control Port are defined as shown in Table 7.5.

Table 8.5—Interrupt Control Port Bit Definitions

Bit	Name	Writing "0" Action	Writing "1" Action
0–4	(Reserved)	(Reserved)	(Reserved)
5	Heartbeat Interrupt Mask	No PCI interrupt on heartbeat	Heartbeat causes PCI interrupt
6	Match Interrupt Mask	No PCI interrupt at start time	Start time causes PCI interrupt
7	FIFO Ready Int. Mask	No PCI interrupt when data is available in FIFO	PCI interrupt when data is available in FIFO
8–31	(Reserved)	(Reserved)	(Reserved)

The board generates the same interrupt regardless of whether it was caused by heartbeat, start time, or FIFO data available. After an interrupt, the user's software must interrogate the board to determine which of these was the cause.

The power-on default is to have all interrupts disabled. Also, sending the "Assert Reset" command disables all interrupts.

CAUTION:



The "FIFO Ready" interrupt occurs each time the FIFO changes from being empty to containing data. If the user's software detects quickly that the first word has been written into the FIFO and reads it out, it is possible that the FIFO will be empty for a moment. Thus, when the second word is put into the FIFO, it generates another interrupt.

The solution is to disable the FIFO Ready interrupt until all 10 words have been read from the FIFO, then re-enable the interrupt.

8.17 Setting the Propagation Delay Correction

This command is used to correct for delays that are due to cable length (timecode or GPS cables). Most applications do not need to compensate for cable delays because the delay is on the order of a hundred nanoseconds, while the clock's resolution is 1 microsecond. However, introducing a deliberate (large) offset can be helpful in situations in which the board is used to trigger an instrument slightly *before* a particular time.

The range of the propagation correction is –1000 µS to +8999 µS. The power-on default is zero.

To specify the propagation delay, first clear the Holding Register, then write four words (representing each of the digits in the delay value), then send the "Set Clock Time/Propagation Time" command. A special number sequence is used to specify negative delays. To specify delays from –1000 µS to – 1 µS send values of 9000 to 9999, respectively. For example, to specify a correction of +4567 µS, send the following sequence of commands to the command port:

```
0x000000f0                          ; Clear the Holding Register
0x00000034  0x00000025              ;
            0x00000016  0x00000007  ; Specifies +4567 µS
0x000000e0                          ; set propagation correction
```

8.18 Setting the Start/Stop ("Match") Times (Not Applicable to Options -FXA, -FXB, or –HDRV)

The **match output** (P1 Pin 8) goes high at the Start time and low at the Stop time. The **match interrupt** occurs at the Start time (not at the Stop time). The **match flag** (in the Status Register) goes true at the Start time and remains true until the user clears it with a software command.

To specify the Start and Stop times, first clear the Holding Register, then command the days-through-seconds portion of the time, send a set command, next send the milliseconds through microseconds, finally, send another set command.

For example, to command a Start time of day 123, hour 11, minute 58, second 17.456789, send the following sequence to the command port:

```
0x000000f0                                  ; Clear Holding Register
0x00000051     0x00000062    0x00000073     ; Day 123
0x00000081     0x00000091                   ; Hour 11
0x000000a5     0x000000b8                   ; Minute 58
0x000000c1     0x000000d7                   ; Second 17
0x000000e1                                  ; send days-seconds
0x00000084     0x00000095    0x000000a6     ; xx.456xxx seconds
0x000000b7     0x000000c8    0x000000d9     ; xx.xxx789 seconds
0x000000e2                                  ; send Start time
```

To specify the Stop time, the sequence is the same, but the final command is 0x000000e3 (instead of 0x000000e2). The sequence must be completed at least 50 mS before the

commanded time occurs. The match output and interrupt (if enabled) operates regardless of whether the board is in-sync or freewheeling.

8.19 Programming the Heartbeat Output (Not Applicable to -HB1PPS, -FXA, -FXB, -LOR1 Options)

The heartbeat output (P1 Pin 6) can be programmed to be either a pulse or a square wave. The specified rate must be an exact multiple of 1.000 μS. The range of programmable rates is:

Minimum Rate *(lowest frequency)* .....21.845 mS (45.7771 Hz)
Maximum Rate *(highest frequency)* .....1.000 μS (1.000 MHz)
Pulse Width *(time low, pulse mode only)*..... 150 nS min, 450 nS max (negative polarity)

To specify the rate (or frequency), compute the divide number N as follows. Note that N must be exactly divisible by 3, meaning that the specified period must be an exact multiple of 1.000 μS.

To specify a period for a pulse or square wave, compute N as:
$N = 3t/10^{-6}$ t is the period in seconds

To specify a frequency for a pulse or square wave, compute N as:
$N = 3 * 10^{6}/F$ F is the frequency in Hertz

Not all values of N are acceptable. Verify that the computed value is evenly divisible by 3 and that it is in the range of 3 to 65,535, inclusive.

Convert N into hexadecimal (Base 16) notation. For example, if the desired output frequency is 10 kHz, N=300 (Base 10), converted to hexadecimal notation yields N=0x012c. Send the hexadecimal number to the board by outputting the following sequence to the command register.

```
0x000000f0                                          ; Clear the Holding Register
0x000000a0    0x000000b1  0x000000c2  0x000000dc    ; specifies N = 0x012c
```

The heartbeat output can be programmed for a square wave or a pulse, and can be programmed either to start immediately, or at the beginning of the next cycle. Send one of the following commands to command port:

```
0x000000e5        ; Pulse mode, starts at beginning of next cycle
0x000000e6        ; Pulse mode, starts immediately
0x000000e7        ; Square wave, starts at beginning of next cycle
0x000000e8        ; Square wave, starts immediately
```

The heartbeat output is present whether the board is in-sync or is freewheeling.

The power-on default is 100 PPS, pulse mode.

8.20 Programming the Heartbeat Output (For Options -HB1PPS, -FXA, -FXB, and -LOR1 Only)

The heartbeat output (P1 Pin 6) can be programmed to be either a pulse or a square wave. The specified rate must be an exact multiple of 1.000 mS. The range of programmable rates is:

```
Minimum Rate (lowest frequency):            65.534 Seconds (0.0152593 Hz)
Maximum Rate (highest frequency):           2 mS (500 Hz)
Pulse Width (time low, pulse mode only):    1 mS (typical)
Programming Resolution:                     1 mS
```

To specify the rate (or frequency), compute the divide number N as follows.

To specify a period for a pulse or square wave, compute N as follows:

N = t/.001 t is the period in seconds

To specify a frequency for a pulse or square wave, compute N as follows:

N = 1000/F F is the frequency in Hertz

Verify that the computed value is in the range of 2 to 65,534, inclusive.

Convert N into hexadecimal (Base 16) notation. For example, if the desired output period is once every 25 seconds, N=25,000 (Base 10), converted to hexadecimal notation yields N=0x61a8. Send the hexadecimal number to the board by outputting the following sequence to the command register.

```
0x000000f0                                      ; Clear the Holding Register
0x000000a6  0x000000b1 0x000000ca 0x000000d8 ; specifies N = 0x61a8
```

The heartbeat output can be programmed for a square wave or a pulse, and can be programmed to start immediately or at the beginning of the next cycle. Send one of the following commands to command port:

```
0x000000e5      ; Pulse mode, starts at beginning of next cycle
0x000000e6      ; Pulse mode, starts immediately
0x000000e7      ; Square wave, starts at beginning of next cycle
0x000000e8      ; Square wave, starts immediately
```

The heartbeat output is present regardless of whether the board is in-sync or freewheeling.

The power-on default is 1PPS, pulse mode.

8.21 Using the Time Tag Input

When the rising edge of the Time Tag Input (P1 Pin 4) occurs, the clock time is latched into a temporary register, and this register is then loaded into the FIFO. An interrupt on the PCI bus is generated, if enabled. The user's software establishes that a time tag has occurred in one of two ways: either by examining the least significant bit of the Status Register (FIFO Ready flag) to determine if it is a zero, or by waiting for an interrupt. Since the clock time is latched when

the rising edge occurs, the Time Tag data will be correct regardless of how long it takes to read the FIFO.

For test purposes, a time tag event can be simulated by writing (any value) to Base + 0x1C. The result is indistinguishable from a time tag event on P1 Pin 4.

The FIFO response to either of these events is shown here:

Word	Bits 7–4	Bits 3–0
0 (first)	0	0
1	0	0
2	0	10^2 Days
3	10^1 Days	10^0 Days
4	10^1 Hours	10^0 Hours
5	10^1 Minutes	10^0 Minutes
6	10^1 Seconds	10^0 Seconds
7	10^{-1} Seconds	10^{-2} Seconds
8	1^{-3} Seconds	10^{-4} Seconds
9 (last)	1^{-5} Seconds	10^{-6} Seconds

For example, if the time tag occurs at day 123, hour 11, minute 58, second 17.456789, the contents read from the FIFO will be:

```
Word        Contents
0 (first)   0xUU00      U = Unknown)
1           0xUU00
2           0xUU01
3           0xUU23
4           0xUU11
5           0xUU58
6           0xUU17
7           0xUU45
8           0xUU67
9 (last)    0xUU89
```

NOTE: The Julian date (not the Gregorian date) is reported.

Erratic operation may result if the rate of the time tags exceeds 1000 per second.

There may be a delay of up to 200 µS before time tag data is available in the FIFO.

Some older boards repeated words 2 and 3 in bytes 0 and 1, respectively.

8.22 Report Firmware Version

The version of the embedded firmware is reported in the FIFO in response to the 0x000000e9 command. For example, firmware version 7A104221 is reported as shown below.

Word	Bits 7–4	Bits 3– 0
0 (first)	E	9
1	E	9
2	7	A
3	1	0
4	4	2
5	2	1
6	Unknown	Unknown
7	Unknown	Unknown
8	Unknown	Unknown
9 (last)	Unknown	Unknown

NOTE: The Firmware version is for diagnostic purposes only. It is not possible to determine which options are present, or which version is more recent, by examining the version number.

The firmware version is also printed on the label on device U19.

Some older boards ignore the 0x00e9 command.

8.23 Report FPGA Version

The FPGA_REV register is a read-only register consisting of one 32-bit word, of which only the lower 16 bits are used. Each byte comprises of a portion of the revision. The FPGA_REV Register is read from location Base + 0x20, and is formatted as shown below.

Table 8.6—FPGA_REV

Location	Nibble	Nibble	Nibble	Nibble
Base + 0x20	0x00 [31:24]	0x00 [23:16]	Major_Rev [15:8]	Minor_Rev [7:0]

Example: If FPGA Revision = 01.00

Major_Rev = 01
Minor_Rev = 00

8.24 Clear Flags Port

Once the Match and/or Heartbeat flag(s) get set, it is necessary to clear the flag by writing a “1” to the appropriate bit of this register at location Base + 0x10.

Table 8.7—Interrupt Control Port Bit Definitions

Bit	Name	Writing “0” Action	Writing “1” Action
0–2	(Reserved)	(Reserved)	(Reserved)

Table 8.7—Interrupt Control Port Bit Definitions			
3	Clear Match	Match flag does not change	Clear match flag to zero
4	Clear Heartbeat	Heartbeat flag does not change	Clear heartbeat flag to zero
5–31	(Reserved)	(Reserved)	(Reserved)

NOTE: If used as an interrupt, the user's software must clear the Match Flag each time the Start time occurs. Failure to do so will result in missed interrupts (if enabled) until the flag is cleared.

If used as an interrupt, the user's software must be fast enough to clear the Heartbeat Flag each time a heartbeat occurs. Failure to do so will result in missed interrupts (if enabled) until the flag is cleared.

8.25 Reset Firmware

CAUTION:  *This command is for diagnostic purposes only. It should not be used during normal operation.*

Writing 0x0000004f to the command port causes the embedded firmware to reset. This command does not reset the hardware or the PCI bus interface. Wait at least eight seconds after sending this command before commanding or interrogating the board.

8.26 Assert/De-assert Reset

These commands are for diagnostic purposes only. Sending the Assert Reset command holds the hardware reset signal on the board in the asserted state. This stops the on-board CPU and clears the interrupt masks and Match and Heartbeat Flags. The only command that the board will respond to in this state is the De-assert Reset command. The PCI bus interface is not affected.

Send the Assert Reset command by writing any data value to location Base + 0x0C. Send the De-assert Reset command by writing any data value to location Base + 0x08. Wait at least eight seconds after sending the De-assert Reset command before commanding or interrogating the board.

NOTE: After the Assert Reset command is sent, the diagnostic light on the rear panel stops flashing (it may be either lit or not lit). This can be used as an indication to determine if the user's software is capable of writing to the board (i.e., that the PCI bus addressing is working correctly).

Sending the De-assert Reset command without first sending an Assert Reset command will also reset the board.

9 Options and Accessories

9.1 Options

Refer to *Configuration* for the jumper settings that support the options herein.

9.1.1 -DCLOBNC

This option provides an IRIG-B, DCLS output on the J2 BNC connector and P1 D-type connector Pin 9. The BNC or the 15-pin D-type connector provides a DC level shifted output with the rising edge on time. The modulated IRIG-B output is eliminated with this option.

9.1.2 -HB1PPS (Cannot Be Combined with Options -FXA, -FXB, -HDRV)

This option provides a 1PPS on the heartbeat output at power up. The heartbeat output (P1 Pin 6) can be programmed as either a pulse or a square wave. The specified rate must be an exact multiple of 1.000 mS. The range of programmable rates is:

Minimum Rate *(lowest frequency)* ..... 65,534 Seconds (0.0152593 Hz)
Maximum Rate *(highest frequency)* .....2 mS (500 Hz)
Pulse Width *(time low, pulse mode only)* .....1 mS (typical)
Programming Resolution .....1 mS

The default rate at power-up is 1Hz, pulse mode.

9.1.3 -FXA (TSAT Only; Cannot Be Combined with Options -HB1PPS, -HDRV)

This option provides an RS-422 driver for the Heartbeat Output, and provides the same range of pulse rates as the –HB1PPS Option. The 15-pin, D-type connector provides the Heartbeat Output on Pin 6 (normally low, pulses high) and Pin 8 (normally high, pulses low). The rising edge of Pin 6 (falling edge of Pin 8) is *on-time*. The pulse width is approximately 1 mS. The power-on default pulse rate is once per second (1PPS). The Match function can still be used to provide an interrupt, if desired. However, the Match Output Pin has been eliminated. There are *no jumpers* installed on Header JP9.

9.1.4 -FXB (TPRO Only; Cannot Be Combined with Options -HB1PPS, -HDRV)

This option provides an RS-422 driver for the Heartbeat Output, and provides the same range of pulse rates as the –HB1PPS Option. The 15-pin, D-type connector provides the Heartbeat Output on Pin 6 (normally low, pulses high) and Pin 8 (normally high, pulses low). The rising edge of Pin 6 (falling edge of Pin 8) is *on-time*. The pulse width is approximately 1 mS. The power-on default pulse rate is once per second (1PPS). The Match function can still be used to provide an interrupt, if desired. However, the Match Output Pin has been eliminated. There are *no jumpers* installed on Header JP9.

9.1.5 -LOR1

This option provides the board with three different outputs on a three-pin header; a 1 Megahertz Output (1MHZ), 1 Pulse Per Second Output (1PPS), and a Ground Output. The 3-pin header is located on JP11 Pins 6, 7, and 8.

The 3-pin header designations are:

- JP11 Pin 6 is 1MHZ
- JP11 Pin 7 is 1PPS
- JP11 Pin 8 is Ground

9.1.6 –M (TPRO Only)

Option –M synchronizes to an external 1PPS input instead of the standard IRIG timecode input. The external 1PPS signal is connected to Pin 15 of the DB15 connector (P1). Ground is connected to either Pin 5 or Pin 7 of the connector. The timing card will detect the presence of the 1PPS signal automatically, so no configuration changes are required for the card to use the 1PPS signal.

The presence of the 1PPS signal is indicated by the onboard LED (LED1) status pattern. Refer to Table 5.1 for more information concerning LED flash patterns.

NOTE: The 10 MHz output is eliminated. If both 1PPS and IRIG-B timecode inputs are present, the board will synchronize to the incoming timecode and ignore the 1PPS. IRG-A is not supported when option –M is enabled.

9.2 Accessories

9.2.1 GPS Optic Isolator

This option provides fiber optic technology for voltage secure environments.

9.2.2 GPS Cables

Contact Spectracom for more information on GPS cable length options.

10 Driver Support

Please contact your sales representative for information about Spectracom's bus-level timing board driver support for Windows, Linux, Solaris and a variety of other platforms. You may also visit our website at www.spectracomcorp.com to download datasheets and manuals.

REVISION HISTORY

Revision Level	*ECN Number*	*Description*
A	**2225**	First iteration of this Spectracom product documentation.
B	**2248**	Added FCC compliance statement.
C	**2316**	PCI-33U product name changed to PCI-U-2.
D	**2332**	Minor corrections.

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