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SMT339 I/O MODULE
USER DOCUMENT

AUTHOR	**PC Pelser**
DATE	**04/12/98**
FILENAME	**SMT339_UserDoc**

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AMENDMENT RECORD

ISSUE	CHANGE NOTE	REMARKS	DATE OF ISSUE	AUTHOR	SIGNATURE
Draft 0.0	-	First internal issue	24 April 1998	PC Pelser	
Draft 0.1	I/Os	Second internal issue	25 May, 1998	PC Pelser	
Version 1.0	Connectors	First external issue	19 November, 1998	PC Pelser	

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1. SCOPE

This document describes the SMT339 I/O TIM module and is intended for use by the user of the SMT339 module.

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2. TECHNICAL DESCRIPTION

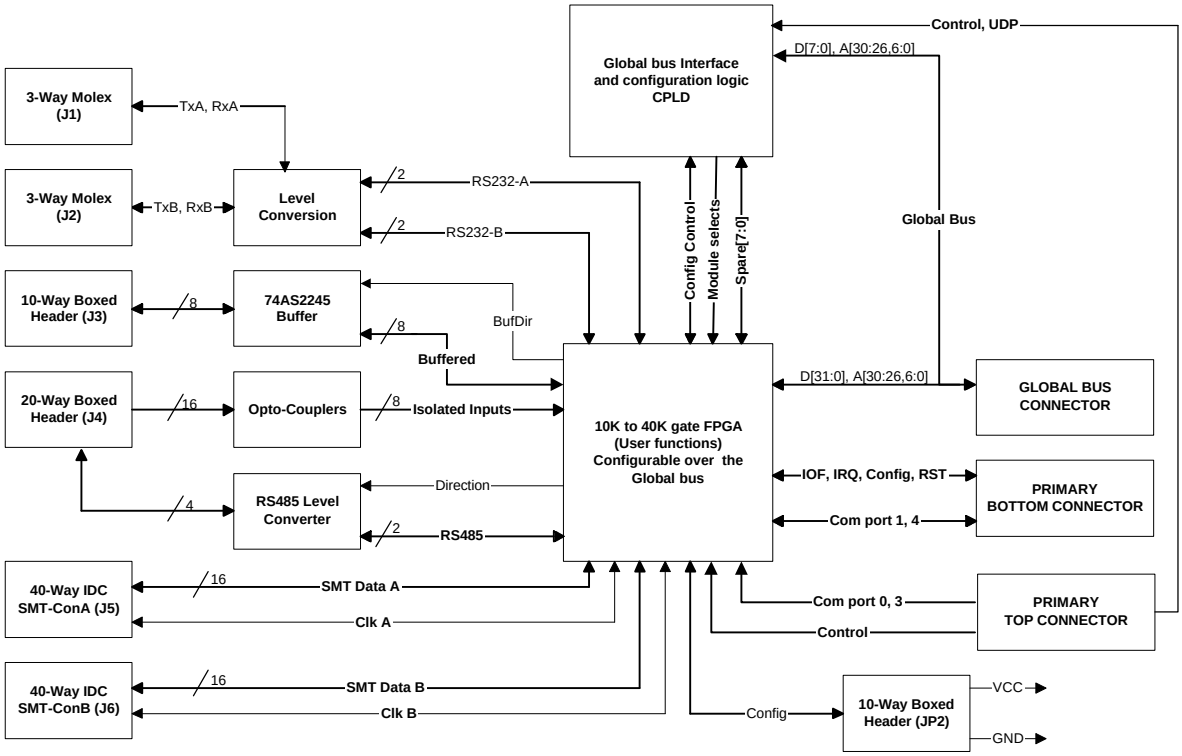


Fig. 1: *SMT339 Block diagram.*

Figure 1 shows the block diagram of the SMT339 I/O module. The following section describes the SMT339 from a user's point of view. Reference is made to the different blocks in Figure 1.

The SMT339 provides opto-coupled, RS485 and TTL I/Os on a standard single TIM site. These I/Os are available to processors via the global bus or Com Port 0,1,3 OR 4. Two 40-way miniature IDC connectors provide bi-directional 16-bit data paths, compatible with the SMT340 and SMT324 IDC connectors. The opto-coupled inputs are connected to a standard 20-way boxed header together with the four RS485 lines.

The 20-way Boxed header provides 8 differential inputs, which are opto-coupled through HCPL2201 high-speed opto-couplers. The HCPL2201 opto-coupler outputs (8) are connected to a FPGA. These inputs provide the module with the capability to monitor 8 opto-coupled inputs. This connector also provides two RS485 lines. The converted RS485 (TTL) are connected to the FPGA which controls the RS485 direction.

The 10-way Boxed header provides an 8-bit buffered data-path. The data-path is buffered with 74AS2245 buffers with internal 25 series resistors in the transmit path. These buffers could be used to drive the opto-couplers of a remote board, or the buffered input of a remote board. The buffer's direction is also under control of the FPGA.

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Two 3-pin Molex connectors are provided for the two full-duplex RS232 serial communication lines. The RS232 levels are converted to TTL before connecting to the FPGA. Standard and specialised UARTs can easily be implemented in the FPGA.

The FPGA can be configured from its own PROM during start-up, or it can be configured over the global bus via the CPLD. Configuration of the CPLD will allow a system to dynamically change the FPGA firmware. The FPGA drives 8 LEDs, and is connected to it's own local oscillator package.

The FPGA firmware will be user defined, and can be done on demand. All information will be provided to users who prefer to implement their own firmware. Typical functions that can be implemented in the FPGA are:

- Full bi-directional global-bus interface
- Full bi-directional com-port interface
- RAM, FIFOs, Dual port RAMs up to a total of 16K bits
- Communication protocols
- Controllers
- DSP pre-processors
- Any digital function that will fit in this size device
- The FPGA provides a total of 2300 registers excluding RAM
- Each register has its own associated 4-input look up table

The SMT339 TIM can typically be used to interface with a SMT342 over the global bus. The SMT339 can then perform customer specific data formatting before sending it to a nearby C40 TIM via com-port.

Due to the parallel nature of a FPGA it is well suited to handle multiple high-speed I/O lines. The FPGA can then provide a cleaner bus-interface to the associated DSP processors.

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3. SMT339 SPECIFICATIONS

The following important specifications should be noted when using the SMT339.

Description	Specification
Opto-coupled inputs	
Forward input voltage	3Volt (to provide 800mV on opto-coupler)
Minimum forward current for switch-on	2.2mA
Maximum forward current	10mA
Anode serial resistance	1KΩ
Maximum working insulation voltage	600Vpeak
Highest transient over-voltage	6000V
Maximum signal rate	5Mbd
RS485 inputs	
Voltage levels	RS422 compatible
Digital bi-directional bus	
Current driving capability	25mA sink and source
Voltage levels	TTL compatible

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4. USER CONFIGURATION

4.1 Configuration switch S1

Configuration switch S1 is used to set default start-up conditions.

Table 1 : *Configuration switch S1*.

Bits	Description	Selection
4:1	SMT339 base address	Compared to address bits 30 to 27
8:5	To FPGA via spares	User defined

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5. SMT339 CONNECTOR DEFINITIONS

The pin-outs for Connectors J5 and J6 are shown in table 2. J5 connects to all A signals while J6 connects to all B signals

Table 2 : *Connector J5 and J6 definition (40-way IDC).*

Pin	Signal	Pin	Signal
1	ClkA/B	2	GND
3	SMTDataA/B0	4	GND
5	SMTDataA/B1	6	GND
7	SMTDataA/B2	8	GND
9	SMTDataA/B3	10	GND
11	SMTDataA/B4	12	GND
13	SMTDataA/B5	14	GND
15	SMTDataA/B6	16	GND
17	SMTDataA/B7	18	GND
19	SMTDataA/B8	20	GND
21	SMTDataA/B9	22	GND
23	SMTDataA/B10	24	GND
25	SMTDataA/B11	26	GND
27	SMTDataA/B12	28	GND
29	SMTDataA/B13	30	GND
31	SMTDataA/B14	32	GND
33	SMTDataA/B15	34	GND
35	NC	36	GND
37	StrbA/B	38	GND
39	NC	40	GND

The pin-outs for the RS232 Connectors J1 and J2 are shown in table 3

Table 3 : *Connector J1 and J2 definition (3-way Molex).*

Pin	Signal
1	RS232-RX
2	GND
3	RS232-TX

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The pin-outs for the buffered data Connector J3 are shown in table 4

Table 4 : *Connector J3 definition (10-way boxed header).*

Pin	Signal	Pin	Signal
1	Buffer	2	GND
3	Buffer	4	Buffer
5	Buffer	6	Buffer
7	Buffer	8	Buffer
9	GND	10	Buffer

The pin-outs for the isolated/RS485 data Connector J4 are shown in table 5

Table 5 : *Connector J4 definition (20-way boxed header).*

Pin	Signal	Pin	Signal
1	RS485AN	2	RS485AP
3	OptoN0	4	OptoP0
5	OptoN1	6	OptoP1
7	OptoN2	8	OptoP2
9	OptoN3	10	OptoP3
11	OptoN4	12	OptoP4
13	OptoN5	14	OptoP5
15	OptoN6	16	OptoP6
17	OptoN7	18	OptoP7
19	RS485BN	20	RS485BP

The pin-outs for the configuration/power Connector JP2 are shown in table 6

Table 6 : *Connector JP2 definition (10-way boxed header).*

Pin	Signal	Pin	Signal
1	JTAG – TCK	2	GND
3	JTAG - TDO	4	VCC
5	JTAG - TMS	6	NC
7	NC	8	NC
9	JTAG - TDI	10	GND

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6. UPGRADE OPTIONS

The FPGA firmware is user definable. Different implementations can be done on demand.

The standard SMT339 has an EPF10K20RC240–4 speed grade FPGA mounted, but faster speed grades can be used where applicable. The SMT339 can also be ordered with a bigger FPGA, up to an EPF10K70RC240-1 if required.

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