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PAS 9796/DIO
ENGINEERING SPECIFICATION

160 CHANNEL
VME DIGITAL INPUT / OUTPUT CARD
Revision B (06/16/2000)

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160 Channel
VME Digital Input / Output Card

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160 Channel
VME Digital Input / Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9796/DIO is a VME based, 160 Channel, TTL level, Digital Input / Output card. One hundred twenty-eight of the channels are arranged as 16 byte wide bi-directional data ports. Each port consists of an eight-bit output data register with output enable, and an eight bit input buffer. The input buffers always monitor the state of the I/O lines, and the output data registers can either drive the I/O lines, or disconnect from the I/O by assuming a high impedance state. Individual data ports can be programmed for input or output by clearing or setting the appropriate bits in the output enable registers. When the data port is configured as an output the state of the output lines can be read back with the input register.

Sixteen flag I/O channels are available that can either be used as interrupt acknowledge lines or as general purpose I/O. Flag channels have the same drive capability and configurability as the data ports. The direction of the flag channels is controlled with two bits in the Control and Status Register. Jumper plugs can be installed to bypass the control bits and always configure the flag channels as outputs.

Sixteen interrupt lines are provided to allow externally connected devices to generate VMEbus interrupts on any level. External interrupts can be individually enabled or disabled using two byte wide Interrupt Mask Registers. Jumpers on the board are used to configure the interrupt circuits to either detect and latch interrupts on the rising or falling edge of the interrupt input signal. All of the interrupt input signals are pulled up with 10 K Ohm resistors to keep unused interrupt logic in the high state.

The channels are divided in four blocks of 40 channels. Each block of I/O lines is terminated on a 50 position shrouded header at the cards front panel. The channels in each block consist of four byte wide bi-directional data ports; four flag I/O lines and four interrupt input lines.

VME systems with A16, A24, or A32 addressing, and data bus widths of 8, 16 and 32 bits are supported. The data ports only support thirty-two bit transfers. The other registers on the card use byte or word transfers. Pluggable jumpers are used to configure the width of the address bus, and the instruction determines the width of the data transfer. A board identifier PROM, Control and Status register and interrupt control registers are also provided.

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Card Features: PAS 9796/DIO

- 160 TTL level I/O signals arranged as, 128 general purpose I/O, 16 flag I/O, 16 interrupts
- General purpose I/O arranged as 16 byte wide bi-directional data ports
- Flag I/O arranged as 2 byte wide bi-directional data ports
- Flag I/O jumper configurable as output only for interrupt acknowledge applications
- Interrupt latch inputs arranged as 2 byte wide input registers
- Interrupt circuit detects rising or falling edge of interrupt input, and latches on the edge
- Interrupt edge detection is jumper selectable per bit for rising or falling edge
- Interrupts are maskable on a per bit basis
- All interrupt input lines are pulled up with 10 K Ohms, to prevent false triggering
- Input / Output lines are terminated on 2, dual 50 position shrouded headers at the front panel
- All output signal lines including flags have high current, 64 mA, sink current capability
- Board identifier PROM; ID code is VMEID PAS9796DIO *. (* Is revision level)
- SYSFAIL LED and Pass LED at the front panel
- VME SYSFAIL assert on power up, jumper selectable
- VME access: D32, D16, D8; A32, A24, A16 Slave
- VME interrupt; switch selectable level 1 through 7
- VME 6U form factor; 233 mm x 160 mm card size.

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II. SPECIFICATIONS

Electrical Specifications

Number of I/O Channels	128
Number of Flag I/O Channels	16
Number of Interrupt Input Lines	16

Output Characteristics
I/O and Flag I/O Channels

Low Level Output Current	64 mA
High Level Output Current	-15 mA
Low Level Output Voltage @ IOL = 48 mAmps	0.35 V (typ.), 0.5 V (max.)
High Level Output Voltage @ IOH = -3 mA	2.4 V (min.), 3.2 V (typ.)
High Level Output Voltage @ IOH = -15 mA	2.0 V (min.)
Output Polarity	High True

Input Characteristics
I/O, Flag and Interrupt Inputs

High Level Input Voltage	2.0 V (min.)
Low Level Input Voltage	0.8 V (max.)
High Level Input Current @ V In = 2.7 V	20 uA (max.)
Low Level Input Current @ V In = 0.4 V	-0.7 mA (max.)

Note: All inputs are pulled up to + 5 Volts with 10 K Ohms. The low level input current includes -0.5 mA of current that flows through the resistor.

Card Power Requirements	5 Volts @ 1 Amp (typ)
VMEbus Compliance	Fully compatible with VMEbus standard
Address Range	A32, A24, and A16 jumper selectable
Address Block Size	2 K consecutive byte locations
Data Width	D32, D16, D8
Interrupts	IRQ1 through IRQ7 Switch selectable

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Environmental Specifications

Operating Temperature Range	0 to 60 degrees Celsius with forced air cooling.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	16 oz. (typ) TBD
Connectors	2 ea. 96 pos. DIN (VME bus connectors) 2 ea. Dual 50 pos. shrouded headers, (Input / Output data connectors)

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Jumpers, Switches and Indicators

The 9796/DIO card contains 38 jumper plugs, two nine-position DIPswitches and four LED indicators. Sixteen of the jumpers are used to set the board's VME base address, and are defined in Table 2 on page 10. When a jumper is installed, the corresponding address bit must be low to select the card's address, and when a jumper is removed the corresponding address bit must be high. The card is shipped configured for address F0000000, so that 12 of the possible 16 address jumpers are installed.

Jumper J3 is used to configure to board to respond only to Supervisor access or to respond to both Non - Privileged and Supervisor accesses. When J3 is installed, the board only responds to Supervisor accesses. When J3 is removed, the board responds to both Non - Privileged and Supervisor accesses.

Jumpers J25 and J26 are used to select the boards operating environment, either A16, A24 or A32, and the installation of these jumpers is defined in table 1. J3 is used in combination with J25 and J26 to determine which address modifiers to board responds to. The address modifiers that the board responds to are defined below, as a function of J3, J25 and J26.

TABLE 1

Address Modifiers

J26	J25	J3	Address Modifiers	Address Space
IN	IN	IN	0D	Extended I/O
IN	IN	OUT	09, 0D	Extended I/O
IN	OUT	IN	2D	Short I/O
IN	OUT	OUT	29,2D	Short I/O
OUT	IN	IN	3D	Standard I/O
OUT	IN	OUT	39, 3D	Standard I/O
OUT	OUT	IN	2D	Short I/O
OUT	OUT	OUT	29, 2D	Short I/O

Jumper J28 allows the SYSFAIL line to be driven with bit 0 of the control register when it is installed.

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TABLE 2

PLUGGABLE JUMPER DEFINITIONS

Jumper #	Function
J3 IN	Supervisor Access
J3 OUT	Supervisor an Non - Privileged
J9	A16
J10	A17
J11	A18
J12	A19
J13	A20
J14	A21
J15	A22
J16	A23
J17	A24
J18	A25
J19	A26
J20	A27
J21	A28
J22	A29
J23	A30
J24	A31
J25 IN, J26 IN	A32 Addressing
J25 IN, J26 OUT	A24 Addressing
J25 OUT, J26 X	A16 Addressing
J28 IN	SYSFAIL controlled by control register

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Jumper plugs JP1 through JP16 are used to define which edge on the interrupt input lines will cause an interrupt to latch. JP1 is used to configure interrupt line 0 on port A, (PAI0) and JP16 is used to configure interrupt line 3 on port D, (PDI3). The relationship between the jumper plugs and the interrupt lines is shown in table 2. When the jumpers are installed in the left position, the interrupt will latch on a low to high transition of the interrupt input signal. When the jumpers are installed in the right position, the interrupt will latch on the high to low transition of the interrupt input signal.

Jumper plugs JP17 and JP18 are used to configure the flag output ports, for either output only operation or for bi-directional operation. When they are installed from position 1 to 2, the corresponding port is configured for bi-directional operation, and the control register specifies the direction. When they are installed from position 2 to 3, the corresponding port is configured for output operation. JP 17 controls flag ports A and B. JP18 controls flag ports C and D.

TABLE 3

Jumper #	Function
JP1	PAI0
JP2	PAI1
JP3	PAI2
JP4	PAI3
JP5	PBI0
JP6	PBI1
JP7	PBI2
JP8	PBI3
JP9	PCI0
JP10	PCI1
JP11	PCI2
JP12	PCI3
JP13	PDI0
JP14	PDI1
JP15	PDI2
JP16	PDI3
JP17	Flag Ports A, B
JP18	Flag Ports C, D

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Interrupt Level and Address Selection Switches (SW-1/2 and SW-3/4)

Two nine position DIP switches are installed to select the interrupt levels and base addresses for each half of the card. The silk screen on the card labels the locations on the card where the switches are installed as, SW1, SW2 and SW3, SW4. A single nine-position switch is installed at each location. The first three positions of each switch select which VME interrupt level that half of the card will use. These positions are labeled 1,2 and 3 on the switch. The remaining 6 positions are labeled 4 through 9 on the switch, and they are used to select the cards base address. The switch labeled SW1, SW2 is used to select the base address of the A and B ports on the card. The connectors for these ports are located directly above the PCB. The switch labeled SW3; SW4 is used to select the base address of the C and D ports. The connectors for these ports are located directly above the connectors for the A and B ports.

The relationship between the interrupt level and switch setting is shown below.

TABLE 4

VMEbus Interrupt Level

Position 1	Position 2	Position 3	VMEbus Interrupt Level
Open	Open	Open	7
Open	Open	Closed	6
Open	Closed	Open	5
Open	Closed	Closed	4
Closed	Open	Open	3
Closed	Open	Closed	2
Closed	Closed	Open	1
Closed	Closed	Closed	None

The relationship between the base address bits and the switch setting is shown below.

TABLE 5

Address Bits

Switch Position	Address Bit
4	10
5	11
6	12
7	13
8	14
9	15

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LED’s

Four LED’s are provided at the front panel to indicate the board's status. Two LED’s are provided for each half of the card and are controlled by the CSR for that half of the card.

The upper two red LED’s are the Fail LED’s, and power up on. These LED’s are controlled with bit 0 of the control registers, and can be turned off by writing a one to that bit. The SYSFAIL line will also be driven when either Fail LED is on, if J28 is installed.

The lower two green LED’s are the Pass LED’s, and power up off. These LED’s are controlled by bit 1 of the control registers, and can be turned on by writing a one to that bit. This LED can be used to indicate the board has passed some initial power up tests.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. P1 is the upper connector and connects to the first 16 data lines, 24 address lines and the control signals. P2 is the lower connector and connects to an additional 16 data lines and 8 address lines to complete the A32, D32 VMEbus interface.

Two dual 50 position shrouded headers are installed through the board's front panel to provide access to the I/O channels. The top connector is P3, and it terminates ports C and D. The lower connector is P4, and it terminates ports A and B. The pin out of these connectors is defined on the following page.

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TABLE 6

P4 Connector Pin Definitions

P4A (On the PCB)			
GND	50	49	GND
GND	48	47	GND
PAF3	46	45	PAI3
PA3-7	44	43	PA3-6
PA3-5	42	41	PA3-4
PA3-3	40	39	PA3-2
PA3-1	38	37	PA3-0
GND	36	35	GND
PAF2	34	33	PAI2
PA2-7	32	31	PA2-6
PA2-5	30	29	PA2-4
PA2-3	28	27	PA2-2
PA2-1	26	25	PA2-0
GND	24	23	GND
PAF1	22	21	PAI1
PA1-7	20	19	PA1-6
PA1-5	18	17	PA1-4
PA1-3	16	15	PA1-2
PA1-1	14	13	PA1-0
GND	12	11	GND
PAF0	10	9	PAI0
PA0-7	8	7	PA0-6
PA0-5	6	5	PA0-4
PA0-3	4	3	PA0-2
PA0-1	2	1	PA0-0

P4B (Above P4A)			
GND	50	49	GND
GND	48	47	GND
PCF3	46	45	PCI3
PC3-7	44	43	PC3-6
PC3-5	42	41	PC3-4
PC3-3	40	39	PC3-2
PC3-1	38	37	PC3-0
GND	36	35	GND
PCF2	34	33	PCI2
PC2-7	32	31	PC2-6
PC2-5	30	29	PC2-4
PC2-3	28	27	PC2-2
PC2-1	26	25	PC2-0
GND	24	23	GND
PCF1	22	21	PCI1
PC1-7	20	19	PC1-6
PC1-5	18	17	PC1-4
PC1-3	16	15	PC1-2
PC1-1	14	13	PC1-0
GND	12	11	GND
PCF0	10	9	PCI0
PC0-7	8	7	PC0-6
PC0-5	6	5	PC0-4
PC0-3	4	3	PC0-2
PC0-1	2	1	PC0-0

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TABLE 7

P3 Connector Pin Definitions

P3A (On the PCB)			
GND	50	49	GND
GND	48	47	GND
PBF3	46	45	PBI3
PB3-7	44	43	PB3-6
PB3-5	42	41	PB3-4
PB3-3	40	39	PB3-2
PB3-1	38	37	PB3-0
GND	36	35	GND
PBF2	34	33	PBI2
PB2-7	32	31	PB2-6
PB2-5	30	29	PB2-4
PB2-3	28	27	PB2-2
PB2-1	26	25	PB2-0
GND	24	23	GND
PBF1	22	21	PBI1
PB1-7	20	19	PB1-6
PB1-5	18	17	PB1-4
PB1-3	16	15	PB1-2
PB1-1	14	13	PB1-0
GND	12	11	GND
PBF0	10	9	PBI0
PB0-7	8	7	PB0-6
PB0-5	6	5	PB0-4
PB0-3	4	3	PB0-2
PB0-1	2	1	PB0-0

P3B (Above P3A)			
GND	50	49	GND
GND	48	47	GND
PDF3	46	45	PDI3
PD3-7	44	43	PD3-6
PD3-5	42	41	PD3-4
PD3-3	40	39	PD3-2
PD3-1	38	37	PD3-0
GND	36	35	GND
PDF2	34	33	PDI2
PD2-7	32	31	PD2-6
PD2-5	30	29	PD2-4
PD2-3	28	27	PD2-2
PD2-1	26	25	PD2-0
GND	24	23	GND
PDF1	22	21	PDI1
PD1-7	20	19	PD1-6
PD1-5	18	17	PD1-4
PD1-3	16	15	PD1-2
PD1-1	14	13	PD1-0
GND	12	11	GND
PDF0	10	9	PDI0
PD0-7	8	7	PD0-6
PD0-5	6	5	PD0-4
PD0-3	4	3	PD0-2
PD0-1	2	1	PD0-0

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III. PROGRAMMING INFORMATION

The 9796/DIO card responds to byte, word and longword transfers to the data port registers. Word and byte transfers to the control registers and the board identifier PROM are also supported. An example of the card's memory map is shown below, and indicates that this card appears as two copies of a card that occupies 1 Kbyte of VME memory, for a total of 2 Kbytes. This memory does not have to be in contiguous address space and two sets of address switches are provided for addressing each half of the card. The same ID PROM is selected for both the high and low 1 Kbyte block. All of the other registers decode unique addresses.

TABLE 8

PAS 9796/DIO MEMORY MAP

BASE A+000	RESERVED	V (56)	001
002	RESERVED	M (4D)	003
004	RESERVED	E (45)	005
006	RESERVED	I (49)	007
008	RESERVED	D (44)	009
00A	RESERVED	P (50)	00B
00C	RESERVED	A (41)	00D
00E	RESERVED	S (53)	00F
000	RESERVED	2 (32)	011
012	RESERVED	7 (37)	013
014	RESERVED	9 (39)	015
016	RESERVED	6 (36)	017
018	RESERVED	D (44)	019
01A	RESERVED	I (49)	01B
01C	RESERVED	O (4F)	01D
01E	RESERVED	B (42)	01F
020	RESERVED	RESERVED	021
07E	RESERVED	RESERVED	07F
080	INTERRUPT LATCH	CONTROL & STATUS	081
082	PEND. INTERRUPT	INTERRUPT MASK	083
084	CLEAR INTERRUPT	INTERRUPT VECTOR	085
086	FLAG I/O PORT	OUTPUT ENABLE	087
088	DATA PORT A0	DATA PORT A1	089
08A	DATA PORT A2	DATA PORT A3	08B
08C	DATA PORT B0	DATA PORT B1	08D
08E	DATA PORT B2	DATA PORT B3	08F
090	RESERVED	RESERVED	091
3FE	RESERVED	RESERVED	3FF
BASE C+000	RESERVED	ID PROM	001
01E	RESERVED	IDPROM	01F

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TABLE 8 CONT.

PAS 9796/DIO MEMORY MAP

020	RESERVED	RESERVED	021
07E	RESERVED	RESERVED	07F
080	INTERRUPT LATCH	CONTROL & STATUS	081
082	PEND. INTERRUPTS	INTERRUPT MASK	083
084	CLEAR INTERRUPTS	INTERRUPT VECTOR	085
086	FLAG I/O PORT	OUTPUT ENABLE	087
088	DATA PORT C0	DATA PORT C1	089
08A	DATA PORT C2	DATA PORT C3	08B
08C	DATA PORT D0	DATA PORT D1	08D
08E	DATA PORT D2	DATA PORT D3	08F
090	RESERVED	RESERVED	091
3FE	RESERVED	RESERVED	3FF

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Board Identifier PROM (Base Address A + 001H to 01FH) Read Only Second Copy (Base Address C + 001H to 41FH)

The Board Identifier PROM is located starting at the board's base plus 1, and continues to the base address plus 1F. A second range of addresses from 401 to 41F is decoded to read the ID PROM. Both address ranges decode to select the same PROM.

Byte and word reads to the Identifier PROM are supported. Only the least significant byte of a word read will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Interrupt Latch Registers (Base Address A + 080H) Read Only Second Address (Base Address C + 080H)

The Interrupt Latch Registers are used to determine which device has generated an interrupt. Each interrupt input provides an edge detection circuit and interrupt latch. These registers display the status of the latched interrupts, and not the current state of the interrupt input lines. The format of these registers is shown below.

TABLE 9

Interrupt Latch Register

7	6	5	4	3	2	1	0
Intrpt In 7	Intrpt In 6	Intrpt In 5	Intrpt In 4	Intrpt In 3	Intrpt In 2	Intrpt In 1	Intrpt In 0

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Control & Status Register (Base Address A + 081H) Read / Write
Second Copy (Base Address C + 081H)

The Control & Status Register, (CSR), provides two bits that are used to set the states of the front panel LED's and SYSFAIL line, an interrupt pending bit, an interrupt enable bit, a software reset bit, and three read / write bits. Two copies of the CSR are provided, and they are addressed at offset 081 from the base addresses. The format of these registers is shown below.

TABLE 10

Control and Status Register

7	6	5	4	3	2	1	0
User Flag	User Flag	En Flag	Soft Rst	Int Enbl	Int Pend	Pass LED	Fail LED

Bit 0 of the CSR steers the FAIL LED at the front panel. The SYSFAIL line on the backplane will also be asserted if J28 is installed, and bit 0 is reset in either CSR. When the card is reset the FAIL LEDs will come on. Writing a one to bit 0 can turn off the LEDs and the SYSFAIL line. Reading bit 0 returns the state that was last written.

Bit 1 of the CSR controls the PASS LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 can turn on the LED. Reading bit 1 returns the state that was last written.

A pending interrupt is indicated when bit 2 of the CSR is a logic 1. In order for an interrupt to be pending at least one of the interrupt latches must be set and that interrupt must be enabled. More detailed status on which interrupt is pending, can be determined by reading the pending interrupt registers. Bit 2 can set even when the interrupt enable bit in the CSR is disabled. This bit is read only.

The card's interrupt logic is enabled by writing a logic 1 to bit 3 of the CSR. With the interrupts enabled, any pending interrupt will cause the interrupt request lines to be driven onto the VMEbus. Writing a logic zero to bit 3 will disable the main interrupt logic. In response to power up or software reset, the interrupt logic will be disabled. Reading bit 3 returns the value that was last written.

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The software-reset function is controlled by bit 4 of the CSR. When bit 4 is set to a logic 1, the card will be in the software reset state. In order to perform normal operations with the card, bit 4 must be reset to a logic 0. When soft ware reset is performed, the registers on the card will reset to the following states;
The Data Ports will all be configured as inputs,
The Data Output Registers will be cleared to 00H,
The Flag I/O Ports will all be configured as inputs,
The Flag Output Registers will be cleared to 00H,
The Interrupt Mask registers will be cleared to 00H, disabling all interrupts.
Reading bit 4 returns the value that was last written.

Bit 5 enables the outputs on Flag I/O Ports. Writing a logic 0 to this bit configures the port as an input by disabling the Flag Output Registers. Writing a logic 1 configures the port for output. Reading this bit returns the value that was last written.

The function of these bits can be bypassed by installing jumper plugs JP17and JP18 to position 2 to 3. When the jumpers are installed, the Flag Ports will always be configured as outputs.

Bits 6 and 7 of the CSR will return the value that was last written. These bits have no other function.

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Pending Interrupt Registers (Base Address A + 082H) Read Only
Second Address (Base Address C + 082H)

The Pending Interrupts Registers display the state of any pending interrupts. In order for an interrupt pending bit to be set, the associated interrupt latch must be set, and the interrupt must be enabled with the Interrupt Mask Register.

TABLE 11

Interrupt Pending Register

7	6	5	4	3	2	1	0
Intrpt 7 Pnd	Intrpt 6 Pnd	Intrpt 5 Pnd	Intrpt 4 Pnd	Intrpt 3 Pnd	Intrpt 2 Pnd	Intrpt 1 Pnd	Intrpt 0 Pnd

A logic 1 indicates a pending interrupt.
A logic 0 indicates no interrupt.

Interrupt Mask Registers (Base Address A + 083H) Read / Write
Second Address (Base Address C + 083H)

The Interrupt Mask Registers are used to enable and disable selected interrupt circuits from generating interrupt requests. Writing a 1 to a bit in these registers will enable the associated circuit to generate an interrupt request. Writing a 0 will disable the associated circuit from generating an interrupt request. These registers reset to all zeros at power up or in response to a software reset, which disables all of the interrupt circuits. The registers can be read to determine which interrupts are enabled. The format of these registers is shown below.

TABLE 12

Interrupt Mask Register

7	6	5	4	3	2	1	0
Intrpt Msk 7	Intrpt Msk 6	Intrpt Msk 5	Intrpt Msk 4	Intrpt Msk 3	Intrpt Msk 2	Intrpt Msk 1	Intrpt Msk 0

Writing a logic 1 will enable the selected interrupt.
Writing a logic 0 will disable the selected interrupt.

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Clear Interrupt Ports (Base Address A + 084H) Write Only
Second Address (Base Address C + 084H)

The Clear Interrupt Ports are used to clear individual bits in the Interrupt Latches. Writing a 1 will clear an interrupt bit that is set, and a 0 will have no effect on the interrupt bits. These registers are used in interrupt service routines to clear the pending interrupt bits, and must also be written at power up to clear all of the bits in the Interrupt Latches. Reading these port addresses will return indeterminate data. The format of the Clear Interrupt Ports is shown below.

TABLE 13

Clear Interrupt Ports

7	6	5	4	3	2	1	0
Intrpt Clr 7	Intrpt Clr 6	Intrpt Clr 5	Intrpt Clr 4	Intrpt Clr 3	Intrpt Clr 2	Intrpt Clr 1	Intrpt Clr 0

Writing a logic 1 will clear an interrupt.
Writing a logic 0 will have no effect.

Interrupt Vector Registers (Base Address A + 085H) Read / Write
Second Address (Base Address C + 085H)

The Interrupt Vector Registers are read write registers that are used to determine the value of the Interrupt Vector that will be driven onto the VME bus during interrupt acknowledge cycles. Reading these registers will return the value that was last written. The interrupt vector registers powers up to indeterminate states, and must be written with valid vectors prior to enabling the card's interrupts. The format of these registers is shown below.

TABLE 14

Interrupt Vector Register

7	6	5	4	3	2	1	0
Intrpt Vec 7	Intrpt Vec 6	Intrpt Vec 5	Intrpt Vec 4	Intrpt Vec 3	Intrpt Vec 2	Intrpt Vec 1	Intrpt Vec 0

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Flag Input /Output Ports (Base Address A + 086H) Read / Write
Second Address (Base Address C + 086H)

The Flag Input / Output Ports are used to control the states of the flag output bits. Writing a logic one to a bit causes the corresponding flag output to go high, and a zero causes it to go low. Reading these registers returns the last value that was written to them. The format of the Flag Input / Output Ports is shown below.

TABLE 15

Flag Input / Output Port

7	6	5	4	3	2	1	0
Flag I/O 7 PBF3	Flag I/O 6 PBF2	Flag I/O 5 PBF1	Flag I/O 4 PBF0	Flag I/O 3 PAF3	Flag I/O 2 PAF2	Flag I/O 1 PAF1	Flag I/O 0 PAF0

A logic 1 corresponds to a high state on the I/O Flag line.
A logic 0 corresponds to a low state on the I/O Flag line.

Output Enable Registers (Base Address A + 087H) Read / Write
Second Address (Base Address C + 087H)

The Output Enable Registers are used to configure the byte wide I/O ports for either input or output operation. Writing a one to an output enable bit configures that port as an output, and a zero configures it as an input. Reading these registers returns the last value that was written. During power up or in response to a software reset, these registers are cleared to all zeros, which specify all of the ports as inputs. The format of the Output Enable Registers is shown below.

TABLE 16

Output Enable Register

7	6	5	4	3	2	1	0
Outpt Enbl 7 ENB3	Outpt Enbl 6 ENB2	Outpt Enbl 5 ENB1	Outpt Enbl 4 ENB0	Outpt Enbl 3 ENA3	Outpt Enbl 2 ENA2	Outpt Enbl 1 ENA1	Outpt Enbl 0 ENA0

A logic 1 configures a port for output.
A logic 0 configures a port for input.

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Input / Output Data Ports (Base Add A + 088H to 08FH) Read / Write
Second Copies (Base Add C + 088H to 08FH)

The Input / Output Data Ports are byte wide bi-directional registers that are connected to the I/O data lines. These registers can be configured for either input or output operation using the Output Enable Registers. Following a reset, all of the Data Ports are configured as Inputs. Reading the ports will return a one for each bit that has a corresponding I/O line in the high state, and a zero for inputs that are in the low state. When the Data Port is configured as an output, bits that are written with ones will cause the corresponding output lines to be driven to the high state, and zeros will produce the low state. The Data Port can be read back when it is configured as an output, and it will return the value that was written last. The format of the I / O Data Ports is shown below.

TABLE 17

Input / Output Data Port

7	6	5	4	3	2	1	0
Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0

A logic 1 corresponds to a high state on the I/O line.
A logic 0 corresponds to a low state on the I/O line.

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