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OPERATING MANUAL

MODEL 1420

DC –20 MHz Direct Digital Frequency
Synthesizer VMEbus Board

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Pentek Model 1420 Operating Manual – Revision History

Date	Rev	Applicable Serial #'s	Comments
09/30/91	A	9146018 – 9208009	Initial product release
12/17/91	B	9208010 – Forward	Artwork changes
01/26/93	C	9208010 – Forward	Add connector pinout, minor text corrections
02/24/93	D	9208010 – Forward	Minor text corrections, fixed error in code sample
02/08/95	E	9208010 – Forward	Reformatted and expanded. Add Sample Programs from Pentek SW disk. Moved SW examples from Section 5 to Appendix A, Qualcomm data sheet info from Section 4 to Appendix B, Specifications from Section 2 to end of Chapter 1.
08/26/96	F	9208010 – Forward	Pinout of A24_base Address jumpers (JB1 & JB2) corrected in Table 2–3. Indicate Pinout in Figure 2–3. Correct Redundant Figure numbering. Add Figures & Tables to Table of Contents.
9/7/99	G	9208010 – Forward	Updates to Table 2.2 to clarify DDS jumper settings. Add note to Sec. 2.4.6.4 stating that the DDS modules cannot be programmed if no clock signal is applied. Sec. 3.4.1.3 – mention that setting all 3 noise reduction bits to '1' disables NR (this is how example code sets them). Remove uncalled function **`setpirb`** from Sec. A.6.

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Chapter 1: Introduction

1.1 Introduction

The Pentek Model 1420 Direct Digital Synthesizer is a complete instrument packaged on a VMEbus card containing either one or two detachable synthesizer modules. Each module contains two independently programmable synthesizers, providing a total of four output channels for the card. The output frequency range of each synthesizer is DC to 20 MHz.

Each of the four outputs can be configured either as a sine wave or TTL−compatible pulse signal available on a BNC connector mounted on the VME front panel. A 10 MHz crystal oscillator provides the frequency reference from which all accuracy and stability specifications are determined. An external 10 MHz reference may be provided to lock the Model 1420 to a system reference.

The Model 1420 may be operated in fixed frequency or Frequency Shift Keying modes (FSK). Several phase modulation modes are also available such as Binary Phase Shift Keying (BPSK) and Multiple Shift Keying (MSK).

The ability to adjust phase between multiple TTL signals is a feature that makes the synthesizer useful in many digital test systems.

1.2 General Description

The Model 1420 consists of a VMEbus card containing either one or two 2−channel DDS (direct digital synthesizer) modules.

1.2.1 VMEbus Card

The VMEbus card provides a physical and electrical interface between the DDS Modules and the VMEbus environment. Each DDS module plugs into a 50 pin socket, permitting modularity and easy servicing.

Circuitry on the board includes: the address decoder; the address modifier PROM; the master clock; control registers with readback capability; two−input digital multiplexers for selecting either the VMEbus or the front panel connectors as the control input source; a 10 MHz crystal oscillator; and a 10 MHz to 50 MHz frequency multiplier, whose output is used as the refer−ence clock for each synthesizer module. The 50 MHz oscillators inside the DDS Modules may be used in lieu of the 10 MHz to 50 MHz multiplier out−put. Figure 1−1, on the next page, shows a block diagram of the Model 1420 VMEbus card.

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1.2 General Description (continued)

1.2.1 VMEbus Card (continued)

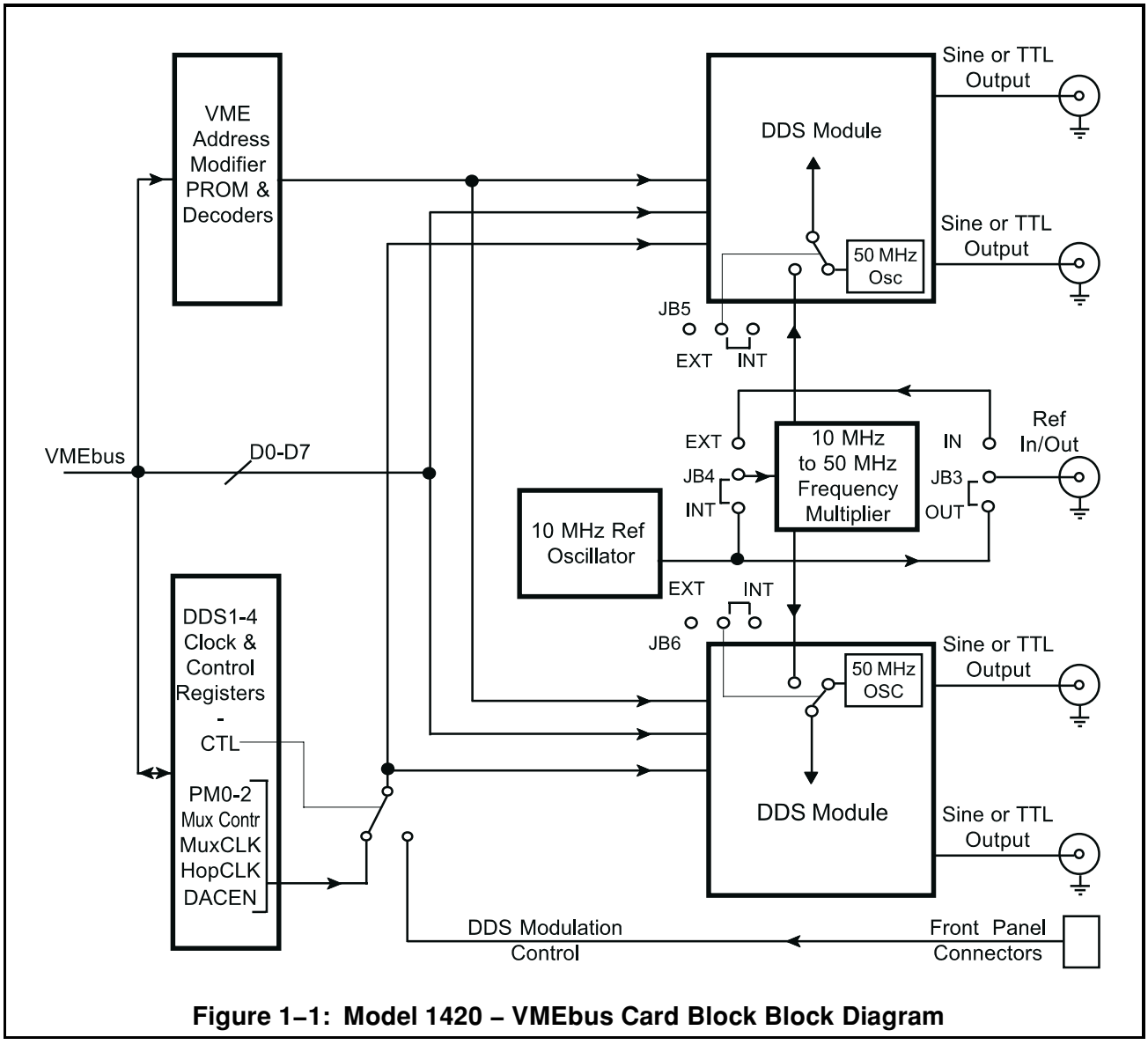


Figure 1–1: Model 1420 – VMEbus Card Block Block Diagram

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1.2 General Description (continued)

1.2.2 DDS Module

Each DDS module uses a monolithic digital integrated circuit, manufactured by Qualcomm, Inc. The circuit contains registers for frequency settings and control modes. It also contains two 32–bit phase accumulators operating at a 50 MHz clock rate. The frequency resolution is, therefore, 2^{-32} x ($50x10^6$) Hz. This equals approximately 0.012 Hz. The output of each accumulator is connected to a sine look–up function which provides a digitized output sine–wave. The two digitized sinewave outputs of the Qualcomm circuit are converted to sampled analog signals by two D/A converters. Two independent low–pass filters remove the sampling components, leaving the fundamental sinewave. Each channel is amplified and connected to the input of an analog comparator. Either the fundamental sinewave or the comparator output is directed to the front panel BNC through a user selectable jumper on the module. A block diagram of the DDS module is shown in Figure 1–2, below.

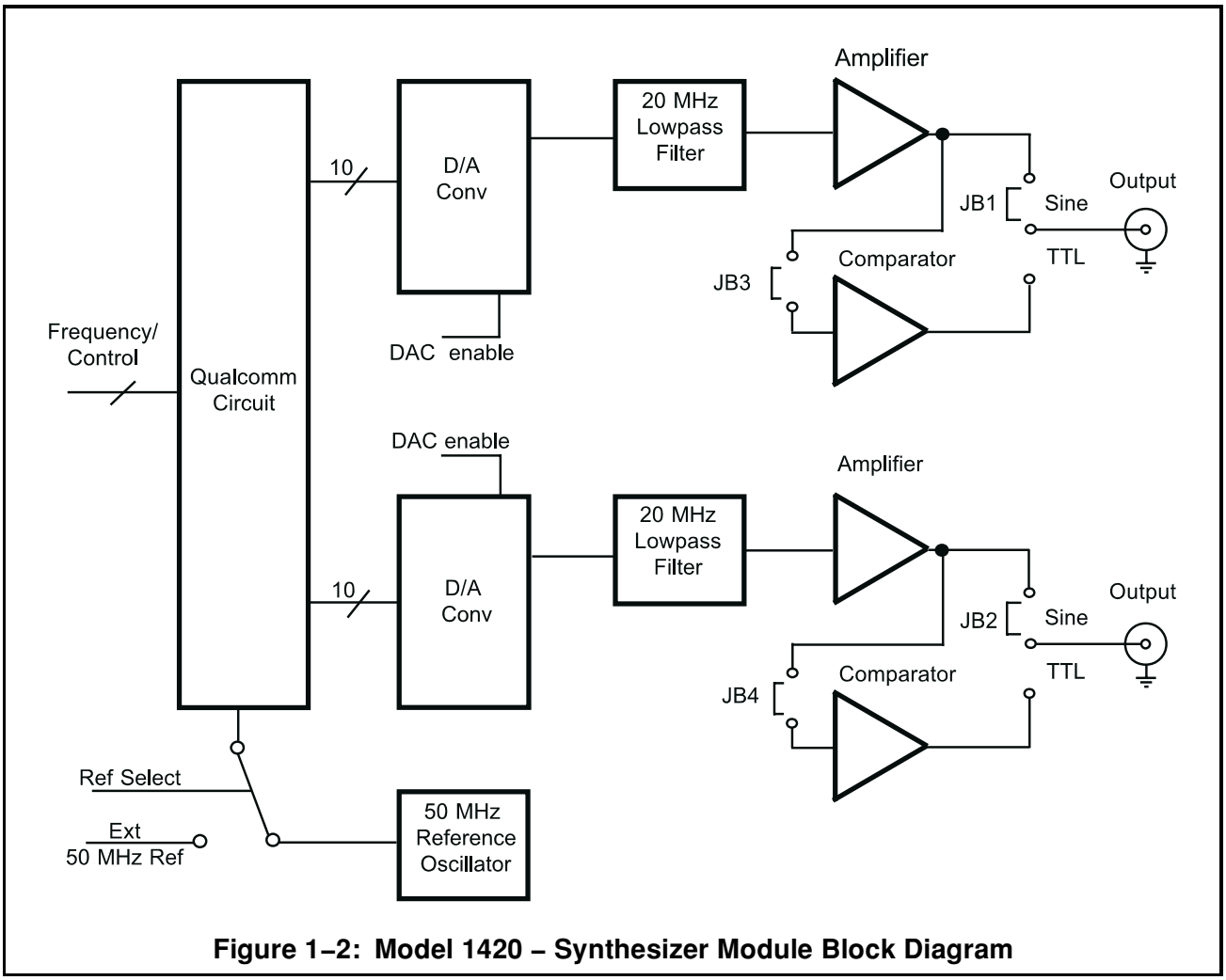


Figure 1–2: Model 1420 – Synthesizer Module Block Diagram

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1.2 General Description (continued)

1.2.3 Qualcomm Circuit Internal Architecture

The Qualcomm circuit contains two independent synthesizer channels. Each channel has two Phase Increment Registers. These double buffered, 32–bit registers are loaded 8 bits at a time with the desired frequency setting. One register is connected to a 32–bit binary phase accumulator through the Frequency Multiplex Switch. The Phase Accumulator output is added to a 3 bit phase modulation code. This permits fast, 45° step, phase modulation. The Phase Modulator output is connected to a sine look–up function that converts the signal to the digitized sine output. Figure 1–3, below, shows a block diagram of the Qualcomm IC. See Appendix B for a detailed description of the Qualcomm integrated circuit.

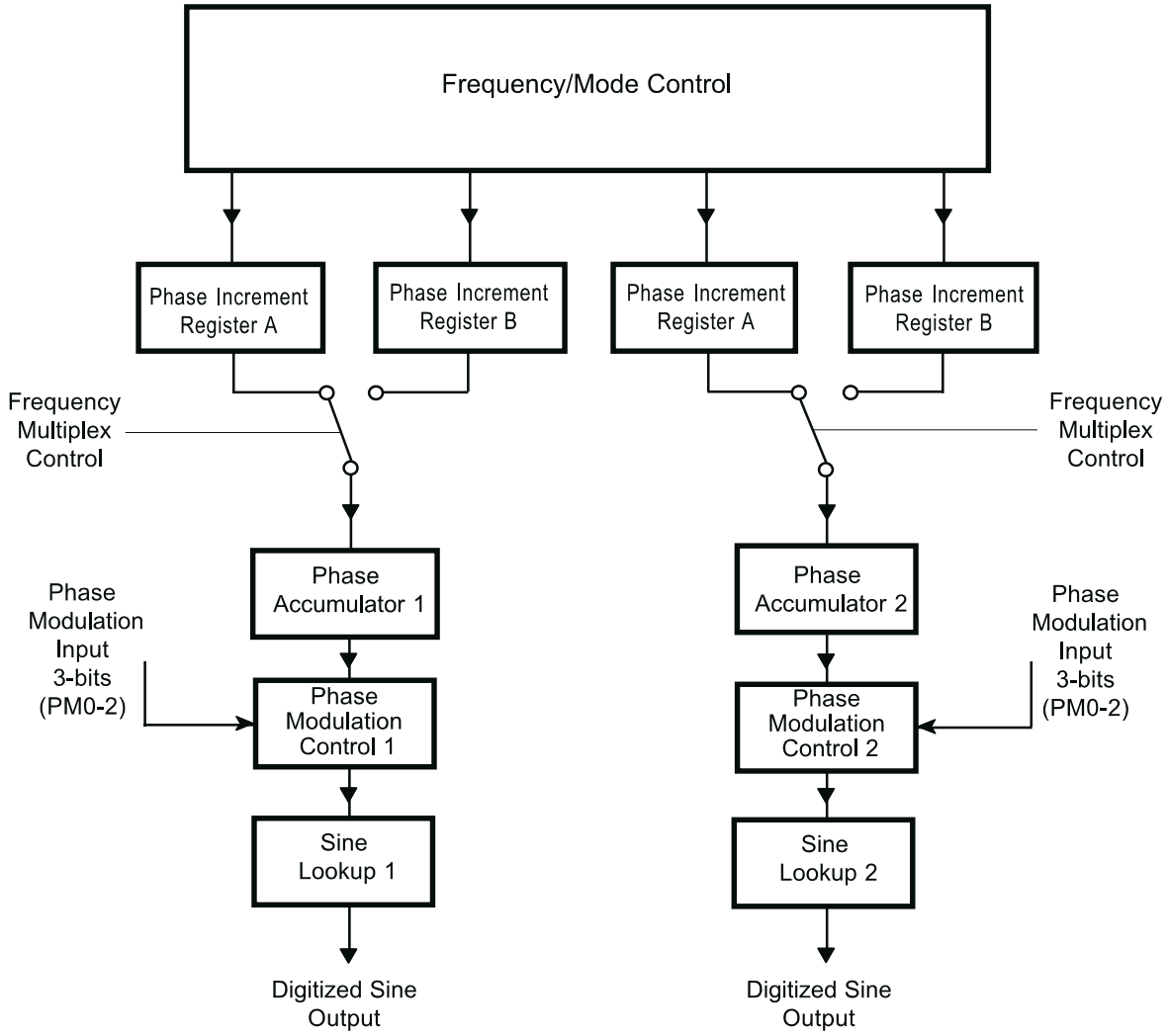


Figure 1–3: Model 1420 – Simplified Qualcomm Circuit Block Diagram

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1.3 Specifications

Number of Channels:
- **Standard:** Four
- **Option 002:** Two

Frequency Range:
- **Standard:** DC to 20 MHz
- **Option 005:** DC to 4 MHz

Frequency Resolution: 32 bits
- **Standard:** Approximately 0.012 Hz
- **Option 005:** Approximately 0.0051 Hz

Frequency Accuracy:
- **Internal reference:** 3 PPM (Opt. 004) or 100 PPM (std)
- **External reference:** Equal to accuracy of 10 MHz TTL input, delivered to front panel BNC connector

Option 004 Reference:
- Accuracy: ± 1 PPM maximum error at 25°C
- Temperature stability: ± 3 PPM from 0°C to 50°C
- Aging (typical, after 30 days): 5 PPM first year, 3 PPM/year thereafter

Sine Output:
- Output level: +10 dBm full scale, into 50 Ω
- Frequency flatness: ±1 dB
- Output impedance: 50 Ω nominal
- Integrated Phase Noise: Less than −55 dBc in a 30 kHz BW
- Harmonic components: Less than −45 dBc
- Spurious components: Less than −55 dBc

TTL Output:
- Selection: Each output is jumper selectable, Sine or TTL

Phase Modulation:
- High Resolution Mode: 0 to 360°, 16−bit resolution, program control only, binary data
- Fast PSK Mode: 0 to 360°, eight 45° steps
- PSK Control: 3 bits, controlled by program or external input lines

Frequency Switching:
- Frequency setting: Two 32−bit registers, program loaded
- Data Type: 32−bit straight binary
- Switching Control: Register selected by program or external line
- Switching Mode: Phase−Continuous, transient−free
- Switching Delay: Less than 1 µsec

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1.3 Specifications (continued)

Front Panel Connectors:

Sine Output:	BNC (female)
Reference Input:	BNC (female)
PSK & FSK Control:	Multi–pin Ribbon (male)

VMEbus Characteristics:

Bus Device Type:	Slave
Data Path Width:	D16
Address Path Width:	A24
Base Address Select:	Jumper Block

Dimensions:

Board Size:	160 mm X 233.35 mm (6.3″ X 9.19″) – 6U
Panel Width:	20.32 mm (0.8“)

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect carefully for possible damage to connectors or components. If any damage is discovered, please contact Pentek immediately, at the phone number shown on this manual's title page. The shipping container and packing materials should be saved in case re–shipment is required.

2.2 Mechanical

The Model 1420 fits into a standard double–height (6U) VMEbus card cage and occupies one slot (20.32 mm or 0.8"), in the card cage. Two DIN 41612 connectors are installed, although P2 is essentially non–functional, except for mechanical integrity.

Each of the two DDS Modules is attached to the VME board by a 50–pin dual–in–line connector. A DDS module may be removed by removing the nut on the front panel BNC connector and pushing the BNC through the front panel. The BNCs are integral parts of the DDS modules.

CAUTION!!

Never remove or reinstall a DDS module from the VME board with power on.

2.3 Inserting the Unit

Align the Model 1420 card edge with the card cage guides and push evenly on both ejector handles until the front panel seats against the upper and lower rails. Secure the unit to the cage by tightening the upper and lower retainer screws in the front panel.

CAUTION!!

Never insert or remove the Model 1420 while power is applied in the card cage.

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2.4 Removing the Unit

Loosen the upper and lower retaining screws; they are captive screws and will remain part of the panel assembly. Gently push both ejector handles apart (away from the center of the panel) until the unit unseats itself from the cage connectors. Then pull outward to remove the unit.

CAUTION!!

Never insert or remove the Model 1420 while power is applied in the card cage.

2.5 Front Panel and Signal Connections

The Front Panel of the Model 1420 is shown in Figure 2–1, at the right. The panel contains BNC connectors for the synthesizer outputs and the Reference Clock Signal, and dual–in–line ribbon cable connectors for the control ports. The signals that are available or may be applied to these connectors are described in the sections below.

2.5.1 Sine Outputs

The Sine outputs are 0.707 V_{RMS} (+10 dBm) with a source impedance of 50 Ω. In order to maintain the specified frequency response and spectral purity, the output must be terminated in 50 Ω.

2.5.2 TTL Outputs

The TTL output buffer is a 74ACT04 device. The output should be terminated in 50 Ω to avoid ringing on leading and trailing edges.

2.5.3 10 MHz Reference Input (Ext Clk In)

The reference input (if used) must be a 10 MHz TTL signal with nominal 50% duty cycle. The termination on the board is four inputs of a 74HCT241. If this input is driven from a cable longer than a few feet, it is recommended that an in–line terminator be placed at the BNC input to avoid ringing.



Figure 2–1: Model 1420 – Front Panel

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2.5 Front Panel and Signal Connections (continued)

2.5.4 Multi–pin Connectors

All inputs are TTL compatible, with a 74ALS–type load. All output signals come from 74ALS devices. Similar precautions as with the reference input should be taken to avoid ringing due to excessively long cables. Two mating connectors and strain reliefs are supplied with every unit.

The recommended connector for this application is:

Flat Cable Connector:	3M #50126–B000
Mating Strain Relief:	3M #3448–50126

Table 2–1: Model 1420 – Front Panel Multi–pin Connector – Signal Assignments

DDS 1 & 2				DDS 3 & 4			
PIN	SIGNAL	I/O	DDS	PIN	SIGNAL	I/O	DDS
1	PMCLK	IN	DDS1	1	PMCLK	IN	DDS3
2	MUXCLK	IN	DDS1	2	MUXCLK	IN	DDS3
3	HOPCLK	IN	DDS1	3	HOPCLK	IN	DDS3
4	PM0	IN	DDS1	4	PM0	IN	DDS3
5	PM2	IN	DDS1	5	PM2	IN	DDS3
6	DACEN	IN	DDS1	6	DACEN	IN	DDS3
7	GND			7	GND		
8	DACEN	IN	DDS2	8	DACEN	IN	DDS4
9	PM2	IN	DDS2	9	PM2	IN	DDS4
10	PM0	IN	DDS2	10	PM0	IN	DDS4
11	HOPCLK	IN	DDS2	11	HOPCLK	IN	DDS4
12	MUXCLK	IN	DDS2	12	MUXCLK	IN	DDS4
13	PMCLK	IN	DDS2	13	PMCLK	IN	DDS4
14	GND			14	GND		
15	GND			15	GND		
16	GND			16	GND		
17	PM1	IN	DDS1	17	PM1	IN	DDS3
18	MUX	IN	DDS1	18	MUX	IN	DDS3
19	CNTRL	OUT	DDS1	19	CNTRL	OUT	DDS3
20	GND			20	GND		
21	CNTRL	OUT	DDS2	21	CNTRL	OUT	DDS4
22	MUX	IN	DDS2	22	MUX	IN	DDS4
23	PM1	IN	DDS2	23	PM1	IN	DDS4
24	GND			24	GND		
25	GND			25	GND		
26	GND			26	GND		

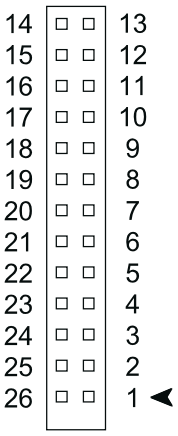


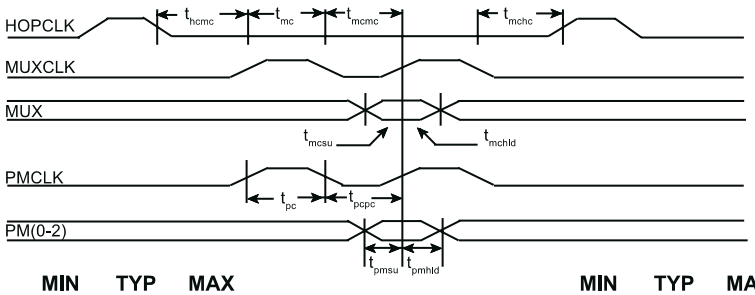
Figure 2–2: Model 1420 – Front Panel Multi-pin Connector Pinout

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2.5 Front Panel and Signal Connections (continued)

2.5.5 Front Panel Multi–Pin Connector Signal Description & Timing

SIGNAL	DESCRIPTION
CNTRL	Data bit that directs modulation information for each DDS channel from front panel connectors (when in the high state) or VMEbus (when in the low state). Data bit is controlled by VMEbus and can be monitored on front panel connectors. All other functions provided by these connectors may also be pro–vided by a bit in a VME–addressable register. See Section 3.4.2 for further details.
DACEN	D/A Converter enable – Logic high to allow data into D/A Converter. When low, data is inhibited and D/A Converter holds last value.
GND	Ground
HOPCLK	Hop clock – Second rank buffer strobe for PIRA, PIRB, and SMC registers. After these registers are loaded, the new value does not become active until HOPCLK goes high.
MUXCLK	Mux clock – used to strobe Multiplexer Control data line.
MUX	Multiplexer Control data bit – selects PIRA or PIRB registers.
PMCLK	Phase modulation clock – used to strobe PM0, PM1, and PM2 phase modulation data bits.
PM0	Phase modulation data bit (1 of 3 bits – LSB).
PM1	Phase modulation data bit (1 of 3 bits – middle bit).
PM2	Phase modulation data bit (1 of 3 bits – MSB).



	MIN	TYP	MAX			MIN	TYP	MAX	
t_{hcmc}	t_{cyc}	-	-	ns	t_{mcsu}	10	15	-	ns
t_{mc}	$3 \cdot t_{cyc}$	-	-	ns	t_{pc}	$3 \cdot t_{cyc}$	-	-	ns
t_{mcmc}	t_{cyc}	-	-	ns	t_{pcpc}	t_{cyc}	-	-	ns
t_{mchc}	$10 \cdot t_{cyc}$	-	-	ns	t_{pmsu}	10	15	-	ns
t_{mchld}	10	15	-	ns	t_{pmhld}	10	15	-	ns

NOTE: In the table above, t_{cyc} is defined as one period of the synthesizer's output frequency.

Figure 2–3: Model 1420 – Control Input Signal Timing

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2.6 Jumper Configuration and Adjustments

Figure 2–4 below, shows the locations of the jumper blocks and adjustment points on the Model 1420. Note that there are jumpers on the DDS Modules, as well as on the VME card, and that the reference designations JB1, JB2, JB3 and JB4 are used three times each (twice in each DDS module, and again on the VMEbus board. Make certain that you know which jumper block is which before changing any settings.

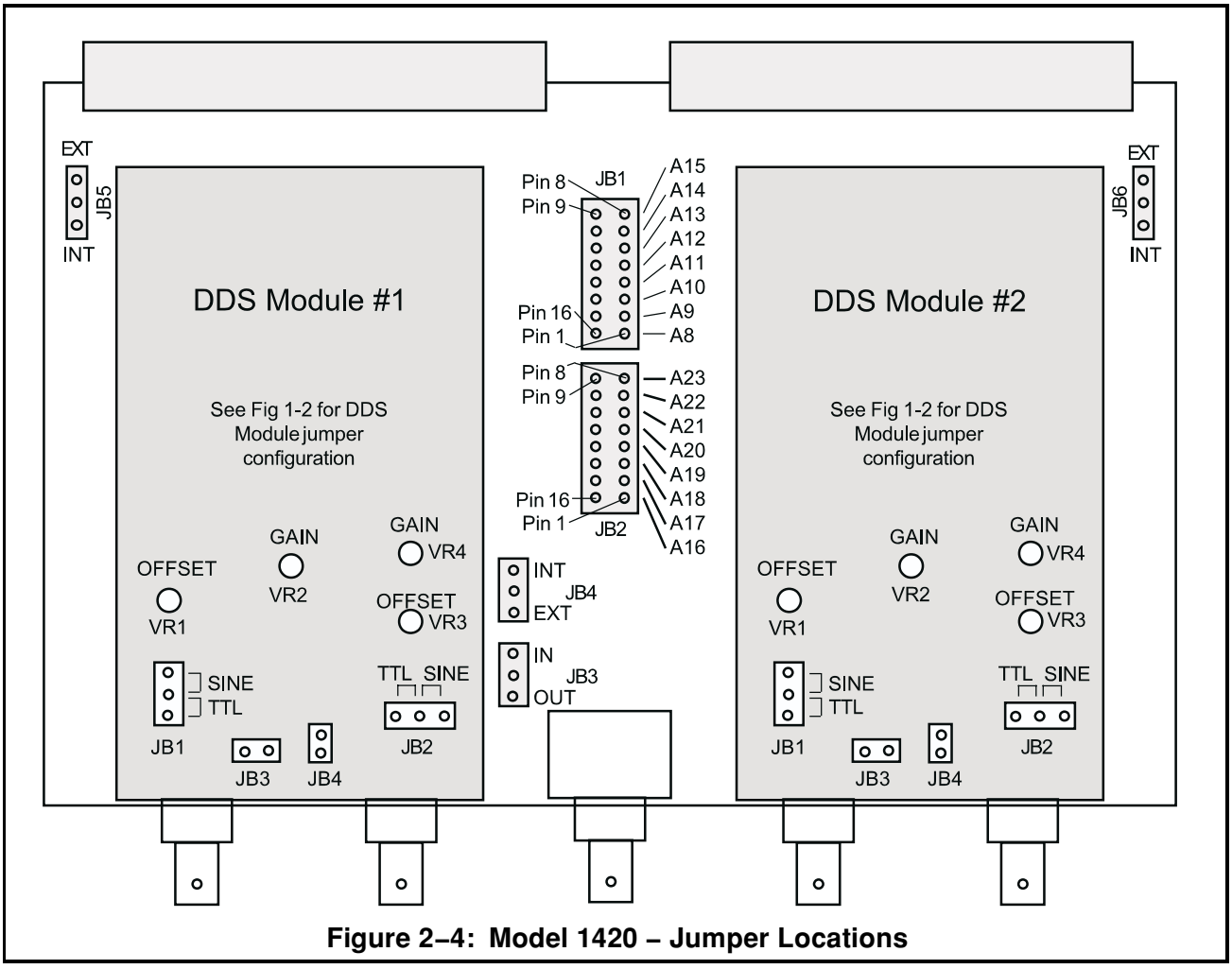


Figure 2–4: Model 1420 – Jumper Locations

2.6.1 DDS Module Jumper Blocks and Adjustments

Both of the DDS Modules in the Model 1420 contain two synthesizer channels. Two configuration jumper blocks are associated with each channel of the DDS Module. One of these determines whether that channel's output will be a Sinusoidal signal or a TTL–compatible logic level signal. The other jumper, installed only when the TTL output is chosen by the first jumper, connects the sine signal to a comparator, whose output becomes the module's TTL output. Provisions are also made for independently adjusting the amplitude and DC offset of each of the sinewave signals. (Figure 1–2, on page 9 of this manual, presents a block diagram of the DDS Module and its jumpers.) The subsec–tions beginning on the next page provide further details.

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2.6 Jumper Configuration and Adjustments (continued)

2.6.1 DDS Module Jumper Blocks and Adjustments (continued)

2.6.1.1 Module Output Select Jumpers – JB1 and JB2 on DDS Modules

The type of output signal delivered by each channel the Model 1420 is determined by the settings of the jumper blocks labeled JB1 and JB2 on the two DDS Modules. Each module can deliver two independent output signals, and each output signal can be configured for a Sinusoidal signal or a TTL–compatible logic signal. The jumper placement to accomplish the selection is indicated on the module housing, as shown in Figure 2–4, on the previous page.

JB1 on DDS Module 1 selects the output signal type for Channel 1, and JB2 on DDS Module 1 selects the output signal type for Channel 2. JB1 on DDS Module 2 selects the output signal type for Channel 3, and JB2 on DDS Module 2 selects the output signal type for Channel 4. The factory default setting of these jumpers is to the TTL position. Note that the TTL output setting requires that the TTL output enable jumpers (JB3 and JB4 on each module – see Section 2.6.1.2, below) also be installed. These should be removed if the Sine output is selected.

2.6.1.2 TTL Output Enable Jumpers – JB3 and JB4 on DDS Modules

The DDS Modules always produce a sinusoidal signal at the programmed frequency. To deliver a TTL–compatible logic signal to the output connector, the sine signal must be connected to the input of a comparator with a TTL output. Jumper blocks JB1 and JB2 (discussed in Section 2.6.1.1, above), when set to the TTL position, connect the comparator's output to the Module's output BNC connector. An installed jumper on jumper blocks JB3 or JB4 connects the sine signal to the comparator's input.

JB3 on DDS Module 1 enables the TTL output for Channel 1, and JB4 on DDS Module 1 enables the TTL output for Channel 2. JB3 on DDS Module 2 enables the TTL output for Channel 3, and JB4 on DDS Module 2 enables the TTL output for Channel 4. All four of these jumpers are installed in the factory default configuration. If a sine output is desired from a given channel, the TTL enable jumper for the channel in question should be removed (in addition to changing the position of the output select jumper, see above). This prevents glitching on the Sine output due to level changes at the comparator's output.

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2.6 Jumper Configuration and Adjustments (continued)

2.6.1 DDS Module Jumper Blocks and Adjustments (continued)

2.6.1.3 Sine Amplitude Adjustment – VR2 and VR4 on DDS Modules

A separate amplitude adjustment pot, labeled GAIN, is provided for each channel of each DDS Module. VR2 on DDS Module 1 is the amplitude adjustment for Channel 1, and VR4 on DDS Module 1 is the amplitude adjustment for Channel 2. VR2 on DDS Module 2 is the amplitude adjustment for Channel 3, and VR4 on DDS Module 2 is the amplitude adjustment for Channel 4.

2.6.1.4 Sine Offset/TTL Symmetry Adjustment – VR1 and VR3 on DDS Modules

A separate offset adjustment pot, labeled OFFSET, is provided for each channel of each DDS Module. VR1 on DDS Module 1 is the offset adjustment for Channel 1, and VR3 on DDS Module 1 is the offset adjustment for Channel 2. VR1 on DDS Module 2 is the offset adjustment for Channel 3, and VR3 on DDS Module 2 is the offset adjustment for Channel 4.

This pot is also used to adjust the symmetry (i. e., duty cycle) of the TTL squarewave signals. Monitor the waveform on an oscilloscope to make the adjustment. The adjustment should be made with the output terminated in a 50 Ω load.

Table 2–2, below, summarizes the functions of all the jumper blocks and adjustments on the Model 1420's DDS Modules.

Table 2–2: Model 1420 – DDS Module Jumper Block and Adjustments

DDS Module	Output Channel	Output Type	JB1	JB2	JB3	JB4	Sine Amplitude	Sine Offset/ TTL Symmetry
1	1	Sine	Sine	Off	X	X	VR2	VR1
1	1	TTL	TTL	On	X	X	N/A	
1	2	Sine	X	X	Sine	Off	VR4	VR3
1	2	TTL	X	X	TTL	On	N/A	
2	3	Sine	Sine	Off	X	X	VR2	VR1
2	3	TTL	TTL	On	X	X	N/A	
2	4	Sine	X	X	Sine	Off	VR4	VR3
2	4	TTL	X	X	TTL	On	N/A	
X – jumper setting doesn't matter								

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2.6 Jumper Configuration and Adjustments (continued)

2.6.2 VMEbus Board Jumper Blocks

Jumper blocks located on the Model 1420's VMEbus board select the device's A24_Base Address, determine whether the EXT CLK BNC connector, at the center of the front panel, is an input or an output, and determine the source of the reference frequency used by the DDS Modules. The subsections beginning on the next page provide further detail.

2.6.2.1 Base Address Jumpers – JB1 and JB2 on VMEbus Board

The Model 1420 occupies 256 bytes of address space, which can be located at any 256–byte boundary in A24 VMEbus address space. To specify the base address of the 256–byte region, two jumper blocks are provided on the VME board, JB1 and JB2. The address bits are designated as shown by the text adjacent to these jumper blocks in Figure 2–4, on page 17. The hexadecimal weight of each bit represented by these jumper block locations is listed in Table 2–3, below. To set the base address, remove a jumper for each address bit equal to logic '1' (i. e., to add that bit's weight to the base address) and install a shorting jumper for a logic '0'.

Table 2–3: Model 1420 – A24 Base Address Jumpers – Jumper Blocks JB1 and JB2

Address Bits and Hexadecimal Weights of Jumper Positions on JB1							
Pins 8 – 9	**Pins 7 – 10**	**Pins 6 – 11**	**Pins 5 – 12**	**Pins 4 – 13**	**Pins 3 – 14**	**Pins 2 – 15**	**Pins 1 – 16**
A15 (0x00 8000)	A14 (0x00 4000)	A13 (0x00 2000)	A12 (0x00 1000)	A11 (0x00 0800)	A10 (0x00 0400)	A9 (0x00 0200)	A8 (0x00 0100)
Address Bits and Hexadecimal Weights of Jumper Positions on JB2							
Pins 8 – 9	**Pins 7 – 10**	**Pins 6 – 11**	**Pins 5 – 12**	**Pins 4 – 13**	**Pins 3 – 14**	**Pins 2 – 15**	**Pins 1 – 16**
A23 (0X80 0000)	A22 (0X40 0000)	A21 (0X20 0000)	A20 (0X10 0000)	A19 (0X08 0000)	A18 (0X04 0000)	A17 (0X02 0000)	A16 (0X01 0000)

2.6.2.2 Front Panel EXT CLK Connector Jumper – JB3 on VMEbus Board

The setting of jumper block JB3 on the Model 1420's VMEbus board determines whether the BNC Connector labeled EXT CLK IN, at the center of the front panel, is used as an input or an output for the reference frequency. The jumper positions are labeled on the board, and are shown in Figure 2–4, on page 17.

When a shorting jumper is placed on the OUT position of JB3 (the factory default setting), the output of the crystal–controlled 10 MHz reference oscillator on the 1420's VME board drives the EXT CLK BNC connector. If the jumper is moved to JB3's IN position, then a signal applied to the EXT CLK connector drives the EXT pin on JB4, where another jumper may be placed to connect that signal to the input of the 1420's Frequency Multiplier circuit. See Figure 1–1, on page 8 of this manual for a block diagram of these connections, and Section 2.6.2.3, on the next page, for further details about JB4.

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2.6 Jumper Configuration and Adjustments (continued)

2.6.2 VMEbus Board Jumper Blocks (continued)

2.6.2.3 Reference Multiplier Input Select Jumper Block – JB4 on VMEbus Board

Jumper block JB4 determines the source of the input signal to the Model 1420's Frequency Multiplier. The output of this circuit is connected to the EXT pins on jumper blocks JB5 and JB6. Here, another jumper may be placed to select the multiplier's output signal as the reference frequency for the DDS Modules.

When the jumper on JB4 is placed at the INT position (the factory default setting), the multiplier's input is driven by the 1420's crystal–controlled 10 MHz reference oscillator. If the jumper is moved to the EXT position, **and** the jumper on JB3 is placed at the IN position, then a signal connected to the Front Panel EXT CLK IN BNC connector provides the input to the multiplier. See Figure 1–1, on page 8 of this manual, for a block diagram showing the connectivity of this jumper. Section 2.6.2.2 provides more details about jumper block JB3, and jumper blocks JB5 and JB6 are described in Section 2.6.2.4, below.

2.6.2.4 DDS Module Reference Frequency Select Jumpers – JB5 and JB6 on VMEbus Board

Each of the two DDS Modules on the Model 1420 contains a 50 MHz oscillator, which may be used as the Module's reference frequency source. This is accomplished by placing a jumper at the INT position of JB5 (for DDS #1) or JB6 (for DDS #2).

If you wish the two DDS modules to be locked to the same reference frequency, the jumpers at JB5 and JB6 should be placed at the EXT position. In this case, the output of the Model 1420's Frequency Multiplier will be used as the reference frequency for the DDS Modules. The multiplier's input may be either the 1420's crystal–controlled 10 MHz reference oscillator, or a signal applied to the front panel EXT CLK IN BNC connector, depending upon jumper settings at JB3 and JB4. Note that both the standard 10 MHz reference oscillator and the Module's 50 MHz internal oscillator are specified at 100 PPM accuracy. The 10 MHz oscillator on units equipped with Option 004 is specified at 3 PPM accuracy.

See the two sections above for details about jumper blocks JB3 and JB4. See Figure 1–1, on page 8 of this manual, for a block diagram showing the connectivity of all these jumper blocks.

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2.6 Jumper Configuration and Adjustments (continued)

2.6.2 VMEbus Board Jumper Blocks (continued)

2.6.2.4 DDS Module Reference Frequency Select Jumpers (continued)

NOTE: The DDS modules cannot be programmed in the absence of a clock signal. This means that when a DDS Module on the Model 1420 is jumper–programmed to use an external reference clock signal (i. e., when the jumper(s) at JB5 and/orJB6 are placed in the EXT position, AND the jumper on JB4 is in the EXT position),then the following conditions **MUST** also be met:

1) The front panel EXT REF connector **MUST** be jumper–programmed as an input (i. e., the jumper on JB3 **MUST** be placed in the IN position).

2) A clock signal **MUST** be connected to the front panel EXT REF connector.

If the above conditions are not met, none of the registers for the improperly configured DDS will be accessible.

2.6.3 Internal Reference Adjust (Option 004)

The Option 004 10 MHz Reference Oscillator is adjustable and may be cali–brated periodically with a frequency counter. The adjustment is made on the back face of the oscillator. Follow the steps below:

1) Set the reference jumpers so that the internal reference is available on the front panel. JB3 should be in the OUT position and JB4 should be in the INT position.

2) Connect a frequency counter to the EXT CLK IN BNC connector.

3) Adjust the sensitivity of the counter to obtain a reading of approximately 10 MHz.

4) Use a small, flat–bladed screwdriver with a blade width of 3/32".

5) Carefully insert the screwdriver until it engages in the adjustment screw.

6) While watching the reading on the frequency counter, slowly rotate the adjustment screw for an exact reading of 10.000 000 MHz.

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Chapter 3: Memory Maps and Operating Procedures

3.1 Introduction

This section describes the VME addressing of the Model 1420. From a programming point of view, the Model 1420 can be modeled as a group of memory mapped registers. These memory mapped registers are offset from the A24 VME base address, which the user sets by placing jumpers on VMEbus board jumper blocks JB1 and JB2. See Figure 2–4 (page 17) for jumper block locations, and Sections 3.2, below, and 2.6.2.1 (page 20) for more information about setting the base address. All transfers use the lower 8 bits of a 16–bit word.

3.2 Base Address Setup

The Model 1420 responds as a VMEbus slave in A24 address space. Sixteen VMEbus address lines, A8 – A23, are compared with the 16 address bits specified by jumper block JB1 and JB2 to determine the base address of the 256–byte region in which the Model 1420 will respond. Refer to Section 2.6.2.1 for jumper bit identification.

3.3 Address Modifier PROM

As shipped from the factory, the Model 1420 will respond to VMEbus address modifier (AM) codes 39, 3A, 3D, and 3E. These codes were factory programmed into the Address Modifier PROM, U7. The customer may alter the AM codes to which the Model 1420 will respond by replacing U7 with a similar type of PROM. This PROM is a Signetics 82S129, or the equivalent, which is a 256x4 bipolar type. The six least signif–icant address bits of the PROM are addressed by the six AM bits, AM0 through AM5. The two most significant PROM address bits are set to logic '0'. Figure 3–1, below, shows these connections schematically.

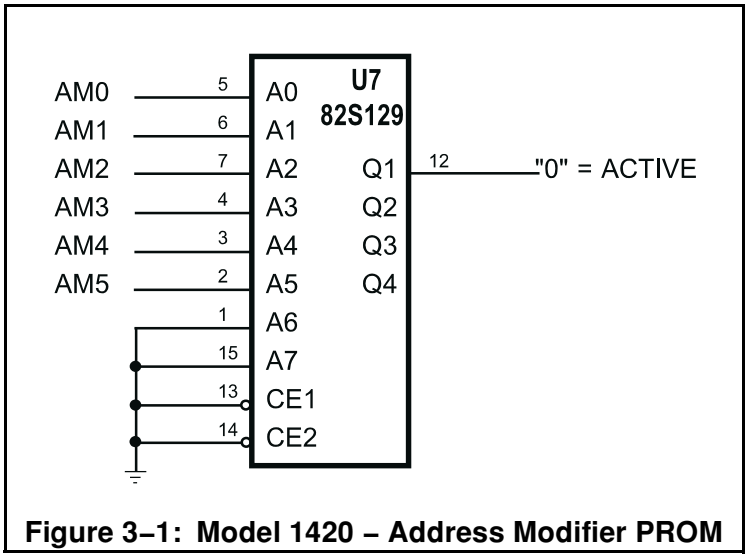


Figure 3–1: Model 1420 – Address Modifier PROM

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3.3 Address Modifier PROM (continued)

The PROM should be programmed such that for each address modifier code that you wish the 1420 to respond to, the Q1 output bit assumes the logic '0' state. All other codes should force the Q1 output to a logic '1'.

3.4 Memory Maps

There are two types of addressable resources on the Model 1420. These are registers that are located on the Model 1420 VMEbus board, and registers that are located in the Qualcomm synthesizer chips inside the DDS modules. The sections below provide address maps for all of these resources, and detailed descriptions of the registers on the VMEbus card. Brief descriptions of the Qualcomm registers are also provided in this chapter. More complete descriptions of these registers can be found in Appendix B of this manual, the Q2334 data sheet.

All addressing is given in the form VME_base+0xUV WXYZ, where VME_base is the A24 slave base address of the Model 1420, and UV WXYZ is the hex offset from the base address. The 0x prefix is commonly used to indicate hexadecimal numbers, and the space between the first two and last four digits of the offset is included for the sake of clarity.

3.4.1 Qualcomm Circuit Registers

The VMEbus A24 slave addresses for the registers in the Qualcomm Q2334 synthesizer chips, contained in the Model 1420's DDS Modules, is presented in Table 3–1, below.

Table 3–1: Model 1420 – VMEbus Slave Address Map for Q2334 Registers

Register	Channel 1 Address	Channel 2 Address	Channel 3 Address	Channel 4 Address
PIRA, Byte 1 - LSB	VME_base+0x00 0000	VME_base+0x00 0020	VME_base+0x00 0040	VME_base+0x00 0060
PIRA, Byte 2	VME_base+0x00 0002	VME_base+0x00 0022	VME_base+0x00 0042	VME_base+0x00 0062
PIRA, Byte 3	VME_base+0x00 0004	VME_base+0x00 0024	VME_base+0x00 0044	VME_base+0x00 0064
PIRA, Byte 4 - MSB	VME_base+0x00 0006	VME_base+0x00 0026	VME_base+0x00 0046	VME_base+0x00 0066
PIRA, Byte 1 - MSB	VME_base+0x00 0008	VME_base+0x00 0028	VME_base+0x00 0048	VME_base+0x00 0068
PIRB, Byte 2	VME_base+0x00 000A	VME_base+0x00 002A	VME_base+0x00 004A	VME_base+0x00 006A
PIRB, Byte 3	VME_base+0x00 000C	VME_base+0x00 002C	VME_base+0x00 004C	VME_base+0x00 006C
PIRB, Byte 4 - MSB	VME_base+0x00 000E	VME_base+0x00 002E	VME_base+0x00 004E	VME_base+0x00 006E
Sync Mode Control	VME_base+0x00 0010	VME_base+0x00 0030	VME_base+0x00 0050	VME_base+0x00 0070
Async Mode Control	VME_base+0x00 0014	VME_base+0x00 0034	VME_base+0x00 0054	VME_base+0x00 0074
Accumulator Reset	VME_base+0x00 0018	VME_base+0x00 0038	VME_base+0x00 0058	VME_base+0x00 0078
Async Hop Clock	VME_base+0x00 001C	VME_base+0x00 003C	VME_base+0x00 005C	VME_base+0x00 007C

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3.4 Memory Maps (continued)

3.4.1 Qualcomm Circuit Registers (continued)

3.4.1.1 Phase Increment Registers – PIRA and PIRB

Each synthesizer channel on the Model 1420 contains two Phase Increment Registers, called PIRA and PIRB. These double–buffered, 32–bit registers contain a value, which is passed to the Phase Accumulator, that controls how much the phase of the output waveform will advance at the next clock. PIRA is used for the increment value for simple, single–frequency operation, while PIRB provides a value that may be used for a second frequency for complex waveforms or other applications, such as Phase– or Frequency–Shift Keying (PSK or FSK).

The frequency of the generated waveform (i. e., f_g) is related to the frequency of the frequency reference (f_r) by the following equation:

$$f_g = \frac{f_r \times \Delta\theta}{2^{32}}$$

where $\Delta\theta$ is the value stored in the Phase Increment Register.

Each of these registers is seen from the VMEbus as four separate 8–bit locations, at four adjacent addresses. Four separate VMEbus write cycles are therefore needed to completely overwrite any of these registers. Because these registers are double–buffered, the values written to them are not transferred to the Phase Accumulators until the assertion of the HOPCLK signal. See Section 3.4.2.1 for more information about the HOPCLK signal. See Table 3–1 for the addresses of the Phase Increment Registers for each channel. See Appendix B for more details about the Phase Increment Registers.

3.4.1.2 Synchronous Mode Control Register – SMC

The Synchronous Mode Control Register for each DDS channel on the Model 1420 is double–buffered, to provide a means of updating control information while the channel is active. Changes to the contents of these registers become effective when the HOPCLK signal switches to the high state.

Only bits D1, D2 and D3 of these registers are used. All other bits are reserved, and should be written with 0's, as indicated in Table 3–2, at the top of the next page, which summarizes the bit definition of these registers. The text below the table describes the functions of the bits.

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3.4 Memory Maps (continued)

3.4.1 Qualcomm Circuit Registers (continued)

3.4.1.2 Synchronous Mode Control Register (continued)

Table 3–2: Model 1420 – Synchronous Mode Control (SMC) Register								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Function	N/U (0)	N/U (0)	N/U (0)	N/U (0)	HPME	EME	EPME	N/U (0)

External Phase Modulation Enable Bit (EPME) – D1:
When this bit is set to the '1' state, External Phase Modulation is enabled. In this mode, phase offsets in 45° increments can be implemented by appropriately setting the PM(0–2) bits from the Channel Control Register (see Section 3.4.2.2) or the front panel control connector, and asserting the PMCLK signal from the Master Clock Register (see Section 3.4.2.1) or the front panel control connector. Clear this bit to the '0' state to disable this function.

External Multiplexer Enable Bit (EME) – D2:
When this bit is set to the '1' state, the MUX signals from the front panel control connector or the Channel Control Register (see Section 3.4.2.2) are used to determine which Phase Increment Register (PIRA or PIRB) drives the Phase Accumulator. (MUX = 0 selects PIRA, MUX = 1 selects PIRB.) The selection is activated on the rising edge of the MUXCLK signal from the Master Clock Register (see Section 3.4.2.1) or the front panel control connector. When this bit is cleared to the '0' state, the state of the MUX signal is ignored and the Phase Accumulator gets its input from PIRA, unless the HOPCLK signal is asserted, in which case PIRB drives the Accumulator (see below).

Hopclock Phase Modulation Enable Bit (HPME) – D3:
When this bit is set to the '1' state, Internal Phase Modulation mode is enabled. In this case, the value stored in the PIRB register is added to the Phase Accumulator once for each assertion of the HOPCLK signal. Clear this bit to the '0' state to disable this function.

Again, remember that because these registers are double–buffered, changes to the states of the bits above do not affect the operation of the synthesizer until the rising edge of the HOPCLK signal.

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3.4 Memory Maps (continued)

3.4.1 Qualcomm Circuit Registers (continued)

3.4.1.3 Asynchronous Mode Control Register – AMC

These registers are **NOT** double–buffered, and therefore should be written to only during the initialization of the Q2334 IC's, **NOT** while the synthesizers are active. Bits D4, D6 and D7 of these registers are reserved, and should be written as 0's, as shown in Table 3–3, below, which summarizes the bit definition of these registers. The text below the table describes the functions of the bits.

Table 3–3: Model 1420 – Asynchronous Mode Control (AMC) Register

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	N/U (0)	N/U (0)	PMAE	N/U (0)	Output Format (1)	Noise Reduction Circuit Enable (1)	(0)	(0)

Noise Reduction Circuit Enable Bits (NRC) – D2, D1 and D0:
For the 10–bit DAC used in the Model 1420's DDS Modules, These three bits should usually be set to 1–0–0, as shown in Table 3–3, above. When bits D2 through D0 are set to binary '1', the Noise Reduction Circuit is disabled.

Output Format Bit (OF) – D3:
For use with the DACs in the Model 1420's DDS Modules, this bit must always be set to the '1' state, as shown in Table 3–3, above. This selects the Offset Binary output mode.

Phase Modulation Register Addition Enable Bit (PMAE) – D5:
This bit controls how the value stored in the PIRB register is used. If this bit is cleared to the '0' state, then when the PIRB is activated, all 32 of its bits are accumulated by the Phase Accumulator. If it is set to the '1' state, the 8 most significant bits of PIRB (when it is activated) are added to the 8 most significant bits of PIRA to form the 8 most significant bits to be accumulated. See Section B.6 for more details.

3.4.1.4 Accumulator Reset Register – ARR

When any data is written to a channel's Accumulator Reset Register, the Accumulator Reset function is armed. The next time that channel's HOPCLK signal is asserted, the Phase Accumulator for that channel will be reset to zero.

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3.4 Memory Maps (continued)

3.4.1 Qualcomm Circuit Registers (continued)

3.4.1.5 Asynchronous Hop Clock – AHC

When any data is written to a channel's AHC register, the values stored in the PIRA, PIRB and SMC registers become activated. This essentially provides a secondary means of activating these registers, which normally await the assertion of the HOPCLK signal. See Section B.8 for more details.

3.4.2 Registers on the VMEbus Board

There are five registers on the VMEbus board that affect the operation of the Model 1420. These are the Master Clock Register, and the four Channel Control registers. All of these registers are Read/Write accessible. In many applications, it may be desirable to make an identical change to the settings of more than one Channel Control Register simultaneously. To facilitate this, addresses are provided where combinations of Channel Control Registers are accessible for Write operations only. Table 3–4, below, shows the address map for the registers located on the Model 1420's VMEbus board.

Table 3–4: Model 1420 – Memory Map for Registers on the VMEbus Board

Address	Access	Resource(s)
VME_base+0x00 0082	***Read/Write***	Channel 1 Control Register
VME_base+0x00 0084	***Read/Write***	Channel 2 Control Register
VME_base+0x00 0086	Write Only	Channels 1 and 2 Control Registers
VME_base+0x00 0088	***Read/Write***	Channel 3 Control Register
VME_base+0x00 008A	Write Only	Channels 1 and 3 Control Registers
VME_base+0x00 008C	Write Only	Channels 2 and 3 Control Registers
VME_base+0x00 008E	Write Only	Channels 1, 2 and 3 Control Registers
VME_base+0x00 0090	***Read/Write***	Channel 4 Control Register
VME_base+0x00 0092	Write Only	Channels 1 and 4 Control Registers
VME_base+0x00 0094	Write Only	Channels 2 and 4 Control Registers
VME_base+0x00 0096	Write Only	Channels 1, 2 and 4 Control Registers
VME_base+0x00 0098	Write Only	Channels 3 and 4 Control Registers
VME_base+0x00 009A	Write Only	Channels 1, 3 and 4 Control Registers
VME_base+0x00 009C	Write Only	Channels 2, 3 and 4 Control Registers
VME_base+0x00 009E	Write Only	Channels 1, 2, 3 and 4 Control Registers
VME_base+0x00 00A0	***Read/Write***	Master Clock Register

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3.4 Memory Maps (continued)

3.4.2 Registers on the VMEbus Board (continued)

3.4.2.1 Master Clock Register – R/W @ VME_base+ 0x00 00A0

Table 3–5, below, summarizes the bit assignments in the Model 1420's Master Clock Register. The function of each bit is discussed below the table. Note that, with the exception of the Channel Control Register Reset Bit (D7), the functions provided by the bits in this register can also be activated from the front panel control connector, depending upon the state of the Control Source Select bit in that channel's Channel Control Register. See Section 3.4.2.2 for more details about the Channel Control Register.

Table 3–5: Model 1420 – Master Clock Register – R/W @ VME_base+0x00 00A0

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	CCReg Reset	Not Used	PM CLK	MUX CLK	HOPCLK Chan 4	HOPCLK Chan 3	HOPCLK Chan 2	HOPCLK Chan 1

Hop Clock Bits (HOPCLK) – D3, D2, D1 and D0:

The HOPCLK signal for each channel in the Model 1420 is used to activate changes made to the double–buffered PIRA, PIRB, and SMC registers. Changes made to these registers become active when the channel's HOPCLK signal makes the transition from the '0' state to the '1' state, which may be accomplished by changing the state of this bit.

Multiplexer Clock Bit (MUXCLK) – D4:

In External Multiplexing Mode, the MUX signal selects the contents of either PIRA (MUX = 0) or PIRB (MUX = 1) to drive the Phase Accumulator. The state of the MUX signal is registered by a rising edge on the MUXCLK signal, which may be provided by this bit. See the paragraph about the External Multiplexer Enable Bit in Section 3.4.1.2 for further details.

Phase Modulation Clock Bit (PMCLK) – D5:

In External Phase Modulation Mode, a rising edge on the PMCLK signal causes the phase of the output to be advanced by an amount determined by the settings of the PM(0–2) bits. The PMCLK signal may be provided by this bit, and the PM(0–2) bits may come from the Channel Control Register. See the paragraph about the External Phase Modulation Enable Bit in Section 3.4.1.2 for further details.

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3.4 Memory Maps (continued)

3.4.2 Registers on the VMEbus Board (continued)

3.4.2.1 Master Clock Register (continued)

Channel Control Register Reset Bit (CCR Reset) – D7:
When this bit is held in the '0' state, all bits in all four Channel Control Registers will be held in the reset (logic '0') state. This bit must be set to the '1' state in order to program any of the Channel Control Registers. The contents of these registers are described in the section below.

3.4.2.2 Channel Control Registers – R/W @
VME_base+0x00 0082 (Ch. A), VME_base+0x00 0084 (Ch. B), VME_base+0x00 0088 (Ch. C) & VME_base+0x00 0090 (Ch. D)

The bits in these four registers are used to determine the phase advance in External Phase Modulation Mode, to select a Phase Increment Register, to enable the synthesizer's analog output, and to select the source of control signals. The bit definition for each of these registers is given in Table 3–6, below. Note that the Model 1420's memory map provides addresses at which any combination of these four registers may be write–only accessed, to allow iden–tical changes to be made in multiple channels with a single VME operation (see Table 3–4, on the page before the previous.)

Table 3–6: Model 1420 – Channel Control Registers – R/W access – see Table 3–4 for Addresses

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	FP_Ctl Enable	Not Used	Not Used	DAC Enable	MUX (PIR Select)	PM2	PM1	PM0

Table 3-7: Model 1420 - External Phase Modulation Bit Settings

Phase Offset	PM2 (D2)	PM1 (D1)	PM0 (D0)
0°	0	0	0
45°	0	0	1
90°	0	1	0
135°	0	1	1
180°	1	0	0
225°	1	0	1
270°	1	1	0
315°	1	1	1

External Phase Modulation Bits (PM(2–0)) – D2, D1 and D0:
When External Phase Modulation Mode is enabled (D1 set in SMC register, see Section 3.4.1.2), and the FP Control Enable bit (D7 in this register) is cleared to the '0' state, these three bits will be used to determine the phase offset that will appear at the output when the PMCLK signal is asserted from the Master Clock Register. (If the FP Control bit is set to the '1' state, both the PMCLK signal and select function provided by these bits come from the front panel control connector.) Table 3–7, left, gives the offsets that will result from the settings of these bits.

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3.4 Memory Maps (continued)

3.4.2 Registers on the VMEbus Board (continued)

3.4.2.2 Channel Control Registers (continued)

Phase Increment Register Select Bit (MUX) – D3:

Each Qualcomm Q2334 IC contains two Phase Increment registers, designated PIRA and PIRB. The value stored in one of these 32–bit, double–buffered registers is passed to the Q2334's Phase Accumulator each time the HOPCLK signal is asserted, and dictates how much the phase of the generated waveform will advance. This bit determines which of the Phase Increment Registers will pass its value to the Phase Accumulator.

When the MUX bit is cleared to the logic '0' state, PIRA will determine the phase advance. PIRA is generally used for the generation of simple, single–frequency signals. When the MUX bit is set to the logic '1' state, PIRB will pass its value to the Phase Accumulator. PIRB is generally used to store a value used to generate additional frequencies, as in PSK or FSK applications. See Section 3.4.1.1 and Appendix B for further information.

D/A Converter Enable Bit (DAC Enable) – D4:

This bit must always be set to the logic '1' state in order to obtain any output signal from the DDS channel. The D/A Converter in the DDS Module changes the binary–coded, numeric output of the Qualcomm Synthesizer chip into an analog signal. This signal may, in turn, be passed through a comparator to provide a TTL logic signal at the output of the Model 1420 (see Section 2.6.1 and Figure 2–4 for details.) **The DAC Enable bit must be set to obtain ANY output,** regardless of what type of signal is desired. If a DAC Enable bit is cleared to the logic '0' state, no output signal can be generated by that channel of the Model 1420.

Front Panel Control Enable Bit (FP_Ctl Enable) – D7:

This bit is used to determine the source of the PMCLK, HOP–CLK, MUXCLK, MUX, DAC Enable and PM (0–2) control signals. When this bit is cleared to the logic '0' state, these signals come from the registers on the Model 1420 VMEbus board. When this bit is set to the logic '1' state, these signals come from the Front Panel Control Connector. The state of this bit, for all four channels, can be monitored on the Front Panel Control Connector.

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Appendix A: Programming Example

A.1 Introduction

This appendix provides sample 'C' language code for operating the Model 1420 in three different host environments. The first two sections (**1420_v.c** and **mapunx_v.c**) provide an example of initializing and controlling the Model 1420 from an embedded processor running SunOS. The next two sections (**1420_s.c** and **mapunx_s.c**) present an example of initialization and control of the Model 1420 from a SUN Workstation using the Bit3 SBUS–VME Adapter. In either of these examples, the variable **BASE_ADDR** must match your Model 1420's VME_base address setting from jumper blocks JB1 and JB2 (see Section 2.6.2.1). The **main()** routine may then call either **sweep()** (to generate a frequency sweep, using initial, final and step values from the **for** statement) or **test2()** (which allows the user to select a particular, fixed frequency to generate). The **mapunx** routines provide a system memory initialization function.

The last example (**83_1420.c**) uses the Pentek Model 4283 as VMEbus Master to initialize and control the Model 1420. In this example, the variable **DDSSEG1** must match the 1420's VME_base address (see above). If the **main()** routine calls **set_freq()**, then the value of the variable **FREQINIT** is used as the fixed frequency to be generated. If the sweep() routine is called instead, then the 1420 will generate a sweep from **FREQINIT** to **MAXFREQ**, using the value **FREQINCREMENT** at its step.

A.2 1420_v.c

```
#include <stdio.h>
#include <math.h>

#define BASE_ADDR 0x00800000L

unsigned long Dsp_Base = BASE_ADDR;

main()
{
          unsigned long i;
          Init_Memory();
          while(1)
             sweep();
}

sweep()
{
          unsigned long phase;
          charbuf[50];
```


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A.2 **1420_v.c** (continued)

```
          init();
          while(1)
          {
             for(phase=0x20000;phase<0x60000000;phase=phase+0x20000)
             {
                delay(1);
                setpira(phase);
                hopclk();
             }
          }
}

test2()
{
          unsigned long phase;
          char  buf[50];
          float freq;
          init();
          printf("Enter floating point frequency:");
          gets(buf);
          sscanf(buf,"%f",&freq);

          phase=(unsigned long)((freq/50.0e6)*4294967296.0);

          printf("Phase=%lx\n",phase);
          setpira(phase);
          hopclk();
}

init()
{
          Pokeb(0xa0,0xf0);  /* start with muxclk, pmclk and reset high */
          Pokeb(0x14,0xf);
          Pokeb(0x34,0xf);
          Pokeb(0x10,0x4);
          Pokeb(0x30,0x4);
          Pokeb(0x54,0xf);
          Pokeb(0x74,0xf);
          Pokeb(0x50,0x4);
          Pokeb(0x70,0x4);

          Pokeb(0x82,0x10);                    /* set mux and strb high */
          Pokeb(0x84,0x10);
          Pokeb(0x88,0x10);
          Pokeb(0x90,0x10);

          Pokeb(0xa0,0xe0);              /* pulse mux clk low then high */
          Pokeb(0xa0,0xf0);
```


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A.2 **1420_v.c** (continued)

```
        Pokeb(0x18,0x0);                    /* reset all accumulators */
        Pokeb(0x38,0x0);
        Pokeb(0x58,0x0);
        Pokeb(0x78,0x0);
}

setpira(phase)
unsigned long phase;
{
        char  temp0,temp1,temp2,temp3;

        temp0 = phase & 0xff;
        temp1 = (phase >> 8) & 0xff;
        temp2 = (phase >> 16) & 0xff;
        temp3 = (phase >> 24) & 0xff;

        Pokeb(0x0,temp0);
        Pokeb(0x2,temp1);
        Pokeb(0x4,temp2);
        Pokeb(0x6,temp3);

        Pokeb(0x20,temp0);
        Pokeb(0x22,temp1);
        Pokeb(0x24,temp2);
        Pokeb(0x26,temp3);

        Pokeb(0x40,temp0);
        Pokeb(0x42,temp1);
        Pokeb(0x44,temp2);
        Pokeb(0x46,temp3);

        Pokeb(0x60,temp0);
        Pokeb(0x62,temp1);
        Pokeb(0x64,temp2);
        Pokeb(0x66,temp3);
}

setpirb(phase)
unsigned long phase;
{
        char  temp0,temp1,temp2,temp3;

        temp0 = phase & 0xff;
        temp1 = (phase >> 8) & 0xff;
        temp2 = (phase >> 16) & 0xff;
        temp3 = (phase >> 24) & 0xff;
```


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A.2 **1420_v.c** (continued)

```
        Pokeb(0x8,temp0);
        Pokeb(0xa,temp1);
        Pokeb(0xc,temp2);
        Pokeb(0xe,temp3);

        Pokeb(0x28,temp0);
        Pokeb(0x2a,temp1);
        Pokeb(0x2c,temp2);
        Pokeb(0x2e,temp3);

        Pokeb(0x48,temp0);
        Pokeb(0x4a,temp1);
        Pokeb(0x4c,temp2);
        Pokeb(0x4e,temp3);

        Pokeb(0x68,temp0);
        Pokeb(0x6a,temp1);
        Pokeb(0x6c,temp2);
        Pokeb(0x6e,temp3);
}

hopclk()
{
        Pokeb(0xa0,0xff);           /* pulse hop clock high then low */
        Pokeb(0xa0,0xf0);
}

delay(time)
unsigned long time;
{
        unsigned int i;
        for (i = 0; i < 0x1000; ++i);
}
```


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A.3 mapunx_v.c

```
/*
   These modules maps the VME Card into virtual memory on a UNIX system
   and handle the subsequent definitions for low level memory access.
*/

#include <sys/ioctl.h>
#include <sys/param.h>
#include <sys/types.h>
#include <sys/mman.h>
#include <sys/file.h>
#include <fcntl.h>
#include <unistd.h>
#include <sgtty.h>
#include <stdio.h>
#include <ctype.h>
#include <math.h>

#undef PAGESIZE
#undef roundup

#define  LO_WORD0x0000FFFF      /* mask for low word of 32-bit number */
#define HI_WORD0xFFFF0000      /* mask for high word of 32-bit number */
#define Make_Long(Hi,Lo) (((((long)(Hi))<<16) & HI_WORD) + (Lo & LO_WORD))

#define BT_RRAM 0x1000000
#define BT_RBIO 0x0400000
#define BT_LBIO 0x0200000

#define PAGESIZE24 16777216
#define PAGESIZE16 65536
char  *Address;                         /* VMEbus A24 memory pointer */
char  *Ctladdr;                         /* VMEbus A16 memory pointer */
char  *Status;

/*
   NOTE: parameters in Init_Memory are NOT used in a virtual memory system.
*/

extern unsigned long Dsp_Base;

void Init_Memory()
{
         int   fd, fd1;

         if (( fd = open("/dev/vme24d16",O_RDWR)) == -1 )
         {
            perror("OPEN FAILED: ");
            return;
         }
```


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A.3 **mapunx_v.c** (continued)

```
        if(!(Address = mmap((caddr_t)0, PAGESIZE24, PROT_READ | PROT_WRITE,
                                                MAP_SHARED, fd, (off_t)0)))
        {
           perror ("MMAP 1 FAILED: ");
           return;
        }
}

/* low level memory access routines */

void Pokew(Addr, Data)
unsigned long Addr;
long Data;
{
        unsigned char  B1,B2,B3,B4;

        B2 = (unsigned char) ( Data & 0xff);
        B1 = (unsigned char) ( (Data >> 8) & 0xff);
        B4 = (unsigned char) ( (Data >> 16) & 0xff);
        B3 = (unsigned char) ( (Data >> 24) & 0xff);

        Address[ Dsp_Base | Addr++ ] = B1;
        Address[ Dsp_Base | Addr++ ] = B2;
        Address[ Dsp_Base | Addr++ ] = B3;
        Address[ Dsp_Base | Addr ] = B4;
}

long Peekw(Addr)
unsigned long Addr;
{
        unsigned char  B1,B2,B3,B4;
        unsigned int   Lo, Hi;

        B2 = Address[ Dsp_Base | Addr++ ];
        B1 = Address[ Dsp_Base | Addr++ ];
        B4 = Address[ Dsp_Base | Addr++ ];
        B3 = Address[ Dsp_Base | Addr ];
        Hi = ( (unsigned int)(B4 << 8) | (unsigned int)B3 );
        Lo = ( (unsigned int)(B2 << 8) | (unsigned int)B1 );
        return( (long)Make_Long(Hi,Lo) );
}

Pokeb(Addr, Data)
unsigned long Addr;
char Data;
{
        Address[ Dsp_Base | ++Addr ] = Data;
}

Peekb(Addr)
unsigned long Addr;
{
        return( Address[ Dsp_Base | ++Addr ] );
}
```


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A.4 1420_s.c

```
#include <stdio.h>
#include <math.h>

#define BASE_ADDR 0x00800000L

unsigned long Dsp_Base = BASE_ADDR;

main()
{
          unsigned long i;

          Init_Memory();

          while(1)
             test2();
}

sweep()
{
          unsigned long phase;
          char  buf[50];

          init();
          while(1)
          {
             for(phase = 0x20000; phase < 0x60000000; phase = phase + 0x20000)
             {
                delay(1);
                setpira(phase);
                hopclk();
             }
          }
}

test2()
{
          unsigned long phase;
          char  buf[50];
          float freq;

          init();
          printf("Enter floating point frequency:");
          gets(buf);
          sscanf(buf,"%f",&freq);
          phase=(unsigned long)((freq/50.0e6)*4294967296.0);
          printf("Phase=%lx\n",phase);
          setpira(phase);
          hopclk();
}
```


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A.4 **1420_s.c** (continued)

```
init()
{
          Pokeb(0xa0,0xf0);  /* start with muxclk, pmclk and reset high */

          Pokeb(0x14,0xf);
          Pokeb(0x34,0xf);
          Pokeb(0x10,0x4);
          Pokeb(0x30,0x4);
          Pokeb(0x54,0xf);
          Pokeb(0x74,0xf);
          Pokeb(0x50,0x4);
          Pokeb(0x70,0x4);

          Pokeb(0x82,0x10);                    /* set mux and strb high */
          Pokeb(0x84,0x10);
          Pokeb(0x88,0x10);
          Pokeb(0x90,0x10);

          Pokeb(0xa0,0xe0);              /* pulse mux clk low then high */
          Pokeb(0xa0,0xf0);

          Pokeb(0x18,0x0);                     /* reset all accumulators */
          Pokeb(0x38,0x0);
          Pokeb(0x58,0x0);
          Pokeb(0x78,0x0);
}

setpira(phase)
unsigned long phase;
{
          char  temp0,temp1,temp2,temp3;

          temp0 = phase & 0xff;
          temp1 = (phase >> 8) & 0xff;
          temp2 = (phase >> 16) & 0xff;
          temp3 = (phase >> 24) & 0xff;

          Pokeb(0x0,temp0);
          Pokeb(0x2,temp1);
          Pokeb(0x4,temp2);
          Pokeb(0x6,temp3);

          Pokeb(0x20,temp0);
          Pokeb(0x22,temp1);
          Pokeb(0x24,temp2);
          Pokeb(0x26,temp3);
```


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A.4 **1420_s.c** (continued)

```
        Pokeb(0x40,temp0);
        Pokeb(0x42,temp1);
        Pokeb(0x44,temp2);
        Pokeb(0x46,temp3);

        Pokeb(0x60,temp0);
        Pokeb(0x62,temp1);
        Pokeb(0x64,temp2);
        Pokeb(0x66,temp3);
}

setpirb(phase)
unsigned long phase;
{
        char  temp0,temp1,temp2,temp3;
        temp0 = phase & 0xff;
        temp1 = (phase >> 8) & 0xff;
        temp2 = (phase >> 16) & 0xff;
        temp3 = (phase >> 24) & 0xff;

        Pokeb(0x8,temp0);
        Pokeb(0xa,temp1);
        Pokeb(0xc,temp2);
        Pokeb(0xe,temp3);

        Pokeb(0x28,temp0);
        Pokeb(0x2a,temp1);
        Pokeb(0x2c,temp2);
        Pokeb(0x2e,temp3);

        Pokeb(0x48,temp0);
        Pokeb(0x4a,temp1);
        Pokeb(0x4c,temp2);
        Pokeb(0x4e,temp3);

        Pokeb(0x68,temp0);
        Pokeb(0x6a,temp1);
        Pokeb(0x6c,temp2);
        Pokeb(0x6e,temp3);
}

hopclk()
{
        Pokeb(0xa0,0xff);           /* pulse hop clock high then low */
        Pokeb(0xa0,0xf0);
}

delay(time)
unsigned long time;
{
        unsigned int i;
        for (i = 0; i < 0x1000; ++i);
}
```


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A.5 mapunx_s.c

```
/*
   These modules map the VME Card into virtual memory on a UNIX system
   and handle the subsequent definitions for low level memory access.
*/

#include <sys/ioctl.h>
#include <sys/param.h>
#include <sys/types.h>
#include <sys/mman.h>
#include <sys/file.h>
#include <fcntl.h>
#include <unistd.h>
#include <sgtty.h>
#include <stdio.h>
#include <ctype.h>
#include <math.h>

#undef PAGESIZE
#undef roundup

#define BT_RRAM 0x1000000
#define BT_RBIO 0x0400000
#define BT_LBIO 0x0200000

#define SEG 0
#define PAGESIZE24 16777216
#define PAGESIZE16 65536

#define LO_WORD0x0000FFFF       /* mask for low word of 32-bit number */
#define HI_WORD   0xFFFF0000   /* mask for high word of 32-bit number */
#define Make_Long(Hi,Lo) (((((long)(Hi))<<16) & HI_WORD) + (Lo & LO_WORD))

char  *Address;                          /* VMEbus A24 memory pointer */
char  *Ctladdr;                          /* VMEbus A16 memory pointer */
char  *Status;
unsigned long loopcount;

/*
   NOTE: parameters in Init_Memory are NOT used in a virtual memory system.
*/
extern unsigned long Dsp_Base;

void Init_Memory()
{
         int   fd, fd1;
         if (( fd = open("/dev/sbus1",O_RDWR ) == -1)
         {
            perror("OPEN FAILED: ");
            return;
         }
```


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A.5 **mapunx_s.c** (continued)

```
        if(!(Address = mmap((caddr_t)0, PAGESIZE24, PROT_READ | PROT_WRITE,
                                        MAP_SHARED, fd, (off_t)BT_RRAM)))
        {
           perror ("MMAP 1 FAILED: ");
           return;
        }

        if(!(Ctladdr = mmap((caddr_t)0, PAGESIZE16, PROT_READ | PROT_WRITE,
                                        MAP_SHARED, fd, (off_t)BT_RBIO)))
        {
           perror ("MMAP 2 FAILED: ");
           return;
        }

        if(!(Status = mmap((caddr_t)0, PAGESIZE16, PROT_READ | PROT_WRITE,
                                        MAP_SHARED, fd, (off_t)BT_LBIO)))
        {
           perror ("MMAP 3 FAILED: ");
           return;
        }

        Status[9] = 0x80;               /* Reset the VMEbus Interface */
        for (loopcount = 0; loopcount<0x100000; loopcount++);/* Kill some time */

        Status[9] = 0x00; /* Clear bit 7 of the Remote Node Status Register */
        Status[0] |= 0x80;          /* Clear Local Node Error Latches */
        Status[9] = 0x8;
        Status[8] = 0x40;
        Status[10] = Dsp_Base >> 24;
        Status[11] = (Dsp_Base >> 16) & 0xff;
        Status[12] = 0x3d;
}

/* low level memory access routines */

void Pokew(Addr, Data)
unsigned long Addr;
long Data;
{
        unsigned char  B1,B2,B3,B4;

        B2 = (unsigned char) ( Data & 0xff);
        B1 = (unsigned char) ( (Data >> 8) & 0xff);
        B4 = (unsigned char) ( (Data >> 16) & 0xff);
        B3 = (unsigned char) ( (Data >> 24) & 0xff);
        Address[ Addr++ ] = B1;
        Address[ Addr++ ] = B2;
        Address[ Addr++ ] = B3;
        Address[ Addr ] = B4;
}
```


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A.5 **mapunx_s.c** (continued)

```
long Peekw(Addr)
unsigned long Addr;
{
        unsigned char  B1,B2,B3,B4;
        unsigned int   Lo, Hi;
        extern unsigned long Dsp_Base;

        B2 = Address[ Addr++ ];
        B1 = Address[ Addr++ ];
        B4 = Address[ Addr++ ];
        B3 = Address[ Addr ];
        Hi = ( (unsigned int)(B4 << 8) | (unsigned int)B3 );
        Lo = ( (unsigned int)(B2 << 8) | (unsigned int)B1 );
        return( (long)Make_Long(Hi,Lo) );
}

void Pokes(Addr, Data)
unsigned long Addr;
unsigned int Data;
{
        unsigned char  B1,B2,B3,B4;

        B2 = (unsigned char) ( Data & 0xff);
        B1 = (unsigned char) ( (Data >> 8) & 0xff);
        Ctladdr[ Addr++ ] = B1;
        Ctladdr[ Addr++ ] = B2;
}

int Peeks(Addr)
unsigned long Addr;
{
        return( Ctladdr[ Addr ] );
}

Pokeb(Addr, Data)
unsigned long Addr;
char Data;
{
        Address[ ++Addr ] = Data;
}

Peekb(Addr)
unsigned long Addr;
{
        return( Address[ ++Addr ] );
}
```


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A.6 83_1420.c

```
#include <math.h>

#define DDSSEG1          0XE00000  /* start address of DDS 256 block of reg */
#define DDSSEG2          0XE00040                /* start add of seg 2 */
#define VMEADDMODREG     0X800001   /* add mod reg in c30 local mem space */
#define VMECONTROLREG    0X800000                        /* control reg */
#define VMEPAGEADDREG    0X800002
#define HIGH16           0X320
#define LOW16            0X120
#define MAXFREQ          (float)100000
#define FREQINCREMENT    (float)100
#define FREQINIT         (float)1000

main()
{
          unsigned long phase;
          int rdelay = 1000000,i;

          /* turn led on/off 5 times as sanity check  */
          for(i=0;i<5;i++)
          {
             asm(" ldi 6,iof");                          /* turn LED on */
             delay(rdelay);
             asm(" ldi 2,iof");                         /* turn LED off */
             delay(rdelay);
          }

          init1420(DDSSEG1);
          sweep(DDSSEG1);
}

sweep(unsigned int dds_offset)
{
          float   freq=FREQINIT;
          float   freq_inc = FREQINCREMENT;

          while(1)
          {
             if((freq = freq + freq_inc) >= MAXFREQ)freq_inc = -freq_inc;
             else if(freq <= FREQINIT)freq_inc = -freq_inc;
             delay(1000);
             set_freq(freq,dds_offset);
          }
}
```


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A.6 83_1420.c (continued)

```
void set_freq(float freq,unsigned int dds_offset)
{
          unsigned long phase;

          phase=(unsigned long)((freq/50.0e6)*4294967296.0);
          setpira(phase,dds_offset);
          hopclk(dds_offset);
          return;
}

init1420(unsigned int dds_offset)
{
          SetVMEAddMod(0X3D);
          SetVMEPageAddReg();
          poke(VMECONTROLREG,0x0,LOW16);

          poke(dds_offset,0x28,0xf0);  /* start with muxclk, pmclk and reset high */

          poke(dds_offset,0x5,0xf);
          poke(dds_offset,0x4,0x4);

          poke(dds_offset,0xd,0xf);
          poke(dds_offset,0xc,0x4);

          poke(dds_offset,0x15,0xf);
          poke(dds_offset,0x14,0x4);

          poke(dds_offset,0x1d,0xf);
          poke(dds_offset,0x1c,0x4);

          poke(VMECONTROLREG,0x0,HIGH16);
          poke(dds_offset,0x20,0x100000);

          poke(VMECONTROLREG,0x0,LOW16);
          poke(dds_offset,0x21,0x10);
          poke(dds_offset,0x22,0x10);
          poke(dds_offset,0x24,0x10);

          poke(dds_offset,0x28,0xe0);   /* pulse mux clk low then high */
          poke(dds_offset,0x28,0xf0);

          poke(dds_offset,0x6,0x0);          /* reset all accumulators */
          poke(dds_offset,0xe,0x0);
          poke(dds_offset,0x16,0x0);
          poke(dds_offset,0x1e,0x0);

          poke(dds_offset,0x7,0x0);               /* write to AHC once */
          poke(dds_offset,0xf,0x0);
          poke(dds_offset,0x17,0x0);
          poke(dds_offset,0x1f,0x0);
}
```


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A.6 **83_1420.c** (continued)

```
void delay(int count)
{
         int i;
         for(i = 0; i < count; i++);
}

void SetVMEAddMod(unsigned char  am_select)
{
         *(unsigned char *)VMEADDMODREG = (unsigned char)am_select;
         return;
}

void SetVMETransSelBits()
{
         *(unsigned int *)VMECONTROLREG = 0X00;
}

void SetVMEPageAddReg()
{
        *(unsigned char *)VMEPAGEADDREG = 0X00;
}

void poke(unsigned int seg,unsigned int add,unsigned int val)
{
         *(unsigned int *)(seg+add) = (unsigned int)val;
         return;
}

setpira(unsigned long phase,unsigned int dds_offset)
{
         unsigned int   temp0,temp1,temp2,temp3;

         temp0 = phase & 0xff;
         temp1 = (phase  & 0xff00) << 8;
         temp2 = (phase & 0xff0000) >> 16;
         temp3 = (phase & 0xff000000) >> 8;

         poke(VMECONTROLREG,0x0,LOW16);

         poke(dds_offset,0x0,temp0);
         poke(dds_offset,0x8,temp0);
         poke(dds_offset,0x10,temp0);
         poke(dds_offset,0x18,temp0);
         poke(dds_offset,0x1,temp2);
         poke(dds_offset,0x9,temp2);
         poke(dds_offset,0x11,temp2);
         poke(dds_offset,0x19,temp2);
```


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A.6 **83_1420.c** (continued)

```
        poke(VMECONTROLREG,0x0,HIGH16);

        poke(dds_offset,0x0,temp1);
        poke(dds_offset,0x8,temp1);
        poke(dds_offset,0x10,temp1);
        poke(dds_offset,0x18,temp1);
        poke(dds_offset,0x1,temp3);
        poke(dds_offset,0x9,temp3);
        poke(dds_offset,0x11,temp3);
        poke(dds_offset,0x19,temp3);

        poke(VMECONTROLREG,0x0,LOW16);
        return;
}

hopclk(unsigned int dds_offset)
{
        poke(dds_offset,0x28,0xf0);
        poke(dds_offset,0x28,0xff); /* pulse hop clock high then low */
        poke(dds_offset,0x28,0xf0);
}
```


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Appendix B: Qualcomm Q2334 Dual Digital Frequency Synthesizer Data Sheet

B.1 Introduction

Most of the following text comes directly from the Qualcomm Q2334 data sheet. It is repeated here for convenience, although the customer may wish to obtain a copy from Qualcomm directly. Any alterations to the original text are included in brackets [].

The address is:

Qualcomm, Inc.
10555 Sorrento Valley Road
San Diego CA 92121–1617

B.2 Architecture

The Q2334 device includes two identical, independent Direct Digital Synthesizer (DDS) functions with a common microprocessor interface. Each DDS includes two double–buffered Phase Increment Registers, a Phase Increment Multiplexer, a Phase Accumulator, a Sine lookup Function, and a Noise Reduction Function. These are described in detail in the following paragraphs.

B.3 Processor Interface

The processor interface is compatible with most commonly used microprocessors. This interface includes address decoding, chip selection, and write controls to set all on–chip control and Phase Increment Registers. [Section 3.4 of this manual] gives the register address maps for [these resources on Model 1420 VMEbus board]. Each register is write–only and is decoded from the five–bit input address bus. It is important to note that the addresses listed as "reserved" must not be written to while using the Q2334 device. [Reserved addresses are not decoded by the VME card and do not appear in the VME address map.]

The two Phase Increment Registers and the Synchronous Control Register for each DDS function are double buffered. That is, these registers can be loaded at any time by the processor, but the values become active only when the signal HOPCLK is asserted. This makes possible the advanced synchronous phase and frequency change features of the Q2334 device which are especially important when using the device in modulation or phase locked loop applications. Writing to the Asynchronous Hop Clock Register will also activate the pre–stored phase increment and control bits for systems in which the HOPCLK signals are not used.

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B.4 Phase Increment Registers

Two independent 32–bit Phase Increment Registers (A and B) are provided for each DDS function in the Q2334 device. Each Phase Increment Register is 32–bits wide. Phase increment Register A of each DDS provides the phase increment for the most basic single–frequency operation. Phase Increment Register B provides the phase increment for a range of functions useful in various modes of operation of the DDS. The 32–bit value for each register is loaded using 4 8–bit write operations. Each Phase Increment Register is double buffered. The phase increment actually used by the Phase Accumulator is unaffected by this new stored value until a transition on the HOPCLK signal occurs.

B.5 Synchronous Mode Control (SMC) Register

Each DDS function on the Q2334 device includes two mode control registers. The Synchronous Mode Control (SMC) Register is double buffered to provide for updating of the control information which will affect the actual DDS operation only when synchronously enabled by the transition of the HOPCLK signal. [Section 3.4] shows the bit definition for this Synchronous Mode Control Register. Bits 0 (the LSB), 4 ,5, 6 and 7 are reserved and should be set to logic 0. The remaining bits of the SMC Register are the Hop Clock Phase Modulation Enable (HPME), External Multiplexer Enable (EME), and the External Phase Modulation Enable (EPME). The HPME bit is used when operating in the Internal Phase Modulation mode. When this bit is set to logic one the phase increment value stored in the PIRB register is added to the Phase Accumulator once each time the HOPCLK signal is asserted. The EME bit enables the External Multiplex Control. When this bit is set to logic one the [MUX] signals determine whether the value stored in the PIRA or PIRB register is used for the phase accumulation process. The selection on the [MUX] signals is synchronously activated on the rising edge of the MUXCLK signals when the EME is set to logic one. The EPME enables the external phase modulation function. The functions of these control bits are further described below in the sections describing modulation modes.

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B.6 Asynchronous Mode Control (AMC) Register

The Asynchronous Mode Control (AMC) Register of each DDS function includes control bits which should only be configured during initialization of the Q2334 device. These control bits, shown in [Section 3.4] include the Phase Modulation Add Enable (PMAE), Sign Type Select, and NRC Enable. Bits 4, 6, and 7 of the AMC Register are reserved and should be set to 0. The PMAE bit controls the way in which the value stored in the PIRB register is used by the Phase Accumulator. When the PMAE bit is set to logic 1 and the PIRB register is active for accumulation in the Phase Accumulator the most significant eight bits of the PIRB register are added to the most significant eight bits of the PIRA register to form the most significant eight bits to be accumulated. The least significant 24 bits of the PIRA register are used as the least significant 24 bits of the Phase Accumulator input value. This technique is useful for systems utilizing the Internal Phase Modulation mode of operation. By storing the synthesizer frequency in the PIRA register and modifying only the most significant byte of the PIRB register a 256 state phase modulator is implemented. This feature saves computation time in the processor controlling the DDS operation when a phase modulation system with 256 state (i. e., 1.41°) phase resolution is adequate. Using only the most significant eight bits of the PIRB register to control the phase modulation allows the user to establish a byte–wide Direct Memory Access (DMA) control from the processor to the DDS function phase modulation register (ie. PIRB), simplifying the processor overhead required to control the DDS function in rapidly switching phase modulation systems. When the PMAE bit is set to logic 0 all 32 bits of the PIRB register will be accumulated in the Phase Accumulator when the PIRB register is active.

The Sign Type bit determines the binary coding of the D/A Converter output bits of each DDS function. When this bit is set to logic 1 the D/A Converter output is encoded in offset binary format. [The sign bit should always be set to logic 1 for the Model 1420's DDS Module.]

When using the on–chip Noise Reduction Circuit (NRC) function the number of significant bits to be used from the D/A Converter Outputs must be programmed into the NRC Enable bits. The D/A Converter bit–width is encoded in three bits as shown in [Section 3.4]. When using a D/A converter with fewer than 12 bits resolution, the most significant D/A Converter Output bits are valid. The NRC function is disabled when the NRC Enable bits are set to 111 (binary). The function of the NRC circuit is described below.

B.7 Accumulator Reset Register (ARR)

Each DDS function on the Q2334 device includes an Accumulator Reset Register (ARR). By writing any value to the ARR the Accumulator Reset Function is armed. The next time the HOPCLK is asserted the Phase Accumulator is reset to zero.

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B.8 Asynchronous Hop Clock (AHC)

Each DDS function includes an Asynchronous Hop Clock (AHC) Register. When any value is written to this register the previously stored values in the double–buffered PIRA, PIRB, and SMC Registers are activated. This allows processor control of activation of these settings in an identical fashion as with the assertion of the HOPCLK signal. Note that the HOPCLK signal must be low when the AHC register is accessed in order to activate the new register values. Activation of the stored settings occurs within 4 SYSCLK periods after writing to the AHC Register. [NOTE: SYSCLK refers to the synthesizer's 50 MHz reference frequency.]

B.9 Frequency Multiplexer

The Frequency Multiplexer function selects which PIR register (A or B) is used for accumulation in the Phase Accumulator function. This multiplexing function provides a simple binary frequency shift keying interface to the DDS. The signal [MUX] controls the selection of the value stored in either the PIRA or the PIRB register, and the signal MUXCLK enables the selection made by the [MUX] signal. The MUXCLK signal is internally synchronized to the SYSCLK signal of the DDS. The selection made by the [MUX] signal is activated synchronously once during the low–to–high transition on the MUXCLK signal. The selection of the [MUX] control may occur as frequently as once every four periods of SYSCLK. Two Frequency Multiplexer functions are provided on the Q2334 device, one for each DDS.

B.10 Phase Accumulator

Two 32–bit wide Phase Accumulators are included in the Q2334 device, one for each DDS function. These accumulators compute and store the sum of the previously computed phase value and the phase increment value, from either the PIRA or PIRB register, once during each period of SYSCLK.

B.11 Phase Modulation Control

The output of the Phase Accumulator can be offset by phase increments of 45°, from 0° to 315° without affecting the operation of the Phase Accumulator using the External Phase Modulation inputs. These inputs are latched into the DDS function when the signal PMCLK is asserted. Changes in the External Phase Modulation are synchronized internally to the DDS function. This provides a simple 8–phase shift keying interface to the DDS.

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B.12 Sine Lookup Function

The most significant 16 bits of the phase accumulator are used by the DDS Sine Lookup Table to generate a 12–bit sine wave value for each period of the SYSCLK. This Sine Lookup Table function uses a proprietary (patent pending) technique for deriving the sinewave value which differs considerably from the traditional method of using a ROM lookup function. This advanced technique provides highly accurate and precise sine–wave generation.

B.13 Noise Reduction Circuit (NRC)

The phase noise spurs associated with the roundoff errors of the quantized sine wave outputs can be significantly reduced by enabling the on chip Noise Reduction Circuit (NRC). This proprietary (patent pending) circuit distributes the noise energy more evenly across the frequency band, reducing the amplitudes of peak phase noise components. It is important to properly set the D/A Converter Size bits in the Asynchronous Mode Control registers described above when the NRC is enabled.

The output of the Noise Reduction Circuit is a 12–bit wide digitized sine wave which is normally connected to an external D/A Converter function. This output value [must] be encoded in Offset Binary [for use in the Model 1420's DDS Module]. A clock strobe signal, DAC STB, is also provided with this 12–bit output to facilitate strobing this digitized sinewave value into a sample–and–hold D/A converter or other register.

B.14 Modes of Operation

B.14.1 Basic Synthesizer mode

In its most basic operational mode each DDS on the Q2334 device can provide a fixed frequency digitized sine wave output. The frequency of this sine output is determined by the frequency of the reference input and the value stored in the Phase Increment registers. Each DDS can be independently set to perform a wide range of expanded functions of the basic operation as described in the following paragraphs.

B.14.2 Phase Modulation

The Q2334 provides two means to implement phase modulation of a basic frequency output, referred to as Internal Phase Modulation and External Phase Modulation. Internal Phase Modulation provides extremely fine resolution of the phase adjustment, while the External Phase Modulation is restricted to phase modifications in 45° increments.

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B.14 Modes of Operation (continued)

B.14.3 Internal Phase Modulation

Internal Phase Modulation operates as a differential phase adjustment technique and requires use of the processor interface. The internal Phase Modulation mode is activated by loading the PIRA register with the correct phase increment for the basic frequency without phase modulation. The PIRB register is then loaded with the phase increment value stored in the PIRA register plus the value of the desired phase offset. The Phase Accumulator uses the PIRA register for most phase accumulations. Setting the HPME bit in the SMC register to logic 1 arms the DDS to use the value in the PIRB register for one phase accumulation cycle when the signal HOPCLK is asserted. Since the phase increment value in the PIRB register is only used once for each HOPCLK assertion the net effect is to cause a phase change to the generated sine–wave. The PIRB must be reloaded before each HOPCLK cycle with the desired phase offset for this next HOPCLK period. The HPME bit will remain set to 1 until reset by the processor.

B.14.4 External Phase Modulation.

External Phase Modulation operates as an absolute phase adjustment technique and utilizes special synchronous inputs separate from the processor interface. When using the External Phase Modulation mode the phase increment value for the unmodulated input is written into the PIRA register. The PIRB register is not normally used in the external phase modulation mode. The External Phase Modulation Enable (EPME) bit in the SMC register is set to logic 1 to enable the External Phase Modulation mode. With this bit set to 1 the phase offset determined by the [PM bits] are latched into the DDS function each time the signal PMCLK is asserted. This [PM bit] setting causes a phase offset in 45° increments. This mode of operation allows very simple control of the DDS as an [8 state] phase shift keyed (8PSK) modulator.

B.14.5 BFSK Modulation Mode

Binary Frequency shift keying (BFSK) Modulation is achieved in the Q2334 by setting the phase increment value in the PIRA register to generate the first frequency and the value in the PIRB register to generate the second frequency. The External Modulation (EME) bit is then set to logic 1 to enable the External Multiplexer controls. If the [MUX] signal is high when the MUXCLK is asserted the phase accumulator accumulates the phase increments from the PIRB register. If the [MUX] signal is low when the MUXCLK is asserted the Phase Accumulator accumulates phase increments from the PIRA register. Changing the value of the [MUX] input therefore causes the alternation between the frequency controlled by the PIRA register and the frequency controlled by the PIRB register.

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B.14 Modes of Operation (continued)

B.14.6 Frequency Hopping Mode

Simple frequency hopping can be enabled by writing a new value of the desired frequency in PIRA. This value will be activated at the next assertion of the HOPCLK signal. The DDS D/A converter output will reflect the change in frequency within 31 SYSCLK periods.

B.14.7 MSK Modulation Mode

Multiple Shift Keying (MSK) Modulation Mode is a special case of the BFSK mode described above. In this case the PIRA register is loaded with the incre–menting phase value while the PIRB register is loaded with the decrementing phase value. The EME bit of the SMC register is set to logic 1, as in the BFSK mode, and the [MUX] and MUXCLK signals control the shift between the val–ues of the PIRA and the PIRB registers.

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