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OPERATING MANUAL

MODEL 1480B

VMEbus DC - 8 MHz
FREQUENCY SYNTHESIZER

PENTEK
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Pentek Model 1480B Operating Manual - Revision History

Date	Rev	Applicable Serial #'s	Comments
12/90	Preliminary	9050009 - 9118001	Initial Product Release
6/91	A	9118002 - 9307110	Change in Address decode logic
12/92	B	9307111 - 9316000	Comparator (TTL O/P drive) changed from LM360 to NE521.
4/93	C	9316000 - Forward	Add info on option 009. TTL O/P must be terminated in 50 ohm. Pages re-numbered. Appendices added for options, code examples.
12/94	C.1	9316000 - Forward	Corrected Sine Output Level spec (into Hi-Z) for Option 101.
11/12/96	C.2	9316000 - Forward	Re-formatted. Minor clarifications & text changes. Added Figures & Tables to Table of Contents.

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Chapter 1: Introduction

1.1 General Description

The Pentek Model 1480B Direct Digital Frequency Synthesizer is a complete instrument packaged on a VMEbus card containing either one or two synthesizer channels. Each channel is independently programmable, and covers a frequency range from DC to 8 MHz.

Direct digital synthesis provides phase-continuous switching between frequencies and permits phase reset control for synchronizing the two channels, creating burst waveforms, or generating complex FSK sequences with repetitive waveforms.

Both sine- and square-wave outputs are provided, either through BNC connectors on the front panel or through the P2 bus connector. An on-board 20 MHz crystal oscillator provides the frequency reference from which all accuracy and stability specifications are determined. An external 20 MHz reference may be provided to lock the Model 1480B to a system reference.

1.2 Theory Of Operation

The Model 1480B consists of one or two DDS (Direct Digital Synthesizer) modules and a VMEbus card.

1.2.1 DDS (Direct Digital Synthesis) Operation

Each DDS module accepts 40-bits of parallel BCD frequency program data and produces a synthesized sinewave between DC and 8 MHz with resolution of 0.001 Hz throughout the range.

The technique of DDS employs a digital phase accumulator which increments in value once each reference clock cycle. The full range of the accumulator represents 360° of the synthesized waveform. The accumulator addresses a sine table ROM, converting the accumulator phase to the instantaneous voltage value of a sine waveform at each phase point. The ROM output drives a D/A converter producing a sampled analog signal. A lowpass filter removes the sampling components, leaving the fundamental sine signal.

Frequency control is achieved by changing the phase increment to the phase accumulator, thus advancing through the 360° range at proportionally different rates.

The DDS modules employed in the Model 1480B are clocked at 20 MHz and feature a 1000 point sine ROM with samples stored to 12-bit accuracy. A 12-bit D/A converter and 8 MHz lowpass filter complete the assembly.

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1.2 Theory Of Operation (continued)

1.1.2 VMEbus Card

The VME Bus card provides a physical and electrical interface between the DDS modules and the VME Bus environment. Each DDS plugs into two 36-pin socket strips, permitting modularity and easy servicing.

Circuitry on the board includes the address decoder, address modifier PROM, primary frequency registers with readback capability, control register, sine-to-square converters, output amplifiers, 20 MHz reference oscillator, and voltage regulators.

1.3 Specifications

VME Bus Characteristics:

Bus Device Type:	Slave
Data Path Width:	D16
Address Path Width:	A24

Address Modifier Codes: 39, 3A, 3D, and 3E (user configurable)

Number of Channels:

Option 001:	Single Channel
Option 002:	Two Channels

Dimensions: Double VME Board (6U): 160 mm x 233.35 mm

Operating Temperature: 0°C to +50°C

Connectors: Power and program via DIN connectors (P1 & P2)

Standard:	Signals via panel mounted BNC's
Option 003:	Signals via P2 DIN connector

Power Requirements:

Option 001:
- + 5 VDC @ 2.0 A
- – 12 VDC @ 200 mA
- +12 VDC @ 10 mA

Option 002:
- + 5 VDC @ 3.0 A
- – 12 VDC @ 400 mA
- +12 VDC @ 20 mA

Frequency Range: DC to 7.999 999 999 MHz

Frequency Resolution: 0.001 Hz throughout the range

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1.3 Specifications (continued)

Frequency Accuracy: (using internal reference oscillator)
Standard: ±100 ppm
Option 004: ± 3 ppm
NOTE: If External 20 MHz reference frequency is applied, the accuracy of this unit tracks the accuracy of the applied signal.

Integrated Phase Noise: – 50 dBc in 30 kHz BW

Spurious Components: – 50 dBc (BNC sine output)

Harmonic Components: – 50 dBc (BNC sine output)

Switching Delay: Less than 1 usec
Switching Mode: Phase-continuous for all changes
Sine Output Level: 0.707 Vrms (+10 dBm) into 50 Ω

Sine Output Impedance: 50 Ω nominal

TTL Outputs: Square Wave
TTL Output Impedance: 50 Ω nominal

Option 004 Reference:
Accuracy: ±1 ppm maximum error at 25°C
Temperature Stability: ±3 ppm from 0°C to 50°C
Aging (typ after 30 days): 5 ppm first year, 3 ppm/year thereafter

Option 101:
Frequency Range: DC - 100 kHz
Number of Channels: Two
Frequency Reference: Same as Option 004 above
Sine Output Level: 1 V_{RMS} (+13 dBm) into 50 Ω at P2 Connector.
2 V_{RMS} (+19 dBm) no load with 1 kΩ source impedance at front panel BNC connectors.

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Chapter 2: Operation

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If you discover any damage, please contact Pentek immediately, at the phone number shown on this manual's title page. Please save the original shipping container and packing material, in case re-shipment is required.

2.2 Mechanical

The Model 1480B fits into a standard double-height (6U) VMEbus card cage and occupies 4HP units. Two DIN 41612 connectors are installed, although P2 is essentially non-functional except for Options 003 and 101 where it is used for sine and square signal connections.

Each of the two DDS Modules is attached to the VME board by two 36-pin SIL connectors. Before installing the Model 1480B into the VME card cage, make sure both DDS modules are fully seated in their connectors.

Caution: Never remove or re-install a DDS module from the VME board with power on.

2.2.1 Inserting the Model 1480B in the VMEbus Card Cage

Align the Model 1480B card edge with the cage card guides and push evenly on both ejector handles until the front panel seats against the upper and lower rails. Secure the unit to the cage by tightening the upper and lower retainer screws in the front panel.

Caution: Never insert or remove the Model 1480B while power is applied in the card cage.

2.2.2 Removing the Model 1480B from the VMEbus Card Cage

Loosen the upper and lower retaining screws; they are captive screws and will remain part of the panel assembly. Gently push both ejector handles apart (away from the center of the panel) until the unit unseats itself from the cage connectors and then pull outward to remove the unit.

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2.3 Signal Connections

Each DDS channel has three output signals: sinewave, TTL squarewave, and complementary TTL squarewave. One common 20 MHz reference input is shared by both channels. Signal connections are available via front panel BNC connectors on the standard unit, and via P2 pins on the Option 003. Option 101 provides signals on both the front panel and P2. The front panel sine outputs for option 101 are for monitoring purposes only and have a 1 kΩ source impedance. Table 2-1, below, shows the connectors for each signal. The nomenclature used in the table for the P2 connector pins conforms to the VMEbus standard. The designation 2A: 13 means P2 connector, Row A, pin 13. The TTL complementary signals are not available in the standard unit. The external reference input is not supported in Option 003.

Table 2-1: Model 1480B - Signal Connections

Signal	Front Panel	P2 Connector
Sine A Return	J7	2A: 13 2A: 12,14
Sine B Return	J5	2A: 28 2A: 27,29
TTL-A Return	J8	2A: 10 2A: 11
TTL-B Return	J6	2A: 25 2A: 26
TTL-A Comp Return	-	2A: 8 2A: 9
TTL-B Comp Return	-	2A: 23 P2A: 24
Ref In/Out	J9	-

2.4 Signal Characteristics

The characteristics of signals that may be applied to, and are generated by, the Pentek Model 1480B are discussed in the subsections that follow.

2.4.1 Sine Outputs

The sine outputs are 0.707 V_{RMS} (+10 dBm) with a source and load impedance of 50 Ω. In order to maintain the specified frequency response and spectral purity, the load must be terminated in 50 Ω. Option 101 provides a 1 V_{RM} (+13 dBm) output level into 50 Ω at the P2 connector (up to 100 kHz). The front panel sine outputs have a 1 kΩ source impedance.

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2.4 Signal Characteristics (continued)

2.4.2 TTL Outputs

The TTL outputs are each capable of driving up to 16 standard TTL loads, which represents a sink current of 25.6 mA. We recommend that the TTL output also be terminated in 50 Ω at the receiving end, to minimize ringing.

2.3.3 20 MHz Reference Input

The reference input must be a 20 MHz TTL signal with a pulse width between 15 and 35 nsec. The termination on the board is one input of a type 74S32 gate. If this input is driven from a cable longer than a few feet, it is recommended that an in-line terminator be placed at J9 to avoid ringing.

2.5 Internal/External Reference Jumpers

In order to select the various modes of the 20 MHz frequency reference operation, the jumpers indicated in Table 2-2, below, must be installed. These jumpers are located in the central region of the VME board between the two DDS modules (see Figure 2-1, at the bottom of this page).

Table 2-2: Model 1480B - Frequency Reference Jumpers

Reference Source	Reference Out	Jumpers Installed
Internal Oscillator	No	JP2, JP3, JP6
	Yes	JP2, JP3, JP5
External TTL Signal	-	JP1, JP4, JP6

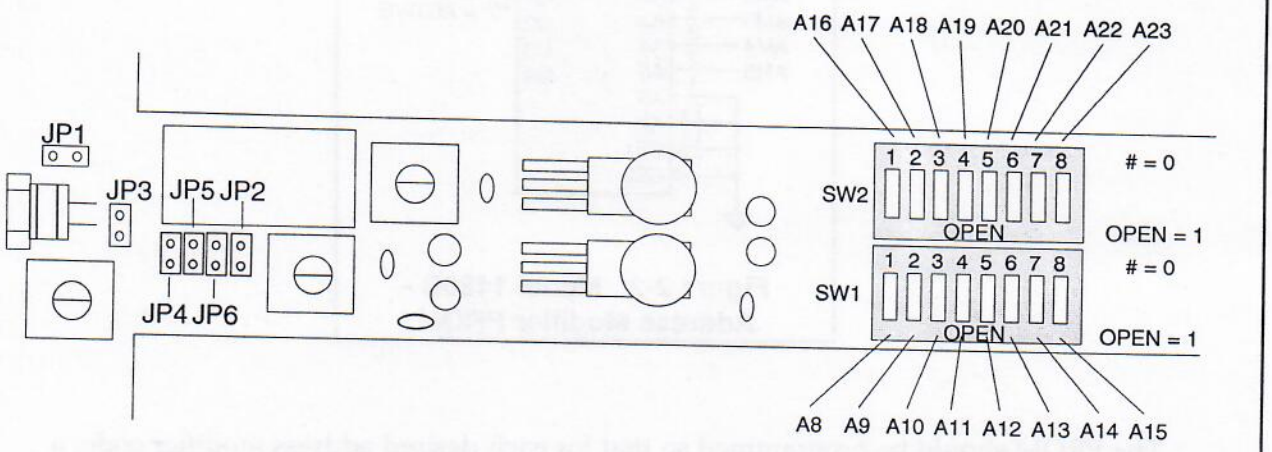


Figure 2-1: Model 1480B - Location of Reference Jumpers and Address Switches

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2.5 Internal/External Reference Jumpers (continued)

The 20 MHz reference can be sourced from either the internal oscillator, or from an external 20 MHz TTL signal. The Reference BNC connector, J9, is used as the *input* connector for an external reference input and as the *output* connector for the internal reference oscillator.

2.6 Base Address DIP Switches

The Model 1480B occupies 256 bytes of address space which can be located at any 256-byte boundary in the 24-bit address space. To specify the base address of the 256-byte region, two DIP switches, SW1 and SW2, are provided on the VME Board. The address bits are designated for the DIP switches in Figure 2-1, at the bottom of the previous page.

In order to set the base address, depress the side marked "OPEN" of each DIP switch for each address bit equal to logic "1" and depress the numbered side for logic "0".

2.7 Address Modifer Code PROM Programming

The customer may alter the Address Modifer (AM) codes to which the board responds by replacing PROM U1 with a specially programmed unit. This PROM is equivalent to Signetics 82S129 which is a 256 x 4 bipolar type. The six least significant address bits of the PROM are addressed by the six AM bits, AM0 through AM5. The two most significant PROM address bits are set to logic "0". Figure 2-2, below, shows these connections schematically.

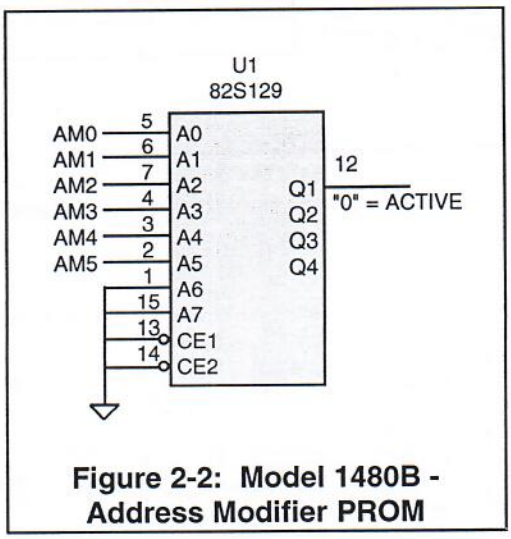


Figure 2-2: Model 1480B - Address Modifier PROM

The PROM should be programmed so that for each desired address modifier code, a logic "0" will appear at the Q1 output bit. All other addresses should produce a logic "1" at Q1.

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2.8 Sine Amplitude Adjustment

Provisions are made for independently adjusting the amplitude of each of the sinewave signals by approximately ±10% about the nominal output level, by the use of potentiometers. The reference designations for these 3/8" square trimmer pots is given in Table 2-3, below. Their locations are shown in Figure 2-3, at the bottom of this page. The adjustment should be made with the output terminated in a 50 Ω load.

Table 2-5: Model 1480B - Adjustment Controls

Channel	Adjustment	Ref. Designation
DDS-A	Amplitude	RV1
	Offset/Symmetry	RV2
DDS-B	Amplitude	RV3
	Offset/Symmetry	RV4

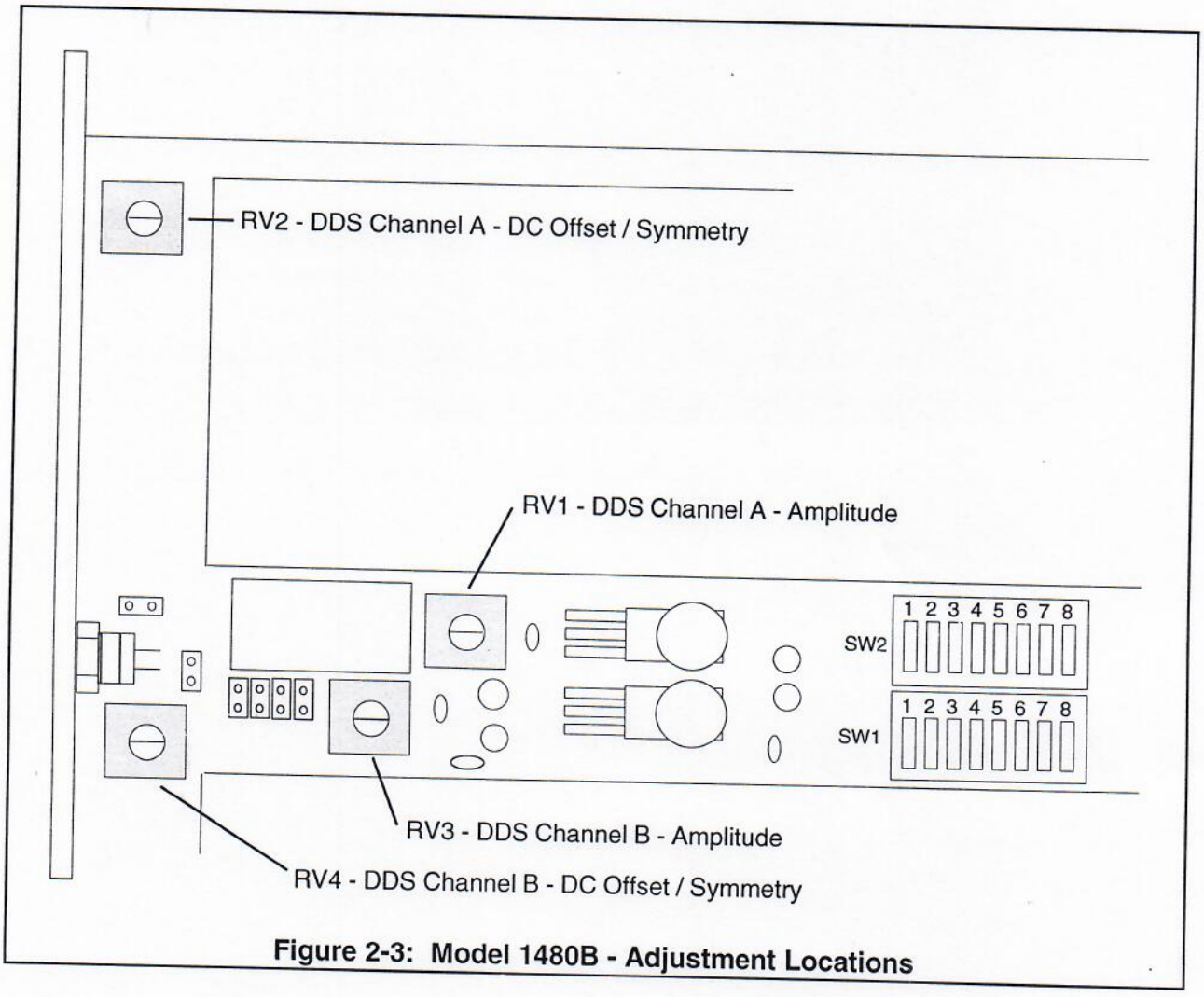


Figure 2-3: Model 1480B - Adjustment Locations

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2.9 Sine DC Offset Adjustment

The DC offset of the sinewave output signals can be adjusted over a range of approximately ±50 mV. The adjustment should be made with the output terminated in a 50 Ω load. Use the Zero Phase command (see Section 3.2.4.2) to force the zero-phase point to make the adjustment easier. Reference designations for these controls are shown in Table 2-3 (in the middle of the prsvious page), and their locations are shown in Figure 2-3 (at the bottomof the previous page).

2.10 TTL Symmetry Adjustment

The DC offset adjustment for the sinewave output also can be used to set symmetry of the TTL squarewave signals. Monitor the waveform on an oscilloscope to make the adjustment.

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Chapter 3: Programming

3.1 Introduction

This chapter describes the VME addressing of the Model 1480B and provides an example of source code to illustrate some programming approaches. Figure 3.1, below, shows a block diagram of the digital control section of the Model 1480B. From a programming point of view, the Model 1480B can be modeled as a group of memory-mapped registers. Two sets of registers are provided for each channel: the **Primary Frequency Register** and the **Secondary Frequency Register.**

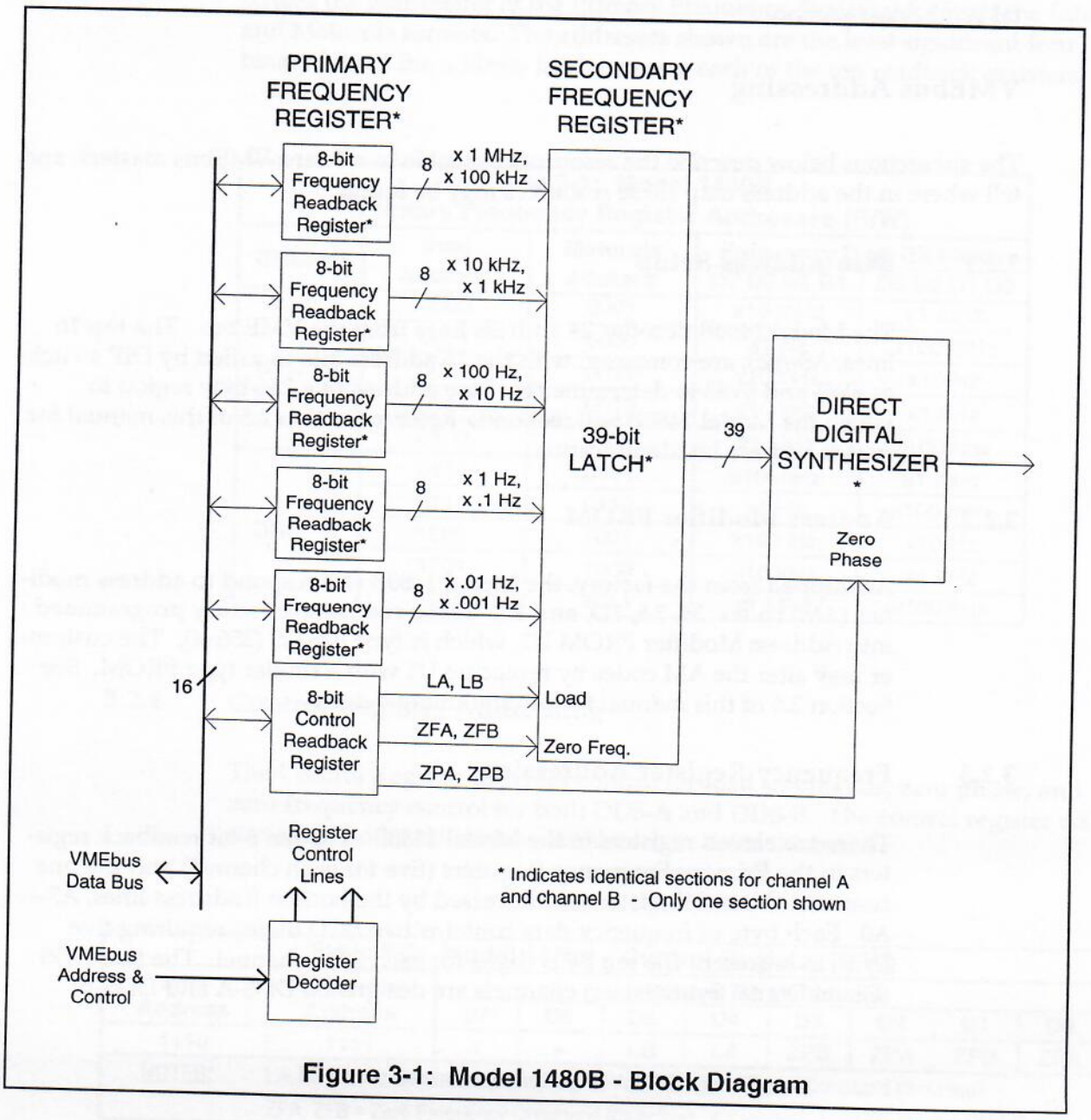


Figure 3-1: Model 1480B - Block Diagram

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