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OPERATING MANUAL

MODEL 4260

Wide/Fast/Differential SCSI-2
Controller MIX Module

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Manual Part No: 800.42600 Rev: B - April 25, 2000

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Pentek Model 4260 Operating Manual
Revision History

Date	Rev	Comments
November 15, 1996	A	Initial product release
June 19, 1997	A.1	Added 4285 MIX baseboard information.
April 25, 2000	B	Chapter 3; added default settings for each registers bitmap. Section 5.12 Corrected typo in formula, an " ~ " appeared instead of an "/" to indicate division. Section 2.3.1; corrected the model number for the Comm Port cable now states #2104, previously stated #2014. Added Appendix A; Symbios SYM53C770 SCSI I/O Processor With Ultra SCSI Manual. Added Appendix B; Texas Instruments TL16C550A Asynchronous Communications Element Manual.

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Appendix B: Texas Instruments TL16C550A Asynchronous Communications Element

B.1 Texas Instruments TL16C550A Asynchronous Communications Element Manual B-1

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Chapter 1: Overview

1.1 General Description

Pentek's Model 4260 is a high-performance SCSI-2 host adapter and RS-232 serial interface designed around the Intel MIX module specification. The Model 4260 is mountable on any of Pentek's VMEbus MIX baseboards, and occupies a single slot in the VMEbus card cage. Up to three Model 4260 modules may be stacked upon a single baseboard, or the 4260 may be used in conjunction with other MIX modules to provide a wide range of I/O solutions.

The Model 4260 is supported by Pentek's File Transfer Language, a software package that simplifies the process of streaming data between Pentek DSP and I/O peripherals. FTL includes a UNIX-like command-line interface, 'C' programming language and SPOX libraries that provide high-level access to supported Pentek devices, and a SCSI file system optimized for streaming. It is available for MS-DOS, Sun UNIX, and HP-UX platforms. For more details on using FTL with the Model 4260, refer to the ***FTL User's Guide***.

1.2 Using This Manual

This manual is divided into the following five chapters and three appendices:

Chapter 1 This chapter provides an overview of the Model 4260, including a block diagram and device specifications.

Chapter 2 This chapter covers Model 4260 configuration, installation, front panel connections, and cabling instructions.

Chapter 3 This chapter describes MIX resources available on the Model 4260. It includes a programming overview and information on using the Model 4260 with various Pentek baseboards.

Chapter 4 This chapter describes SIOP resources available on the Model 4260. For more information on the SYM53C770 SIOP, refer to the ***Symbios Logic SYM53C770 Data Manual*** and ***Programmer's Guide***.

Chapter 5 This chapter describes UART resources available on the Model 4260. For more information on the TL16C550A UART, refer to the ***Texas Instruments Data Transmission Circuits Data Book***.

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1.3 Block Diagram and Circuit Description

The Model 4260 (see block diagram below) features the Symbios Logic SYM53C770 SCSI I/O Processor (SIOP) for handling low level transactions with SCSI devices, thus relieving the MIX baseboard processor from what would be a significant computational load.

The RS-232C port on the Model 4260 allows asynchronous serial communications with terminal or modem devices, providing all of the required handshaking signals plus a programmable baud rate generator for a variety of communication system configurations.

A front panel 'C40 comm port provides a direct, bidirectional link between the Model 4260 and 'C40 comm port peripherals such as A/D and D/A converters, digital receivers, and TAXI adapters.

Local 256k x 32 dual-access SRAM provides efficient and convenient staging for input and output data. The SRAM appears as a memory-mapped resource to any MIX bus master, including all Pentek MIX baseboards and 'C40 DSP processor MIX modules.

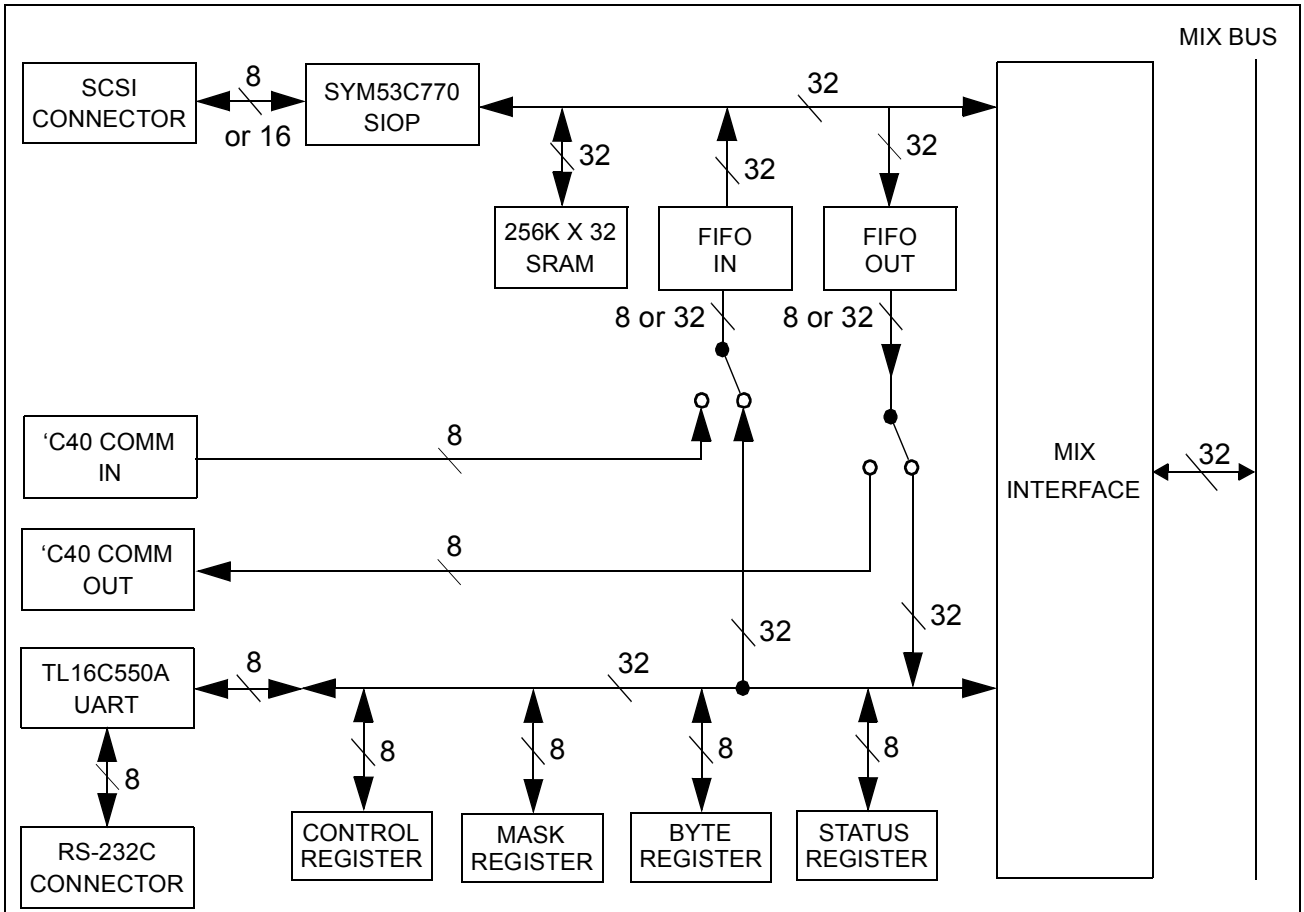


Figure 1-1: Model 4260 Block Diagram

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1.4 Specifications

SCSI-2 Interface	
Bus Width	8 bits Narrow/Fast
	16 bits Wide/Fast
SCSI Throughput:	
Narrow/Fast	10 MByte/sec.
Wide/Fast	20 MByte/sec.
Connectors:	Low Density/High Density
Block Size:	Variable
SCSI Processor	
Model:	Symbios Logic 53C770 intelligent controller
SCSI Core:	50 MByte/sec.
SCRIPTS Core:	RISC type, register based, 2 MIPS
DMA Core:	16-bit or 32-bit transfers, including misaligned 96B FIFO
RAM:	1k x 32 bits
Serial Interface	
UART Type	Texas Instruments TL16C550A
Baud Rate	Up to 38,400
Input Lines	SIN, RTS, DSR, RI
Output Lines	SOUT, DTR, CTS, DCD
Dual access SRAM	256k x 32 bits
MIX Interface	32 bit slave
Power Requirements	1.0A @+5VDC
(from MIX bus)	0.05A @ +12VDC
	0.05A @ -12VDC
Dimensions	
Height	10.3″
Depth	4.0″
Width	0.80″

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors and components. If you discover any damage, contact Pentek immediately at the phone number shown on the title page of this manual. Please save the original shipping container and packing material in case re-shipment is required.

2.2 Setting Jumper Configuration

Before installing the Model 4260, the unit must be configured for proper operation.

2.2.1 SCSI Termination

The SCSI bus must be terminated at both physical endpoints of the bus cable. Signal reflection and uneven loading of line drivers will result in bus failure if terminators are not present. Typically, one terminator will be placed on the host computer (initiator) and one on the last drive (target) in the chain.

SCSI termination is selected either by jumper settings (Options 001 through 003) or the placement of terminating resistors (Options 005 and 006) on the Model 4260 mezzanine board. Also selectable is whether or not the Model 4260 will provide termination power. Pages 15 through 19 provide more information. See Table 2-1 to find the page appropriate to your board.

Table 2-1: Model 4260 SCSI Configuration and Port Pin-Out

Option	Description	See Page
001	50-Pin Standard SCSI Connector, Single-Ended, 8-Bit	Page 15
002	50-Pin High Density SCSI Connector, Single-Ended, 8-Bit	Page 16
003	68-Pin High Density SCSI Connector, Single-Ended, 16-Bit	Page 17
005	50-Pin High Density SCSI Connector, Differential, 8-Bit	Page 18
006	68-Pin High Density SCSI Connector, Differential, 16-Bit	Page 19



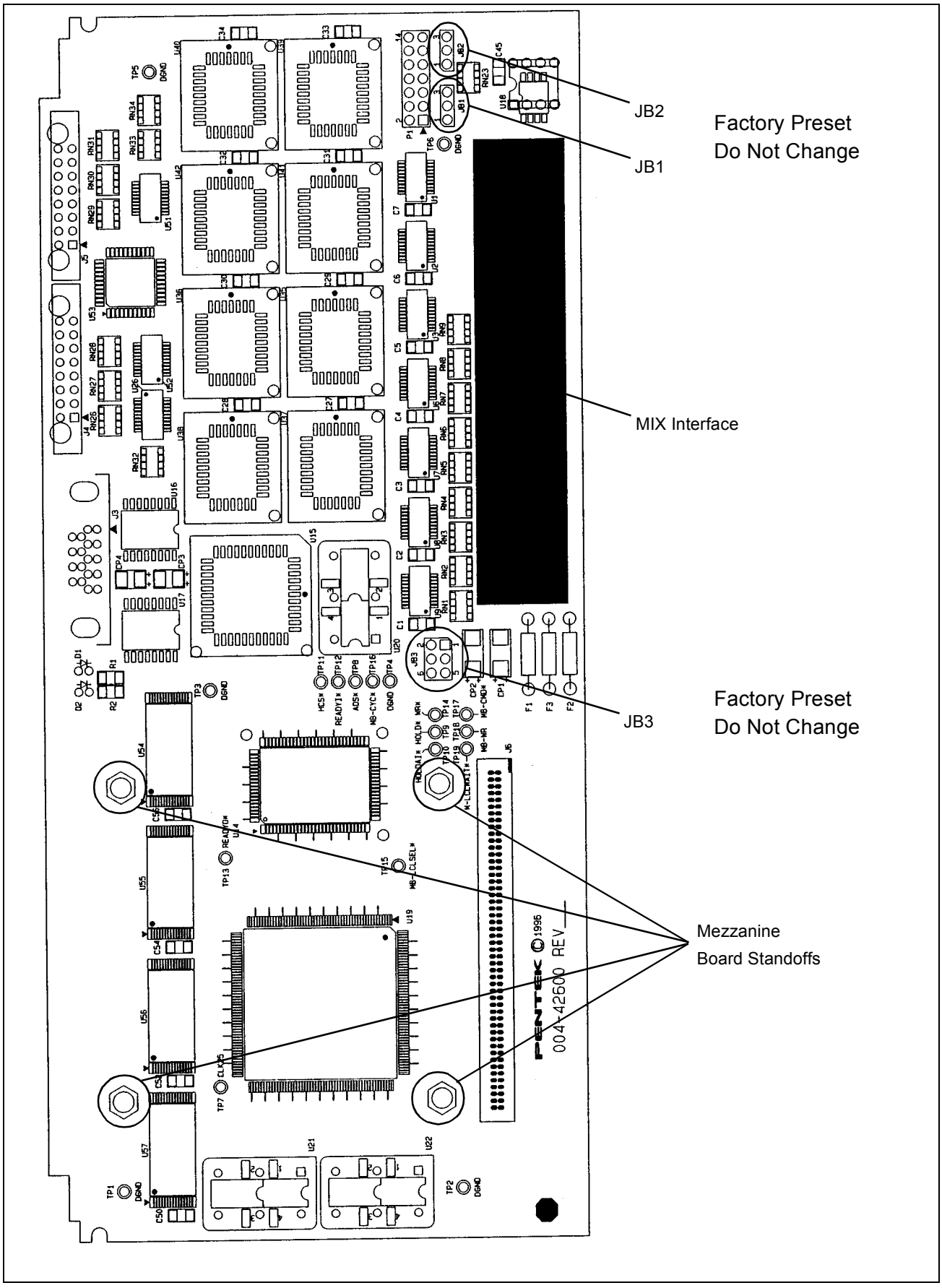
NOTE

Depending on the date of manufacture, the terminating resistors used by Model 4260 Options 005 and 006 may be in the form of Single In-Line Packages (SIP's) or Dual In-Line Packages (DIP's). Figure 2-5 illustrates SIP orientation, and Figure 2-6 illustrates DIP orientation.

2.2.2 MIX Module Jumpers

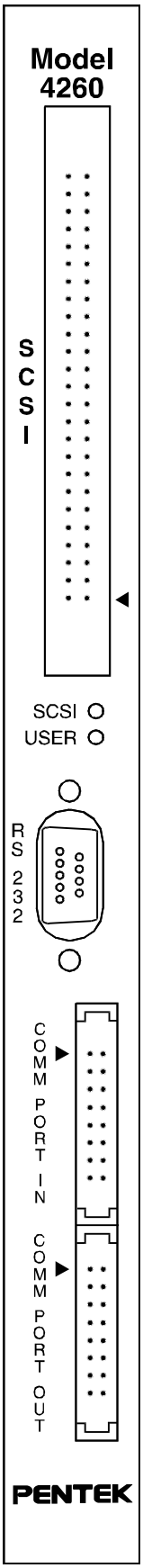
Jumper JB1, JB2, and JB3 on the Model 4260 MIX module are factory preset and should not be changed.

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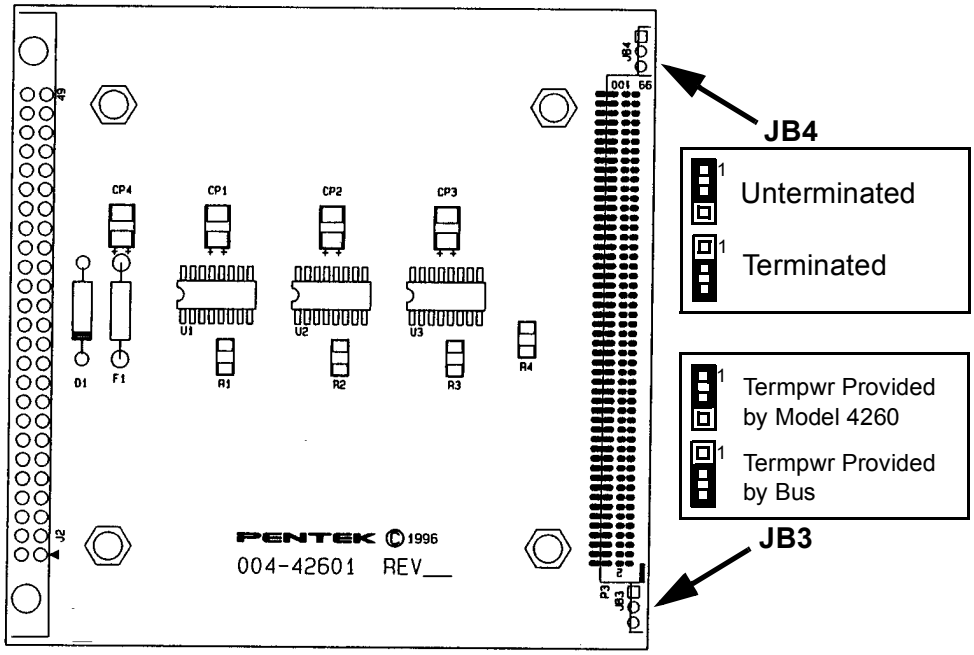
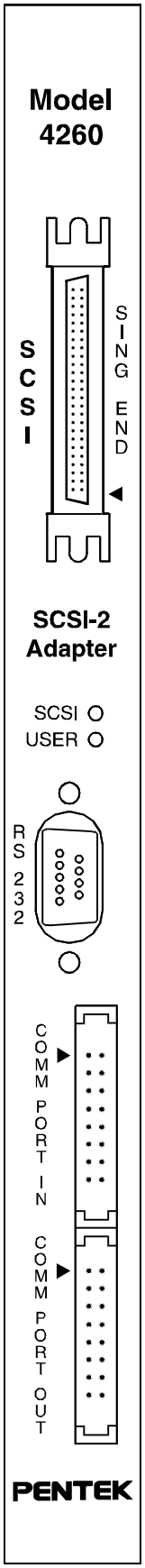


Table 2-2: Pin Assignments: 50-Pin Standard Single-Ended (8-bit)

Pin	Signal	Description	Pin	Signal	Description
50	-I/O	Input/Output (target)	49	GND	Ground
48	-REQ	Request bus transaction	47	GND	Ground
46	-C/D	Control/Data	45	GND	Ground
44	-SEL	Select (ID is on data lines)	43	GND	Ground
42	-MSG	Message	41	GND	Ground
40	-RST	Resets the bus (OR-tied)	39	GND	Ground
38	-ACK	Acknowledge	37	GND	Ground
36	-BSY	Bus is busy (OR-tied)	35	GND	Ground
34	GND	Ground	33	GND	Ground
32	-ATN	Attention (initiator driven)	31	GND	Ground
30	GND	Ground	29	GND	Ground
28	RES	Reserved	27	RES	Reserved
26	TERMPWR	Terminator power	25	OPEN	Open
24	RES	Reserved	23	RES	Reserved
22	GND	Ground	21	GND	Ground
20	GND	Ground	19	GND	Ground
18	-DB(P)	Data line: Odd Parity	17	GND	Ground
16	-DB(7)	Data line: bit 7	15	GND	Ground
14	-DB(6)	Data line: bit 6	13	GND	Ground
12	-DB(5)	Data line: bit 5	11	GND	Ground
10	-DB(4)	Data line: bit 4	9	GND	Ground
8	-DB(3)	Data line: bit 3	7	GND	Ground
6	-DB(2)	Data line: bit 2	5	GND	Ground
4	-DB(1)	Data line: bit 1	3	GND	Ground
2	-DB(0)	Data line: bit 0	1	GND	Ground

Figure 2-2: Model 4260 Option 001 - 50-Pin Standard Single-Ended, 8-Bit

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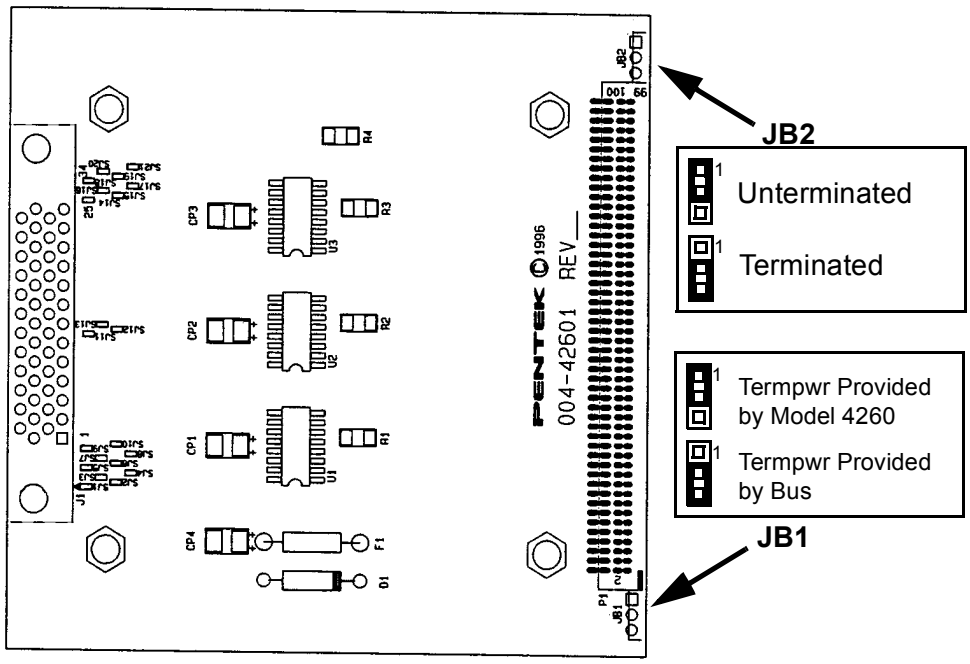
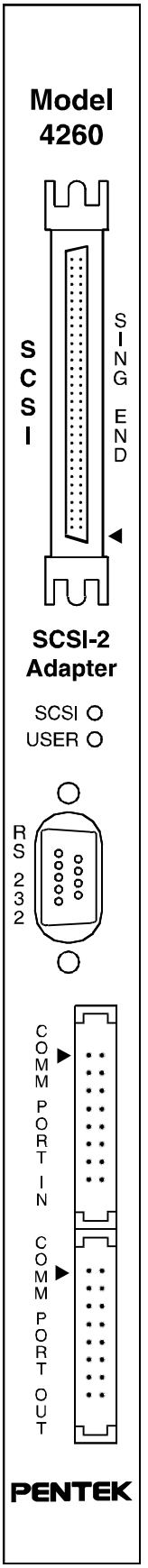


Table 2-3: Pin Assignments: 50-Pin High Density Single-Ended (8-bit)

Pin	Signal	Description	Pin	Signal	Description
50	-I/O	Input/Output (target)	49	GND	Ground
48	-REQ	Request bus transaction	47	GND	Ground
46	-C/D	Control/Data	45	GND	Ground
44	-SEL	Select (ID is on data lines)	43	GND	Ground
42	-MSG	Message	41	GND	Ground
40	-RST	Resets the bus (OR-tied)	39	GND	Ground
38	-ACK	Acknowledge	37	GND	Ground
36	-BSY	Bus is busy (OR-tied)	35	GND	Ground
34	GND	Ground	33	GND	Ground
32	-ATN	Attention (initiator driven)	31	GND	Ground
30	GND	Ground	29	GND	Ground
28	RES	Reserved	27	RES	Reserved
26	TERMPWR	Terminator power	25	OPEN	Open
24	RES	Reserved	23	RES	Reserved
22	GND	Ground	21	GND	Ground
20	GND	Ground	19	GND	Ground
18	-DB(P)	Data line: Odd Parity	17	GND	Ground
16	-DB(7)	Data line: bit 7	15	GND	Ground
14	-DB(6)	Data line: bit 6	13	GND	Ground
12	-DB(5)	Data line: bit 5	11	GND	Ground
10	-DB(4)	Data line: bit 4	9	GND	Ground
8	-DB(3)	Data line: bit 3	7	GND	Ground
6	-DB(2)	Data line: bit 2	5	GND	Ground
4	-DB(1)	Data line: bit 1	3	GND	Ground
2	-DB(0)	Data line: bit 0	1	GND	Ground

Figure 2-3: Model 4260 Option 002 - 50-Pin High Density Single-Ended, 8-Bit

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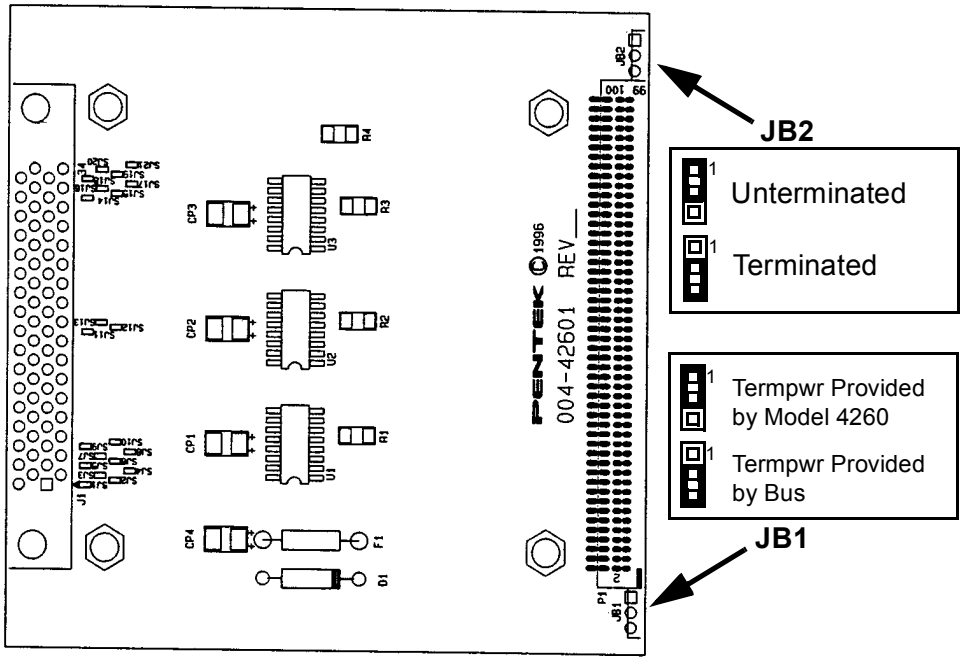
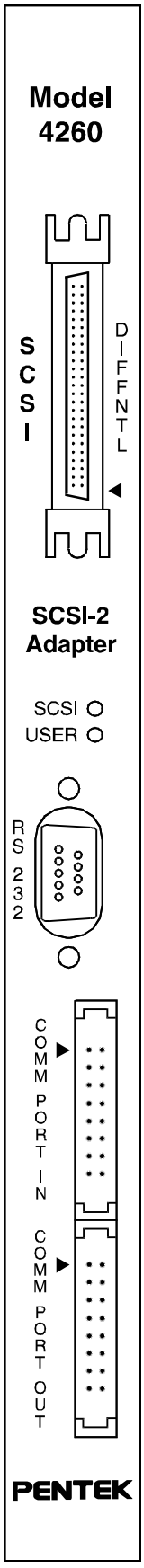


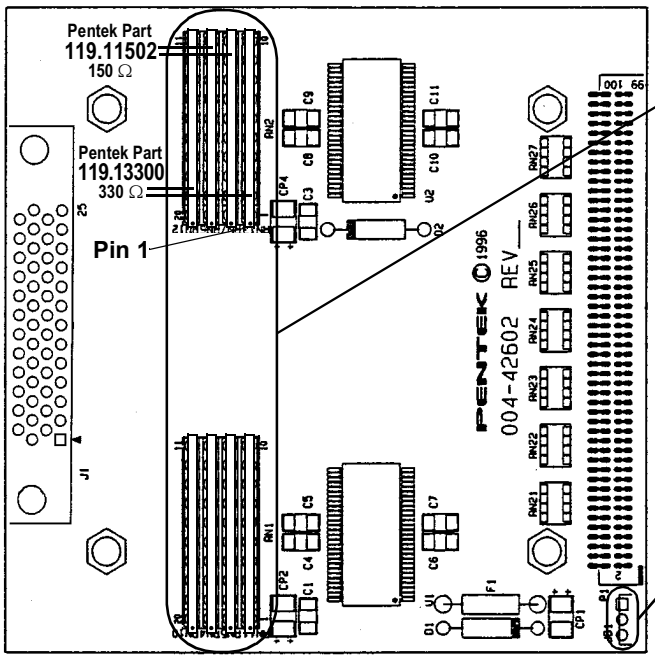
Table 2-4: Pin Assignments: 68-Pin High Density Single-Ended (16-bit)

Pin	Signal	Description	Pin	Signal	Description
68	-DB(11)	Data line: bit 11	67	GND	Ground
66	-DB(10)	Data line: bit 10	65	GND	Ground
64	-DB(9)	Data line: bit 9	63	GND	Ground
62	-DB(8)	Data line: bit 8	61	GND	Ground
60	-I/O	Input/Output (target)	59	GND	Ground
58	-REQ	Request bus transaction	57	GND	Ground
56	-C/D	Control/Data	55	GND	Ground
54	-SEL	Select (ID is on data lines)	53	GND	Ground
52	-MSG	Message	51	GND	Ground
50	-RST	Resets the bus (OR-tied)	49	GND	Ground
48	-ACK	Acknowledge	47	GND	Ground
46	-BSY	Bus is busy (OR-tied)	45	GND	Ground
44	GND	Ground	43	GND	Ground
42	-ATN	Attention (initiator driven)	41	GND	Ground
40	GND	Ground	39	GND	Ground
38	RES	Reserved	37	RES	Reserved
36	TERMPWR	Terminator power	35	TERMPWR	Terminator power
34	TERMPWR	Terminator power	33	TERMPWR	Terminator power
32	GND	Ground	31	GND	Ground
30	GND	Ground	29	GND	Ground
28	-DB(P)	Data line: Odd Parity	27	RES	Reserved
26	-DB(7)	Data line: bit 7	25	OPEN	Open
24	-DB(6)	Data line: bit 6	23	RES	Reserved
22	-DB(5)	Data line: bit 5	21	GND	Ground
20	-DB(4)	Data line: bit 4	19	GND	Ground
18	-DB(3)	Data line: bit 3	17	GND	Ground
16	-DB(2)	Data line: bit 2	15	GND	Ground
14	-DB(1)	Data line: bit 1	13	GND	Ground
12	-DB(0)	Data line: bit 0	11	GND	Ground
10	-DB(P1)	Data line: bit P1	9	GND	Ground
8	-DB(15)	Data line: bit 15	7	GND	Ground
6	-DB((14)	Data line: bit 14	5	GND	Ground
4	-DB(13)	Data line: bit 13	3	GND	Ground
2	-DB(12)	Data line: bit 12	1	GND	Ground

Figure 2-4: Model 4260 Option 003 - 68-Pin High Density Single-Ended, 16-Bit

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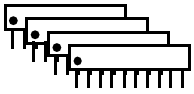


(Shown terminated by Single In-Line Resistors)

SCSI Termination

Resistors In: Terminated
Resistors Out: Unterminated

May be in the form of:



Single In-Line Resistors (8)

or:



Dual In-Line Resistors (2)



Termpwr Provided by Model 4260



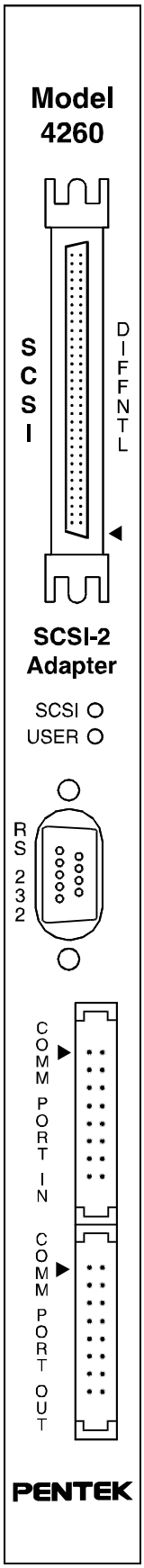
Termpwr Provided by Bus

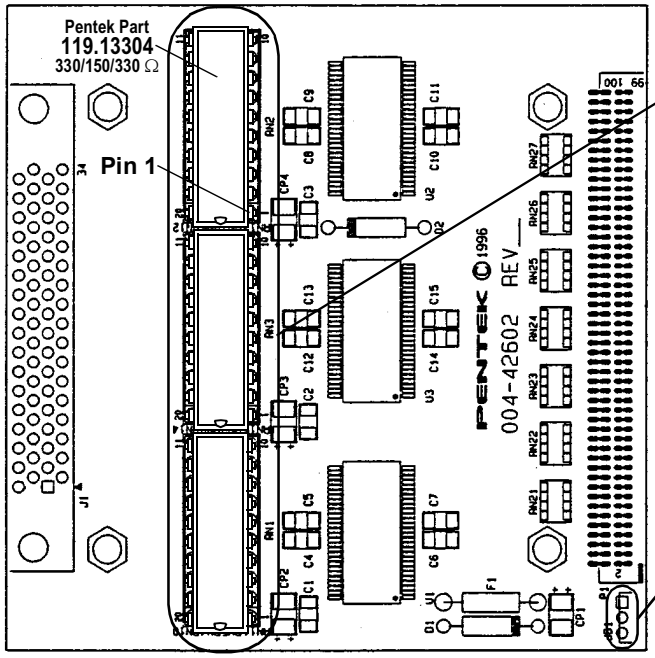
Table 2-5: Pin Assignments: 50-Pin High Density Differential (8-bit)

Pin	Signal	Description	Pin	Signal	Description
50	GND	Ground	49	GND	Ground
48	-I/O	Input/Output (target)	47	+I/O	Input/-Output (target)
46	-REQ	Request bus transaction	45	+REQ	Request bus transaction
44	-C/D	Control/Data	43	+C/D	Control/Data
42	-SEL	Select (ID is on data lines)	41	+SEL	Select (ID is on data lines)
40	-MSG	Message	39	+MSG	Message
38	-RST	Resets the bus (OR-tied)	37	+RST	Resets the bus (OR-tied)
36	-ACK	Acknowledge	35	+ACK	Acknowledge
34	-BSY	Bus is busy (OR-tied)	33	+BSY	Bus is busy (OR-tied)
32	GND	Ground	31	GND	Ground
30	-ATN	Attention (initiator driven)	29	+ATN	Attention (initiator driven)
28	RES	Reserved	27	RES	Reserved
26	TERMPWR	Terminator power	25	TERMPWR	Terminator power
24	RES	Reserved	23	RES	Reserved
22	GND	Ground	21	DIFSENS	Differential Sense
20	-DB(P)	Data line: Odd Parity	19	+DB(P)	Data line: Odd Parity
18	-DB(7)	Data line: bit 7	17	+DB(7)	Data line: bit 7
16	-DB(6)	Data line: bit 6	15	+DB(6)	Data line: bit 6
14	-DB(5)	Data line: bit 5	13	+DB(5)	Data line: bit 5
12	-DB(4)	Data line: bit 4	11	+DB(4)	Data line: bit 4
10	-DB(3)	Data line: bit 3	9	+DB(3)	Data line: bit 3
8	-DB(2)	Data line: bit 2	7	+DB(2)	Data line: bit 2
6	-DB(1)	Data line: bit 1	5	+DB(1)	Data line: bit 1
4	-DB(0)	Data line: bit 0	3	+DB(0)	Data line: bit 0
2	GND	Ground	1	GND	Ground

Figure 2-5: Model 4260 Option 005 - 50-Pin High Density Differential, 8 Bit

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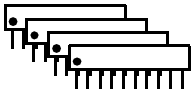


(Shown terminated by Dual In-Line Resistors)

SCSI Termination

Resistors In: Terminated
Resistors Out: Unterminated

May be in the form of:



Single In-Line Resistors (12)

or:



Dual In-Line Resistors (3)



1 Termpwr Provided by Model 4260

1 Termpwr Provided by Bus

Table 2-6: Pin Assignments: 68-Pin High Density Diffential (16-bit)

Pin	Signal	Description	Pin	Signal	Description
68	-DB(11)	Data line: bit 11	67	+DB(11)	Data line: bit 11
66	-DB(10)	Data line: bit 10	65	+DB(10)	Data line: bit 10
64	-DB(9)	Data line: bit 9	63	+DB(9)	Data line: bit 9
62	-DB(8)	Data line: bit 8	61	+DB(8)	Data line: bit 8
60	GND	Ground	59	GND	Ground
58	-I/O	Input/-Output (target)	57	+I/O	Input/-Output (target)
56	-REQ	Request bus transaction	55	+REQ	Request bus transaction
54	-C/D	Control/Data	53	+C/D	Control/Data
52	-SEL	Select (ID is on data lines)	51	+SEL	Select (ID is on data lines)
50	-MSG	Message	49	+MSG	Message
48	-RST	Resets the bus (OR-tied)	47	+RST	Resets the bus (OR-tied)
46	-ACK	Acknowledge	45	+ACK	Acknowledge
44	-BSY	Bus is busy (OR-tied)	43	+BSY	Bus is busy (OR-tied)
42	GND	Ground	41	GND	Ground
40	-ATN	Attention (initiator driven)	39	+ATN	Attention (initiator driven)
38	RES	Reserved	37	RES	Reserved
36	TERMPWR	Terminator power	35	TERMPWR	Terminator power
34	TERMPWR	Terminator power	33	TERMPWR	Terminator power
32	GND	Ground	31	DIFFSENS	Differential Sense
30	-DB(P)	Data line: Odd Parity	29	+DB(P)	Data line: Odd Parity
28	-DB(7)	Data line: bit 7	27	+DB(7)	Data line: bit 7
26	-DB(6)	Data line: bit 6	25	+DB(6)	Data line: bit 6
24	-DB(5)	Data line: bit 5	23	+DB(5)	Data line: bit 5
22	-DB(4)	Data line: bit 4	21	+DB(4)	Data line: bit 4
20	-DB(3)	Data line: bit 3	19	+DB(3)	Data line: bit 3
18	-DB(2)	Data line: bit 2	17	+DB(2)	Data line: bit 2
16	-DB(1)	Data line: bit 1	15	+DB(1)	Data line: bit 1
14	-DB(0)	Data line: bit 0	13	+DB(0)	Data line: bit 0
12	GND	Ground	11	GND	Ground
10	-DB(P1)	Data line: bit P1	9	+DB(P1)	Data line: bit P1
8	-DB(15)	Data line: bit 15	7	+DB(15)	Data line: bit 15
6	-DB(14)	Data line: bit 14	5	+DB(14)	Data line: bit 14
4	-DB(13)	Data line: bit 13	3	+DB(13)	Data line: bit 13
2	-DB(12)	Data line: bit 12	1	+DB(12)	Data line: bit 12

Figure 2-6: Model 4260 Option 006 - 68-Pin High Density Differential, 16-Bit

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2.3 Front Panel Connectors

2.3.1 'C40 Comm Port Interface

The Model 4260's front panel 'C40 comm port interface permits a direct, bidirectional link between the 4260 and Pentek 'C40 DSP boards or other 'C40 comm port peripherals. Data from these peripherals can be streamed directly to disk or tape.

To minimize excess cable length, cables can be assembled using a 3M hand press with locator plate #3443-110 and standard 16-conductor, 0.050 pitch flat ribbon cable such as 3M #3365/16.



NOTE

For consistency, make sure that pin 1 of each connector is connected to pin 1 of the ribbon cable. Pin 1 of the cable is identified by a colored stripe (see Figure 2-7).

Comm port cables are available pre-assembled from Pentek as Model 2104. Unterminated configurations accommodate cable lengths of up to 6". A series terminator board, mounted external to the 4260 (directly at the Comm Port connector), is also available as Model 2112, Option 024. With proper terminations at each end, cable lengths of up to 18" are accommodated.

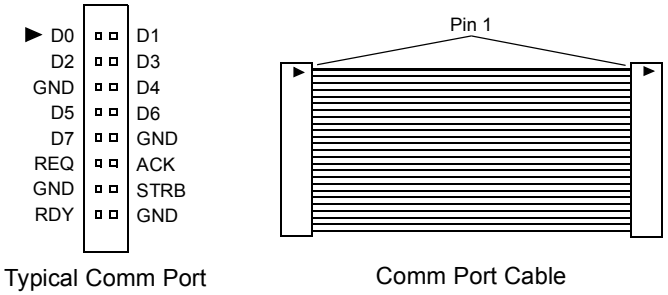
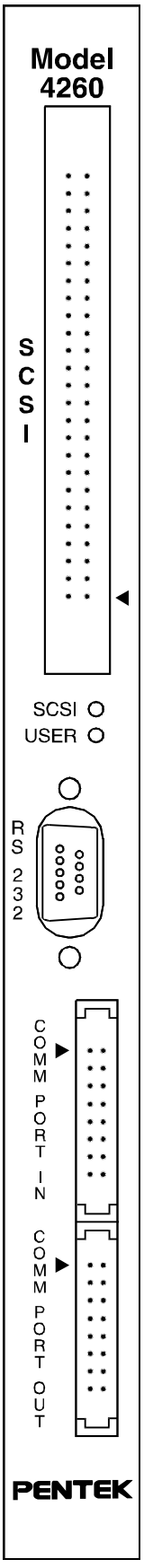


Figure 2-7: Comm Port Pin-Out





CAUTION

When two comm ports are cabled together, NEVER attempt to have both of them write simultaneously. This will cause SERIOUS DAMAGE to BOTH ports.

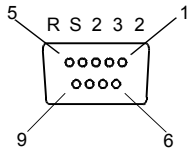
Also, it is recommended that all comm port cabling be completed BEFORE APPLYING POWER to the Model 4260.

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2.3 Front Panel Connectors (continued)

2.3.2 RS-232C Serial Port Interface

The RS-232C Port on the model 4260 allows asynchronous serial communications with terminal or modem devices, providing handshaking signals and a programmable baud rate generator. Figure 2-8 depicts the front panel RS-232C connector:



1	DCD	6	DSR
2	RD	7	RTS
3	TD	8	CTS
4	DTR	9	RI
5	GND		

Figure 2-8: RS-232C Port Orientation

2.3.3 SCSI Connector

Refer to pages 15 through 19 for SCSI port orientation and pin-out.

2.4 LED Indicators

2.4.1 SCSI LED Indicator

The **SCSI** LED is controlled by the Model 4260's SIOP, and is activated when the SIOP asserts SCSI $\overline{\text{BSY}}$. This LED is not user-programmable.



NOTE

When another device is master (drives BSY), the SCSI LED will not be lit even though the bus is active.

2.4.2 USER LED Indicator

The **USER** LED is user-programmable, and accessed by bit D6 of the Control Register as described in Section 3.4.2.

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2.5 Installing the Model 4260 on the MIX Baseboard

See Pentek's MIX Tutorial for VMEbus Systems (P/N 800.00001) for MIX module stack assembly instructions.

2.6 Installing the Assembly into the VMEbus Card Cage

Pentek's MIX Tutorial for VMEbus Systems (P/N 800.00001) also covers insertion of the assembled module stack in the card cage.

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Chapter 3: Memory Map and Control Registers

3.1 Programming Overview

The following sections cover access to the Model 4260 from the MIX Baseboard and the issuing of commands for control and data transfers. There are two cases to be considered, dependent upon the type of Baseboard used. This chapter gives details for Baseboards that use direct MIX addressing, such as Pentek's Models 4200, 4200A, 4201, 4201A, 4202, 4284, and 4285. General information on the use of these Baseboards is given in Pentek's MIX Tutorial for VMEbus Systems (P/N 800.00001). Pentek's MIX Tutorial also gives general information on access to the MIX modules from Baseboards that use an Address Page Register, such as Pentek's Model 4283. Memory Maps and addressing examples for the Model 4283 are also included in this chapter.

3.2 Address Maps

The sections below will present address maps for the resources available on the Model 4260 for each type of MIX Baseboard available from Pentek. Each of the resources will be assigned a symbolic address/name by which that resource will be referred to in subsequent sections of the manual. There are four cases to consider, each of which is covered in a separate section.

By convention, the MIX addresses given in this manual are generally given as 8-digit hexadecimal codes, with a space between the first and second four digits, simply for notional convenience. The form is MIX_base+0xYYYY ZZZZ. The leading '0x' is common notation for a hex value in the 'C' programming language.

Since each hex digit represents 4 bits, the 8-digit MIX address represents 32 bits of address. The MIX_base part of the address is dependent upon the Baseboard in use, and is used to select each module by its stack position. This geographical addressing scheme avoids the need for address jumpers and possible conflicts, but requires that software must accommodate the physical placement of modules in the MIX stack.

The exception to this convention will be for the Model 4283 Baseboard, whose TMS320C30 processor only has a 24-bit address bus on the port it uses for the MIX bus. In this case, a page register is used for module selection (as opposed to different base addresses for each module), and the addresses are given as 6-digit hexadecimal codes, in the form of 0xYY ZZZZ.

A final point must now be made about MIX nomenclature. Module 0 (or MIX position 0) refers to the closest module to the Baseboard, whether or not it is nested. Module 1 (or MIX position 1) is the device that may be mounted above Module 0, and Module 2 is the device that may be stacked upon Module 1.

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3.2 Address Maps (continued)

3.2.1 Using Model 4200/01 Series Baseboards

Pentek's Models 4200 and 4201 Baseboards use a 16 MHz 68030 processor as the MIX controller. The 4200A and 4201A use a 40 MHz 68030. From the 68030's viewpoint, the MIX bus is mapped identically for all four of these Baseboards. The MIX_base address for Module 0 (which may either be nested, sharing the Baseboard's VMEbus slot, or stacked in the adjacent VMEbus slot), is 0xC000 0000. For the next device in the stack, Module 1, the base address is 0xD000 0000. Finally, for the last MIX Module in the stack, Module 2, the MIX_base address is 0xE000 0000. Table 3-1 gives the physical addresses, in the memory space of the 68030 processor on any of these four baseboards, that correspond to the symbolic names used to represent the Model 4260's MIX resources in subsequent sections of the manual.

Table 3-1: Memory Map for Use with Model 4200, 4200A, 4201 and 4201A MIX Baseboards 68030 View

Resource/Name	4200/01 68030 Address	Access
Dual Access SRAM Base Address	MIX_base+0x0000 0000	Read/Write
Status Register	MIX_base+0x0800 0000	Read Only
Control Register	MIX_base+0x0800 0004	Read/Write
Byte Enable Register	MIX_base+0x0800 0008	Read/Write
Mask Interrupts Register	MIX_base+0x0800 000C	Read/Write
Reserved	MIX_base+0x0800 0010	N/A
Output FIFO	MIX_base+0x0800 0014	Read/Write
Input FIFO	MIX_base+0x0800 0018	Read/Write
UART Resources Base Address	MIX_base+0x0800 0020	See Chapter 5
SIOP Resources Base Address	MIX_base+0x0800 00E0	See Chapter 4

MIX_base Address:

If 4260 is in MIX position 0, MIX_base = 0xC000 0000
If 4260 is in MIX position 1, MIX_base = 0xD000 0000
If 4260 is in MIX position 2, MIX_base = 0xE000 0000

Note that the 4200 series of VME/MIX Baseboards also support mastering of the MIX bus by Upper MIX Bus Masters (UMBMs), and by VMEbus Masters. For further information about MIX Bus access on these Baseboards in this manner please refer to Pentek's MIX Tutorial for VMEbus Systems (P/N 800.00001) or to the Baseboard's or UMBM's Operating Manual.

3.2.2 Using the Model 4202 Baseboard

The Model 4202 is a VMEbus slave-only Baseboard, and contains no processor. This device maps the resources connected to its MIX Bus into VMEbus A32, A24, or A16 slave address space. The VMEbus A32 or A24 base address is programmed into a register in the 4202's A16 interface by a VMEbus Master (the A16 base address is set by switches on the board). This register is cleared at power-up, resulting in a default base address of 0x0000 0000 in A32 space, or 0x00 0000 in A24 space.

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3.2 Address Maps (continued)

3.2.2 Using the Model 4202 Baseboard (continued)

In direct accessing mode, the two most significant bits of the VMEbus address (i. e., A31 and A30 in A32 space, A23 and A22 in A24 space, or A15 and A14 in A16 space) select a particular 4202 Baseboard, by comparison with the two Least Significant Bits (D1 and D0) of the VMEbus Address Register. The next two VMEbus address bits (i. e., A29 and A28 in A32 space, A21 and A20 in A24 space, or A13 and A12 in A16 space) select among the MIX modules stacked on the 4202. Thus, assuming A32 operation and that the VMEbus Address Register is NOT written to, the MIX_base address for Module 0 is 0x0000 0000. Making the same assumptions, Module 1's MIX_base address is 0x1000 0000 and the MIX_base address for Module 2 is 0x2000 0000.

Table 3-2, below, presents the slave memory map for a Model 4260 installed on a Model 4202 Baseboard, assuming direct addressing, A32 or A24 operation, and that nothing has been written to the 4202's VME Address Register.

Table 3-2: Memory Map for Use with the Model 4202 MIX Baseboard

Resource/Name	VMEbus Address	Access
Dual Access SRAM Base Address	MIX_base+0x0000 0000	Read/Write
Status Register	MIX_base+0x0800 0000*	Read Only
Control Register	MIX_base+0x0800 0004*	Read/Write
Byte Enable Register	MIX_base+0x0800 0008*	Read/Write
Mask Interrupts Register	MIX_base+0x0800 000C*	Read/Write
Reserved	MIX_base+0x0800 0010*	N/A
Output FIFO	MIX_base+0x0800 0014*	Read/Write
Input FIFO	MIX_base+0x0800 0018*	Read/Write
UART Resources Base Address	MIX_base+0x0800 0020*	See Chapter 5
SIOP Resources Base Address	MIX_base+0x0800 00E0*	See Chapter 4

Default MIX_base Address:

If 4260 is in MIX position 0, MIX_base = 0x0000 0000 for A32, or 0x00 0000 for A24
If 4260 is in MIX position 1, MIX_base = 0x1000 0000 for A32, or 0x10 0000 for A24
If 4260 is in MIX position 2, MIX_base = 0x2000 0000 for A32, or 0x20 0000 for A24

*** - in A24 space, access at 0x08 0zzz**

3.2.3 Using the Model 4283 Baseboard

On the Model 4283 Baseboard, there are two levels of addressing: 1) selection of the particular expansion module by its stack position and 2) selection of one of the resources within the module.

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3.2 Address Maps (continued)

3.2.3 Using the Model 4283 Baseboard (continued)

3.2.3.1 Module Selection

The TMS320C30 selects among MIX Modules by using a two bit field in the Model 4283 Page Register, located at address 0x80 0002 in the TMS320C30 address space. These two bits select one of the three possible MIX stack positions according to Table 3-3 below.

Table 3-3: Module Selection - Model 4283 Page Register 'C30 Address 0x80 0002

Page Register Bits>	D31-D18	D17	D16	D15	D14	D13-D0	Example
Stack Position 0	x	MXA27	1	1	MXA21	x	0x01 8000
Stack Position 1	x		1	0		x	0x01 0000
Stack Position 2	x		0	1		x	0x00 8000
x = other functions							

3.2.3.2 Register Selection Within the Module

One the module has been selected, all resources (including the FIFO's) of the Model 4260 appear in the TMS320C30 address map according to Table 3-4. Accessing these registers is accomplished by simply reading and writing these locations.

The 24-bit addressing scheme accesses 32-bit data locations for the TMS320C30, even though many elements correspond to 8-bit or 16-bit devices.

Table 3-4: Memory Map for Use with the Model 4283 MIX Baseboard

Resource/Name	4283 'C30 Address	Access
Dual Access SRAM Base Address	0x80 4000*	Read/Write
Status Register	0x80 4000	Read Only
Control Register	0x80 4001	Read/Write
Byte Enable Register	0x80 4002	Read/Write
Mask Interrupts Register	0x80 4003	Read/Write
Reserved	0x80 4004	N/A
Output FIFO	0x80 4005	Read/Write
Input FIFO	0x80 4006	Read/Write
UART Resources Base Address	0x80 4008	See Chapter 5
SIOP Resources Base Address	0x80 4080	See Chapter 4

*To access the shared memory, MXA27 must be driven low.
To access the Model 4260's registers, MXA27 must be driven high by setting bit 17 in the Model 4283's Page Address Register.

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3.2 Address Maps (continued)

3.2.4 Using the Model 4284 Baseboard

The Model 4284 Baseboard uses a TMS320C40 Digital Signal Processor to master transactions with the MIX bus. The three MIX module locations are each mapped into separate, 64 M-Longword regions of the 'C40's memory space. Module 0's MIX_base address in the 'C40 memory map is 0x2000 0000. The MIX_base address for Module 1 is 0x2400 0000, and the 'C40's MIX_base address for Module 2 is 0x2800 0000. Table 3-5 presents the memory map for the MIX resources on the Model 4260, as seen by the 'C40 processor on the Model 4284 Baseboard.

Table 3-5: Memory Map for Use with the Model 4284 MIX Baseboard

Resource/Name	4284 'C40 Address	Access
Dual Access SRAM Base Address	MIX_base+0x0000 0000	Read/Write
Status Register	MIX_base+0x0200 0000	Read Only
Control Register	MIX_base+0x0200 0001	Read/Write
Byte Enable Register	MIX_base+0x0200 0002	Read/Write
Mask Interrupts Register	MIX_base+0x0200 0003	Read/Write
Reserved	MIX_base+0x0200 0004	N/A
Output FIFO	MIX_base+0x0200 0005	Read/Write
Input FIFO	MIX_base+0x0200 0006	Read/Write
UART Resources Base Address	MIX_base+0x0200 0008	See Chapter 5
SIOP Resources Base Address	MIX_base+0x0200 0080	See Chapter 4

MIX_base Address:
If 4260 is in MIX position 0, MIX_base = 0x2000 0000
If 4260 is in MIX position 1, MIX_base = 0x2400 0000
If 4260 is in MIX position 2, MIX_base = 0x2800 0000

This Baseboard also supports mastering of the MIX bus by processor modules in the MIX stack, known as UMBM's (Upper MIX Bus Masters). For further details on this type of transaction, please refer to Pentek's MIX Tutorial for VMEbus Systems (P/N 800.00001), the Model 4284 Operating Manual, or the UMBM's Operating Manual.

3.2.5 Using the Model 4285 Baseboard

When the Model 4285 is equipped with one of the MIX Expansion Bus Adapters (Options 031 or 036) all eight of its 'C40 processors can access modules on the MIX bus via the 4285's Main Bus. Additionally, four of the processors (A, B, E and F) have a separate access path to devices on the MIX bus via their Global I/O expansion ports. Separate control registers are provided for each of these five interfaces to the MIX bus. Two addressing modes, Normal and Compressed, are available for any of these access paths.

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3.2 Address Maps (continued)

3.2.5 Using the Model 4285 Baseboard (continued)

The control registers mentioned above each provide a 5-bit address page field. For this Baseboard, however, the page setting is NOT used to determine which MIX module is being addressed (i. e., the direct addressing method is used). The mapping of the page field onto the address bus is a function of the selected addressing mode. For complete details, refer to the Operating Manual for the Model 4285. For purposes of this operation summary, we will say that in Normal Addressing Mode, page bit 2 is used to assert the MXA27 address bit, while in Compressed Mode, MXA27 is asserted by 'C40 Global Address bit GA20.

Table 3-6, below, presents the memory map for the slave resources on the Model 4260, as seen by the 'C40 processors on the Model 4285 Baseboard. The table also provides the MIX_Base addresses, in the memory spaces of the 'C40 processors, for the Expansion bus and Global I/O access paths. For further information on the use of the 4285 as a MIX baseboard, including VME access to MIX resources on the 4285, please refer to Section 3.4 of the 4285 Operating Manual.

Table 3-6: Memory Map for Use with the Model 4285 MIX Baseboard

4285 'C40 Address	Symbolic Name	Resource
Dual Access SRAM Base Address	MIX_base+0x0000 0000	Read/Write
Status Register	MIX_base+0x0200 0000	Read Only
Control Register	MIX_base+0x0200 0001	Read/Write
Byte Enable Register	MIX_base+0x0200 0002	Read/Write
Mask Interrupts Register	MIX_base+0x0200 0003	Read/Write
Reserved	MIX_base+0x0200 0004	N/A
Output FIFO	MIX_base+0x0200 0005	Read/Write
Input FIFO	MIX_base+0x0200 0006	Read/Write
UART Resources Base Address	MIX_base+0x0200 0008	See Chapter 5
SIOP Resources Base Address	MIX_base+0x0200 0080	See Chapter 4

MIX_base Address for Expansion Bus:

If Model 4260 is in MIX position 0, MIX_base = 0x9000 0000
If Model 4260 is in MIX position 1, MIX_base = 0x9020 0000
If Model 4260 is in MIX position 2, MIX_base = 0x9040 0000

MIX_base Address for Global I/O Bus:

If Model 4260 is in MIX position 0, MIX_base = 0xC800 0000
If Model 4260 is in MIX position 1, MIX_base = 0xC820 0000
If Model 4260 is in MIX position 2, MIX_base = 0xC840 0000

NOTE: MXA27 is asserted via page bit 2 in Normal addressing mode, or via 'C40 address bit GA20 in Compressed addressing mode

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3.3 Status Register

The Status Register (see Table 3-7) is used to read FIFO conditions and the interrupt status of the SIOP and UART. This register is accessed at an address dependent upon the type of baseboard used and the MIX stack position of the Model 4260. All bits of the Status Register are cleared to logic '0' on power up. These bits reflect the current state of a FIFO or Service Request and are not cleared when read.

This read-only register uses only the bottom 8 bits of the 32-bit word from the MIX bus. When reading the Status Register, bits 8 through 31 are indeterminate and should be ignored.

Table 3-7: Model 4260 - Status Register - Read Only

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	FIFO Out Full	FIFO Out Half Full	FIFO Out Empty	FIFO In Full	FIFO In Half Full	FIFO In Empty	UART Service Request	SIOP Service Request
Bit Definition	1 = true 0 = false	1 = true 0 = false	1 = true 0 = false	1 = true 0 = false	1 = true 0 = false	1 = true 0 = false	1 = true 0 = false	1 = true 0 = false
The default setting for Status Register bits D0 through D7 is '0' (false).								

3.3.1 FIFO Full - Bits D7 (Input FIFO) and D4 (Output FIFO)

This bit reflects the current state of the FIFO Full flag. When this bit is set to the logic '1' (true) state, the FIFO is full. When this bit is cleared to the logic '0' (false) state, the FIFO is not full. This bit can be used to insure that data reads from the FIFO for the entire FIFO depth are allowed.

3.3.2 FIFO Half Full - Bits D6 (Input FIFO) and D3 (Output FIFO)

This bit reflects the current state of the FIFO Half Full flag. When this bit is set to the logic '1' (true) state, the FIFO is at least half full. When this bit is cleared to logic '0' (false) state, the FIFO is less than half full. This bit can be used to insure that a data read cycle from the FIFO for up to half the FIFO depth is allowed.

3.3.3 FIFO Empty - Bits D5 (Input FIFO) and D2 (Output FIFO)

This bit reflects the current state of the FIFO Empty flag. When set to the logic '1' (true) state, the FIFO is empty. When this bit is cleared to the logic '0' (false) state, there is data in the FIFO. This bit insures that a data read from the FIFO is allowed.

3.3.4 UART Service Request - Bit D1

This bit reflects the current state of the UART Interrupt flag. When this bit is set to logic '1' (true), the UART is requesting service.

3.3.5 SIOP Service Request - Bit D0

This bit reflects the current state of the SIOP Interrupt flag. When this bit is set to logic '1' (true), the SIOP is requesting service.

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3.4 Control Register

The Control Register (see Table 3-8) is used to control the operation of the Model 4260's FIFOs. The register is accessed at an address dependent upon the type of baseboard used and the MIX stack position of the Model 4260.

This register is a read/write device that uses only the bottom 8 bits of the 32-bit word from the MIX bus. When writing to the Control Register, data in bit positions 8 through 31 will have no effect. When reading from the Control Register address, bits 0 through 7 will reflect the contents of the Control Register, and bits 8 through 31 will be indeterminate and should be ignored.

Table 3-8: Model 4260 - Control Register - Read/Write

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	Reserved	LED (User)	Reserved	Bus Off (Release SIOP bus)	FIFO Out Reset*	FIFO In Reset*	UART Reset*	SIOP Reset*
Bit Definition	Always Write '0'	0=LED Off 1=LED On	Always Write '0'	'1' = True '0' = False	logic '0' = True logic '1' = False			

The default setting for Control Register bits D0 through D7 is '0'.

3.4.1 Reserved - Bit D7

This bit is reserved, and should always be cleared to the '0' state.

3.4.2 User LED Indicator Driver - Bit D6

The User LED Indicator on the Model 4260's front panel is turned on when this bit is in the '1' state. To turn the LED off, clear this bit to the '0' state.

3.4.3 Reserved - Bit 5

This bit is reserved, and should always be cleared to the '0' state.

3.4.4 Bus Off - Bit D4

Setting this bit to the logic '1' state (true) causes the SIOP to finish its cycle and remain off the bus until the bit is cleared to logic '0'.

3.4.5 Reset - Bits D3 - D0

Clearing bit D3 or D2 to the logic '0' state will reset the output FIFO or input FIFO respectively. Resetting a FIFO flushes all data and clears all condition flags.

Clearing bit D1 or D0 to the logic '0' state will reset the UART and SIOP respectively. On reset, all register values are returned to their power-on defaults.

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3.5 Byte Enable Register

This register is a read/write device that uses only the bottom 8 bits of the 32-bit word from the MIX bus. When writing to the Byte Enable Register address, data in bit positions 8 through 31 will have no effect. When reading from the Byte Enable Register address, bits 0 through 7 will reflect the contents of the Byte Enable Register, and bits 8 through 31 will be indeterminate and should be ignored.

Table 3-9: Model 4260 - Byte Enable Register - Read/Write

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	Invert Int on Out FIFO's Empty Flag	Invert Int on In FIFO's Full Flag	Comm Out Enable	Comm In Enable	MIX Byte Enable 3*	MIX Byte Enable 2*	MIX Byte Enable 1*	MIX Byte Enable 0*
Bit Definition	'0' = False (Normal) '1' = True (Inverted)		'0' = False (MIX bus) '1' = True (Comm)		'0' = True (Byte Lane Enabled) '1' = False (Byte Lane Disabled)			

The default setting for Byte Enable Register bits D0 through D7 is '0'.

3.5.1 MIX Byte Enables - Bits D0 - D3

These four bits allow a byte sent over the MIX bus to be justified in one of the four byte positions on the 32 bit data bus, or a word to be justified in either of two positions. Only one of these four bits should be in the low state for byte transfers, two should be low for word transfers, and all four are low for Longword transactions.

When the 4260 is powered on, these bits are all set low, which enables Longword exchanges. This default configuration is the setting you will want for almost all MIX bus transactions. Table 3-10, below, describes the relationship between which byte enable bits are activated (i.e., low) and which bits of the MIX data bus will be used in a given data exchange.

Table 3-10: Model 4260 - MIX Bus Byte Enables and Data Bus Usage

Transfer Type	Cycle # (Note 1)	Byte Enable Signals				Data Bus Utilization				Physical Address		Comment
		MXBE3*	MXBE2*	MXBE1*	MXBE0*	D31-D24	D23-D16	D15-D8	D7-D0	A1	A0	
32-bit	-	L	L	L	L	m	n	k	l	0	0	Single Cycle
32-bit	1	H	H	L	L	X	X	k	l	0	0	1 word +
2 cycle	2	L	L	H	H	X	X	m	n	1	0	1 word
24-bit	-	H	L	L	L	X	m	n	l	0	0	Single Cycle
24-bit	-	L	L	L	H	m	n	l	X	0	1	Single Cycle
24-bit	1	H	L	L	L	X	X	n	l	0	0	1 word +
2 cycle	2	H	L	H	H	X	X	X	m	1	0	1 byte
24-bit	1	L	L	L	H	X	X	l	X	0	1	1 byte +
2 cycle	2	L	L	H	H	X	X	m	l	1	0	1 word
16-bit	-	H	H	L	L	X	X	m	l	0	0	Single Cycle
16-bit	-	L	L	H	H	X	X	m	l	1	0	Single Cycle
16-bit	1	H	L	L	H	X	X	l	X	0	1	2 bytes =
2 cycle	2	H	L	H	H	X	X	X	m	1	0	1 word
8-bit	-	H	H	H	L	X	X	X	l	0	0	Single Cycle
8-bit	-	H	H	L	H	X	X	l	X	0	0	Single Cycle
8-bit	-	H	L	H	H	X	X	X	l	1	0	Single Cycle
8-bit	-	L	H	H	H	X	X	l	X	1	1	Single Cycle

NOTES: (1) Cycle # indicates the order in which multiple MIX cycles MUST be run.
(2) X = no byte, m = most significant byte, n = next more significant byte, k = next less significant byte, l = least significant byte
(3) For Pentek MIX modules, use the 32-bit single cycle setting, which is the default.

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3.5 Byte Enable Register (continued)

3.5.2 Comm In Enable - Bit D4

When this bit is cleared to the '0' state, data enters the input FIFO from the comm in port. When this bit is set to the '1' state, data enters the input FIFO directly from the MIX bus. This bit defaults to the logic '0' state on reset.

When changing this bit, it is generally a good idea to reset the corresponding FIFO (Bit D2 of the Control Register).

3.5.3 Comm Out Enable - Bit D5

When this bit is cleared to the '0' state, data moves from the output FIFO to the comm out port. When this bit is set to the '1' state, data moves from the output FIFO directly to the MIX bus. This bit defaults to the logic '0' state on reset.

When changing this bit, it is generally a good idea to reset the corresponding FIFO (Bit D3 of the Control Register).

3.5.4 Invert Interrupt on Input FIFO Full Flag - Bit D6

When bit D6 of the Byte Enable Register is cleared to logic '0' (false), an interrupt occurs when the Input FIFO Full Flag of the Status Register changes from logic '1' to logic '0' (when the FIFO becomes NOT full). When bit D6 is set to logic '1' (true), an interrupt occurs when the FIFO's Full flag changes from logic '0' to logic '1' (when the FIFO becomes Full).

3.5.5 Invert Interrupt on Output FIFO Empty Flag - Bit D7

When bit D7 of the Byte Enable Register is cleared to logic '0' (false), an interrupt occurs when the Output FIFO Empty Flag of the Status Register changes from logic '1' to logic '0' (when the FIFO receives data and becomes NOT empty). When bit D7 is set to logic '1' (true), an interrupt occurs when the FIFO's Empty flag changes from logic '0' to logic '1' (when the FIFO becomes empty).

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3.6 Interrupt Mask Register

These bits are used to establish the conditions for generating an interrupt to the MIX bus. For each bit set to logic '1' state, a MIX bus interrupt will be generated when the corresponding condition occurs. Clearing all bits to the logic '0' state will disable all interrupt generation.

This register is a read/write device that uses only the bottom 8 bits of the 32-bit word from the MIX bus. When writing to the Interrupt Mask Register, data in bit positions 8 through 31 will have no effect. When reading from the Interrupt Mask Register address, bits 0 through 7 will reflect the contents of the Interrupt Mask Register, and bits 8 through 31 will be indeterminate and should be ignored.

Table 3-11: Model 4260 - Interrupt Mask Bits - Read/Write

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	FIFO Out Full*	FIFO Out Half Full*	FIFO Out Not Empty*	FIFO In Not Full*	FIFO In Not Half Full*	FIFO In Empty*	UART*	SIOP*
Bit Definition	logic '0' = Interrupts Masked logic '1' = Interrupts Enabled							

The default setting for Interrupt Mask bits D0 through D7 is '0' (Interrupts Masked).

3.6.1 FIFO Out Full Interrupt Mask - Bits D7

When the output FIFO becomes full, the FIFO Out Full Flag of the Status Register changes from false (logic '0') to true (logic '1'). This event can be used to generate an interrupt on the MIX bus by setting the FIFO Out Full Interrupt Mask bit to the logic '1' state. If the mask bit is set to logic '1' when the FIFO is already full, an interrupt will be generated immediately.

3.6.2 FIFO Out Half Full Interrupt Mask - Bits D6

When the output FIFO becomes half (or more) full, the FIFO Out Half Full Flag of the Status Register changes from false (logic '0') to true (logic '1'). This event can be used to generate an interrupt on the MIX bus by setting the FIFO Out Half Full Interrupt Mask bit to the logic '1' state. If the mask bit is set to logic '1' when the FIFO is already half (or more) full, an interrupt will be generated immediately. This is the interrupt normally used for real-time operation.

3.6.3 FIFO Out Not Empty Interrupt Mask - Bits D5

When the first data enters the output FIFO, the FIFO Out Empty Flag of the Status Register changes from true (logic '1') to false (logic '0'). This event can be used to generated an interrupt on the MIX bus by setting the FIFO Empty Interrupt Mask bit to the logic '1' state. If the mask bit is set to logic '1' when the FIFO is already not empty, an interrupt will be generated immediately. This is the used for low data rates where each data element is to be processed immediately.



NOTE

When bit D7 of the Byte Enable Register is set to logic '1' (true), an interrupt will occur when the Input FIFO becomes empty.

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3.6 Interrupt Mask Register (continued)

3.6.4 FIFO In Not Full Interrupt Mask - Bits D4

When the input FIFO is not full, the FIFO In Full Flag of the Status Register changes from true (logic '1') to true (logic '0'). This event can be used to generate an interrupt on the MIX bus by setting the FIFO Full Interrupt Mask bit to the logic '1' state. If the mask bit is set to logic '1' when the FIFO is already not full, an interrupt will be generated immediately.



NOTE

When bit D6 of the Byte Enable Register is set to logic '1' (true), an interrupt will occur when the Input FIFO becomes full.

3.6.5 FIFO In Not Half Full Interrupt Mask - Bits D3

When the input FIFO becomes less than half full, the FIFO In Half Full Flag of the Status Register changes from true (logic '1') to true (logic '0'). This event can be used to generate an interrupt on the MIX bus by setting the FIFO Half Full Interrupt Mask bit to the logic '1' state. If the mask bit is set to logic '1' when the FIFO is already less than half full, an interrupt will be generated immediately.

3.6.6 FIFO In Empty Interrupt Mask - Bits D2

When the input FIFO becomes empty, the FIFO In Empty Flag of the Status Register changes from false (logic '0') to true (logic '1'). This event can be used to generated an interrupt on the MIX bus by setting the FIFO Empty Interrupt Mask bit to the logic '1' state. If the mask bit is set to logic '1' when the FIFO is already empty, an interrupt will be generated immediately.

3.6.7 UART and SIOP Interrupt Mask - Bits D1 and D0

These bits allow UART and SIOP service requests to generate MIX interrupts.

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Chapter 4: SYM53C770 Registers

4.1 General Information

This chapter, which contains information found in the ***SYM53C770 Data Manual,*** describes the SYM53C770 register set. Address maps for each Pentek MIX baseboard are provided in the beginning of this chapter. The sections that follow describe each register in detail. For more information on accessing these registers, see Chapter 3 and Pentek's MIX Tutorial for VMEbus Systems (P/N 800.00001). For more information on the Symbios SYM53C770 SCSI I/O Processor With Ultra SCSI Manual see Appendix A.

Throughout this section, the terms "set" and "assert" are used to refer to bits that are programmed to a binary one. Similarly, the terms "deassert," "clear," and "reset" are used to refer to bits that are programmed to a binary zero. Reserved bits should always be written to zero; mask all information read from them. Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active high; the feature is enabled by setting the bit. The bottom of every register diagram shows the default register values, which are enabled after the chip is powered on or reset. Registers can be addressed as bytes, words or longwords. Other access sizes will result in bus errors.



NOTE

The only register that the host CPU can access while the SYM53C770 is executing SCRIPTS is the ISTAT register; attempts to access other registers will interfere with the operation of the chip. However, all registers are accessible via SCRIPTS.

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4.1 General Information (continued)

4.1.1 Using Model 4200, 4200A, 4201 and 4201A MIX Baseboards

Table 4-1 gives the physical addresses, in the memory space of the 68030 processor on any of these four Baseboards, that correspond to the symbolic names used to represent the Model 4260's SIOP resources in subsequent sections of the manual.

Table 4-1: Memory Map of SIOP Resources - Model 4200, 4200A, 4201, 4201A MIX Baseboards

Resource/Name	Symbolic Name	4200/01 68030 Address	Access
Internal Memory	RAM	MIX_base+0x0800 1000 to MIX_base+0x0800 13FF	Read/Write
SCSI Control 0 Register	SCNTL0	MIX_base+0x0800 00E0	Read/Write
SCSI Chip ID Register	SCID	MIX_base+0x0800 00E4	Read/Write
SCSI First Byte Received Register	SFBR	MIX_base+0x0800 00E8	Read/Write
DMA Status Register	DSTAT	MIX_base+0x0800 00EC	Read Only
DMA Status Register	DSA	MIX_base+0x0800 00F0	Read/Write
Interrupt Status Register	ISTAT	MIX_base+0x0800 00F4	Read/Write
Chip Test Zero Register	CTEST0	MIX_base+0x0800 00F8	Read/Write
Temporary Stack Registers	TEMP	MIX_base+0x0800 00FC	Read/Write
DMA FIFO Register	DFIFO	MIX_base+0x0800 0100	Read/Write
DMA Byte Counter Registers	DBC	MIX_base+0x0800 0104	Read/Write
DMA Next Data Address Registers	DNAD	MIX_base+0x0800 0108	Read/Write
DMA Scripts Pointer Registers	DSP	MIX_base+0x0800 010C	Read/Write
DMA Scripts Pointer Save Registers	DSPS	MIX_base+0x0800 0110	Read/Write
Scratch Register A	SCRATCHA	MIX_base+0x0800 0114	Read/Write
DMA Mode Register	DMODE	MIX_base+0x0800 0118	Read/Write
Adder Sum Output Register	ADDER	MIX_base+0x0800 011C	Read Only
SCSI Interrupt Enable Zero Register	SIEN0	MIX_base+0x0800 0120	Read/Write
SCSI Longitudinal Parity Register	SLPAR	MIX_base+0x0800 0124	Read/Write
SCSI Timer Register 0	STIME0	MIX_base+0x0800 0128	Read/Write
SCSI Test Register 0	STEST0	MIX_base+0x0800 012C	Read/Write
SCSI Input Data Latch Register	SIDL	MIX_base+0x0800 0130	Read Only
SCSI Output Data Latch Register	SODL	MIX_base+0x0800 0134	Read/Write
SCSI Bus Data Lines Register	SBDL	MIX_base+0x0800 0138	Read Only
Scratch Register B	SCRATCHB	MIX_base+0x0800 013C	Read/Write
Scratch Register C	SCRATCHC	MIX_base+0x0800 0140	Read/Write
Scratch Register D	SCRATCHD	MIX_base+0x0800 0144	Read/Write
Scratch Register E	SCRATCHE	MIX_base+0x0800 0148	Read/Write
Scratch Register F	SCRATCHF	MIX_base+0x0800 014C	Read/Write
Scratch Register G	SCRATCHG	MIX_base+0x0800 0150	Read/Write
Scratch Register H	SCRATCHH	MIX_base+0x0800 0154	Read/Write
Scratch Register I	SCRATCHI	MIX_base+0x0800 0158	Read/Write
Scratch Register J	SCRATCHJ	MIX_base+0x0800 015C	Read/Write

MIX_base Address:
If 4260 is in MIX position 0, MIX_base = 0xC000 0000
If 4260 is in MIX position 1, MIX_base = 0xD000 0000
If 4260 is in MIX position 2, MIX_base = 0xE000 0000

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4.1 General Information (continued)

4.1.2 Using the Model 4202 Baseboard

Table 4-2, below, presents the slave memory map of SIOP resources for a Model 4260 installed on a Model 4202 Baseboard, assuming direct addressing, A32 or A24 operation, and that nothing has been written to the 4202's VME Address Register.

Table 4-2: Memory Map of SIOP Resources - Model 4202 MIX Baseboard

Resource/Name	Symbolic Name	VMEbus Address*	Access
Internal Memory	RAM	MIX_base+0x0800 1000 to MIX_base+0x0800 13FF	Read/Write
SCSI Control 0 Register	SCNTL0	MIX_base+0x0800 00E0	Read/Write
SCSI Chip ID Register	SCID	MIX_base+0x0800 00E4	Read/Write
SCSI First Byte Received Register	SFBR	MIX_base+0x0800 00E8	Read/Write
DMA Status Register	DSTAT	MIX_base+0x0800 00EC	Read Only
DMA Status Register	DSA	MIX_base+0x0800 00F0	Read/Write
Interrupt Status Register	ISTAT	MIX_base+0x0800 00F4	Read/Write
Chip Test Zero Register	CTEST0	MIX_base+0x0800 00F8	Read/Write
Temporary Stack Registers	TEMP	MIX_base+0x0800 00FC	Read/Write
DMA FIFO Register	DFIFO	MIX_base+0x0800 0100	Read/Write
DMA Byte Counter Registers	DBC	MIX_base+0x0800 0104	Read/Write
DMA Next Data Address Registers	DNAD	MIX_base+0x0800 0108	Read/Write
DMA Scripts Pointer Registers	DSP	MIX_base+0x0800 010C	Read/Write
DMA Scripts Pointer Save Registers	DSPS	MIX_base+0x0800 0110	Read/Write
Scratch Register A	SCRATCHA	MIX_base+0x0800 0114	Read/Write
DMA Mode Register	DMODE	MIX_base+0x0800 0118	Read/Write
Adder Sum Output Register	ADDER	MIX_base+0x0800 011C	Read Only
SCSI Interrupt Enable Zero Register	SIEN0	MIX_base+0x0800 0120	Read/Write
SCSI Longitudinal Parity Register	SLPAR	MIX_base+0x0800 0124	Read/Write
SCSI Timer Register 0	STIME0	MIX_base+0x0800 0128	Read/Write
SCSI Test Register 0	STEST0	MIX_base+0x0800 012C	Read/Write
SCSI Input Data Latch Register	SIDL	MIX_base+0x0800 0130	Read Only
SCSI Output Data Latch Register	SODL	MIX_base+0x0800 0134	Read/Write
SCSI Bus Data Lines Register	SBDL	MIX_base+0x0800 0138	Read Only
Scratch Register B	SCRATCHB	MIX_base+0x0800 013C	Read/Write
Scratch Register C	SCRATCHC	MIX_base+0x0800 0140	Read/Write
Scratch Register D	SCRATCHD	MIX_base+0x0800 0144	Read/Write
Scratch Register E	SCRATCHE	MIX_base+0x0800 0148	Read/Write
Scratch Register F	SCRATCHF	MIX_base+0x0800 014C	Read/Write
Scratch Register G	SCRATCHG	MIX_base+0x0800 0150	Read/Write
Scratch Register H	SCRATCHH	MIX_base+0x0800 0154	Read/Write
Scratch Register I	SCRATCHI	MIX_base+0x0800 0158	Read/Write
Scratch Register J	SCRATCHJ	MIX_base+0x0800 015C	Read/Write

Default MIX_base Address:

If 4260 is in MIX position 0, MIX_base = 0x0000 0000 for A32, or 0x00 0000 for A24
If 4260 is in MIX position 1, MIX_base = 0x1000 0000 for A32, or 0x10 0000 for A24
If 4260 is in MIX position 2, MIX_base = 0x2000 0000 for A32, or 0x20 0000 for A24

*** - in A24 space, access at 0x08 0zzz**

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4.1 General Information (continued)

4.1.3 Using the Model 4283 MIX Baseboard

Once the module has been selected, as described in Chapter 3, all SIOP resources of the Model 4260 appear in the TMS320C30 address map according to Table 4-3. Accessing these registers is accomplished by simply reading and writing these locations.

Table 4-3: Memory Map of SIOP Resources - Model 4283 MIX Baseboard

Resource/Name	Symbolic Name	4283 'C30 Address	Access
Internal Memory	RAM	0x80 4400 to 0x80 44FF	Read/Write
SCSI Control 0 Register	SCNTL0	0x80 4080	Read/Write
SCSI Chip ID Register	SCID	0x80 4081	Read/Write
SCSI First Byte Received Register	SFBR	0x80 4082	Read/Write
DMA Status Register	DSTAT	0x80 4083	Read Only
DMA Status Register	DSA	0x80 4084	Read/Write
Interrupt Status Register	ISTAT	0x80 4085	Read/Write
Chip Test Zero Register	CTEST0	0x80 4086	Read/Write
Temporary Stack Registers	TEMP	0x80 4087	Read/Write
DMA FIFO Register	DFIFO	0x80 4088	Read/Write
DMA Byte Counter Registers	DBC	0x80 4089	Read/Write
DMA Next Data Address Registers	DNAD	0x80 408A	Read/Write
DMA Scripts Pointer Registers	DSP	0x80 408B	Read/Write
DMA Scripts Pointer Save Registers	DSPS	0x80 408C	Read/Write
Scratch Register A	SCRATCHA	0x80 408D	Read/Write
DMA Mode Register	DMODE	0x80 408E	Read/Write
Adder Sum Output Register	ADDER	0x80 408F	Read Only
SCSI Interrupt Enable Zero Register	SIEN0	0x80 4090	Read/Write
SCSI Longitudinal Parity Register	SLPAR	0x80 4091	Read/Write
SCSI Timer Register 0	STIME0	0x80 4092	Read/Write
SCSI Test Register 0	STEST0	0x80 4093	Read/Write
SCSI Input Data Latch Register	SIDL	0x80 4094	Read Only
SCSI Output Data Latch Register	SODL	0x80 4095	Read/Write
SCSI Bus Data Lines Register	SBDL	0x80 4096	Read Only
Scratch Register B	SCRATCHB	0x80 4097	Read/Write
Scratch Register C	SCRATCHC	0x80 4098	Read/Write
Scratch Register D	SCRATCHD	0x80 4099	Read/Write
Scratch Register E	SCRATCHE	0x80 409A	Read/Write
Scratch Register F	SCRATCHF	0x80 409B	Read/Write
Scratch Register G	SCRATCHG	0x80 409C	Read/Write
Scratch Register H	SCRATCHH	0x80 409D	Read/Write
Scratch Register I	SCRATCHI	0x80 409E	Read/Write
Scratch Register J	SCRATCHJ	0x80 409F	Read/Write
To access the Model 4260's registers, MXA27 must be driven high by setting bit 17 in the Model 4283's Page Address Register.			

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4.1 General Information (continued)

4.1.4 Using the Model 4284 MIX Baseboard

Table 4-4 presents the memory map for SIOP resources on the Model 4260, as seen by the 'C40 processor on the Model 4284 Baseboard.

Table 4-4: Memory Map of SIOP Resources - Model 4284 MIX Baseboard

Resource/Name	Symbolic Name	4284 'C40 Address	Access
Internal Memory	RAM	MIX_base+0x0200 0000 to MIX_base+0x0203 FFFF	Read/Write
SCSI Control 0 Register	SCNTL0	MIX_base+0x0200 0080	Read/Write
SCSI Chip ID Register	SCID	MIX_base+0x0200 0081	Read/Write
SCSI First Byte Received Register	SFBR	MIX_base+0x0200 0082	Read/Write
DMA Status Register	DSTAT	MIX_base+0x0200 0083	Read Only
DMA Status Register	DSA	MIX_base+0x0200 0084	Read/Write
Interrupt Status Register	ISTAT	MIX_base+0x0200 0085	Read/Write
Chip Test Zero Register	CTEST0	MIX_base+0x0200 0086	Read/Write
Temporary Stack Registers	TEMP	MIX_base+0x0200 0087	Read/Write
DMA FIFO Register	DFIFO	MIX_base+0x0200 0088	Read/Write
DMA Byte Counter Registers	DBC	MIX_base+0x0200 0089	Read/Write
DMA Next Data Address Registers	DNAD	MIX_base+0x0200 008A	Read/Write
DMA Scripts Pointer Registers	DSP	MIX_base+0x0200 008B	Read/Write
DMA Scripts Pointer Save Registers	DSPS	MIX_base+0x0200 008C	Read/Write
Scratch Register A	SCRATCHA	MIX_base+0x0200 008D	Read/Write
DMA Mode Register	DMODE	MIX_base+0x0200 008E	Read/Write
Adder Sum Output Register	ADDER	MIX_base+0x0200 008F	Read Only
SCSI Interrupt Enable Zero Register	SIEN0	MIX_base+0x0200 0090	Read/Write
SCSI Longitudinal Parity Register	SLPAR	MIX_base+0x0200 0091	Read/Write
SCSI Timer Register 0	STIME0	MIX_base+0x0200 0092	Read/Write
SCSI Test Register 0	STEST0	MIX_base+0x0200 0093	Read/Write
SCSI Input Data Latch Register	SIDL	MIX_base+0x0200 0094	Read Only
SCSI Output Data Latch Register	SODL	MIX_base+0x0200 0095	Read/Write
SCSI Bus Data Lines Register	SBDL	MIX_base+0x0200 0096	Read Only
Scratch Register B	SCRATCHB	MIX_base+0x0200 0097	Read/Write
Scratch Register C	SCRATCHC	MIX_base+0x0200 0098	Read/Write
Scratch Register D	SCRATCHD	MIX_base+0x0200 0099	Read/Write
Scratch Register E	SCRATCHE	MIX_base+0x0200 009A	Read/Write
Scratch Register F	SCRATCHF	MIX_base+0x0200 009B	Read/Write
Scratch Register G	SCRATCHG	MIX_base+0x0200 009C	Read/Write
Scratch Register H	SCRATCHH	MIX_base+0x0200 009D	Read/Write
Scratch Register I	SCRATCHI	MIX_base+0x0200 009E	Read/Write
Scratch Register J	SCRATCHJ	MIX_base+0x0200 009F	Read/Write

MIX_base Address:
If 4260 is in MIX position 0, MIX_base = 0x2000 0000
If 4260 is in MIX position 1, MIX_base = 0x2400 0000
If 4260 is in MIX position 2, MIX_base = 0x2800 0000

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4.1 General Information (continued)

4.1.5 Using the Model 4285 MIX Baseboard

Table 4-5 presents the memory map for SIOP resources on the Model 4260, as seen by the 'C40 processor on the Model 4285 Baseboard.

Table 4-5: Memory Map of SIOP Resources - Model 4285 MIX Baseboard

Resource/Name	Symbolic Name	4285 'C40 Address	Access
Internal Memory	RAM	MIX_base+0x0200 0000 to MIX_base+0x0203 FFFF	Read/Write
SCSI Control 0 Register	SCNTL0	MIX_base+0x0200 0080	Read/Write
SCSI Chip ID Register	SCID	MIX_base+0x0200 0081	Read/Write
SCSI First Byte Received Register	SFBR	MIX_base+0x0200 0082	Read/Write
DMA Status Register	DSTAT	MIX_base+0x0200 0083	Read Only
DMA Status Register	DSA	MIX_base+0x0200 0084	Read/Write
Interrupt Status Register	ISTAT	MIX_base+0x0200 0085	Read/Write
Chip Test Zero Register	CTEST0	MIX_base+0x0200 0086	Read/Write
Temporary Stack Registers	TEMP	MIX_base+0x0200 0087	Read/Write
DMA FIFO Register	DFIFO	MIX_base+0x0200 0088	Read/Write
DMA Byte Counter Registers	DBC	MIX_base+0x0200 0089	Read/Write
DMA Next Data Address Registers	DNAD	MIX_base+0x0200 008A	Read/Write
DMA Scripts Pointer Registers	DSP	MIX_base+0x0200 008B	Read/Write
DMA Scripts Pointer Save Registers	DSPS	MIX_base+0x0200 008C	Read/Write
Scratch Register A	SCRATCHA	MIX_base+0x0200 008D	Read/Write
DMA Mode Register	DMODE	MIX_base+0x0200 008E	Read/Write
Adder Sum Output Register	ADDER	MIX_base+0x0200 008F	Read Only
SCSI Interrupt Enable Zero Register	SIEN0	MIX_base+0x0200 0090	Read/Write
SCSI Longitudinal Parity Register	SLPAR	MIX_base+0x0200 0091	Read/Write
SCSI Timer Register 0	STIME0	MIX_base+0x0200 0092	Read/Write
SCSI Test Register 0	STEST0	MIX_base+0x0200 0093	Read/Write
SCSI Input Data Latch Register	SIDL	MIX_base+0x0200 0094	Read Only
SCSI Output Data Latch Register	SODL	MIX_base+0x0200 0095	Read/Write
SCSI Bus Data Lines Register	SBDL	MIX_base+0x0200 0096	Read Only
Scratch Register B	SCRATCHB	MIX_base+0x0200 0097	Read/Write
Scratch Register C	SCRATCHC	MIX_base+0x0200 0098	Read/Write
Scratch Register D	SCRATCHD	MIX_base+0x0200 0099	Read/Write
Scratch Register E	SCRATCHE	MIX_base+0x0200 009A	Read/Write
Scratch Register F	SCRATCHF	MIX_base+0x0200 009B	Read/Write
Scratch Register G	SCRATCHG	MIX_base+0x0200 009C	Read/Write
Scratch Register H	SCRATCHH	MIX_base+0x0200 009D	Read/Write
Scratch Register I	SCRATCHI	MIX_base+0x0200 009E	Read/Write
Scratch Register J	SCRATCHJ	MIX_base+0x0200 009F	Read/Write

MIX_base Address for Expansion Bus:
If Model 4260 is in MIX position 0, MIX_base = 0x9000 0000
If Model 4260 is in MIX position 1, MIX_base = 0x9020 0000
If Model 4260 is in MIX position 2, MIX_base = 0x9040 0000

MIX_base Address for Global I/O Bus:
If Model 4260 is in MIX position 0, MIX_base = 0xC800 0000
If Model 4260 is in MIX position 1, MIX_base = 0xC820 0000
If Model 4260 is in MIX position 2, MIX_base = 0xC840 0000

NOTE: MXA27 is asserted via page bit 2 in Normal addressing mode, or via 'C40 address bit GA20 in Compressed addressing mode

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4.2 SCSI Control Zero Register (SCNTL0)

SCSI Control Zero Register (SCNTL0) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	ARB1	ARB0	START	$\overline{\text{WATN}}$	EPC	EPG	AP	TRG
Default	1	1	0	0	0	0	0	0

4.2.1 Bit 7 & 6 - ARB1 & ARB0

These two bits select the Arbitration Mode.

Table 4-6: Arbitration Mode		
ARB1	**ARB0**	**Arbitration Mode**
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection or reselection

Simple Arbitration:

1) The SYM53C770 waits for a bus free condition to occur.

2) It asserts $\overline{\text{BSY}}$ and its SCSI ID (contained in the SCID register) onto the SCSI bus. If the $\overline{\text{SEL}}$ signal is asserted by another SCSI device, the SYM53C770 will deassert $\overline{\text{BSY}}$, deassert its ID and set the Lost Arbitration bit (bit 3) in the SSTAT0 register.

3) After an arbitration delay, the CPU should read the SBDL register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the SYM53C770 has won arbitration.

4) Once the SYM53C770 has won arbitration, it must assert SEL via the SOCL register for a bus clear plus a bus settle delay (1.2 µs). A low level selection can be performed after this delay.

Full Arbitration, Selection/Reselection:

1) The SYM53C770 waits for a bus free condition.

2) It asserts $\overline{\text{BSY}}$ and its SCSI ID (the ID stored in the SCID register) onto the SCSI bus.

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4.2 SCSI Control Zero Register (SCNTL0) (continued)

4.2.1 Bit 7 & 6 - ARB1 & ARB0 (continued)

3) If the $\overline{\text{SEL}}$ signal is asserted by another SCSI device or if the SYM53C770 detects a higher priority ID, the SYM53C770 will deassert $\overline{\text{BSY}}$, deassert its ID, and wait until the next bus free state to try arbitration again.

4) The SYM53C770 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the SSTAT0 register, bit 2.

5) The SYM53C770 performs selection by asserting the following onto the SCSI bus: $\overline{\text{SEL}}$, the target's ID (stored in the SDID register) and the SYM53C770's ID (the highest priority ID stored in the SCID register).

6) After a selection is complete, the Function Complete bit is set in the SIST0 register, bit 6.

7) If a selection time-out occurs, the Selection Time-out bit is set in the SIST1 register, bit 2.

4.2.2 Bit 5 - START (Start sequence)

When this bit is set, the SYM53C770 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is used in low level mode; when executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor. An arbitration sequence should not be started if the Connected bit, bit 4 in the SCNTL1 register, indicates that SYM53C770 is already connected to the SCSI bus.

This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, bit 4 in the SCNTL1 register should be checked to verify that the SYM53C770 did not connect to the SCSI bus.

4.2.3 Bit 4 - WATN (Select with $\overline{\text{ATN}}$ on a start sequence)

When this bit is set and the SYM53C770 is in initiator mode, the SCSI $\overline{\text{ATN}}$ signal will be asserted during SYM53C770 selection of a target device. This is to inform the target that the SYM53C770 has a message to send. If a selection time-out occurs while attempting to select a target device, $\overline{\text{ATN}}$ will be deasserted at the same time $\overline{\text{SEL}}$ is deasserted.

When this bit is clear, the $\overline{\text{ATN}}$ signal will not be asserted during selection.

This bit is controlled by the SCRIPTS processor during SCRIPTS execution, but it may be set manually in low level mode.

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4.2 SCSI Control Zero Register (SCNTL0) (continued)

4.2.3 Bit 4 - WATN (Select with ATN on a start sequence) (continued)

When this bit is set, the SYM53C770 checks the SCSI data bus for odd parity when data is received from the SCSI bus in either initiator or target mode. It also checks the host data bus for odd parity if bit 2, the Enable Parity Generation bit, is cleared. Host data bus parity is checked as data is loaded into the SODL register when sending SCSI data in either initiator or target mode. If a parity error is detected, bit 0 of the SSTAT0 register is set and an interrupt may be generated.

4.2.4 Bit 3 - EPC (Enable parity checking)

If the SYM53C770 is operating in initiator mode and a parity error is detected, it may assert $\overline{\text{ATN}}$, but the transfer continues until the target changes phase.

When this bit is cleared, parity errors are not reported.

4.2.5 Bit 2 - EPG (Enable parity generation/parity through)

When this bit is set, the SYM53C770 generates SCSI parity. The host data bus parity lines DP(3-0) are ignored and should not be used as parity signals. When this bit is cleared, the parity present on the host data parity lines flows through the SYM53C770's internal FIFOs and is driven onto the SCSI bus when sending data (if the host bus is set to even parity, it is changed to odd before it is sent to the SCSI bus).

This bit enables the DP3 $\overline{\text{ABRT}}$ pin to function as an abort input ($\overline{\text{ABRT}}$).

4.2.6 Bit 1 - AAP (Assert $\overline{\text{ATN}}$ on parity error)

When this bit is set, the SYM53C770 automatically asserts the SCSI $\overline{\text{ATN}}$ signal when it detects a parity error. $\overline{\text{ATN}}$ is only asserted in initiator mode. The $\overline{\text{ATN}}$ signal is asserted before deasserting $\overline{\text{ACK}}$ during the transfer of the byte with the parity error.

The Enable Parity Checking bit must also be set for the SYM53C770 to assert $\overline{\text{ATN}}$ in this manner. The following parity errors can occur:

1) A parity error detected on data received from the SCSI bus.

2) A parity error detected on data transferred to the SYM53C770 from the host data bus.

If the Assert $\overline{\text{ATN}}$ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, $\overline{\text{ATN}}$ will not be automatically asserted on the SCSI bus when a parity error is received.

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4.2 SCSI Control Zero Register (SCNTL0) (continued)

4.2.7 Bit 0 - TRG (Target mode)

This bit determines the default operating mode of the SYM53C770. The user must manually set target or initiator mode. This can be done using the SCRIPTS language (SET target or CLEAR target). When this bit is set, the chip is a target device by default. When the target mode bit is cleared, the SYM53C770 is an initiator device by default.

NOTE: Writing this bit while not connected may cause the loss of a selection or reselection due to the changing of target or initiator roles.

4.3 SCSI Control One Register (SCNTL1)

SCSI Control One Register (SCNTL1) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	EXC	ADB	DHP	CON	RST	AESP	IARB	SST
Default	0	0	0	0	0	0	0	0

4.3.1 Bit 7 - EXC (Extra clock cycle of data setup)

When this bit is set, an extra clock period of data setup is added to each SCSI send data transfer. The extra data setup time can provide additional system design margin, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time.

4.3.2 Bit 6 - ADB (Assert SCSI data bus)

When this bit is set, the SYM53C770 drives the contents of the SCSI Output Data Latch register (SODL) onto the SCSI data bus. When the SYM53C770 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus.

The low order data and parity signal will always be asserted onto the SCSI bus, whereas the high-order data and parity signal will only be asserted onto the SCSI bus if the Enable Wide SCSI bit (SCNTL3, bit 3) is asserted and a data phase is specified by the SCSI phase signals. When the SYM53C770 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the SYM53C770 is connected to the SCSI bus.

This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low level mode.

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4.3 SCSI Control One Register (SCNTL1) (continued)

4.3.3 Bit 5 - DHP (Disable Halt on Parity Error or ATN) (Target Only)

The DHP bit is only defined for target mode operation. When this bit is cleared, the SYM53C770 halts the SCSI data transfer when a parity error is detected or when the $\overline{\text{ATN}}$ signal is asserted. If $\overline{\text{ATN}}$ or a parity error is received in the middle of a data transfer, the SYM53C770 may transfer up to three additional bytes (or words, if wide SCSI is enabled) before halting to synchronize between internal core cells. During synchronous operation, the SYM53C770 will halt when there are no more outstanding synchronous offsets. If the SYM53C770 is receiving data, any data residing in the SCSI or DMA FIFOs is sent to memory before halting. While sending data in target mode with pass parity enabled, the byte with the parity error will not be sent across the SCSI bus.

When this bit is set, the SYM53C770 does not halt the SCSI transfer when $\overline{\text{ATN}}$ or a parity error is received.

4.3.4 Bit 4 - CON (Connected)

This bit is automatically set any time the SYM53C770 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the SYM53C770 has responded to a bus initiated selection or reselection. It will also be set after successfully completing simple arbitration when operating in low level mode. When this bit is clear, the SYM53C770 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

4.3.5 Bit 3 - RST (Assert SCSI $\overline{\text{RST}}$ signal)

Setting this bit asserts the SCSI $\overline{\text{RST}}$ signal. The $\overline{\text{RST}}$ output remains asserted until this bit is cleared. The 25 μs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor.

In differential mode, $\overline{\text{RST}}$ becomes an input, and setting this bit causes RSTDIR to be asserted.

NOTE: Setting this bit in SCRIPTS causes a fatal interrupt, which will halt SCRIPTS execution.

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4.3 SCSI Control One Register (SCNTL1) (continued)

4.3.6 Bit 2 - AESP (Assert even SCSI parity (force bad parity))

When this bit is set and the Enable Parity Generation bit is set (bit 2 in the SCNTL0 register), the SYM53C770 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the SYM53C770. If parity checking is enabled, then the SYM53C770 checks data received for odd parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.

4.3.7 Bit 1 - IARB (Immediate Arbitration)

Setting this bit will cause the SCSI core to immediately begin arbitration once a Bus Free phase is detected following an expected SCSI disconnect. This bit is useful for multi-threaded applications. The ARB1-0 bits in SCNTL0 should be set for full arbitration and selection before setting Immediate Arbitration.

Arbitration will be re-tried until won. At that point, the SYM53C770 will hold BSY and SEL asserted, and wait for a select or reselect sequence to be requested. The Immediate Arbitration bit will be reset automatically when the selection or reselection sequence is completed, or times out.

An unexpected disconnect condition will clear IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit (SCNTL2 bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the Abort bit in the SCRIPTS processor registers should be set. Then one of two things will eventually happen:

1) The Won Arbitration bit (SSTAT0 bit 2) will be asserted. In this case, the Immediate Arbitration bit needs to be reset. This will complete the abort sequence and disconnect the SYM53C770 from the SCSI bus. If it is not acceptable to go to Bus Free phase immediately following the arbitration phase, a low level selection may instead be performed.

2) The abort will complete because the SYM53C770 loses arbitration. This can be detected by the Immediate Arbitration bit being deasserted. The Lost Arbitration bit (SSTAT0 bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

4.3.8 Bit 0 - SST (Start SCSITransfer)

This bit is automatically set during SCRIPTS execution, and should not be used. It causes the SCSI core to begin a SCSI transfer, including REQ/ACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O bit in SOCL. This bit is self-resetting. This bit should not be set for low level operation.

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4.4 SCSI Control Two Register (SCNTL2)

SCSI Control Two Register (SCNTL2) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	SDU	CHM	SLPMD	SLPHBEN	WSS	VUE1	VUE0	WSR
Default	0	0	0	0	0	0	0	0

4.4.1 Bit 7 - SDU (SCSI Disconnect Unexpected)

When this bit is set, the SCSI core is not expecting the SCSI bus to enter the Bus Free phase. If it does, an unexpected disconnect error will be generated (see the Unexpected Disconnect bit in the SIST0 register, bit 2).

During normal SCRIPTS mode operation, this bit is set automatically whenever the SCSI core is reselected, or successfully selects another SCSI device. The SDU bit should be reset with a register write (Move 0x7f & SCNTL2 to SCNTL2) before the SCSI core expects a disconnect to occur, normally prior to sending an Abort, Abort Tag, Bus Device Reset, Clear Queue or Release Recovery message, or before deasserting ACK after receiving a Disconnect command or Command Complete message.

4.4.2 Bit 6 - CHM (Chained Mode)

This bit determines whether or not the SCSI core is programmed for chained SCSI mode. It is automatically set by the Chained Block Move (CHMOV) SCRIPTS instruction and is automatically cleared by the Block Move SCRIPTS instruction (MOVE).

Chained mode is primarily used to transfer consecutive wide data blocks. Using chained mode facilitates partial receive transfers and allows correct partial send behavior. When this bit is set and a data transfer ends on an odd byte boundary, the SYM53C770 will store the last byte in the SCSI Wide Residue Data Register during a receive operation or in the SCSI Output Data Latch register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed.

4.4.3 Bit 5 - SLPMD (SLPAR Mode Bit)

If this bit is clear, the SLPAR register functions like the SYM53C720. If this bit is set, the SLPAR register reflects the high or low byte of the SLPAR word, depending on the state of SCNTL2 bit 4. It also allows a seed value to be written to the SLPAR register.

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4.4 SCSI Control Two Register (SCNTL2) (continued)

4.4.4 Bit 4 - SLPHBEN (SLPAR High Byte Enable)

If this bit is clear, the low byte of the SLPAR word is present in the SLPAR register. If this bit is set, the high byte of the SLPAR word is present in the SLPAR register.

4.4.5 Bit 3 - WSS (Wide SCSI Send)

When read, this bit returns the value of the Wide SCSI Send (WSS) flag. Asserting this bit will clear the WSS flag. This clearing function is self-resetting.

When the WSS flag is high following a wide SCSI send operation, the SCSI core is holding a byte of "chain" data in the SODL register. This data will become the first low-order byte sent when "married" with a high-order byte during a subsequent data send transfer.

Performing a SCSI receive operation will clear this bit. Also, performing any non-wide transfer will clear this bit.

4.4.6 Bit 2 - VUE1 (Vendor Unique Enhancements bit 1)

This bit is a read only value indicating whether the group code field in the SCSI instruction is standard or vendor unique. If reset, the bit indicates standard group codes; if set, the bit indicates vendor unique group codes. The value in this bit is reloaded at the beginning of all asynchronous target receives. The default for this bit is reset.

4.4.7 Bit 1 - VUE0 (Vendor Unique Enhancements bit 0)

This bit is used to disable the automatic byte count reload during Block Move instructions in the command phase. If this bit is reset, the device will reload the Block Move byte count if the first byte received is one of the standard group codes. If this bit is set, the device will not reload the Block Move byte count, regardless of the group code.

4.4.8 Bit 0 - WSR (Wide SCSI Receive)

When read, this bit returns the value of the Wide SCSI Receive (WSR) flag. Asserting this bit will clear the WSR flag. This clearing function is self-resetting. The WSR flag indicates that the SCSI core received data from the SCSI bus, detected a possible partial transfer at the end of a chained or non-chained block move command, and temporarily stored the high-order byte in the SWIDE register rather than passing the byte out the DMA channel.

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4.4 SCSI Control Two Register (SCNTL2) (continued)

4.4.8 Bit 0 - WSR (Wide SCSI Receive) (continued)

The hardware uses the WSR status flag to determine what behavior must occur at the start of the next data receive transfer. When the flag is set, the stored data in SWIDE may be "residue" data, valid data for a subsequent data transfer, or overrun data. The byte may be read as normal data by starting a data receive transfer.

Performing a SCSI send operation will clear this bit. Also, performing any non-wide transfer will clear this bit.

4.5 SCSI Control Three Register (SCNTL3)

SCSI Control Three Register (SCNTL3) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	F20	SCF2	SCF1	SCF0	EWS	CCF2	CCF1	CCF0
Default	0	0	0	0	0	0	0	0

4.5.1 Bit 7 - F20 (Fast -20 Mode)

Setting this bit enables Fast-20 synchronous SCSI transfers in systems that have an 80 MHz clock. The default value of this bit is 0. This bit should remain cleared in systems that have a 40MHz clock, unless the SCSI clock doubler feature is used to increase the SCLK frequency to at least 80 MHz.

When this bit is set, the signal filtering period for $\overline{\text{SREQ}}$ and $\overline{\text{SACK}}$ automatically changes to 15 ns, regardless of the value of the Extend REQ/ ACK Filtering bit in the STEST2 register.

4.5.2 Bits 6-4 - SCF2-0 (Synchronous Clock Conversion Factor)

These bits select a factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. They should be written to the same value as the Clock Conversion Factor bits below unless fast SCSI operation is desired. See the table under the description of bits 2-0 of this register for the valid combinations. For more information on how the synchronous transfer rate is determined, refer to Chapter 2 of the *SYM53C770 Data Manual*.



NOTE

To migrate from a Fast SCSI-2 system with a 40MHz clock, divide the clock by a factor of two or more to achieve the same synchronous transfer rate in a system with an 80MHz clock.

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4.5 SCSI Control Three Register (SCNTL3) (continued)

4.5.3 Bit 3 - EWS (Enable Wide SCSI)

When this bit is clear, all information transfer phases are assumed to be eight bits transmitted on $\overline{SD7\text{-}0}$, $\overline{SDP0}$. When this bit is set, data transfers are done 16 bits at a time with the least significant byte on $\overline{SD7\text{-}0}$, $\overline{SDP0}$ and the most significant byte on SD14-8, $\overline{SDP1}$. Command, status, and message phases remain eight bits.

4.5.4 Bits 2-0 - CCF2-0 (Clock Conversion Factor)

These bits select a factor by which the frequency of SCLK is divided before being presented to the SCSI core. The bits are encoded as follows. All other combinations are reserved and should never be used. Also note that the synchronous portion of the SCSI core can be run at a different clock rate for fast SCSI. See the synchronous clock conversion factor bits above.

Table 4-7: Clock Conversion Factor

SCF2 CCF2	SCF1 CCF1	SCF0 CCF0	Factor Frequency	SCSI Clock (MHz)
0	0	0	SCLK/3	50.01 - 75
0	0	1	SCLK/1	16.67 - 25
0	1	0	SCLK/1.5	25.01 - 37.5
0	1	1	SCLK/2	37.51 - 50
1	0	0	SCLK/3	50.01 - 75
1	0	1	SCLK/4	75.01 - 100.00
1	1	0	Reserved	
1	1	1	Reserved	

It is important these bits be set to the proper values to guarantee that the SYM53C770 meets the SCSI timings as defined by the ANSI specification.

To migrate from a Fast SCSI-2 system with a 40MHz clock, divide the clock by a factor of two or more to achieve the same synchronous transfer rate in a system with an 80MHz clock.

If the SCSI clock doubler is enabled, use the desired frequency after doubling to determine the conversion factor.

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4.6 SCSI Chip ID Register (SCID)

SCSI Chip ID Register (SCID) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	RES	RRE	SRE	RES	ID3	ID2	ID1	ID0
Default	X	0	0	X	0	0	0	0

4.6.1 Bit 7 - Reserved

4.6.2 Bit 6 - RRE (Enable Response to Reselection)

When this bit is set, the SYM53C770 is able to respond to bus-initiated reselection at the chip ID in the RESPID0 and RESPID1 registers. Note that the SYM53C770 will not automatically reconfigure itself to initiator mode as a result of being reselected.

4.6.3 Bit 5 - SRE (Enable Response to Selection)

When this bit is set, the SYM53C770 is able to respond to bus-initiated selection at the chip ID encoded in the RESPID0 and RESPID1 registers. Note that the SYM53C770 will not automatically reconfigure itself to target mode as a result of being selected.

4.6.4 Bit 4 - Reserved

4.6.5 Bits 3-0 - Encoded Chip SCS1 ID

These bits are used to store the SYM53C770 encoded SCSI ID. This is the ID which the chip will assert when arbitrating for the SCSI bus. The priority of the sixteen possible IDs, in descending order is:

Table 4-8: Encoded Chip SCSI ID

SCSI ID	Binary	Priority	SCSI ID	Binary	Priority
7	0111	Highest	15	1111	
6	0110		14	1110	
5	0101		13	1101	
4	0100		12	1100	
3	0011		11	1011	
2	0010		10	1010	
1	0001		9	1001	
0	0000		8	1000	Lowest

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4.7 SCSITransfer Register (SXFER)

SCSITransfer Register (SXFER) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	TP2	TP1	TP0	MO4	MO3	MO2	MO1	MO0
Default	0	0	0	0	0	0	0	0

NOTE: When using Table Indirect I/O commands, bits 7-5 and 3-0 of this register will be loaded from the I/O data structure.

4.7.1 Bits 7-5 - TP2-0 (SCSI Synchronous Transfer Period)

These bits determine the SCSI synchronous transfer period used by the SYM53C770 when sending synchronous SCSI data in either initiator or target mode. See the following table:

Table 4-9: SCSI Synchronous Transfer Period

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

The synchronous transfer period the SYM53C770 should use when transferring SCSI data is found as in the following example: The SYM53C770 is interfaced to a hard disk which can transfer data at 10 MB/s synchronously. The SYM53C770's SCLK is running at 40 MHz. The synchronous transfer period (SXFERP) is found as follows:

SXFERP = Period/SSCP + ExtCC

Period = 1 ÷ Frequency ÷ 10 MB/s = 100 ns

SSCP = 1 ÷ SSCF = 1 ÷ 40 MHz = 25 ns (This SCSI synchronous core clock is determined in SCNTL3 bits 6-4.)

ExtCC = 1 if SCNTL1 bit 7 is asserted and the SYM53C770 is sending data. (ExtCC = 0 if the SYM53C770 is receiving data.)

SXFERP = 100 ÷ 25 = 4

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4.7 SCSITransfer Register (SXFER) (continued)

Table 4-10: Example of synchronous transfer periods

SCSI-1 transfer rates:					SCSI-2 and Fast-20 transfer rates:				
CLK (MHZ)	SCSI CLK ÷ SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate(MB/s)	CLK (MHZ)	SCSI CLK ÷ SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate(MB/s)
100	÷4	5	200	5.0	100	÷1	4	40	25.0
80	÷4	4	200	5.0	100	÷2	4	80	12.5
80	÷4	5	250	4.0	100	÷1	5	50	20.0
66.67	÷3	4	180	5.55	100	÷2	5	100	10.0
66.67	÷3	5	225	4.44	80	÷1	4	50	20.0
50	÷2	4	160	6.25	80	÷2	4	100	10.0
50	÷2	5	200	5	66.77	÷1.5	4	90	11.1*
40	÷2	4	200	5	66.77	÷1.5	5	112.5	8.88
37.50	÷1.5	4	160	6.25	50	÷1	4	80	12.5*
33.33	÷1.5	4	180	5.55	50	÷1	5	100	10.0
25	÷1	4	160	6.25	40	÷1	4	100	10.0
20	÷1	4	200	5	37.50	÷1	4	106.67	9.375
16.67	÷1	4	240	4.17	33	÷1	4	120	8.33
					25	÷1	4	160	6.25
					20	÷1	4	200	5
					16.67	÷1	4	240	4.17
					* Violates SCSI specifications. Slower rates are achieved using larger XFERP values and/or different SCLK prescale values				

4.7.2 Bits 4-0 - MO4-MO0 (Max SCSI synchronous offset)

These bits describe the maximum SCSI synchronous offset used by the SYM53C720/SE/53C770 when transferring synchronous SCSI data in either initiator or target mode.

The table on the following page describes the possible combinations and their relationship to the synchronous data offset used by the SYM53C720/SE/53C770. These bits determine the SYM53C720/SE/53C770's method of transfer for Data In and Data Out phases only; all other information transfers will occur asynchronously.

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4.7 SCSITransfer Register (SXFER) (continued)

4.7.2 Bits 4-0 - MO4-MO0 (Max SCSI synchronous offset) (continued)

Table 4-11: Max SCSI Synchronous Offset

MO4	MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0	0 - Asynchronous
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	X	X	X	1	Reserved
1	X	X	1	X	Reserved
1	X	1	X	X	Reserved
1	1	X	X	X	Reserved

4.8 SCSI Destination ID Register (SDID)

SCSI Destination ID Register (SDID) - Read/Write

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RES	RRE	SRE	RES	ID3	ID2	ID1	ID0
Default	X	X	X	X	0	0	0	0

4.8.1 Bits 7-4 - Reserved

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4.8 SCSI Destination ID Register (SDID) (continued)

4.8.2 Bits 3-0 - Encoded Destination SCSI ID bits 3-0

Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases respectively.

When executing SCSI SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTS Select or Reselect instruction. The value written should be the binary-encoded ID value. The priority of the 16 possible IDs, in descending order, is shown in Table 4-8.

4.9 General Purpose Register (GPREG)

General Purpose Register (GPREG) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved			GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Default	X	X	X	0	1	1	1	1

4.9.1 Bits 7-5 - Reserved

4.9.2 Bits 4-0 - GPIO4-0 (General Purpose Inputs/Outputs)

These bits allow the SYM53C770 to detect the input signals of a connected device. The general purpose inputs can be used to sense the SYM53C770 chip ID or board configuration at power up. A Register-to-Register Move instruction may be used to move the sensed value into the appropriate register. These are live signals; if the pin is changing, the data is also changing. The bit values in the General Purpose Control Register (47h) determine whether these bits are inputs or outputs.

Bits 3-0 power up as inputs, and Bit 4 powers up as an output. The general purpose output feature may be used to enable attached ROM, RAM, LEDs, or other components on an SYM53C770 board.



NOTE

The input pins all have 100 mA internal pull-ups.

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4.10 SCSI First Byte Received Register (SFBR)

SCSI First Byte Received Register (SFBR) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	0	0	0	0	0	0	0	0

4.10.1 Bits 7-0 - 1B7-0 (First byte received)

This register contains the first byte received in any asynchronous information transfer phase. For example, when the SYM53C770 is operating in initiator mode, this register contains the first byte received in Message In, Status, and Data In phases.

When a Block Move Instruction is executed for a particular phase, the first byte received is stored in this register -- even if the present phase is the same as the last phase. The first byte value received for a particular input phase is not valid until after a Move instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

This register also holds the state of the lower eight bits of the SCSI data bus during a selection or reselection unless the COM bit in the DCNTL register is set.

4.11 SCSI Output Control Latch Register (SOCL)

SCSI Output Control Latch Register (SOCL) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	AEQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
Default	0	0	0	0	0	0	0	0

4.11.1 Bit 7 - REQ (Assert SCSI $\overline{\text{REQ}}$ signal)

4.11.2 Bit 6 - ACK (Assert SCSI $\overline{\text{ACK}}$ signa1)

4.11.3 Bit 5 - BSY (Assert SCSI $\overline{\text{BSY}}$ signal)

4.11.4 Bit 4 - SEL (Assert SCSI $\overline{\text{SEL}}$ signal)

4.11.5 Bit 3 - ATN (Assert SCSI $\overline{\text{ATN}}$ signa1)

4.11.6 Bit 2 - MSG (Assert SCSI $\overline{\text{MSG}}$ signal)

4.11.7 Bit 1 - C/D (Assert SCSI $\overline{\text{C_D}}$ signal)

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4.11 SCSI Output Control Latch Register (SOCL) (continued)

4.11.8 Bit 0 - I/O (Assert SCSI $\overline{I_O}$ signal)

This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SOCL should only be used when transferring data via programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the SYM53C770 starts executing SCSI SCRIPTS.

4.12 SCSI Selector ID Register (SSID)

SCSI Selector ID Register (SSID) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	VAL	Reserved			Encoded SCSI Destination ID			
Default	X	X	X	X	X	X	X	X

4.12.1 Bit 7 - VAL (SCSIValid Bit)

If VAL is asserted, the two SCSI IDs were detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID was present and the contents of the encoded destination ID are meaningless.

4.12.2 Bits 6-4 - Reserved

4.12.3 Bits 3-0 - Encoded Destination SCSI ID

Reading the SSID register immediately after the SYM53C770 has been selected or reselected returns the binary-encoded SCSI ID of the device which performed the operation. These bits are invalid for targets that are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit, bit 7.

4.13 SCSI Bus Control Lines Register (SBCL)

SCSI Bus Control Lines Register (SBCL) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
Default	X	X	X	X	X	X	X	X

4.13.1 Bit 7 - REQ ($\overline{REQ}$ status)

4.13.2 Bit 6 - ACK ($\overline{ACK}$ status)

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4.13 SCSI Bus Control Lines Register (SBCL) (continued)

4.13.3 Bit 5 - BSY (BSY status)

4.13.4 Bit 4 - SEL (SEL status)

4.13.5 Bit 3 - ATN (ATN status)

4.13.6 Bit 2 - MSG (MSG status)

4.13.7 Bit 1 - C/D (C_D status)

4.13.8 Bit 0 - I/O (I_O status)

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read; they may change while being read. This register can be used for diagnostics testing or operation in low level mode.

4.14 DMA Status Register (DSTAT)

DMA Status Register (DSTAT) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DFE	HPE	BF	ABRT	SSI	SIR	WTD	IID
Default	X	X	X	X	X	X	X	X

Reading this register will clear any of bits 6-0 at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the SYM53C770 stacks interrupts). The DIP bit in the ISTAT register will also be cleared. DMA interrupt conditions may be individually masked through the DIEN register.

When performing consecutive 8-bit reads of the DSTAT, SIST0 and SIST1 registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. To avoid missing a SCSI interrupt while reading any of these registers when the ISTAT SIP and DIP bits may not be set, read SIST0 and SIST1 before DSTAT.

4.14.1 Bit 7 - DFE (DMA FIFO empty)

This status bit is set when the DMA FIFO is empty. This bit may be changing at the time this register is read. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and will not cause an interrupt. This bit is not cleared by reading the register.

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4.14 DMA Status Register (DSTAT) (continued)

4.14.2 Bit 6 - HPE (Host Parity Error)

This bit is set when a host bus parity error is detected during a slave write or DMA read operation.

4.14.3 Bit 5 - BF (Bus fault)

This bit is set when a host bus fault condition is detected. A host bus fault can only occur when the SYM53C770 is bus master, and is defined as a memory cycle that is ended by the assertion of $\overline{\text{BERR}}$ or $\overline{\text{TEA}}$.

4.14.4 Bit 4 - ABRT (Aborted)

This bit is set when an abort condition occurs. An abort condition occurs because of the following: the DP3 $\overline{\text{ABRT}}$ input signal is asserted by another device (parity generation mode) or a software abort command is issued by setting bit 7 of the ISTAT register.

4.14.5 Bit 3 - SSI (SCRIPTS step interrupt)

If the Single-Step Mode bit in the DCNTL register is set, this bit will be set and an interrupt generated after successfully executing each SCRIPTS instruction.

4.14.6 Bit 2 - SIR (SCRIPTS interrupt instruction received)

This status bit is set whenever a SCRIPTS Interrupt instruction is received. Bit 1 WTD (Watchdog time-out detected) This status bit is set when the watchdog timer decrements to 0. The watchdog timer is only used for the host memory interface. When the timer decrements to 0, it indicates that the memory system did not assert the acknowledge signal within the specified time-out period.

4.14.7 Bit 0 - IID (Illegal instruction detected)

This status bit is set any time an illegal instruction is detected, whether the SYM53C770 is operating in single-step mode or automatically executing SCSI SCRIPTS. This bit will also be set if the SYM53C770 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.

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4.15 SCSI Status Zero Register (SSTAT0)

SCSI Status Zero Register (SSTAT0) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	ILF	ORF	OLF	AIP	LOA	WOA	$\overline{\text{RST}}$	$\overline{\text{SDP}}$
Default	0	0	0	0	0	0	0	0

4.15.1 Bit 7 - ILF (SIDL least significant byte full)

This bit is set when the least significant byte in the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not Bow through this register.

4.15.2 Bit 6 - ORF (SODR least significant byte full)

This bit is set when the least significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It cannot be read or written by the user. This bit can be used to determine how many bytes reside in the chip when an error occurs.

4.15.3 Bit 5 - OLF (SODL least significant byte full)

This bit is set when the least significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SODR register before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

4.15.4 Bit 4 - AIP (Arbitration in progress)

Arbitration in Progress (AIP = 1) indicates that the SYM53C770 has detected a Bus Free condition, asserted BSY, and asserted its SCSI ID onto the SCSI bus.

4.15.5 Bit 3 - LOA (Lost arbitration)

When set, LOA indicates that the SYM53C770 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the $\overline{\text{SEL}}$ signal.

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4.15 SCSI Status Zero Register (SSTAT0) (continued)

4.15.6 Bit 2 - WOA (Won arbitration)

When set, WOA indicates that the SYM53C770 has detected a Bus Free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCNTL0 register must be full arbitration and selection for this bit to be set.

4.15.7 Bit 1 - RSTI (SCSI RSTI signal)

This bit reports the current status of the SCSI $\overline{\text{RST}}$ signal, and the RST signal (bit 6) in the ISTAT register. This bit is not latched and may be changing when read.

4.15.8 Bit 0 - $\overline{\text{SDP0}}$ (SCSI $\overline{\text{SDP0}}$ parity signal)

This bit represents the active high current status of the SCSI $\overline{\text{SDP0}}$ parity signal. This signal is not latched and may be changing as it is read.

4.16 SCSI Status One Register (SSTAT1)

SCSI Status One Register (SSTAT1) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	FF3	FF2	FF1	FF0	SDP	MSG	C/D	I/O
Default	0	0	0	0	X	X	X	X

4.16.1 Bits 7-4 - FF3-0 (FIFO flags)

Table 4-12: FIFO Flags

FF4 (SSTAT2 Bit 4)	FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16

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4.16 SCSI Status One Register (SSTAT1) (continued)

These five bits define the number of bytes or words that currently reside in the SYM53C770's SCSI synchronous data FIFO. They are not latched and they will change as data moves through the FIFO.

4.16.2 Bit 3 - SDP0 (Latched SCSI parity)

This bit reflects the SCSI parity signal (SDP0) corresponding to the data latched in the SCSI Input Data Latch register (SIDL). It changes when a new byte is latched into the least significant byte of the SIDL register. This bit is active high, i.e., it is set when the parity signal is active.

4.16.3 Bit 2 - MSG (SCSI $\overline{\text{MSG}}$ signal)

4.16.4 Bit 1 - CID (SCSI $\overline{\text{C_D}}$ signal)

4.16.5 Bit 0 - IIO (SCSI $\overline{\text{I_O}}$ signal)

These SCSI phase status bits are latched on the asserting edge of $\overline{\text{REQ}}$ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low level mode.

4.17 SCSI Status Two Register (SSTAT2)

SCSI Status Two Register (SSTAT2) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	ILF1	ORF1	OLF1	FF4	SPL1	DIFF	LDSC	SDP1
Default	0	0	0	0	X	0	1	X

4.17.1 Bit 7 - ILF1 (SIDL most significant byte full)

This bit is set when the most significant byte in the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through the SIDL register.

4.17.2 Bit 6 - ORF1 (SODR most significant byte full)

This bit is set when the most significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is not accessible to the user. This bit can be used to determine how many bytes reside in the chip when an error occurs.

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4.17 SCSI Status Two Register (SSTAT2) (continued)

4.17.3 Bit 5 - OLF1 (SODL most significant byte full)

This bit is set when the most significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SODR register before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

4.17.4 Bit 4 - FF4 (FIFO Flags bit 4)

This is the most significant bit in the SCSI FIFO Flags field, with the rest of the bits in SSTAT1. For a complete description of this field, see the definition for SSTAT1 bits 7-4.

4.17.5 Bit 3 - Latched SCSI parity for SD15-8

This active high bit reflects the SCSI odd parity signal corresponding to the data latched into the most significant byte in the SIDL register.

4.17.6 Bit 2 - DIFFSENSE SENSE

If this bit is reset, the correct cable type has been connected for the differential operation. If this bit is set, a single ended cable has been connected to the device's DIFFSENSE pin.

4.17.7 Bit 1 - LDSC (Last Disconnect)

Used in conjunction with the Connected (CON) bit in SCNTL1, this status bit allows the user to detect the case in which a target device disconnects, and then some SCSI device selects or reselects, the SYM53C770. If the Connected bit is asserted and the LDSC bit is asserted, a disconnect has occurred. This bit is set when the Connected bit in SCNTL1 is off. This bit is cleared when a Block Move instruction is executed while the Connected bit in SCNTL1 is on.

4.17.8 Bit 0 - SDP1 (SCSI SDP1 Signal)

This bit represents the active-high current state of the SCSI SDP1 parity signal. It is unlatched and may be changing as it is read.

4.18 Data Structure Address Registers (DSA)

Read/Write

This 32-bit register contains the base address used for all table indirect calculations. During any Memory-to-Memory Move operation, the contents of this register are shadowed.

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4.19 Interrupt Status Register (ISTAT)

Interrupt Status Register (ISTAT) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	ABRT	RST	SIGP	SEM	CON	INTF	SIP	DIP
Default	0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the SYM53C770 is executing SCRIPTS (without interfering in the operation of the SYM53C770). It may be used to poll for interrupts if interrupts are disabled. There may be stacked interrupts pending; read this register after clearing an interrupt to check for stacked interrupts.

4.19.1 Bit 7 - ABRT (Abort operation)

Setting this bit aborts the current operation being executed by the SYM53C770. If this bit is set and an interrupt is received, reset this bit before reading the DSTAT register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1) Set this bit

2) Wait for an interrupt

3) Read the ISTAT register

4) If the SCSI Interrupt Pending bit is set, then read the SIST0 or SIST1 register to determine the cause of the SCSI Interrupt and go back to Step 2

5) If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 00h value to this register

6) Read the DSTAT register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.



NOTE

The abort function cannot be used during a select or reselect instruction. In these cases, the time-out feature should be used.

After an abort, follow the data recovery steps in Chapter 2 to make sure no data is left in the chip.

4.19.2 Bit 6 - RST (Software reset)

Setting this bit resets the SYM53C770. All registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI $\overline{\text{RST}}$ signal to be asserted. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit). This reset will not clear the Enable Acknowledge (EA) bit, Function Code 1 bit, or the ID Mode bit.

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4.19 Interrupt Status Register (ISTAT) (continued)

4.19.3 Bit 5 - SIGP (Signal process)

SIGP is a R/W bit that can be written at any time, and polled and reset via CTEST2. The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPT. The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/Reselection. Setting this bit causes that op code to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/ reselection condition. For more information on the SIGP bit, refer to the SYM53C770 Programming Guide.

4.19.4 Bit 4 - SEM (Semaphore)

This bit can be set by the SCRIPTS processor using a SCRIPTS register write instruction. The bit may also be set by an external processor while the SYM53C770 is executing a SCRIPT. This bit enables the SYM53C770 to notify an external processor of a predefined condition while SCRIPTS are running. The external processor may also notify the SYM53C770 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

4.19.5 Bit 3 - CON (Connected)

This bit is automatically set any time the SYM53C770 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the SYM53C770 has responded to a bus-initiated selection or reselection. It will also be set after successfully completing arbitration when operating in low level mode. When this bit is clear, the SYM53C770 is not connected to the SCSI bus.

4.19.6 Bit 2 - INTF (Interrupt on the Fly)

This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. This bit can be used to notify a service routine, running on the main processor while the SCRIPTS processor is still executing a SCRIPTS program.



NOTE

This bit must be written to one in order to clear it after it has been set.

If the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip status registers. An interrupt on the fly interrupt must be cleared before servicing any other interrupts indicated by SIP or DIP.

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4.19 Interrupt Status Register (ISTAT) (continued)

4.19.7 Bit 1 - SIP (SCSI interrupt pending)

This status bit is set when an interrupt condition is detected in the SCSI portion of the SYM53C770. The following conditions will cause a SCSI interrupt to occur:

- ❑ A phase mismatch (initiator mode) or $\overline{\text{ATN}}$ becomes active (target mode)
- ❑ An arbitration sequence is complete
- ❑ A selection or reselection time-out occurs
- ❑ The SYM53C770 was selected
- ❑ The SYM53C770 was reselected
- ❑ A SCSI gross error occurs
- ❑ An unexpected disconnect occurs
- ❑ A SCSI reset occurs
- ❑ A parity error is detected
- ❑ The handshake-to-handshake timer is expired
- ❑ The general purpose timer is expired

To determine exactly which condition(s) caused the interrupt, the SIST0 and SIST1 registers should be read. Both registers must be read to clear the interrupt. This bit is synchronous to BCLK, but may change during read cycles.

4.19.8 Bit 0 - DIP (DMA interrupt pending)

This status bit is set when an interrupt condition is detected in the DMA portion of the SYM53C770. The following conditions will cause a DMA interrupt to occur:

- ❑ A host parity error is detected
- ❑ A bus fault is detected
- ❑ An abort condition is detected
- ❑ A SCRIPTS instruction is executed in single-step mode
- ❑ A SCRIPTS interrupt instruction is executed
- ❑ The Watchdog Timer decrements to zero
- ❑ An illegal instruction is detected

To clear DIP and determine exactly which condition(s) caused the interrupt, read the DSTAT register.

This bit is synchronous to BCLK, but may change during read cycles.

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4.20 Chip Test Zero Register (CTEST0)

Chip Test Zero Register (CTEST0) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	CDIS	SC1	SC0	GRP	DFP	EHP	TT1	C386E
Default	0	0	0	0	X	0	0	0

4.20.1 Bit 7 - CDIS (Cache burst disable)

When this bit is set, the SYM53C770 will not request a cache line burst. When this bit is clear, the chip will attempt cache line bursts when all necessary conditions are met.



NOTE

If the hardware does not support cache-line bursts, this bit should be set to maximize performance.

4.20.2 Bits 6-5 - SC1-0 (Snoop control)

The values of these bits are asserted on the corresponding device pins during bus mastership if bit 0 of CTEST3 is clear. Otherwise, the SC1 pin will always be driven with the value of the SC1 bit, and the SC0 pin will reflect the state of the internal host cycle request signal. These bits are not available for snoop mode if the Size Throttle Enable bit (DCNTL1, bit 7) is set.

4.20.3 Bit 4 - GRP (Generate Receive Parity)

When this bit is set and the SYM53C770 is in parity pass through mode (Bit 2 in the SCNTL0 register is clear), parity received on the SCSI bus will not pass through the DMA FIFO. Parity will be generated as data enters the DMA FIFO, eliminating the possibility of bad SCSI parity passing through to the host bus. A SCSI parity error interrupt will be generated but a system parity problem will not be created. After reset or when the bit is cleared, and when parity pass through mode is enabled (Bit 2 in SCNTL0 is clear), parity received on the SCSI bus will pass through the SYM53C770 unmodified.

4.20.4 Bit 3 - DFP (DMA FIFO parity)

This bit represents the parity bit of the DMA FIFO when reading data out of the DMA FIFO via programmed I/O. In order to transfer data to or from the DMA FIFO, perform a read or a write to the CTEST6 register. Manually loading the FIFO moves this bit into the FIFO as the parity bit, along with the byte that came was written to the CTEST6 register. For the details of performing a diagnostic test of the DMA FIFO, refer to the SYM720/770 Programming Guide.

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4.20 Chip Test Zero Register (CTEST0) (continued)

4.20.5 Bit 2 - EHP (Even host parity)

Parity is generated for all slave mode register reads and master mode memory writes. This bit controls the parity sense. Setting this bit causes the SYM53C770 to generate even parity when driving data on the host data bus. The SYM53C770 inverts the parity bit received from the SCSI bus to create even parity. In addition, the even parity received from the host bus is inverted to odd parity before the SYM53C770 checks parity and sends the data to the SCSI bus. Clearing this bit causes the SYM53C770 to maintain odd parity throughout the chip.

4.20.6 Bit 1 - TT1 (Transfer type bit)

The inverted value of this bit is asserted on the TT1 pin during bus mastership in Bus Modes 2, 3 and 4 only. This bit is not used in Bus Mode l. In Bus Mode 4, the TT1 pin is supported only if Cache 386 mode is not enabled. The TT0 bit is in the DMODE register.

4.20.7 Bit 0 - C386E (Cache 386 Enable)

Asserting this bit enables caching in the 80386DX bus mode. Caching implies that the chip will supply an address together with an Address Strobe ($\overline{ADS}$), and on the consecutive clocks the SYM53C770 will wait for four $\overline{READYI}$ pulses and will either supply four longwords of data or receive four longwords of data. The SYM53C770 does not support caching in 80386SX mode or slave mode.

The chip generates the Cache Burst Request (CBREQ) signal and samples the Transfer Burst Inhibit (TBI) signal during the first data transfer (first $\overline{READYI}$). $\overline{CBREQ}$ indicates an attempt to execute a line transfer of four longwords. $\overline{TBI}$ asserted indicates that the system memory does not support the SYM53C770 burst request. The chip powers up with this feature disabled. The bit will be reset during either a software or hardware reset.

4.21 Chip Test One Register (CTEST1)

Chip Test One Register (CTEST1) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFL0
Default	1	1	1	1	0	0	0	0

4.21.1 Bits 7-4 - FMT3-0 (Byte Empty in DMA FIFO)

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 will be set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

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4.21 Chip Test One Register (CTEST1) (continued)

4.21.2 Bits 3-0 - FFL3-0 (Byte Full in DMA FIFO)

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 will be set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

4.22 Chip Test Two Register (CTEST2)

Chip Test Two Register (CTEST2) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DDIR	SIGP	RES	RES	DFP	TEOP	OREQ	DACK
Default	0	0	X	X	0	0	0	1

4.22.1 Bit 7 - DDIR (Data Transfer Direction)

This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus.

4.22.2 Bit 6 - SIGP (Signal process)

This bit is a copy of the SIGP bit in the ISTAT register (bit 5). The SIGP bit is used to signal a running SCRIPTS operation. When this register is read, the SIGP bit in the ISTAT register is cleared.

4.22.3 Bit 5-4 - Reserved

4.22.4 Bit 3 - DFP (DMA FIFO parity)

This bit represents the parity bit of the DMA FIFO when the CTEST6 register reads data out of the FIFO. Reading the CTEST6 register unloads one data byte from the bottom of the DMA FIFO. When the CTEST6 register is read the parity signal is latched into this bit location and the next byte falls down to the bottom of the FIFO.

4.22.5 Bit 2 - TEOP (SCSI true end of process)

This bit indicates the status of the SYM53C770's internalities signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the SYM53C770. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

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4.22 Chip Test Two Register (CTEST2) (continued)

4.22.6 Bit 1 - DREQ (Data request status)

This bit indicates the status of the SYM53C770's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

4.22.7 Bit 0 - DACK (Data acknowledge status)

This active low bit indicates the status of the SYM53C770's internal Data Acknowledge signal ($\overline{\text{DACK}}$). When this bit is set, $\overline{\text{DACK}}$ is inactive. When this bit is clear, $\overline{\text{DACK}}$ is active.

4.23 Chip Test Three Register (CTEST3)

Chip Test Three Register (CTEST3) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	VS	V2	V1	V0	FLF	CLF	FM	SM
Default	X	X	X	X	0	0	0	0

4.23.1 Bits 7-4 - V3-0 (Chip revision level)

These bits identify the chip revision level for software purposes.

4.23.2 Bit 3 - FLF (Flush DMA FIFO)

When this bit is set, data residing in the DMA FIFO is transferred to or from memory, starting at the address in the DNAD register. The internal DMAWR signal, controlled by the CTEST5 register, determines the direction of the transfer. This bit is not self clearing; once the SYM53C770 has successfully transferred the data, this bit should be reset.

4.23.3 Bit 2 - CLF (Clear DMA FIFO)

When this bit is set, all data pointers for the DMA FIFO are cleared. Any data in the FIFO is lost. This bit automatically resets after the SYM53C770 has successfully cleared the appropriate FIFO pointers.

4.23.4 Bit 1 - FM (Fetch pin mode)

When set, this active low bit causes the $\overline{\text{FETCH}}$ pin to deassert during indirect apd table indirect read operations. $\overline{\text{FETCH}}$ will only be active during the op code portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM. If this bit is not set, $\overline{\text{FETCH}}$ will be asserted for all bus cycles during instruction fetches.

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4.23 Chip Test Three Register (CTEST3) (continued)

4.23.5 Bit 0 - SM (Snoop pins mode)

When set, the snoop pins change functions and become pure outputs that are always driven, except when in ZMODE. The values driven are listed in the following table. When clear, the snoop pins are driven during host bus ownership with the values of the CTEST0 SC(1-0) bits.

Pin: SC0. Function: Becomes a copy of the internal bus request signal. Signal will assert prior to $\overline{TS}$/ $\overline{BR}$ and will be negated during the $\overline{TS}$/ $\overline{BR}$ of the last bus cycle.

NOTE: This signal cannot be used when the STE bit in the DCNTL register is set.

4.24 Temporary Stack Registers (TEMP)

Read/Write

This 32-bit register stores the instruction address pointer for a CALL or a RETURN instruction.

The address pointer stored in this register is loaded into the DSP register. This address points to the next instruction to be executed. Do not write to TEMP while the SYM53C770 is executing SCSI SCRIPTS.

During any Memory-to-Memory Move operation, the contents of this register are shadowed.

4.25 DMA FIFO Register (DFIFO)

DMA FIFO Register (DFIFO) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	RES	BO6	BO5	BO4	BO3	BO2	BO1	SO0
Default	X	0	0	0	0	0	0	0

4.25.1 Bit 7 - Reserved

4.25.2 Bits 6-0 - BO6-0 (Byte offset counter)

These seven bits indicate the amount of data transferred between the SCSI core and the DMA core. It may be used to determine the number of bytes in the DMA FIFO when a DMA error occurs. These bits are unstable while data is being transferred between the two cores; once the chip has stopped transferring data, these bits are stable.

The following steps will determine how many bytes are left in the DMA FIFO:

1) Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register.

2) AND the result with 7Fh for a byte count between zero and 96.

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4.26 Chip Test Four Register (CTEST4)

Chip Test Four Register (CTEST4) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	MUX	ZMOD	ZSD	SRTM	EHPC	FBL2	FBL1	FBL0
Default	0	0	0	0	0	0	0	0

4.26.1 Bit 7 - MUX (Host bus multiplex mode)

When set, the MUX bit puts the SYM53C770 into host bus multiplex mode. In this mode, the chip asserts a valid address for one BCLK (during which AS/TS is valid and the data bus is tristated), and then tristates the address bus and drives the data bus (if a write). This allows the address and data buses to be tied together. It should be written before acquiring bus mastership. Multiplex mode is only available in Bus Mode 2.

4.26.2 Bit 6 - ZMOD (High impedance mode)

Setting this bit causes the SYM53C770 to place all output and bidirectional pins into a high-impedance state. In order to read data out of the SYM53C770, this bit must be cleared.

This bit is intended for board-level testing only. Setting this bit during system operation will likely result in a system failure.

4.26.3 Bit 5 - ZSD (SCSI DMA High Impedance Mode)

Setting this bit causes the SYM53C770 to place the SCSI data bus (SD (15-0)) and the parity lines (SDP (1-0)) in a high-impedance state. In order to transfer data on the SCSI bus, this bit must be cleared. This bit differs from the SCSI High Impedance Mode bit in the STEST2 register, in that it only affects the SCSI data lines.

4.26.4 Bit 4 - SRTM (Shadow Register Test Mode)

Asserting this bit allows the user to read the shadowed temporary stack (TEMP) and Data-Structure Address (DSA) registers. These registers are shadowed because both are written over during a Memory to Memory move operation. The DSA and TEMP registers contain the base address used for table indirect calculations, and the instruction address pointer for a call or return instruction, respectively.

4.26.5 Bit 3 - EHPC (Enable Host Parity Check)

Setting this bit enables parity checking during slave write and DMA read execution if the Enable Parity Generation bit is cleared (SCNTL0 bit 2). The system powers up with this bit disabled so that the SYM53C770 will function properly with systems that do not support parity.

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4.26 Chip Test Four Register (CTEST4) (continued)

4.26.6 Bits 2-0 - FBL2-0 (FIFO byte control)

Table 4-13: FIFO Byte Control				
FBL2	**FBL1**	**FBL0**	**DMA FIFO Byte Lane**	**Pins**
0	X	X	Disabled	n/a
1	0	0	0	D(7-0)
1	0	1	1	D(15-8)
1	1	0	2	D(23-16)
1	1	1	3	D(31-24)

These bits define which byte lane of the DMA FIFO is read or written when the CTEST6 register is read or written. If the FBL2 bit is set, then FBL1 and FBL0 determine which of four byte lanes can be read or written. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero (set it to this value before executing SCSI SCRIPTS).

4.27 Chip Test Five Register (CTEST5)

Chip Test Five Register (CTEST5) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	ADCK	BBCK	FPTM	MASR	DDIR	RAM1	RAM1	RAMEN
Default	0	0	0	0	0	0	0	0

4.27.1 Bit 7 - ADCK (Clock address incrementor)

Setting this bit increments the address pointer contained in the DNAD register. The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

4.27.2 Bit 6 - BBCK (Clock byte counter)

Setting this bit decrements the byte count contained in the DBC register. The DBC register supports 24 bits. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DBC register.

4.27.3 Bit 5 - FPTM (Fetch pin test mode)

Setting this bit causes the fetch pin to assert during all opcode fetches to the internal scripts ram. This bit can be used during code debug to verify that internal script instruction fetches and execution have occurred. When reset, or after power-up, the fetch pin asserts only during external accesses.

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4.27 Chip Test Five Register (CTEST5) (continued)

4.27.4 Bit 4 - MASR (Master control for set or reset pulses)

This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is reset, bit 3 deasserts the corresponding signals. This bit and bit 3 should not be changed in the same write cycle.

4.27.5 Bit 3 - DDIR (DMA direction)

Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus. Bit 2-1 RAM1-0 (SCRIPTS RAM bits 1-0) These bits are used to enable the 4K internal SCRIPTS RAM. Their values combine to allow three different implementation of the SCRIPTS RAM. For more information on the internal SCRIPTS RAM, see Chapter 2 of the *SYM53C770 Data Manual*.

Table 4-14: DMA Direction

Bit 2	Bit 1	Method
0	0	SCRIPTS RAM disabled
0	1	SCRIPTS RAM accessed through indexed addressing in chip register space
1	0	SCRIPTS RAM accessed through increased chip select address space
1	1	SCRIPTS RAM access through additional chip select pin

4.27.6 Bit 0 - RAMEN (RAM Base Address Enable)

When this bit is set, the SCRATCHA register is shadowed to hold the base address of the internal SCRIPTS RAM. This allows the internal chip logic to recognize the location of the SCRIPTS RAM in the system memory map.

The actual contents of the SCRATCHA register are preserved. This bit also causes SCRATCHB to become the indexed address pointer when the indexed mode has been enabled. The actual contents of SCRATCHB are preserved.

4.28 Chip Test Six Register (CTEST6)

Read/Write

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. When data is read from the DMA FIFO, the parity bit for that byte is latched and stored in the DMA FIFO parity bit in the CTEST2 register.

To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting SCRIPTS.

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4.29 DMA Byte Counter Registers (DBC)

Read/Write

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the SYM53C770. The DBC counter is decremented each time that the $\overline{AS}$ ($\overline{TS}$ in Bus Mode 2, $\overline{ADS}$ in Bus Modes 3 and 4) signal is pulsed by the SYM53C770. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DBC register is FFFFFFh. If the instruction is Block Move and a value of 000000h is loaded into the DBC register, an illegal instruction interrupt will occur if the SYM53C770 is not in target mode Command phase. The DBC register is also used during table indirect I/O SCRIPTS to hold the offset value.

4.30 DMA Command Register (DCMD)

Read/Write

This 8-bit register determines the instruction for the SYM53C770 to execute. This register has a different format for each instruction. For a complete description, refer to the SYM53C770 instruction set in Chapter 5.

4.31 DMA Next Data Address Registers (DNAD)

Read/Write

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DSPS register. Its value may not be valid except in certain abort conditions.

4.32 DMA SCRIPTS Pointer Registers (DSP)

Read/Write

To execute SCSI SCRIPTS, the address of the first SCSI SCRIPTS routine must be written to this register. In normal SCRIPTS operation, once the starting address of the SCSI SCRIPTS is written to this register, the SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a SCRIPTS step interrupt after each instruction is executed. The DSP register does not need to be written with the next address, but the Start DMA bit (bit 2, DCNTL register) must be set each time the step interrupt occurs to fetch and execute the next SCSI SCRIPTS instruction. When writing this register eight bits at a time, writing the upper eight bits begins execution of the SCSI SCRIPTS routine.

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4.33 DMA SCRIPTS Pointer Save Registers (DSPS)

Read/Write

This register contains the second longword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS Interrupt instruction is fetched, this register holds the interrupt vector.

4.34 Scratch Register A (SCRATCHA)

Read/Write

This is a general purpose user definable scratch pad register. Normal SCRIPTS operations will not destroy the contents of this register; only Register Read/Write and Memory Moves into the SCRATCHA register will alter its contents. SCRIPTS programs may read or write individual bytes in this register by using the names SCRATCHA0 and SCRATCHA1. When the internal SCRIPTS RAM is enabled using any of the three methods described in Chapter 2, and when bit 0 is set in the CTEST5 register, this register is shadowed to provide a base address for the SCRIPTS RAM. The shadowed version of this register allows the internal logic of the SYM53C770 to recognize the location of the SCRIPTS RAM in the system memory map. The contents of the SCRATCHA register are preserved when shadowed.

4.35 DMA Mode Register (DMODE)

DMA Mode Register (DMODE) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	BL1	BL0	FC2	FC1	PD	FAM	UO	MAN
Default	0	0	0	0	0	0	0	0

4.35.1 Bit 7-6 - BL1-0 (Burst length)

Table 4-15: BL1 BL0 Burst Length		
BL1	**BL0**	**Burst Length**
0	0	2-transfer burst
0	1	4-transfer burst
1	0	8-transfer burst
1	1	16-transfer burst

These bits control the maximum number of bus cycles performed per bus ownership. The SYM53C770 asserts the Bus Request output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request (Hold in Bus Modes 3 and 4) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed.

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4.35 DMA Mode Register (DMODE) (continued)

4.35.2 Bit 5-4 - FC2-1

To perform cache line bursts, these bits must be set to 4, 8 or 16 transfers and cache bursting must be enabled (by clearing the CDIS bit (bit 7) in the CTEST0 register).

The SYM53C770 inserts a "fairness delay" of exactly 5 CLKs between bus ownerships. This gives the CPU and other bus master devices the opportunity to access memory between bursts.

The fairness timer has been modified in the SYM53C770 to improve DMA transfer rates while still allowing other DMA masters to gain access to the bus. In the SYM53C720, the fairness delay was 5-8 CLKs. In the SYM 53C770, the fairness delay is fixed at 5 CLKs. Bit 5-4 FCZ-1 (Function code) (Bus Modes 1, 3 and 4), or TMZ-1 (Transfer Modifier) (Bus Mode 2)

These bits, along with bit 6 in the DCNTL register (Bus Mode), define the function of the FC2-1 TM2-1 signals as illustrated in Table 4-3.

Table 4-16: FC2-1_TM2-1 Pin Function

DCNT bit 6	DMODE bits 5-4	FC2-1_TM2-1 Pin Function
0	00	User defined. The value of bits 5-4 correspond directly to the signal pins (FC2-1_TM2-1). The values of these bits are asserted onto the device pins during bus mastership.
0	01	
0	10	
0	11	
1	00	FC2_TM2 becomes a Preview of Address input signal used to tell the SYM53C770 that the system is ready for the next address value. FC1-TM1 is an output that is always asserted.
1	01	
1	10	
1	11	

4.35.3 Bit 3 - PD (Program/data)

This bit effects the function of the FC0 TM0 pin. It works in conjunction with the Bus Mode bit (bit 6 of the DCNTL register), as shown in Table 4-3. When the Bus Mode bit is not set, the SYM53C770 can store SCRIPTS routines and data in separate memory banks. When the Bus Mode bit is set, the SYM53C770 performs the same function as the $\overline{DC}$ signal that is commonly found in Intel processors.

Table 4-17: FC2-0_TM0 Pin Function

DCNTL bit 6	DMODE bits 3	FC0_TM0 Pin Function
0	0	Driven high when data is moved to or from memory
0	1	Driven low when fetching instructions from memory. This is only done during instruction fetch cycles
1	0	Driven high when the SYM53C770 is bus master, indication that data space is being accessed. When the SYM53C770 is not bus master, FC0_TM0 is tristated.
1	1	Driven low, indicating that control space is being accessed.

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4.35 DMA Mode Register (DMODE) (continued)

4.35.4 Bit 2 - FAM (Fixed address mode)

When the Fixed Address Mode bit is set, the address pointer in the DNAD register is disabled and will not increment after each data transfer. If this bit is clear, the pointer increments after each data transfer. The fixed address mode feature is used to transfer data to or from a fixed port address. This port width must be 32 bits and longword-aligned. Setting this bit does not affect SCRIPTS fetching instructions; only data transfer instructions are affected. In fixed address mode, if a SCSI interrupt occurs while the SYM53C770 is receiving data, the data must be flushed manually.

Once the interrupt occurs (within the chip), the DMA FIFO Empty bit (bit 7 in the DSTAT register) may not 4ave been set w4en reading the DMA Status register (DSTAT). At this point, the user may clear the DMA FIFO by writing to the Clear DMA FIFO bit (bit 2) in the CTEST3 register and setting the CSF (Clear SCSI FIFO) bit, bit 1 in the STEST3 register. The Block Move instruction may now be restarted. Instead of clearing the FIFO, it may be flushed, This is done as follows:

1) Reset the FAM bit

2) Load the DMA Next Address register (DNAD) with a valid memory address

3) Write to the Flush DMA FIFO bit (bit 3) in the CTEST3 register; 4) set the FAM bit again.

The Block Move instruction may now be restarted, assuming the byte count and address have been updated.

4.35.5 Bit 1 - UOITTO (User programmable transfer type)

In all bus modes, $\overline{\text{UPSO- TTO}}$ is a general purpose output pin. The value in the register bit is asserted onto the $\overline{\text{UPSO- TTO}}$ pin while the SYM53C720 is a bus master. The TT1 bit is in CTESTO.

4.35.6 Bit 0 - MAN (Manual start mode)

Setting this bit disables the SYM53C770 from automatically fetc4ing and executing SCSI SCRIPTS after the DSP register is written. When the Start DMA bit in the DCNTL register is cleared, the chip is running in normal mode. Once the Start DMA bit in the DCNTL register is set, the SYM53C770 automatically fetches and executes each instruction. Clearing this bit causes the SYM53C770 to automatically fetch and execute SCSI SCRIPTS after the DSP register is written.

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4.36 DMA Interrupt Enable Register (DIEN)

DMA Interrupt Enable Register (DIEN) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	RES	HPED	BF	ABRT	SSI	SIR	WTD	IID
Default	X	0	0	0	0	0	0	0

4.36.1 Bit 7 - Reserved

4.36.2 Bit 6 - HPED (Host parity error detected during DMA read or Slave write)

4.36.3 Bit 5 - BF (Bus fault)

4.36.4 Bit 4 - ABRT (Aborted)

4.36.5 Bit 3 - SSI (SCRIPTS step interrupt)

4.36.6 Bit 2 - SIR (SCRIPTS interrupt instruction received)

4.36.7 Bit 1 - WTD (Watchdog time-out detected)

4.36.8 Bit 0 - IID (Illegal instruction detected)

This register contains the interrupt enable bits corresponding to the interrupting conditions described in the DSTAT register. To mask an interrupt, clear the appropriate mask bit. Masking an interrupt prevents $\overline{\text{IRQ}}$ from being asserted for the corresponding interrupt, but the status bit will still be set in the DSTAT register. Masking an interrupt will not prevent the DIP bit (bit 0 in the ISTAT register) from being set. All DMA interrupts are considered fatal, therefore SCRIPTS will stop running when a DMA interrupt occurs, whether or not the interrupt is masked. Setting a mask bit enables the assertion of $\overline{\text{IRQ}}$ for the corresponding interrupt.

The SYM53C770 $\overline{\text{IRQ}}$ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the $\overline{\text{IRQ}}$ output is asserted will not cause $\overline{\text{IRQ}}$ to be deasserted. For more information on enabling interrupts, please refer to Chapter 2 of the *SYM53C770 Data Manual*.

4.37 DMA Watchdog Timer Register (DWT)

Read/Write

The DMA watchdog timer register provides a time-out mechanism during data transfers between the SYM53C770 and memory. This register determines the amount of time that the SYM53C770 will wait for the assertion of the $\overline{\text{STERM}}$- $\overline{\text{TA/READYIN}}$ signal after starting a bus cycle. Write the time-out value to this register during initialization. Every time that the SYM53C770 transfers data to/from memory, the value stored in this register is loaded into the counter. Disable the time-out feature by writing 00h to this register.

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4.37 DMA Watchdog Timer Register (DWT) (continued)

The unit time base for this register is 32* BCLK input period. For example, at 50 MHz the time base for this register is 32 * 20 ns = 640 ns. If a time-out of 50 µs is desired, then this register should be loaded with a value of 4Eh. The minimum time-out value that should be loaded into this register is 02h; the value 01h will not provide a reliable time-out period.

4.38 DMA Control Register (DCNTL)

DMA Control Register (DCNTL) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	STE	BSM	EA	SSM	BW16	STD	FA	COM
Default	0	0	0	0	0	0	0	0

4.38.1 Bit 7 - STE (Size Throttle Enable)

Asserting this bit causes the SYM53C770 to relinquish bus ownership every time the transfer size changes. When the size bits change from 01 (byte), 10 (word), or 00/11 (longword), the SYM53C770 will relinquish the bus and attempt to complete the transfer in succeeding cycles. The chip powers up with this bit disabled. The bit will be reset during a software or hardware reset. When cache line bursting is enabled, the SYM53C770 performs one transfer at a time until it reaches a cache line boundary. If this bit is set the snoop mode function of the SC0 pin, internal bus request, is not available.

4.38.2 Bit 6 - BSM (Bus Mode)

Setting this bit changes the function of the Function Code (FC2-0) or Transfer Modifier (TM2-0) pins. FC0 TM0 becomes a data control signal, FC1 TM1 becomes an output that is always asserted, and FC2 TM2 becomes an input to allow Preview of Address ($\overline{PA}$). For more information on the operation of this bit, refer to the descriptions of bits 5-3 in the DMODE register.

4.38.3 Bit 5 - EA (Enable ACK)

Setting this bit will cause the $\overline{STERM}$ ($\overline{TA}$ in Bus Mode 2, $\overline{ReadyIn}$ in Bus Modes 3 and 4) pin to become bidirectional, so the SYM53C770 will generate $\overline{STERM}$ during slave accesses. When this bit is clear, the SYM53C770 will monitor $\overline{STERM}$ to determine the end of a cycle. This bit takes effect during the cycle in which it is set; setting this bit must be the first I/O performed to the SYM53C770 if this feature is desired. This bit is not cleared with a software reset. Refer to the Bidirectional $\overline{STERM}$-$\overline{TA}$ section in Chapter 2, for more information on how this bit operates.

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4.38 DMA Control Register (DCNTL) (continued)

4.38.4 Bit 4 - SSM (Single-step mode)

Setting this bit causes the SYM53C770 to stop after executing each SCRIPTS instruction, and generate a SCRIPTS step interrupt. When this bit is clear the SYM53C770 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, this bit should be clear.

To restart the SYM53C770 after it generates a SCRIPTS Step interrupt, the ISTAT and DSTAT registers should be read to clear the interrupt and then the START DMA bit in this register should be set.

4.38.5 Bit 3 - BW16 (Host Bus Width Equal to 16)

When this bit is set, the SYM53C770 host interface will become 16 bits wide. This bit can only be set in Little Endian mode.



NOTE

Data lines 31-16 must be tied to data lines 15-0, respectively. Cache bursting is not available in this mode.

4.38.6 Bit 2 - STD (Start DMA operation)

The SYM53C770 fetches a SCSI SCRIPTS instruction from the address contained in the DSP register when this bit is set. This bit is required if the SYM53C770 is in one of the following modes:

1) Manual start mode

   Bit 0 in the DMODE register is set

2) Single-step mode

   Bit 4 in the DCNTL register is set when the SYM53C770 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the SYM53C770 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after a single-step interrupt.

4.38.7 Bit 1 - FA (Fast arbitration)

When this bit is set, the SYM53C770 becomes bus master after receiving a Bus Grant (HLDAI in Bus Modes 3 and 4), saving one clock cycle of arbitration time. When this bit is clear, the SYM53C770 will follow the normal arbitration sequence.

4.38.8 Bit 0 - COM (53C700 compatibility)

When this bit is clear, the SYM53C770 will be compatible with the 53C700. Selection/reselection IDs will be stored in the SSID and SFBR registers. When this bit is set, the ID is stored in the SSID register, protecting the SFBR from an overwrite if a selection/reselection occurs during a DMA register to register operation. The default condition of this bit (clear) causes the SYM53C770 to function as a 53C700.

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4.39 Adder Sum Output Register (ADDER)

This register contains the output of the internal adder and is used primarily for test purposes.

4.40 SCSI Interrupt Enable Zero Register (SIEN0)

SCSI Interrupt Enable Zero Register (SIEN0) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	M/A	CMP	SEL	ASL	SGE	UDC	RST	PAR
Default	0	0	0	0	0	0	0	0

This register contains the interrupt enable bits corresponding to the interrupting conditions described in the SIST0 register. To mask an interrupt, clear the appropriate mask bit. Masking an interrupt prevents $\overline{\text{IRQ}}$ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST0 register. Masking an interrupt will not prevent the ISTAT SIP bit from being set, except in the case of non-fatal interrupts (SEL, RSL, CMP, and M/A (target mode only). Setting a mask bit unmasks the corresponding interrupt, enabling the assertion of $\overline{\text{IRQ}}$ for that interrupt. A masked non-fatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking does not begin until either the SIP (bit 1) or DIP (bit 0) bit in the ISTAT register is set.

The SYM53C770 $\overline{\text{IRQ}}$ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the $\overline{\text{IRQ}}$ output is asserted will not cause $\overline{\text{IRQ}}$ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the SIP bit in the ISTAT register to clear and allow pending interrupts to fall through (interrupt stacking will be disabled). The bits in this register should not be toggled on or off during normal operation. They should be set or cleared during the initialization routine. For more information on interrupts, refer to Chapter 2 of the *SYM53C770 Data Manual*, "Functional Description."

4.40.1 Bit 7 MIA (SCSI Phase Mismatch - Initiator Mode; SCSI ATN Condition - Target Mode)

In initiator mode, this bit is set when the SCSI phase asserted by the target and sampled during REQ does not match the expected phase in the SOCL register. This expected phase is automatically written by SCSI transfer SCRIPTS. In target mode, this bit is set when the initiator has asserted ATN. See the Disable halt on parity error or ATN condition bit in the SCNTL1 register for more information on when this status is actually raised.

4.40.2 Bit 6 - CMP (Function Complete)

This bit is set when full arbitration and selection sequence has completed.

4.40.3 Bit 5 - SEL (Selected)

The SYM53C770 has been selected as a SCSI target device. The Enable response to selection bit in the SCID register must be set for this to occur.

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4.40 SCSI Interrupt Enable Zero Register (SIEN0) (continued)

4.40.4 Bit 4 - RSL (Reselected)

The SYM53C770 has been reselected as a SCSI initiator device. The Enable response to reselection bit in the SCID register must be set for this to occur.

4.40.5 Bit 3 - SGE (SCSI Gross Error)

The following conditions are considered SCSI Gross Errors:

1) Data underflow: the SCSI FIFO was read when no data was present.

2) Data overflow: the SCSI FIFO was written to while full.

3) Offset underflow: in target mode, an ACK pulse was received before the corresponding REQ was sent.

4) Offset overflow: in initiator mode, a REQ pulse was received which caused the maximum offset (Defined by the MO3-0 bits in the SXFER register) to be exceeded.

5) In initiator mode, a phase change occurred with an outstanding REQ/ ACK offset.

6) Residual data in SCSI FIFO: a transfer other than synchronous data receive was started with data left in the SCSI synchronous receive FIFO.

4.40.6 Bit 2 - UDC (Unexpected Disconnect)

This condition only occurs in initiator mode. It happens when the target to which the SYM53C770 is connected disconnects from the SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCNTL2 register for more information on expected versus unexpected disconnects. Any disconnect in low level mode causes this condition.

4.40.7 Bit 1 - RST (SCSI Reset Condition)

The SCSI RST signal has been asserted by the SYM53C770 or any other SCSI device. Note that this condition is edge-triggered so that multiple interrupts cannot occur because of a single RST pulse.

4.40.8 Bit 0 - PAR (SCSI Parity Error)

The SYM53C770 detected a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or ATN Condition bits in the SCNTL1 register for more information on when this condition will actually be raised.

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4.41 SCSI Interrupt Enable One Register (SIEN1)

SCSI Interrupt Enable One Register (SIEN1) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved					STO	GEN	HTH
Default	X	X	X	X	X	0	0	0

This register contains the interrupt enable bits corresponding to the interrupting conditions described in the SIST1 register. To mask an interrupt, clear the appropriate mask bit. Masking an interrupt prevents $\overline{IRQ}$ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST1 register. Masking an interrupt will not prevent the SIP bit (bit 1) in the ISTAT register from being set. Setting a mask bit un-masks the corresponding interrupt, enabling the assertion of $\overline{IRQ}$ for that interrupt. A masked non-fatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking does not begin until either the DIP (bit 0) or SIP (bit 1) bit in the ISTAT register is set. The SYM53C770 $\overline{IRQ}$ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the $\overline{IRQ}$ output is asserted will not cause $\overline{IRQ}$ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the SIP bit (bit 1) in the ISTAT register to clear and allow pending interrupts to fall through (interrupt stacking will be disabled). The bits in this register should not be toggled on or off during normal operation. They should be set or cleared during the initialization routine.

4.41.1 Bits 7-3 - Reserved

4.41.2 Bit 2 - STO (Selection or Reselection Time-out)

This bit is set when the SCSI device which the SYM53C770 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the STIME0 register bits 3-0 for more information on the time-out timer.

4.41.3 Bit 1 - GEN (General Purpose Timer Expired)

This bit is set when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

4.41.4 Bit 0 - HTH (Handshake to Handshake Timer Expired)

This bit is set when the handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

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4.42 SCSI Interrupt Status Zero Register (SIST0)

SCSI Interrupt Status Zero Register (SIST0) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
Default	0	0	0	0	0	0	0	0

Reading the SIST0 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN0 register or not. Each bit asserted indicates that the corresponding condition has occurred. Reading the SIST0 will reset the selected conditions. The SIP bit in the ISTAT register will be cleared after both SIST0 and SIST1 are read. Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the SYM53C770 stacks interrupts). SCSI interrupt conditions may be individually masked through the SIEN0 register. When performing consecutive 8-bit reads of the DSTAT, SIST0, and SIST1 registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. To avoid missing a SCSI interrupt while reading any of these registers when the ISTAT SIP and DIP bits may not be set, read SIST0 and SIST1 before DSTAT. For more information on interrupts, refer to Chapter Two, Functional Description.

4.42.1 Bit 7 - M/A (Initiator Mode: Phase Mismatch; Target Mode: $\overline{\text{ATN}}$ Active)

In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when $\overline{\text{REQ}}$ is asserted by the target. In target mode, this bit is set when the $\overline{\text{ATN}}$ signal is asserted by the initiator. This status bit is used in diagnostics testing or in low level mode. It is set in low level mode any time there is a phase change.

4.42.2 Bit 6 - CMP (Function Complete)

This bit is set when full arbitration and selection sequence has completed.

4.42.3 Bit 5 - SEL (Selected)

This bit is set when the SYM53C770 is selected by another SCSI device. The enable response to selection bit must have been set in the SCID register for the SYM53C770 to respond to selection attempts.

4.42.4 Bit 4 - RSL (Reselected)

This bit is set when the SYM53C770 is reselected by another SCSI device. The Enable Response to Reselection bit must have been set in the SCID register for the SYM53C770 to respond to reselection attempts.

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4.42 SCSI Interrupt Status Zero Register (SIST0) (continued)

4.42.5 Bit 3 - SGE (SCSI Gross Error)

This bit is set when the SYM53C770 encounters a SCSI Gross Error Condition. The following conditions can result in a SCSI Gross

Error Condition:

1) Data Underflow - the SCSI FIFO register was read when no data was present.

2) Data Overflow - too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.

3) Offset Underflow - the SYM53C770 is operating in target mode and an $\overline{\text{ACK}}$ pulse is received when the outstanding offset is zero.

4) Offset Overflow - the other SCSI device sent a $\overline{\text{REQ}}$ or $\overline{\text{ACK}}$ pulse with data which exceeded the maximum synchronous offset defined by the SXFER register.

5) Residual data in the Synchronous data FIFO - a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.

6) A phase change occurred with an outstanding synchronous offset when the SYM53C770 was operating as an initiator.

4.42.6 Bit 2 - UDC (Unexpected Disconnect)

This bit is set when the SYM53C770 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the SYM53C770 is an initiator. When the SYM53C770 operates in low level mode, any disconnect will cause an interrupt, even a valid SCSI disconnect. This bit will also be set if a selection time-out occurs (it may occur before, at the same time, or stacked after the STO interrupt, since this is not considered an expected interrupt).

4.42.7 Bit 1 - RST (SCSI RSTI Received)

This bit is set when the SYM53C770 detects an active $\overline{\text{RST}}$ signal, whether the reset was generated external to the chip or caused by the Assert $\overline{\text{RST}}$ bit in the SCNTL1 register. This SYM53C770 SCSI reset detection logic is edge-sensitive so that multiple interrupts will not be generated for a single assertion of the SCSI $\overline{\text{RST}}$ signal.

4.42.8 Bit 0 - PAR (Parity Error)

This bit is set when the SYM53C770 detects a parity error when receiving or sending SCSI data. The Enable Parity Checking bit (bit 3 in the SCNTL0 register) must be set for this bit to become active. A parity error can occur when receiving data from the SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SODL register. A parity error can occur from the host bus only if Pass Through parity is enabled (bit 3 in the SCNTL0 register = 1, bit 2 in the SCNTL0 register = 0).

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4.43 SCSI Interrupt Status One Register (SIST1)

SCSI Interrupt Status One Register (SIST1) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved					STO	GEN	HTH
Default	X	X	X	X	X	0	0	0

Reading the SIST1 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN1 register or not. Each bit that is set indicates that the corresponding condition has occurred. Reading this register will reset the selected conditions, and will reset the SIST1 register. The SIP bit in the ISTAT register will be cleared after both SIST0 and SIST1 are read.

4.43.1 Bits 7-3 Reserved Bit 2 STO (Selection or Reselection Time-out)

The SCSI device which the SYM53C770 was attempting to select or reselect did not respond within the programmed time-out period (See the description of the STIME0 register, bits 3-0, for more information on the time-out timer). After the SYM53C770 has won arbitration, it waits for selection or reselection. When selected, it fetches the next instruction from the address pointed to by the DSP register. The SCRIPTS routine can then execute the next instruction before the selection has completed. The chip will continue executing SCRIPTS until it encounters an interrupt, or a SCRIPTS instruction that requires it to respond.

4.43.2 Bit 1 - GEN (General Purpose Timer Expired)

The general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

4.43.3 Bit 0 - HTH (Handshake-to-Handshake Timer Expired)

The handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

4.44 SCSI Longitudinal Parity Register (SLPAR)

The SLPAR register consists of two multiplexed bytes; other register bit settings determine what is displayed at this memory location at any given time. When bit 5 in the SCNTL2 (SLPMD) register is cleared, the chip XORs the high and low bytes of the SLPAR register together to give a single-byte value which is displayed in the SLPAR register. If the SLPMD bit is set, then the SLPAR register shows either the high byte or the low byte of the SLPAR word. The SLPAR High Byte Enable bit, SCNTL2 bit 4, determines which byte of the SLPAR register is visible on the SLPAR register at any given time. If this bit is cleared, the SLPAR register contains the low byte of the SLPAR word; if it is set, the SLPAR register contains the high byte of the SLPAR word. This register performs a bytewise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SLPAR should go to zero (assuming it started at zero).

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4.44 SCSI Longitudinal Parity Register (SLPAR) (continued)

As an example, suppose that the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active-high):

Table 4-18: SCSI Longitudinal Parity

Data/Check Bytes	Running SLPAR	Comments
-	00000000	SLPAR initialized to zero
1. 11001100 (Data)	11001100	XOR data byte with SLPAR, place result in SLPAR
2. 01010101 (Data)	10011001	XOR data byte with SLPAR, place result in SLPAR
3. 00001111 (Data)	10010110	XOR data byte with SLPAR, place result in SLPAR
4. 10010110 (Check)	00000000	XOR check byte with SLPAR, place resulting SLPAR. The result should be zeros; a one in any bit position indicates a transmission error.

The SLPAR register can also be used to generate the check bytes for SCSI send operations. If the SLPAR register contains all zeros prior to sending a block move, it will contain the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus. Writing any value to this register resets it to zero. The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances.

4.45 SCSIWide Residue Data Register (SWIDE)

After a wide SCSI data receive operation, this register will contain a residual data byte if the last byte received was never sent across the DMA bus. It represents either the first data byte of a subsequent data transfer, or it is a residue byte which should be cleared when an Ignore Wide Residue message is received. It may also be an overrun data byte.

4.46 Memory Access Control Register (MACNTL)

Memory Access Control Register (MACNTL) - Read/Write

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	TYP3	TYP2	TYP1	TYP0	DataWR	DataRD	PSCRIPT	SCRIPT
Default	X	X	X	X	0	0	0	0

MACNTL is used to determine if an external access is to local or far memory.

4.46.1 Bits 7-4 TYP3-0 (Chip Type)

These bits identify the chip type for software purposes.

Table 4-19: SCSI Chip Identification

Bits 7654	Chip Type
0000	720
0001	720SE
0010	770

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4.46 Memory Access Control Register (MACNTL) (continued)

4.46.2 Bits 3-0

These bits are used to define if a data write, data read, pointer to a SCRIPTS fetch and a SCRIPTS fetch, respectively, are considered local memory accesses. If any of the bits are set, the access will be considered local. The bits power up cleared, indicating far memory. Internal logic will determine if the specific transfer is considered local or far. The $\overline{\text{MAC}}$ signal, pin 26 (also referred to as the near/far pin), will be asserted high when the transfer is to local memory. Assuming the SCRIPTS fetch bit is set, the near/far pin will not be affected until completion of the next Transfer Control instruction. Changes to the $\overline{\text{MAC}}$ signal will be available at the pin at the same time the Bus Request pin is asserted.

4.47 General Purpose Control Register (GPCNTL)

General Purpose Control Register (GPCNTL) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved			GPIO en 4	GPIO en3	GPIO en2	GPIO en1	GPIO en0
Default	X	X	X	0	1	1	1	1

GPCNTL is used to determine if the pins controlled by the General Purpose register (GPREG, address 07 (04)h) are inputs or outputs.

4.47.1 Bits 7-5 - Reserved

4.47.2 Bit 4 - GPIO en4 (General Purpose Output Enable 4)

GPCNTL, corresponding to bit 4 in the GPREG register and pin 43, powers up as a general purpose output.

4.47.3 Bits 3-0 - GPIO en3-0 (General Purpose Output Enable 3-0)

Bits 3-0 in GPCNTL, corresponding to bits 3-0 in the GPREG register and pins 39-42, power up as general purpose inputs. If any of the bits are cleared, this indicates an output and if any of the bits are set this indicates an input. When the bits are enabled as inputs, an internal pullup is also enabled.

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4.48 SCSITimer Register 0 (STIME0)

SCSITimer Register 0 (STIME0) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	HTH3	HTH2	HTH1	HTH0	SEL3	SEL2	SEL1	SEL0
Default	0	0	0	0	0	0	0	0

4.48.1 Bits 7-4 - HTH (Handshake-to-Handshake Timer Period)

These bits select Handshake-to-Handshake Time-out Period, the maximum time between SCSI handshakes (REQ to REQ in target mode, or ACK to ACK in initiator mode). When this timing is exceeded, the HTH bit in the SIST1 register is set, and an interrupt is optionally generated, if bit 0 in the SIEN1 register is set.

The following table applies to the Handshake-to-Handshake Timer and the General Purpose Timer (STIME1 bits 3-0).

Table 4-20: Handshake-to-Handshake Timer Period

HTH 7-4, GEN 3-0	Minimum Time-out w/o scale factor bit set (50 MHz CLK)	Minimum Time-out with scale factor bit set (50 MHz CLK)
0000	Disabled	Disabled
0001	100 µs	1.6 ms
0010	200 µs	3.2 ms
0011	400 µs	6.4 ms
0100	800 µs	12.8 ms
0101	1.6 ms	25.6 ms
0110	3.2 ms	51.2 ms
0111	6.4 ms	102.4 ms
1000	12.8 ms	204.8 ms
1001	25.6 ms	409.6 ms
1010	51.2 ms	819.2 ms
1011	102.4 ms	1.6 sec
1100	204.8 ms	3.2 sec
1101	409.6 ms	6.4 sec
1110	819.2 ms	12.8 sec
1111	1.6 sec	25.6 sec

4.48.2 Bits 3-0 - SEL (Selection Time-out Period)

These bits select the SCSI selection/reselection time-out period. When this timing (plus the 200 µs selection abort time) is exceeded, the STO bit in the SIST1 register is set. An interrupt is optionally generated, if bit 2 in the SIEN1 register is set.

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4.49 SCSITimer Register One (STIME1)

SCSITimer Register One (STIME1) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	RES	HTHBA	CENSF	HTHSF	GEN3	GEN2	GEN1	GEN0
Default	X	0	0	0	0	0	0	0

4.49.1 Bits 7 - Reserved

4.49.2 Bit 6 - Handshake-to-Handshake Timer Bus Activity Enable Bit (HTHBA)

Setting this bit causes this timer to begin testing for SCSI request/acknowledge activity as soon as SCSI busy is asserted regardless of the agents participating in the transfer.

4.49.3 Bit 5 - General Purpose Timer Scale Factor Bit (GENSF)

4.49.4 Bit 4 - Handshake-to-Handshake Timer Scale Factor Bit (HTHSF)

Setting these bits cause the timer to shift by a factor of 16.

4.49.5 Bits 3-0 - GEN3-0 (General Purpose Timer Period)

These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the SIST1 register is set and an interrupt is optionally generated, if bit 1 in the SIEN1 register is set. Refer to the table under STIME0, bits 3-0, for the available time-out periods.

4.50 Response ID Zero Register (RESPID0)

Read/Write

4.51 Response ID One Register (RESPID1)

Read/Write

RESPID0 and RESPID1 contain the selection or reselection IDs. In other words, these two 8-bit registers contain the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit of RESPID1 representing ID 15 and the least significant bit of RESPID0 representing ID 0. The SCID register still contains the chip ID used during arbitration. The chip can respond to more than one ID because more than one bit can be set in the RESPID1 and RESPID0 registers. However, the chip can arbitrate with only one ID value in the SCID register.

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4.52 SCSITest Register Zero (STEST0)

SCSITest Register Zero (STEST0) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	SSAID				SLT	ART	SOZ	SOM
Default	X	X	X	X	0	X	1	1

4.52.1 Bits 7-4 - SSAID (SCSI Selected ASID)

These bits are read only and contain 4 bits that encode the possible 0-15 ID's the SYM53C770 can be selected as. During the selection phase, when a valid ID is put on the bus, and the SYM53C770 responds to that ID as the ID it was selected as, this ID is written into the SSAID register.

4.52.2 Bit 3 - SLT (Selection Response Logic Test)

This bit is asserted when the SYM53C770 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.

4.52.3 Bit 2 - ART (Arbitration Priority Encoder Test)

This bit will always be asserted when the SYM53C770 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing, but it may be used during low level mode operation to determine if the SYM53C770 has won arbitration.

4.52.4 Bit 1 - SOZ (SCSI Synchronous Offset Zero)

This bit indicates that the current synchronous SCSI REQ/ACK offset is zero. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set, the SYM53C770, as an initiator, is waiting for the target to request data transfers. If the SYM53C770 is a target then the initiator has sent the offset number of acknowledges.

4.52.5 Bit 0 - SOM (SCSI Synchronous Offset Maximum)

This bit indicates that the current synchronous SCSI REQ/ACK offset is the maximum specified by bits 3-0 in the SCSITransfer register. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set the SYM53C770, as a target, is waiting for the initiator to acknowledge the data transfers. If the SYM53C770 is an initiator then the target has sent the offset number of requests.

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4.53 SCSITest Register One (STEST1)

SCSITest Register One (STEST1) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved				DBLEN	DBLSEL	SFP1	SFP0
Default	X	X	X	X	0	0	X	X

4.53.1 Bits 7-4 - Reserved

4.53.2 Bit 3 - SCLK Doubler Enable (DBLEN)

Set this bit to bring the SCSI clock doubler out of the powered-down state. The default value of this bit is clear (SCSI clock doubler powered down). Set bit 2 after setting this bit, to double the SCLK frequency.

4.53.3 Bit 2 - SCLK Doubler Select (DBLSEL)

Set this bit after powering up the SCSI clock doubler to double The SCLK frequency. This bit has no effect unless bit 3 is set.

4.53.4 Bits 1-0 - SFP1-0 (SCSI FIFO Parity)

These bits represent the parity that is read from the SCSI FIFO byte lanes during test access through the SODL register. To read the SCSI FIFO in test mode, read these bits after reading the SODL register. SFP1 represents parity for the most significant byte and SFPO represents parity for the least significant byte. See the description of the SCSI FIFO Test Mode bit in the STEST3 register for more information on testing the SCSI FIFO. Doubling the SCSI CLK Frequency The SYM53C770 SCSI clock doubler doubles a 40-50 MHz SCSI clock, increasing the frequency to 80-100 MHz. Follow these steps to use the clock doubler:

1) Set the SCLK Doubler Enable bit (STEST1, bit 3)

2) Wait 20 μs

3) Halt the SCSI clock by setting the Halt SCSI Clock bit (STEST3 bit 5)

4) Set the clock conversion factor using the SCF and CCF fields in the SCNTL3 register

5) Set the SCLK Doubler Select bit (STESTl, bit2)

6) Clear the Halt SCSI Clock bit

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4.54 SCSITest Register Two (STEST2)

SCSITest Register Two (STEST2) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	SCE	ROF	DIF	SLB	SZM	AWS	EXT	LOW
Default	0	0	0	0	0	0	0	0

4.54.1 Bit 7 - SCE (SCSI Control Enable)

Setting this bit allows all SCSI control and data lines to be asserted through the SOCL and SODL registers regardless of whether the SYM53C770 is configured as a target or initiator.



NOTE

This bit should not be set during normal operation, since it could cause contention on the SCSI bus. It is included for diagnostic purposes only.

4.54.2 Bit 6 - ROF (Reset SCSI Offset)

Setting this bit clears any outstanding synchronous SCSI REQ/ACK offset. This bit should be set if a SCSI gross error condition occurs, to clear the offset when a synchronous transfer does not complete successfully. The bit automatically clears itself after resetting the synchronous offset.

4.54.3 Bit 5 - DIF (SCSI Differential Mode)

Setting this bit allows the SYM53C770 to interface properly to external differential transceivers. Its only real effect is to tristate the BSY, SEL, and RST pads so they can be used as pure inputs. Clearing this bit enables single ended mode operation. This bit should be set in the initialization routine if the differential pair interface is to be used.

4.54.4 Bit 4 - SLB (SCSI Loopback Mode)

Setting this bit allows the SYM53C770 to perform SCSI loopback diagnostics. That is, it enables the SCSI core to simultaneously perform as both initiator and target.

4.54.5 Bit 3 - SZM (SCSI High-Impedance Mode)

Setting this bit places all open-drain 48 mA SCSI drivers to a high-impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.

4.54.6 Bit 2 - AWS (Always Wide SCSI)

When this bit is set, all SCSI information transfers will be done in 16-bit wide mode. This includes data, message, command, status and reserved phases. This bit should normally be deasserted since 16-bit wide message, instruction, and status phases are not supported by the SCSI specifications. This bit is not guaranteed to function properly with future SCSI specifications.

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4.54 SCSITest Register Two (STEST2) (continued)

4.54.7 Bit 1 - EXT (Extend REQIACK Filtering)

The SCSI core contains a special digital filter on the REQ and ACK pins which will disregard glitches on deasserting edges. Asserting this bit will increase the filtering period from 30ns to 60ns on the deasserting edge of the REQ and ACK signals.



NOTE

This bit must never be set during fast SCSI (> 5M transfers per second) operations, because a valid assertion could be treated as a glitch.

4.54.8 Bit 0 - LOW (SCSI Low level Mode)

Setting this bit places the SYM53C770 in low level mode. In this mode, no DMA operations can occur, and no SCRIPTS instructions can be executed. Arbitration and selection may be performed by setting the start sequence bit as described in the SCNTL0 register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.



NOTE

It is not necessary to set this bit for access to the SCSI bit-level registers (SODL, SBCL, and input registers). This bit must be clear for the chip to properly respond to selection or reselection.

4.55 SCSITest Register Three (STEST3)

SCSITest Register Three (STEST3) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	TE	STR	HSC	DSI	S16	TTM	CSF	FTM
Default	X	X	0	0	0	0	0	0

4.55.1 Bit 7 - TE (TolerANT Enable)

Asserting this bit enables TolerANT Active Negation. TolerANT causes the SCSI Request, Acknowledge, Data, and parity signals to be actively deasserted, in addition to relying on external pullups when the SYM53C770 is driving these signals. Active deassertion of these signals will occur only when the SYM53C770 is in an information transfer phase. When operating in a differential environment or at fast SCSI timings, Active Negation should be enabled to improve setup and deassertion times. Active Negation is disabled after chip or software reset, or when this bit is cleared.

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4.55 SCSITest Register Three (STEST3) (continued)

4.55.2 Bit 6 - STR (SCSI FIFO Test Read)

Setting this bit places the SCSI core into a test mode in which the SCSI FIFO can be easily read. Reading the least significant byte of the SODL register will cause the FIFO to unload. The functions are summarized in the table below.

Table 4-21: SCSI FIFO Test Read

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Read	15-0	Unload
SODL0	Read	7-0	Unload
SODL1	Read	15-8	None

4.55.3 Bit 5 - HSC (Halt SCSI Clock)

Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit may be used for test purposes or to lower I_{DD} during a power down mode.

4.55.4 Bit 4 - DSI (Disable Single Initiator Response)

If this bit is set, the SYM53C770 will ignore all bus-initiated selection attempts which employ the single-initiator option from SCSI-1. In order to select the SYM53C770 while this bit is set, the SYM53C770's SCSI ID and the initiator's SCSI ID must both be asserted. This bit should be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response. This bit works in conjunction with the VAL bit in the SSID register.

4.55.5 Bit 3 - S16 (16-bit System)

If this bit is set, all devices in the SCSI system implementation are assumed to be 16 bits. This causes the SYM53C770 to always check the parity bit for SCSI IDs 15-8 during bus-initiated selection or reselection, assuming parity checking has been enabled. If an 8-bit SCSI device attempts to select the SYM53C770 while this bit is set, the SYM53C770 will ignore the selection attempt, because the parity bit for IDs 15-8 will be undriven. See the description of the Enable Parity Checking bit in the SCNTL0 register for more information.

4.55.6 Bit 2 - TTM (Timer Test Mode)

Asserting this bit facilitates testing of the selection time-out, general purpose, and handshake-to-handshake timers by greatly reducing all three time-out periods. Setting this bit starts all three timers and if the respective bits in the SIEN1 register are asserted, the SYM53C770 will generate interrupts at time-out.

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4.56 SCSI Bus Data Lines Register (SBDL)

Read Only

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high (enabled when the bits are set). The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data via programmed I/O. This register can also be used for diagnostic testing or in low level mode.

4.57 Scratch Register B (SCRATCHB)

Read/Write

This is a general purpose, user definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves directed at the SCRATCHB register will alter its contents. If the internal SCRIPTS RAM is enabled using the indexed addressing method, a shadowed version of this register is used to address 128 blocks of 32-byte segments of the SCRIPTS RAM. Each 32-byte block of data is loaded into the SCRATCHC-J registers.

4.58 Scratch Registers C-J (SCRATCHC-J)

Read/Write

These are general purpose, user definable scratch pad registers. They are accessible through read/modify/write instructions and are defined as SCRATCHC through SCRATCHJ. When the indexed addressing method is used to enable and access the internal SCRIPTS RAM, the SCRIPTS RAM replaces these registers and can optionally be used as a block of scratchpad RAM. For more information on this and other methods of implementing the SCRIPTS RAM, see Chapter 2 of the *SYM53C770 Data Manual*.

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Chapter 5: TL16C550A Registers

5.1 General Information

This section presents address maps for UART resources available on the Model 4260 for each type of MIX baseboard available from Pentek. Refer to Chapter 3 and Pentek's MIX Tutorial for VMEbus Systems (P/N 800.00001) for more information on how to access these resources.

5.1.1 Using Model 4200, 4200A, 4201 and 4201A MIX Baseboards

Table 5-1 gives the physical addresses, in the memory space of the 68030 processor on any of these four baseboards, that correspond to the symbolic names used to represent the Model 4260's UART resources.

Table 5-1: Memory Map of UART Resources - Model 4200, 4200A, 4201, 4201A MIX Baseboards

Resource/Name	Symbolic Name	4200/01 68030 Address	Access
Receiver Buffer Register	RBR	MIX_base+0x0800 003C	Read Only
Transmitter Holding Reg.	THR	MIX_base+0x0800 003C	Write Only
Interrupt Enable Register	IER	MIX_base+0x0800 0038	Read/Write
Interrupt ID Register	IIR	MIX_base+0x0800 0034	Read Only
Line Control Register	LCR	MIX_base+0x0800 0030	Read/Write
Modem Control Register	MCR	MIX_base+0x0800 002C	Read/Write
Line Status Register	LSR	MIX_base+0x0800 0028	Read/Write
Modem Status Register	MSR	MIX_base+0x0800 0024	Read/Write
Scratch Register	SCR	MIX_base+0x0800 0020	Read/Write
Divisor Latch (lsb)	DLL	MIX_base+0x0800 003C	Read/Write
Divisor Latch (msb)	DLM	MIX_base+0x0800 0038	Read/Write

MIX_base Address:
If 4260 is in MIX position 0, MIX_base = 0xC000 0000
If 4260 is in MIX position 1, MIX_base = 0xD000 0000
If 4260 is in MIX position 2, MIX_base = 0xE000 0000

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5.1 General Information (continued)

5.1.2 Using the Model 4202 MIX Baseboard

Table 5-2, below, presents the slave memory map of UART resources for a Model 4260 installed on a Model 4202 Baseboard, assuming direct addressing, A32 or A24 operation, and that nothing has been written to the 4202's VME Address Register.

Table 5-2: Memory Map of UART Resources - Model 4202 MIX Baseboard

Resource/Name	Symbolic Name	VMEbus Address*	Access
Receiver Buffer Register	RBR	MIX_base+0x0800 003C	Read Only
Transmitter Holding Reg.	THR	MIX_base+0x0800 003C	Write Only
Interrupt Enable Register	IER	MIX_base+0x0800 0038	Read/Write
Interrupt ID Register	IIR	MIX_base+0x0800 0034	Read Only
Line Control Register	LCR	MIX_base+0x0800 0030	Read/Write
Modem Control Register	MCR	MIX_base+0x0800 002C	Read/Write
Line Status Register	LSR	MIX_base+0x0800 0028	Read/Write
Modem Status Register	MSR	MIX_base+0x0800 0024	Read/Write
Scratch Register	SCR	MIX_base+0x0800 0020	Read/Write
Divisor Latch (lsb)	DLL	MIX_base+0x0800 003C	Read/Write
Divisor Latch (msb)	DLM	MIX_base+0x0800 0038	Read/Write

Default MIX_base Address:

If 4260 is in MIX position 0, MIX_base = 0x0000 0000 for A32, or 0x00 0000 for A24
If 4260 is in MIX position 1, MIX_base = 0x1000 0000 for A32, or 0x10 0000 for A24
If 4260 is in MIX position 2, MIX_base = 0x2000 0000 for A32, or 0x20 0000 for A24

*** - in A24 space, access at 0x08 0zzz**

5.1.3 Using the Model 4283 MIX Baseboard

One the module has been selected, the UART resources of the Model 4260 appear in the TMS320C30 address map according to Table 5-3. Accessing these registers is accomplished by simply reading and writing these locations.

Table 5-3: Memory Map of UART Resources - Model 4283 MIX Baseboard

Resource/Name	Symbolic Name	4283 'C30 Address	Access
Receiver Buffer Register	RBR	0x80 400F	Read Only
Transmitter Holding Reg.	THR	0x80 400F	Write Only
Interrupt Enable Register	IER	0x80 400E	Read/Write
Interrupt ID Register	IIR	0x80 400D	Read Only
Line Control Register	LCR	0x80 400C	Read/Write
Modem Control Register	MCR	0x80 400B	Read/Write
Line Status Register	LSR	0x80 400A	Read/Write
Modem Status Register	MSR	0x80 4009	Read/Write
Scratch Register	SCR	0x80 4008	Read/Write
Divisor Latch (lsb)	DLL	0x80 400F	Read/Write
Divisor Latch (msb)	DLM	0x80 400E	Read/Write

To access the Model 4260's registers, MXA27 must be driven high by setting bit 17 in the Model 4283's Page Address Register.

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5.1 General Information (continued)

5.1.4 Using the Model 4284 MIX Baseboard

Table 5-4 presents the memory map for UART resources on the Model 4260, as seen by the 'C40 processor on the Model 4284 Baseboard.

Table 5-4: Memory Map of UART Resources - Model 4284 MIX Baseboard

Resource/Name	Symbolic Name	4284 'C40 Address	Access
Receiver Buffer Register	RBR	MIX_base+0x0200 000F	Read Only
Transmitter Holding Reg.	THR	MIX_base+0x0200 000F	Write Only
Interrupt Enable Register	IER	MIX_base+0x0200 000E	Read/Write
Interrupt ID Register	IIR	MIX_base+0x0200 000D	Read Only
Line Control Register	LCR	MIX_base+0x0200 000C	Read/Write
Modem Control Register	MCR	MIX_base+0x0200 000B	Read/Write
Line Status Register	LSR	MIX_base+0x0200 000A	Read/Write
Modem Status Register	MSR	MIX_base+0x0200 0009	Read/Write
Scratch Register	SCR	MIX_base+0x0200 0008	Read/Write
Divisor Latch (lsb)	DLL	MIX_base+0x0200 000F	Read/Write
Divisor Latch (msb)	DLM	MIX_base+0x0200 000E	Read/Write

MIX_base Address:
If 4260 is in MIX position 0, MIX_base = 0x2000 0000
If 4260 is in MIX position 1, MIX_base = 0x2400 0000
If 4260 is in MIX position 2, MIX_base = 0x2800 0000

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5.1 General Information (continued)

5.1.5 Using the Model 4285 MIX Baseboard

Table 5-5 presents the memory map for UART resources on the Model 4260, as seen by the 'C40 processor on the Model 4284 Baseboard.

Table 5-5: Memory Map of UART Resources - Model 4285 MIX Baseboard

Resource/Name	Symbolic Name	4285 'C40 Address	Access
Receiver Buffer Register	RBR	MIX_base+0x0200 000F	Read Only
Transmitter Holding Reg.	THR	MIX_base+0x0200 000F	Write Only
Interrupt Enable Register	IER	MIX_base+0x0200 000E	Read/Write
Interrupt ID Register	IIR	MIX_base+0x0200 000D	Read Only
Line Control Register	LCR	MIX_base+0x0200 000C	Read/Write
Modem Control Register	MCR	MIX_base+0x0200 000B	Read/Write
Line Status Register	LSR	MIX_base+0x0200 000A	Read/Write
Modem Status Register	MSR	MIX_base+0x0200 0009	Read/Write
Scratch Register	SCR	MIX_base+0x0200 0008	Read/Write
Divisor Latch (lsb)	DLL	MIX_base+0x0200 000F	Read/Write
Divisor Latch (msb)	DLM	MIX_base+0x0200 000E	Read/Write

MIX_base Address for Expansion Bus:
If Model 4260 is in MIX position 0, MIX_base = 0x9000 0000
If Model 4260 is in MIX position 1, MIX_base = 0x9020 0000
If Model 4260 is in MIX position 2, MIX_base = 0x9040 0000

MIX_base Address for Global I/O Bus:
If Model 4260 is in MIX position 0, MIX_base = 0xC800 0000
If Model 4260 is in MIX position 1, MIX_base = 0xC820 0000
If Model 4260 is in MIX position 2, MIX_base = 0xC840 0000

NOTE: MXA27 is asserted via page bit 2 in Normal addressing mode, or via 'C40 address bit GA20 in Compressed addressing mode

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5.2 Receiver Buffer Register (RBR)

Read Only

The ACE's receiver section consists of a receiver shift register (RSR) and a receiver buffer register (RBR). The RBR is actually a 16-byte FIFO. Timing is supplied by the 16 X Receiver Clock (RCLK). Receiver section control is a function of the ACEs line control register.

The ACE's RSR receives serial data from the serial input (SlN) pin. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the receiver buffer register and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the receiver buffer register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

5.3 Transmitter Holding Register (THR)

Write Only

The ACE's transmitter section consists of a transmitter holding register (THR) and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is suppled by the baud out (BAUDOUT) clock signal. Transmitter section control is a function of the ACE's line control register.

The ACE's THR receives data off the internal data bus and, when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at the serial output (SOUT). In the TL16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This Interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

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5.4 Interrupt Enable Register (IER)

Read/Write

The Interrupt enable register enables each of the five types of interrupts (refer to Table 5-7) and the INTRPT output signal in response to an interrupt generation. The interrupt enable register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized below.

Interrupt Enable Register (IER) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved				EDSSI	ELSI	ETBEI	ERB
Bit Definition	Always set to logic '0'				logic '0' = Disabled logic '1' = Enabled			

5.4.1 Bits 7-4 - Reserved

Bits 7 through 4 in the interrupt enable register are not used and are always set to logic 0.

5.4.2 Bit 3 - Enable Modem Status Interrupt (EDSSI)

This bit, when set to logic 1, enables the modem status interrupt.

5.4.3 Bit 2 - Enable Receiver Line Status Interrupt (ELSI)

This bit, when set to logic 1, enables the receiver line status interrupt.

5.4.4 Bit 1 - Enable Transmitter Holding Register Empty Interrupt (ETBEI)

This bit, when set to logic 1, enables the transmitter holding register empty interrupt.

5.4.5 Bit 0 - Enable Received Data Available Interrupt (ERB)

This bit, when set to logic 1, enables the received data available interrupt.

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5.5 FIFO Control Register (FCR)

Write Only

The FIFO control register (FCR) is a write-only register at the same location as the IIR, which is a read-only register. The FCR is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

5.5.1 Bit 7 - Receiver Trigger, MSB (FCR7)

5.5.2 Bit 6 - Receiver Trigger, LSB (FCR6)

FCR6 and FCR7 are used to set the trigger level for the receiver FIFO interrupt.

Table 5-6: Receiver FIFO Trigger Level

Bit 7	Bit 6	Bytes
0	0	01
0	1	04
1	0	08
1	1	14

5.5.3 Bits 5-4 - Reserved (FCR5-FCR4)

FCR4 and FCR5 are reserved for future use.

5.5.4 Bit 3 - DMA Mode Select (FCR3)

If FCR0 is a 1, setting FCR3 to a 1 causes the RXRDY and TXRDY to change from mode 0 to mode 1.

5.5.5 Bit 2 - Transmitter FIFO Reset (FCR2)

FCR2, when set to logic 1, clears all bytes in the transmit FIFO and resets its counter to 0. The shift register is not cleared. The 1 that is written to this bit position is self clearing.

5.5.6 Bit 1 - Receiver FIFO Reset (FCR1)

FCR1, when set to logic 1, clears all bytes in the receiver FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self clearing.

5.5.7 Bit 0 - FIFO Enable (FCR0)

FCR0, when set to logic 1, enables the transmit and receive FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed. Changing this bit clears the FIFOs.

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5.6 Interrupt Identification Register (IIR)

Read Only

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 - Receiver line status (highest priority)
- Priority 2 - Receiver data ready or receiver character timeout
- Priority 3 - Transmitter holding register empty
- Priority 4 - Modem status (lowest priority)

When an interrupt is generated, the interrupt identification register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4. Detail on each bit are as follows:

5.6.1 Bits 7-6 - FIFOs Enabled

These two bits are always 0 in the TL16C450 mode. They are set when bit 0 of the FIFO control register is equal to 1.

Table 5-7: Interrupt Control Functions

Interrupt Identification Register				Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
Bit 3	Bit 2	Bit 1	Bit 0				
0	0	0	1	None	None	None	-
0	1	1	0	1	Receiver Line Status	Overrun error, parity error, framing error, or break interrupt	Reading the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode	Reading the receiver buffer register
1	1	0	0	2	Character timeout indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time	Reading the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transfer holding register empty	Reading the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	4	Modem Status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

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5.6 Interrupt Identification Register (IIR) (continued)

5.6.2 Bits 5-4 - Reserved

These two bits are not used and are always set at logic 0.

5.6.3 Bits 3-1 - Interrupt ID

Bits 1 and 2 are used to identify the highest priority interrupt pending, as indicated in Table 5-7.

Bit 3 is always 0 in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a timeout interrupt Is pending.

5.6.4 Bit 0 - Interrupt Pending

This bit can be used either in a hardwire-prioritized, or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

5.7 Line Control Register (LCR)

Read/Write

The system programmer controls the format of the asynchronous data communication exchange through the line control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the line control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are described below.

Line Control Register (LCR) - Read/Write								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DLAB	Set Break	Stick Parity	EPS	PEN	STB	WLS1	WLS0
Bit Definition	0 = Access RBR, THR, or IER Registers 1 = Access DLL/DLM	0 = Break Disabled 1 = Force Break	0 = Stick Parity Disabled 1 = Stick Parity Enabled	0 = Odd Parity 1 = Even Parity	0 = Parity Enable 1 = Parity Disabled	0 = 1 Stop Bit 1 = Stop Bits According to WLS1/WLS0	See Table 5-9	

5.7.1 Bit 7 - Divisor Latch Access Bit (DLAB)

This bit is the divisor latch access bit (DLAB). Bit 7 must be set to a logic 1 to access the divisor latches of the baud generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

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5.7.2 Bit 6 - Break Control Bit

This bit is the break control bit. Bit 6 is set to a logic 1 to force a break condition, i.e., a condition where the serial output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic; it only effects the serial output.

5.7.3 Bit 5 - Stick Parity Bit

This is the stick parity bit. When bits 3, 4, and 5 are logic 1s, the parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1's and bit 4 is a logic 0, the parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0, stick parity is disabled.

5.7.4 Bit 4 - Even Parity Select Bit (EPS)

Bit 4 is the even parity select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces even parity (an even number of logic 1's in the data and parity bits) and a logic 0 in bit 4 produces odd parity (an odd number of logic 1's).

5.7.5 Bit 3 - Parity Enable Bit (PEN)

This bit is the parity enable bit. When bit 3 is a logic 1, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.

5.7.6 Bit 2 - Number of Stop Bits (STB)

This bit specifies either one, one and one-half, or two stop bits in each transmitted character. If bit 2 Is a logic 0, one stop bit is generated in the data. If bit 2 is a logic 1, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks the first stop bit only, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in the following.

Table 5-8: Number of Stop Bits

Bit 2	Word Length Selected by Bits 1 & 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1½
1	6 bits	2
1	7 bits	2
1	8 bits	2

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5.7 Line Control Register (LCR) (continued)

5.7.7 Bits 1-0 - Word Length Select Bit (WLS1, WLS0)

These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

Table 5-9: Word Length Select Bits

Bit 1	Bit 2	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

5.8 Modem Control Register (MCR)

Read Only

The modem control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described below.

Modem Control Register (MCR) - Read Only

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved			LOOP	OUT 2	OUT 1	RTS	DTR
Bit Function	Permanently set to logic 0			0=Normal 1=Loopback	logic '0' = high state (Inactive) logic '1' = low state (Active)			

5.8.1 Bit 7-5 - Reserved

These bits are permanently set to logic 0.

5.8.2 Bit 4 - Loop

Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:

1) The transmitter serial output (SOUT) is set high.

2) The receiver serial input (SIN) is disconnected.

3) The output of the transmitter shift register is looped back into the receiver shift register input.

4) The four modem control inputs (CTS, DSR, DCD, and RI) are disconnected.

5) The four modem control outputs (DTR, RTS, OUT 1, and OUT 2) are internally connected to the four modem control inputs.

6) The four modem control output pins are forced to their inactive states (high).

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5.8 Modem Control Register (MCR) (continued)

5.8.2 Bit 4 - Loop (continued)

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the modem control register instead of the four modem control inputs. All interrupts are still controlled by the interrupt enable register.

5.8.3 Bit 3 - Output 2 (OUT 2)

Bit 3 (OUT 2) controls the output 2 (OUT 2) signal, a user-designated output signal, in a manner identical to bit 0's control over the DTR output.

5.8.4 Bit 2 - Output 1 (OUT 1)

Bit 2 (OUT 1) controls the output 1 (OUT 1) signal, a user-designated output signal, in a manner identical to bit 0's control over the DTR output.

5.8.5 Bit 1 - Request To Send (RTS)

Bit 1 (RTS) controls the request to send (RTS) output in a manner identical to Bit 0's control over the DTR output.

5.8.6 Bit 0 - Data Terminal Ready (DTR)

Bit 0 (DTR) controls the data terminal ready (DTR) output. Setting this bit to a logic 1 forces the DTR output to its low state. When bit 0 is set to a logic 0, DTR goes high.

5.9 Line Status Register (LSR)

Read Only

The line status register provides information to the CPU concerning the status of data transfers. Bits 1 through 4 are the error conditions that produce a receiver line status interrupt. The contents of this register are described below.

Line Status Register (LSR) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	LSR7	TEMT	THRE	BI	FE	PE	OE	DR
Bit Function	See Section 5.9.1	0 = Not Empty 1 = Empty		0 = No Break 1 = Break	0 = No Error 1 = Error			0=Not Ready 1=Ready

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5.9 Line Status Register (LSR) (continued)

5.9.1 Bit 7 - Error in Receiver FIFO (LSR7)

In the TL16C550A, this bit is always reset to logic 0. In the TL16C450 mode, this bit is always a 0. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

5.9.2 Bit 6 - Transmitter Empty Indicator (TEMT)

Bit 6 is the transmitter empty (TEMT) indicator. This bit is set to a logic 1 when the transmitter holding register and the transmitter shift register are both empty. When either the transmitter holding register or the transmitter shift register contains a data character, the TEMT bit is reset to logic 0. In the FIFO mode, this bit is set to a 1 when the transmitter FIFO and shift register are both empty.

5.9.3 Bit 5 - Transmitter Holding Register Empty Indicator (THRE)

Bit 5 is the transmitter holding register empty (THRE) indicator. This bit is set to logic 1 when the transmitter holding register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the transmitter holding register are transferred to the transmitter shift register. This bit is reset to logic 0 concurrent with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

5.9.3 Bit 4 - Break Interrupt Indicator (BI)

Bit 4 is the break interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and Stop bits. The BI bit is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

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5.9 Line Status Register (LSR) (continued)

5.9.4 Bit 3 - Framing Error Indicator (FE)

Bit 3 is the framing error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) stop bit. The FE bit is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE will try to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE then samples this start bit twice and then accepts the input data.

5.9.5 Bit 2 - Parity Error Indicator (PE)

Bit 2 is the parity error (PE) indicator. When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the line control register (bit 4). The PE bit is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

5.9.6 Bit 1 - Overrun Error Indicator (OE)

Bit 1 is the overrun error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the receiver buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the line status register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten but is not transferred to the FIFO.

5.9.7 Bit 0 - Data Ready Indicator (DR)

Bit 0 is the data ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the receiver buffer register or the FIFO and is reset to logic 0 by reading all of the data in the receiver buffer register or the FIFO.

5.10 Modem Status Register (MSR)

Read Only

The modem status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU.

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5.10 Modem Status Register (MSR) (continued)

Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the modem status register. The contents of this register are described below.

Modem Status Register (MSR) - Read Only								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DCD	RI	DSR	CTS	ΔDDCD	TERI	ΔDDSR	ΔDCTS
Bit Function	See Below							

5.10.0 Bit 7 - Data Carrier Detect (DCD)

Bit 7 is the complement of the data carrier detect (DCD) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control registers bit 3 (OUT 2).

5.10.1 Bit 6 - Ring Indicator (RI)

Bit 6 is the complement of the ring indicator (RI) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control register bit 2 (OUT 1).

5.10.2 Bit 5 - Data Set Ready (DSR)

Bit 5 is the complement of the data set ready (DSR) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control register bit 1 (DTR).

5.10.2 Bit 4 - Clear To Send (CTS)

Bit 4 is the complement of the clear to send (CTS) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control register bit 1 (RTS).

5.10.3 Bit 3 - Delta Data Carrier Detect Indicator (DDCD)

Bit 3 is the change in data carrier detect (DDCD) indicator. This bit indicates that the DCD input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

5.10.4 Bit 2 - Trailing Edge of Ring Indicator (TERI)

Bit 2 is the trailing edge of ring indicator (TERI) detector. This bit indicates that the RI input to the chip has changed from a low to a high state. When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

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5.10 Modem Status Register (MSR) (continued)

5.10.5 Bit 1 - Delta Data Set Ready (DDSR)

Bit 1 is the change in data set ready (DDSR) indicator. This bit indicates that the DSR input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

5.10.6 Bit 0 - Delta Clear To Send (DCTS)

Bit 0 is the change in clear to send (DCTS) indicator. This bit indicates that the CTS input has changed state since the last time it was read by the CPU . When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

5.11 Scratch Register (SCR)

Read/Write

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it will temporarily hold the programmer's data without affecting any other ACE operation.

5.12 Programmable Baud Generator

The ACE contains a programmable baud generator that takes a clock input in the range between DC and 8 MHz and divides it by a divisor in the range between 1 and (2 ^ 16)-1. The output frequency of the baud generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

divisor # = XIN frequency input / (desired baud rate X 16)

Two 8-bit registers, called divisor latches, are used to store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

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5.13 FIFO Interrupt-Mode Operation

When the receiver FIFO and receiver interrupts are enabled (FCRO = 1, IERO = 1) receiver interrupts will occur as follows:

1) The receive data available interrupt will be issued to the microprocessor when the FIFO has reached its programmed trigger level. It will be cleared as soon as the FIFO drops below its programmed trigger level.

2) The IIR receive data available indication also occurs when the FIFO trigger level is reached, and, like the interrupt, it is cleared when the FIFO drops below the trigger level.

3) The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (llR = 04) interrupt.

4) The data ready bit (LSRO) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled, receiver FIFO timeout interrupts will occur as follows:

1) FIFO timeout interrupt will occur if the following conditions exist:

   a) At least one character is in the FIFO.

   b) The most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed, the second one is included in this time delay).

   c) The most recent microprocessor read of the FIFO was longer than 4 continuous character times ago. This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with 12-bit character.

2) Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

3) When a timeout interrupt has occurred, it is cleared and the timer reset when the microprocessor reads one character from the receiver FIFO.

4) When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCRO = 1, lER1 = 1), transmit interrupts will occur as follows:

1) The transmitter holding register interrupt (02) occurs when the transmit FIFO is empty. It is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.

2) The transmit FIFO empty indications will be delayed 1 character time minus the last stop bit time when the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCRO will be immediate, if it is enabled.

Character timeout and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt; transmit FIFO empty has the same priority as the current transmitter holding register empty interrupt.

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5.14 FIFO Polled-Mode Operation

With FCRO = 1, resetting IERO, lER1, lER2, lER3, or all four to 0 puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program will check receiver and transmitter status via the LSR. As stated previously:

1) LSRO will be set as long as there is one byte in the receiver FIFO.

2) LSR1 through LSR4 will specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since lER2 = 0.

3) LSR5 will indicate when the transmit FIFO is empty.

4) LSR6 will indicate that both the transmit FIFO and shift registers are empty.

5) LSR7 will indicate whether there are any errors in the receiver FIFO.

There is no trigger level reached or timeout conditions indicated in the FIFO polled mode. However, the receiver and transmit FIFO,s are still fully capable of holding characters.

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Appendix A: Symbios SYM53C770 SCSI I/O Processor With Ultra SCSI

A.1 The following Pages contain the Symbios SYM53C770 SCSI I/O Processor With Ultra SCSI Manual.

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SYM53C770
SCSI I/O Processor
With Ultra SCSI

Data Manual
Version 2.0

INCREASING SCSI RELIABILITY
TolerANT
ACTIVE NEGATION TECHNOLOGY

T18962I

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Ultra SCSI is the term used by the SCSI Trade Association to describe Fast-20 SCSI, as documented in the SCSI-3 Fast-20 Parallel Interface standard, X3.277-199X. Ultra2 SCSI is the term used by the SCSI Trade Association to describe Fast-40 SCSI, as documented in early versions of the SPI-2 draft standard.

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Preface

SCSI and PCI Reference Information

This manual assumes some prior knowledge of current and proposed SCSI and PCI standards. For background information, please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-199X (SCSI-2)

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
(800)-854-7179 or (303) 397-7956 (outside U.S.) FAX (303) 397-2740
Ask for document number X3.131-1994 (SCSI-2) or X3.253 *(SCSI-3 Parallel Interface)*

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia, SCSI Tutor*

Prentice Hall
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

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SCSI Electronic Bulletin Board

(719) 533-7950

Symbios Logic Internet Anonymous FTP Site
ftp.symbios.com (204.131.200.1)
Directory: /pub/symchips/scsi

Symbios Logic World-Wide Web Home Page
http://www.symbios.com

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2575 N. E. Katherine
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SYM53C720/SE/53C770 Programming Guide

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Document History

Page No.	Date	Remarks
all	9/94	Rev. 1.0
all	2/96	Updated/added information on SYM53C770
	7/96	Version 2.0 Changed Fast-20 to Ultra SCSI throughout document

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Chapter 1

Introduction

General Description

The SYM53C770 is a member of the 53C7XX family of intelligent, single-chip, third generation SCSI host adapters. A high performance SCSI core and an intelligent 16- or 32-bit bus master DMA core are integrated with a SCSI SCRIPTS processor to accommodate the flexibility requirements of not only SCSI-1 and SCSI-2, but future SCSI standards as well. In addition, the SYM53C770 solves the protocol overhead problems that have plagued all previous intelligent and non-intelligent adapter designs.

The SYM53C770 is designed to completely implement a multi-threaded I/O algorithm in either a workstation or file server environment, completely free of processor intervention except at the end of an I/O transfer. In addition, the SYM53C770 provides automatic relocation of SCRIPTS, and requires no dynamic alteration of SCRIPTS instructions at the start of an I/O operation. All of the SCRIPTS code may be placed on a PROM. The SYM53C770 allows easy firmware upgrades and is SCRIPTS-compatible with the SYM53C710 and the SYM53C8XX family.

The SYM53C770 supports four different host processor interfaces, or bus modes. Bus Mode 1 closely resembles the Motorola 68030 interface, and Bus Mode 2 closely resembles the Motorola 68040 interface. Bus Mode 3 closely resembles the Intel 80386SX interface; the 16-bit host interface should be enabled in this mode. Finally, Bus Mode 4 closely resembles the 80386DX interface. Bus Modes 1, 2 and 4 support both the Big and Little Endian byte ordering schemes and Bus Mode 3 supports Little Endian byte ordering, for a total of seven operating modes. The modes are selected by using the bus mode select pins (BS 2-0).

The SYM53C770 is a pin-for-pin- replacement of the SYM53C720. It performs Ultra SCSI data transfers at 20 MB/S (8-bit) or 40 MB/S (16-bit). It is packaged in a 208-pin quad flat pack, and performs both single-ended and differential transfers.

Benefits of Ultra SCSI

Ultra SCSI is an extension of the SCSI-3 standard that expands the bandwidth of the SCSI bus and allows faster synchronous SCSI transfer rates. When enabled, Ultra SCSI performs 20 mega-transfers during an I/O operation, which results in approximately doubling the synchronous transfer rates of fast SCSI-2. The SYM53C770 can perform 8-bit, Ultra SCSI synchronous transfers as fast as 20 MB/s. This advantage is most noticeable in heavily loaded systems, or large-block size applications such as video on-demand and image processing.

One advantage of Ultra SCSI is that it significantly improves SCSI bandwidth while preserving existing hardware and software investments. The SYM53C770 is compatible with all existing SYM53C720 and SYM53C720SE software; the only changes required are to enable the chip to perform synchronous negotiations for Ultra SCSI rates. The SYM53C770 can use the same board socket as an SYM53C720, with the addition of an 80/100MHz SCLK or internal SCSI clock doubler (clock doubler works at 40 to 50 MHz input) which will provide the correct frequency when transferring synchronous SCSI data at 50 nanosecond transfer rates. Some changes to existing

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cabling or system designs may be needed to maintain signal integrity at Ultra SCSI synchronous transfer rates. These design issues are discussed in Chapter 2.

Symbios Logic TolerANT ® Technology

The SYM53C770 features Symbios Logic TolerANT® SCSI driver and receiver technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI REQ, ACK, Data and Parity signals to be actively driven high by transistors on each pin. The 48 mA drivers actively force the SCSI bus signal to the high (negated) state faster than passive pull-up drivers. TolerANT receivers filter SCSI bus signals to eliminate unwanted transitions without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate the double clocking of data, which is the single biggest data reliability problem with the SCSI interface. TolerANT improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. The benefits of this technology include increased immunity to noise when the signal is going high, increased performance due to balanced duty cycles, and improved Fast SCSI transfer rates. Active Negation is enabled by setting bit 7 in the STEST3 register. It can be used in both single-ended and differential mode. SYM Active Negation technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

SYM53C770 Features Summary

Performance

- Performs Ultra SCSI synchronous transfers as fast as 40 MB/s (with wide SCSI)
- Includes 4KB internal RAM for SCRIPTS instruction storage
- Supports variable block size and scatter/gather data transfers
- Supports 16- and 32-bit data bursts with variable burst lengths
- Performs memory-to-memory DMA transfers in excess of 44 MB/s
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts, including restore data pointers
- Reduces ISR overhead with unique interrupt status reporting
- Performs memory transfers in excess of 100 MB/s (@ 33 MHz)
- Uses a 96-byte DMA FIFO to support cache line bursting
- Uses up to 16 levels of synchronous SCSI offset for optimum speed matching during Ultra SCSI transfers
- Provides an additional 32 scratch registers

Integration

- Functions as full 16- or 32-bit DMA bus master
- Contains high performance wide SCSI core
- Includes RISC-based SCSI SCRIPTS processor
- Allows intelligent host adapter performance on a motherboard

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Ease of Use

- Reduces SCSI development effort
- Supports Big and Little Endian environments
- Uses existing SYM53C720 SCRIPTS
- Includes development tools and sample SCSI SCRIPTS
- Supports maskable and pollable interrupts
- Supports wide SCSI, A or P cable, and up to 16 devices
- Interfaces with seven different host processor buses, including Motorola (680X0 family) and Intel (80X86 family)
- Supports odd-byte block sizes in conjunction with wide SCSI
- Provides three programmable SCSI timers: Select/Reselect, Handshake-to-Handshake, and General Purpose. The time-out period is programmable from 100 µs to greater than 1.6 seconds.
- The handshake-to-handshake and general purpose timers use a scale factor to increase the amount of time before expiration.
- The handshake-to-handshake timer has an optional mode that allows it to operate as a bus activity timer for all SCSI transfers.

Flexibility

- Uses a high level programming interface (SCSI SCRIPTS)
- Allows tailored SCSI sequences to be executed from main memory or from a host adapter board's local memory
- Allows use of flexible sequences to tune I/O performance or to adapt to unique SCSI devices
- Accommodates changes in the logical I/O interface definition
- Supports low level programmability (register oriented)
- Allows a target to disconnect and later reselect with no interrupt to the system processor
- Allows a multi-threaded I/O algorithm to be executed in SCSI SCRIPTS with fast I/O context switching
- Allows relative jumps
- Allows indirect fetching of DMA address and byte counts so that SCRIPTS can be placed in a PROM
- Includes separate SCSI and system clocks
- Doubles the SCSI clock input during Ultra SCSI transfer modes
- Uses a new SSAID (SCSI Selected as ID) register

Reliability

- Symbios Logic TolerANT SCSI driver and receiver technology
- 2 K volts ESD protection on SCSI signals
- Typical 350 mV SCSI bus hysteresis
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- Voltage feed through protection (minimum leakage current through SCSI pads)
- 20% of pins power and ground
- Ground isolation of I/O pads and chip logic

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Testability

- All SCSI signals accessible through programmed I/O
- SCSI loopback diagnostics
- Self-selection capability
- SCSI bus signal continuity checking
- Support for single step mode operation

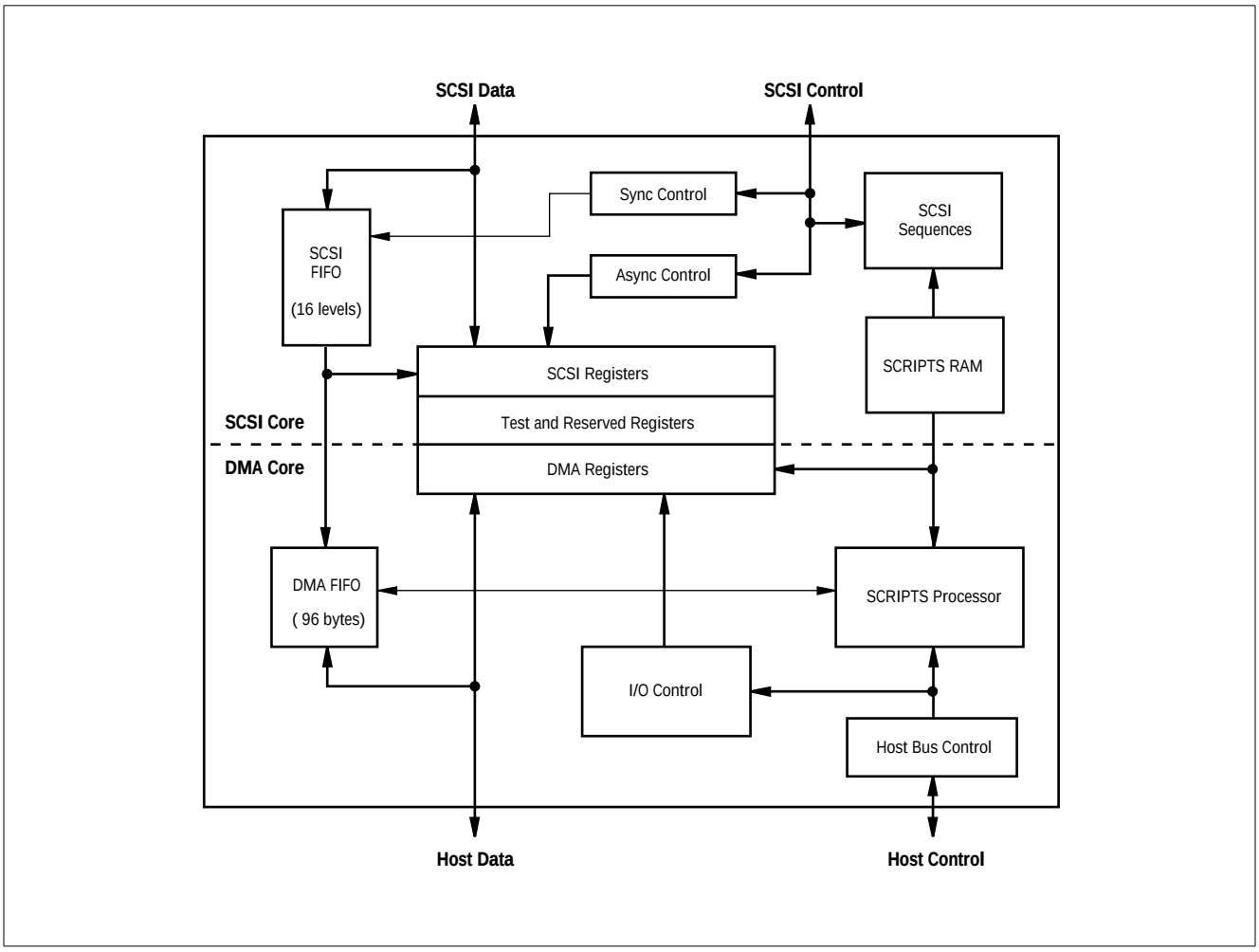


Figure 1-1: SYM53C770 Block Diagram

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Summary of New Features in the SYM53C770

For more information on enabling or using these new features, please refer to the chapter indicated with each topic.

- Support for Ultra SCSI data transfers (Chapter 2, Chapter 4, Chapter 6)
- DMA FIFO increased to 96 bytes (Chapter 2)
- SCSI offset increased to 16 levels (Chapter 4, SXFER register description)
- Internal SCRIPTS RAM (Chapter 2, Chapter 4)
- Expanded timers (Chapter 4, STIME0 and STIME1 register descriptions)
- Expanded SLPAR register (Chapter 4, SLPAR register description)
- Additional Read-Modify-Write Instructions (Chapter 5, Read/Write instructions)
- SCSI Clock Doubler (Chapter 2, Chapter 4)
- SCSI Selected As ID register (Chapter 4)
- Fairness timer update (Chapter 4, DMODE register description)
- Additional 32 Scratch registers (Chapter 4)
- Vendor unique enhancements (Chapter 4, SCNTL2 register description)
- DIFFSENSE Sense bit to detect a differential System (Chapter 5, SSTAT2 register description)

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Chapter 2

Functional Description

The SYM53C770 is composed of three interrelated functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS Processor. This chapter describes the major functional aspects of the chip. For detailed information on implementing or using specific features, refer to later chapters in this manual. Chapter 3 contains detailed information on the SYM53C770 pins. Chapter 4 describes all of the operating registers and bits. Chapter 4 describes the SYM53C770 instruction set, and Chapter 5 contains the chip electrical specifications and timings.

SCSI Core

The SCSI core supports the SCSI-2 fast and wide bus. It supports synchronous transfer rates of up to 20 MB/s or 40 MB/s in Fast 20, and asynchronous transfer rates up to 10 MB/s. The programmable SCSI interface makes it easy to “fine tune” the system for specific mass storage devices or advanced SCSI requirements.

The SCSI core offers low level register access or a high-level control interface. Like first generation SCSI devices, the SYM53C770 SCSI core can be accessed as a register-oriented device. The ability to sample and/or assert any signal on the SCSI bus can be used in error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core may perform a self-selection and operate as both an initiator and a target. This can test all data paths in the chip. The SYM53C770 uses an “AND tree” to test the SCSI pins for physical connection to the board or the SCSI bus.

Unlike previous generation devices, the SCSI core can be controlled by the SCRIPTS processor, a high-level logical interface optimized for SCSI protocol. SCRIPTS routines controlling the SCSI core are fetched out of the main host memory or local PROM. These commands instruct the SCSI core to select, reselect, disconnect, wait for a disconnect, transfer information, change bus phases and in general, implement all aspects of the SCSI protocol.

DMA Core

The DMA core is a bus master DMA device that is made to attach to Intel (80386SX and 80386DX), and Motorola (68030 and 68040) processors.

The SYM53C770 supports 16- or 32-bit memory and automatically supports misaligned DMA transfers. A 96-byte FIFO allows the SYM53C770 to burst two, four, eight, or sixteen longwords across the memory bus interface. This DMA interface does not support dynamic bus sizing.

The DMA core communicates with the SCSI core through the SCRIPTS processor, which supports uninterrupted scatter/gather memory operations.

SCRIPTS Processor

The SCSI SCRIPTS processor allows both DMA and SCSI instructions to be fetched from host memory or internal SCRIPTS RAM. Algorithms written in SCSI SCRIPTS control the actions of the SCSI and DMA cores and are executed from 16- or 32-bit system memory. Complex SCSI bus sequences are executed independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. This compares with 2-8 ms required for traditional intelligent host

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adapters. The SCRIPTS processor supports customized algorithms to tune SCSI bus performance, adjust to new bus device types (i.e. scanners, communication gateways, etc.), or incorporate changes in the SCSI logical bus definitions without sacrificing I/O performance. SCSI SCRIPTS are independent of the CPU and system bus in use. For detailed information on SCSI SCRIPTS, please see the *SYM53C720/SE/ 53C770 Programming Guide*.

Internal SCRIPTS RAM

The SYM53C770 has 4 KB (1K x 32 bits) of internal, general purpose RAM. The RAM is designed for SCRIPTS program storage, but is not limited to this type of information. When the chip fetches SCRIPTS instructions or Table Indirect information from the internal RAM, these fetches remain internal to the chip and do not use the host bus. Other types of access to the RAM by the SYM53C770 use the host bus as if they were external accesses. When the internal RAM is enabled, the SYM53C770 uses the shadowed SCRATCHA register as the base address of the RAM when bit 0 is set in the CTEST5 register.

The internal RAM can be enabled and used in three ways:

1. Register-based through indexed addressing;
2. Increased chip select address space that includes support for the chip registers and internal RAM with a single chip select pin; and
3. An additional chip select pin supporting only internal RAM with the original Chip Select pin supporting only the chip registers.

The register-based method allows use of the SCRIPTS RAM in existing SYM53C720 designs without hardware changes. To use this method, clear CTEST5 bit 2 and set CTEST5 bit 1. The internal RAM is mapped into the chip registers using indexed addressing in a shadowed SCRATCHB register. The RAM replaces the SCRATCHC-J registers, and may optionally be used as a block of scratchpad RAM. When the chip determines that a SCRIPTS address is in the internal RAM space, the opcode fetch sequence accesses the internal RAM without using the host bus. Indirect and table indirect functions also determine if the address is contained in internal RAM space and fetch data from the RAM without host bus access. Read-Modify-Write operations or Memory Move instructions can be used to modify the RAM while SCRIPTS are running, but the host cannot access the RAM during SCRIPTS operation.

The increased chip select address space method defines 4K byte address space for the chip registers and the 4K byte space for the SCRIPTS RAM. To enable this mode, set CTEST5 bit 2 and clear CTEST5 bit 1. The registers are located at addresses 0000h through 007Fh, repeating at intervals of 128 bytes until the 4K byte boundary. The RAM occupies addresses 1000h through 1FFFh. The RAM is accessible by the host during SCRIPTS execution, but up to seven additional wait states may be added to a slave read or write access if it occurs while an internal SCRIPTS access is in progress. Read-Modify-Write operations or Memory Move instructions can be used to modify the RAM while SCRIPTS are running.

An additional chip select pin the RAMCS/ pin can be used to define a 4K byte address space for the internal RAM by setting bits 1 and 2 of the CTEST5 register. The RAM is accessible by the host during SCRIPTS execution, but up to seven additional wait states may be added to a slave read or write access if it occurs while an internal SCRIPTS access is in progress. Read-Modify-Write operations or Memory Move instructions can be used to modify the RAM while SCRIPTS are running.

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Designing a Ultra SCSI System

Migrating an existing single-ended SCSI design from SCSI-2 to Ultra SCSI requires minor software modifications as well as consideration for some hardware design guidelines. Since Ultra SCSI is based on existing SCSI standards, it can use existing software programs as long as the software is able to negotiate for Ultra SCSI synchronous transfer rates.

In the area of hardware, the primary area of concern in single-ended systems is to maintain signal integrity at high data transfer rates. To assure reliable operation at Ultra SCSI transfer speeds, follow the system design parameters recommended in the SCSI-3 Fast-20 Parallel Interface draft standard, which is available from the SCSI BBS referenced at the beginning of this manual. Chapter 7 contains Ultra SCSI timing information. In addition to the guidelines in the draft standard, make the following software and hardware adjustments to accommodate Ultra SCSI transfers:

- Set the Ultra Enable bit to enable Ultra SCSI transfers. (SCNTL3, bit 7)
- Set the TolerANT Enable bit, bit 7 in the STEST3 register whenever the Ultra SCSI Enable bit is set.
- Do not extend the SREQ/SACK filtering period with STEST2 bit 1.
- Use an 80/100 MHz SCSI clock or enable the SCSI clock doubler (clock doubler works at 40 to 50 MHz input) using bits 2 and 3 of the STEST1 register. Set the halt SCSI clock (HSC) bit in STEST3 before switching to the doubled SCSI clock.

Using the SCSI Clock Doubler

The SYM53C770 can double the frequency of a 40-50 MHz SCSI clock, allowing the system to perform Ultra SCSI transfers in systems that do not have 80 MHz clock input. This option is user-selectable with bit settings in the STEST1, STEST3, and SCNTL3 registers. At power-on or reset, the doubler is disabled and powered down. Follow these steps to use the clock doubler:

1. Set the SCLK Doubler Enable bit (STEST1, bit 3)
2. Wait 20 µs
3. Halt the SCSI clock by setting the Halt SCSI Clock bit (STEST3 bit 5)
4. Set the clock conversion factor using the SCF and CCF fields in the SCNTL3 register
5. Set the SCLK Doubler Select bit (STEST1, bit 2)
6. Clear the Halt SCSI Clock bit.

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Big/Little Endian Support

The Bus Mode Select pin gives the SYM53C770 the flexibility of operating with either Big or Little Endian byte orientation. Internally, in either mode, the byte lanes of the DMA FIFO and registers are not modified. The SYM53C770 supports byte, word, and longword slave accesses in both Big and Little Endian modes (word accesses must be word-aligned).

When a longword is accessed, no repositioning of the individual bytes is necessary, since longwords are addressed by the address of the least significant byte. SCRIPTS always uses longwords in 32-bit systems, so compatibility is maintained between systems using different byte orientations. When a word is accessed, individual bytes must be repositioned. Internally, the SYM53C770 adjusts the byte control logic of the DMA FIFO and register decodes to access the appropriate byte lanes. The registers will always appear on the same byte lane, but the address of the register will be repositioned. Words are addressed by the address of the least significant byte. Big/Little Endian mode selection has the most effect on individual byte access, as illustrated in Table 2-1.

Note: the SYM 53C770 supports Big Endian addressing in 16-bit systems with Bus Modes 1 and 2 only.

Data to be transferred between system memory and the SCSI bus always starts at address zero and continues through address ‘n’ - there is no byte ordering in the chip. The first byte in from the SCSI bus goes to address 0, the second to address 1, etc. Going out onto the SCSI bus, address zero is the first byte out on the SCSI bus, address 1 is the second byte, etc.

Correct SCRIPTS will be generated if the SCRIPTS compiler is run on a system that has the same byte ordering as the target system. Any SCRIPTS patching in memory must patch the instruction in the order that the SCRIPTS processor expects it.

Software drivers for the SYM53C770 should access registers by their logical name (i.e., “SCNTL0”) rather than by their address. The logical name should be equated to the register’s Big Endian address in Big Endian mode (SCNTL0 = 03h), and its Little Endian address in Little Endian Mode (SCNTL0 = 00h). This way, there is no change to the software when moving from one mode to the other; only the equate statement setting the operating modes needs to be changed. Addressing of registers from within a SCRIPTS instruction is independent of bus mode. Internally, the SYM53C770 always operates in Little Endian mode.

Big Endian Mode

Big Endian addressing is used primarily in designs based on Motorola processors. The SYM53C770 treats D(31-24) as the lowest physical memory address. The register map is left- justified (Address 03h = SCNTL0).

Little Endian Mode

Little Endian is used primarily in designs based on Intel processors. This mode treats D(7-0) as the lowest physical memory address. The register map is right-justified (Address 00h = SCNTL0).

Table 2-1: Big and Little Endian Addressing

System data bus	(31-24)	(23-16)	(15-8)	(7-0)
53C770 pins	(31-24)	(23-16)	(15-8)	(7-0)
Register	SCNTL3	SCNTL2	SCNTL1	SCNTL0
Little Endian addr	03h	02h	01h	00h
Big Endian addr	00h	01h	02h	03h

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Loopback Mode

The SYM53C770 loopback mode allows testing of both initiator and target functions and, in effect, lets the chip talk to itself. This allows diagnostic testing of the DMA and SCSI cores, the SCRIPTS processor, and all internal data paths. When the Loopback Enable bit is set in the STEST2 register, the SYM53C770 allows control of all SCSI signals, whether it is operating in initiator or target mode. For more information on loopback operation, refer to the *SYM53C720/SE/53C770 Programming Guide*.

Parity Options

The SYM53C770 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. The following bits are involved in parity control and observation:

1. Assert ATN/ on Parity Errors – Bit 1 in the SCNTL0 register. This bit causes the SYM53C770 to automatically assert SCSI ATN/ when it detects a parity error (on either the SCSI or the data bus) while operating as an initiator.
2. Enable Parity Generation – Bit 2 in the SCNTL0 register. This bit determines whether the SYM53C770 generates parity sent to the SCSI bus or allows parity to “flow through” the chip to/from the SCSI bus and system bus.
3. Enable Parity Checking – Bit 3 in the SCNTL0 register. This bit enables the SYM53C770 to check for parity errors. The SYM53C770 checks for odd parity.
4. Assert Even SCSI Parity – Bit 2 in the SCNTL1 register. This bit determines the SCSI parity sense generated by the SYM53C770 being sent to the host. Parity generation must be enabled.
5. Disable Halt on ATN/ or a Parity Error (Target Mode Only) – Bit 5 in the SCNTL1 register. This bit causes the SYM53C770 to halt operations when a parity error is detected in target mode.
6. Enable Parity Error Interrupt – Bit 0 in the SIEN0 register. This bit determines whether the SYM53C770 will generate an interrupt when it detects a parity error.
7. Parity Error – Bit 0 in the SIST0 register. This status bit is set whenever the SYM53C770 has detected a parity error on either the SCSI bus or the system bus.
8. Status of SCSI Parity Signal – Bit 0 in the SSTAT0 register and bit 0 in SSTAT2. These status bits represent the live SCSI Parity Signal (SDP0 and SDP1).
9. Latched SCSI Parity Signal – Bit 3 in the SSTAT1 register and bit 3 in SSTAT2. These status bits contain the SCSI parity of the bytes latched in the SIDL.
10. DMA FIFO Parity – Bit 3 in the CTEST2 register. This status bit represents the parity bit in the DMA FIFO after data is read from the FIFO by reading the CTEST6 register.
11. DMA FIFO Parity – Bit 3 in the CTEST0 register. This write-only bit is written to the DMA FIFO after writing data to the DMA FIFO by writing the CTEST6 register.
12. SCSI FIFO Parity – Bit 0 in the STEST1 register. This status bit represents the parity bit in the SCSI FIFO after data is read from the FIFO by reading the SODL register, once bit 0 in STEST3 is asserted.
13. Generate Receive Parity —Bit 4 in the CTEST0 register. When this bit is set and the SYM53C770 is in parity pass-through mode (bit 2 in the SCNTL0 register is clear), parity received on the SCSI bus will not pass through the DMA FIFO. New parity will be generated.

    When this bit is cleared, and parity pass through mode is enabled (Bit 2of SCNTL0 is

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clear), parity received on the SCSI bus will pass through the SYM53C770 unmodified.

14. Enable Host Parity Checking—CTEST4, bit 3. Setting this bit enables parity checking during slave write and DMA read execution, if the Enable Parity Generation bit is cleared (SCNTL0 bit 2).

Table 2-2: SCSI Parity Control

EPG	EPC	AESP	Description
0	0	0	Will not check for parity errors. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	0	1	Will not check for parity errors. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
0	1	0	Checks for odd parity on both host and SCSI data when received. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data, Parity flows from SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	1	1	Checks for odd parity on both host and SCSI data when received. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
1	0	0	Will not check for parity errors. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	0	1	Will not check for parity errors. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
1	1	0	Checks for odd parity on SCSI data received. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	1	1	Checks for odd parity on SCSI data received. Parity on DP(3-0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.

Key:

EPG = Enable Parity Generation (bit 2 SCNTL0)

EPC = Enable Parity Checking (bit 3 SCNTL0)

AESP = Assert Even SCSI Parity (bit 2 SCNTL1)

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This table describes the options available when a parity error occurs. This table only applies when the Enable Parity Checking bit is set.

Table 2-3: Parity Errors and Interrupts

DHP	PAR	Description
0	0	Will NOT halt when a parity error occurs in target or initiator mode.
0	1	Will interrupt when a parity error occurs in target or initiator mode.*
1	0	Will halt when a parity error occurs in target mode and will NOT generate an interrupt
1	1	Will halt when a parity error occurs in target mode and will generate an interrupt in target or initiator mode

Key:DHP = Disable Halt on ATN/ or Parity Error (bit 5 SCNTL1) PAR= Parity Error (bit 0 SIEN0)

**Initiator mode parity error interrupts are generated at the end of a block move.*

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DMA FIFO

The SYM53C770 DMA FIFO is a 36 x 24 bit FIFO. It is divided into 4 byte lanes, each 9 bits wide and 24 transfers deep.

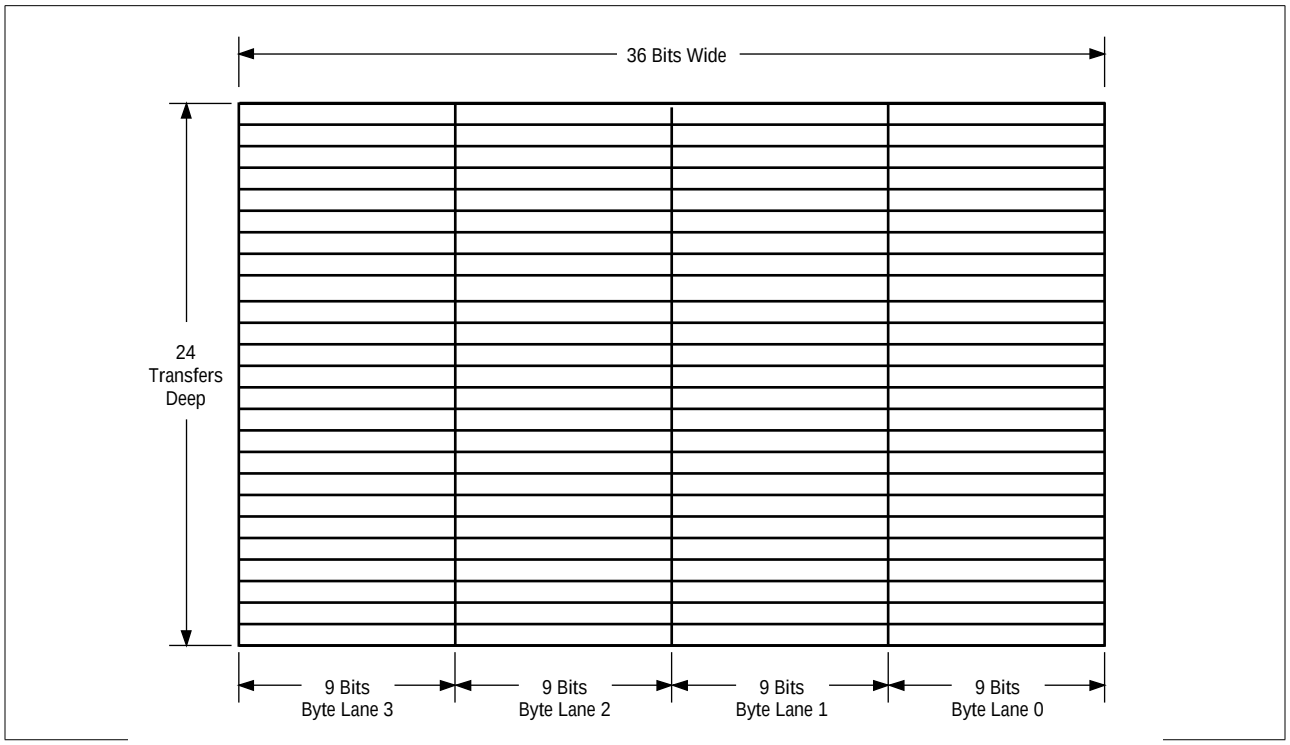


Figure 2-1: DMA FIFO Byte Lanes

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Data Path

When the SYM53C770 halts a data transfer operation, check the data path to determine if any bytes remain that have not been transferred. The data path through the SYM53C770 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously. Figure 2-2 shows how data is moved to/from the SCSI bus in each of the different modes.

DMA FIFO

In all types of transfers, the DMA FIFO is used in the data path. The DFE bit in the DSTAT register indicates whether there is any data in the DMA FIFO. To check the DMA FIFO, use the following procedure. The other parts of the data path may contain data. To check the data path, follow the steps indicated for each type of transfer.

Checking the Data Path

When transferring data from the host bus to the SCSI bus, subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for the byte count between 0 and 96.

When transferring data from the SCSI bus to the host bus, subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh and take the two's complement to obtain the byte count between 0 and 96.

Asynchronous SCSI Send

Read the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODL register. If bit 5 is set in the SSTAT0 or SSTAT2, then the least significant byte or the most significant byte in the SODL register is full, respectively. Checking this bit also reveals bytes left in the SODL register from a Chained Move operation with an odd byte count.

Synchronous SCSI Send

1. Read bit 5 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODL register. If bit 5 is set in the SSTAT0 or SSTAT2, then the least significant byte or the most significant byte in the SODL register is full, respectively. Checking this bit also reveals bytes left in the SODL register from a Chained Move operation with an odd byte count.
2. Read bit 6 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODR register. If bit 6 is set in the SSTAT0 or SSTAT2, then the least significant byte or the most significant byte in the SODR register is full, respectively.

Asynchronous SCSI Receive

1. Read bit 7 in the SSTAT0 and SSTAT2 register to determine if any bytes are left in the SIDL register. If bit 7 is set in the SSTAT0 or SSTAT2, then the least significant byte or the most significant byte is full, respectively.
2. If any wide transfers have been performed using the Chained Move instruction, read the Wide SCSI Receive bit (SCNTL2, bit 0) to determine whether a byte is left in the SWIDE register.

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Synchronous SCSI Receive

Read the SSTAT0 and SSTAT2 registers and examine bits 7-4, the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.

If any wide transfers have been performed using the Chained Move instruction, read the Wide SCSI Receive bit (SCNTL2, bit 0) to determine whether a byte is left in the SWIDE register.

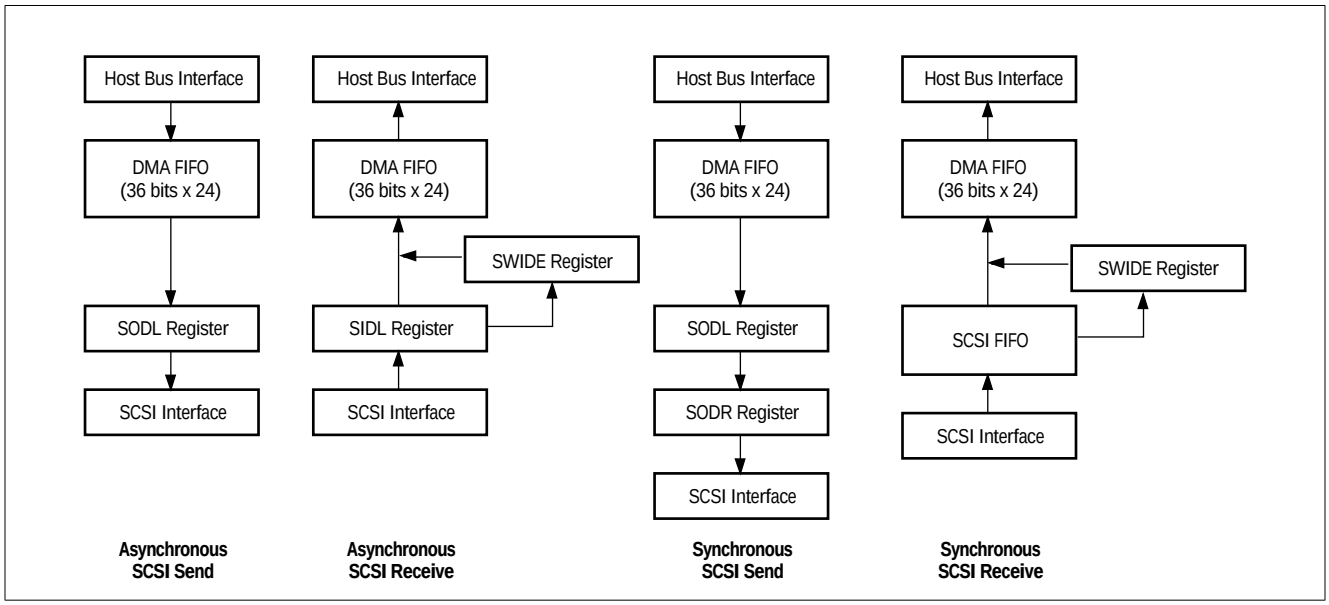


Figure 2-2: SYM53C770 Data Paths

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Host Interface

The SYM53C770 can be interfaced with both 680X0-type and 80X86-type host processors using Big or Little Endian byte ordering, for a total of seven host bus interface modes. The modes are selected with the Bus Mode Select pins, defined in Chapter 3. Refer to Appendix C for detailed information on interfacing the SYM53C770 to the host bus.

Misaligned Transfers

The SYM53C770 accommodates block data transfers beginning or ending on odd byte or odd word addresses in system memory. Such addresses are termed “misaligned.” An odd byte is defined as one in which the address contains A0 = 1; an odd word is defined as one in which the address contains A1 = 1. Misaligned transfers differ depending on the type of transfer and whether they occur at the start or end of the transfer. The SYM53C770 does not perform 24-bit transfers.

Transfer Size Throttling

The burst control logic in the SYM53C770 includes an optional throttling technique which will not allow a size change to occur within a bus ownership. When size throttling is enabled, a new bus ownership will occur each time the transfer changes size. When size throttling is enabled, bit 0 (Snoop Pins Mode) of the CTEST3 register should be clear. Size throttling can be enabled or disabled using the Size Throttle Enable bit, bit 7 in the DCNTL register. Cache line bursting is controlled with the Cache Burst Disable bit, bit 7 in the CTEST0 register.

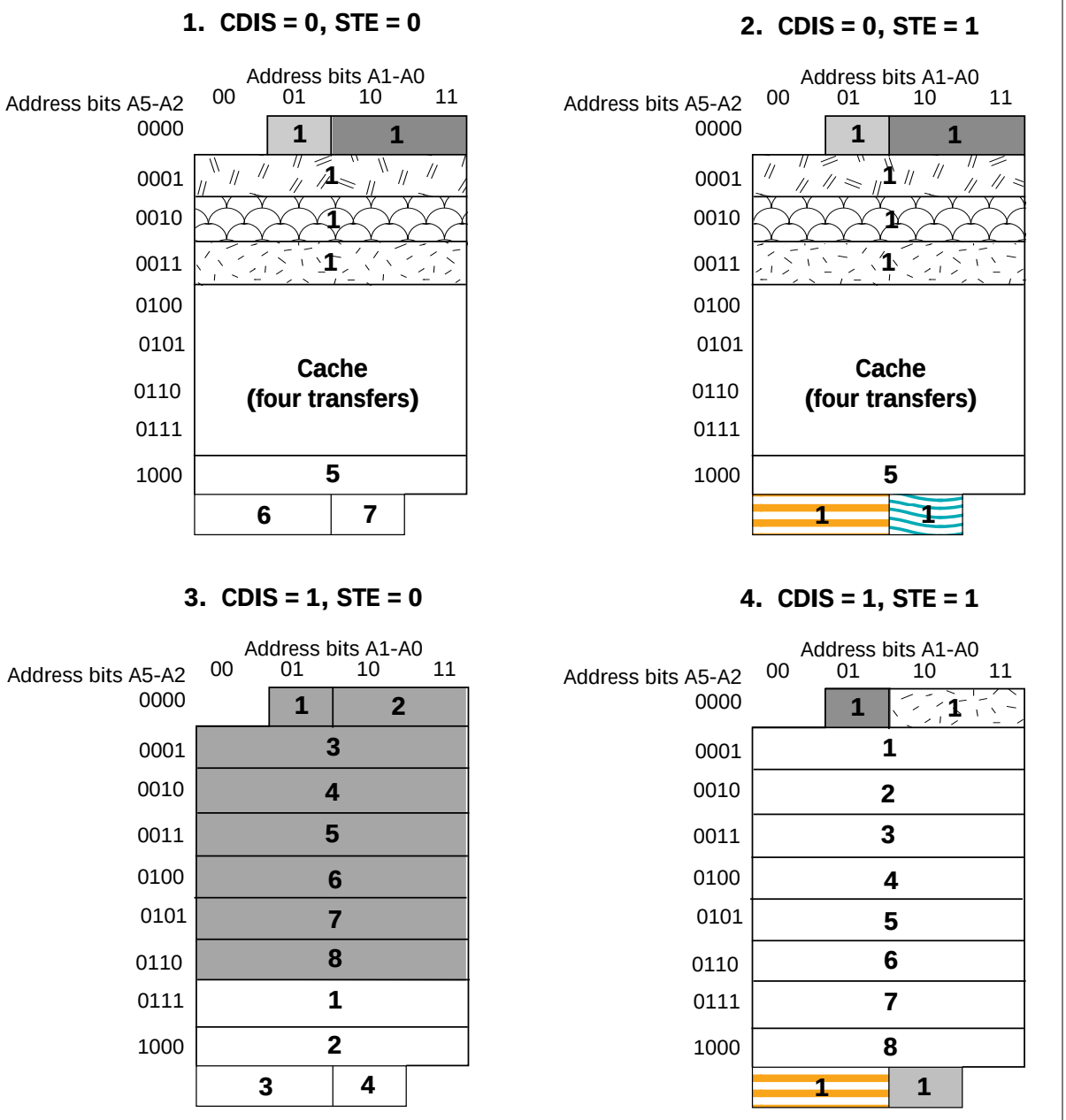
Figure 2-3 illustrates the function of the CDIS and STE bits. In Item 1, cache line bursting is enabled and size throttling is disabled. Since the starting address is at an odd byte boundary, the SYM53C770 lines up to a word boundary by performing a single-byte transfer in a single bus ownership. Then, since the address is at an odd word boundary (bit A1 = 1), the SYM53C770 lines up to a longword boundary by performing a single word transfer in a single bus ownership. At this point, one longword transfer is performed per bus ownership until the address bits line up to a cache line boundary A(3) = A(2) = A(1) = A(0) = 0. Once aligned, the cache line, longword, word and byte are transferred in a single bus ownership to complete the transfer.

In Item 2, cache line bursting and size throttling are enabled. The SYM53C770 lines up to a cache line boundary as described for Figure 1 above. Once aligned, the cache line and longword are transferred in the same bus ownership since the two are considered the same size. The remaining word and byte are transferred in two separate bus ownerships to complete the transfer.

In Item 3, cache line bursting and size throttling are disabled. The SYM53C770 completes eight transfers in one bus ownership, since the burst length is set to eight. The remaining four transfers are transferred in one bus ownership to complete the transfer.

In Item 4, cache line bursting is disabled and size throttling is enabled. The SYM53C770 lines up to a longword boundary. Since the address starts on an odd byte boundary, the SYM53C770 lines up to a word boundary by performing a single byte transfer in a single bus ownership. Then, since the address is at an odd word boundary, the SYM53C770 lines up to a longword boundary by performing a single word transfer in a single bus ownership. Once aligned, longwords are transferred in the same bus ownership. The remaining word and byte are transferred in separate bus ownerships to complete the transfer.

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Notes:
1. CDIS = Cache Burst Disable bit; STE = Size Throttle Enable bit.
2. At the start of the diagram, 38 bytes remain to be transferred.
3. The programmable burst length is 8.
4. Each of the shaded areas represents a new bus ownership.
5. The numbers within the shaded areas represent the number of transfers performed in the bus ownershi
6. For cache alignment and bursting to be attempted, the entire transfer must be at least 31 bytes, this is dictated by chip architecture.

Figure 2-3: Transfer Size Throttling

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BERR/_TEA/ Pin Function

This section describes the function of the BERR/_TEA/ pin on the SYM53C770 SCSI I/O Processor.

Functionality of BERR/_TEA/ in Master Mode

In Master Mode, BERR/_TEA/ is used in conjunction with TA/ to indicate to the SYM53C770 that one of the following conditions has occurred:

TEA/	TA/	Condition
1	1	Execute a wait state
1	0	Normal cycle acknowledge
0	1	Bus error condition has occurred
0	0	Retry the current cycle after relinquishing the bus*

** In Bus Mode 1, the chip will attempt a bus retry operation only if BERR/ is asserted in conjunction with HALT/*

** In Bus Mode 2, the chip will attempt a bus retry operation if TEA/ is asserted in conjunction with TA/.*

Functionality of BERR/_TEA/ in Slave Mode

In Slave Mode the 53C770 responds to requests from an external master in one of the following ways:

TEA/	SLACK/	TA/ *	Condition
1	1	1	Requests the bus master to insert a wait state
1	0	0	Normal cycle acknowledge
0	1	1	Access exception has occurred
0	0	0	Reserved

** TA/ will not be asserted during slave cycles unless the Enable Ack bit in the DCNTL register is set.*

Address exceptions are:

Bus Mode 1: All of the cases mentioned above plus any 3 byte transfer.

Bus Mode 2:
- any misaligned 2-byte transfer (A0 = 1)
- any misaligned longword (A1-A0 not equal to 00)
- any 2-byte transfer in Big Endian mode

Bus Mode 3 and 4: No bus exceptions will occur and the TEA/ pin will never be asserted. One-, two-, three-, and four-byte operations are allowed.

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Bus Retry

Bus Retry allows the SYM53C770 to retry the previous cycle using the same address, size, and other information. Bus retry occurs when an external device asserts the appropriate bus signals, forcing the chip to release the host bus. It will try to regain control of the host bus immediately, without a fairness delay. Once the chip regains control of the host bus, it will retry the previous cycle.

Non-Cache Line Burst

In Bus Mode 1, an external device initiates a bus retry by asserting the HALT/ and BERR/ signals. In Bus Mode 2, the TA/ and TEA/ signals are used to initiate a bus retry. In Bus Modes 3 and 4, a bus retry is initiated by asserting the TEA/and READYI/ signals. When an external device asserts these signals, the SYM53C770 asserts the Bus Request (BR/) signal (Bus Modes 1 and 2) or the HOLD/ signal (Bus Modes 3 and 4). This is done without a fairness delay to try to regain control of the host bus. This repeats indefinitely (as long as the signals remain asserted) until the cycle completes normally, or a bus error occurs. During a non-cache line burst, a bus retry can be executed in any cycle.

Cache Line Burst

During a cache line burst, the bus retry must be executed during the first cycle for the Bus Retry to execute properly in all bus modes.

In Bus Mode 1, if the SYM53C770 is attempting a cache line burst, it will retry the bus cycle and assert Cache Burst Request (CBREQ/) again. If a bus retry is attempted during one of the subsequent cycles of the cache line burst, the SYM53C770 halts the transfer until the HALT/ signal is deasserted. If the Bus Error (BERR/) signal is still asserted at this time, the transfer will abort.

In Bus Mode 2, if the SYM53C770 is attempting a cache line burst, it will retry the bus cycle and assert SIZ0 and SIZ1 again. If a bus retry is attempted during one of the subsequent cycles of the cache line burst, the transfer will abort. If the Transfer Error (TEA/) signal is still asserted at this time, the SYM53C770 will abort the transfer.

In Bus Mode 4 (Bus Mode 3 does not support cache line bursting), if the SYM53C770 is attempting a cache line burst, it will retry the bus cycle and assert Cache Burst Request (CBREQ/) again. If a bus retry is attempted during one of the subsequent cycles of the cache line burst, the SYM53C770 will halt the transfer until the READYI/ signal is asserted. If the TEA/ signal is still asserted at this time, the SYM53C770 will abort the transfer.

If the BERR/ or TEA/ signal is asserted without HALT/, TA/, or READYI/, a Bus Fault interrupt will be generated, which sets bit 5 in the DSTAT register (0Ch). The SYM53C770 will not automatically attempt to regain control of the host bus. A bus retry cannot be attempted during a Preview of Address (PA). For more information on the PA/ signal, refer to Chapter 3 and Chapter 4.

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Using the Back Off Signal to Relinquish the Bus

The SYM53C770 may also relinquish the host bus when the Back Off (BOFF/) signal is asserted. For more information on the operation of this signal, refer to Chapter 3, “Signal Descriptions.” BOFF/ causes the SYM53C770 to release the bus and stay off in accordance with the timings in Chapter 7, “Electrical Characteristics. “Because BOFF/ is sampled only at the beginning and end of each cycle, the SYM53C770 may get off the bus by executing a bus retry, then assert BOFF/ at the end of the cycle to prevent the chip from immediately trying to regain control of the bus. During a backoff or retry, register access functions normally. When the device resumes DMA operation, retried data is transferred.

Bidirectional STERM/-TA/ -ReadyIn/

The STERM/_TA/_ReadyIn/ (referred to in this section as STERM/) signal terminates a read or write cycle. In a typical system, STERM/ is a wired-OR signal driven by slave devices and monitored by bus masters. When the master is faster than the slave device being accessed, a cycle may be terminated as soon as the slave is ready. Slave devices that are faster than the master present a special problem in that they are required to insert wait states to allow the master to catch up. The SYM53C770 can accommodate both situations.

During slave accesses, the SLACK/-ReadyO/ (Referred to as SLACK/) output provides an indication that the SYM53C770 is ready to terminate a read or write cycle. After asserting SLACK/, the SYM53C770 will sample STERM/ on every subsequent rising BCLK edge until it is sampled active, at which time the read/write cycle will be terminated. Any time between SLACK/ and STERM/ is treated as a wait state; a read/write cycle may be stretched indefinitely. However on a write cycle, data is taken into the SYM53C770 before the SLACK/ signal is asserted. Wait states may not be added to allow for late write data.

Typically, SLACK/ is tied back to STERM/ as in Figure 2-4. If the system CPU is not capable of completing a slave cycle in the minimum time required by the SYM53C770, SLACK/ must be delayed before asserting STERM/. If the system CPU is capable of running slave write cycles with zero additional wait states, no delay is necessary.

In systems where the CPU is faster than the SYM53C770, SLACK/ may be connected to STERM/ with external logic, but the best solution is to set the Enable Acknowledge (EA) bit in the DCNTL register to internally connect SLACK/ to STERM. When the EA bit is set, the STERM/ pin changes from being an input in both master and slave modes, and becomes bidirectional: input in master mode, and output in slave mode. This way, no external logic is required and proper timing for

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zero wait state operation is guaranteed. Setting the EA bit must be the first slave I/O access to the SYM53C770. In addition, when the Enable Acknowledge bit is set, a signal with the same timing characteristics as SLACK/ will be driven onto the STERM/_TA/ pin, as illustrated in Figure 2-5. The external timings on this signal will be the same as the signal generated whether or not the EA bit is used. The additional control logic will tristate STERM/_TA/ for 5 ns after it is deasserted. The SLACK/ signal will always be driven.

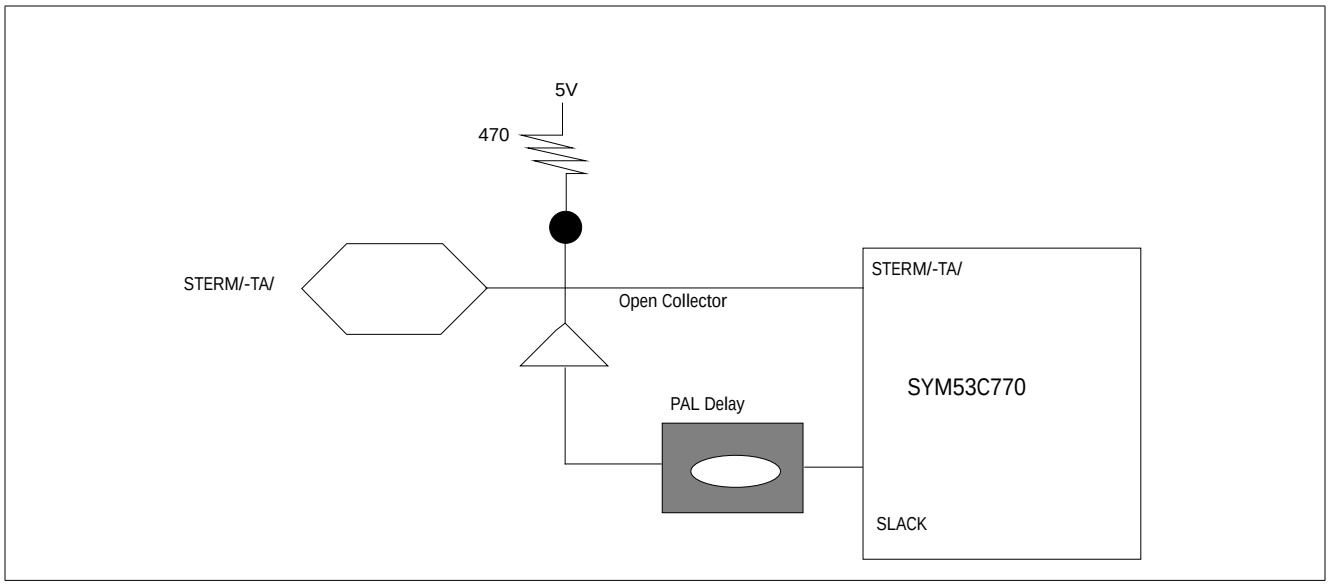


Figure 2-4: SLACK/ tied back to STERM/, EA bit not set

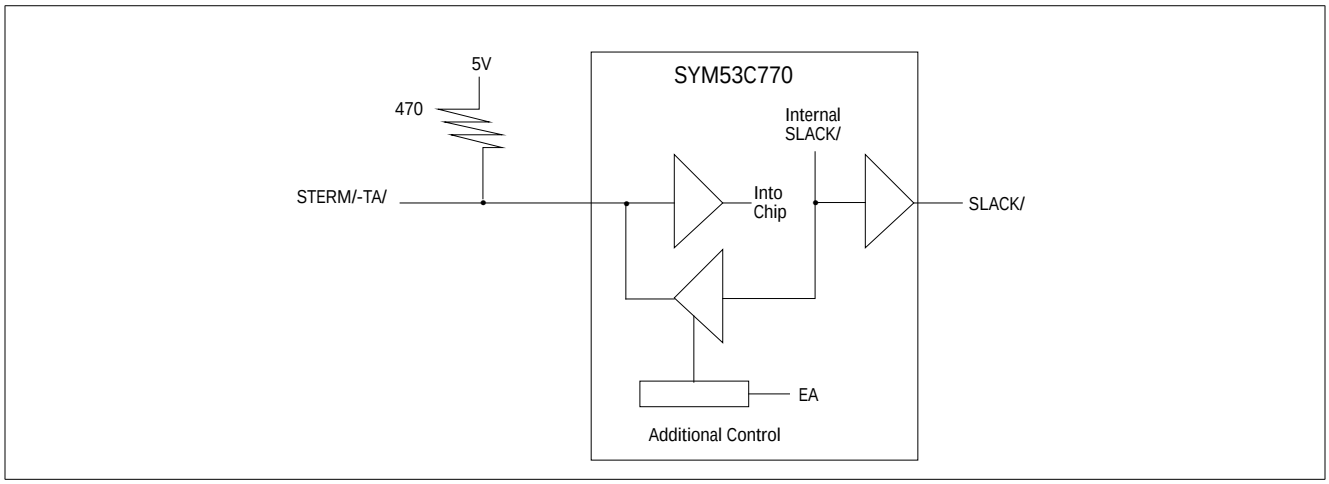


Figure 2-5: Bidirectional STERM/, EA bit set

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SCSI Bus Interface

The SYM53C770 contains open-drain output drivers that can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered-down SYM53C770 has no effect on an active SCSI bus (CMOS "voltage feed-through"). Additionally, Symbios Logic TolerANT provides signal filtering at the inputs of REQ/ and ACK/ to increase immunity to signal reflections.

In differential mode, the SDIR (15-0), SDIRP (1-0), IGS, TGS, RSTDIR, BSYDIR, and SELDIR signals control the direction of external differential pair transceivers. See Figure 2-6 for the suggested differential wiring diagram. The suggested value for the 15 pull-up resistors in the diagram is 1.5K Ω. The pull-up value should be no lower than the transceiver I_{OL} can tolerate, but not so high as to cause RC timing problems.

SCSI Termination

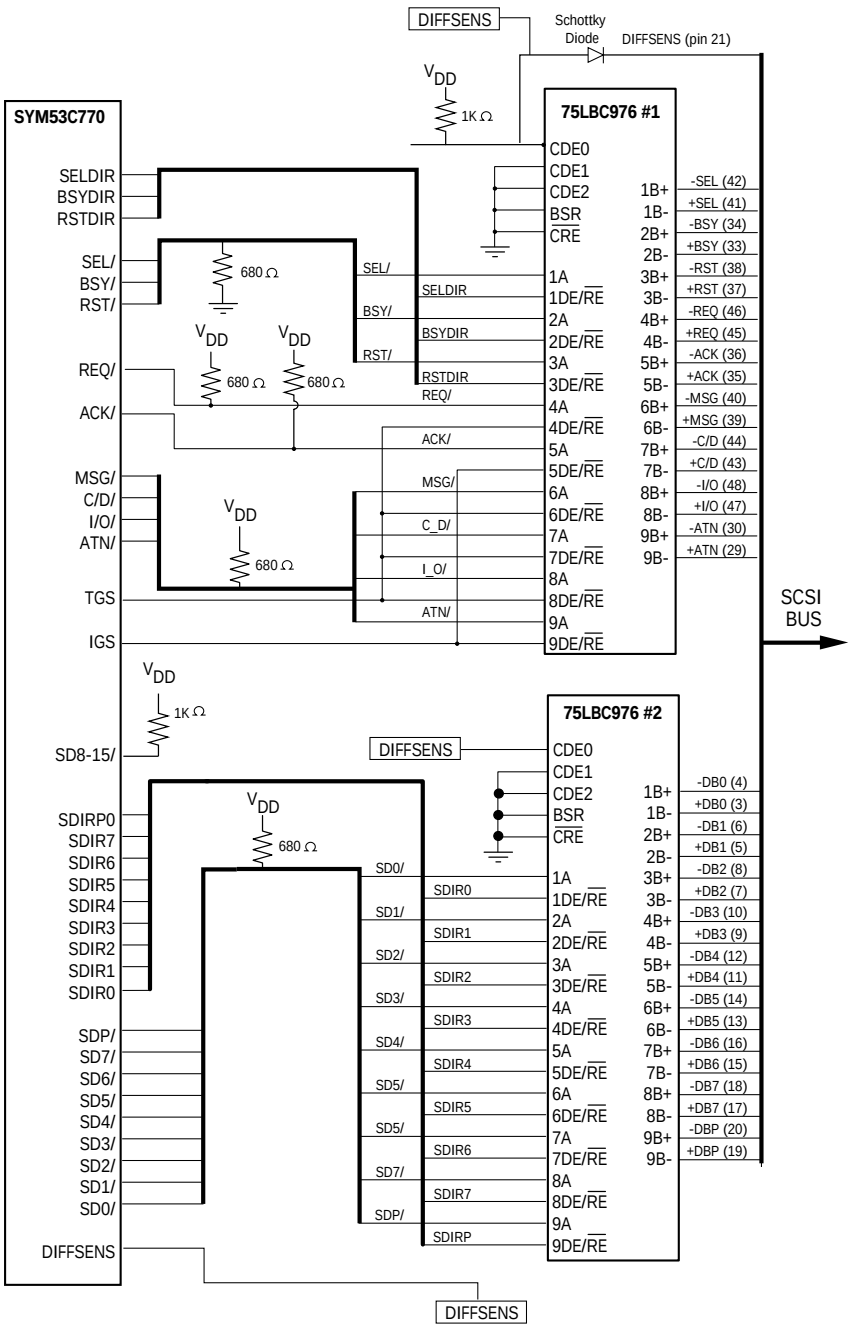
SCSI terminators provide the biasing needed to pull inactive signals to an inactive voltage level, and are required for both single-ended and differential applications. Terminators must be installed at the extreme ends of the SCSI cable, and only at the ends; no system should ever have more or less than two sets of terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so that if not needed they may be removed. Single-ended cables are terminated differently from differential cables. Single-ended cables use a 220 Ω pull-up to the termination power supply (Term-Power) line and a 330 Ω pull-down to Ground. Differential cables use a 330 Ω pull-up from "– SIG" to Term-Power, a 330 Ω pull-down from "+ SIG" to Ground, and a 150 Ω resistor from "– SIG" to "+ SIG".

Because of the high-performance nature of the SYM53C770, Regulated (or Active) termination is recommended. Figure 2-7 shows a Unitrode active terminator. For additional information, refer to the SCSI-2 Specification. TolerANT active negation can be used with any type of termination.

Note: if the SYM53C770 is used in a design with a 8-bit SCSI bus, all 16 data lines must be terminated or pulled high.

Note: active termination is required in single-ended Ultra SCSI systems.

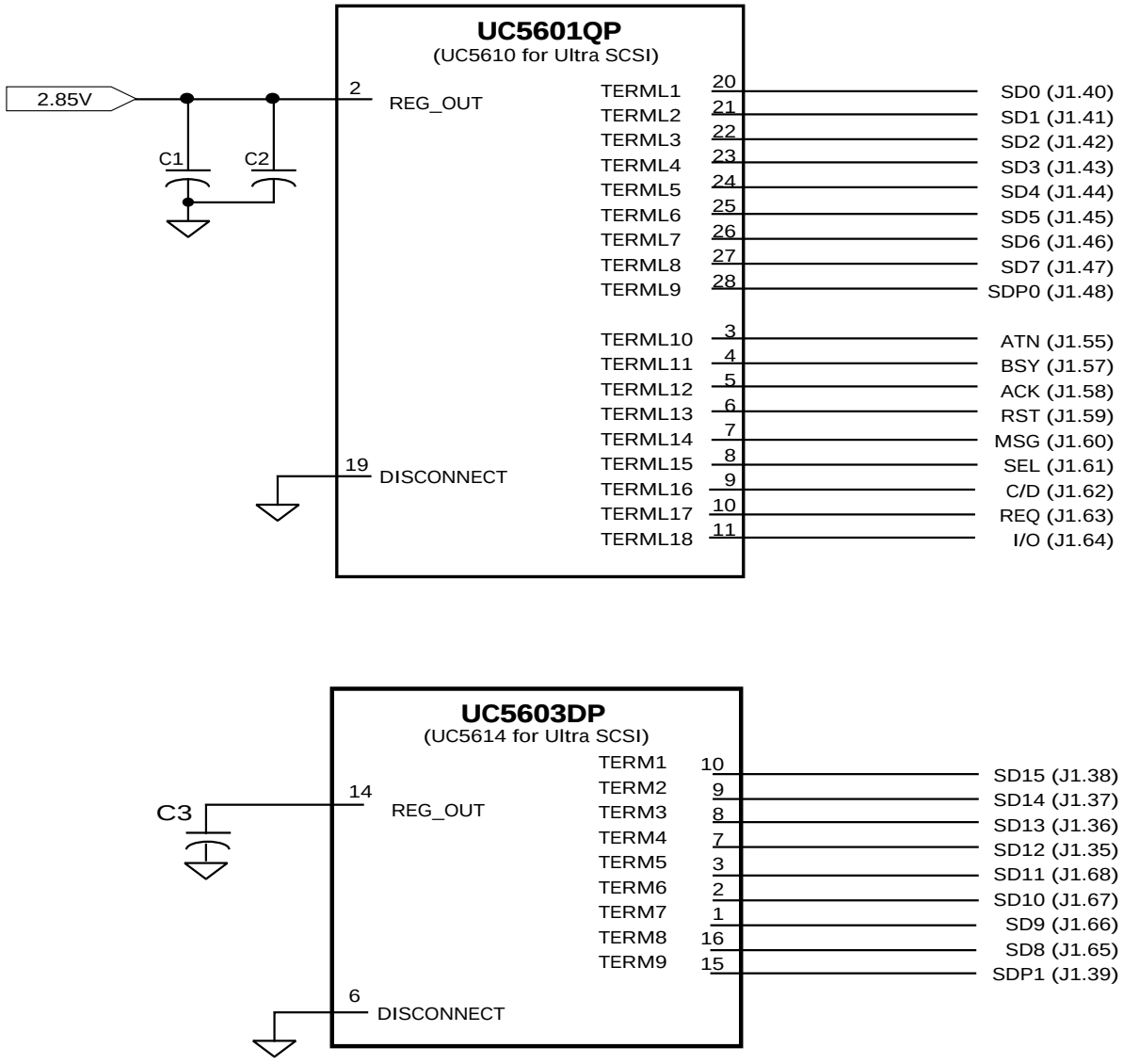
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Note: Use the SN75976A to achieve Ultra SCSI transfer rates.

Figure 2-6: 53C770 Differential Wiring Diagram

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Key

C1	10 µF SMT
C2	0.1 µF SMT
C3	2.2 µF SMT
J1	68-pin, high density “P” connector

Figure 2-7: Regulated Termination

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(Re)Select During (Re)Selection

In multi-threaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select one target and gets reselected by another. The analogous situation for target devices is being selected while trying to perform a reselection. The SCSI SCRIPTS language allows interrupt-free handling of multi-threaded operations. Refer to the *SYM53C770 Programming Guide* for more information on multithreaded operations.

Once a change in operating mode occurs, the initiator SCRIPTS routine should start with a Set Initiator instruction or the target SCRIPTS routine should start with a Set Target instruction. The Enable Response to Selection and Enable Response to Reselection bits (SCID bits 5 and 6, respectively) should both be asserted so that the SYM53C770 may respond as an initiator or as a target.

The selection or reselection enable bits allow the SYM53C770 to respond as either a target or an initiator. For example, if only selection is enabled, the SYM53C770 cannot be reselected as an initiator. There are also interrupt status and interrupt enable bits in the SIST0 and SIEN0 registers respectively, indicating if the SYM53C770 has been selected (bit 5) or reselected (bit 4).

Synchronous Operation

The SYM53C770 transfers synchronous SCSI data in both initiator and target modes. The SXFER register controls both the synchronous offset and the transfer period, and may be loaded by the CPU before SCRIPTS execution begins or from within a SCRIPTS program. The SYM53C770 can always receive data from the SCSI bus at a synchronous transfer period as short as 160 ns for SCSI-1 or 80 ns for SCSI-2, regardless of the transfer period used to send data. Therefore, when negotiating for synchronous data transfers, the suggested transfer period is 80 or 160 ns. Depending on the SCLK frequency and the synchronous clock divider, the SYM53C770 can send synchronous data at intervals as short as 100 or 200 ns.

Determining the Data Transfer Rate

This section is an overview of how the SYM53C770 controls synchronous data transfers. For more information, refer to the full bit descriptions in Chapter 4. Synchronous data transfer rates are controlled by bits in two different registers of the SYM53C770. A brief description of the bits is provided below.
Figure 2-8 illustrates the clock division factors used in each register, and the role of the register bits in determining the transfer rate.

SCNTL3 Register, bits 6-4 (SCF2-0)

The SCF2-0 bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The output from this divider must not exceed 80 MHz. The receive rate is 1/4 of the divider output. For example, if SCLK is 80 MHz and the SCF value is set to divide by two, then the maximum rate at which data can be received is 10 MHz (80/2)/4 = 10.

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SCNTL3 Register, bits 2-0 (CCF2-0)

The CCF2-0 bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI core logic. This divider must be set according to the input clock frequency in the table.

SXFER Register, bit 7-5 (TP2-0)

The TP2-0 bits determine the SCSI synchronous transfer period when sending synchronous SCSI data in either initiator or target mode.

Ultra SCSI Synchronous Data Transfers

Ultra SCSI is simply an extension of current Fast SCSI-2 synchronous transfer specifications. It allows synchronous transfer periods to be negotiated to as low as 50 ns, which is half the 100 ns period allowed under Fast SCSI-2. This will allow a maximum transfer rate of 40 MB/s on a 16-bit SCSI bus. The SYM53C770 requires an 80MHz SCSI clock input to perform Ultra SCSI transfers. In addition, the following bit values affect the chip's ability to support Ultra SCSI synchronous transfer rates:

- Clock Conversion Factor bits, SCNTL3 register bits 2-0 and Synchronous Clock Conversion Factor bits, SCNTL3 register bits 6-4.

  These fields support a value of 101 (binary), allowing the SCLK frequency to be divided down by 4. This allows systems using an 80/100 MHz clock or the internal clock doubler (clock doubler works at 40 to 50 MHz input), to operate at Fast SCSI-2 transfer rates as well as Ultra SCSI rates, if needed.

- Ultra Enable bit, SCNTL 3 register bit 7.

  Setting this bit enables Ultra SCSI synchronous transfers in systems that have an 80MHz clock or that use the SCSI clock doubler.

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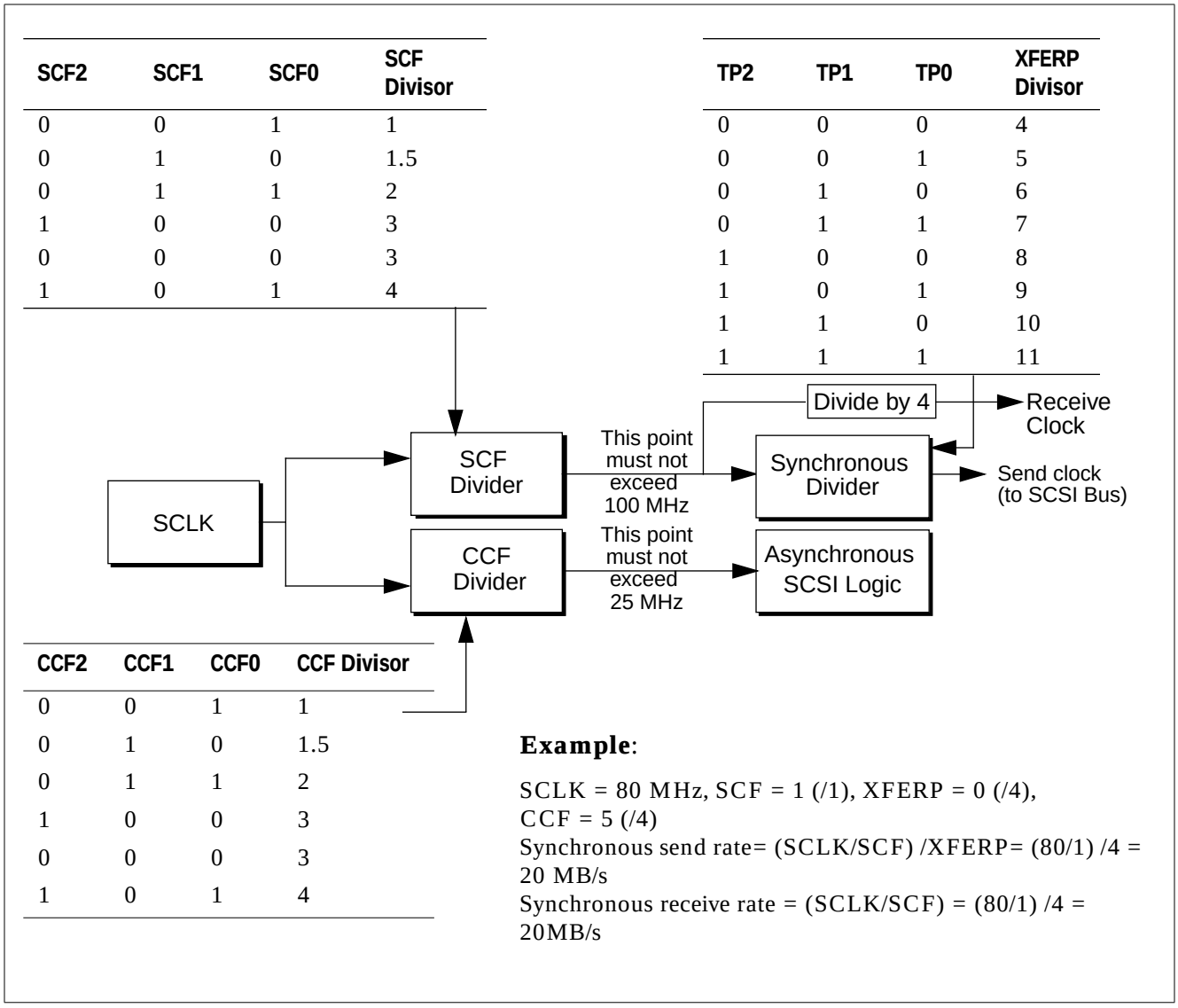


Figure 2-8: Determining the Synchronous Transfer Rate

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Interrupt Handling

The SCRIPTS processor in the SYM53C770 performs most functions independently of the host microprocessor. However, certain interrupt situations must be handled by the external microprocessor. This section explains all aspects of interrupts as they apply to the SYM53C770.

Polling vs. Hardware Interrupts

The external microprocessor can be informed of an interrupt condition by polling or hardware interrupts. Polling means that the microprocessor must continually loop and read a register until it detects a bit set that indicates an interrupt. This method is the fastest, but it wastes CPU time that could be used by other system tasks. The preferred method of detecting interrupts in most systems is hardware interrupts. In this case, the SYM53C770 will assert the Interrupt Request (IRQ/) line which interrupts the microprocessor, causing the microprocessor to execute an interrupt service routine. A hybrid approach would use hardware for long waits, and use polling for short waits.

Registers

The registers in the SYM53C770 that are used for detecting or defining interrupts are the ISTAT, SIST0, SIST1, DSTAT, SIEN0, SIEN1, and DIEN. ISTAT is the only register that can be accessed as a slave during SCRIPTS operation, therefore it is the register that is polled when polled interrupts are used. It is also the first register that should be read when the IRQ/ pin has been asserted in association with a hardware interrupt. The INTF (Interrupt on the Fly) bit should be the first interrupt serviced. To service this interrupt, write a one to the INTF bit. If the SIP bit in the ISTAT register is set, then a SCSI-type interrupt has occurred and the SIST0 and SIST1 registers should be read. If the DIP bit in the ISTAT register is set, then a DMA-type interrupt has occurred and the DSTAT register should be read. SCSI-type and DMA-type interrupts may occur simultaneously, so in some cases both SIP and DIP may be set.

The SIST0 and SIST1 registers contain the SCSI-type interrupt bits. Reading these registers will determine which condition or conditions caused the SCSI-type interrupt, and will clear that SCSI interrupt condition. If the SYM53C770 is receiving data from the SCSI bus and a fatal interrupt condition occurs, the SYM53C770 will attempt to send the contents of the DMA FIFO to memory before generating the interrupt. If the SYM53C770 is sending data to the SCSI bus and a fatal SCSI interrupt condition occurs, data could be left in the DMA FIFO. Because of this the DMA FIFO Empty (DFE) bit in DSTAT should be checked. If this bit is clear, set the CLF (Clear DMA FIFO) and CSF (Clear SCSI FIFO) bits before continuing.

The DSTAT register contains the DMA-type interrupt bits. Reading this register will determine which condition or conditions caused the DMA-type interrupt, and will clear that DMA interrupt condition. Bit 7 in DSTAT, DFE, is purely a status bit; it will not generate an interrupt under any circumstances and will not be cleared when read. DMA interrupts will flush neither the DMA nor SCSI FIFO before generating the interrupt, so the DFE bit in the DSTAT register should be checked after any DMA interrupt. If the DFE bit is clear, then the FIFOs must be cleared by setting the CLF and CSF bits, or flushed by setting the FLF (Flush DMA FIFO) bit. The CLF bit is bit 2 in CTEST3. The FLF bit is bit 3 in CTEST3. The CSF bit is bit 1 in STEST3.

The SIEN0 and SIEN1 registers are the interrupt enable registers for the SCSI interrupts in SIST0 and SIST1. The DIEN register is the interrupt enable register for DMA interrupts in DSTAT.

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Fatal vs. Non-Fatal Interrupts

A fatal interrupt, as the name implies, always causes SCRIPTS to stop running. A non-fatal interrupt will cause SCRIPTS to stop running only if the interrupt is enabled. Interrupt enabling and masking will be discussed later in this section.

All DMA interrupts (indicated by the DIP bit in ISTAT and one or more bits in DSTAT being set) are fatal. Some SCSI interrupts (indicated by the SIP bit in the ISTAT and one or more bits in SIST0 or SIST1 being set) are non-fatal.When the chip is an initiator, only the CMP (Function Complete) and SEL (Selected or Reselected) interrupts are non-fatal.

When operating in Target mode CMP, SEL, and M/A (Target mode: ATN/ active) are non-fatal. Refer to the description for the DHP (Disable Halt on a Parity Error or ATN/ active (Target Mode Only)) bit in the SCNTL1 register to configure the chip's behavior when the ATN/ interrupt is enabled during Target mode operation. The Interrupt on the Fly interrupt is also non-fatal, since SCRIPTS can continue when it occurs. The reason for non-fatal interrupts is to prevent SCRIPTS from stopping when an interrupt occurs that does not require service from the CPU. This prevents an interrupt when arbitration is complete (CMP set), when the SYM53C770 has been selected or reselected (SEL set), when there is a general purpose or handshake to handshake time-out, or when the initiator has asserted ATN (target mode: ATN/ active). These interrupts are not needed for events that occur during high-level SCRIPTS operation.

Enabling Interrupts

In the SYM53C770, the SCSI and DMA Interrupt Enable registers (SIEN and DIEN) are used to enable the various interrupting conditions. The default value of these registers is to disable, or mask, all interrupts. Masking an interrupt means ignoring that interrupt. To mask any of these interrupts, clear the appropriate bits in the SIEN (for SCSI interrupts) registers or DIEN (for DMA interrupts) registers. How the chip will respond to masked interrupts depends on: whether polling or hardware interrupts are being used; whether the interrupt is fatal or non-fatal; and whether the chip is operating in Initiator or Target mode.

If a non-fatal interrupt is masked and that condition occurs, SCRIPTS will not stop, the appropriate bit in the SIST0 or SIST1 will still be set, the SIP bit in the ISTAT will not be set, and the IRQ/ pin will not be asserted. See the section on non-fatal vs. fatal interrupts for a list of the non-fatal interrupts.

If a fatal interrupt is masked and that condition occurs, then SCRIPTS will still stop, the appropriate bit in the DSTAT, SIST0, or SIST1 register will be set, the SIP or DIP bits in the ISTAT will be set, and the IRQ/ pin will not be asserted. When the chip is initialized, enable all fatal interrupts if you are using hardware interrupts. If a fatal interrupt is disabled and that interrupt condition occurs, SCRIPTS will halt and the system will never know it unless it times out and checks the ISTAT after a certain period of inactivity.

If you are polling the ISTAT instead of using hardware interrupts, then masking a fatal interrupt will make no difference since the SIP and DIP bits in the ISTAT inform the system of interrupts, not the IRQ/ pin. Masking an interrupt after IRQ/ is asserted will not cause IRQ/ to be deasserted.

Stacked Interrupts

The SYM53C770 has the ability to stack interrupts if they occur one after the other. If the SIP or DIP bits in the ISTAT register are set (first level), then there is already at least one pending interrupt and any future interrupts will be stacked in extra registers behind the SIST0, SIST1, and DSTAT registers (second level). When two interrupts have occurred and the two levels of the stack are full, any further interrupts will set additional bits in the extra registers behind SIST0, SIST1, and DSTAT. When the first level of interrupts are cleared, all the interrupts that came in afterward will move into the SIST0, SIST1, and DSTAT. After the first

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interrupt is cleared by reading the appropriate register, the IRQ/ pin will be deasserted for a set time as published in Chapter 6; the stacked interrupt(s) will move into the SIST0, SIST1, or DSTAT; and the IRQ/ pin will be asserted once again.

Since a masked non-fatal interrupt will not set the SIP or DIP bits, interrupt stacking will not occur as a result of a masked, non-fatal interrupt. A masked, non-fatal interrupt will still post the interrupt in SIST0 or SIST1, but will not assert the IRQ/ pin. Since no interrupt is generated, future interrupts will move right into the SIST0 or SIST1 instead of being stacked behind another interrupt. When another condition occurs that generates an interrupt, the bit corresponding to the earlier masked non-fatal interrupt will still be set.

A related situation to interrupt stacking is when two interrupts occur simultaneously. Since stacking does not occur until the SIP or DIP bits are set, there is a small timing window in which multiple interrupts can occur but will not be stacked. These could be multiple SCSI interrupts (SIP set), multiple DMA interrupts (DIP set), or a combination of SCSI and DMA interrupts (both SIP and DIP set). As previously mentioned, DMA interrupts will not attempt to flush the FIFOs before generating the interrupt. It is important to set either the CLF (Clear DMA) or CSF (SCSI FIFO) bit if a DMA interrupt occurs and the DFE (DMA FIFO Empty) bit is not set. This is because any future SCSI interrupts will not be posted until the DMA FIFO is clear of data. These ‘locked out’ SCSI interrupts will be posted as soon as the DMA FIFO is empty.

Halting in an Orderly Fashion

When an interrupt occurs, the SYM53C770 will attempt to halt in an orderly fashion. All instructions may halt before completion, except for the ones described below.

- If an interrupt occurs in the middle of an instruction fetch, the fetch will be completed, except in the case of a Bus Fault or Watchdog Time-out. Execution will not begin, but the DSP will point to the next instruction since it is updated when the current SCRIPTS routine is fetched.
- If the DMA direction is a write to memory and a SCSI interrupt occurs, the SYM53C770 will attempt to flush the DMA FIFO to memory before halting. Under any other circumstances only the current cycle will be completed before halting, so the DFE bit in DSTAT should be checked to see if any data remains in the DMA FIFO.
- SCSI REQ/ACK handshakes that have begun will be completed before halting.
- The SYM53C770 will attempt to clean up any outstanding synchronous offset before halting.
- In the case of Transfer Control Instructions, once instruction execution begins it will continue to completion before halting.
- If the instruction is a JUMP/CALL WHEN <phase>, the DSP will be updated to the transfer address before halting.

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Sample Interrupt Service Routine

The following is a sample of an interrupt service routine for the SYM53C770. It can be repeated if polling is used, or should be called when the IRQ/ pin is asserted if hardware interrupts are used.

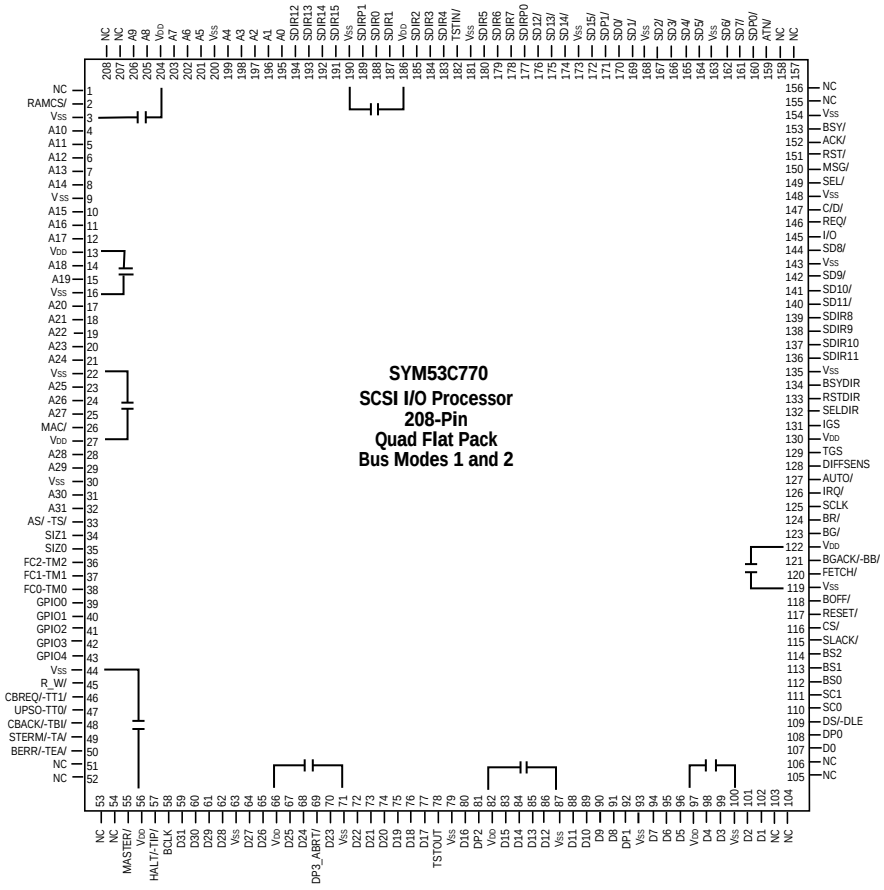
1. Read ISTAT.
2. If the INTF bit is set, it must be written to a one to clear this status.
3. If only the SIP bit is set, read SIST0 and SIST1 to clear the SCSI interrupt condition and get the SCSI interrupt status. The bits in the SIST0 and SIST1 tell which SCSI interrupt(s) occurred and determine what action is required to service the interrupt(s).
4. If only the DIP bit is set, read the DSTAT to clear the interrupt condition and get the DMA interrupt status. The bits in the DSTAT will tell which DMA interrupt(s) occurred and determine what action is required to service the interrupt(s).
5. If both the SIP and DIP bits are set, read SIST0, SIST1, and DSTAT to clear the SCSI and DMA interrupt condition and get the interrupt status. If using 8-bit reads of the SIST0, SIST1, and DSTAT registers to clear interrupts, insert 12 BCLKs between the consecutive reads to ensure that the interrupts clear properly. Both the SCSI and DMA interrupt conditions should be handled before leaving the ISR. The DMA interrupt should be serviced before the SCSI interrupt because a serious DMA interrupt condition could influence how the SCSI interrupt is acted upon.
6. When using polled interrupts, go back to step 1 before leaving the interrupt service routine, in case any stacked interrupts moved in when the first interrupt was cleared. When using hardware interrupts, the IRQ/ pin will be asserted again if there are any stacked interrupts. This should cause the system to re-enter the interrupt service routine.

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Chapter 3

SYM53C770 Signal Descriptions

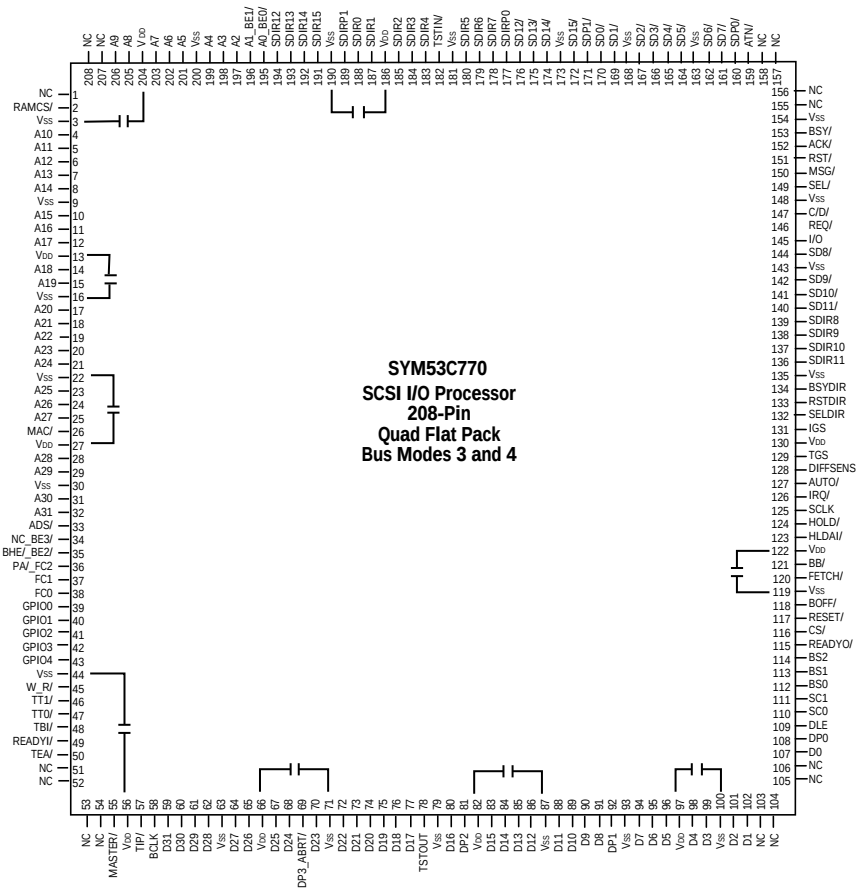
The SYM53C770 host bus can operate in one of four modes: Bus Mode 1 (68030-like), Bus Mode 2 (68040-like), Bus Mode 3 (80386SX-like), and Bus Mode 4 (80386DX-like). Both Big and Little Endian byte ordering are supported in Bus Modes 1, 2, and 4. The bus mode is selected by using the BS(2-0) pins. A function is listed on the table as NC (not connected) if it is not active for a given bus mode. A slash ("/") indicates an active-low signal. All pins have a totem pole (push-pull) architecture unless otherwise noted.



Note: the decoupling capacitor arrangements shown above are recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 µF should provide adequate noise isolation. Because of the number of high current drivers on the SYM53C770, a multi-layer PC board with power and ground planes is required.

Figure 3-1: SYM53C770 Pin Diagram, Bus Modes 1 and 2

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Note: the decoupling capacitor arrangements shown above are recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 µF should provide adequate noise isolation. Because of the number of high current drivers on the SYM53C770, a multi-layer PC board with power and ground planes is required.

Figure 3-2: SYM53C770 Pin Diagram, Bus Modes 3 and 4

Table 3-1: Power and Ground Pins

Symbol	Pin No.	Description
V_{SS}	3, 9, 16, 22, 30, 44, 63, 71, 79, 87, 93, 100, 119, 135, 143, 148, 154, 163, 168, 173, 181, 190, 200	
V_{DD}	13, 27, 56, 66, 82, 97, 122, 130, 186, 204	

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Table 3-2: Address and Data Pins

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave Type, Master Type)
D(31-0)	D(31-0)	D(31-0)	D(31-0)	59-62, 64-65, 67-68, 70, 72-77, 80, 83-86, 88-91, 94-96, 98, 99, 101, 102, 107	*Host Data Bus* (I/O, I/O) —Main data path into host memory for all bus modes. Note: to interface to a 16-bit bus, Bit 3 in the DCNTL register should be set and data lines 31 through 16 should be tied to data lines 15 through 0, respectively.
DP(2-0)	DP(2-0)	DP(2-0)	DP(2-0)	81, 92, 108	*Host Bus Data Parity* (I/O, I/O) In all bus modes: DP0 provides parity for D(7-0) DP1 provides parity for D(15-8) DP2 provides parity for D(23-16) Note: to interface to a 16-bit bus and to support parity, DP3 and DP2 should be tied to DP1 and DP0, respectively.
DP3_ Abort/	DP3_ Abort/	DP3_ Abort/	DP3_ Abort/	69	*Host Bus Data Parity* (I/O, I/O)—In all bus modes, DP3 provides parity for D(31-24). Parity is valid on all byte lanes, including unused lanes. To disable Parity Through mode, set bit 2 in the SCNTL0 register. DP3 becomes a hardware abort input (ABRT/) when Parity Through mode is disabled. When Abort/ is asserted, the SYM53C770 will finish the current transfer, then get off the bus. An abort leaves data in an undetermined state and does not flush the FIFOs.
DS/	DLE	DLE	DLE	109	DS/—*Data Strobe* (Z, O)—In Bus Mode 1, this signal indicates that valid data has been or should be placed on the data lines. It is typically used when data becomes valid asynchronously to the clock. DLE—*Data Latch* Enable (I, I)—In Bus Modes 2, 3, and 4, this signal transparently latches read data into the SYM53C770 prior to an Acknowledge. It is typically used when data becomes valid asynchronously to the clock. Tie this signal high if it is not used.

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Table 3-2: Address and Data Pins (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave Type, Master Type)
A(31-2)	A(31-2)	A(31-2)	A(31-2)	32, 31, 29, 28, 25-23, 21-17, 15, 14, 12-10, 8-4, 206, 205, 203-201, 199-195	*Address Bus* (I, O)—In all bus modes, this signal provides an address bus to the host memory.
A(1-0)	A(1-0)	A(1-0)	BE/(1-0)	196, 1950	A(1-0)—In Bus Modes 1,2, and 3, these pins are part of the address bus. BE/(1-0)—In Bus Mode 4, this signal enables data transfer on the byte lane D(15-8) and D(7-0).
AS/	TS/	ADS/	ADS/	33	AS/—*Address Strobe* (I, O)—In Bus Mode 1, this signal indicates that a valid address is on A(31-0). TS/—*Transfer Start* (I, O)—In Bus Mode 2, Transfer Start indicates that a bus cycle is starting and all of the status and address lines are valid. ADS/—*Address Status* (I, O)—In Bus Modes 3 and 4, this signal indicates that a valid bus cycle definition and address are being driven.

Table 3-3: Arbitration Pins

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No	Description (Slave Type, Master Type)
BR/	BR/	HOLD/	HOLD/	124	BR/—*Bus Request* (O, O)—In Bus Modes 1 and 2, this signal indicates there is a request to use the host bus. HOLD/—*Hold* (O, O)—In Bus Modes 3 and 4, this signal indicates there is a request to use the host bus.
BG/	BG/	HLDAI/	HLDAI/	123	BG/—*Bus Grant* (I, I)—In Bus Modes 1 and 2, this signal indicates that the host bus has been granted to the SYM53C770. HLDAI/—*Hold Acknowledge* (I, I)—In Bus Modes 3 and 4, this signal indicates that the previous bus master has given up use of the host bus.

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Table 3-3: Arbitration Pins (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No	Description (Slave Type, Master Type)
BGACK/	BB/	BB/	BB/	121	BGACK/—*Bus Grant Acknowledge* (Z, I/O)— In Bus Mode 1, this signal indicates that the SYM53C770 or another device has taken control of the host signals. BB/—*Bus Busy* (wire-OR) (Z, I/O)—In Bus Modes 2, 3, and 4, this signal indicates that the SYM53C770 or another device has taken control of the host bus signals.
BOFF/	BOFF/	BOFF/	BOFF/	118	*Back Off* (I, I)— In all bus modes, this forces the SYM53C770 to relinquish bus mastership at the end of the current cycle, if the proper setup timing requirements are met. When BOFF/ is deasserted, a new arbitration will take place and the cycles will resume. BOFF/ is sampled at every start cycle. During worst case operation, if timing is not met it will take the SYM53C770 two clocks to get off the host bus. The start cycle will become a release cycle. If BOFF/ is asserted during arbitration, the SYM53C770 will complete arbitration and get off the bus at the first start cycle.

Table 3-4: System Pins

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
BCLK	BCLK	BCLK	BCLK	58	*Bus Clock* (I, I)—This clock controls all host-related activity in all bus modes.
RESET/	RESET/	RESET/	RESET/	117	*Chip Reset* (I, I)—Forces a full chip reset in all bus modes.
CS/	CS/	CS/	CS/	116	*Chip Select* (I, I)—Selects the SYM53C770 as a slave I/O device in all bus modes. When CS/ is detected: Bus Mode 1—CBACK/ is deasserted Bus Modes 2, 3, 4—TBI/ is asserted
RAMCS/	RAMCS/	RAMCS/	RAMCS/	2	*SCRIPTS RAM Chip Select* (I, I)—When enabled, defines a 4K byte address space for the 4K bytes SCRIPTS RAM. This type of SCRIPTS RAM access is enabled by setting bits 1 and 2 of the CTEST5 register.
IRQ/	IRQ/	IRQ/	IRQ/	126	*Interrupt* (O, O)—In all bus modes, this signal indicates that service is required from the host CPU.

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Table 3-4: System Pins (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
UPSO	TT0/	TT0/	TT0/	47	UPSO—*User Programmable Status* (Z, O)—General purpose line in Bus Mode 1. The value in the register bit is asserted while the chip is bus master. TT0/—*Transfer Type Zero* (Z, O)—In Bus Modes 2, 3, and 4 this signal indicates the current bus transfer type. This pin can be programmed from a register bit (default = 0). It is asserted only when the SYM53C770 is bus master.
SIZ0	SIZ0	BHE/	BE2/	35	SIZ0—*Transfer Size Zero* (I, O)—In Bus Modes 1 and 2, SIZ0 indicates the current transfer size in combination with SIZ1 (see table under the SIZ1 pin description). BHE/—*Byte High Enable* (I, O)—In Bus Mode 3, this signal enables data transfer on the high order byte lane D(15-8). BE2/—*Byte Enable Two* (I, O)—In Bus Mode 4, this signal enables data transfer on byte lane D(23-16).
SIZ1	SIZ1	NC	BE3/	34	SIZ1—*Transfer Size One* (I, O)—In Bus Modes 1 and 2, SIZ1 indicates the current transfer size in combination with the SIZ0 pin, as shown in the table below: **SIZ1, SIZ0** 0,0 Longword (4 bytes) 0,1 Byte (1 byte) 1,0 Word (2-byte slave accesses are allowed, if word-aligned) 1,1 Bus Mode 1, Illegal; Bus Mode 2, Cache Line Burst (since cache line bursts are not supported in slave mode, this size request will result in standard longword slave access). BE3/—*Byte Enable Three* (I, O)—In Bus Mode 4, this signal enables data transfer on byte lane D(31-24).

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Table 3-4: System Pins (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
STERM/	TA/	READYI/	READYI/	49	STERM/—*Synchronous Cycle Termination* (I/O, I)—In Bus Mode 1, this signal acknowledges transfer to a 32-bit wide port. TA/—*Transfer Acknowledge* (I/O, I)—In Bus Mode 2, this signal acknowledges transfer to a 32-bit wide port. READYI/—*Ready In* (I, I)—In Bus Modes 3 and 4 during master mode operation, this signal indicates that the slave device is ready to transfer or receive data. During slave mode, this signal is monitored by the SYM53C770 to determine when to stop driving the bus.

Table 3-5: Interface Control Pins

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
R_W/	R_W/	W_R/	W_R/	45	*Read/Write* (I, O)—Indicates the current direction of the data transfer relative to the current master.
SLACK/	SLACK/	READYO/	READYO/	115	SLACK/—*Slave Acknowledge* (O, O)—Asserted in Bus Modes 1 and 2 to indicate the internal end of a valid slave mode cycle. The external slave cycle ends when the SYM53C770 observes either STERM/-TA/ or BERR/-TEA. READYO/—*Ready Out* (O, O)—Asserted in Bus Modes 3 and 4 to indicate the end of a slave mode cycle.
FC2_PA/	TM2	FC2_PA/	FC2_PA/	36	*Function Codes/Preview of Address, Transfer Modifier* FC2, TM2 (Z, O)—User definable from bit 5 in the DMODE register in conjunction with the Bus Mode bit (bit 6) in the DCNTL register. PA/ (I, I)—This input signal is used to tell the SYM53C770/SE that the system is ready for the next address/value and byte enable signal. FC2 becomes PA/ when the Bus Mode bit (DCNTL bit 6) is set.

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Table 3-5: Interface Control Pins (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
FC(1-0)	TM(1-0)	FC(1-0)	FC(1-0)	37-38	*Function Codes and Transfer Modifiers* For all bus modes: FC0-TM0 (Z, O)—Indicates the status of the current bus cycle. For more information on the operation of this pin, refer to description of the the Program Data bit (DMODE bit 3) in Chapter 4. FC(1)-TM(1) (Z, O)—User definable from bit 4 in the DMODE register in conjunction with bit 6 in the DCNTL register. For more information, refer to the description of the Function Code 1 bit (DMODE bit 4) in Chapter 4.
SC(1-0)	SC(1-0)	SC(1-0)	SC(1-0)	111, 110	*Snoop Control* (Z(O), O)—Indicates the bus snooping level in all bus modes. The bits are user-programmable through register bits. They are asserted when the SYM53C770 is bus master. SC(1-0) may be optionally used as pure outputs, active in both master and slave modes.
MASTER/	MASTER/	MASTER/	MASTER/	55	*Master Status* (O, O)—Driven low when the SYM53C770 becomes bus master. This signal is valid in all bus modes. This signal is driven at all times except when the SYM53C770 is in Z mode
FETCH/	FETCH/	FETCH/	FETCH/	120	*Fetching Op Code* (O, O)—In all bus modes, this signal indicates that the next bus request will be for an op code fetch.
CBREQ/	TT1/	TT1/	CBREQ/	46	CBREQ/—*Cache Burst Request* (Z, O)—In Bus Modes 1 and 4, Cache Burst Request indicates an attempt to execute a line transfer of four longwords. CBREQ/ is valid in Mode 4 only when 386 Cache Mode is enabled (Cache 386 bit, CTEST0 register). TT1/—*Transfer Type Bit One* (Z, O)—Transfer Type bit one is a three-state output line indicating the current bus transfer type in all four bus modes. TT1/ is not valid in Bus Mode 4 if Cache 386 mode is enabled. This bit can be programmed from bit 1 in the CTEST0 register. It is only asserted when the SYM53C770 is bus master.

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Table 3-5: Interface Control Pins (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
CBACK/	TBI/	TBI/	TBI/	48	CBACK/—*Cache Burst Acknowledge* (O, I)—In Bus Mode 1 this signal indicates that the memory system or SYM53C770 can handle a burst request. In slave mode this signal is deasserted in response to CS/. TBI/—*Transfer Burst Inhibit* (O, I)—In Bus Modes 2, 3, and 4 Transfer Burst Inhibit indicates that the memory or the SYM53C770 cannot handle a burst request at this time. In slave mode this signal is asserted in response to CS/.
BS(2-0)	BS(2-0)	BS(2-0)	BS(2-0)	114-112	Bus Mode Select (I, I)—These signals are active in all four bus modes. They select between Motorola/Intel (BS2), Big/Little Endian (BS1), and 386SX/_030 and 386DX/_040 (BS0). **BS2 BS1 BS0 Bus Mode** 0 0 0 80386DX-like, Little Endian, Bus Mode 4 0 0 1 80386SX-like, Little Endian, Bus Mode 3 0 1 0 80386DX-like, Big Endian, Bus Mode 4 0 1 1 Reserved 1 0 0 68040-like, Little Endian, Bus Mode 2 1 0 1 68030-like, Little Endian, Bus Mode 1 1 1 0 68040-like, Big Endian, Bus Mode 2 1 1 1 68030-Like, Big Endian, Bus Mode 1

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Table 3-6: Additional Interface Pins

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, master type)
MAC/	MAC/	MAC/	MAC/	26	*Memory Access Control* (O, O)—This signal indicates if the next access will be to local (on-board) or far (system) memory. When MAC/=1, the memory access is to local memory. When MAC/ = 0, the access is to far memory. The default setting is zero; all accesses are far.
TSTOUT	TSTOUT	TSTOUT	TSTOUT	78	*Test Out* (O, O)—This signal is used to test the connectivity of the SYM53C770 signals using an "AND" tree scheme. The Test Out pin is only driven when the Test In pin is driven low; otherwise the signal is tristated.
TSTIN/	TSTIN/	TSTIN/	TSTIN/	182	*Test In* (I, I)—When this pin is driven low, the SYM53C770 connects all input and outputs (excluding certain SCSI bus signals) to an "AND tree." The SCSI control signals and data lines (SD15-0, SDP1-0, CD/, IO/, MSG/, REQ/, ACK/, BSY/, SEL/, ATN/, RST/, and DIFFSENS) are not connected to the "AND tree." The output of the "AND tree" is connected to the Test Out pin. This allows manufacturers to verify chip connectivity to the board, and to determine exactly which pins are not properly attached. When the TSTIN pin is driven low, internal pull-ups are enabled on all input, output, and bidirectional pins, all outputs and bidirectional signals will be tristated, and the TSTOUT pin will be enabled. Connectivity can be tested by driving one of the SYM53C770 pins low. The TSTOUT pin should respond accordingly by driving low.
BERR/	TEA/	TEA/	TEA/	50	BERR/—*Bus Error Acknowledge* (O, I)—In Bus Mode 1, this indicates that a bus fault has occurred. Used with HALT/ to force a bus retry. Will be asserted on an illegal slave access. TEA/—*Transfer Error* Acknowledge (O, I)—Indicates that a bus fault has occurred in Bus Modes 2, 3, or 4. Used in conjunction with TA/-READYI/ to force a bus retry. Will be asserted on an illegal slave access.

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Table 3-6: Additional Interface Pins (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, master type)
HALT/	TIP/	TIP/	TIP/	57	HALT/—*Halt* (Z, I)—Input only in Bus Mode 1, used with BERR/ to indicate a bus retry cycle. TIP/—*Transfer in Progress* (Z, O)—Output signal for Bus Modes 2, 3, and 4, indicating that bus activity is in progress.
AUTO/	AUTO/	AUTO/	AUTO/	127	*SCRIPTS Autostart Mode* (I, I)—In all bus modes, this signal selects between automatic SCRIPTS and manual SCRIPTS start modes. AUTO/ = 0 Auto start. The DMA SCRIPTS Pointer register (DSP) will point to an address of all zeroes following a chip reset. This address is the starting address of the SCRIPTS instructions. The SCRIPTS instructions will be automatically fetched and executed until an Interrupt instruction occurs. AUTO/ = 1 Manual start. The DSP must be written to so that it points to the starting address of the SCRIPTS instructions. The SCRIPTS instructions will be automatically fetched and executed until an interrupt condition occurs.
GPIO(4-0)	GPIO(4-0)	GPIO(4-0)	GPIO(4-0)	43-39	*General Purpose Input/Output* (I/O, I/O)—In all bus modes, these signals are user-programmable inputs/outputs. GPIO(3-0) power up as inputs, and GPIO4 powers up as an output.

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Table 3-7: SCSI Pins

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
DIFFSENS	DIFFSENS	DIFFSENS	DIFFSENS	128	*Differential Sense* (I, I)—This pin detects the presence of a single-ended device on a differential system. When using external differential transceivers and a zero is detected on this pin, all chip SCSI outputs will be tristated to avoid damage to the transceivers. When running in single-ended mode, this pin should be tied high. The normal value of this pin is 1.
SCLK	SCLK	SCLK	SCLK	125	*SCSI Clock* (I, I)—SCLK is used to derive all SCSI-related timings. The speed of this clock will be determined by the application requirements; in some applications, SCLK and BCLK may be tied to the same source.
SDATA/	SDATA/	SDATA/	SDATA/	172, 174-176, 140-142, 144, 161, 162, 164-167, 169, 170, 171, 160	*SCSI Data* (I/O, I/O)—These open collector signals include the following data lines and parity signals for all bus modes. SD15-0/ 16-bit SCSI data bus SDP1-0/ SCSI data parity pins
SCTRL/	SCTRL/	SCTRL/	SCTRL/	147, 145, 150, 146, 152, 153, 149, 159, 151	Open Collector *SCSI Control* signals (I/O, I/O): C_D/ SCSI phase line, command/data I_O/ SCSI phase line, input/output MSG/ SCSI phase line, message REQ/ Data handshake signal from target device ACK/ Data handshake signal from initiator device BSY/* SCSI bus arbitration signal, signal busy SEL/* SCSI bus arbitration signal, select device ATN/ Attention, the initiator is requesting a message out phase RST/* SCSI bus reset * *Input only in differential mode*

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Table 3-7: SCSI Pins (Continued)

Bus Mode 1	Bus Mode 2	Bus Mode 3	Bus Mode 4	Pin No.	Description (Slave type, Master type)
SDIR(15-0)	SDIR(15-0)	SDIR(15-0)	SDIR(15-0)	191-194, 136-139, 178-180, 183-185, 187, 188	*SCSI Data Direction Control* (O, O)—Differential driver direction control for SCSI data lines.
SDIRP0	SDIRP0	SDIRP0	SDIRP0	177	*SCSI Parity Direction Control* (O, O)—Differential driver direction control for SCSI parity signal (bits 7-0).
SDIRP1	SDIRP1	SDIRP1	SDIRP1	189	*SCSI Parity Direction Control* (O, O)—Differential driver direction control for SCSI parity signal (bits 15-8).
BSYDIR	BSYDIR	BSYDIR	BSYDIR	134	*SCSI BSY/ Control* (O, O)—Differential driver enable control for SCSI BSY/ signal.
SELDIR	SELDIR	SELDIR	SELDIR	132	*SCSI SEL/ Control* (O, O)—Differential driver enable control for SCSI SEL/ signal.
RSTDIR	RSTDIR	RSTDIR	RSTDIR	133	*SCSI RST/ Control* (O, O)—Differential driver enable control for SCSI RST/ signal.
IGS	IGS	IGS	IGS	131	*Initiator Direction Control* (O, O)—Differential driver direction control for initiator driver group.
TGS	TGS	TGS	TGS	129	*Target Direction Control* (O, O)—Differential driver direction control for target driver group.

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Chapter 4
Registers

This chapter describes the SYM53C770 registers. Table 5-1 summarizes the SYM53C770 register set. Figure 5-1, the register map, lists registers by both their Big and Little Endian addresses. The Big Endian address for each register is shown in parentheses. The terms “set” and “assert” are used to refer to bits that are programmed to a binary one. Similarly, the terms “deassert,” “clear” and “reset” are used to refer to bits that are programmed to a binary zero. Reserved bits should always be written to zero; mask all information read from them. Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active high; the feature is enabled by setting the bit.

The bottom of every register diagram shows the default register values, which are enabled after the chip is powered on or reset. Registers can be addressed as bytes, words or longwords. Other access sizes will result in bus errors.

Note: the only register that the host CPU can access while the SYM53C770 is executing SCRIPTS is the ISTAT register; attempts to access other registers will interfere with the operation of the chip. However, all registers are accessible via SCRIPTS.

Table 4-1: SYM53C770 Register Addresses and Descriptions

Little Endian Address	Big Endian Address	Read/ Write	Label	Description	Page
00	03	R./W	SCNTL0	SCSI Control Zero	4-5
01	02	R/W	SCNTL1	SCSI Control One	4-7
02	01	R/W	SCNTL2	SCSI Control Register Two	4-9
03	00	R/W	SCNTL3	SCSI Control Three	4-10
04	07	R/W	SCID	SCSI Chip ID	4-11
05	06	R/W	SXFER	SCSI Transfer	4-12
06	05	R/W	SDID	SCSI Destination ID	4-14
07	04	R/W	GPREG	General Purpose	4-15
08	0B	R/W	SFBR	SCSI First Byte Received	4-15
09	0A	R/W	SOCL	SCSI Output Control Latch	4-16
0A	09	R	SSID	SCSI Selector ID Register	4-16
0B	08	R	SBCL	SCSI Bus Control Lines	4-17
0C	0F	R	DSTAT	DMA Status	4-17
0D	0E	R	SSTAT0	SCSI Status Zero	4-18
0E	0D	R	SSTAT1	SCSI Status One	4-19
0F	0C	R	SSTAT2	SCSI Status Two	4-20

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Table 4-1: SYM53C770 Register Addresses and Descriptions (Continued)

Little Endian Address	Big Endian Address	Read/ Write	Label	Description	Page
10-13	10-13	R/W	DSA	Data Structure Address	4-21
14	17	R/W	ISTAT	Interrupt Status	4-22
18	1B	R/W	CTEST0	Chip Test Zero	4-24
19	1A	R	CTEST1	Chip Test One	4-25
1A	19	R	CTEST2	Chip Test Two	4-26
1B	18	R/W	CTEST3	Chip Test Three	4-27
1C-1F	1C-1F	R/W	TEMP	Temporary Stack	4-28
20	23	R/W	DFIFO	DMA FIFO	4-28
21	22	R/W	CTEST4	Chip Test Four	4-29
22	21	R/W	CTEST5	Chip Test Five	4-30
23	20	R/W	CTEST6	Chip Test Six	4-31
24-26	24-27	R/W	DBC	DMA Byte Counter	4-31
27	24	R/W	DCMD	DMA Command	4-32
28-2B	28-2B	R/W	DNAD	DMA Next Data Address	4-32
2C-2F	2C-2F	R/W	DSP	DMA SCRIPTS Pointer	4-33
30-33	30-33	R/W	DSPS	DMA SCRIPTS Pointer Save	4-33
34-37	34-37	R/W	SCRATCHA	Scratch Register A	4-34
38	3B	R/W	DMODE	DMA Mode	4-34
39	3A	R/W	DIEN	DMA Interrupt Enable	4-36
3A	39	R/W	DWT	DMA Watchdog Timer	4-37
3B	38	R/W	DCNTL	DMA Control	4-37
3C-3F	3C-3F	R	ADDER	Adder Sum Output	4-39
40	43		SIEN0	SCSI Interrupt Enable Zero	4-39
41	42	R/W	SIEN1	SCSI Interrupt Enable One	4-41
42	41	R	SIST0	SCSI Interrupt Status Zero	4-42
43	40	R	SIST1	SCSI Interrupt Status One	4-43
44	47	R/W	SLPAR	SCSI Longitudinal Parity	4-44
45	46	R	SWIDE	SCSI Wide Residue Data	4-45
46	45	R/W	MACNTL	Memory Access Control	4-46
47	44	R/W	GPCNTL	General Purpose Control	4-46
48	4B	R/W	STIME0	SCSI Timer Register	4-47
49	4A	R/W	STIME1	SCSI Timer Register One	4-48
4A	49	R/W	RESPID0	Response ID Zero	4-48
4B	48	R/W	RESPID1	Response ID One	4-48

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Table 4-1: SYM53C770 Register Addresses and Descriptions (Continued)

Little Endian Address	Big Endian Address	Read/ Write	Label	Description	Page
4C	4F	R	STEST0	SCSI Test Register Zero	4-49
4D	4E	R	STEST1	SCSI Test Register One	4-50
4E	4D	R/W	STEST2	SCSI Test Register Two	4-51
4F	4C	R/W	STEST3	SCSI Test Register Three	4-52
50-51	52-53	R	SIDL	SCSI Input Data Latch	4-53
54-55	56-57	R/W	SODL	SCSI Output Data Latch	4-54
58-59	5A-5B	R	SBDL	SCSI Bus Data Lines	4-54
5C-5F	5C-5F	R/W	SCRATCHB	Scratch Register B	4-55
60h-7Fh	60h-7Fh	R/W	SCRATCHC-J	General Purpose Scratch Registers C-J	4-55

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Figure 4-1: SYM53C770 Register Address Map

Big Endian Mode					SCRIPTS and Little Endian Mode
00	SCNTL3	SCNTL2	SCNTL1	SCNTL0	00
04	GPREG	SDID	SXFER	SCID	04
08	SBCL	SSID	SOCL	SFBR	08
0C	SSTAT2	SSTAT1	SSTAT0	DSTAT	0C
10	DSA				10
14	RESERVED			ISTAT	14
18	CTEST3	CTEST2	CTEST1	CTEST0	18
1C	TEMP				1C
20	CTEST6	CTEST5	CTEST4	DFIFO	20
24	DCMD		DBC		24
28	DNAD				28
2C	DSP				2C
30	DSPS				30
34	SCRATCH A				34
38	DCNTL	DWT	DIEN	DMODE	38
3C	ADDER				3C
40	SIST1	SIST0	SIEN1	SIEN0	40
44	GPCNTL	MACNTL	SWIDE	SLPAR	44
48	RESPID1	RESPID0	STIME1	STIME0	48
4C	STEST3	STEST2	STEST1	STEST0	4C
50	RESERVED		SIDL		50
54	RESERVED		SODL		54
58	RESERVED		SBDL		58
5C	SCRATCH B				5C
60	SCRATCH C				60
64	SCRATCHD				64
68	SCRATCHE				68
6C	SCRATCHF				6C
70	SCRATCHG				70
74	SCRATCHH				74
78	SCRATCHI				78
7C	SCRATCHJ				7C

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Register 00 (03)
SCSI Control Zero (SCNTL0)
Read/Write

ARB1	ARB0	START	WATN/	EPC	EPG	AAP	TRG
7	6	5	4	3	2	1	0
Default>>							
1	1	0	0	0	0	0	0

Bit 7 ARB1 (Arbitration mode bit 1)

Bit 6 ARB0 (Arbitration mode bit 0)

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection or reselection

Simple Arbitration

1. The SYM53C770 waits for a bus free condition to occur.
2. It asserts BSY/ and its SCSI ID (contained in the SCID register) onto the SCSI bus. If the SEL/ signal is asserted by another SCSI device, the SYM53C770 will deassert BSY/, deassert its ID and set the Lost Arbitration bit (bit 3) in the SSTAT0 register.
3. After an arbitration delay, the CPU should read the SBDL register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the SYM53C770 has won arbitration.
4. Once the SYM53C770 has won arbitration, it must assert SEL via the SOCL register for a bus clear plus a bus settle delay (1.2 µs). A low level selection can be performed after this delay.

Full Arbitration, Selection/Reselection

1. The SYM53C770 waits for a bus free condition.
2. It asserts BSY/ and its SCSI ID (the ID stored in the SCID register) onto the SCSI bus.
3. If the SEL/ signal is asserted by another SCSI device or if the SYM53C770 detects a higher priority ID, the SYM53C770 will deassert BSY/, deassert its ID, and wait until the next bus free state to try arbitration again.
4. The SYM53C770 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the SSTAT0 register, bit 2.
5. The SYM53C770 performs selection by asserting the following onto the SCSI bus: SEL/, the target's ID (stored in the SDID register) and the SYM53C770's ID (the highest priority ID stored in the SCID register).
6. After a selection is complete, the Function Complete bit is set in the SIST0 register, bit 6.
7. If a selection time-out occurs, the Selection Time-out bit is set in the SIST1 register, bit 2.

Bit 5 START (Start sequence)

When this bit is set, the SYM53C770 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is used in low level mode; when executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor. An arbitration sequence should not be started if the Connected bit, bit 4 in the SCNTL1 register, indicates that SYM53C770 is already connected to the SCSI bus.

This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, bit 4 in the SCNTL1 register should be checked to verify that the SYM53C770 did not connect to the SCSI bus.

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Bit 4 WATN (Select with ATN/ on a start sequence)

When this bit is set and the SYM53C770 is in initiator mode, the SCSI ATN/ signal will be asserted during SYM53C770 selection of a target device. This is to inform the target that the SYM53C770 has a message to send. If a selection time-out occurs while attempting to select a target device, ATN/ will be deasserted at the same time SEL/ is deasserted.

When this bit is clear, the ATN/ signal will not be asserted during selection.

This bit is controlled by the SCRIPTS processor during SCRIPTS execution, but it may be set manually in low level mode.

Bit 3 EPC (Enable parity checking)

When this bit is set, the SYM53C770 checks the SCSI data bus for odd parity when data is received from the SCSI bus in either initiator or target mode. It also checks the host data bus for odd parity if bit 2, the Enable Parity Generation bit, is cleared. Host data bus parity is checked as data is loaded into the SODL register when sending SCSI data in either initiator or target mode. If a parity error is detected, bit 0 of the SSTAT0 register is set and an interrupt may be generated.

If the SYM53C770 is operating in initiator mode and a parity error is detected, it may assert ATN/, but the transfer continues until the target changes phase.

When this bit is cleared, parity errors are not reported.

Bit 2 EPG (Enable parity generation/parity through)

When this bit is set, the SYM53C770 generates SCSI parity. The host data bus parity lines DP(3-0) are ignored and should not be used as parity signals. When this bit is cleared, the parity present on the host data parity lines flows through the SYM53C770's internal FIFOs and is driven onto the SCSI bus when sending data (if the host bus is set to even parity, it is changed to odd before it is sent to the SCSI bus).

This bit enables the DP3_ABRT/ pin to function as an abort input (ABRT/).

Bit 1 AAP (Assert ATN/ on parity error)

When this bit is set, the SYM53C770 automatically asserts the SCSI ATN/ signal when it detects a parity error. ATN/ is only asserted in initiator mode. The ATN/ signal is asserted before deasserting ACK/ during the transfer of the byte with the parity error. The Enable Parity Checking bit must also be set for the SYM53C770 to assert ATN/ in this manner. The following parity errors can occur:

1. A parity error detected on data received from the SCSI bus.
2. A parity error detected on data transferred to the SYM53C770 from the host data bus.

If the Assert ATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, ATN/ will not be automatically asserted on the SCSI bus when a parity error is received.

Bit 0 TRG (Target mode)

This bit determines the default operating mode of the SYM53C770. The user must manually set target or initiator mode. This can be done using the SCRIPTS language (SET target or CLEAR target).

When this bit is set, the chip is a target device by default. When the target mode bit is cleared, the SYM53C770 is an initiator device by default.

CAUTION:

Writing this bit while not connected may cause the loss of a selection or reselection due to the changing of target or initiator roles.

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Register 01 (02)
SCSI Control One (SCNTL1)
Read/Write

EXC	ADB	DHP	CON	RST	AESP	IARB	SST
7	6	5	4	3	2	1	0
Default >>>							
0	0	0	0	0	0	0	0

Bit 7 EXC (Extra clock cycle of data setup)

When this bit is set, an extra clock period of data setup is added to each SCSI send data transfer. The extra data setup time can provide additional system design margin, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time.

Bit 6 ADB (Assert SCSI data bus)

When this bit is set, the SYM53C770 drives the contents of the SCSI Output Data Latch register (SODL) onto the SCSI data bus. When the SYM53C770 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. The low order data and parity signal will always be asserted onto the SCSI bus, whereas the high order data and parity signal will only be asserted onto the SCSI bus if the Enable Wide SCSI bit (SCNTL3, bit 3) is asserted and a data phase is specified by the SCSI phase signals. When the SYM53C770 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the SYM53C770 is connected to the SCSI bus.

This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low level mode.

Bit 5 DHP (Disable Halt on Parity Error or ATN) (Target Only)

The DHP bit is only defined for target mode operation. When this bit is cleared, the SYM53C770 halts the SCSI data transfer when a parity error is detected or when the ATN/ signal is asserted. If ATN/ or a parity error is received in the middle of a data transfer, the SYM53C770 may transfer up to three additional bytes (or words, if wide SCSI is enabled) before halting to synchronize between internal core cells. During synchronous operation, the SYM53C770 will halt when there are no more outstanding synchronous offsets. If the SYM53C770 is receiving data, any data residing in the SCSI or DMA FIFOs is sent to memory before halting. While sending data in target mode with pass parity enabled, the byte with the parity error will not be sent across the SCSI bus.

When this bit is set, the SYM53C770 does not halt the SCSI transfer when ATN/ or a parity error is received.

Bit 4 CON (Connected)

This bit is automatically set any time the SYM53C770 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the SYM53C770 has responded to a bus initiated selection or reselection. It will also be set after successfully completing simple arbitration when operating in low level mode. When this bit is clear, the SYM53C770 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

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Bit 3 RST (Assert SCSI RST/ signal)

Setting this bit asserts the SCSI RST/ signal. The RST/ output remains asserted until this bit is cleared. The 25 µs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor. In differential mode, RST/ becomes an input, and setting this bit causes RSTDIR to be asserted.

Note: setting this bit in SCRIPTS causes a fatal interrupt, which will halt SCRIPTS execution.

Bit 2 AESP (Assert even SCSI parity (force bad parity))

When this bit is set and the Enable Parity Generation bit is set (bit 2 in the SCNTL0 register), the SYM53C770 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the SYM53C770. If parity checking is enabled, then the SYM53C770 checks data received for odd parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.

Bit 1 IARB (Immediate Arbitration)

Setting this bit will cause the SCSI core to immediately begin arbitration once a Bus Free phase is detected following an expected SCSI disconnect. This bit is useful for multi-threaded applications. The ARB1-0 bits in SCNTL0 should be set for full arbitration and selection before setting Immediate Arbitration.

Arbitration will be re-tried until won. At that point, the SYM53C770 will hold BSY and SEL asserted, and wait for a select or reselect sequence to be requested. The Immediate Arbitration bit will be reset automatically when the selection or reselection sequence is completed, or times out.

An unexpected disconnect condition will clear IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit (SCNTL2 bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the Abort bit in the SCRIPTS processor registers should be set. Then one of two things will eventually happen:

1. The Won Arbitration bit (SSTAT0 bit 2) will be asserted. In this case, the Immediate Arbitration bit needs to be reset. This will complete the abort sequence and disconnect the SYM53C770 from the SCSI bus. If it is not acceptable to go to Bus Free phase immediately following the arbitration phase, a low level selection may instead be performed.
2. The abort will complete because the SYM53C770 loses arbitration. This can be detected by the Immediate Arbitration bit being deasserted. The Lost Arbitration bit (SSTAT0 bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

Bit 0 SST (Start SCSI Transfer)

This bit is automatically set during SCRIPTS execution, and should not be used. It causes the SCSI core to begin a SCSI transfer, including REQ/ACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O bit in SOCL. This bit is self-resetting. This bit should not be set for low level operation.

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Register 02 (01)
SCSI Control Register Two (SCNTL2)
Read/Write

SDU	CHM	SLPMD	SLPHBEN	WSS	VUE1	VUE0	WSR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 SDU (SCSI Disconnect Unexpected)

When this bit is set, the SCSI core is not expecting the SCSI bus to enter the Bus Free phase. If it does, an unexpected disconnect error will be generated (see the Unexpected Disconnect bit in the SIST0 register, bit 2).

During normal SCRIPTS mode operation, this bit is set automatically whenever the SCSI core is reselected, or successfully selects another SCSI device. The SDU bit should be reset with a register write (Move 0x7f_&_SCNTL2_to_SCNTL2) before the SCSI core expects a disconnect to occur, normally prior to sending an Abort, Abort Tag, Bus Device Reset, Clear Queue or Release Recovery message, or before deasserting ACK after receiving a Disconnect command or Command Complete message.

Bit 6 CHM (Chained Mode)

This bit determines whether or not the SCSI core is programmed for chained SCSI mode. This bit is automatically set by the Chained Block Move (CHMOV) SCRIPTS instruction and is automatically cleared by the Block Move SCRIPTS instruction (MOVE).

Chained mode is primarily used to transfer consecutive wide data blocks. Using chained mode facilitates partial receive transfers and allows correct partial send behavior. When this bit is set and a data transfer ends on an odd byte boundary, the SYM53C770 will store the last byte in the SCSI Wide Residue Data Register during a receive operation or in the SCSI Output Data Latch register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed.

Bit 5 SLPMD (SLPAR Mode Bit)

If this bit is clear, the SLPAR register functions like the SYM53C720. If this bit is set, the SLPAR register reflects the high or low byte of the SLPAR word, depending on the state of SCNTL2 bit 4. It also allows a seed value to be written to the SLPAR register.

Bit 4 SLPHBEN (SLPAR High Byte Enable)

If this bit is clear, the low byte of the SLPAR word is present in the SLPAR register. If this bit is set, the high byte of the SLPAR word is present in the SLPAR register.

Bit 3 WSS (Wide SCSI Send)

When read, this bit returns the value of the Wide SCSI Send (WSS) flag. Asserting this bit will clear the WSS flag. This clearing function is self-resetting.

When the WSS flag is high following a wide SCSI send operation, the SCSI core is holding a byte of “chain” data in the SODL register. This data will become the first low-order byte sent when “married” with a high-order byte during a subsequent data send transfer.

Performing a SCSI receive operation will clear this bit. Also, performing any non-wide transfer will clear this bit.

Bit 2 VUE1 (Vendor Unique Enhancements bit 1)

This bit is a read only value indicating whether the group code field in the SCSI instruction is standard or vendor unique. If reset, the bit indicates standard group codes; if set, the bit indicates vendor unique group codes. The value in this bit is reloaded at the beginning of all asynchronous target receives. The default for this bit is reset.

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Bit 1 VUE0 (Vendor Unique Enhancements bit 0)

This bit is used to disable the automatic byte count reload during Block Move instructions in the command phase. If this bit is reset, the device will reload the Block Move byte count if the first byte received is one of the standard group codes. If this bit is set, the device will not reload the Block Move byte count, regardless of the group code.

Bit 0 WSR (Wide SCSI Receive)

When read, this bit returns the value of the Wide SCSI Receive (WSR) flag. Asserting this bit will clear the WSR flag. This clearing function is self-resetting.

The WSR flag indicates that the SCSI core received data from the SCSI bus, detected a possible partial transfer at the end of a chained or non-chained block move command, and temporarily stored the high-order byte in the SWIDE register rather than passing the byte out the DMA channel. The hardware uses the WSR status flag to determine what behavior must occur at the start of the next data receive transfer. When the flag is set, the stored data in SWIDE may be "residue" data, valid data for a subsequent data transfer, or overrun data. The byte may be read as normal data by starting a data receive transfer.

Performing a SCSI send operation will clear this bit. Also, performing any non-wide transfer will clear this bit.

Register 03 (00)
SCSI Control Three (SCNTL3)
Read/Write

Ultra	SCF2	SCF1	SCF0	EWS	CCF2	CCF1	CCF0
7	6	5	4	3	2	1	0
Default>>							
0	0	0	0	0	0	0	0

Bit 7 Ultra (Ultra Enable)

Setting this bit enables Ultra SCSI synchronous SCSI transfers in systems that have an 80 MHz clock. The default value of this bit is 0. This bit should remain cleared in systems that have a 40MHz clock, unless the SCSI clock doubler feature is used to increase the SCLK frequency to at least 80 MHz.

When this bit is set, the signal filtering period for SREQ/ and SACK/ automatically changes to 15 ns, regardless of the value of the Extend REQ/ACK Filtering bit in the STEST2 register.

Bits 6-4 SCF2-0 (Synchronous Clock Conversion Factor)

These bits select a factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. They should be written to the same value as the Clock Conversion Factor bits below unless fast SCSI operation is desired. See the table under the description of bits 2-0 of this register for the valid combinations.

Note: for additional information on how the synchronous transfer rate is determined, refer to Chapter 2.

Note: to migrate from a Fast SCSI-2 system with a 40MHz clock, divide the clock by a factor of two or more to achieve the same synchronous transfer rate in a system with an 80MHz clock.

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Bit 3 EWS (Enable Wide SCSI)

When this bit is clear, all information transfer phases are assumed to be eight bits transmitted on SD7-0/, SDP0/. When this bit is set, data transfers are done 16 bits at a time with the least significant byte on SD7-0/, SDP0/ and the most significant byte on SD14-8, SDP1/. Command, status, and message phases remain eight bits.

Bits 2-0 CCF2-0 (Clock Conversion Factor)

These bits select a factor by which the frequency of SCLK is divided before being presented to the SCSI core. The bits are encoded as follows. All other combinations are reserved and should never be used. Also note that the synchronous portion of the SCSI core can be run at a different clock rate for fast SCSI. See the synchronous clock conversion factor bits above.

SCF2 CCF2	SCF1 CCF1	SCF0 CCF0	Factor Frequency	SCSI Clock (MHz)
0	0	0	SCLK/3	50.01-75
0	0	1	SCLK/1	16.67-25
0	1	0	SCLK/1.5	25.01-37.5
0	1	1	SCLK/2	37.51-50
1	0	0	SCLK/3	50.01-75
1	0	1	SCLK/4	75.01-100.00
1	1	0	Reserved	
1	1	1	Reserved	

Note: It is important that these bits be set to the proper values to guarantee that the SYM53C770 meets the SCSI timings as defined by the ANSI specification.

Note: to migrate from a Fast SCSI-2 system with a 40MHz clock, divide the clock by a factor of two or more to achieve the same synchronous transfer rate in a system with an 80MHz clock.

Note: if the SCSI clock doubler is enabled, use the desired frequency after doubling to determine the conversion factor.

Register 04 (07)
SCSI Chip ID (SCID)
Read/Write

RES 7	RRE 6	SRE 5	RES 4	ID3 3	ID2 2	ID1 1	ID0 0
Default>>							
X	0	0	X	0	0	0	0

Bit 7 Reserved

Bit 6 RRE (Enable Response to Reselection)

When this bit is set, the SYM53C770 is able to respond to bus-initiated reselection at the chip ID in the RESPID0 and RESPID1 registers. Note that the SYM53C770 will not automatically reconfigure itself to initiator mode as a result of being reselected.

Bit 5 SRE (Enable Response to Selection)

When this bit is set, the SYM53C770 is able to respond to bus-initiated selection at the chip ID encoded in the RESPID0 and RESPID1 registers. Note that the SYM53C770 will not automatically reconfigure itself to target mode as a result of being selected.

Bit 4 Reserved

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Bits 3-0 Encoded Chip SCSI ID

These bits are used to store the SYM53C770 encoded SCSI ID. This is the ID which the chip will assert when arbitrating for the SCSI bus. The priority of the sixteen possible IDs, in descending order is:

SCSI ID	Binary Encoded Value	Priority
7	0111	highest
6	0110	
5	0101	
4	0100	
3	0011	
2	0010	
1	0001	
0	0000	
15	1111	
14	1110	
13	1101	
12	1100	
11	1011	
10	1010	
9	1001	
8	1000	lowest

Register 05 (06)
SCSI Transfer (SXFER)
Read/Write

TP2 7	TP1 6	TP0 5	MO4 4	MO3 3	MO2 2	MO1 1	MO0 0
Default>>>							
0	0	0	0	0	0	0	0

Note: when using Table Indirect I/O commands, bits 7-5 and 3-0 of this register will be loaded from the I/O data structure.

Note: for additional information on how the synchronous transfer rate is determined, refer to Chapter 2, "Functional Description

Bits 7-5 TP2-0 (SCSI Synchronous Transfer Period)

These bits determine the SCSI synchronous transfer period (XFERP) used by the SYM53C770 when sending synchronous SCSI data in either initiator or target mode. These bits control the programmable dividers in the chip.

Note: for Ultra SCSI transfers, the ideal transfer period is 4, however, 5 is acceptable. Setting the transfer period to a value greater than 5 is not recommended.

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

The synchronous transfer period the SYM53C770 should use when transferring SCSI data is found as in the following example: The SYM53C770 is connected to a hard disk

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which can transfer data at 10 MB/s synchronously. The SYM53C770's SCLK is running at 40 MHz. The synchronous transfer period (SXFERP) is found as follows:

Synchronous Send Rate = (SCLK/SCF)/XFERP

Synchronous Receive Rate = (SCLK/SCF) / 4

Key:

SCLK = SCLK

XFERP = Synchronous transfer period, SCNTL3 bits

SCF = Synchronous Clock Conversion Factor SCNTL3 bits

Examples of synchronous transfer periods for SCSI-1 transfer rates.

CLK (MHz)	SCSI CLK ÷ SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Send Rate (MB/s)	Synch Receive Rate (MB/s)
80	÷ 4	4	200	5	5
80	÷ 4	5	250	4	5
66.67	÷ 3	4	180	5.55	5.55
66.67	÷ 3	5	225	4.44	5.55
50	÷ 2	4	160	6.25	6.25
50	÷ 2	5	200	5	6.25
40	÷ 2	4	200	5	5
37.50	÷ 1.5	4	160	6.25	6.25
33.33	÷ 1.5	4	180	5.55	5.55
25	÷ 1	4	160	6.25	6.25
20	÷ 1	4	200	5	5
16.67	÷ 1	4	240	4.17	4.17

Example transfer periods for fast SCSI-2 and Ultra SCSI transfer rates.

CLK (MHz)	SCSI CLK ÷ SCNTL3 bits 6-4	XFERP	Synch Transfer Period (ns)	Synch Send Rate (MB/s)	Synch Receive Rate (MB/s)
80	÷ 1	4	50	20.0	20.0
80	÷ 2	4	100	10.0	10.0
66.67	÷ 1.5	4	90	11.11	11.11
66.67	÷ 1.5	5	112.5	8.88	8.88
50	÷ 1	4	80	12.5	12.5
50	÷ 1	5	100	10.0	12.5
40	÷ 1	4	100	10.0	10.0
37.50	÷ 1	4	106.67	9.375	9.375
33.33	÷ 1	4	120	8.33	8.33
25	÷ 1	4	160	6.25	6.25
20	÷ 1	4	200	5	5
16.67	÷ 1	4	240	4.17	4.17

Bit 4 Reserved

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Bits 3-0 MO4-MO0 (Max SCSI synchronous offset)

These bits describe the maximum SCSI synchronous offset used by the SYM53C720/SE when transferring synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the SYM53C720/SE. These bits determine the SYM53C720/SE/'s method of transfer for Data In and Data Out phases only; all other information transfers will occur asynchronously.

MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0-Asynchronous
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	X	X	1	Reserved
1	X	1	X	Reserved
1	1	X	X	Reserved

Register 06 (05)
SCSI Destination ID (SDID)
Read/Write

RES 7	RES 6	RES 5	RES 4	ID3 3	ID2 2	ID1 1	ID0 0
Default>>>							
X	X	X	X	0	0	0	0

Bits 7-4 Reserved

Bits 3-0 Encoded Destination SCSI ID bits 3-0

Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases respectively. When executing SCSI SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTS Select or Reselect instruction. The value written should be the binary-encoded ID value. The priority of the 16 possible IDs, in descending order, is:

SCSI ID	Binary Encoded Value	Priority
7	0111	highest
6	0110	
5	0101	
4	0100	
3	0011	
2	0010	
1	0001	
0	0000	
15	1111	
14	1110	
13	1101	
12	1100	
11	1011	
10	1010	
9	1001	
8	1000	lowest

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Register 07 (04)
General Purpose (GPREG)
Read/Write

RES 7	RES 6	RES 5	GPIO4 4	GPIO3 3	GPIO2 2	GPIO1 1	GPIO0 0
Default>>>							
X	X	X	0	1	1	1	1

Bits 7-5 Reserved

Bits 4-0 GPIO4-0 (General Purpose Inputs/ Outputs)

These bits allow the SYM53C770 to detect the input signals of a connected device. The general purpose inputs can be used to sense the SYM53C770 chip ID or board configuration at power up. A Register-to-Register Move instruction may be used to move the sensed value into the appropriate register. These are live signals; if the pin is changing, the data is also changing. The bit values in the General Purpose Control Register (47h) determine whether these bits are inputs or outputs.

Bits 3-0 power up as inputs, and Bit 4 powers up as an output. The general purpose output feature may be used to enable attached ROM, RAM, LEDs, or other components on an SYM53C770 board.

Note: the input pins all have 100 µA internal pull-ups.

Register 08 (0B)
SCSI First Byte Received (SFBR)
Read/Write

7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-0 1B7-0 (First byte received)

This register contains the first byte received in any asynchronous information transfer phase. For example, when the SYM53C770 is operating in initiator mode, this register contains the first byte received in Message In, Status, and Data In phases.

When a Block Move Instruction is executed for a particular phase, the first byte received is stored in this register— even if the present phase is the same as the last phase. The first byte value received for a particular input phase is not valid until after a Move instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

This register also holds the state of the lower eight bits of the SCSI data bus during a selection or reselection, unless the COM bit in the DCNTL register is set.

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Register 09 (0A)
SCSI Output Control Latch (SOCL)
Read /Write

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 REQ (Assert SCSI REQ/ signal)

Bit 6 ACK (Assert SCSI ACK/ signal)

Bit 5 BSY (Assert SCSI BSY/ signal)

Bit 4 SEL (Assert SCSI SEL/ signal)

Bit 3 ATN (Assert SCSI ATN/ signal)

Bit 2 MSG (Assert SCSI MSG/ signal)

Bit 1 C/D (Assert SCSI C_D/ signal)

Bit 0 I/O (Assert SCSI I_O/ signal)

This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SOCL should only be used when transferring data via programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the SYM53C770 starts executing SCSI SCRIPTS.

Register 0A (09)
SCSI Selector ID Register (SSID)
Read Only

VAL	Reserved			Encoded SCSI Destination ID			
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

Bit 7 VAL (SCSI Valid Bit)

If VAL is asserted, the two SCSI IDs were detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID was present and the contents of the encoded destination ID are meaningless.

Bits 6-4 Reserved

Bits 3-0 Encoded Destination SCSI ID

Reading the SSID register immediately after the SYM53C770 has been selected or reselected returns the binary-encoded SCSI ID of the device which performed the operation. These bits are invalid for targets that are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit, bit 7.

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Register 0B (08)
SCSI Bus Control Lines (SBCL)
Read Only

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

Bit 7 REQ (REQ/ status)

Bit 6 ACK (ACK/ status)

Bit 5 BSY (BSY/ status)

Bit 4 SEL (SEL/ status)

Bit 3 ATN (ATN/ status)

Bit 2 MSG (MSG/ status)

Bit 1 C/D (C_D/ status)

Bit 0 I/O (I_O/ status)

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read; they may change while being read. This register can be used for diagnostics testing or operation in low level mode.

Register 0C (0F)
DMA Status (DSTAT)
Read Only

DFE	HPE	BF	ABRT	SSI	SIR	WTD	IID
7	6	5	4	3	2	1	0
Default>>>							
1	0	0	0	0	0	0	0

Reading this register will clear any of bits 6-0 at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the SYM53C770 stacks interrupts). The DIP bit in the ISTAT register will also be cleared. DMA interrupt conditions may be individually masked through the DIEN register.

When performing consecutive 8-bit reads of the DSTAT, SIST0 and SIST1 registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. To avoid missing a SCSI interrupt while reading any of these registers when the ISTAT SIP and DIP bits may not be set, read SIST0 and SIST1 before DSTAT.

Bit 7 DFE (DMA FIFO empty)

This status bit is set when the DMA FIFO is empty. This bit may be changing at the time this register is read. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and will not cause an interrupt. This bit is not cleared by reading the register.

Bit 6 HPE (Host Parity Error)

This bit is set when a host bus parity error is detected during a slave write or DMA read operation.

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Bit 5 BF (Bus fault)

This bit is set when a host bus fault condition is detected. A host bus fault can only occur when the SYM53C770 is bus master, and is defined as a memory cycle that is ended by the assertion of BERR/ or TEA/.

Bit 4 ABRT (Aborted)

This bit is set when an abort condition occurs. An abort condition occurs because of the following: the DP3_ABRT/ input signal is asserted by another device (parity generation mode) or a software abort command is issued by setting bit 7 of the ISTAT register.

Bit 3 SSI (SCRIPTS step interrupt)

If the Single-Step Mode bit in the DCNTL register is set, this bit will be set and an interrupt generated after successfully executing each SCRIPTS instruction.

Bit 2 SIR (SCRIPTS interrupt instruction received)

This status bit is set whenever a SCRIPTS Interrupt instruction is received.

Bit 1 WTD (Watchdog time-out detected)

This status bit is set when the watchdog timer decrements to zero. The watchdog timer is only used for the host memory interface. When the timer decrements to zero, it indicates that the memory system did not assert the acknowledge signal within the specified time-out period.

Bit 0 IID (Illegal instruction detected)

This status bit will be set any time an illegal instruction is detected, whether the SYM53C770 is operating in single-step mode or automatically executing SCSI SCRIPTS.

This bit will also be set if the SYM53C770 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.

Register 0D (0E)
SCSI Status Zero (SSTAT0)
Read Only

ILF	ORF	OLF	AIP	LOA	WOA	RST/	SDP/
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 ILF (SIDL least significant byte full)

This bit is set when the least significant byte in the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

Bit 6 ORF (SODR least significant byte full)

This bit is set when the least significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It cannot be read or written by the user. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 5 OLF (SODL least significant byte full)

This bit is set when the least significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SODR register before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous

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transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 4 AIP (Arbitration in progress)
Arbitration in Progress (AIP = 1) indicates that the SYM53C770 has detected a Bus Free condition, asserted BSY, and asserted its SCSI ID onto the SCSI bus.

Bit 3 LOA (Lost arbitration)
When set, LOA indicates that the SYM53C770 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.

Bit 2 WOA (Won arbitration)
When set, WOA indicates that the SYM53C770 has detected a Bus Free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCNTL0 register must be full arbitration and selection for this bit to be set.

Bit 1 RST/ (SCSI RST/ signal)
This bit reports the current status of the SCSI RST/ signal, and the RST signal (bit 6) in the ISTAT register. This bit is not latched and may be changing when read.

Bit 0 SDP0/ (SCSI SDP0/ parity signal)
This bit represents the active high current status of the SCSI SDP0/ parity signal. This signal is not latched and may be changing as it is read.

Register 0E (0D)
SCSI Status One (SSTAT1)
Read Only

FF3	FF2	FF1	FF0	SDP	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	X	X	X	X

Bits 7-4 FF3-0 (FIFO flags)

FF4 (SSTAT2 Bit 4)	FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16

These five bits define the number of bytes or words that currently reside in the SYM53C770's SCSI synchronous data FIFO. These bits are not latched and they will change as data moves through the FIFO.

Bit 3 SDP0 (Latched SCSI parity)
This bit reflects the SCSI parity signal (SDP0) corresponding to the data latched in the SCSI Input Data Latch register (SIDL). It changes

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when a new byte is latched into the least significant byte of the SIDL register. This bit is active high, i.e., it is set when the parity signal is active.

Bit 2 MSG (SCSI MSG/ signal)

Bit 1 C/D (SCSI C_D/ signal)

Bit 0 I/O (SCSI I_O/ signal)

These SCSI phase status bits are latched on the asserting edge of REQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low level mode.

Register 0F (0C)
SCSI Status Two (SSTAT2)
Read Only

ILF1	ORF1	OLF1	FF4	SPL1	DIFF	LDSC	SDP1
7	6	5	4	3	2	1	0
Default: >>>							
0	0	0	0	X	0	1	X

Bit 7 ILF1 (SIDL most significant byte full)

This bit is set when the most significant byte in the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through the SIDL register.

Bit 6 ORF1 (SODR most significant byte full)

This bit is set when the most significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is not accessible to the user. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 5 OLF1 (SODL most significant byte full)

This bit is set when the most significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SODR register before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

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Bit 4 FF4 (FIFO Flags bit 4)
This is the most significant bit in the SCSI FIFO Flags field, with the rest of the bits in SSTAT1. For a complete description of this field, see the definition for SSTAT1 bits 7-4.

Bit 3 Latched SCSI parity for SD15-8
This active high bit reflects the SCSI odd parity signal corresponding to the data latched into the most significant byte in the SIDL register.

Bit 2 DIFFSENSE SENSE
If this bit is reset, the correct cable type has been connected for the differential operation. If this bit is set, a single ended cable has been connected to the device's DIFFSENSE pin.

Bit 1 LDSC (Last Disconnect)
Used in conjunction with the Connected (CON) bit in SCNTL1, this status bit allows the user to detect the case in which a target device disconnects, and then some SCSI device selects or reselects, the SYM53C770. If the Connected bit is asserted and the LDSC bit is asserted, a disconnect has occurred. This bit is set when the Connected bit in SCNTL1 is off. This bit is cleared when a Block Move instruction is executed while the Connected bit in SCNTL1 is on.

Bit 0 SDP1 (SCSI SDP1 Signal)
This bit represents the active-high current state of the SCSI SDP1 parity signal. It is unlatched and may be changing as it is read.

Registers 10-13 (10-13)
Data Structure Address (DSA)
Read/Write

This 32-bit register contains the base address used for all table indirect calculations. During any Memory-to-Memory Move operation, the contents of this register are shadowed.

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Register 14 (17)
Interrupt Status (ISTAT)
Read/Write

ABRT	RST	SIGP	SEM	CON	INTF	SIP	DIP
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the SYM53C770 is executing SCRIPTS (without interfering in the operation of the SYM53C770). It may be used to poll for interrupts if interrupts are disabled. There may be stacked interrupts pending; read this register after clearing an interrupt to check for stacked interrupts.

Bit 7 ABRT (Abort operation)

Setting this bit aborts the current operation being executed by the SYM53C770. If this bit is set and an interrupt is received, reset this bit before reading the DSTAT register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1. Set this bit
2. Wait for an interrupt
3. Read the ISTAT register
4. If the SCSI Interrupt Pending bit is set, then read the SIST0 or SIST1 register to determine the cause of the SCSI Interrupt and go back to Step 2
5. If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 00h value to this register
6. Read the DSTAT register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

Note: the abort function cannot be used during a select or reselect instruction. In these cases, the time-out feature should be used.

After an abort, follow the data recovery steps in Chapter 2 to make sure no data is left in the chip.

Bit 6 RST (Software reset)

Setting this bit resets the SYM53C770. All registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit). This reset will not clear the Enable Acknowledge (EA) bit, Function Code 1 bit, or the ID Mode bit—DCNTL, bit 0.

Bit 5 SIGP (Signal process)

SIGP is a R/W bit that can be written at any time, and polled and reset via CTEST2. The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPT.

The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/ Reselection. Setting this bit causes that op code to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/ reselection condition. For more information on the SIGP bit, refer to the *SYM53C720/SE/53C770 Programming Guide*.

Bit 4 SEM (Semaphore)

This bit can be set by the SCRIPTS processor using a SCRIPTS register write instruction. The bit may also be set by an external processor while the SYM53C770 is executing a SCRIPT. This bit enables the SYM53C770 to notify an external processor of a predefined condition while SCRIPTS are running. The external processor may also notify the SYM53C770 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

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Bit 3 CON (Connected)

This bit is automatically set any time the SYM53C770 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the SYM53C770 has responded to a bus-initiated selection or reselection. It will also be set after successfully completing arbitration when operating in low level mode. When this bit is clear, the SYM53C770 is not connected to the SCSI bus.

Bit 2 INTF (Interrupt on the Fly)

This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. This bit can be used to notify a service routine running on the main processor while the SCRIPTS processor is still executing a SCRIPTS program.

Note: this bit must be written to one in order to clear it after it has been set.

Note: if the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip status registers. An interrupt on the fly interrupt must be cleared before servicing any other interrupts indicated by SIP or DIP.

Bit 1 SIP (SCSI interrupt pending)

This status bit is set when an interrupt condition is detected in the SCSI portion of the SYM53C770. The following conditions will cause a SCSI interrupt to occur:

- A phase mismatch (initiator mode) or ATN/ becomes active (target mode)
- An arbitration sequence is complete
- A selection or reselection time-out occurs
- The SYM53C770 was selected
- The SYM53C770 was reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected
- The handshake-to-handshake timer is expired
- The general purpose timer is expired

To determine exactly which condition(s) caused the interrupt, the SIST0 and SIST1 registers should be read. Both registers must be read to clear the interrupt.

This bit is synchronous to BCLK, but may change during read cycles.

Bit 0 DIP (DMA interrupt pending)

This status bit is set when an interrupt condition is detected in the DMA portion of the SYM53C770. The following conditions will cause a DMA interrupt to occur:

- A host parity error is detected
- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single-step mode
- A SCRIPTS interrupt instruction is executed
- The Watchdog Timer decrements to zero
- An illegal instruction is detected

To clear DIP and determine exactly which condition(s) caused the interrupt, read the DSTAT register.

This bit is synchronous to BCLK, but may change during read cycles.

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Register 18 (1B)
Chip Test Zero (CTEST0)
Read/Write

CDIS	SC1	SC0	GRP	DFP	EHP	TT1	C386E
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	X	0	0	0

Bit 7 CDIS (Cache burst disable)

When this bit is set, the SYM53C770 will not request a cache line burst. When this bit is clear, the chip will attempt cache line bursts when all necessary conditions are met.

Note: if the hardware does not support cache-line bursts, this bit should be set to maximize performance.

Bits 6-5 SC1-0 (Snoop control)

The values of these bits are asserted on the corresponding device pins during bus mastership if bit 0 of CTEST3 is clear. Otherwise, the SC1 pin will always be driven with the value of the SC1 bit, and the SC0 pin will reflect the state of the internal host cycle request signal. These bits are not available for snoop mode if the Size Throttle Enable bit (DCNTL1, bit 7) is set.

Bit 4 GRP (Generate Receive Parity)

When this bit is set and the SYM53C770 is in parity pass through mode (Bit 2 in the SCNTL0 register is clear), parity received on the SCSI bus will not pass through the DMA FIFO. Parity will be generated as data enters the DMA FIFO, eliminating the possibility of bad SCSI parity passing through to the host bus. A SCSI parity error interrupt will be generated but a system parity problem will not be created. After reset or when the bit is cleared, and when parity pass through mode is enabled (Bit 2 in SCNTL0 is clear), parity received on the SCSI bus will pass through the SYM53C770 unmodified.

Bit 3 DFP (DMA FIFO parity)

This bit represents the parity bit of the DMA FIFO when reading data out of the DMA FIFO via programmed I/O. In order to transfer data to or from the DMA FIFO, perform a read or a write to the CTEST6 register. Manually loading the FIFO moves this bit into the FIFO as the parity bit, along with the byte that came was written to the CTEST6 register. For the details of performing a diagnostic test of the DMA FIFO, refer to the *SYM53C720/SE/53C770 Programming Guide*.

Bit 2 EHP (Even host parity)

Parity is generated for all slave mode register reads and master mode memory writes. This bit controls the parity sense.

Setting this bit causes the SYM53C770 to generate even parity when driving data on the host data bus. The SYM53C770 inverts the parity bit received from the SCSI bus to create even parity. In addition, the even parity received from the host bus is inverted to odd parity before the SYM53C770 checks parity and sends the data to the SCSI bus. Clearing this bit causes the SYM53C770 to maintain odd parity throughout the chip.

Bit 1 TT1 (Transfer type bit)

The inverted value of this bit is asserted on the TT1 pin during bus mastership in Bus Modes 2, 3 and 4 only. This bit is not used in Bus Mode 1. In Bus Mode 4, the TT1 pin is supported only if Cache 386 mode is not enabled. The TT0 bit is in the DMODE register.

Bit 0 C386E (Cache 386 Enable)

Asserting this bit enables caching in the 80386DX bus mode. Caching implies that the chip will supply an address together with an Address Strobe (ADS/), and on the consecutive clocks the SYM53C770 will wait for four READYI/ pulses and will either supply four longwords of data or receive four longwords of data. The SYM53C770 does not support caching in 80386SX mode or slave mode. The chip

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generates the Cache Burst Request (CBREQ) signal and samples the Transfer Burst Inhibit (TBI) signal during the first data transfer (first READYI/). CBREQ/ indicates an attempt to execute a line transfer of four longwords. TBI/ asserted indicates that the system memory does not support the SYM53C770 burst request. The chip powers up with this feature disabled. The bit will be reset during either a software or hardware reset.

Register 19 (1A)
Chip Test One (CTEST1)
Read Only

FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFl0
7	6	5	4	3	2	1	0
Default >>>							
1	1	1	1	0	0	0	0

Bits 7-4 FMT3-0 (Byte Empty in DMA FIFO)

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 will be set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

Bits 3-0 FFL3-0 (Byte Full in DMA FIFO)

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 will be set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

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Register 1A (19)
Chip Test Two (CTEST2)
Read Only

DDIR	SIGP	RES	RES	DFP	TEOP	DREQ	DACK
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	X	0	0	0	1

Bit 7 DDIR (Data Transfer Direction)
This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus.

Bit 6 SIGP (Signal process)
This bit is a copy of the SIGP bit in the ISTAT register (bit 5). The SIGP bit is used to signal a running SCRIPTS operation. When this register is read, the SIGP bit in the ISTAT register is cleared.

Bit 5 Reserved

Bit 4 Reserved

Bit 3 DFP (DMA FIFO parity)
This bit represents the parity bit of the DMA FIFO when the CTEST6 register reads data out of the FIFO. Reading the CTEST6 register unloads one data byte from the bottom of the DMA FIFO. When the CTEST6 register is read the parity signal is latched into this bit location and the next byte falls down to the bottom of the FIFO.

Bit 2 TEOP (SCSI true end of process)
This bit indicates the status of the SYM53C770's internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the SYM53C770. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

Bit 1 DREQ (Data request status)
This bit indicates the status of the SYM53C770's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

Bit 0 DACK (Data acknowledge status)
This active low bit indicates the status of the SYM53C770's internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

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Register 1B (18)
Chip Test Three (CTEST3)
Read/Write

V3	V2	V1	V0	FLF	CLF	FM	SM
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	0	0	0

Bits 7-4 V3-0 (Chip revision level)

These bits identify the chip revision level for software purposes.

Bit 3 FLF (Flush DMA FIFO)

When this bit is set, data residing in the DMA FIFO is transferred to or from memory, starting at the address in the DNAD register. The internal DMAWR signal, controlled by the CTEST5 register, determines the direction of the transfer. This bit is not self clearing; once the SYM53C770 has successfully transferred the data, this bit should be reset.

Bit 2 CLF (Clear DMA FIFO)

When this bit is set, all data pointers for the DMA FIFO are cleared. Any data in the FIFO is lost. This bit automatically resets after the SYM53C770 has successfully cleared the appropriate FIFO pointers.

Bit 1 FM (Fetch pin mode)

When set, this active low bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ will only be active during the op code portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM.

If this bit is not set, FETCH/ will be asserted for all bus cycles during instruction fetches.

Bit 0 SM (Snoop pins mode)

When set, the snoop pins change functions and become pure outputs that are always driven, except when in ZMODE. The values driven are listed in the following table. When clear, the snoop pins are driven during host bus ownership with the values of the CTEST0 SC(1-0) bits.

Pin	Function
SC0	Becomes a copy of the internal bus request signal. Signal will assert prior to TS/_BR/ and will be negated during the TS/_BR/ of the last bus cycle. Note: this signal cannot be used when the STE bit in the DCNTL register is set.

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Registers 1C-1F (1C-1F) Temporary Stack (TEMP) Read/Write

This 32-bit register stores the instruction address pointer for a CALL or a RETURN instruction. The address pointer stored in this register is loaded into the DSP register. This address points to the next instruction to be executed. Do not write to TEMP while the SYM53C770 is executing SCSI SCRIPTS.

During any Memory-to-Memory Move operation, the contents of this register are shadowed.

Register 20 (23) DMA FIFO (DFIFO) Read/Write

RES	BO6	BO5	BO4	BO3	BO2	BO1	BO0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bit 7 Reserved

Bits 6-0 BO6-0 (Byte offset counter)

These seven bits indicate the amount of data transferred between the SCSI core and the DMA core. It may be used to determine the number of bytes in the DMA FIFO when a DMA error occurs. These bits are unstable while data is being transferred between the two cores; once the chip has stopped transferring data, these bits are stable.

The following steps will determine how many bytes are left in the DMA FIFO:

1. Subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register.
2. AND the result with 7Fh for a byte count between zero and 96.

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Register 21 (22)
Chip Test Four (CTEST4)
Read/Write

MUX	ZMOD	ZSD	SRTM	EHPC	FBL2	FBL1	FBL0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 MUX (Host bus multiplex mode)

When set, the MUX bit puts the SYM53C770 into host bus multiplex mode. In this mode, the chip asserts a valid address for one BCLK (during which AS/TS is valid and the data bus is tristated), and then tristates the address bus and drives the data bus (if a write). This allows the address and data buses to be tied together. It should be written before acquiring bus mastership. Multiplex mode is only available in Bus Mode 2.

Bit 6 ZMOD (High impedance mode)

Setting this bit causes the SYM53C770 to place all output and bidirectional pins into a high-impedance state. In order to read data out of the SYM53C770, this bit must be cleared.

This bit is intended for board-level testing only. Setting this bit during system operation will likely result in a system failure.

Bit 5 ZSD (SCSI DMA High Impedance Mode)

Setting this bit causes the SYM53C770 to place the SCSI data bus (SD (15-0)) and the parity lines (SDP (1-0)) in a high-impedance state. In order to transfer data on the SCSI bus, this bit must be cleared. This bit differs from the SCSI High Impedance Mode bit in the STEST2 register, in that it only affects the SCSI data lines.

Bit 4 SRTM (Shadow Register Test Mode)

Asserting this bit allows the user to read the shadowed temporary stack (TEMP) and Data Structure Address (DSA) registers. These registers are shadowed because both are written over during a Memory to Memory move operation. The DSA and TEMP registers contain the base address used for table indirect calculations, and the instruction address pointer for a call or return instruction, respectively.

Bit 3 EHPC (Enable Host Parity Check)

Setting this bit enables parity checking during slave write and DMA read execution if the Enable Parity Generation bit is cleared (SCNTL0 bit 2). The system powers up with this bit disabled so that the SYM53C770 will function properly with systems that do not support parity.

Bits 2-0 FBL2-0 (FIFO byte control)

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	X	X	Disabled	n/a
1	0	0	0	D(7-0)
1	0	1	1	D(15-8)
1	1	0	2	D(23-16)
1	1	1	3	D(31-24)

These bits define which byte lane of the DMA FIFO is read or written when the CTEST6 register is read or written. If the FBL2 bit is set, then FBL1 and FBL0 determine which of four byte lanes can be read or written. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero (set it to this value before executing SCSI SCRIPTS).

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Register 22 (21)
Chip Test Five (CTEST5)
Read/Write

ADCK	BBCK	RES	MASR	DDIR	RAM0	RAM1	RAMEN
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	0	0	0	0	0

Bit 7 ADCK (Clock address incrementor)
Setting this bit increments the address pointer contained in the DNAD register. The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

Bit 6 BBCK (Clock byte counter)
Setting this bit decrements the byte count contained in the DBC register. The DBC register supports 24 bits. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DBC register.

Bit 5 Reserved

Bit 4 MASR (Master control for set or reset pulses)
This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is reset, bit 3 deasserts the corresponding signals. This bit and bit 3 should not be changed in the same write cycle.

Bit 3 DDIR (DMA direction)
Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

Bit 2-1 RAM1-0 (SCRIPTS RAM bits 1-0)
These bits are used to enable the 4K internal SCRIPTS RAM. Their values combine to allow three different implementation of the SCRIPTS RAM. For more information on the internal SCRIPTS RAM, see Chapter 2, ".

Table 4-1: SCRIPTS RAM Access

Bit 2	Bit 1	Method
0	0	SCRIPTS RAM disabled
0	1	SCRIPTS RAM accessed through indexed addressing in chip register space
1	0	SCRIPTS RAM accessed through increased chip select address space
1	1	SCRIPTS RAM access through additional chip select pin

Bit 0 RAMEN (RAM Base Address Enable)
When this bit is set, the SCRATCHA register is shadowed to hold the base address of the internal SCRIPTS RAM. This allows the internal chip logic to recognize the location of the SCRIPTS RAM in the system memory map. The actual contents of the SCRATCHA register are preserved. This bit also causes SCRATCHB to become the indexed address pointer when the indexed mode has been enabled. The actual contents of SCRATCHB are preserved.

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Register 23 (20)
Chip Test Six (CTEST6)
Read/Write

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. When data is read from the DMA FIFO, the parity bit for that byte is latched and stored in the DMA FIFO parity bit in the CTEST2 register.

To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting SCRIPTS.

Registers 24-26 (25-27)
DMA Byte Counter (DBC)
Read/Write

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the SYM53C770. The DBC counter is decremented each time that the AS/ (TS/ in Bus Mode 2, ADS/ in Bus Modes 3 and 4) signal is pulsed by the SYM53C770. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DBC register is FFFFFFh. If the instruction is Block Move and a value of 000000h is loaded into the DBC register, an illegal instruction interrupt will occur if the SYM53C770 is not in target mode Command phase.

The DBC register is also used during table indirect I/O SCRIPTS to hold the offset value.

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Register 27 (24)
DMA Command (DCMD)
Read/Write

This 8-bit register determines the instruction for the SYM53C770 to execute. This register has a different format for each instruction. For a complete description, refer to the SYM53C770 instruction set in Chapter 5.

Registers 28-2B (28-2B)
DMA Next Data Address (DNAD)
Read/Write

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DSPS register. Its value may not be valid except in certain abort conditions.

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Registers 2C-2F (2C-2F)
DMA SCRIPTS Pointer (DSP)
Read/Write

To execute SCSI SCRIPTS, the address of the first SCSI SCRIPTS routine must be written to this register. In normal SCRIPTS operation, once the starting address of the SCSI SCRIPTS is written to this register, the SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a SCRIPTS step interrupt after each instruction is executed. The DSP register does not need to be written with the next address, but the Start DMA bit (bit 2, DCNTL register) must be set each time the step interrupt occurs to fetch and execute the next SCSI SCRIPTS instruction. When writing this register eight bits at a time, writing the upper eight bits begins execution of the SCSI SCRIPTS routine.

Registers 30-33(30-33)
DMA SCRIPTS Pointer Save (DSPS)
Read/Write

This register contains the second longword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS Interrupt instruction is fetched, this register holds the interrupt vector.

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Registers 34-37 (34-37)
Scratch Register A (SCRATCHA)
Read/Write

This is a general purpose user definable scratch pad register. Normal SCRIPTS operations will not destroy the contents of this register; only Register Read/Write and Memory Moves into the SCRATCHA register will alter its contents.

Note: the SYN53C770 cannot fetch SCRIPTS instructions from this location.

SCRIPTS programs may read or write individual bytes in this register by using the names SCRATCHA0 and SCRATCHA1.

When the internal SCRIPTS RAM is enabled using any of the three methods described in Chapter 2, and when bit 0 is set in the CTEST5 register, this register is shadowed to provide a base address for the SCRIPTS RAM. The shadowed version of this register allows the internal logic of the SYM53C770 to recognize the location of the SCRIPTS RAM in the system memory map. The contents of the SCRATCHA register are preserved when shadowed.

Register 38 (3B)
DMA Mode (DMODE)
Read/Write

BL1	BL0	FC2	FC1	PD	FAM	UO	MAN
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7-6 BL1-0 (Burst length)

BL1	BL0	Burst Length
0	0	2 - transfer burst
0	1	4- transfer burst
1	0	8- transfer burst
1	1	16 - transfer burst

These bits control the maximum number of bus cycles performed per bus ownership. The SYM53C770 asserts the Bus Request output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request (Hold in Bus Modes 3 and 4) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed.

To perform cache line bursts, these bits must be set to 4, 8 or 16 transfers and cache bursting must be enabled (by clearing the CDIS bit, bit 7 in the CTEST0 register).

The SYM53C770 inserts a “fairness delay” of exactly 5 CLKs between bus ownerships. This gives the CPU and other bus master devices the opportunity to access memory between bursts.

Note: the fairness timer has been modified in the SYM53C770 to improve DMA transfer rates while still allowing other DMA masters to gain access to the bus. In the SYM53C720, the fairness delay was 5-8 CLKs. In the SYM 53C770, the fairness delay is fixed at 5 CLKs.

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Bit 5-4 FC2-1 (Function code) (Bus Modes 1, 3 and 4), or TM2-1 (Transfer Modifier) (Bus Mode 2)

These bits, along with bit 6 in the DCNTL register (Bus Mode), define the function of the FC2-1_TM2-1 signals as illustrated in Table 4-3.

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Table 4-2: FC2-1_TM2-1 Pin Function

DCNTL bit 6	DMODE bits 5-4	FC2-1_TM2-1 Pin Function
0	00	User defined. The value of bits 5-4 correspond directly to the signal pins (FC2-1_TM2-1). The values of these bits are asserted onto the device pins during bus mastership.
0	01	
0	10	
0	11	
1	00	FC2_TM2 becomes a Preview of Address input signal used to tell the SYM53C770 that the system is ready for the next address value. FC1-TM1 is an output that is always asserted.
1	01	
1	10	
1	11	

Bit 3 PD (Program/data)

This bit affects the function of the FC0_TM0 pin. It works in conjunction with the Bus Mode bit (bit 6 of the DCNTL register), as shown in Table 4-3. When the Bus Mode bit is not set, the SYM53C770 can store SCRIPTS routines and data in separate memory banks. When the Bus Mode bit is set, the SYM53C770 performs the same function as the DC/ signal that is commonly found in Intel processors.

Table 4-3: FC0_TM0 Pin Function

DCNTL bit 6	DMODE bit 3	FC0_TM0 Pin Function
0	0	Driven high when data is moved to or from memory
0	1	Driven low when fetching instructions from memory. This is only done during instruction fetch cycles.
1	0	Driven high when the SYM53C770 is bus master, indicating that data space is being accessed. When the SYM53C770 is not bus master, FC0_TM0 is tristated.
1	1	Driven low, indicating that control space is being accessed.

Bit 2 FAM (Fixed address mode)

When the Fixed Address Mode bit is set, the address pointer in the DNAD register is disabled and will not increment after each data transfer. If this bit is clear, the pointer increments after each data transfer. The fixed address mode feature is used to transfer data to or from a fixed port address. This port width must be 32 bits and longword-aligned. Setting this bit does not affect SCRIPTS fetching instructions; only data transfer instructions are affected.

In fixed address mode, if a SCSI interrupt occurs while the SYM53C770 is receiving data, the data must be flushed manually. Once the interrupt occurs (within the chip), the DMA FIFO Empty bit (bit 7 in the DSTAT register) may not have been set when reading the DMA Status register (DSTAT). At this point, the user may clear the DMA FIFO by writing to the Clear DMA FIFO bit (bit 2) in the CTEST3 register and setting the CSF (Clear SCSI FIFO) bit, bit 1 in the STEST3 register. The Block Move instruction may now be restarted. Instead of clearing the FIFO, it

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may be flushed. This is done as follows: 1) reset the FAM bit; 2) load the DMA Next Address register (DNAD) with a valid memory address; 3) write to the Flush DMA FIFO bit (bit 3) in the CTEST3 register; 4) set the FAM bit again. The Block Move instruction may now be restarted, assuming the byte count and address have been updated.

Bit 1 UO/TT0 (User programmable transfer type)

In all bus modes, UPSO-TT0/ is a general purpose output pin. The value in the register bit is asserted onto the UPSO-TT0/ pin while the SYM53C720 is a bus master. The TT1 bit is in CTEST0.

Bit 0 MAN (Manual start mode)

Setting this bit disables the SYM53C770 from automatically fetching and executing SCSI SCRIPTS after the DSP register is written. When the Start DMA bit in the DCNTL register is cleared, the chip is running in normal mode. Once the Start DMA bit in the DCNTL register is set, the SYM53C770 automatically fetches and executes each instruction. Clearing this bit causes the SYM53C770 to automatically fetch and execute SCSI SCRIPTS after the DSP register is written.

Register 39 (3A)
DMA Interrupt Enable (DIEN)
Read/Write

RES	HPED	BF	ABRT	SSI	SIR	WTD	IID
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bit 7 Reserved

Bit 6 HPED (Host parity error detected during DMA read or Slave write)

Bit 5 BF (Bus fault)

Bit 4 ABRT (Aborted)

Bit 3 SSI (SCRIPTS step interrupt)

Bit 2 SIR (SCRIPTS interrupt instruction received)

Bit 1 WTD (Watchdog time-out detected)

Bit 0 IID (Illegal instruction detected)

This register contains the interrupt enable bits corresponding to the interrupting conditions described in the DSTAT register. To mask an interrupt, clear the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the DSTAT register. Masking an interrupt will not prevent the DIP bit (bit 0 in the ISTAT register) from being set. All DMA interrupts are considered fatal, therefore SCRIPTS will stop running when a DMA interrupt occurs, whether or not the interrupt is masked. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt.

The SYM53C770 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. For more information on enabling interrupts, please refer to Chapter 2.

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Register 3A (39)
DMA Watchdog Timer (DWT)
Read/Write

7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

The DMA watchdog timer register provides a time-out mechanism during data transfers between the SYM53C770 and memory. This register determines the amount of time that the SYM53C770 will wait for the assertion of the STERM/-TA/-READYIN/ signal after starting a bus cycle. Write the time-out value to this register during initialization. Every time that the SYM53C770 transfers data to/from memory, the value stored in this register is loaded into the counter. Disable the time-out feature by writing 00h to this register.

The unit time base for this register is 32* BCLK input period. For example, at 50 MHz the time base for this register is 32 * 20 ns = 640 ns. If a time-out of 50 µs is desired, then this register should be loaded with a value of 4Eh.

The minimum time-out value that should be loaded into this register is 02h; the value 01h will not provide a reliable time-out period.

Register 3B (38)
DMA Control (DCNTL)
Read/Write

STE 7	BSM 6	EA 5	SSM 4	BW16 3	STD 2	FA 1	COM 0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 STE (Size Throttle Enable)

Asserting this bit causes the SYM53C770 to relinquish bus ownership every time the transfer size changes. When the size bits change from 01 (byte), 10 (word), or 00/11 (long-word), the SYM53C770 will relinquish the bus and attempt to complete the transfer in succeeding cycles. The chip powers up with this bit disabled. The bit will be reset during a software or hardware reset. When cache line bursting is enabled, the SYM53C770 performs one transfer at a time until it reaches a cache line boundary. If this bit is set the snoop mode function of the SC0 pin, internal bus request, is not available.

Bit 6 BSM (Bus Mode)

Setting this bit changes the function of the Function Code (FC2-0) or Transfer Modifier (TM2-0) pins. FC0_TM0 becomes a data control signal, FC1_TM1 becomes an output that is always asserted, and FC2_TM2 becomes an input to allow Preview of Address (PA/). For more information on the operation of this bit, refer to the descriptions of bits 5-3 in the DMODE register.

Bit 5 EA (Enable ACK)

Setting this bit will cause the STERM/ (TA/ in Bus Mode 2, ReadyIn/ in Bus Modes 3 and 4) pin to become bidirectional, so the SYM53C770 will generate STERM/ during slave accesses. When this bit is clear, the SYM53C770 will monitor STERM/ to determine the end of a cycle. This bit takes effect during the cycle in which it is set; setting this bit must be the first I/O performed to the SYM53C770 if this feature is desired. This bit

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is not cleared with a software reset. Refer to the Bidirectional STERM/-TA/ section in Chapter 2, for more information on how this bit operates.

Bit 4 SSM (Single-step mode)

Setting this bit causes the SYM53C770 to stop after executing each SCRIPTS instruction, and generate a SCRIPTS step interrupt. When this bit is clear the SYM53C770 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, this bit should be clear. To restart the SYM53C770 after it generates a SCRIPTS Step interrupt, the ISTAT and DSTAT registers should be read to clear the interrupt and then the START DMA bit in this register should be set.

Bit 3 BW16 (Host Bus Width Equal to 16)

When this bit is set, the SYM53C770 host interface will become 16 bits wide. This bit can only be set in Little Endian mode.

Note: data lines 31-16 must be tied to data lines 15-0, respectively.

Note: cache bursting is not available in this mode.

Bit 2 STD (Start DMA operation)

The SYM53C770 fetches a SCSI SCRIPTS instruction from the address contained in the DSP register when this bit is set. This bit is required if the SYM53C770 is in one of the following modes:

1. Manual start mode – Bit 0 in the DMODE register is set
2. Single-step mode – Bit 4 in the DCNTL register is set

When the SYM53C770 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the SYM53C770 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after a single-step interrupt.

Bit 1 FA (Fast arbitration)

When this bit is set, the SYM53C770 will immediately become bus master after receiving a Bus Grant (HLDAI in Bus Modes 3 and 4), saving one clock cycle of arbitration time. When this bit is clear, the SYM53C770 will follow the normal arbitration sequence.

Bit 0 COM (53C700 compatibility)

When this bit is clear, the SYM53C770 will behave in a manner compatible with the 53C700. Selection/reselection IDs will be stored in both the SSID and SFBR registers.

When this bit is set, the ID will be stored only in the SSID register, protecting the SFBR from being overwritten should a selection/reselection occur during a DMA register to register operation. The default condition of this bit (clear) causes the SYM53C770 to function the same as the 53C700.

Note: This bit is not cleared with a software reset.

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Register 3C-3F (3C-3F)
Adder Sum Output (ADDER)
Read Only

This register contains the output of the internal adder, and is used primarily for test purposes.

Register 40 (43)
SCSI Interrupt Enable Zero (SIEN0)
Read/Write

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This register contains the interrupt enable bits corresponding to the interrupting conditions described in the SIST0 register. To mask an interrupt, clear the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST0 register. Masking an interrupt will not prevent the ISTAT SIP bit from being set, except in the case of non-fatal interrupts (SEL, RSL, CMP, and M/A (target mode only). Setting a mask bit unmasks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked non-fatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking does not begin until either the SIP (bit 1) or DIP (bit 0) bit in the ISTAT register is set.

The SYM53C770 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the SIP bit in the ISTAT register to clear and allow pending interrupts to fall through (interrupt stacking will be disabled). The bits in this register should not be toggled on or off during normal operation. They should be set or cleared during the initialization routine.

For more information on interrupts, refer to Chapter 2, “Functional Description.”

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Bit 7 M/A (SCSI Phase Mismatch - Initiator Mode; SCSI ATN Condition - Target Mode)

In initiator mode, this bit is set when the SCSI phase asserted by the target and sampled during REQ does not match the expected phase in the SOCL register. This expected phase is automatically written by SCSI transfer SCRIPTS.

In target mode, this bit is set when the initiator has asserted ATN. See the Disable halt on parity error or ATN condition bit in the SCNTL1 register for more information on when this status is actually raised.

Bit 6 CMP (Function Complete)

This bit is set when full arbitration and selection sequence has completed.

Bit 5 SEL (Selected)

The SYM53C770 has been selected as a SCSI target device. The Enable response to selection bit in the SCID register must be set for this to occur.

Bit 4 RSL (Reselected)

The SYM53C770 has been reselected as a SCSI initiator device. The Enable response to reselection bit in the SCID register must be set for this to occur.

Bit 3 SGE (SCSI Gross Error)

The following conditions are considered SCSI Gross Errors:

1. Data underflow: the SCSI FIFO was read when no data was present.
2. Data overflow: the SCSI FIFO was written to while full.
3. Offset underflow: in target mode, an ACK pulse was received before the corresponding REQ was sent.
4. Offset overflow: in initiator mode, a REQ pulse was received which caused the maximum offset (Defined by the MO3-0 bits in the SXFER register) to be exceeded.
5. In initiator mode, a phase change occurred with an outstanding REQ/ACK offset.
6. Residual data in SCSI FIFO: a transfer other than synchronous data receive was started with data left in the SCSI synchronous receive FIFO.

Bit 2 UDC (Unexpected Disconnect)

This condition only occurs in initiator mode. It happens when the target to which the SYM53C770 is connected disconnects from the SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCNTL2 register for more information on expected versus unexpected disconnects. Any disconnect in low level mode causes this condition.

Bit 1 RST (SCSI Reset Condition)

The SCSI RST signal has been asserted by the SYM53C770 or any other SCSI device. Note that this condition is edge-triggered so that multiple interrupts cannot occur because of a single RST pulse.

Bit 0 PAR (SCSI Parity Error)

The SYM53C770 detected a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or ATN Condition bits in the SCNTL1 register for more information on when this condition will actually be raised.

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Register 41 (42)
SCSI Interrupt Enable One (SIEN1)
Read/Write

RES	RES	RES	RES	RES	STO	GEN	HTH
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	0	0	0

This register contains the interrupt enable bits corresponding to the interrupting conditions described in the SIST1 register. To mask an interrupt, clear the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the SIST1 register. Masking an interrupt will not prevent the SIP bit (bit 1) in the ISTAT register from being set. Setting a mask bit un-masks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked non-fatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking does not begin until either the DIP (bit 0) or SIP (bit 1) bit in the ISTAT register is set.

The SYM53C770 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the SIP bit (bit 1) in the ISTAT register to clear and allow pending interrupts to fall through (interrupt stacking will be disabled). The bits in this register should not be toggled on or off during normal operation. They should be set or cleared during the initialization routine.

Bits 7-3 Reserved

Bit 2 STO (Selection or Reselection Time-out)

This bit is set when the SCSI device which the SYM53C770 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the STIME0 register bits 3-0 for more information on the time-out timer.

Bit 1 GEN (General Purpose Timer Expired)

This bit is set when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

Bit 0 HTH (Handshake to Handshake Timer Expired)

This bit is set when the handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

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Register 42 (41)
SCSI Interrupt Status Zero (SIST0)
Read Only

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Reading the SIST0 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN0 register or not. Each bit asserted indicates that the corresponding condition has occurred. Reading the SIST0 will reset the selected conditions. The SIP bit in the ISTAT register will be cleared after both SIST0 and SIST1 are read.

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the SYM53C770 stacks interrupts). SCSI interrupt conditions may be individually masked through the SIEN0 register.

When performing consecutive 8-bit reads of the DSTAT, SIST0, and SIST1 registers (in any order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. To avoid missing a SCSI interrupt while reading any of these registers when the ISTAT SIP and DIP bits may not be set, read SIST0 and SIST1 before DSTAT. For more information on interrupts, refer to Chapter Two, Functional Description.

Bit 7 M/A (Initiator Mode: Phase Mismatch; Target Mode: ATN/ Active)

In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when REQ/ is asserted by the target. In target mode, this bit is set when the ATN/ signal is asserted by the initiator. This status bit is used in diagnostics testing or in low level mode. It is set in low level mode any time there is a phase change.

Bit 6 CMP (Function Complete)

This bit is set when full arbitration and selection sequence has completed.

Bit 5 SEL (Selected)

This bit is set when the SYM53C770 is selected by another SCSI device. The enable response to selection bit must have been set in the SCID register for the SYM53C770 to respond to selection attempts.

Bit 4 RSL (Reselected)

This bit is set when the SYM53C770 is reselected by another SCSI device. The Enable Response to Reselection bit must have been set in the SCID register for the SYM53C770 to respond to reselection attempts.

Bit 3 SGE (SCSI Gross Error)

This bit is set when the SYM53C770 encounters a SCSI Gross Error Condition. The following conditions can result in a SCSI Gross Error Condition:

1. Data Underflow - the SCSI FIFO register was read when no data was present.
2. Data Overflow - too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.
3. Offset Underflow - the SYM53C770 is operating in target mode and an ACK/ pulse is received when the outstanding offset is zero.
4. Offset Overflow - the other SCSI device sent a REQ/ or ACK/ pulse with data which exceeded the maximum synchronous offset defined by the SXFER register.
5. Residual data in the Synchronous data FIFO - a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.
6. A phase change occurred with an outstanding synchronous offset when the SYM53C770 was operating as an initiator.

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Bit 2 UDC (Unexpected Disconnect)

This bit is set when the SYM53C770 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the SYM53C770 is an initiator. When the SYM53C770 operates in low level mode, any disconnect will cause an interrupt, even a valid SCSI disconnect.

This bit will also be set if a selection time-out occurs (it may occur before, at the same time, or stacked after the STO interrupt, since this is not considered an expected interrupt).

Bit 1 RST (SCSI RST/ Received)

This bit is set when the SYM53C770 detects an active RST/ signal, whether the reset was generated external to the chip or caused by the Assert RST/ bit in the SCNTL1 register. This SYM53C770 SCSI reset detection logic is edge-sensitive so that multiple interrupts will not be generated for a single assertion of the SCSI RST/ signal.

Bit 0 PAR (Parity Error)

This bit is set when the SYM53C770 detects a parity error when receiving or sending SCSI data. The Enable Parity Checking bit (bit 3 in the SCNTL0 register) must be set for this bit to become active. A parity error can occur when receiving data from the SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SODL register. A parity error can occur from the host bus only if Pass Through parity is enabled (bit 3 in the SCNTL0 register = 1, bit 2 in the SCNTL0 register = 0).

Register 43 (40)
SCSI Interrupt Status One (SIST1)
Read Only

RES 7	RES 6	RES 5	RES 4	RES 3	STO 2	GEN 1	HTH 0
Default>>>							
X	X	X	X	X	0	0	0

Reading the SIST1 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN1 register or not. Each bit that is set indicates that the corresponding condition has occurred.

Reading this register will reset the selected conditions, and will reset the SIST1 register. The SIP bit in the ISTAT register will be cleared after both SIST0 and SIST1 are read.

Bits 7-3 Reserved

Bit 2 STO (Selection or Reselection Time-out)

This bit is set when the SCSI device which the SYM53C770 was attempting to select or reselect did not respond within the programmed time-out period (See the description of the STIME0 register, bits 3-0, for more information on the time-out timer). After the SYM53C770 has won arbitration, it waits for selection or reselection to complete. While waiting, it fetches the next instruction from the address pointed to by the DSP register. The SCRIPTS routine can then execute the next instruction before the selection has completed. The chip will continue executing SCRIPTS until it encounters an interrupt, or a SCRIPTS instruction that requires it to respond. If time out occurs and a block move instruction was loaded, FIFO needs to be flushed.

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Bit 1 GEN (General Purpose Timer Expired)

This bit is set when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

Bit 0 HTH (Handshake to Handshake timer Expired)

This bit is set when the handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

Register 44 (47) SCSI Longitudinal Parity (SLPAR) Read/Write

The SLPAR register consists of two multiplexed bytes; other register bit settings determine what is displayed at this memory location at any given time. When bit 5 in the SCNTL2 (SLPMD) register is cleared, the chip XORs the high and low bytes of the SLPAR register together to give a single-byte value which is displayed in the SLPAR register. If the SLPMD bit is set, then the SLPAR register shows either the high byte or the low byte of the SLPAR word. The SLPAR High Byte Enable bit, SCNTL2 bit 4, determines which byte of the SLPAR register is visible on the SLPAR register at any given time. If this bit is cleared, the SLPAR register contains the low byte of the SLPAR word; if it is set, the SLPAR register contains the high byte of the SLPAR word.

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This register performs a bytewise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SLPAR should go to zero (assuming it started at zero). For example, the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active high):

Data/Check Bytes	Running SLPAR	Comments
—	00000000	SLPAR initialized to zero
1. 11001100 (Data)	11001100)	XOR data byte with SLPAR, place result in SLPAR
2. 01010101 (Data)	10011001	XOR data byte with SLPAR, place result in SLPAR
3. 00001111 (Data)	10010110	XOR data byte with SLPAR, place result in SLPAR
4. 10010110 (Check)	00000000	XOR check byte with SLPAR, place result in SLPAR. The result should be zeros; a one in any bit position indicates a transmission error.

The SLPAR register can also be used to generate the check bytes for SCSI send operations. If the SLPAR register contains all zeros prior to sending a block move, it will contain the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus.

Writing any value to this register resets it to zero.The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances.

Register 45 (46)
SCSI Wide Residue Data (SWIDE)
Read Only

After a wide SCSI data receive operation, this register will contain a residual data byte if the last byte received was never sent across the DMA bus. It represents either the first data byte of a subsequent data transfer, or it is a residue byte which should be cleared when an Ignore Wide Residue message is received. It may also be an overrun data byte.

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Register 46 (45)
Memory Access Control (MACNTL)
Read/Write

TYP3	TYPE2	TYP1	TYP0	DataWR	DataRD	PSCRIPT	SCRIPT
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	0	0	0

MACNTL is used to determine if an external access is to local or far memory.

Bits 7-4 TYP3-0 (Chip Type)

These bits identify the chip type for software purposes.

Bits 7654	Chip Type
0000	720
0001	720SE
0010	770

Bits 3-0

These bits are used to define if a data write, data read, pointer to a SCRIPTS fetch and a SCRIPTS fetch, respectively, are considered local memory accesses. If any of the bits are set, the access will be considered local. The bits power up cleared, indicating far memory. Internal logic will determine if the specific transfer is considered local or far. The MAC/ signal, pin 26 (also referred to as the near/far pin), will be asserted high when the transfer is to local memory. Assuming the SCRIPTS fetch bit is set, the near/far pin will not be affected until completion of the next Transfer Control instruction. Changes to the MAC/ signal will be available at the pin at the same time the Bus Request pin is asserted.

Register 47 (44)
General Purpose Control (GPCNTL)
Read/Write

RES	RES	RES	GPIO_en4	GPIO_en3	GPIO_en2	GPIO_en1	GPIO_en0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	0	1	1	1	1

GPCNTL is used to determine if the pins controlled by the General Purpose register (GPREG, address 07 (04)h) are inputs or outputs.

Bits 7-5 Reserved

Bit 4 GPIO_en4 (General Purpose Output Enable 4)

GPCNTL, corresponding to bit 4 in the GPREG register and pin 43, powers up as a general purpose output.

Bits 3-0 GPIO_en3-0 (General Purpose Output Enable 3-0)

Bits 3-0 in GPCNTL, corresponding to bits 3-0 in the GPREG register and pins 39-42, power up as general purpose inputs. If any of the bits are cleared, this indicates an output and if any of the bits are set this indicates an input. When the bits are enabled as inputs, an internal pullup is also enabled.

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Register 48 (4B)
SCSI Timer Register 0 (STIME0)
Read /Write

HTH3	HTH2	HTH1	HTH0	SEL3	SEL2	SEL1	SEL0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-4 HTH (Handshake-to-Handshake Timer Period)

These bits select Handshake-to-Handshake Time-out Period, the maximum time between SCSI handshakes (REQ to REQ in target mode, or ACK to ACK in initiator mode). When this timing is exceeded, the HTH bit in the SIST1 register is set, and an interrupt is optionally generated, if bit 0 in the SIEN1 register is set. The following table applies to the Handshake-to-Handshake Timer and the General Purpose Timer (STIME1 bits 3-0).

HTH 7-4, GEN 3-0	Minimum Time-out w/o scale factor bit set (50 MHz CLK)	Minimum Time-out with scale factor bit set (50 MHz CLK)
0000	Disabled	Disabled
0001	100 µs	1.6 ms
0010	200 µs	3.2 ms
0011	400 µs	6.4 ms
0100	800 µs	12.8 ms
0101	1.6 ms	25.6 ms
0110	3.2 ms	51.2 ms
0111	6.4 ms	102.4 ms
1000	12.8 ms	204.8 ms
1001	25.6 ms	409.6 ms
1010	51.2 ms	819.2 ms
1011	102.4 ms	1.6 sec
1100	204.8 ms	3.2 sec
1101	409.6 ms	6.4 sec
1110	819.2 ms	12.8 sec
1111	1.6sec	25.6 sec

Bits 3-0 SEL (Selection Time-out Period)

These bits select the SCSI selection/reselection time-out period. When this timing (plus the 200 µs selection abort time) is exceeded, the STO bit in the SIST1 register is set. An interrupt is optionally generated, if bit 2 in the SIEN1 register is set.

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Register 49 (4A)
SCSI Timer Register One (STIME1)
Read/Write

RES	HTHBA	GENSF	HTHSF	GEN3	GEN2	GEN1	GEN0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bits 7 Reserved

Bit 6 Handshake-to-Handshake Timer Bus Activity Enable Bit (HTHBA)

Setting this bit causes this timer to begin testing for SCSI request/acknowledge activity as soon as SCSI busy is asserted regardless of the agents participating in the transfer.

Bit 5 General Purpose Timer Scale Factor Bit (GENSF)

Setting this bit causes this timer to shift by a factor of 16.

Bit 4 Handshake-to-Handshake Timer Scale Factor Bit (HTHSF) Bit (HTHSF)

Setting this bit causes this timer to shift by a factor of 16.

Bits 3-0 GEN3-0 (General Purpose Timer Period)

These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the SIST1 register is set and an interrupt is optionally generated, if bit 1 in the SIEN1 register is set. Refer to the table under STIME0, bits 3-0, for the available time-out periods.

Register 4A (49)
Response ID Zero (RESPID0)
Read/Write

Register 4B (48)
Response ID One (RESPID1)
Read/Write

RESPID0 and RESPID1 contain the selection or reselection IDs. In other words, these two 8-bit registers contain the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit of RESPID1 representing ID 15 and the least significant bit of RESPID0 representing ID 0. The SCID register still contains the chip ID used during arbitration. The chip can respond to more than one ID because more than one bit can be set in the RESPID1 and RESPID0 registers. However, the chip can arbitrate with only one ID value in the SCID register.

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Register 4C (4F)
SCSI Test Register Zero (STEST0)
Read Only

SSAID 7	SSAID 6	SSAID 5	SSAID 4	SLT 3	ART 2	SOZ 1	SOM 0
Default>>>							
X	X	X	X	0	X	1	1

Bits 7-4 SSAID (SCSI Selected ASID)

These bits are read only and contain 4 bits that encode the possible 0-15 ID's the SYM53C770 can be selected as. During the selection phase, when a valid ID is put on the bus, and the SYM53C770 responds to that ID as the ID it was selected as, this ID is written into the SSAID register.

Bit 3 SLT (Selection Response Logic Test)

This bit is asserted when the SYM53C770 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.

Bit 2 ART (Arbitration Priority Encoder Test)

This bit will always be asserted when the SYM53C770 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing, but it may be used during low level mode operation to determine if the SYM53C770 has won arbitration.

Bit 1 SOZ (SCSI Synchronous Offset Zero)

This bit indicates that the current synchronous SCSI REQ/ACK offset is zero. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set, the SYM53C770, as an initiator, is waiting for the target to request data transfers. If the SYM53C770 is a target then the initiator has sent the offset number of acknowledges.

Bit 0 SOM (SCSI Synchronous Offset Maximum)

This bit indicates that the current synchronous SCSI REQ/ACK offset is the maximum specified by bits 3-0 in the SCSI Transfer register. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set the SYM53C770, as a target, is waiting for the initiator to acknowledge the data transfers. If the SYM53C770 is an initiator then the target has sent the offset number of requests.

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Register 4D (4E)
SCSI Test Register One (STEST1)
Read Only

RES	RES	RES	RES	DBLEN	DBLSEL	SFP1	SFP0
7	6	5	4	3	2	1	0
Default >>>							
X	X	X	X	0	0	X	X

Bits 7-4 Reserved

Bit 3 SCLK Doubler Enable (DBLEN)

Set this bit to bring the SCSI clock doubler out of the powered-down state. The default value of this bit is clear (SCSI clock doubler powered down). Set bit 2 after setting this bit, to double the SCLK frequency.

Bit 2 SCLK Doubler Select (DBLSEL)

Set this bit after powering up the SCSI clock doubler to double the SCLK frequency. This bit has no effect unless bit 3 is set.

Bits 1-0 SFP1-0 (SCSI FIFO Parity)

These bits represent the parity that is read from the SCSI FIFO byte lanes during test access through the SODL register. To read the SCSI FIFO in test mode, read these bits after reading the SODL register. SFP1 represents parity for the most significant byte and SFP0 represents parity for the least significant byte. See the description of the SCSI FIFO Test Mode bit in the STEST3 register for more information on testing the SCSI FIFO.

Doubling the SCSI CLK Frequency

The SYM53C770 SCSI clock doubler doubles a 40-50 MHz SCSI clock, increasing the frequency to 80-100 MHz. Follow these steps to use the clock doubler:

1. Set the SCLK Doubler Enable bit (STEST1, bit 3)
2. Wait 20 µs
3. Halt the SCSI clock by setting the Halt SCSI Clock bit (STEST3 bit 5)
4. Set the clock conversion factor using the SCF and CCF fields in the SCNTL3 register
5. Set the SCLK Doubler Select bit (STEST1, bit2)
6. Clear the Halt SCSI Clock bit

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Register 4E (4D)
SCSI Test Register Two (STEST2)
Read/Write

SCE	ROF	DIF	SLB	SZM	AWS	EXT	LOW
7	6	5	4	3	2	1	0
Default >>>							
0	0	0	0	0	0	0	0

Bit 7 SCE (SCSI Control Enable)
This bit, when set, allows all SCSI control and data lines to be asserted through the SOCL and SODL registers regardless of whether the SYM53C770 is configured as a target or initiator.

Note: this bit should not be set during normal operation, since it could cause contention on the SCSI bus. It is included for diagnostic purposes only.

Bit 6 ROF (Reset SCSI Offset)
Setting this bit clears any outstanding synchronous SCSI REQ/ACK offset. This bit should be set if a SCSI gross error condition occurs, to clear the offset when a synchronous transfer does not complete successfully. The bit automatically clears itself after resetting the synchronous offset.

Bit 5 DIF (SCSI Differential Mode)
Setting this bit allows the SYM53C770 to interface properly to external differential transceivers. Its only real effect is to tristate the BSY/, SEL/, and RST/ pads so that they can be used as pure inputs. Clearing this bit enables single ended mode operation. This bit should be set in the initialization routine if the differential pair interface is to be used.

Bit 4 SLB (SCSI Loopback Mode)
Setting this bit allows the SYM53C770 to perform SCSI loopback diagnostics. That is, it enables the SCSI core to simultaneously perform as both initiator and target.

Bit 3 SZM (SCSI High-Impedance Mode)
Setting this bit places all the open-drain 48 mA SCSI drivers into a high-impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.

Bit 2 AWS (Always Wide SCSI)
When this bit is set, all SCSI information transfers will be done in 16-bit wide mode. This includes data, message, command, status and reserved phases. This bit should normally be deasserted since 16-bit wide message, instruction, and status phases are not supported by the SCSI specifications. This bit is not guaranteed to function properly with future SCSI specifications.

Bit 1 EXT (Extend REQ/ACK Filtering)
The SCSI core contains a special digital filter on the REQ/ and ACK/ pins which will cause glitches on deasserting edges to be disregarded. Asserting this bit will increase the filtering period from 30ns to 60ns on the deasserting edge of the REQ/ and ACK/ signals.

Note: this bit must never be set during fast SCSI (> 5M transfers per second) operations, because a valid assertion could be treated as a glitch.

Bit 0 LOW (SCSI Low level Mode)
Setting this bit places the SYM53C770 in low level mode. In this mode, no DMA operations can occur, and no SCRIPTS instructions can be executed. Arbitration and selection may be performed by setting the start sequence bit as described in the SCNTL0 register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

Note: it is not necessary to set this bit for access to the SCSI bit-level registers (SODL, SBCL, and input registers). This bit must be clear for the chip to properly respond to selection or reselection.

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Register 4F (4C)
SCSI Test Register Three (STEST3)
Read/Write

TE	STR	HSC	DSI	S16	TTM	CSF	FTM
7	6	5	4	3	2	1	0
Default>>>							
X	X	0	0	0	0	0	0

Bit 7 TE (TolerANT Enable)

Asserting this bit enables TolerANT Active Negation. TolerANT causes the SCSI Request, Acknowledge, Data, and parity signals to be actively deasserted, in addition to relying on external pullups when the SYM53C770 is driving these signals. Active deassertion of these signals will occur only when the SYM53C770 is in an information transfer phase. When operating in a differential environment or at fast SCSI timings, Active Negation should be enabled to improve setup and deassertion times. Active Negation is disabled after chip or software reset, or when this bit is cleared.

Bit 6 STR (SCSI FIFO Test Read)

Setting this bit places the SCSI core into a test mode in which the SCSI FIFO can be easily read. Reading the least significant byte of the SODL register will cause the FIFO to unload. The functions are summarized in the table below.

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Read	15-0	Unload
SODL0	Read	7-0	Unload
SODL1	Read	15-8	None

Bit 5 HSC (Halt SCSI Clock)

Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit may be used for test purposes or to lower I_{DD} during a power down mode.

Bit 4 DSI (Disable Single Initiator Response)

If this bit is set, the SYM53C770 will ignore all bus-initiated selection attempts which employ the single-initiator option from SCSI-1. In order to select the SYM53C770 while this bit is set, the SYM53C770's SCSI ID and the initiator's SCSI ID must both be asserted. This bit should be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response. This bit works in conjunction with the VAL bit in the SSID register.

Bit 3 S16 (16-bit System)

If this bit is set, all devices in the SCSI system implementation are assumed to be 16 bits. This causes the SYM53C770 to always check the parity bit for SCSI IDs 15-8 during bus-initiated selection or reselection, assuming parity checking has been enabled. If an 8-bit SCSI device attempts to select the SYM53C770 while this bit is set, the SYM53C770 will ignore the selection attempt, because the parity bit for IDs 15-8 will be undriven. See the description of the Enable Parity Checking bit in the SCNTL0 register for more information.

Bit 2 TTM (Timer Test Mode)

Asserting this bit facilitates testing of the selection time-out, general purpose, and handshake-to-handshake timers by greatly reducing all three time-out periods. Setting this bit starts all three timers and if the respective bits in the SIEN1 register are asserted, the SYM53C770 will generate interrupts at time-out.

Bit 1 CSF (Clear SCSI FIFO)

Setting this bit will cause the "full flags" for the SCSI FIFO to be cleared. This empties the FIFO. This bit is self-resetting. The SIDL, SODL, and SODR Least and Most Significant Byte Full bits in the SSTAT0 and SSTAT2 registers are also cleared.

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Bit 0 STW (SCSI FIFO Test Write)

Setting this bit places the SCSI core into a test mode in which the FIFO can be easily read and written. While this bit is set, writes to the least significant byte of the SODL register will cause the entire word contained in this register to be loaded into the FIFO. Writing the least significant byte of the SODL register will cause the FIFO to load. These functions are summarized in the table below:

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Write	15-0	Load
SODL0	Write	7-0	Load
SODL1	Write	15-8	None

Registers 50-51 (52-53) SCSI Input Data Latch (SIDL) Read Only

This register is used primarily for diagnostic testing, programmed I/O operation or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SODL register and then read back into the SYM53C770 by reading this register to allow loopback testing. When receiving SCSI data, the data will flow into this register and out to the host FIFO. This register differs from the SBDL register; SIDL contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and will cause a parity error interrupt if the data is not valid.

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Registers 54-55 (56-57) SCSI Output Data Latch (SODL) Read/Write

This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCNTL1 register. This register is used to send data via programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip.

Registers 58-59 (5A-5B) SCSI Bus Data Lines (SBDL) Read Only

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high (enabled when the bits are set). The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data via programmed I/O. This register can also be used for diagnostic testing or in low level mode.

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Registers 5C-5F
Scratch Register B (SCRATCHB)
Read/Write

This is a general purpose, user definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves directed at the SCRATCHB register will alter its contents.

Note: the SYN53C770 cannot fetch SCRIPTS instructions from this location.

If the internal SCRIPTS RAM is enabled using the indexed addressing method, a shadowed version of this register is used to address 128 blocks of 32-byte segments of the SCRIPTS RAM. Each 32-byte block of data is loaded into the SCRATCHC-J registers.

Registers 60h-7fh
Scratch Registers C-J (SCRATCHC-J)
Read/Modify/Write

These are general purpose, user definable scratch pad registers. They are accessible through read/modify/write instructions and are defined as SCRATCHC through SCRATCHJ.

Note: the SYN53C770 cannot fetch SCRIPTS instructions from this location.

When the indexed addressing method is used to enable and access the internal SCRIPTS RAM, the SCRIPTS RAM replaces these registers and can optionally be used as a block of scratchpad RAM. For more information on this and other methods of implementing the SCRIPTS RAM, see Chapter 2.

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Chapter 5

Instruction Set of the I/O Processor

This chapter provides a high-level overview of the SCSI instruction types supported by Symbios Logic SCSI SCRIPTS and the SYM53C770. For detailed descriptions of the individual instructions, refer to the *SYM53C720/se/53C770 Programming Guide*.

SCSI SCRIPTS

After power up and initialization of the SYM53C770, the chip may operate with a low level register interface or in SCSI SCRIPTS mode. With the low level register interface, the user has access to the DMA control logic and the SCSI bus control logic. The chip operates much like an SYM53C80 when in low level mode. An external processor has access to the SCSI bus signals and the low level DMA signals, which allows creation of complicated board level test algorithms. The low level interface provides backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip's pins.

To operate in the SCSI SCRIPTS mode, the SYM53C770 requires only a SCRIPTS start address. All commands are fetched from local or external memory. The SYM53C770 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an interrupt command is encountered, or until an unexpected event (such as a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the SYM53C770 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DMA SCRIPTS Pointer (DSP) register to restart the automatic fetch and execution of instructions.

The SCSI SCRIPTS mode of execution allows the SYM53C770 to make decisions based on the status of the SCSI bus, which off-loads the microprocessor from servicing the numerous interrupts inherent in I/O operations.

Given the rich set of SCSI-oriented features included in the command set, and the ability to reenter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Therefore, switching to low level mode for error recovery should never be required.

Four types of SCSI SCRIPTS instructions are implemented in the SYM53C770:

- Block Move
- I/O or Read/Write
- Transfer Control
- Memory Move

Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DCMD and DBC registers, the second into the DSPS register. The third word, used only by Memory Move instructions, is loaded into the TEMP register.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries. There are two restrictions on

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the placement of data in system memory: the eight bytes of data in the command must be contiguous; and indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

Block Move Instructions

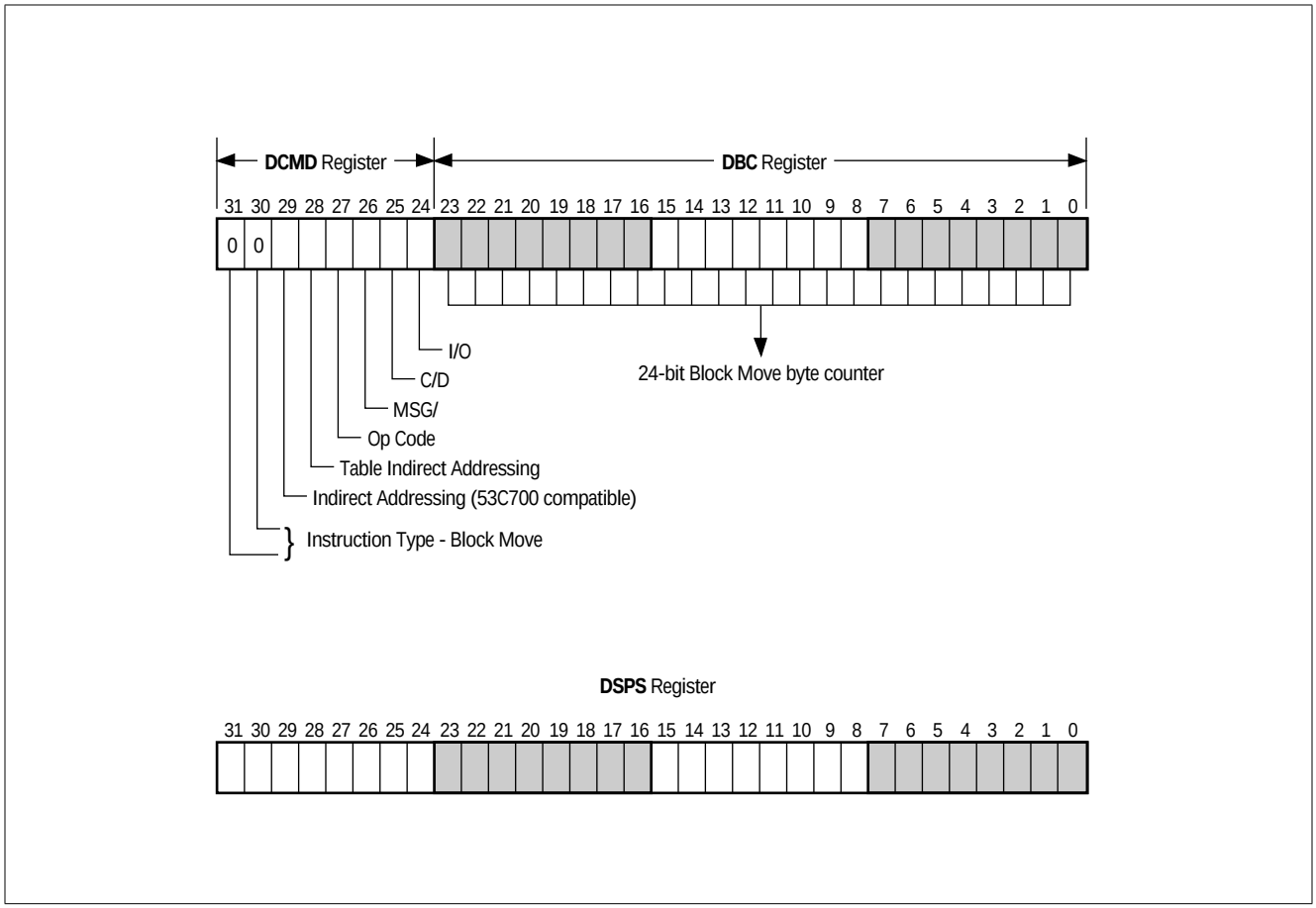


Figure 5-1: Block Move Instruction Register

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First Longword

Bits 31-30 Block Move Instruction

A value of 00 in the two high order bits of the DCMD register indicates the Block Move instruction type.

Bit 29 Indirect Addressing

When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the DNAD register and incremented as data is transferred.

When set, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's DNAD register via a third long word fetch (4-byte transfer across the host computer bus).

Direct
The byte count and absolute address are as follows:

Command	Byte Count
Address of Data	

Indirect
Use the byte count and fetch the data address from the address in the command. The byte count is contained in the DBC register and the data address is fetched from the DSPS register.

Command	Byte Count
Address of Pointer to Data	

Once the data buffer address is loaded, it is executed as if the chip operates in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the Symbios Logic SCSI SCRIPTS compiler, the address is placed in the SCRIPTS program at compile time. Then at the actual data transfer time, the chip fetches a longword from the address specified in the program and writes this value to the DSPS register. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

Bit 28 Table Indirect Addressing

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the DSA register. Both the transfer count and the source/destination address are fetched from this address. For more information on table indirect addressing, refer to the *SYM53C720/se/53C770 Programming Guide*.

Table Indirect
Use the signed integer offset in bits 23-0 of the second longwords of the instruction to fetch first the byte count and then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure. Sign-extended values of all ones for negative values are allowed, but ignored.

Command	Not Used
	Table Offset

Prior to the start of an I/O, the Data Structure Base Address register (DSA) must be loaded with the base address of the I/O data structure. The address may be any longword on a longword boundary.

At the start of an I/O, the DSA is added to the 24-bit signed table offset value from the op code to generate the address of the table entry; both positive and negative offsets are allowed. A subsequent fetch from this address brings the byte counts and buffer addresses into the chip.

Bit 27 Op Code

This one-bit field defines the instruction to be executed, either a block move (MOVE) or a chained block move (CHMOV). The Op Code Field bit has different meaning depending on whether the SYM53C770 is operating in Initiator or Target mode. If the Op Code bit is asserted (target mode) or deasserted (initiator mode) during a chained block move instruction, the corresponding

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bit in the SCNTL2 register (SCNTL bit 6) is asserted. The Op Code bit and the SCNTL2 bit are cleared once a block move instruction is executed.

Target Mode

OPC	Instruction Defined
0	MOVE
1	CHMOV

1. The SYM53C770 verifies that it is connected to the SCSI bus as a target before executing this instruction.
2. The SYM53C770 asserts the SCSI phase signals (MSG/, C_D/, and I_O/) as defined by the Phase Field bits in the instruction.
3. If the instruction is for the Command phase, the SYM53C770 receives the first command byte and decodes its SCSI Group Code.
   a. If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the SYM53C770 overwrites the DBC register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.
   b. If any other Group Code is received, the DBC register is not modified and the SYM53C770 will request the number of bytes specified in the DBC register. If the DBC register contains 000000h an illegal instruction interrupt is generated.
4. The SYM53C770 transfers the number of bytes specified in the DBC register starting at the address specified in the DNAD register. If the Op Code bit is set and a data transfer ends on an odd byte boundary, the SYM53C770 will store the last byte in the SWIDE register during a receive operation or in the SODL register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed. See Figure 5-2.
5. If the SCSI ATN/ signal is asserted by the initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SCNTL1 register controls whether an interrupt will be generated.

Initiator Mode

OPC	Instruction Defined
0	CHMOV
1	MOVE

1. The SYM53C770 verifies that it is connected to the SCSI bus as an initiator before executing this instruction.
2. The SYM53C770 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with REQ/ asserted) for which the SYM53C770 has not yet transferred data by responding with an ACK/.
3. The SYM53C770 compares the SCSI phase bits in the DCMD register with the latched SCSI phase lines stored in the SSTAT1 register. These phase lines are latched when REQ/ is asserted.
4. If the SCSI phase bits match the value stored in the SSTAT1 register, the SYM53C770 will transfer the number of bytes specified in the DBC register starting at the address pointed to by the DNAD register. If the op code bit is cleared and a data transfer ends on an odd byte boundary, the SYM53C770 will be store the last byte in the SCSI Wide Residue Data Register during a receive operation, or in the SCSI Output Data Latch Register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed. See Figure 5-2.

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5. If the SCSI phase bits do not match the value stored in the SSTAT1 register, the SYM53C770 generates a phase mismatch interrupt and the command is not executed.
6. During a Message Out phase, after the SYM53C770 has performed a select with Attention, the SYM53C770 will deassert ATN/ during the final REQ/ACK handshake.
7. When the SYM53C770 is performing a block move for Message In phase, it will not deassert the ACK/ signal for the last REQ/ACK handshake. The ACK signal must be cleared using the Clear ACK I/O instruction.

Bits 26-24 SCSI Phase

This 3-bit field defines the desired SCSI information transfer phase. When the SYM53C770 operates in Initiator mode, these bits are compared with the latched SCSI phase bits in the SSTAT1 register. When the SYM53C770 operates in target mode, the SYM53C770 asserts the phase defined in this field. The following table describes the possible combinations and the corresponding SCSI phase.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Message out
1	1	1	Message in

Bits 23-0 Transfer Counter

A 24-bit field specifying the number of data bytes to be moved between the SYM53C770 and system memory. The field is stored in the DBC register. When the SYM53C770 transfers data to/from memory, the DBC register is decremented by the number of bytes transferred. In addition, the DNAD register is incremented by the number of bytes transferred. This process is repeated until the DBC register has been decremented to zero. At that time, the SYM53C770 fetches the next instruction.

Second Longword

Bits 31-0 Start Address

This 32-bit field specifies the starting address of the data to be moved to/from memory. This field is copied to the DNAD register. When the SYM53C770 transfers data to or from memory, the DNAD register is incremented by the number of bytes transferred.

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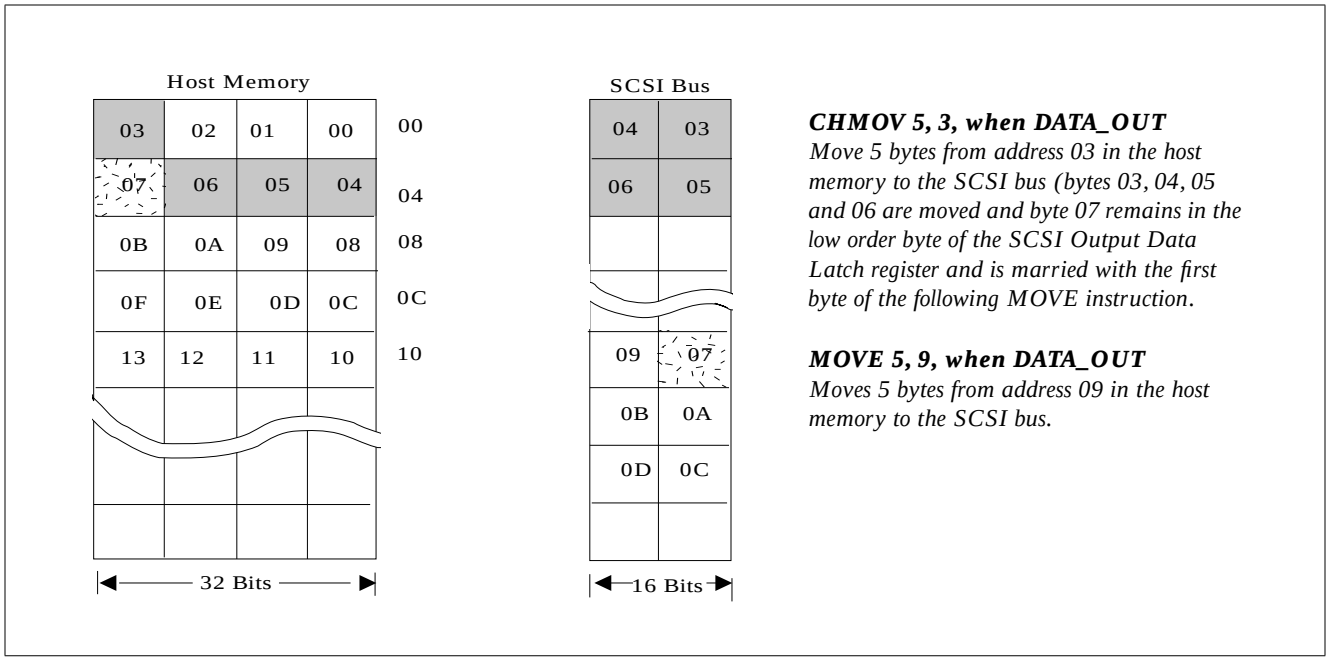


Figure 5-2: Block Move and Chained Block Move Instructions

I/O Instructions

First Longword

Bits 31-30 I/O Instruction

Bits 29-27 Op Code

The following Op Code Field bits have different meanings, depending on whether the SYM53C770 is operating in initiator or target mode.

Note: the following op codes determine if the instruction is a Read/Write or an I/O instruction. Op code selections 101, 110, and 111 are Read/Write instructions, and are described in that section.

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction (Target only)

1. The SYM53C770 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the SYM53C770 loses arbitration, then it tries again during the next available arbitration cycle without reporting any lost arbitration status.

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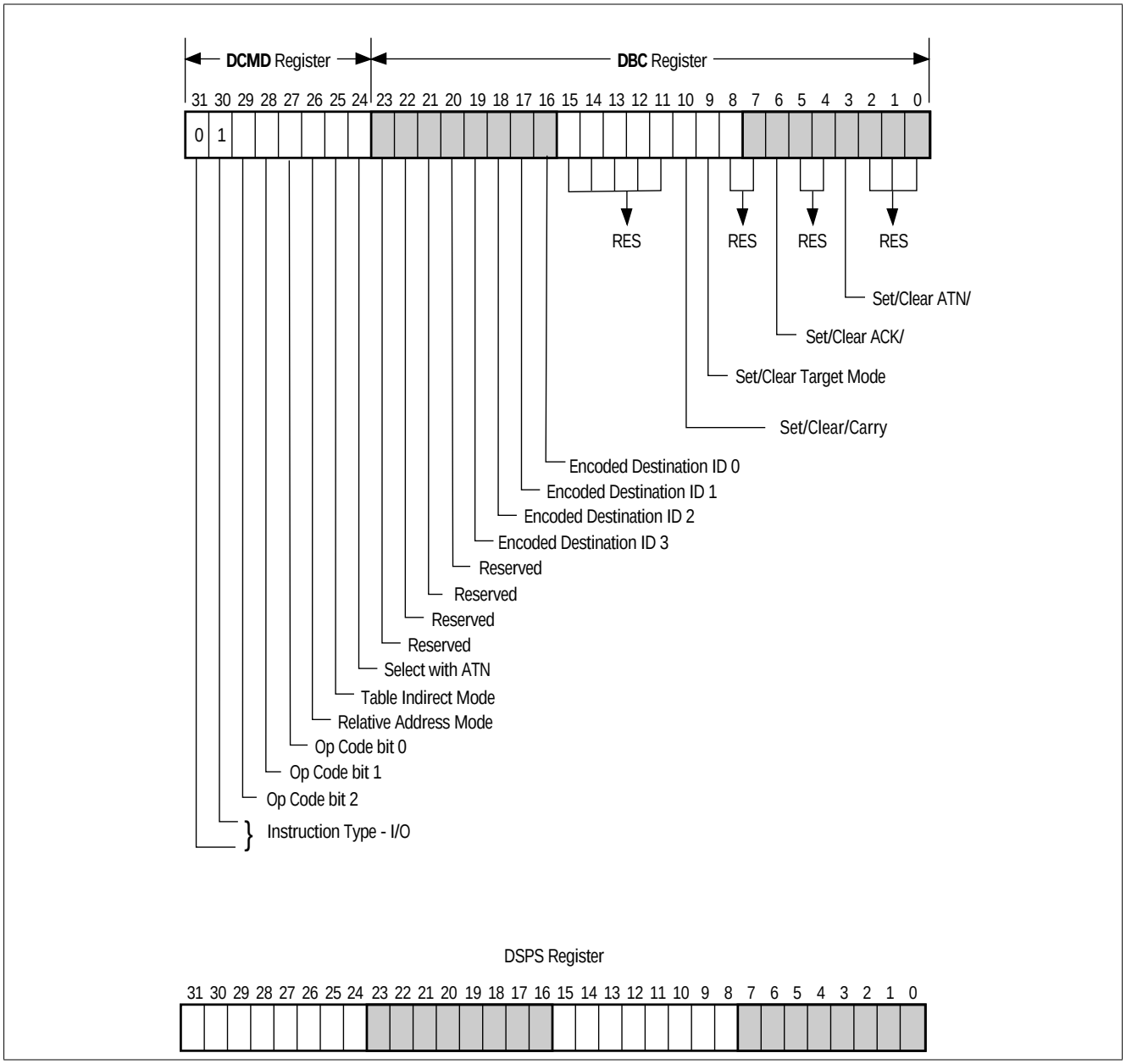


Figure 5-3: I/O Instruction Register

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2. If the SYM53C770 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the SYM53C770 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register.
3. If the SYM53C770 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The SYM53C770 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.

Disconnect Instruction (Target only)

The SYM53C770 disconnects from the SCSI bus by deasserting all SCSI signal outputs. The SCSI direction control signals are deasserted, which disables the differential pair output drivers.

Wait Select Instruction

1. If the SYM53C770 is selected, it fetches the next instruction from the address pointed to by the DSP register.
2. If reselected, the SYM53C770 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The SYM53C770 should manually be set to initiator mode when reselected.
3. If the CPU sets the SIGP bit in the ISTAT register, the SYM53C770 will abort the WAIT SELECT instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set the corresponding bit in the ALU is set.

Note: none of the signals are set on the SCSI bus in target mode.

Clear Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. When the target bit is cleared, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Note: none of the signals are reset on the SCSI bus in target mode.

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Select
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

Select Instruction

1. The SYM53C770 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the SYM53C770 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2. If the SYM53C770 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. It then fetches the next instruction from the address pointed to by the DSP register. This fetch can occur before the target responds to selection.
3. If the SYM53C770 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The SYM53C770 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.
4. If the Select with ATN/ field is set, the ATN/ signal is asserted during the selection phase.

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Wait Disconnect Instruction

The SYM53C770 waits for the target to perform a disconnect from the SCSI bus. A disconnect occurs when BSY/ and SEL/ are inactive for a minimum of one Bus Free Delay (800 ns).

Wait Reselect Instruction

1. If the SYM53C770 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The SYM53C770 should be manually set to target mode when selected.
2. If the SYM53C770 is reselected, it fetches the next instruction from the address pointed to by the DSP register.
3. If the CPU sets the SIGP bit in the ISTAT register, the SYM53C770 will abort the Wait Reselect instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. When the target bit is set, the corresponding bit in the SCNTL0 register is also set.

Clear Instruction

When the ACK/or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. ACK/ or ATN/ should not be set except for testing purposes. When the target bit is cleared, the corresponding bit in the SCNTL0 register is cleared.

Bit 26 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DNAD register is used as a relative displacement from the current DSP address.

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

Bit 25 Table Indirect Mode

When this bit is set, the 24-bit signed value in the DBC register is used as an offset relative to the value in the Data Structure Base Address (DSA) register. The SCSI ID, synchronous offset and synchronous period are loaded from this address.

Prior to the start of an I/O, the DSA must be loaded with the base address of the I/O data structure. The address may be any longword on a longword boundary.

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the op code to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory.

1. The I/O data structure must lie within the 8 MB above or below the base address.
2. An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SXFER register. The configuration bits are ordered as in the SCNTL3 register.

config	ID	offset/ period	(00)

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This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Bits 25 and 26 may be set individually or in combination:

	Bit 25	Bit 26
Direct	0	0
Table Indirect	0	1
Relative	1	0
Table Relative	1	1

Direct
Uses the device ID and physical address in the command.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect
Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

Relative
Uses the device ID in the command, but treats the alternate address as a relative jump

Command	ID	Not Used	Not Used
	Alternate Jump Offset		

Table Relative
Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. Adds the value in bits 23-0 of the first four bytes of the SCRIPTS routine to the data structure base address to form the fetch address.

Command	Table Offset
	Alternate Jump Offset

Bit 24 Select with ATN/
This bit specifies whether ATN/ will be asserted during the selection phase when the SYM53C770 is executing a Select instruction. When operating in initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

Bit 23-20 Reserved

Bits 19-16 Encoded SCSI Destination ID
This four-bit field specifies the encoded destination ID for an I/O instruction.

Bit 10 Set/Clear Carry
This bit is used in conjunction with a Set or Clear command to set or clear the Carry bit.

Bit 9 Set/Clear Target Mode
This bit is used in conjunction with a Set or Clear command to set or clear target mode. Setting this bit with a Set command configures the SYM53C770 as a target device (this sets bit 0 of the SCNTL0 register). Clearing this bit with a Clear instruction configures the chip as an initiator device.

Bit 6 Set/Clear ACK/

Bit 3 Set/Clear ATN/
These two bits are used in conjunction with a Set or Clear command to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI ACK/ signal; bit 3 controls the SCSI ATN/ signal.

Setting either of these bits will set or reset the corresponding bit in the SOCL register, depending on the command used. The Set command is used to assert ACK/ and/or ATN/ on the SCSI bus. The Clear command is used to deassert ACK/ and/or ATN/ on the SCSI bus.

Since ACK/ and ATN/ are initiator signals, they will not be asserted on the SCSI bus unless the SYM53C770 is operating as an initiator or the SCSI Loopback Enable bit is set in the STEST2 register.

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The Set/Clear SCSI ACK/ATN instruction would be used after message phase Block Move operations to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an Assert SCSI ATN instruction would be issued before a Clear SCSI ACK instruction. After the target has serviced the request for a message-out phase, ATN is deasserted with a Clear SCSI ATN instruction.

Second Longword

Bits 31-0 Jump Address

This 32-bit field specifies the address of the instruction to fetch when the SYM53C770 encounters a jump condition. The SYM53C770 fetches instructions from the address pointed to by this field whenever the SYM53C770 encounters a SCSI condition that is different from the condition specified in the instruction.

For example, during the execution of a Select instruction in initiator mode, if the SYM53C770 is reselected, then the next instruction is fetched from the address pointed to by the jump address field. For a complete description of the different jump conditions, refer to the description of each instruction.

Read/Write Instructions

The Read/Write instruction supports addition, subtraction, and comparison of two separate values within the chip. It performs the desired operation on the specified register and the SFBR register, then stores the result back to the specified register or SFBR.

The op code bits determine if the instruction is a Read/Write or an I/O instruction. Op code selections 000, 001, 010, 011, and 100 are I/O instructions, and are described in that section.

First Longword

Bits 31-30 Read/Write Instruction

Bits 29-27 Op code

The combinations of these bits determine if the instruction is a Read/Write or an I/O instruction. Op codes 000 through 100 are considered I/O instructions.

Bits 26-24 Operator

These bits are used in conjunction with the op code bits to determine which instruction is currently selected. The supported combinations are defined in Table 5-1.

Bit 24, which in earlier versions of the SYM53C770 was Carry Enable, is now included with the Operator bits.

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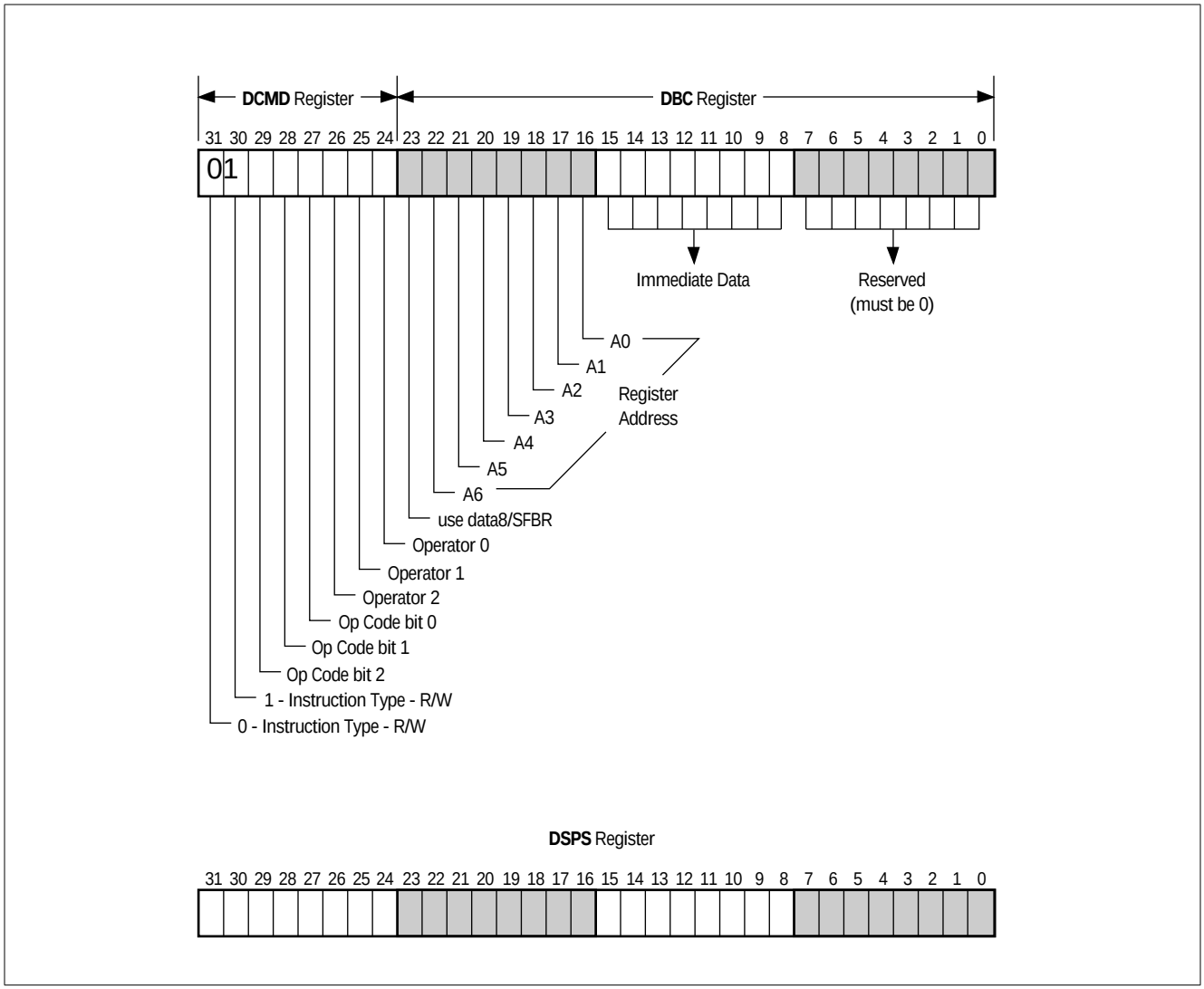


Figure 5-4: Read/Write Instruction Register

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Table 5-1: Read/Write Instructions

Operator bits 26-24	Op Code 111 Read Modify Write	Op Code 110 Move to SFBR	Op Code 101 Move from SFBR
000	Move data into register. Syntax: “Move data8 to RegA”	Move data into SFBR register. Syntax: “Move data8 to SFBR”	Move data into register. Syntax: “Move data8 to RegA”
001*	Shift register one bit to the left and place the result in the same register. Syntax: “Move RegA SHL RegA”	Shift register one bit to the left and place the result in the SFBR register. Syntax: “Move RegA SHL SFBR”	Shift the SFBR register one bit to the left and place the result in the register. Syntax: “Move SFBR SHL RegA”
010	OR data with register and place the result in the same register. Syntax: “Move RegA | data8 to RegA”	OR data with register and place the result in the SFBR register. Syntax: “Move RegA | data8 to SFBR”	OR data with SFBR and place the result in the register. Syntax: “Move SFBR | data8 to RegA”
011	XOR data with register and place the result in the same register. Syntax: “Move RegA XOR data8 to RegA”	XOR data with register and place the result in the SFBR register. Syntax: “Move RegA XOR data8 to SFBR”	XOR data with SFBR and place the result in the register. Syntax: “Move SFBR XOR data8 to RegA”
100	AND data with register and place the result in the same register. Syntax: “Move RegA & data8 to RegA”	AND data with register and place the result in the SFBR register. Syntax: “Move RegA & data8 to SFBR”	AND data with SFBR and place the result in the register. Syntax: “Move SFBR & data8 to RegA”
101*	Shift register one bit to the right and place the result in the same register. Syntax: “Move RegA SHR RegA”	Shift register one bit to the right and place the result in the SFBR register. Syntax: “Move RegA SHR SFBR”	Shift the SFBR register one bit to the right and place the result in the register. Syntax: “Move SFBR SHR RegA”
110	Add data to register without carry and place the result in the same register. Syntax: “Move RegA + data8 to RegA”	Add data to register without carry and place the result in the SFBR register. Syntax: “Move RegA + data8 to SFBR”	Add data to SFBR without carry and place the result in the register. Syntax: “Move SFBR + data8 to RegA”
111	Add data to register with carry and place the result in the same register. Syntax: “Move RegA + data8 to RegA with carry”	Add data to register with carry and place the result in the SFBR register. Syntax: “Move RegA + data8 to SFBR with carry”	Add data to SFBR with carry and place the result in the register. Syntax: “Move SFBR + data8 to RegA with carry”

Notes:

1. Substitute the desired register name or address for “RegA” in the syntax examples
2. data8 indicates eight bits of data
3. Use SFBR instead of data8 to operate on two register values

** Data is shifted through the Carry bit and the Carry bit is shifted into the data byte*

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Bit 23 Use data8/SFBR

When this bit is set, SFBR will be used instead of the data8 value during a Read-Modify-Write instruction (see Table 5-1). This allows the user to operate on two register values.

Bits 22-16 Register Address A(6-0)

Register values may be changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A(6-0) select an 8-bit source/destination register within the SYM53C770. Register addresses are always Little Endian addresses.

Bits 15-8 Immediate Data

Bits 7-0 Reserved

Read-Modify-Write Cycles

The register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation can be used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

Subtraction is not available when SFBR is used instead of data8 in the instruction syntax. To subtract one value from another when using SFBR, first XOR the value to subtract (subtrahend) with 0xFF, and add 1 to the resulting value. This creates the 2's compliment of the subtrahend. Add these two values to obtain the difference of the original two values.

Move to/from SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SFBR. The possible functions of this command are:

- Write one byte (value contained within the SCRIPTS instruction) into any chip register.
- Move to/from the SFBR from/to any other register.
- Alter the value of a register with AND/OR/ ADD operators.
- After moving values to the SFBR, the compare and jump, call, or similar commands may be used to check the value.
- A Move-to-SFBR followed by a Move-from-SFBR can be used to perform a register to register move.

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Transfer Control Instructions

First Longword

Bits 31-30 Transfer Control Instruction

Bits 29-27 Op Code

This 3-bit field specifies the type of transfer control instruction to be executed. All transfer control instructions can be conditional. They can be dependent on a true/false comparison of the ALU Carry bit or a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in initiator or target mode.

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	X	X	Reserved

Jump Instruction

1. The SYM53C770 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the SYM53C770 loads the DSP register with the contents of the DSPS register. The DSP register now contains the address of the next instruction.
2. If the comparisons are false the SYM53C770 fetches the next instruction from the address pointed to by the DSP register, leaving the instruction pointer unchanged.

Call Instruction

1. The SYM53C770 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the SYM53C770 loads the DSP register with the contents of the DSPS register and that address value becomes the address of the next instruction.

   When the SYM53C770 executes a Call instruction, the instruction pointer contained in the DSP register is stored in the TEMP register.

   When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register.
2. If the comparisons are false, the SYM53C770 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer is not modified.

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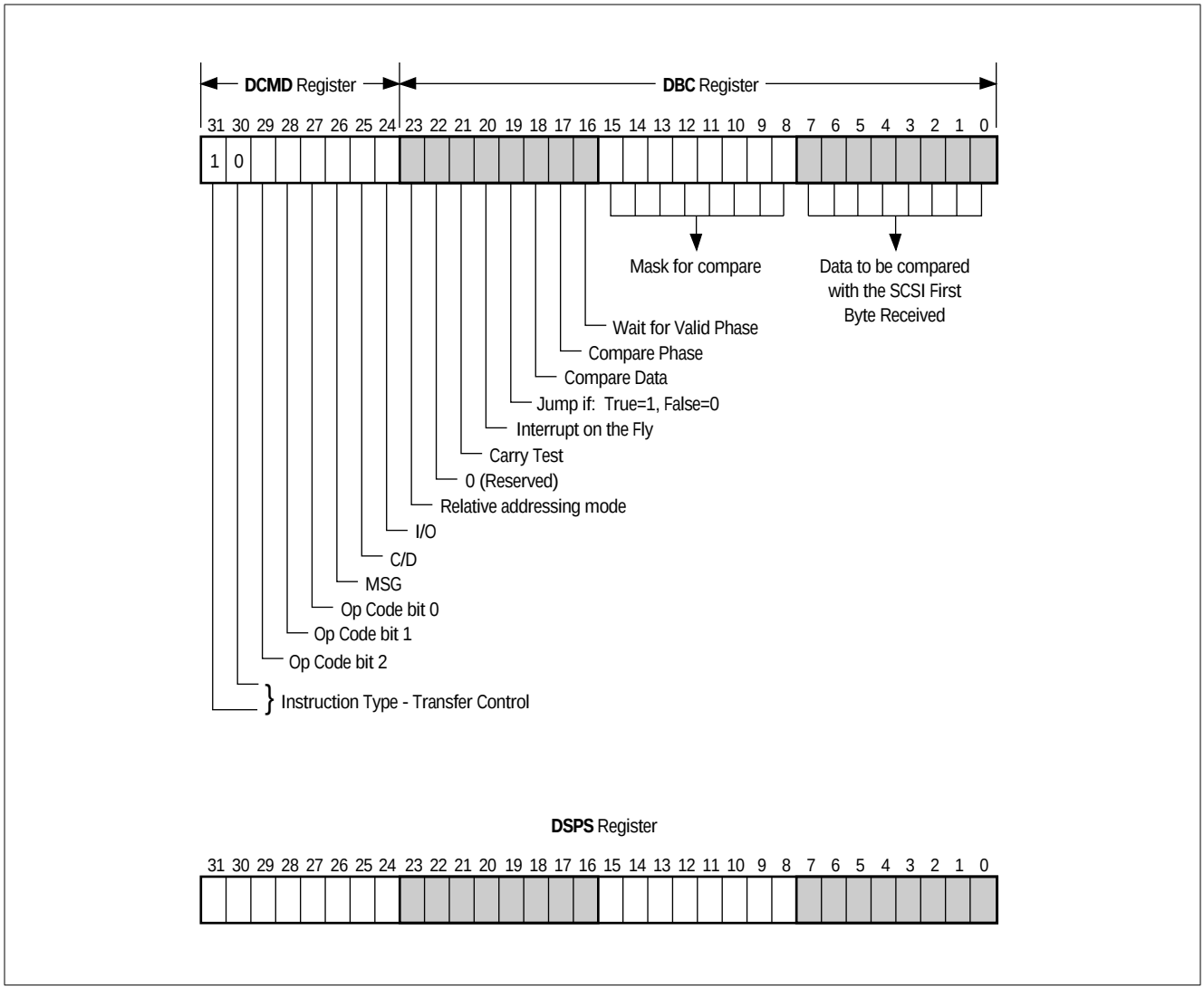


Figure 5-5: Transfer Control Instruction Register

Return Instruction

1. The SYM53C770 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the SYM53C770 loads the DSP register with the contents of the DSPS register. That address value becomes the address of the next instruction.

   When the SYM53C770 executes a Call instruction, the current instruction pointer contained in the DSP register is stored in the TEMP register.

   When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register.

   The SYM53C770 does not check to see whether the Call instruction has already been executed. It will not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

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2. If the comparisons are false, then the SYM53C770 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer will not be modified.

Interrupt Instructions

Interrupt

1. The SYM53C770 can do a true/false comparison of the ALU bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the SYM53C770 generates an interrupt by asserting the IRQ/ signal.
2. The 32-bit address field stored in the DSPS register (not DNAD as in 53C700) can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.
3. The SYM53C770 halts and the DSP register must be written to start any further operation.

Interrupt on-the-Fly

The SYM53C770 can do a true/false comparison of the ALU carry bit or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the SYM53C770 will assert the Interrupt on the fly bit (ISTAT bit 2).

Bits 26-24 SCSI Phase

This 3-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when REQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the SYM53C770 is operating in initiator mode; when the SYM53C770 is operating in the target mode, these bits should be cleared.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Message out
1	1	1	Message in

Bit 23 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DSPS register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative mode does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address – Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address – Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPTS routine currently being executed by the SYM53C770. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (twos compliment), the jump can be forward or backward.

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A relative transfer can be to any address within a 16-MB segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPTS routine is written using only relative transfers it would not require any run time alteration of physical addresses, and could be stored in and executed from a PROM.

Bit 22 Reserved

Bit 21 Carry Test

When this bit is set, decisions based on the ALU carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

Bit 20 Interrupt on the Fly

When this bit is asserted, the interrupt instruction will not halt the SCRIPTS processor. Once the interrupt occurs, the Interrupt on the Fly bit (ISTAT bit 2) will be asserted.

Bit 19 Jump If True/False

This bit determines whether the SYM53C770 should branch when a comparison is true or when a comparison is false. This bit applies to both Phase Compares and Data Compares. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

Bit 18 Compare Data

When this bit is set, then the first byte received from the SCSI data bus (contained in SFBR register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.

Bit 17 Compare Phase

When the SYM53C770 is in initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by REQ) are compared to the Phase Field in the Transfer Control instruction; if they match, then the comparison is true. The Wait for Valid Phase bit controls when the compare will occur.

When the SYM53C770 is operating in target mode this bit, when set, tests for an active SCSI ATN/ signal.

Bit 16 Wait For Valid Phase

If the Wait for Valid Phase bit is set, then the SYM53C770 waits for a previously unserviced phase before comparing the SCSI phase and data.

If the Wait for Valid Phase bit is clear, then the SYM53C770 compares the SCSI phase and data immediately.

Bits 15-8 Data Compare Mask

The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored.

For instance, a mask of 01111111b and data compare value of 1XXXXXXXb allows the SCRIPTS processor to determine whether or not the high order bit is on while ignoring the remaining bits.

Bits 7-0 Data Compare Value

This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

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Second Longword

Bits 31-0 Jump Address

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the SYM53C770 has fetched the instruction from the address pointed to by these 32 bits, this address is incremented by four, loaded into the DSP register and becomes the current instruction pointer.

Memory Move Instructions

The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

Allowing the SYM53C770 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 MB may be transferred with one instruction. There are two restrictions:

1. Both the source and destination addresses must start with the same address alignment (A(1-0) must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur. If cache line burst is enabled and the byte count is greater than 32 bytes, address lines A(3-0) must be the same.
2. Indirect addresses are not allowed.

A special block move instruction passes the source and destination addresses and the byte count to the SYM53C770. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPT is fetched from system memory.

Upon completion of the move, an interrupt instruction or jump to a SCSI function should be executed.

The DSPS and DSA registers are additional holding registers used during the Memory Move

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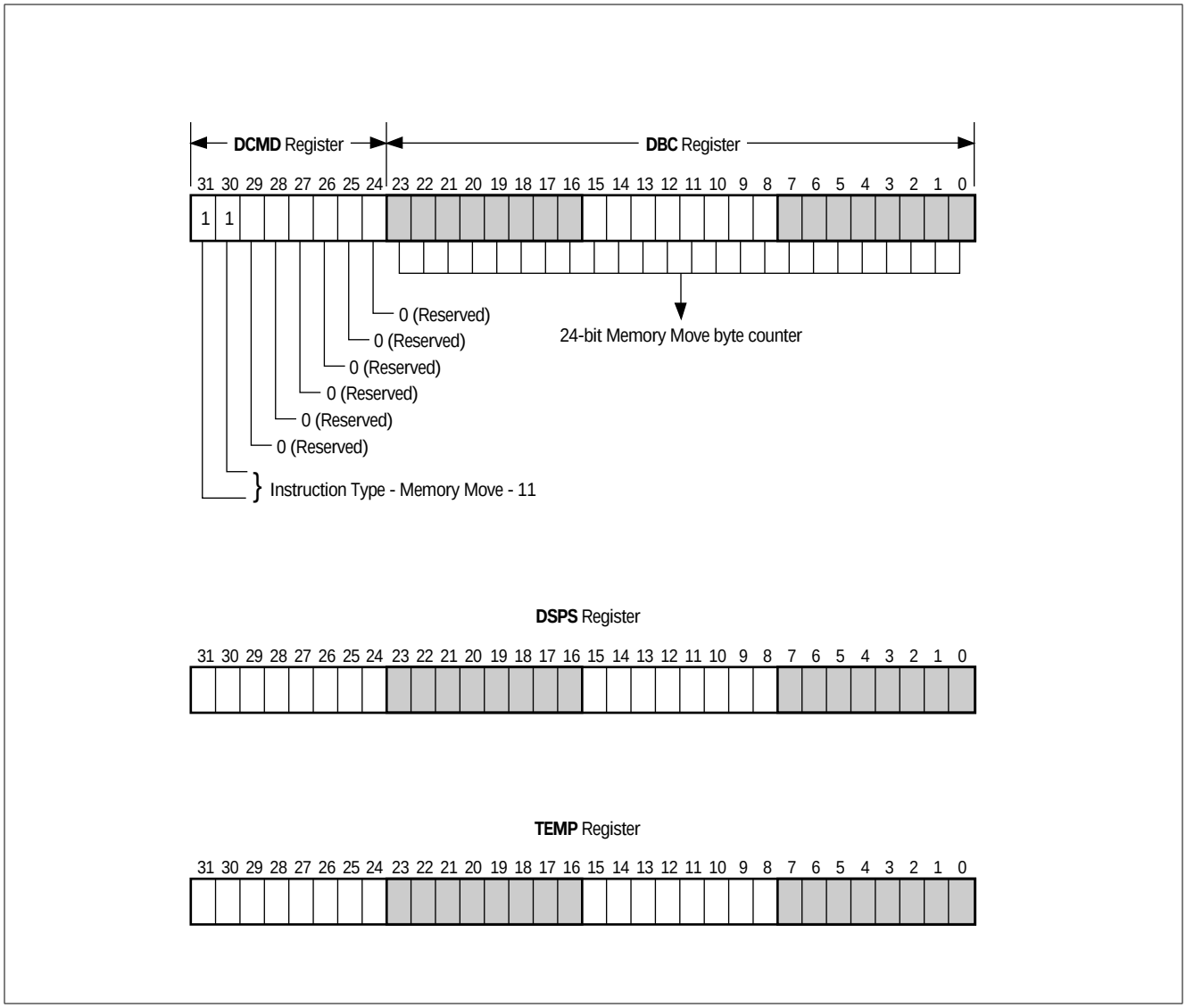


Figure 5-6: Memory Move Instruction Register

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First Longword

Bits 31-30 Memory Move Instruction

Bits 29-24 Reserved

These bits are reserved and must be zero. If any of these bits is set, an illegal instruction interrupt will occur.

Bits 23-0 Transfer Count

The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.

Second Longword

Bits 31-0 Source Address

This is the absolute 32-bit starting address of the data in memory.

Third Longword

Bits 31-0 Destination Address

This is the absolute 32-bit destination address of where to move the data.

Read/Write System Memory from a SCRIPTS Routine

By using the Memory Move instruction, single or multiple register values may be transferred to/from system memory.

Because the Chip Select (CS/) input is derived from an address decode, it could activate during a Memory Move operation if the source/destination address decodes to within the chip's register space. If this occurs, the register indicated by the lower seven bits of the memory address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate SYM53C770 register (for example, from a SCRATCH register), and then to the SFBR.

The same address alignment restrictions apply to register access operations as to normal memory-to-memory transfers.

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Chapter 6
Electrical Characteristics

Absolute Maximum Stress Ratings*

Table 6-1: Absolute Maximum Stress Ratings

Parameter	Symbol	Min	Max	Units
Storage temperature	T_{STG}	-55	150	ºC
Supply voltage	V_{DD}	-0.5	7.0	V
Input voltage	V_{IN}	V_{SS}-0.5	V_{DD} + 0.5	V
Latch-up current	I_{LP}	± 200	-	mA**
Electrostatic discharge	ESD***	-	2K	V

** Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of this specification is not implied.*

*** -2V = Vpin > +8V*

**** SCSI pins only. Measured according to MIL-STD-883C, Method 3015.7*

Operating Conditions

Table 6-2: Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{DD}	4.75	5.25	V
Supply current (Static)	I_{DD}	-	1	mA
Supply current (Dynamic)	I_{DD}	-	75	mA
Operating temperature (free air)	T_A	0	70	ºC
Thermal resistance (junction-ambient)	U_{JA}	50	65	ºC/W
Power dissipation	P_{DD}	0	0.40	W

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DC Characteristics

V_{DD} = 5V ± 5%, T_A = 0 to 70 °C, unless otherwise noted.

Table 6-3: SCSI Signals — SD(15-0)/*, SDP0/*, REQ/*, MSG/, I_O/, C_D/, ATN/, ACK/*, BSY/, SEL/, RST/, SDP1*

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Output low voltage	V_{OL}	V_{SS}	0.5	V	I_{OL} = 48 mA
Hysteresis	V_{HYS}	300	-	mV	-
Input leakage current	I_{IN}	-10	10	µA	-
Input leakage—SCSI RST/		-400	10	µA	-
Tristate leakage current	I_{OZ}	-10	10	µA	-

**TolerANT not enabled*

Table 6-4: Input Signals—BG/-HLDAI/, BOFF/, RESET/, CS/, BS(2-0)/, BCLK, SCLK, AUTO/, DIFFSENS, RAMCS/

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Input leakage current	I_{IN}	-10.0	10.0	µA	-

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Table 6-5: Input Signal—TSTIN/

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Input high leakage current	I_{IH}	-10	10	µA	$V_{IH} = V_{DD}$
Input low pull-up current	I_{IL}	-200	-50	µA	V_{IL} = 0 V

Table 6-6: Output Signals—SDIR(15-0), SDIRP0, BSYDIR, SELDIR, RSTDIR, TGS, IGS, SDIRP1

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -4 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 4 mA
Output high current	I_{OH}	-2.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	4.0	-	mA	V_{OL} = 0.4 V

Table 6-7: Output Signals—FETCH/, IRQ/, TSTOUT

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -8 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 8mA
Output high current	I_{OH}	-4.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	8.0	-	mA	V_{OL} = 0.4 V

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Table 6-8: Output Signal—SLACK/-READYO/, MASTER/, MAC/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -16 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 16 mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	16.0	-	mA	V_{OL} = 0.4 V

Table 6-9: Tristate Output Signals—A(31-7), FC(2-0)-TM(2-0), SC(1-0), UPSO-TT0/, CBREQ/-TT1/, BR/-HOLD/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -16 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 16mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	16.0	-	mA	V_{OL} = 0.4 V
Tristate leakage current	I_{OZ}	-10	10	µA	-

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Table 6-10: Bidirectional Signals—A(6-0), D(31-0), DP(3-0), DS/-DLE/, AS/-TS/-ADS/, R_W/, BE0, BE1/, SIZ1-0, BHE/-BE2, SIZ1-BE3, BERR/-TEA/, HALT/-TIP/, BGACK-BB/, CBACK/-TBI/, STERM/-TA/-READYI/, GPIO (4-0)

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -16 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 16 mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	16.0	-	mA	V_{OL} = 0.4 V
Input leakage current	I_{IN}	-10	10	µA	-
Tristate leakage current	I_{OZ}	-10	10	µA	-

Table 6-11: Capacitance

Parameter	Symbol	Min	Max	Units
Input capacitance of input pads	C_I	-	7	pF
Input capacitance of I/O pads	C_{IO}	-	10	pF

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Symbios Logic TolerANT Technology

Table 6-12: TolerANT Active Negation Technology Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}[1]	Output high voltage	2.5	3.1	3.5	V	I_{OH} = 2.5 mA
V_{OL}	Output low voltage	0.1	0.2	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	-	7.0	V	-
V_{IL}	Input low voltage	-0.5	-	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	-0.66	-0.74	-0.77	V	V_{DD} = 4.75V I_I = -20 mA
V_{TH}	Threshold, high to low	1.1	1.2	1.3	V	-
V_{TL}	Threshold, low to high	1.5	1.6	1.7	V	-
V_{TH}-V_{TL}	Hysteresis	300	350	400	mV	-
I_{OH}[1]	Output high current	2.5	15	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	150	200	mA	V_{OL} = 0.5 V
I_{OSH}[1]	Short-circuit output high current	-	-	625	mA	Output driving low, pin shorted to V_{DD} supply[2]
I_{OSL}	Short-circuit output low current	-	-	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	-	0.05	10	µA	-0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V
I_{LL}	Input low leakage	-	-0.05	-10	µA	-0.5 < V_{DD} < 5.25 V_{PIN} = 0.5 V
R_I	Input resistance	-	20	-	MΩ	SCSI pins[3]

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

[1] *Active negation outputs only: Data, Parity, SREQ/, SACK/*

[2] *Single pin only; irreversible damage may occur if sustained for one second*

[3] *SCSI RESET pin has 10 kΩ pull-up resistor*

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Table 6-12: TolerANT Active Negation Technology Electrical Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
C_P	Capacitance per pin	-	8	10	pF	PQFP
t_R[1]	Rise time, 10% to 90%	9.7	15.0	18.5	ns	Figure 7-1
t_F	Fall time, 90% to 10%	5.2	8.1	14.7	ns	Figure 7-1
dV_H/dt	Slew rate, low to high	0.15	0.23	0.49	V/ns	Figure 7-1
dV_L/dt	Slew rate, high to low	0.19	0.37	0.67	V/ns	Figure 7-1
ESD	Electrostatic discharge	2	-	-	KV	MIL-STD-883C; 3015-7
	Latch-up	100	-	-	mA	-
	Filter delay	20	25	30	ns	Figure 7-2
	Extended filter delay	40	50	60	ns	Figure 7-2

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

[1] *Active negation outputs only: Data, Parity, SREQ/, SACK/*

[2] *Single pin only; irreversible damage may occur if sustained for one second*

[3] *SCSI RESET pin has 10 kΩ pull-up resistor*

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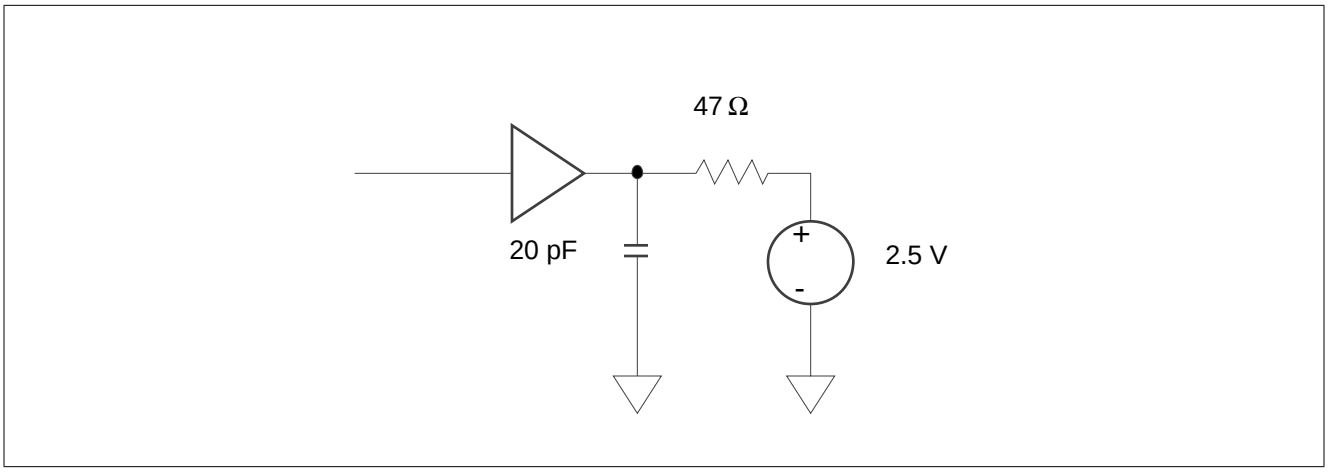


Figure 6-1: Rise and Fall Time Test Conditions

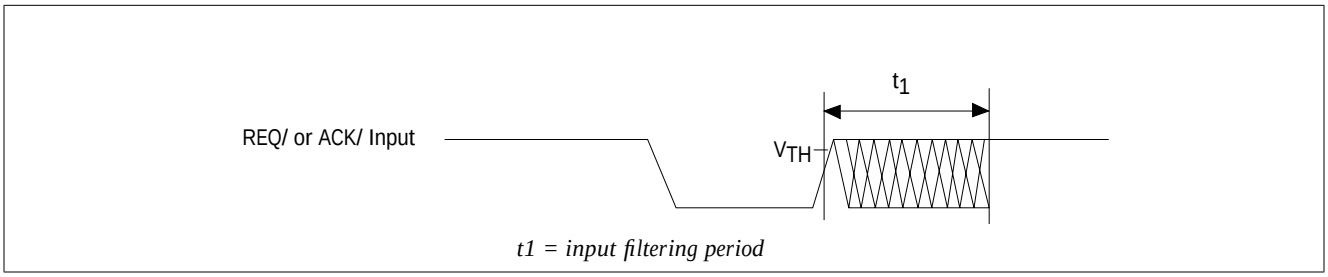


Figure 6-2: SCSI Input Filtering

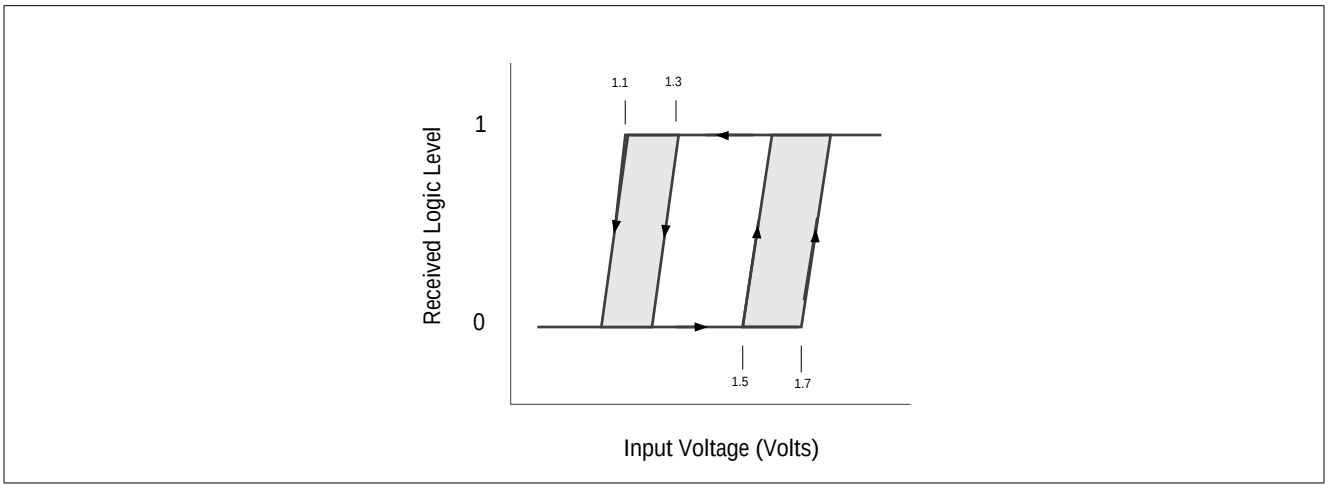


Figure 6-3: Hysteresis of SCSI Receiver

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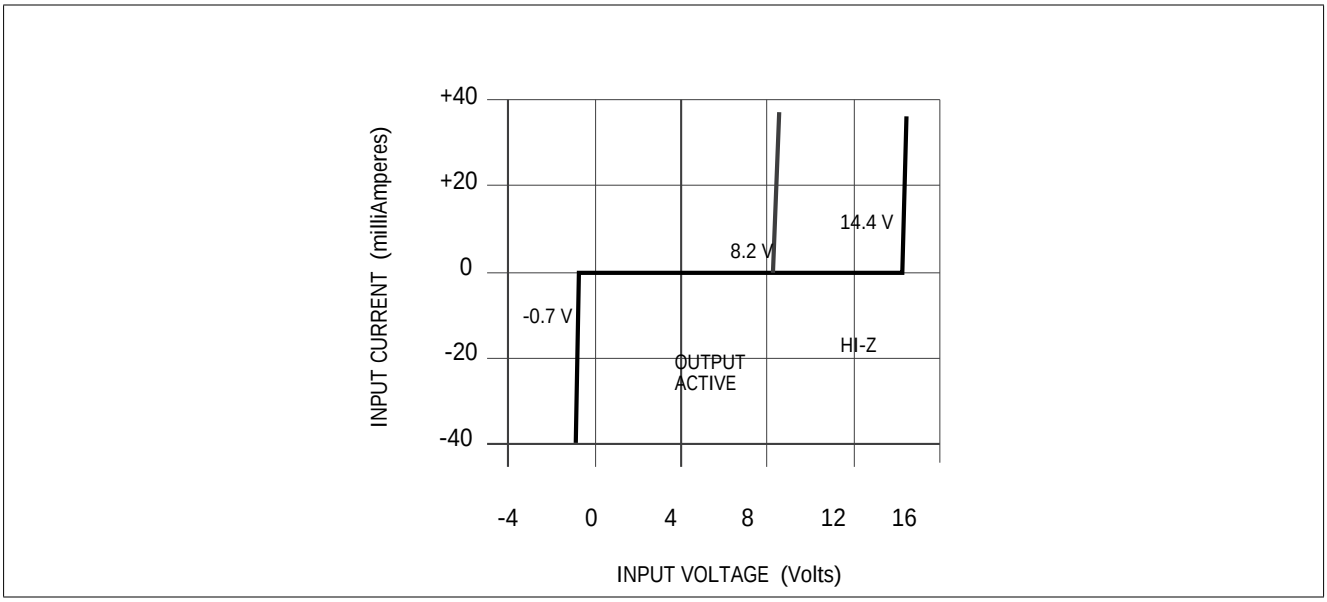
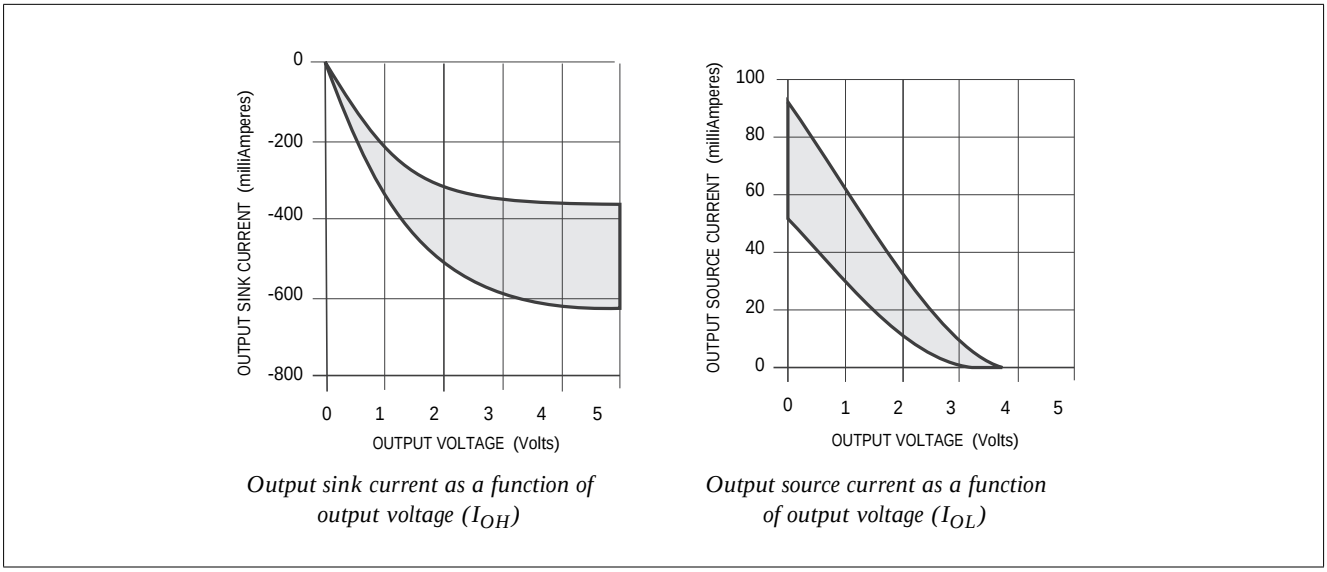


Figure 6-4: Input current as a Function of Input Voltage



Output sink current as a function of output voltage (I_{OH})

Output source current as a function of output voltage (I_{OL})

Figure 6-5: Output Current as a Function of Output Voltage

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AC Characteristics

The AC characteristics in this section apply over the entire range of operating conditions (refer to Table 6-2, “Operating Conditions”). Chip timings are based on simulation at worst case voltage, temperature, and processing.

Clock Timings

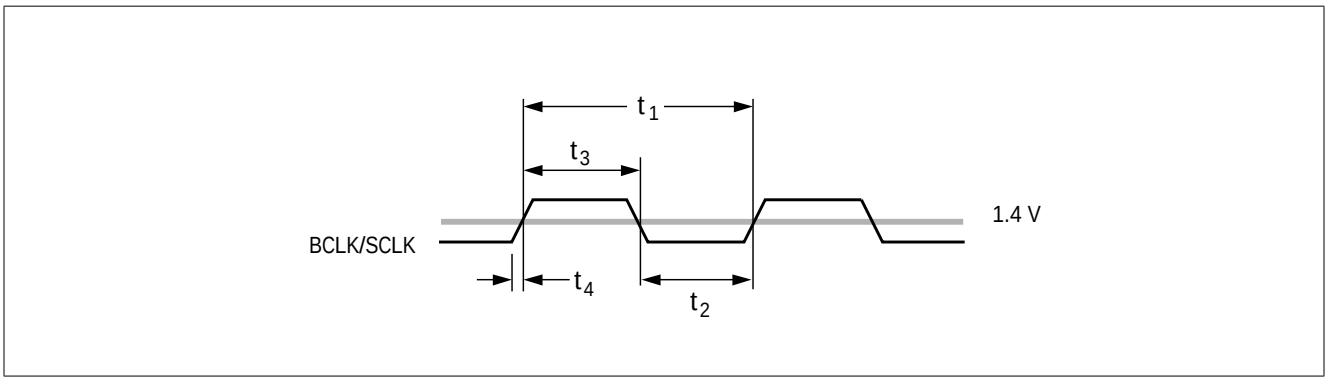


Figure 6-6: Clock Waveform

Table 6-13: Clock Timings

Parameter	Symbol	Min	Max	Units
Bus clock cycle time (BCLK)	t_1			
Bus Mode 1		40	DC	ns
Bus Mode 2, 3, 4		30	DC	ns
SCSI clock cycle time (SCLK)*		15	60	ns
BCLK low time	t_2	40% of BCLK cycle time	DC	ns
Bus Mode 1			DC	ns
Bus Modes 2, 3, 4				
SCLK low time*		40% of SCLK cycle time	33	ns
BCLK high time	t_3	40% of BCLK cycle time	-	ns
Bus Mode 1			-	ns
Bus Modes 2, 3, 4				
SCLK high time		40% of SCLK cycle time	33	ns
BCLK slew rate	t_4	1	-	V/ns
SCLK slew rate		1	-	V/ns

** This parameter must be met to insure SCSI timings are within specification*

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Reset Input

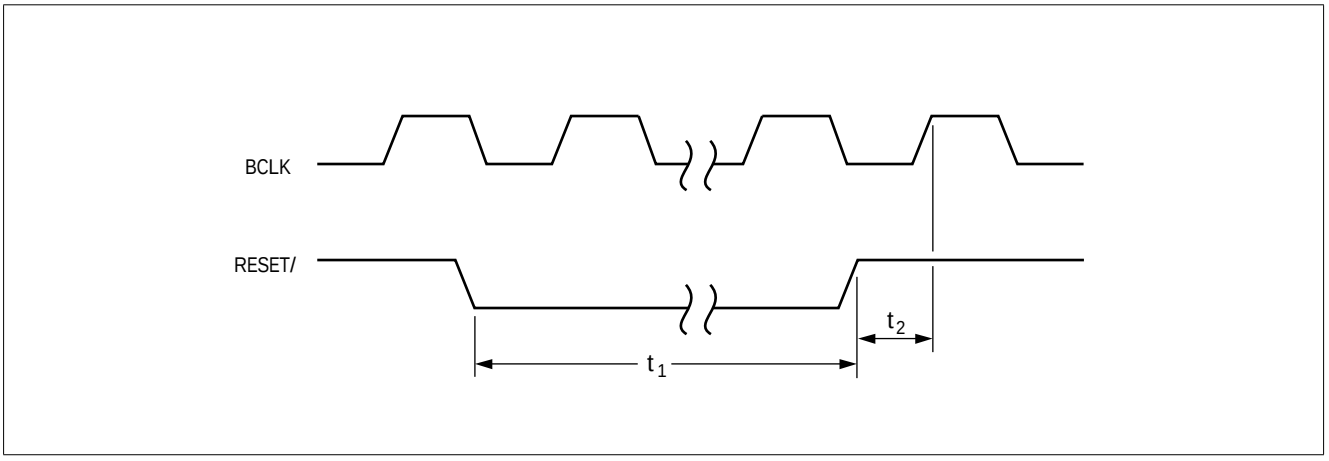


Figure 6-7: Reset Input Waveforms

Table 6-14: Reset Input Timings

Parameter	Symbol	Min	Max	Units
Reset pulse width	t_1	10	-	BCLK
Reset deasserted setup to BCLK high	t_2	10	-	ns

Interrupt Output

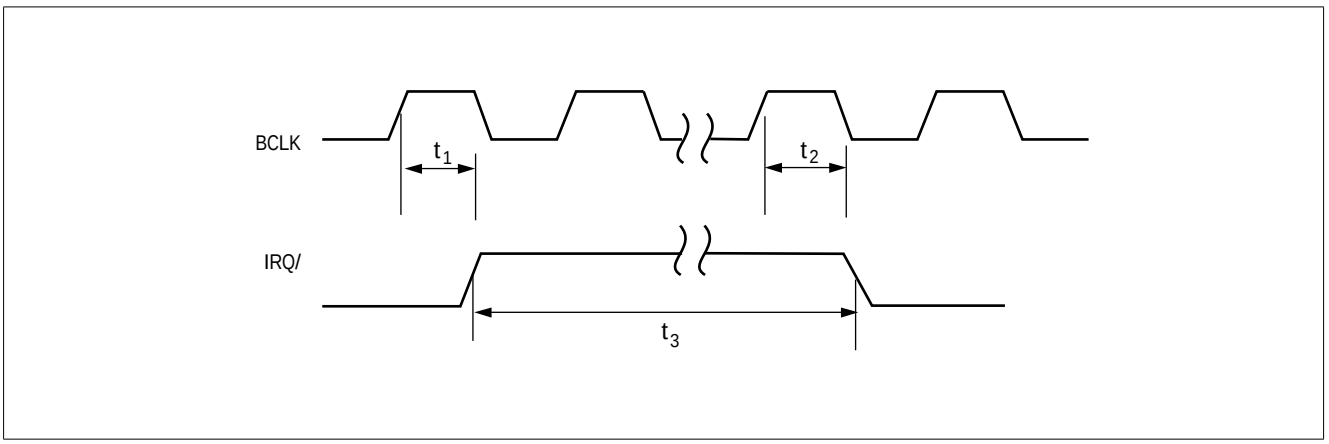


Figure 6-8: Interrupt Output Waveforms

Table 6-15: Interrupt Output Timings

Parameter	Symbol	Min	Max	Units
BCLK high to IRQ/ high	t_1	-	20	ns
BCLK high to IRQ/ low	t_2	-	58	ns
IRQ/ deassertion time	t_3	3	-	BCLK

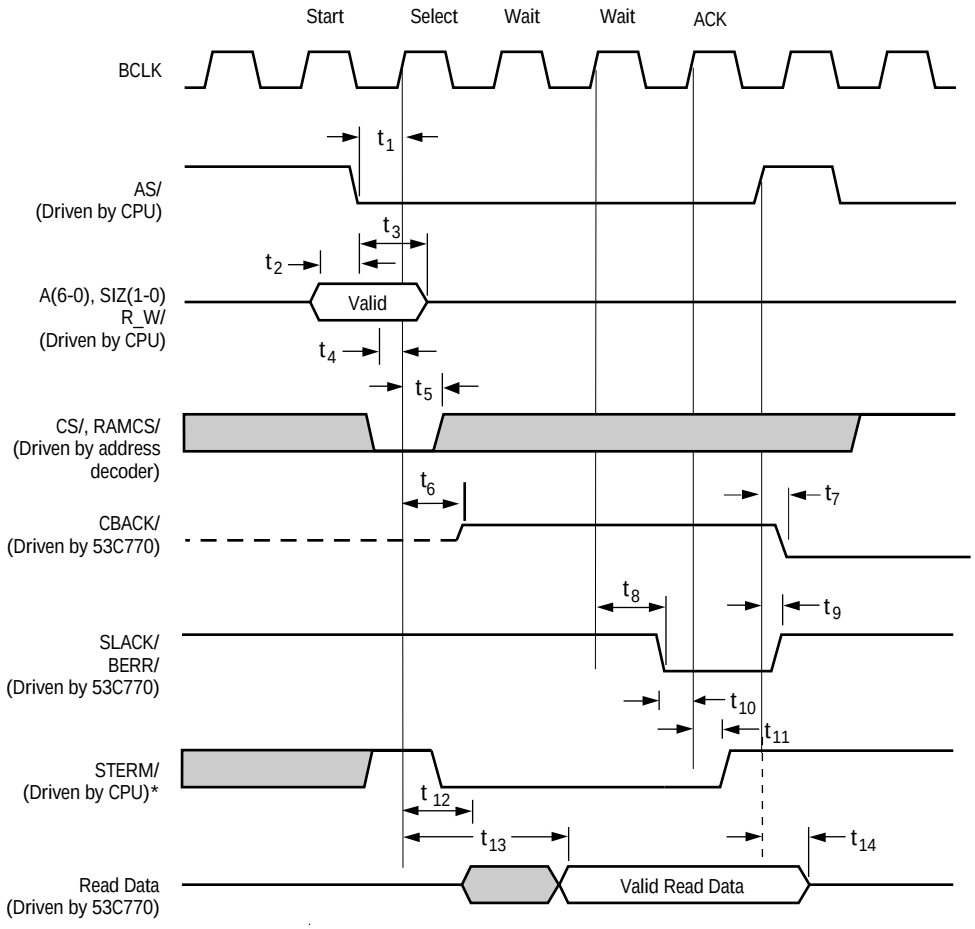
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Bus Mode 1 Slave Cycle

Bus Mode 1 Slave Read Sequence

1. R_W/, Address, and Size lines are asserted by the CPU.
2. Address Strobe is asserted by the CPU.
3. Chip Select is validated by the SYM53C770 on any following rising edge of BCLK.
4. Cache Burst Acknowledge is deasserted by the SYM53C770.
5. Two clock cycles of wait state are inserted (these wait states are required) and the data lines are asserted by the SYM53C770.
6. Slave Acknowledge is asserted by the SYM53C770 if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7. STERM/ is sampled.
8. Address Strobe is deasserted by the CPU.
9. Slave Acknowledge or Bus Error is deasserted by the SYM53C770 and the data lines are tristated by the SYM53C770.

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** This signal may be driven the by SYM53C770 if the Enable ACK bit is set (DCNTL bit 5). See the explanation in Chapter 2 for use of this signal as an output.*

Note: The 53C770 must see address strobes (AS/) paired up with synchronous cycle terminations (STERM/), even though the slave cycle may not be intended for the 53C770.

Figure 6-9: Bus Mode 1 Slave Read Waveforms

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Table 6-16: Bus Mode 1 Slave Read Timings

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(6-0), SIZ(1-0), R_W/ setup to AS/	t_2	4	-	ns
A(6-0), SIZ(1-0), R_W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	30	ns
AS/ high to CBACK/ low	t_7	3	17	ns
BCLK high to SLACK/, BERR/ low	t_8	-	22	ns
AS/ high to SLACK/, BERR/ high	t_9	-	22	ns
STERM/ setup to BCLK high	t_{10}	3	-	ns
STERM/ hold from BCLK high	t_{11}	7	-	ns
BCLK high to data bus driven	t_{12}	8	28	ns
BCLK high to read data valid	t_{13}	-	75	ns
AS/ high to data bus high-Z	t_{14}	7	32	ns

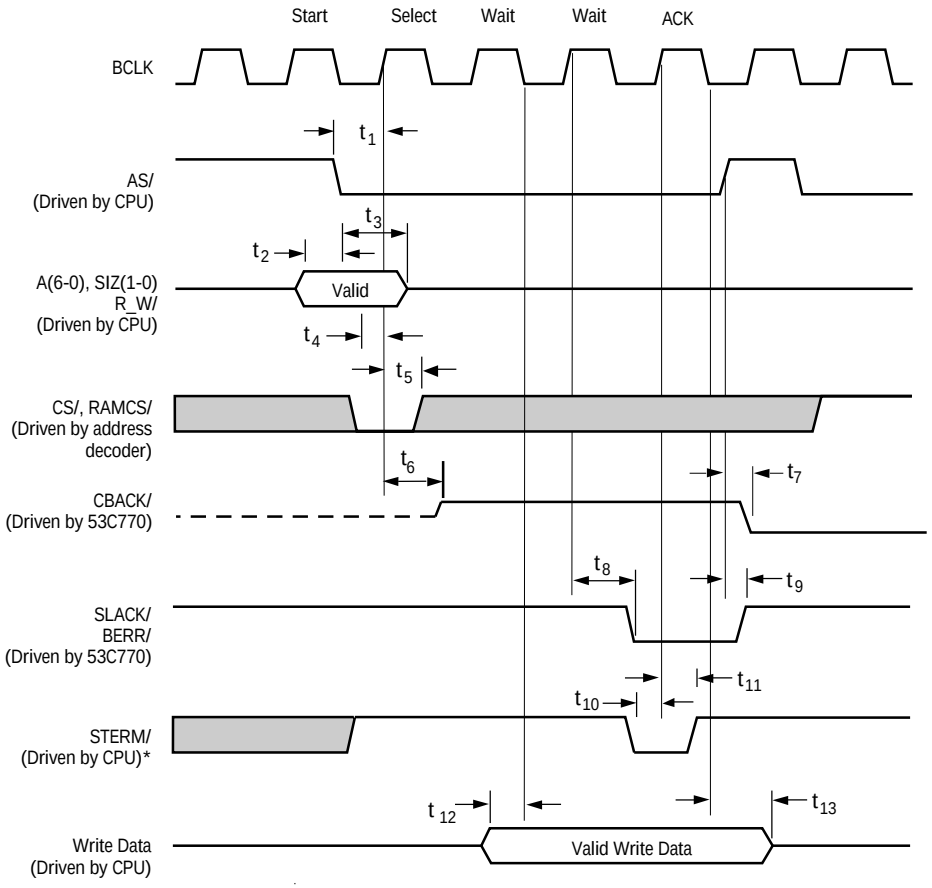
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Bus Mode 1 Slave Write Sequence

1. R_W/, Address, and Size lines are asserted by the CPU.
2. Address Strobe is asserted by the CPU.
3. Chip Select is validated by the SYM53C770 on any following rising edge of BCLK.
4. Cache Burst Acknowledge is deasserted by the SYM53C770
5. The data lines are asserted by the CPU.
6. Slave Acknowledge is asserted by the SYM53C770 if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7. STERM/ is sampled.
8. Address Strobe is deasserted by the CPU.
9. Slave Acknowledge or Bus Error is deasserted by the SYM53C770.

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10.



** This signal may be driven by the SYM53C770 if the Enable ACK bit is set (DCNTL bit 5). See Chapter 2 for information on using this signal as an output.*
Note: data is latched on the rising edge of the ACK cycle when SLACK/ is asserted. Wait states cannot be inserted by using STERM/

Figure 6-10: Bus Mode 1 Slave Write Waveforms

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Table 6-17: Bus Mode 1 Slave Write Timings

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(6-0), SIZ(1-0), R_W/ setup to AS/	t_2	4	-	ns
A(6-0), SIZ(1-0), R/W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	30	ns
AS/ high to SLACK/ BERR/ high	t_7	3	17	ns
BCLK high to SLACK/, BERR/ low	t_8	-	22	ns
AS/ high to SLACK/, BERR/ high	t_9	-	22	ns
STERM/ (input) setup to BCLK high	t_{10}	3	-	ns
STERM/ (input) hold from BCLK high	t_{11}	7	-	ns
Write data setup to BCLK low	t_{12}	4	-	ns
Write data hold from BCLK low	t_{13}	6	-	ns

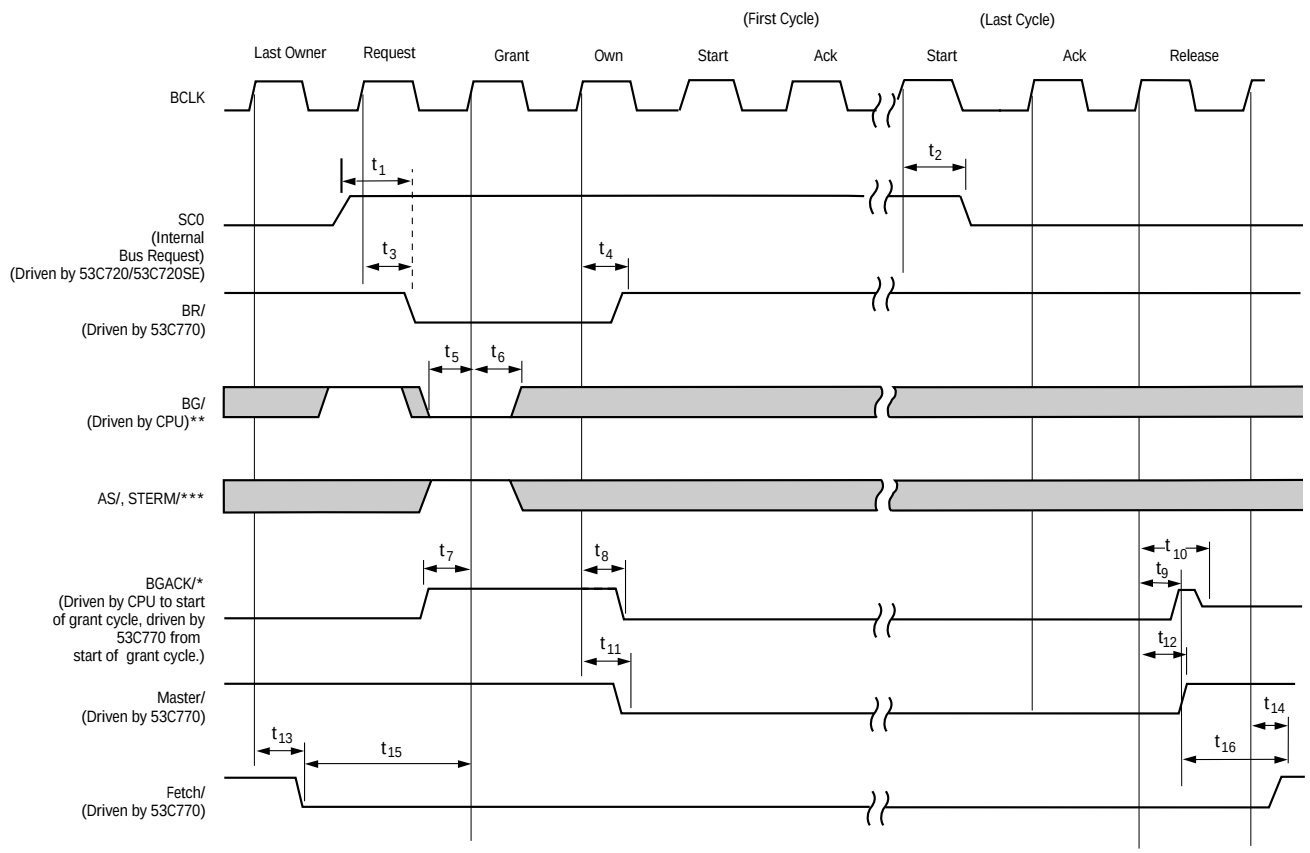
Note: The 53C770 must see address strobes (AS/) paired up with synchronous cycle terminations (STERM/), even though the slave cycle may not be intended for the 53C770.

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Bus Mode 1 Host Bus Arbitration

Bus Arbitration Sequence

1. The SYM53C770 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2. Bus Request is asserted.
3. The SYM53C770 waits for Bus Grant and checks that Bus Grant Acknowledge is deasserted. Then the SYM53C770 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.



**If the Fast Arbitration bit is set (DCNTL bit 1), the SYM53C770 will drive the BGACK/ signal as soon as it receives a Bus Grant. One clock cycle of arbitration will be saved.*

****AS/ and STERM/ must be deasserted at this point for the SYM53C770 to take control of the bus.*

Note: the SYM53C770 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access—it deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will then generate an interrupt, which the system may service.

Figure 6-11: Bus Mode 1 Host Bus Arbitration

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Table 6-18: Bus Mode 1 Host Bus Arbitration Timings

Parameter	Symbol	Min	Max	Unit
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle•	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BGACK/ setup to BCLK high (any rising edge after BR/)	t_7	5	-	ns
BCLK high to BGACK/ low	t_8	4	24	ns
BCLK high to BGACK/ high	t_9	3	19	ns
BCLK high to BGACK/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BGACK/ high to FETCH/ high**	t_{16}	1	2	BCLK

** When Snoop Mode bit 0 of CTEST3 is set to 1*

*** During a retry operation, FETCH/ will remain low until a successful completion of the op code fetch or a fatal bus error.*

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Bus Mode 1 Fast Arbitration

Fast Arbitration Sequence*

1. The internally determines if bus mastership is required. FETCH/ is asserted during cycles in which the SYM53C770 is retrieving new SCRIPTS instructions.
2. Bus Request is asserted.
3. The SYM53C770 waits for Bus Grant. The SYM53C770 becomes bus master asynchronously on the leading edge of BG/. The SYM53C770 asynchronously asserts Bus Grant Acknowledge and Master, then deasserts Bus Request.
4. The SYM53C770 issues a start cycle on the next rising edge of BCLK.

** The Fast Arbitration bit must be set.*

Note: In fast arbitration mode, the SYM53C770 will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BGACK/

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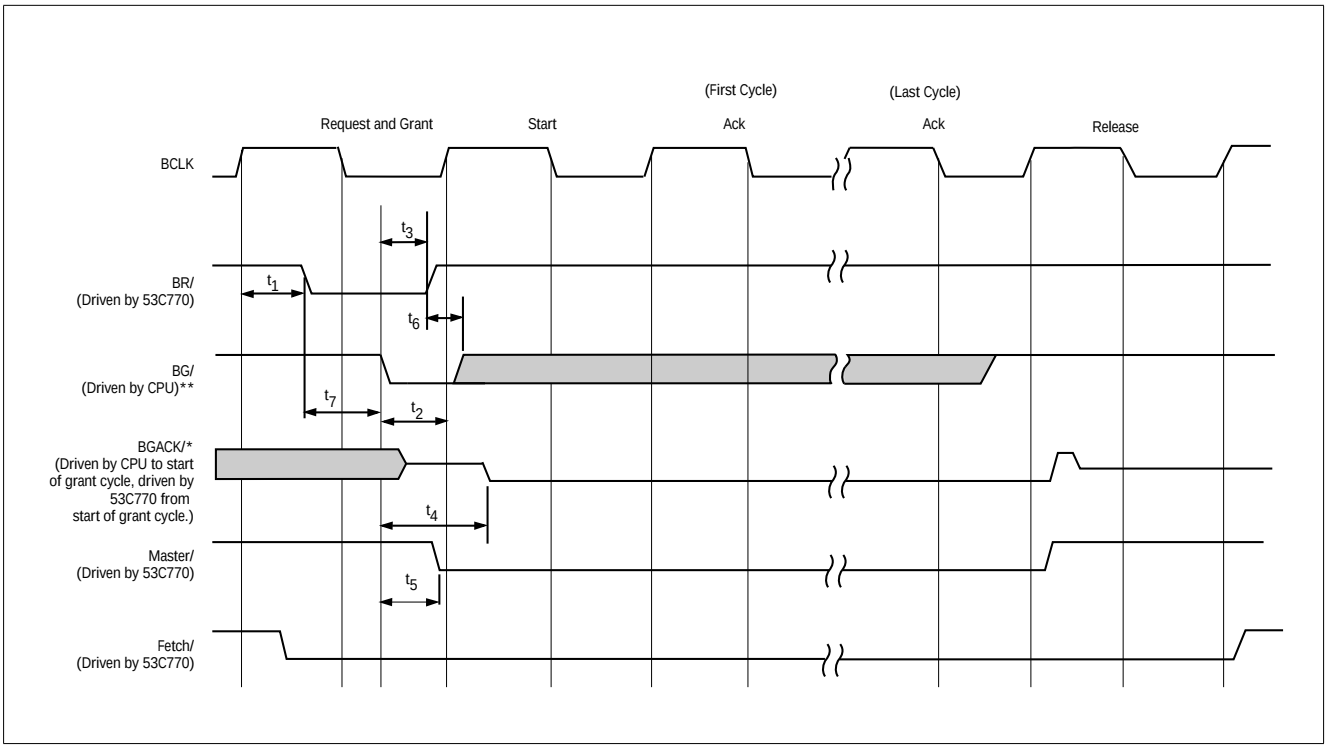


Figure 6-12: Bus Mode 1 Fast Arbitration

Table 6-19: Bus Mode 1 Fast Arbitration Timings

Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	20	ns
BG/ setup to BCLK high	t_2	12	-	ns
BG/ asserted to BR/ deasserted	t_3	-	22	ns
BG/ asserted to BGACK/ asserted	t_4	-	20	ns
BG/ asserted to MASTER/ asserted	t_5	-	16	ns
BG/ hold after BR/ deasserted*	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns

**BG/ may not be asserted prior to BR/*

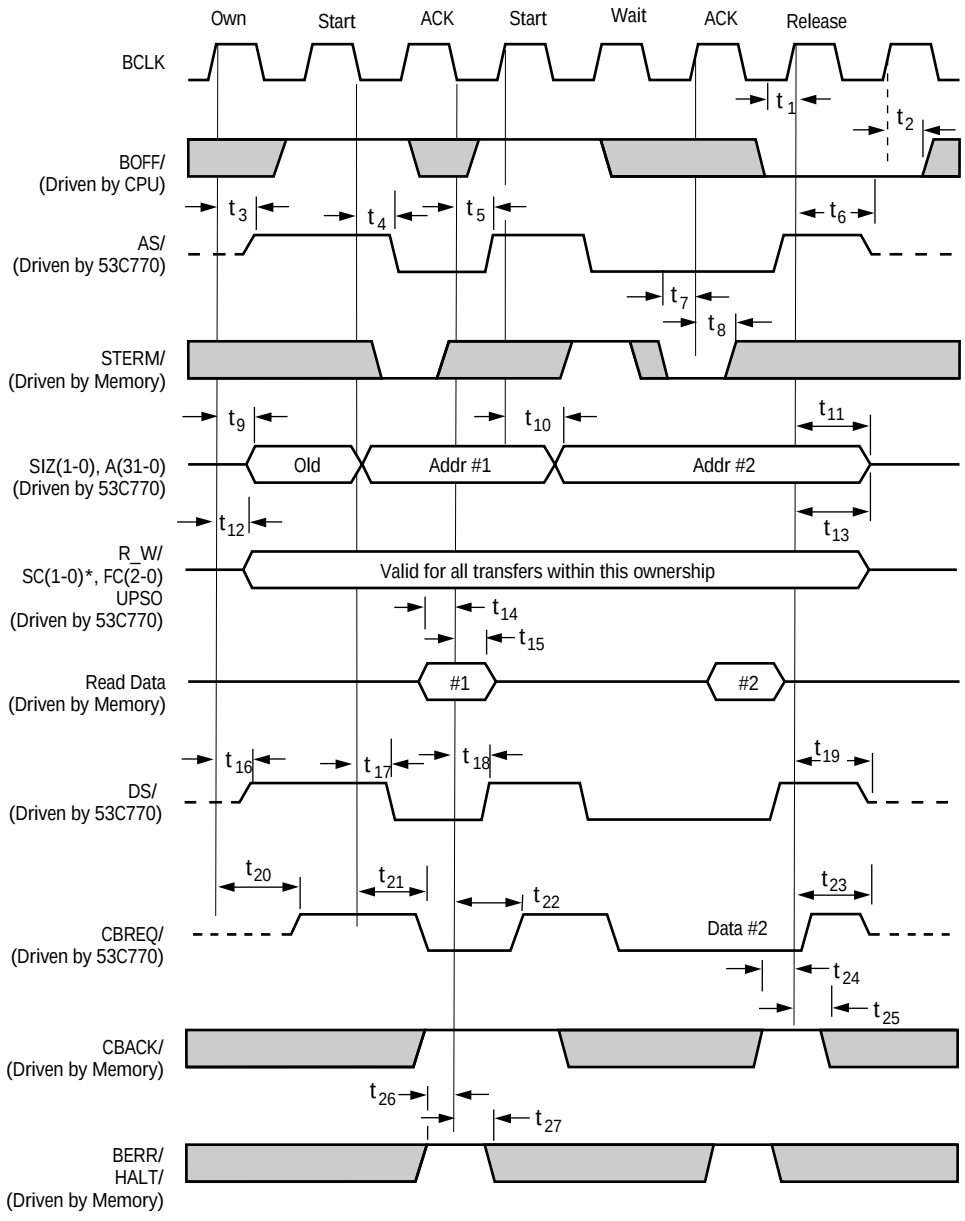
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Bus Mode 1 Master Cycle

Bus Mode 1 Master Read Sequence

1. The SYM53C770 has attained bus mastership.
2. The SYM53C770 asserts the R_W/, Snoop Control, Function Control, and general purpose lines.
3. The SYM53C770 asserts the address and size lines.
4. The SYM53C770 asserts Address Strobe, Cache Burst Request (if bursting is enabled), and Data Strobe.
5. The SYM53C770 waits for Synchronous Termination, Valid Data, Cache Burst Acknowledge, Bus Error, and Halt.
   - If Cache Burst Acknowledge is asserted, attempt bursting. Otherwise, proceed with non-cache transfers.
   - If Bus Error and Halt are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or Halt, and the SYM53C770 requires more cycles, then return to step 3.
6. Upon acknowledge of the last bus cycle, the SYM53C770 deasserts Master and Bus Grant Acknowledge.
7. The SYM53C770 floats the control and address lines.

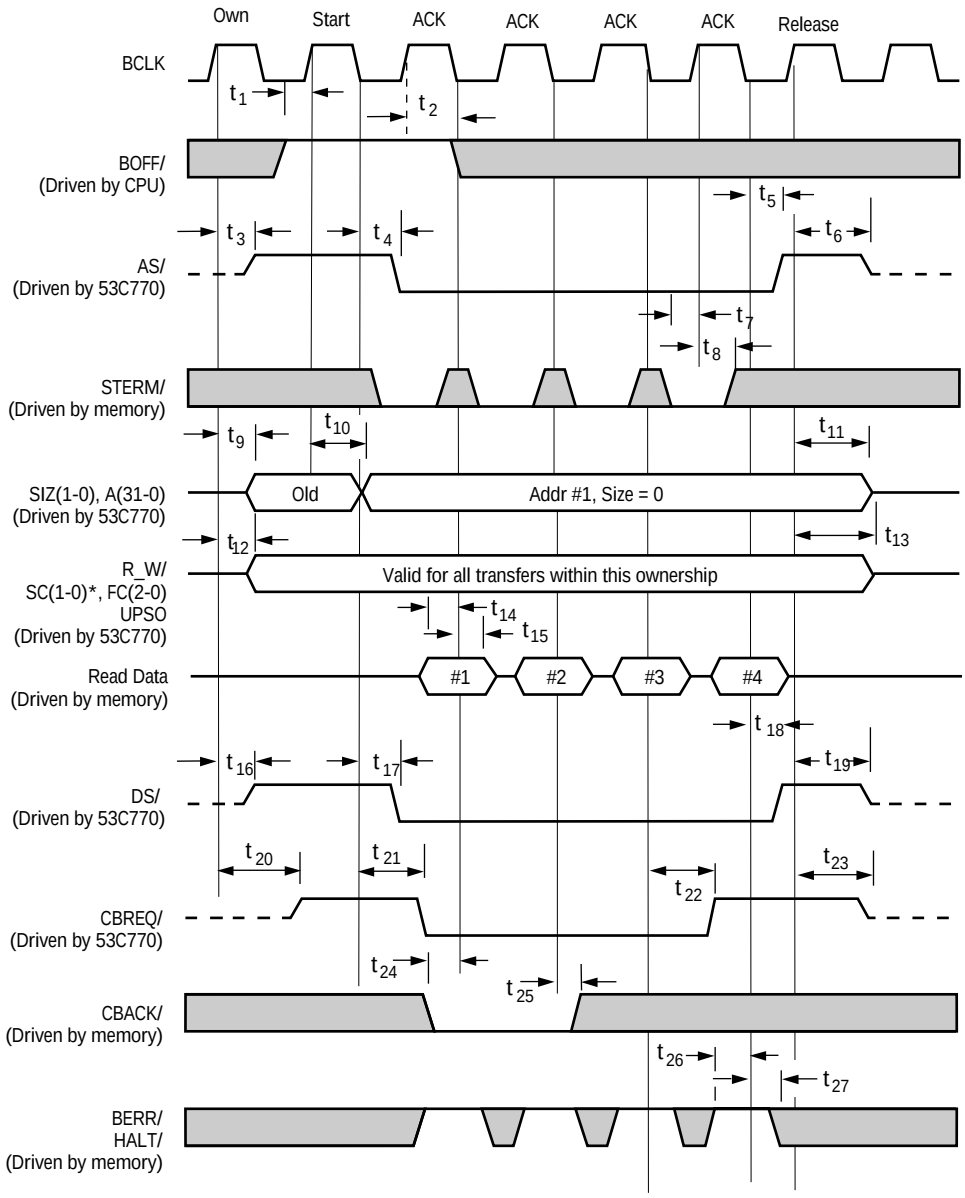
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** SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0*

Figure 6-13: Bus Mode 1 Bus Master Read (Cache Line Burst Requested but not Acknowledged)

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** SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0*

Figure 6-14: Bus Mode 1 Bus Master Read (Cache Line Burst)

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Table 6-20: Bus Mode 1 Master Read Timings

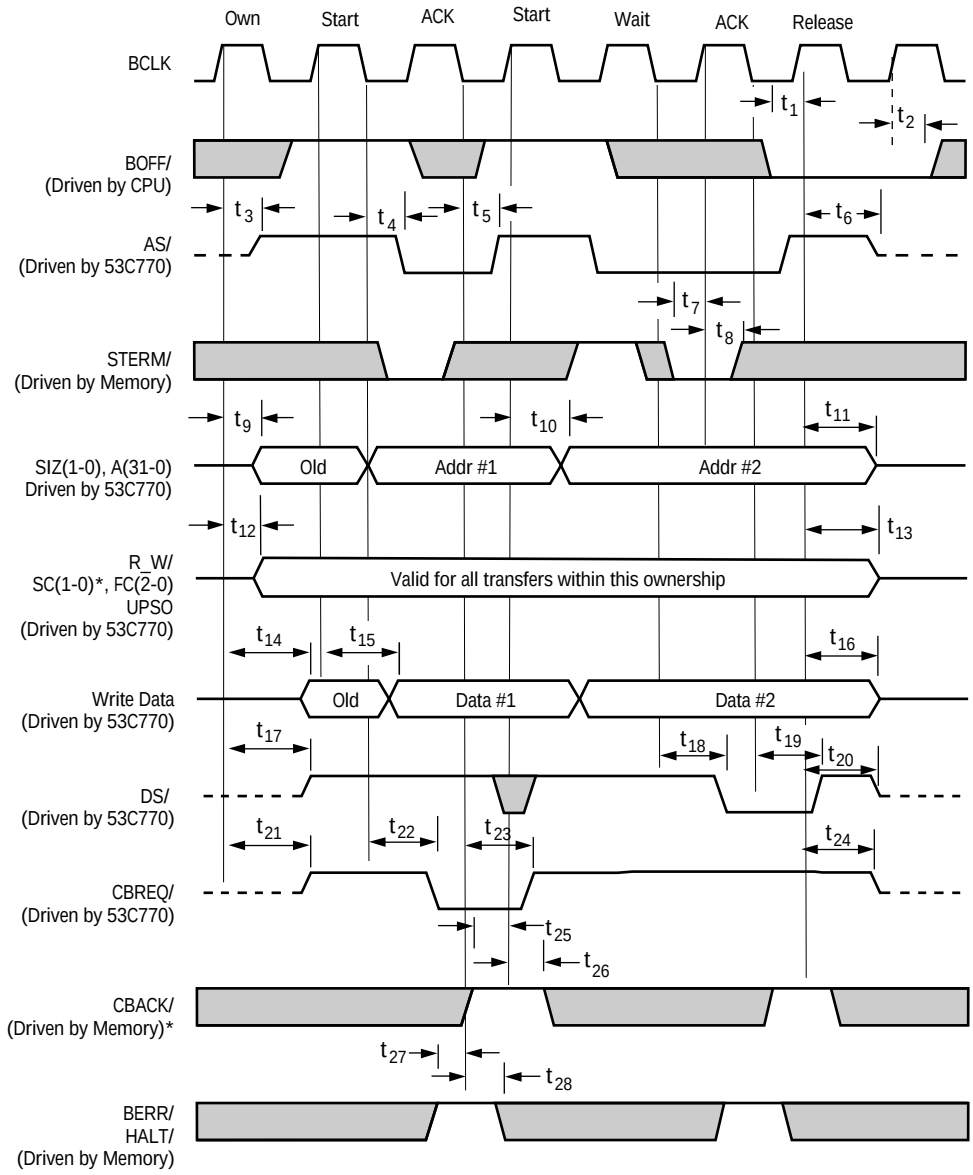
Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	32	ns
BCLK low to AS/ low	t_4	3	15	ns
BCLK low to AS/ high	t_5	3	15	ns
BCLK high to AS/ high-Z	t_6	7	34	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/ hold from BCLK high	t_8	7	-	ns
BCLK high to SIZ(1-0), A(31-0) driven	t_9	5	28	ns
BCLK high to SIZ (1-0), A(31-0) valid	t_{10}	4	20	ns
BCLK high to SIZ(1-0), A(31-0) high-Z	t_{11}	7	34	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO high-Z	t_{13}	6	30	ns
Read Data setup to BCLK low	t_{14}	4	-	ns
Read Data hold from BCLK low	t_{15}	6	-	ns
BCLK h igh to DS/ driven	t_{16}	5	28	ns
BCLK low to DS/ low	t_{17}	3	17	ns
BCLK low to DS/ high	t_{18}	3	17	ns
BCLK high to DS/ high-Z	t_{19}	7	32	ns
BCLK high to CBREQ/ driven	t_{20}	5	28	ns
BCLK low to CBREQ/ low	t_{21}	3	18	ns
BCLK low to CBREQ/ high	t_{22}	3	18	ns
BCLK high to CBREQ/ high-Z	t_{23}	7	32	ns
CBACK/ setup to BCLK low	t_{24}	8	-	ns
CBACK/ hold from BCLK low	t_{25}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{26}	6	-	ns
BERR/, HALT/ hold from BCLK low	t_{27}	4	-	ns

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Bus Mode 1 Bus Master Write Sequence

1. The SYM53C770 has attained bus mastership.
2. The SYM53C770 asserts the R_W/, Snoop Control, Function Control, and General Purpose lines
3. The SYM53C770 asserts the Address, Size, and Data lines
4. The SYM53C770 asserts Address Strobe and Cache Burst Request.
5. The SYM53C770 asserts Data Strobe.
6. The SYM53C770 waits for Synchronous Termination, Cache Burst Acknowledge, Bus Error, and Halt.
   - If Cache Burst Acknowledge is asserted, attempt bursting.Otherwise, proceed with non-cache transfers.
   - If Bus Error and Halt are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or Halt, and the SYM53C770 requires more cycles, then return to step 3.
7. Upon acknowledge of the last bus cycle, the SYM53C770 deasserts Master and Bus Grant Acknowledge
8. The SYM53C770 floats the Control, Address, and Data lines.

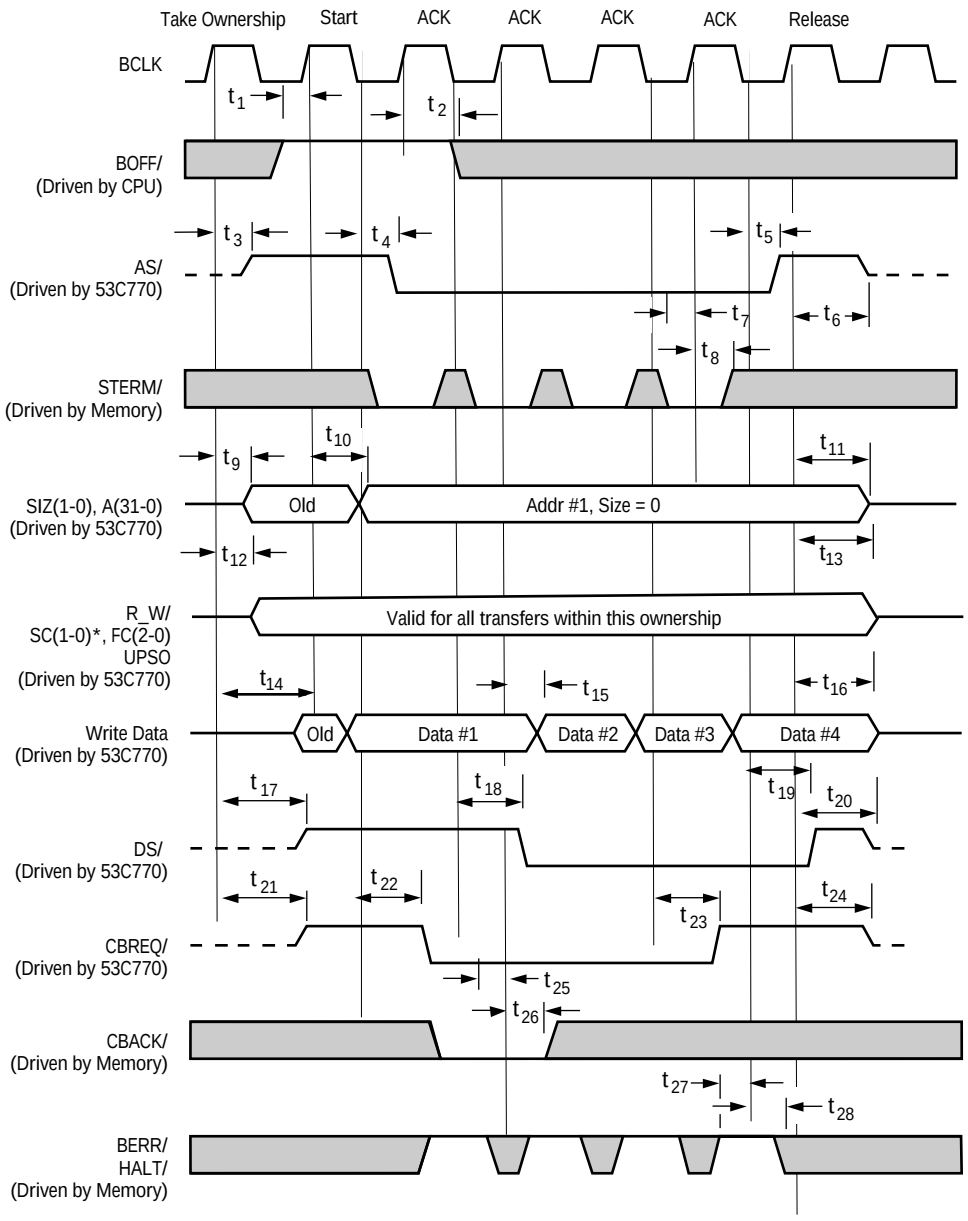
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**SC(1-0 timings apply only if Snoop Mode bit o of CTEST3 = 0*

Figure 6-15: Bus Mode 1 Bus Master Write (Cache Line Burst Requested but not Acknowledged)

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** SC(1-0) timings apply only if the Snoop Mode bit (CTEST3 bit 0) is clear.*

Figure 6-16: Bus Mode 1 Bus Master Write (Cache Line Burst)

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Table 6-21: Bus Mode 1 Master Write Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	32	ns
BCLK low to AS/ low	t_4	3	15	ns
BCLK low to AS/ high	t_5	3	15	ns
BCLK high to AS/ high-Z	t_6	7	34	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/ hold from BCLK high	t_8	7	-	ns
BCLK high to SIZ(1-0), A(31-0) driven	t_9	5	28	ns
BCLK high to SIZ(1-0), A(31-0), valid	t_{10}	4	20	ns
BCLK high to SIZ(1-0), A(31-0) high-Z	t_{11}	7	34	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO high-Z	t_{13}	6	30	ns
BCLK high to Write Data driven	t_{14}	6	34	ns
BCLK high to Write Data valid	t_{15}	6	24	ns
BCLK high to Write Data high-Z	t_{16}	6	32	ns
BCLK high to DS/ driven	t_{17}	5	32	ns
BCLK low to DS/ low	t_{18}	3	17	ns
BCLK low to DS/ high	t_{19}	3	17	ns
BCLK high to DS/ high-Z	t_{20}	7	34	ns
BCLK high to CBREQ/ driven	t_{21}	5	30	ns
BCLK low to CBREQ/ low	t_{22}	3	18	ns
BCLK low to CBREQ/ high	t_{23}	3	18	ns
BCLK high to CBREQ/ high-Z	t_{24}	7	32	ns
CBACK/ setup to BCLK high	t_{25}	8	-	ns
CBACK/ hold from BCLK high	t_{26}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{27}	6	-	ns
BERR/, HALT hold from BCLK low	t_{28}	4	-	ns

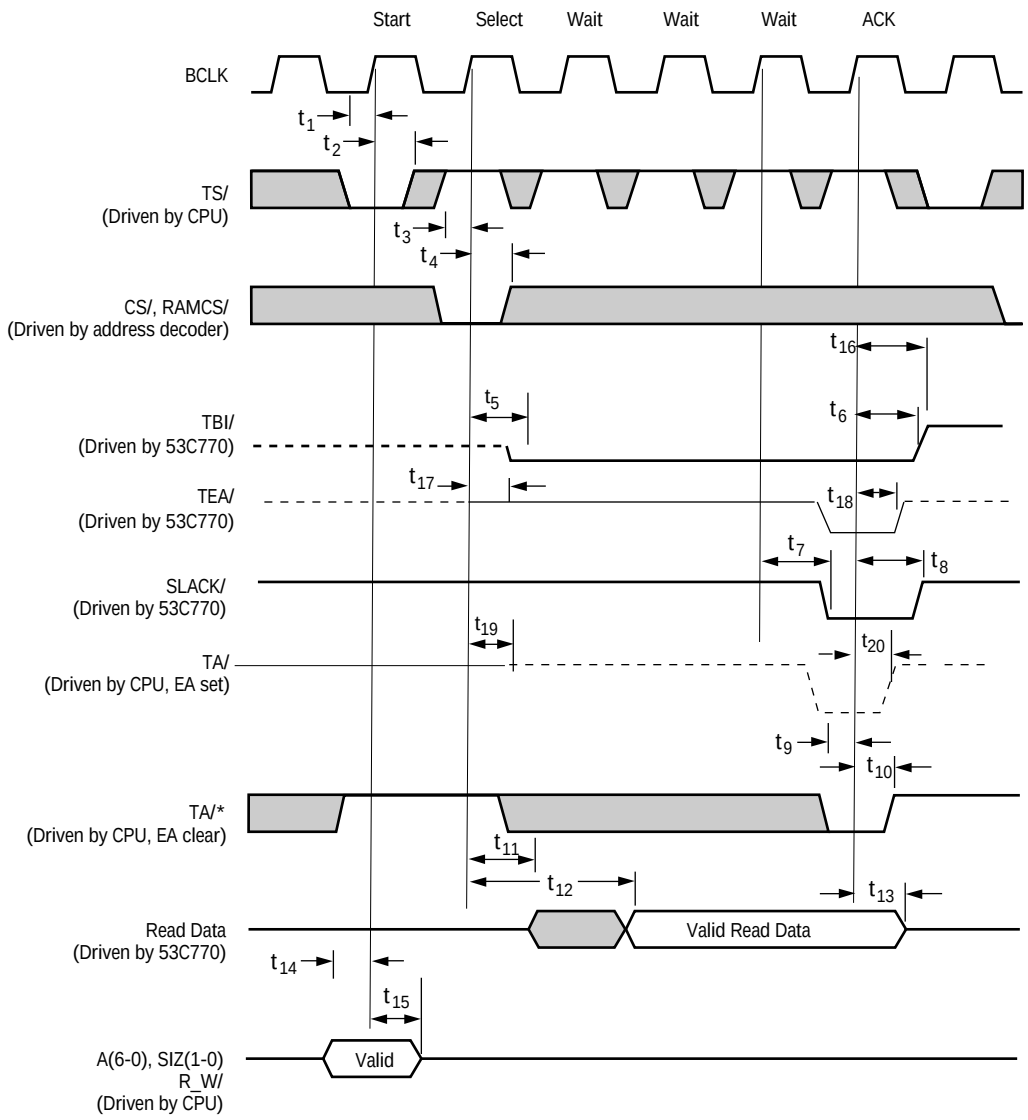
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Bus Mode 2 Slave Cycle

Bus Mode 2 Slave Read Sequence

1. R_W/, Address, Transfer Start, and the Size lines are asserted by the CPU.
2. Chip Select is validated by the SYM53C770 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Transfer Start is deasserted by the CPU.
5. Three clock cycles of wait state are inserted (these wait states are required) and the data lines are asserted.
6. Slave Acknowledge is asserted by the SYM53C770, if no errors are detected.
7. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
8. Slave Acknowledge or Transfer Error Acknowledge is deasserted.
9. The SYM53C770 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no errors are detected.
10. The data lines are tristated by the SYM53C770.

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** This signal may be driven by the SYM53C770 if the Enable Ack bit is set (DCNTL bit 5). See the explanation in Chapter 2 of this manual for use of this signal as an output.*

Note: The 53C770 must see transfer starts (TS/) paired up with transfer acknowledges, (TA/) even though the slave cycle may not be intended for the 53C770.

Figure 6-17: Bus Mode 2 Slave Read Waveforms

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Table 6-22: Bus Mode 2 Slave Read Timings

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	20	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	-	75	ns
BCLK high to data bus high-Z	t_{13}	7	34	ns
A(6-0), SIZ(1-0), R_W/ setup to BCLK high	t_{14}	4	-	ns
A(6-0), SIZ(1-0), R_W/ hold from BCLK high	t_{15}	12	-	ns
BCLK high to TBI/ high-Z	t_{16}	8	32	ns
BCLK high to TEA/ driven	t_{17}	8	27	ns
BCLK high to TEA/ high-Z	t_{18}	9	34	ns
BCLK high to TA/ driven	t_{19}	8	27	ns
BCLK high to TA/ high-Z	t_{20}	9	33	ns

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Bus Mode 2 Slave Write Sequence

1. R_W/, Address, Transfer Start, and the Size Lines are asserted by the CPU.
2. Chip Select is validated by the SYM53C770 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Transfer Start is deasserted by the CPU.
5. The data lines are asserted by the CPU.
6. Three clock cycles of wait state are inserted (these wait states are required).
7. Slave Acknowledge is asserted by the SYM53C770, if no errors are detected.
8. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
9. The SYM53C770 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if there are no errors.
10. Slave Acknowledge or Transfer Error Acknowledge is deasserted.

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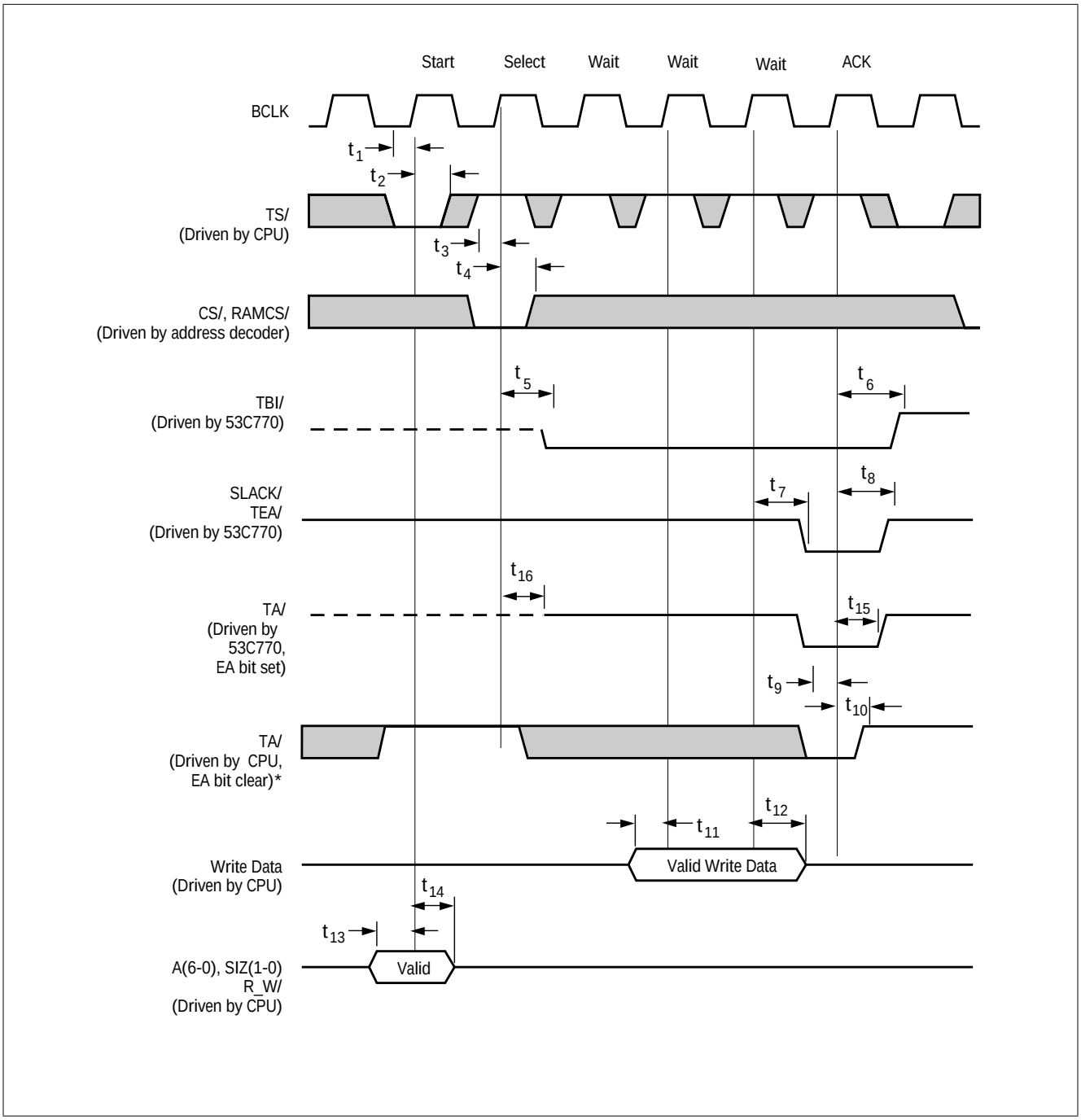


Figure 6-18: Bus Mode 2 Slave Write Waveforms

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Table 6-23: Bus Mode 2 Slave Write Timings

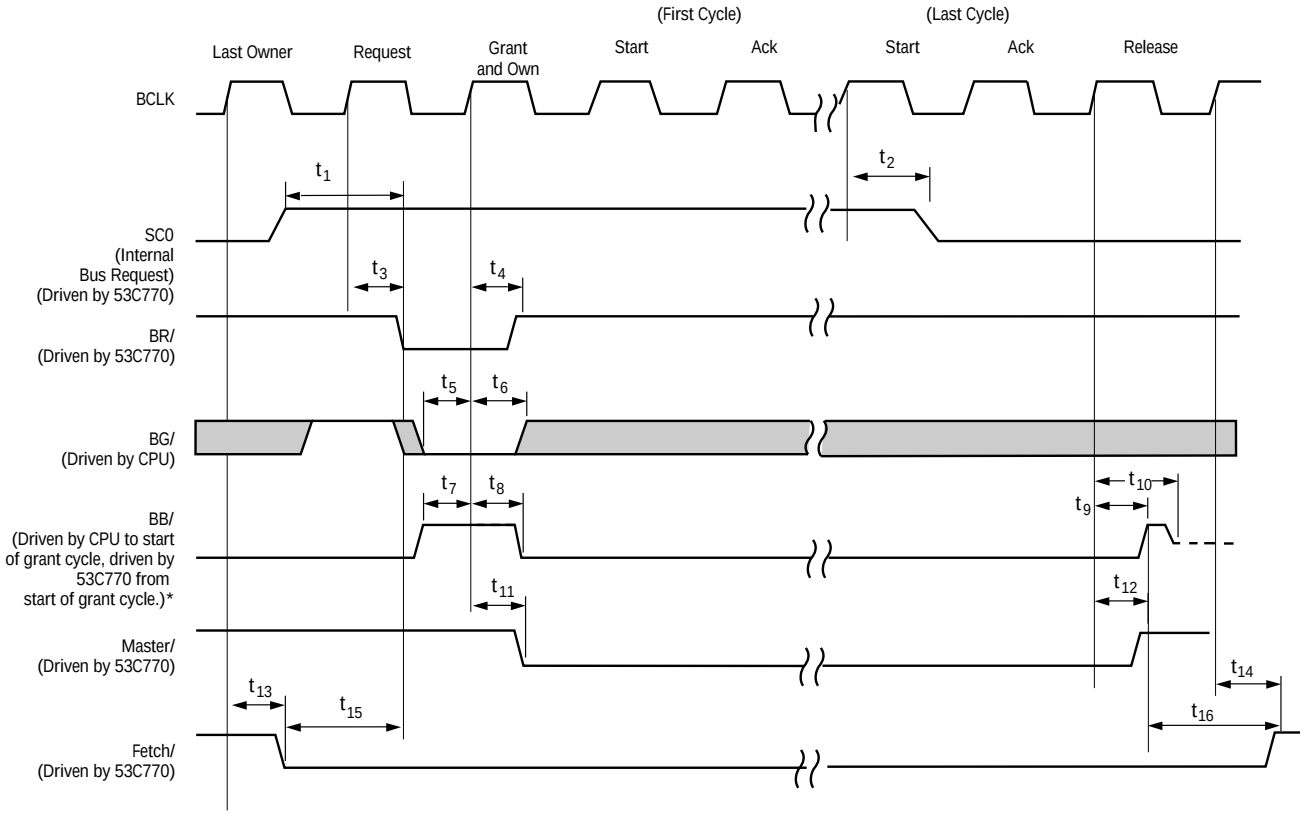
Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	20	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
Valid write data setup to BCLK high	t_{11}	6	-	ns
Valid write data hold from BCLK high	t_{12}	14	-	ns
A(6-0), SIZ(1-0), R_W/ setup to BCLK high	t_{13}	4	-	ns
A(6-0), SIZ(1-0), R_W/ hold from BCLK high	t_{14}	12	-	ns
BCLK high to TA/ driven	t_{15}	8	27	ns
BCLK high to TA/ high-Z	t_{16}	9	33	ns

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Bus Mode 2 Host Bus Arbitration

Bus Mode 2 Bus Arbitration Sequence

1. The SYM53C770 internally determines bus mastership is required. FETCH/ is asserted during cycles in which the SYM53C770 is retrieving new SCRIPTS instructions.
2. Bus Request is asserted.
3. The SYM53C770 waits for BG/ and checks that BB/ is deasserted. Then the SYM53C770 asserts BB/ and MASTER/, and deasserts BR/.



** If the Fast Arbitration bit is set (DCNTL bit 1), the SYM53C770 will drive the Bus Grant Acknowledge signal as soon as it receives a bus grant. One clock cycle of arbitration will be saved.*

Note: the SYM53C770 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access—it deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will next generate an interrupt which the system may service.

Figure 6-19: Bus Mode 2 Host Bus Arbitration

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Table 6-24: Bus Mode 2 Host Bus Arbitration Timings

Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after BR/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	24	ns
BCLK high to BB/ high	t_9	3	19	ns
BCLK high to BB/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

**When Snoop Mode bit of CTEST3 is set to 1.*

***During a retry operation, FETCH/ will remain low until successful completion of an op code fetch or a fatal bus error.*

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Bus Mode 2 Fast Arbitration

Bus Mode 2 Fast Arbitration Sequence*

1. The SYM53C770 determines bus mastership is required. FETCH/ is asserted during cycles in which the SYM53C770 is retrieving new SCRIPTS instructions.
2. Bus request is asserted
3. The SYM53C770 waits for Bus Grant. The SYM53C770 becomes bus master asynchronously on the leading edge of BG/. Then the SYM53C770 asynchronously asserts Bus Busy and Master, and deasserts Bus Request.
4. The SYM53C770 issues a start cycle on the next rising edge of BCLK.

** Fast Arbitration bit must be set.*

Note: in fast arbitration mode, the SYM53C770 will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BB/.

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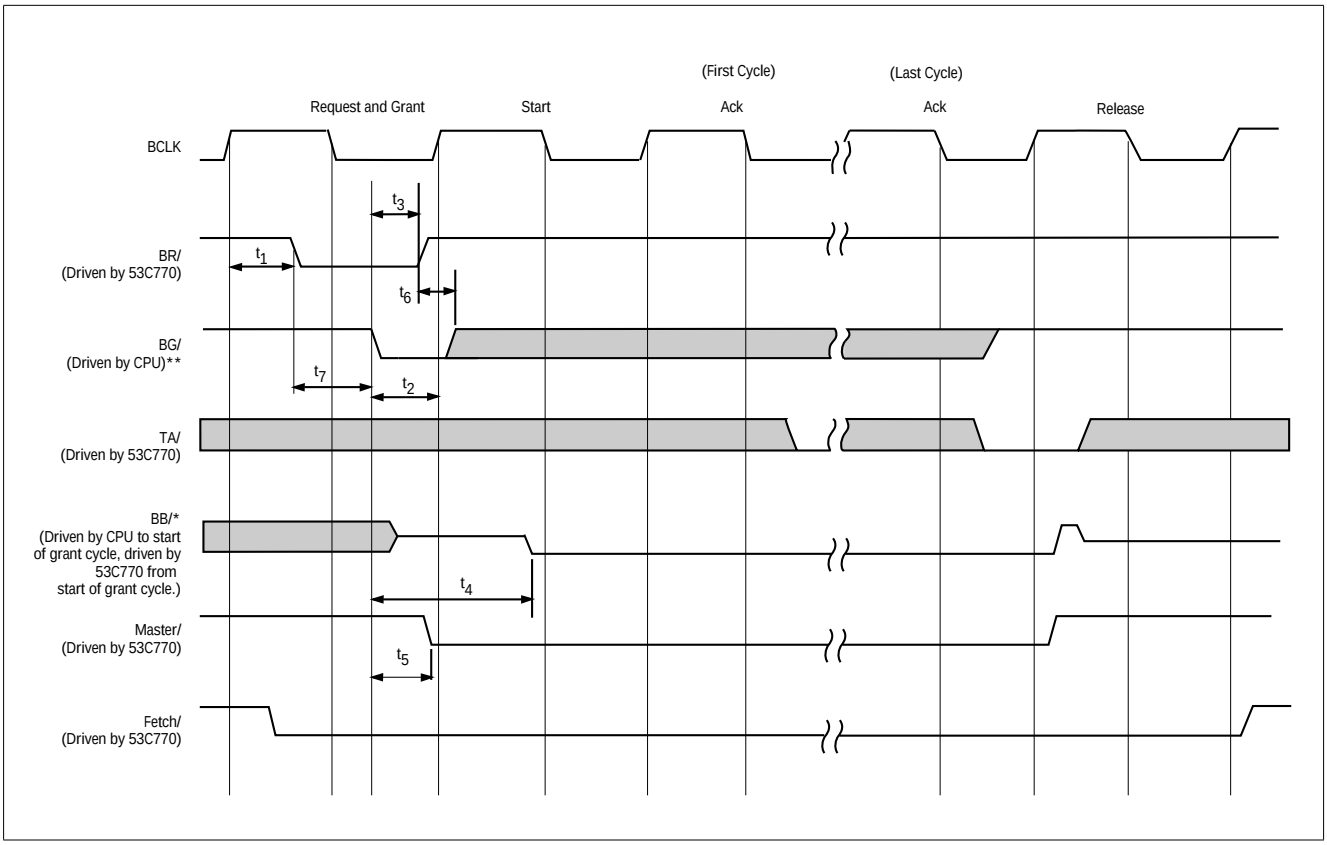


Figure 6-20: Bus Mode 2 Fast Arbitration

Table 6-25: Bus Mode 2 Fast Arbitration Timings

Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	20	ns
BG/ setup to BCLK high	t_2	12	-	ns
BG/ asserted to BR/ deasserted	t_3	-	22	ns
BG/ asserted to BB/ asserted	t_4	-	20	ns
BG/ asserted to MASTER/ asserted	t_5	-	16	ns
BG/ hold after BR/ deasserted	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns

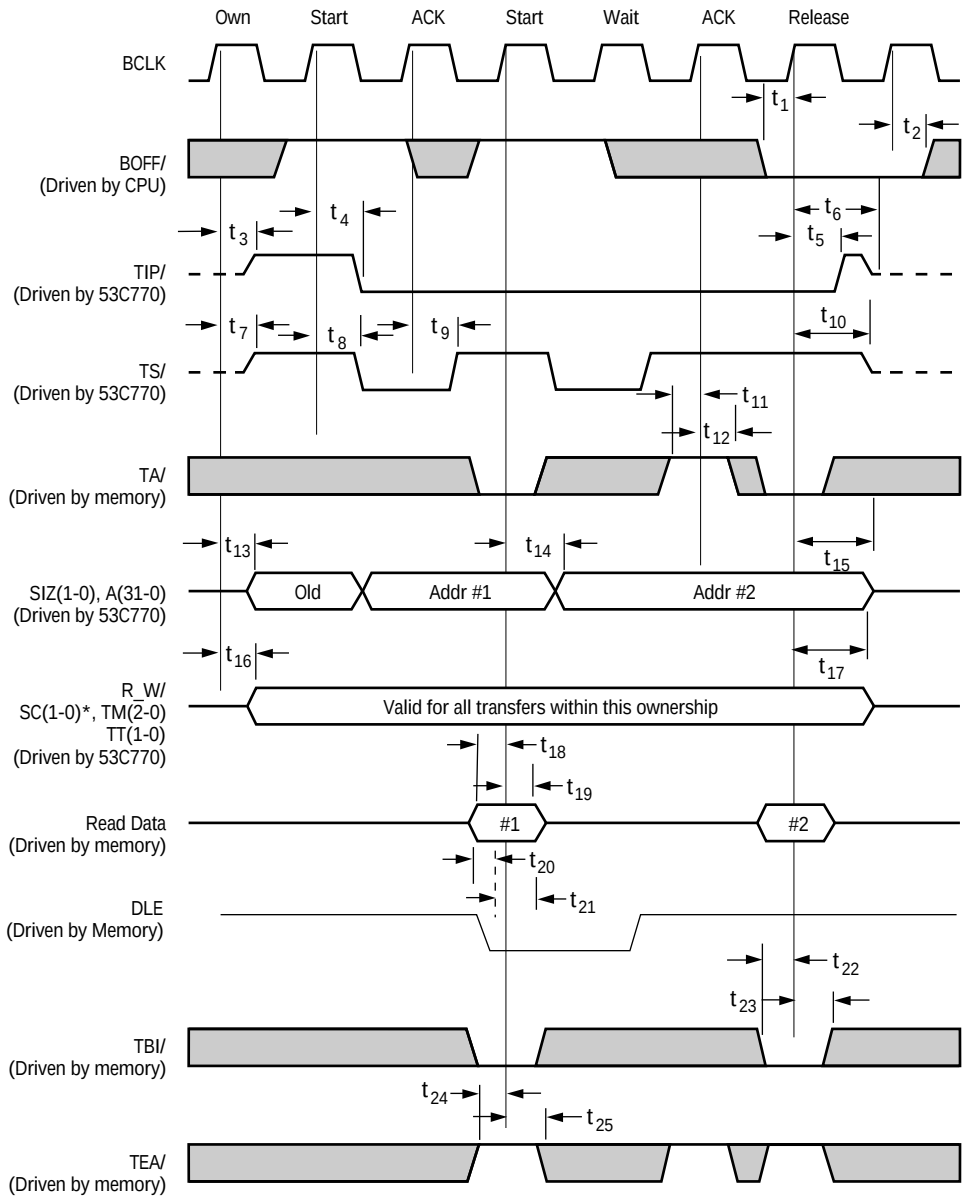
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Bus Mode 2 Master Cycle

Bus Mode 2 Master Read Sequence

1. The SYM53C770 has attained bus mastership.
2. The SYM53C770 asserts the R_W/, Snoop Control, Transfer Modifier, and Transfer Type lines.
3.
   a. The SYM53C770 asserts Transfer in Progress.
   b. The SYM53C770 asserts Transfer Start, Address, and Size lines.
4. The SYM53C770 deasserts Transfer Start.
5. The SYM53C770 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the SYM53C770 requires more cycles, then return to step 3b.
6. Upon acknowledge of the last bus cycle, the SYM53C770 deasserts Master, Bus Busy, and Transfer in Progress.
7. The SYM53C770 floats the Control and Address lines.

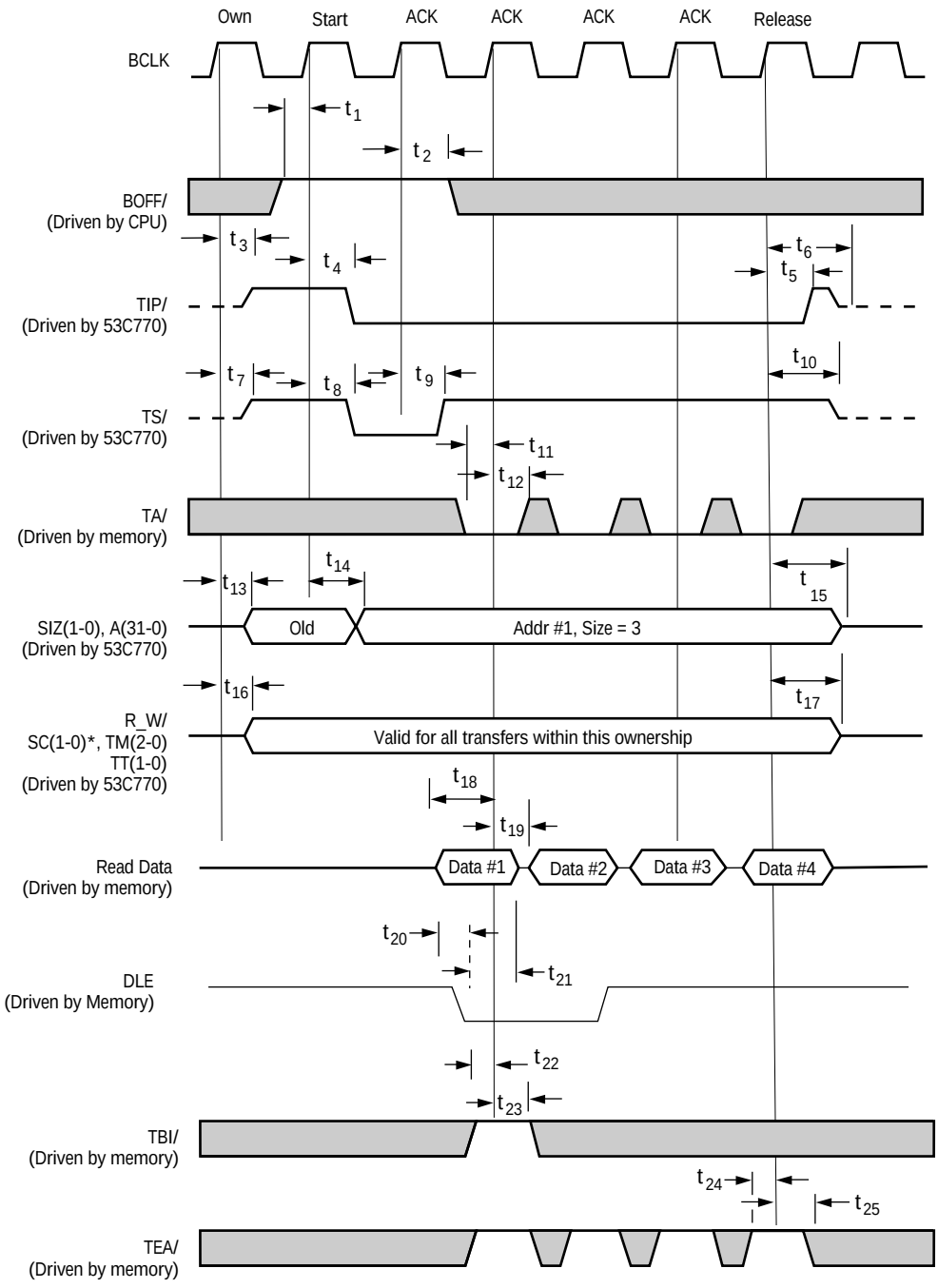
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SC(1-0) timings apply only if Snoop Mode bit, bit 0 of CTEST3 = 0

Figure 6-21: Bus Mode 2 Bus Master Read (Cache Line Burst Requested but not Acknowledged)

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SC(1-0) timings apply only if the Snoop Mode bit (bit 0 of CTEST0) is zero.

Figure 6-22: Bus Mode 2 Bus Master Read (Cache Line Burst)

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Table 6-26: Bus Mode 2 Bus Master Read Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	30	ns
BCLK high to TS/ low	t_8	3	17	ns
BCLK high to TS/ high	t_9	4	17	ns
BCLK high to TS/ high-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	5	20	ns
BCLK high to A(31-0), SIZ(1-0)	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) high-Z	t_{17}	-	32	ns
Read Data setup to BCLK high	t_{18}	6	-	ns
Read data hold from BCLK high	t_{19}	6	-	ns
Read data setup to DLE low	t_{20}	4	-	ns
Read data hold from DLE low	t_{21}	6	-	ns
TBI/ setup to BCLK high	t_{22}	6	-	ns
TBI/ hold from BCLK high	t_{23}	4	-	ns
TEA/ setup to BCLK high	t_{24}	9	-	ns
TEA/ hold from BCLK high	t_{25}	5	-	ns

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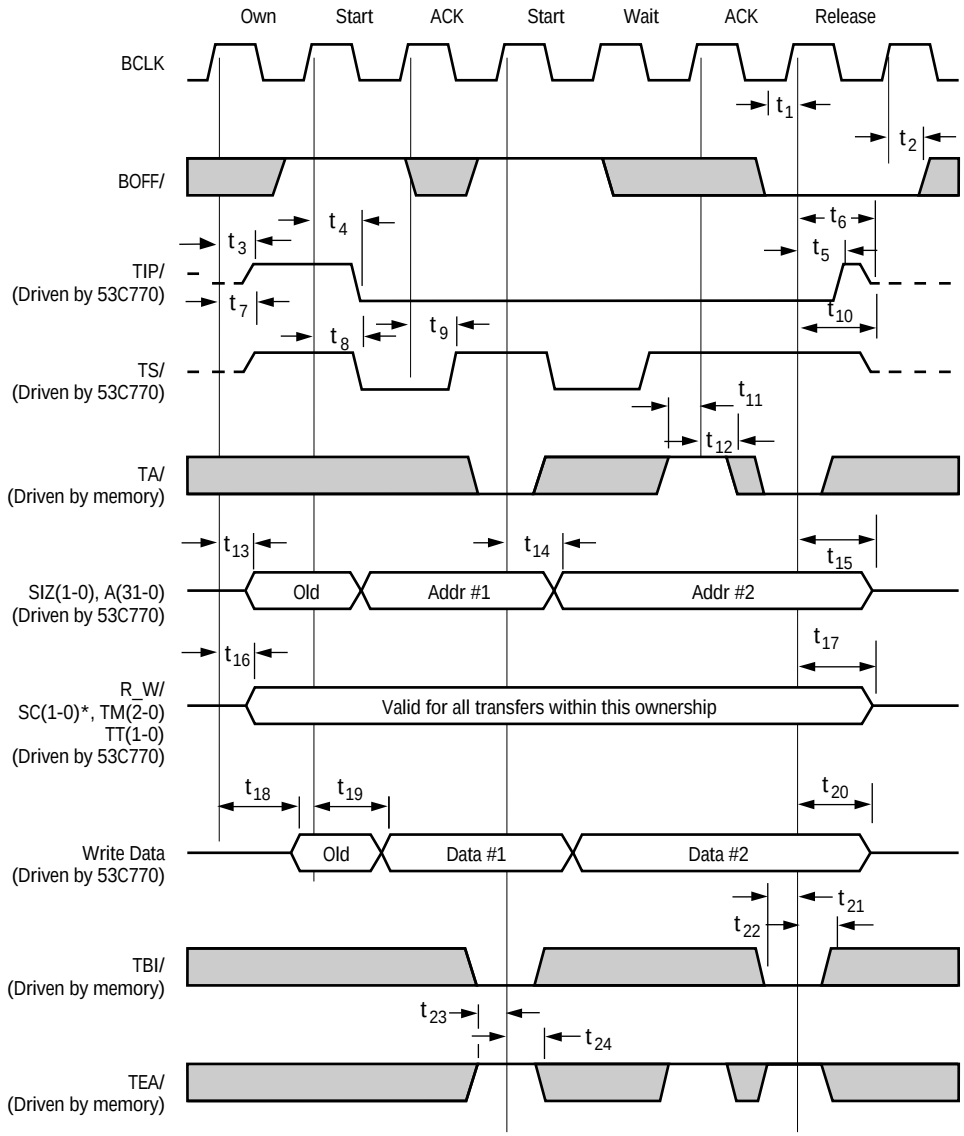
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Bus Mode 2
Bus Master Write Sequence

1. The SYM53C770 has attained bus mastership.
2. The SYM53C770 asserts the R_W/, Snoop Control, Transfer Modifier, and Transfer Type Lines.
3.
   a. The SYM53C770 asserts Transfer in Progress
   b. The SYM53C770 asserts Transfer Start, Address, Size lines, and Data lines.
4. The SYM53C770 deasserts Transfer Start.
5. The SYM53C770 waits for Transfer Acknowledge, Transfer Burst Inhibit, and Transfer Error Acknowledge
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the SYM53C770 requires more cycles, then return to step 3b.
6. Upon acknowledge of the last bus cycle, the SYM53C770 deasserts Master, Busy, and Transfer in Progress.
7. The SYM53C770 floats the Control, Address, and Data lines.

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**SC(1-0) timings apply only if the Snoop Mode bit (bit 0 of CTEST3) is zero.*

Figure 6-23: Bus Mode 2 Bus Master Write (Cache Line Burst Requested but not Acknowledged)

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Table 6-27: Bus Mode 2 Bus Master Write Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	30	ns
BCLK high to TS/ low	t_8	3	17	ns
BCLK high to TS/ high	t_9	3	17	ns
BCLK high to TS/ high-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	30	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-0), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to write data driven	t_{18}	5	34	ns
BCLK high to write data valid	t_{19}	7	24	ns
BCLK high to Write data high-Z	t_{20}	5	30	ns
TBI/ setup to BCLK high	t_{21}	6	-	ns
TBI/ hold from BCLK high	t_{22}	4	-	ns
TEA/ setup to BCLK high	t_{23}	9	-	ns
TEA/ hold from BCLK high	t_{24}	5	-	ns

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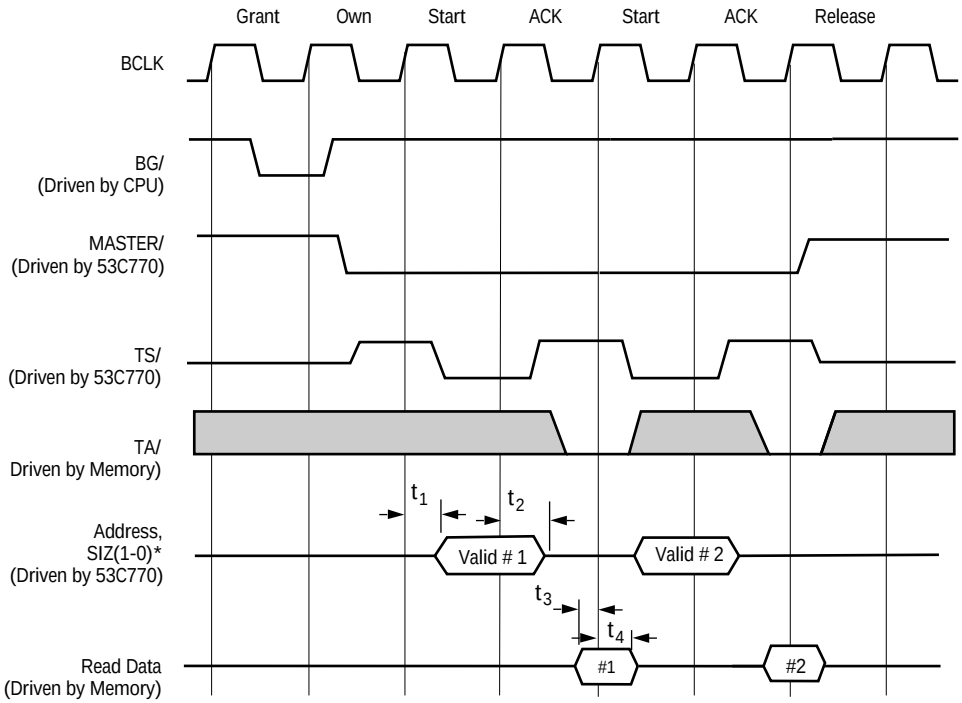
Bus Mode 2 Mux Mode Cycle

Mux Mode Read Sequence

1. The SYM53C770 has attained bus mastership
2. The SYM53C770 asserts the R_W/, Snoop Control, Function Control, and Transfer Type lines.
3.
   a. The SYM53C770 asserts Transfer in Progress.
   b. The SYM53C770 asserts the Transfer Start, Address, and Size lines.
4. The SYM53C770 deasserts Transfer Start and floats the address lines.
5. The SYM53C770 waits for transfer acknowledge, Valid Data driven on the data pins, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the SYM53C770 requires more cycles, then return to step 3b.
6. The SYM53C770 deasserts the control lines.
7. Upon acknowledgment of the last bus cycle, the SYM53C770 deasserts Master and Bus Grant Acknowledge.

Note: this mode of operation expects D(31-0) to be physically tied to A(31-0), respectively.

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** For cache line bursting, the value of the SIZ(1-0) bits must be 03h*

Figure 6-24: Mux Mode Read Cycle (Cache Line Burst Requested but not Acknowledged)

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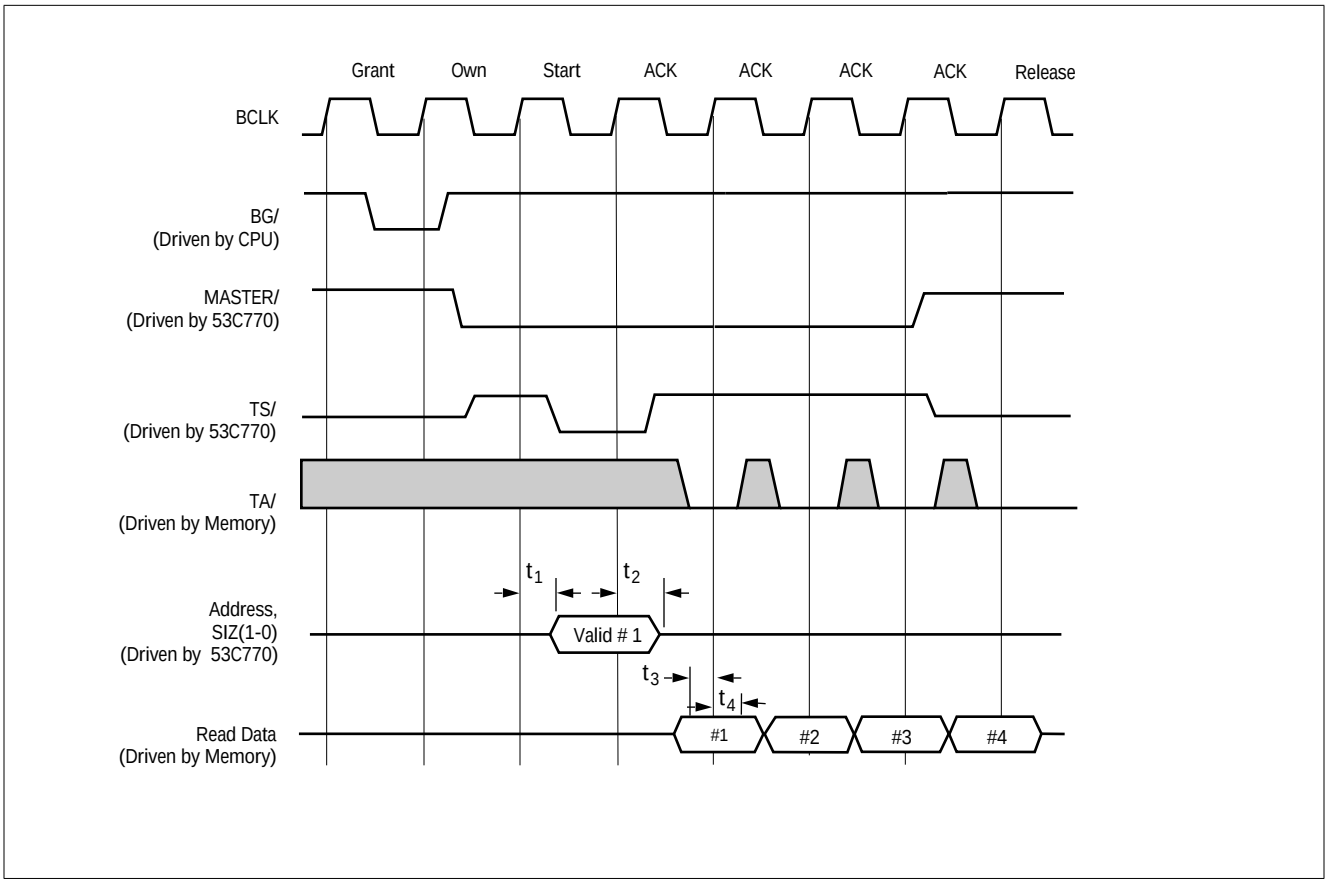


Figure 6-25: Mux Mode Read Cycle (Cache Line Burst)

Table 6-28: Bus Mode 2 Mux Mode Read Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Address driven	t_1	5	22	ns
BCLK high to Address high-Z	t_2	-	23	ns
Read Data setup to BCLK high	t_3	5	-	ns
Read data hold from BCLK high	t_4	6	-	ns

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Mux Mode Write Sequence

1. The SYM53C770 has attained bus mastership.
2. The SYM53C770 asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.
3.
   a. The SYM53C770 asserts Transfer in Progress.
   b. The SYM53C770 asserts Transfer Start, Address, Size lines, and floats the Data lines.
4. The SYM53C770 deasserts Transfer Start, floats the address bus, and asserts the data bus.
5. The SYM53C770 waits for Transfer Acknowledge, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted, Transfer Error Acknowledge is not asserted, and the SYM53C770 requires more cycles, return to step 3b.
6. The SYM53C770 deasserts the Control and Data lines.
7. Upon acknowledge of the last bus cycle, the SYM53C770 deasserts Master and Bus Grant Acknowledge.

Note: This mode of operation expects D(31-0) to be physically tied to A(31-0), respectively.

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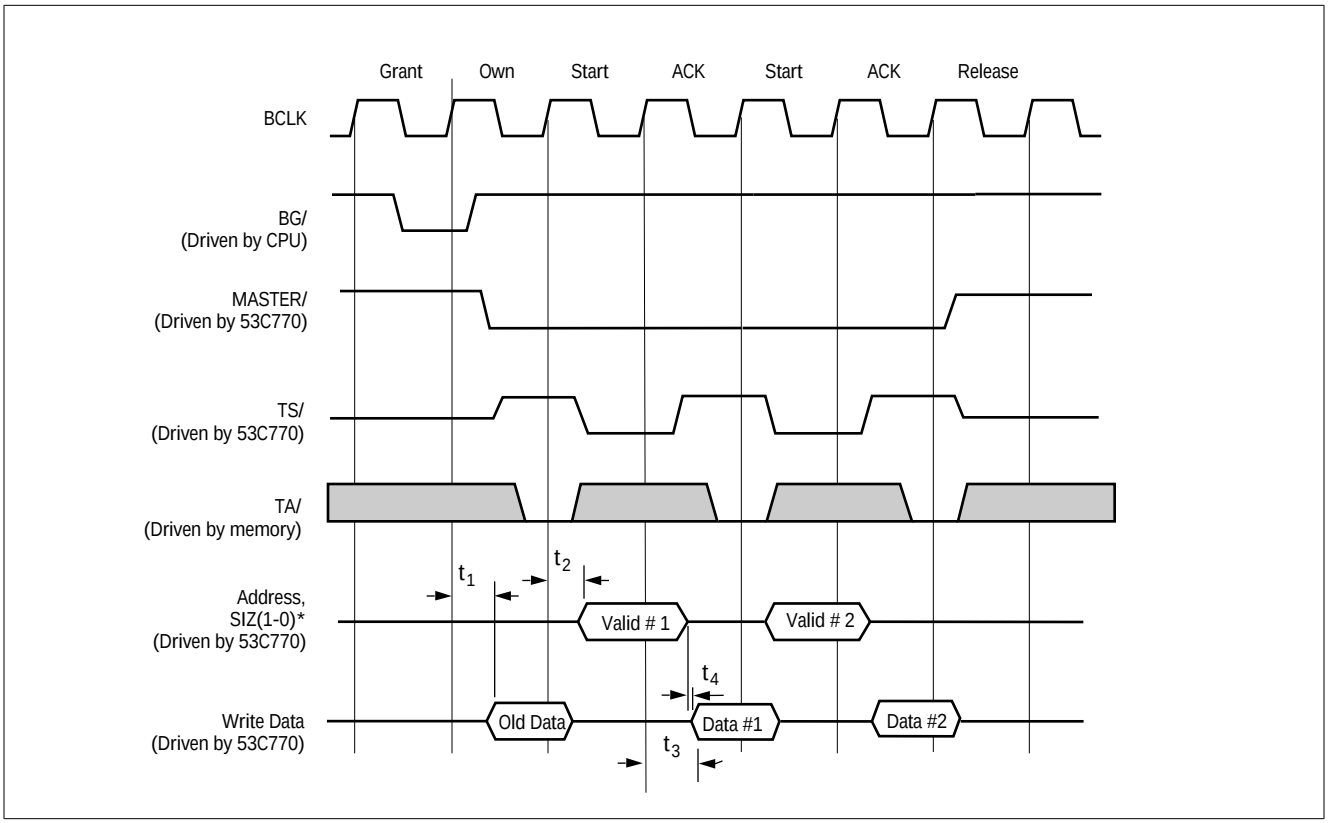


Figure 6-26: Mux Mode Write Cycle (Non-Cache Line Burst)

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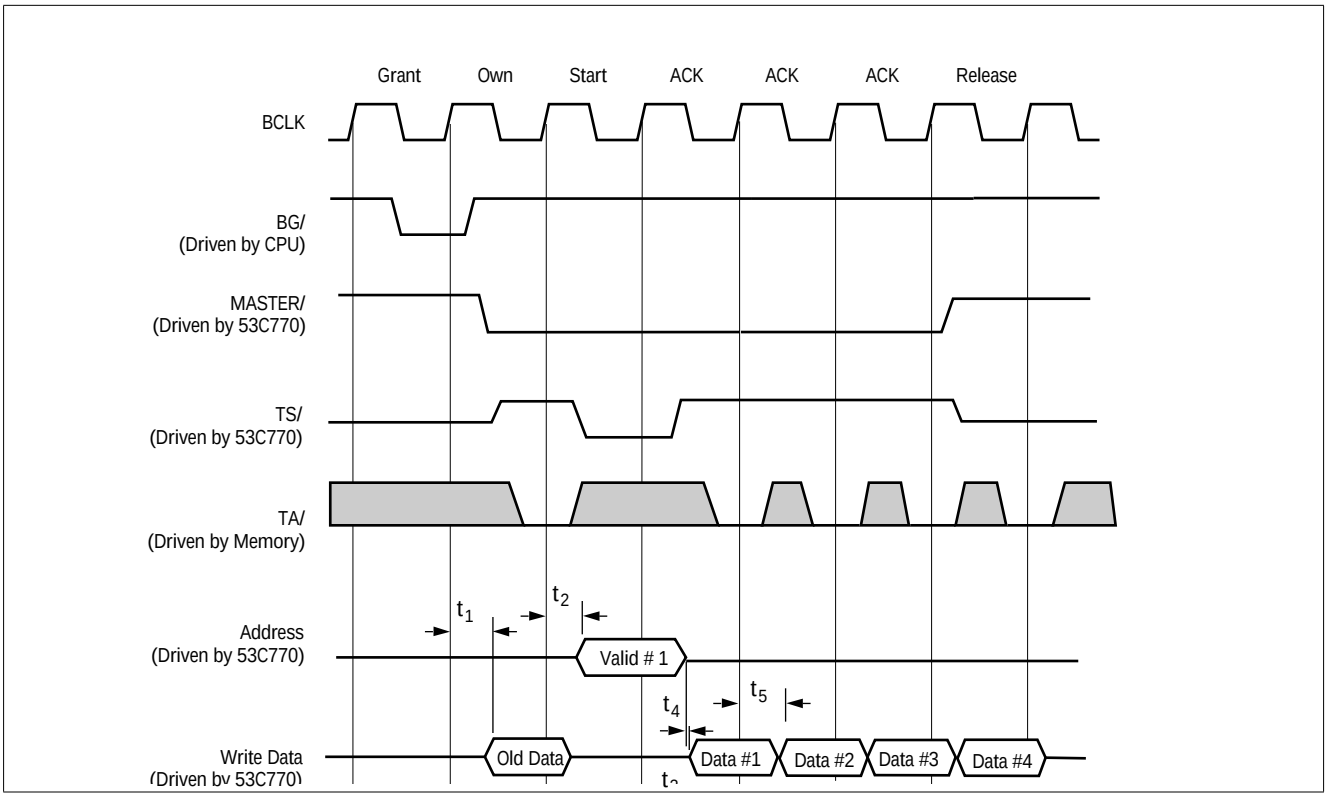


Figure 6-27: Mux Mode Write Cycle (Cache Line Burst)

Table 6-29: Bus Mode 2 Mux Mode Write Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Old Data driven	t_1	-	34	ns
BCLK high to Address driven	t_2	5	22	ns
BCLK high to New Data driven	t_3	8	24	ns
Write data High-Z to driven switching time	t_4	1	-	ns
BCLK high to Next Data	t_5	-	24	ns

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Bus Mode 3 and 4 Slave Cycle

Bus Mode 3 and 4 Slave Read Sequence

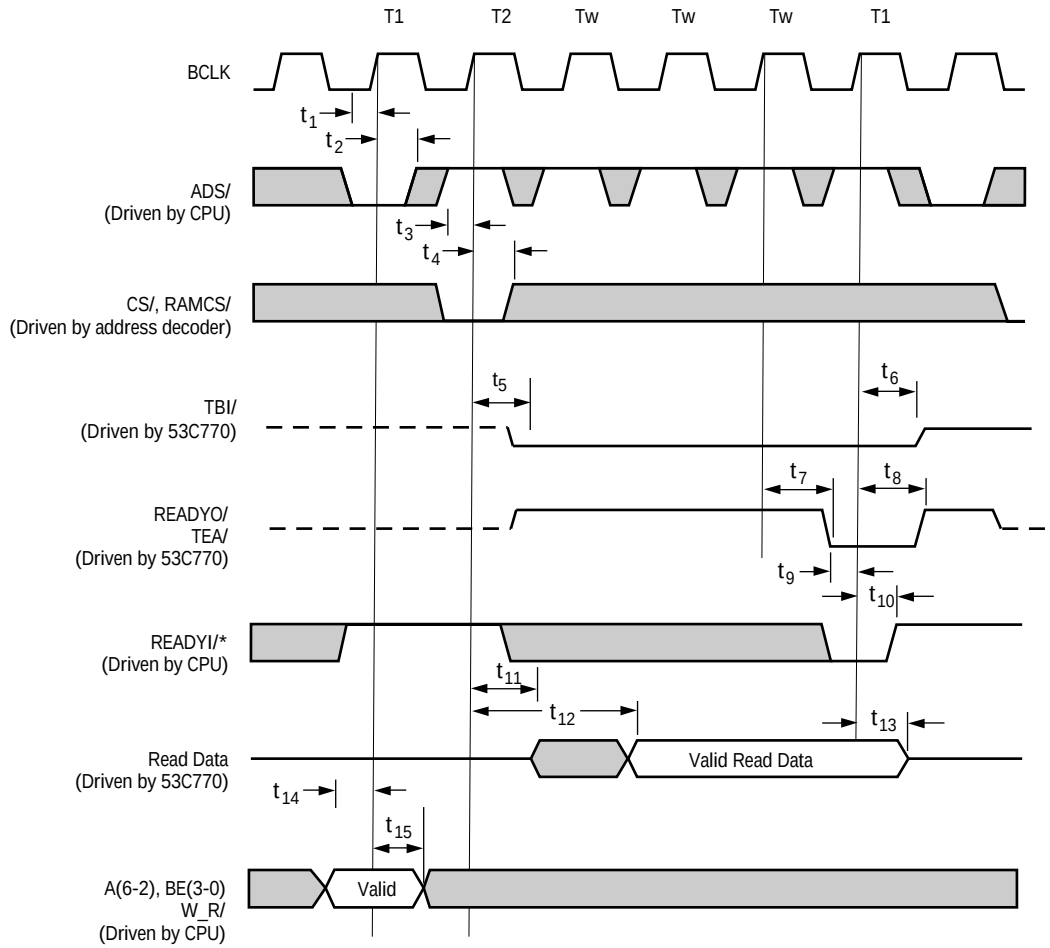
1. Address, Address Status, Read, and the Byte Enable signals are asserted by the CPU.[1]
2. Chip Select is validated by the SYM53C770 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Address Status may be deasserted by the CPU.
5. Three clock cycles of wait state are inserted (these wait states are required) and the Data lines are asserted.
6. Ready Out is asserted by SYM53C770, if no errors are detected.
7. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
8. Ready Out or Transfer Error Acknowledge is deasserted.
9. The SYM53C770 waits for Ready In to be asserted and then ends the slave cycle, if no errors are detected.
10. The Data lines are tristated by the SYM53C770.

Recommended Setup for Bus Mode 3 and 4

1. Disable Cache Line Burst Mode (if cache line is not supported; set CTEST0, bit 7).
2. Set the Bus Mode bit (DCNTL, bit 6).
3. Set the Snoop Mode bit (CTEST3, bit0).
4. Tie BB/ high resistively.
5. Tie TEA/ high resistively.

[1] The waveforms in this section show the address/byte enable signals for Bus Mode 4, A(31-2), BE(3-0). These waveforms also apply to the Bus Mode 3 Address/byte enable lines, A(31-0), BHE/.

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** This signal may be driven by the SYM53C770 if the Enable Acknowledge bit is set (DCNTL bit 5). See the explanation in Chapter 2 of this manual for use of this signal as an output.*

Figure 6-28: Bus Mode 3 and 4 Slave Read Cycle

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Table 6-30: Bus Mode 3 and 4 Slave Read Timings

Parameter	Symbol	Min	Max	Units
ADS/ setup to BCLK high	t_1	4	-	ns
ADS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after ADS/	t_3	5	-	ns
CS/ hold from BCLK high after ADS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to READYO/, TEA/ low	t_7	5	20	ns
BCLK high to READYO/, TEA/ high	t_8	4	20	ns
READYI/ setup to BCLK high during or after READYO/, TEA/	t_9	9	-	ns
READYI/ hold from BCLK high during or after READYO/, TEA/	t_{10}	5	-	ns
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	-	75	ns
BCLK high to data bus high-Z	t_{13}	7	34	ns
A(6-2), BE(3-0), W_R/ setup to BCLK high[1]	t_{14}	4	-	ns
A(2-6), (3-0)				
A(6-2), BE(3-0), W_R/ hold from BCLK high[2]	t_{15}	12	-	ns

1. The waveforms in these sections show the address/byte enable signals for Bus Mode 4, A(31-2), BE(3-0). These waveforms also apply to the bus Mode 3 address/byte enable lines, A(31-0), BHE/.

2. See note 1 above.

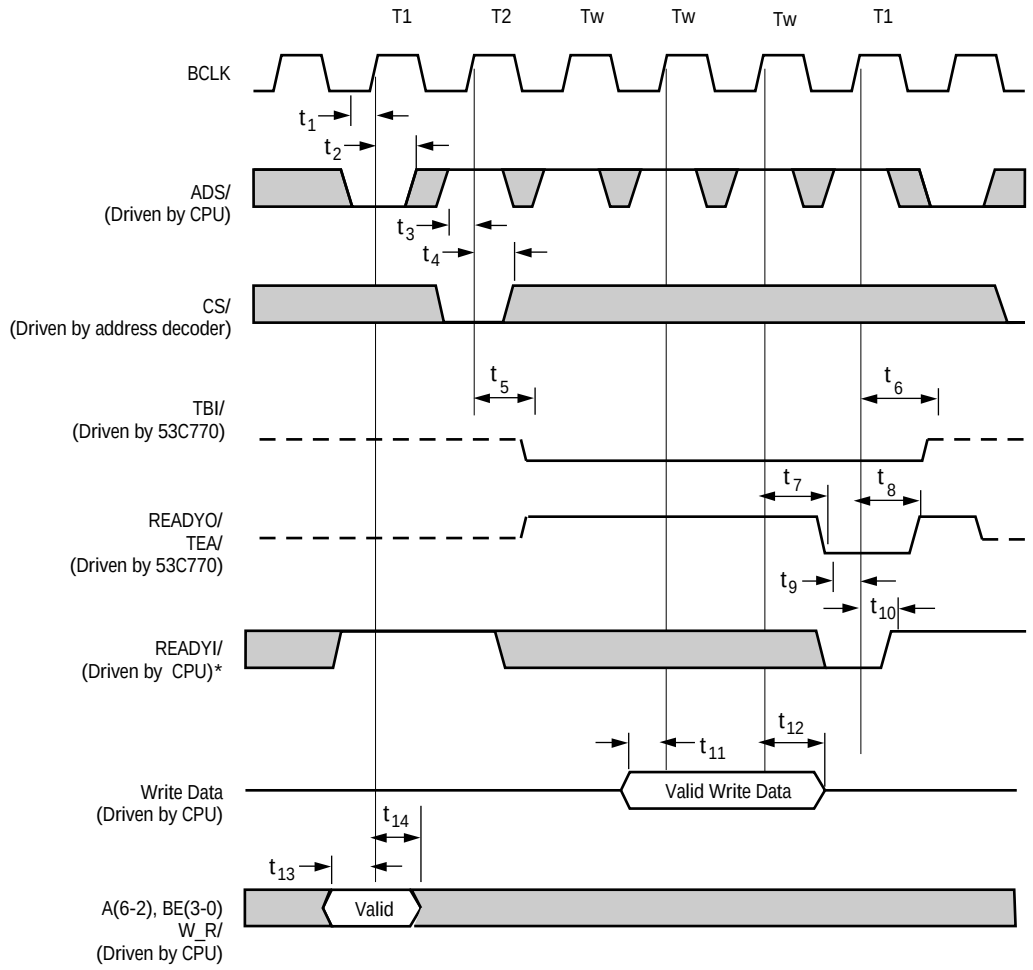
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Bus Mode 3 and 4 Slave Write Sequence

1. W_R/, the address lines, and the Address Status and Byte Enable signals are asserted by the CPU.[1]
2. Chip Select is validated by the SYM53C770 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Address Status may be deasserted by the CPU.
5. The data lines are asserted by the CPU.
6. Three clock cycles of wait state are inserted (these wait states are required).
7. Ready Out is asserted by the SYM53C770, if no errors are detected.
8. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
9. Ready Out or Transfer Error Acknowledge is deasserted.
10. The SYM53C770 waits for Ready In to be asserted and then ends the slave cycle, if there are no errors.

[1] The waveforms in this section show the address/byte enable signals for Bus Mode 4, A(31-2), BE(3-0). These waveforms also apply to the Bus Mode 3 Address/byte enable lines, A(31-0), BHE/.

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**This signal may be driven by the SYM53C770 if the Enable Acknowledge bit (DCNTL bit 5) is set. See the explanation in Chapter 2 of this manual for use of this signal as an output.*

Figure 6-29: Bus Mode 3 and 4 Slave Write Cycle

Table 6-31: Bus Mode 3 and 4 Slave Write Timings

Parameter	Symbol	Min	Max	Units
ADS/ setup to BCLK high	t_1	4	-	ns
ADS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after ADS/	t_3	5	-	ns
CS/ hold from BCLK high after ADS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns

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Table 6-31: Bus Mode 3 and 4 Slave Write Timings

Parameter	Symbol	Min	Max	Units
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to READYO/, TEA/ low	t_7	5	20	ns
BCLK high to READYO/, TEA/ high	t_8	4	20	ns
READYI/ setup to BCLK high during or after READYO/, TEA/	t_9	9	-	ns
READYI/ hold from BCLK high during or after READYO/, TEA/	t_{10}	5	-	ns
Valid write data setup to BCLK high	t_{11}	6	-	ns
Valid write data hold from BCLK high	t_{12}	14	-	ns
A(6-2), BE (3-0), W_R/ setup to BCLK high[1]	t_{13}	4	-	ns
A(6-2), BE(3-0), W_R/ hold from BCLK high[2]	t_{14}	12	-	ns

1. The waveforms in this section show the address/byte enable signals for Bus Mode 4, A(31-2), BE(3-0). These waveforms also apply to the Bus Mode 3 Address/byte enable lines, A(31-0), BHE/.

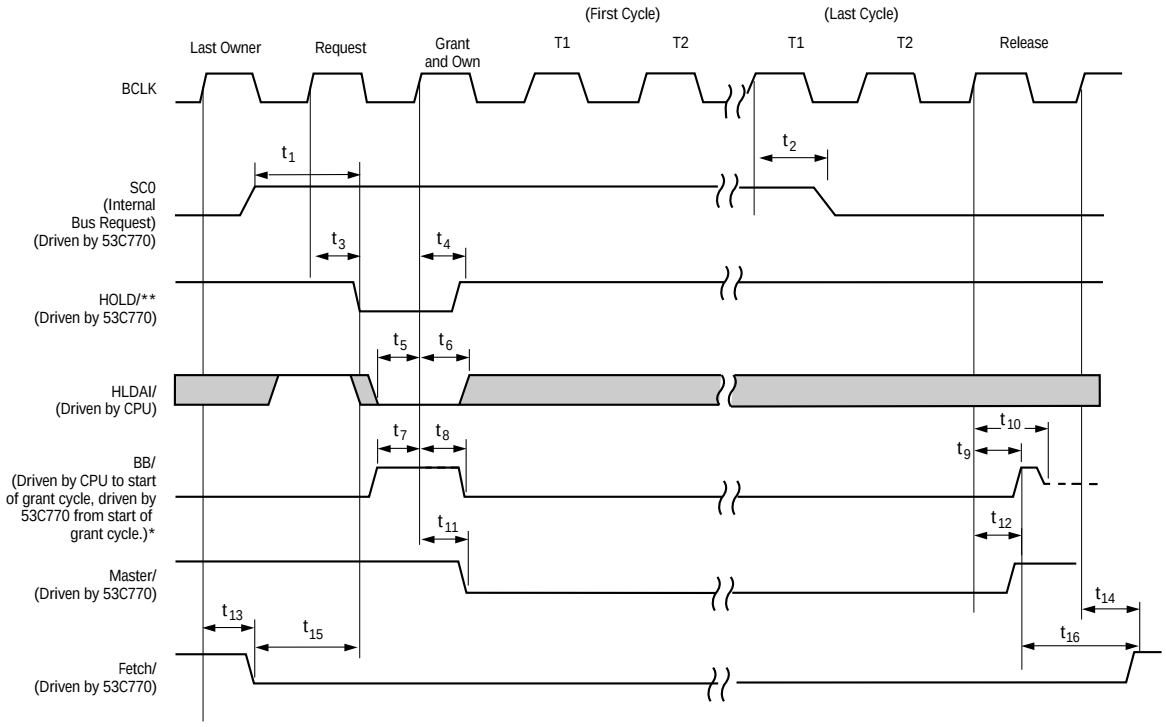
2. See note 1 above.

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Bus Mode 3 and 4 Host Bus Arbitration

Bus Arbitration Sequence

1. The SYM53C770 internally determines bus mastership is required. FETCH/ is asserted during cycles in which the SYM53C770 is retrieving new SCRIPTS instructions.
2. HOLD/ is asserted.
3. The SYM53C770 waits for Hold Acknowledge and checks that Bus Busy is deasserted. Then the SYM53C770 asserts Hold Acknowledge and Master, and deasserts Hold.



** BB/ should be tied high resistively if not used.*

***HOLD/ may be NANDed with MASTER/ to obtain HOLD required by the 80286 or 80386 processors.*

Note: the SYM53C770 will periodically assert the HOLD/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the HLDAI/ signal to complete the normal bus arbitration and handshake. The chip no longer wants host bus access—it deasserts the HOLD/, MASTER/, and all control lines after one BCLK, and does not assert ADS/, the signal that indicates a valid bus cycle is starting. The chip will then generate an interrupt, which the system may then service.

Figure 6-30: Bus Modes 3 and 4 Host Bus Arbitration

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Table 6-32: Bus Mode 3 and 4 Bus Arbitration Timings

Parameter	Symbol	Min	Max	Units
SC0 high to HOLD/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to HOLD/ low	t_3	4	20	ns
BCLK high to HOLD/ high	t_4	5	25	ns
HLDAI/ setup to BCLK high (any rising edge after HOLD/)	t_5	4	-	ns
HLDAI/ hold from BCLK high (any rising edge after HOLD/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after HOLD/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	24	ns
BCLK high to BB/ high	t_9	3	19	ns
BCLK high to BB/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
RETCH/ low to HOLD/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

**When Snoop Mode bit 0 of CTEST3 is set to 1.*

***During a retry operation, FETCH/ will remain low until a successful completion of the op code fetch or a fatal bus error.*

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Bus Mode 3 and 4 Fast Arbitration

Fast Arbitration Sequence

1. The SYM53C770 internally determines if bus mastership is required. FETCH/ is asserted during cycles in which the SYM53C770 is retrieving new SCRIPTS instructions.
2. HOLD/ is asserted.
3. The SYM53C770 waits for Hold Acknowledge (HLDAI). The SYM53C770 becomes bus master asynchronously on the leading edge of HLDAI/. The the SYM53C770 asynchronously asserts Bus Busy and Master, and deasserts HOLD/.
4. The SYM53C770 issues a start cycle on the next rising edge of BCLK.

Note: in fast arbitration mode, the SYM53C770 will take bus ownership on the assertion of HLDAI, regardless of the state of HOLD/ or BB/.

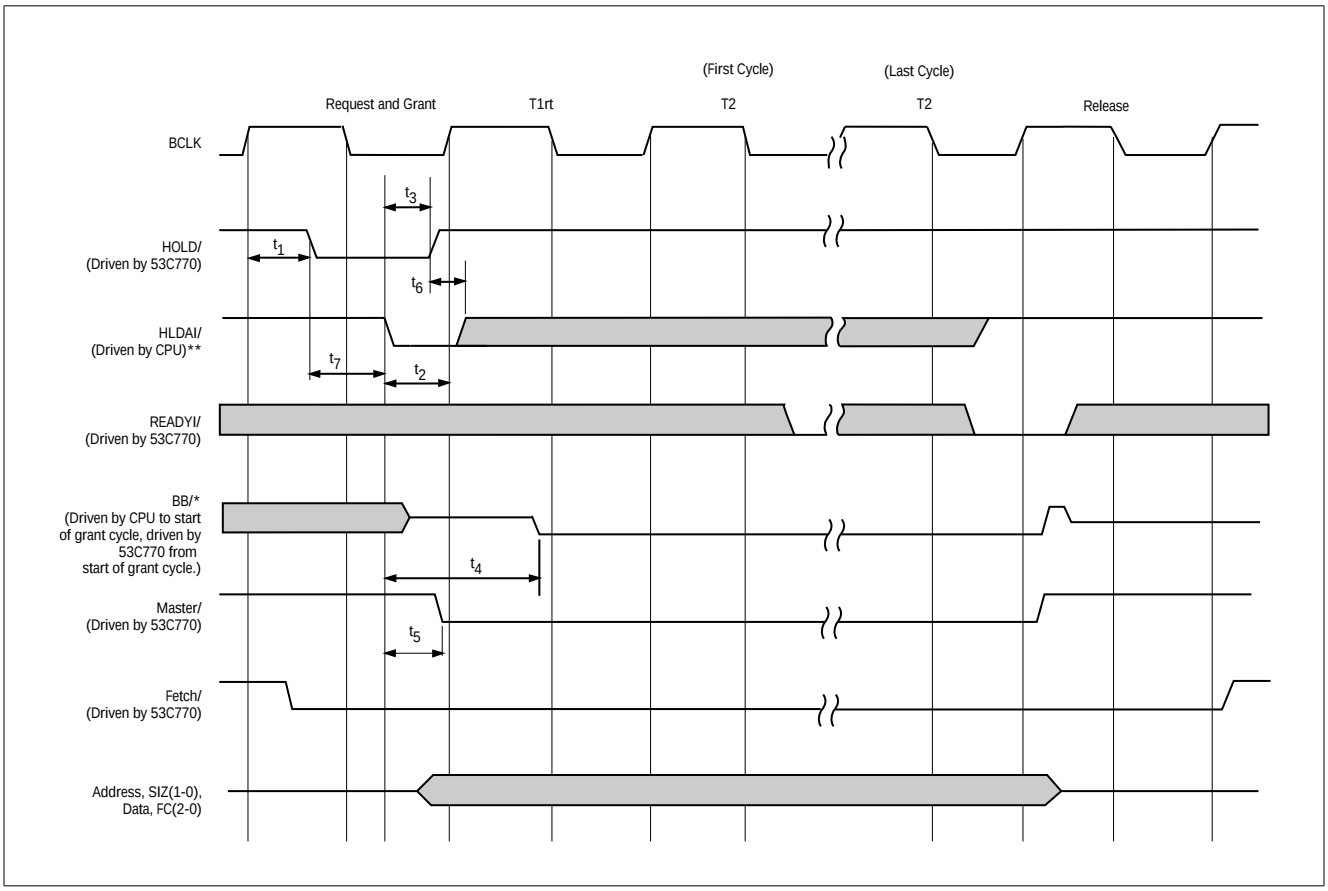


Figure 6-31: Bus Mode 3 and 4 Fast Arbitration

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Table 6-33: Bus Mode 3 and 4 Fast Arbitration

Parameter	Symbol	Min	Max	Units
BCLK high to HOLD/ asserted	t_1	-	20	ns
HLDAI/ setup to BCLK high	t_2	12	-	ns
HLDAI/ asserted to HOLD/ deasserted	t_3	-	22	ns
HLDAI/ asserted to BB/ asserted	t_4	-	20	ns
HLDAI/ asserted to MASTER/ asserted	t_5	-	16	ns
HLDAI/ hold after HOLD/ deasserted*	t_6	0	-	ns
HOLD/ asserted to HLDAI/ asserted	t_7	0	-	ns

**HLDAI/ may not be asserted prior to HOLD/*

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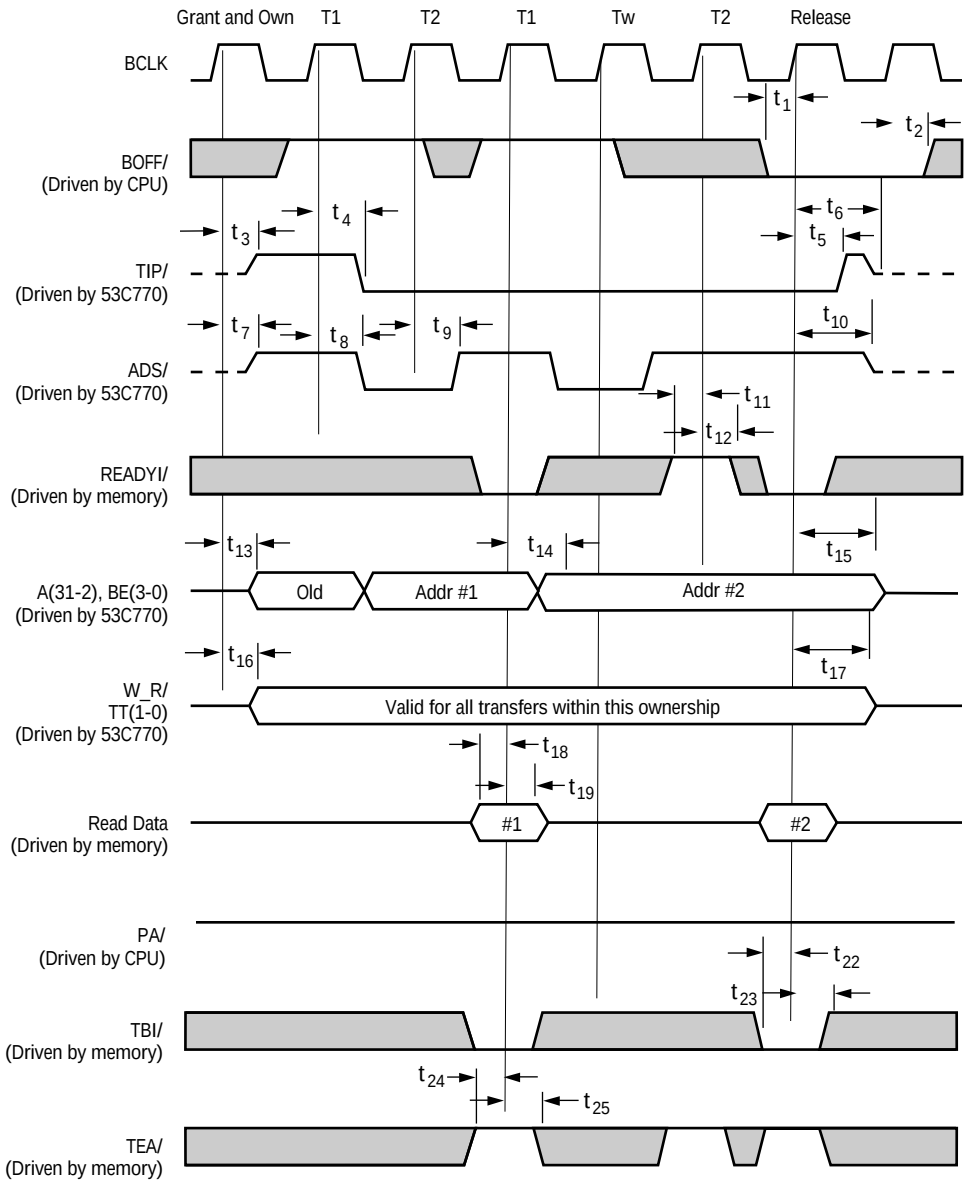
Bus Mode 3 and 4 Master Cycle

Bus Mode 3 and 4 Bus Master Read Sequence

1. The SYM53C770 has attained bus mastership.
2. The SYM53C770 asserts the W_R/, Transfer Modifier and Transfer Type lines.
3.
   a. The SYM53C770 asserts Transfer in Progress
   b. The SYM53C770 asserts Address Status, Address, and Byte Enable signals.[1]
4. The SYM53C770 deasserts Address Status.
5. The SYM53C770 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit, and Transfer Error Acknowledge
   - If Transfer Burst Inhibit is not asserted attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.
   - If Ready In is asserted and Transfer Error Acknowledge is not asserted and the SYM53C770 requires more cycles, then return to step 3b.
6. Upon acknowledge of the last bus cycle, the SYM53C770 deasserts Master, Bus Busy, and Transfer in Progress.
7. The SYM53C770 floats the Control and Address lines.

[1] The waveforms in this section show the address/byte enable signals for Bus Mode 4, A(31-2), BE(3-0). These waveforms also apply to the Bus Mode 3 Address/byte enable lines, A(31-0), BHE/.

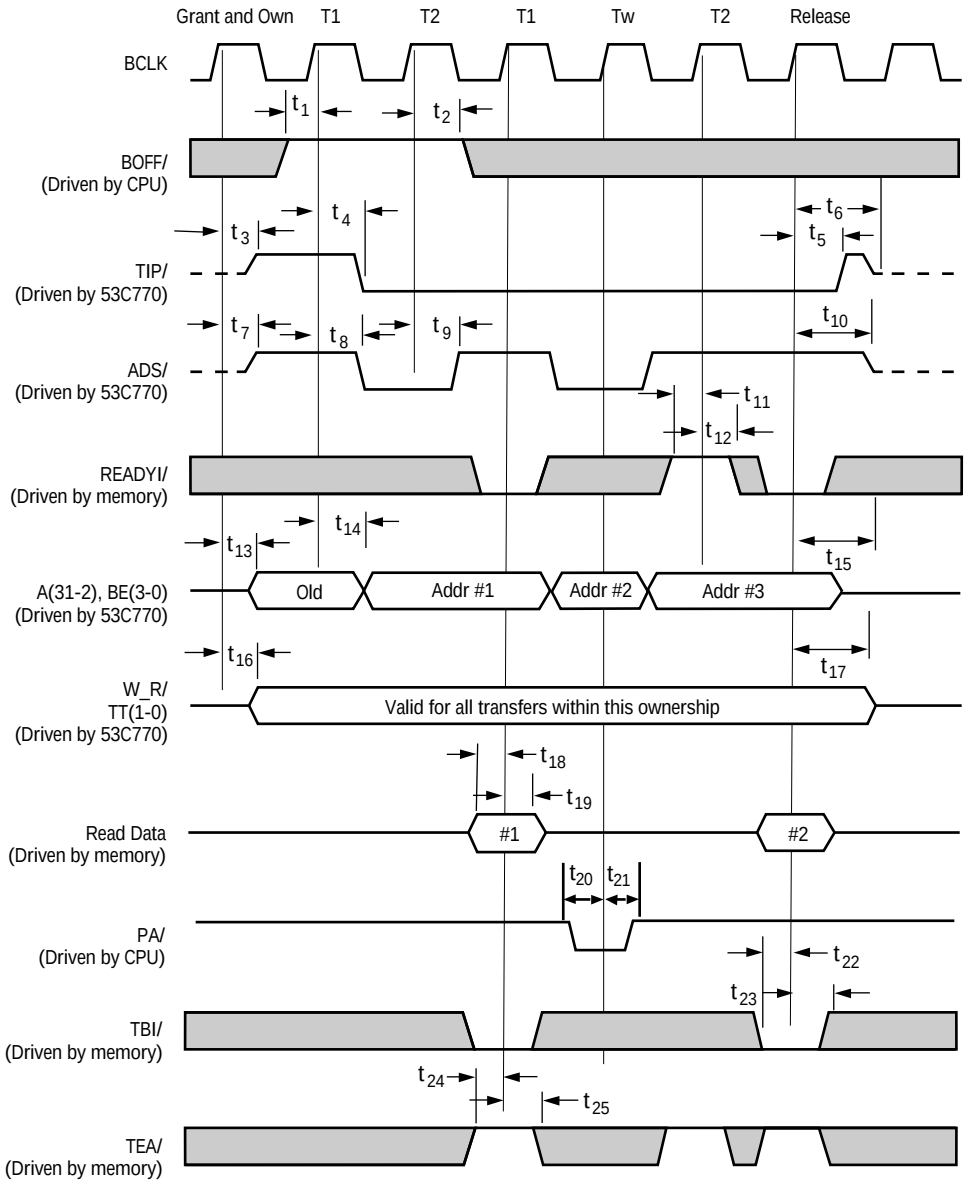
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Note: this diagram shows two back-to-back cycles for a burst size of two.

Figure 6-32: Bus Mode 3 and 4 Bus Master Read (Non-Preview of Address)

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Note: this diagram shows two back-to back cycles for a burst size of two

Figure 6-33: Bus Mode 3 and 4 Bus Master Read (Preview of Address)

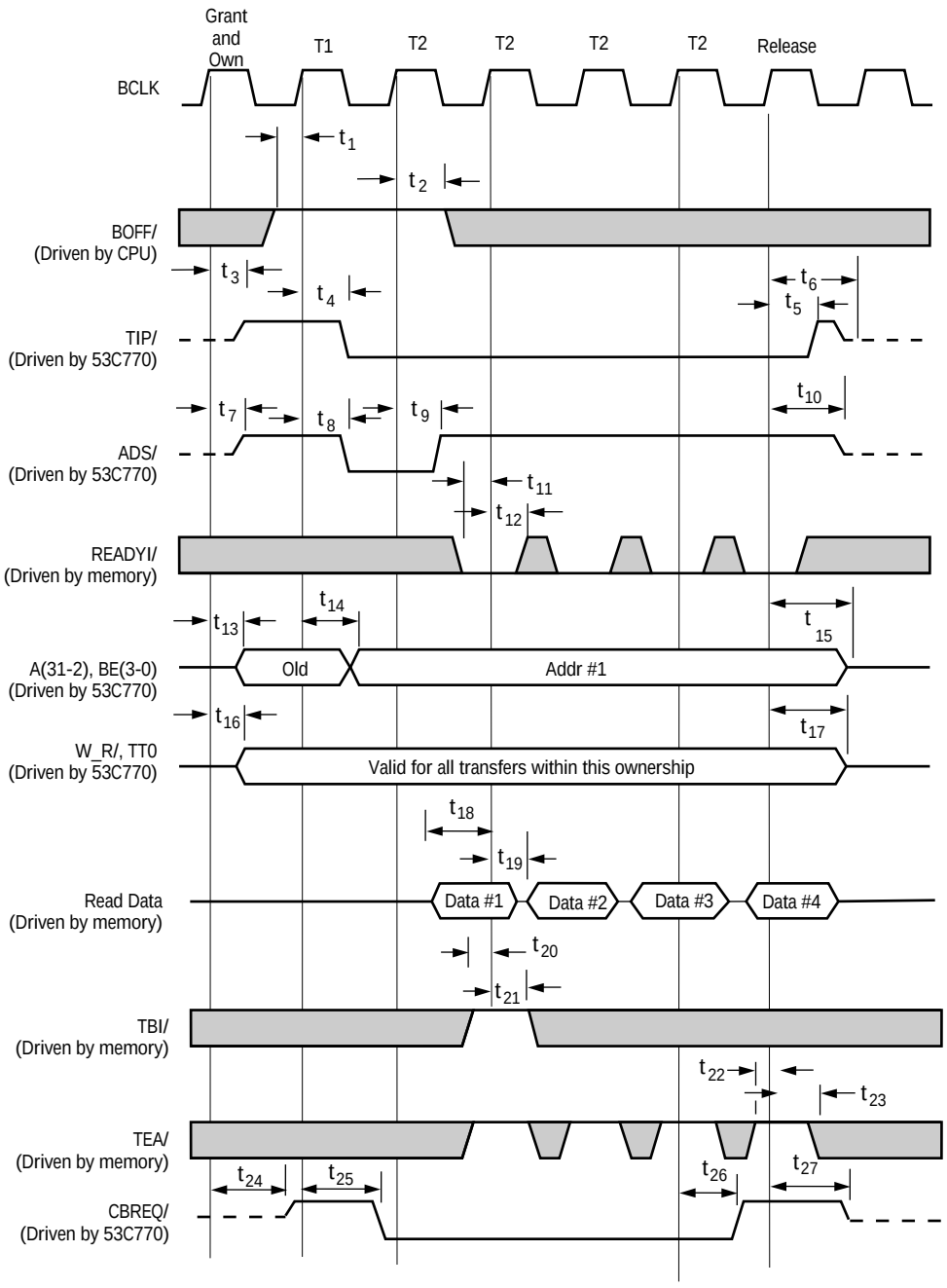
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Table 6-34: Bus Mode 3 and 4 Bus Master Read Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READY/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), BE(3-0) driven[1]	t_{13}	5	28	ns
BCLK high to A(31-2), BE(3-0) valid[2]	t_{14}	3	20	ns
BCLK high to A(31-2), BE(3-0) high-Z[3]	t_{15}	7	32	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{16}	5	30	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{17}	-	32	ns
Read Data setup to BCLK high	t_{18}	6	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
PA/ setup to BCLK high	t_{20}	5	-	ns
PA/ hold from BCLK high	t_{21}	5	-	ns
TBI/ setup to BCLK high	t_{22}	6	-	ns
TBI/ hold from BCLK high	t_{23}	4	-	ns
TEA/ setup to BCLK high	t_{24}	9	-	ns
TEA/ hold from BCLK high	t_{25}	5	-	ns

1. The waveforms in these sections show the address/byte enable signals for Bus Mode 4, A(31-2), BE(3-0). These waveforms also apply to the bus Mode 3 address/byte enable lines, A(31-0), BHE/
2. See note 1 above.
3. See note 1 above

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Note: this diagram shows one cache line burst of four.

Figure 6-34: Bus Mode 4 Bus Master Read (Cache Line Burst)

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Table 6-35: Bus Mode 4 Bus Master Read Timings (Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), BE (3-0) driven[1]	t_{13}	5	28	ns
BCLK high to A(31-2), BE (3-0) valid[2]	t_{14}	3	20	ns
BCLK high to A(31-2), BE (3-0) high-Z[3]	t_{15}	7	32	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{16}	5	30	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{17}	5	32	ns
Read Data setup to BCLK high	t_{18}	6	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
TBI/ setup to BCLK high	t_{20}	6	-	ns
TBI/ hold from BCLK high	t_{21}	4	-	ns
TEA/ setup to BCLK high	t_{22}	9	-	ns
TEA/ hold from BCLK high	t_{23}	5	-	ns
BCLK high to CBREQ/ driven	t_{24}	5	28	ns
BCLK high to CBREQ/ low	t_{25}	5	20	ns
BCLK/ high to CBREQ/ high	t_{26}	5	20	ns
BCLK high to CBREQ/ high-Z	t_{27}	7	32	ns

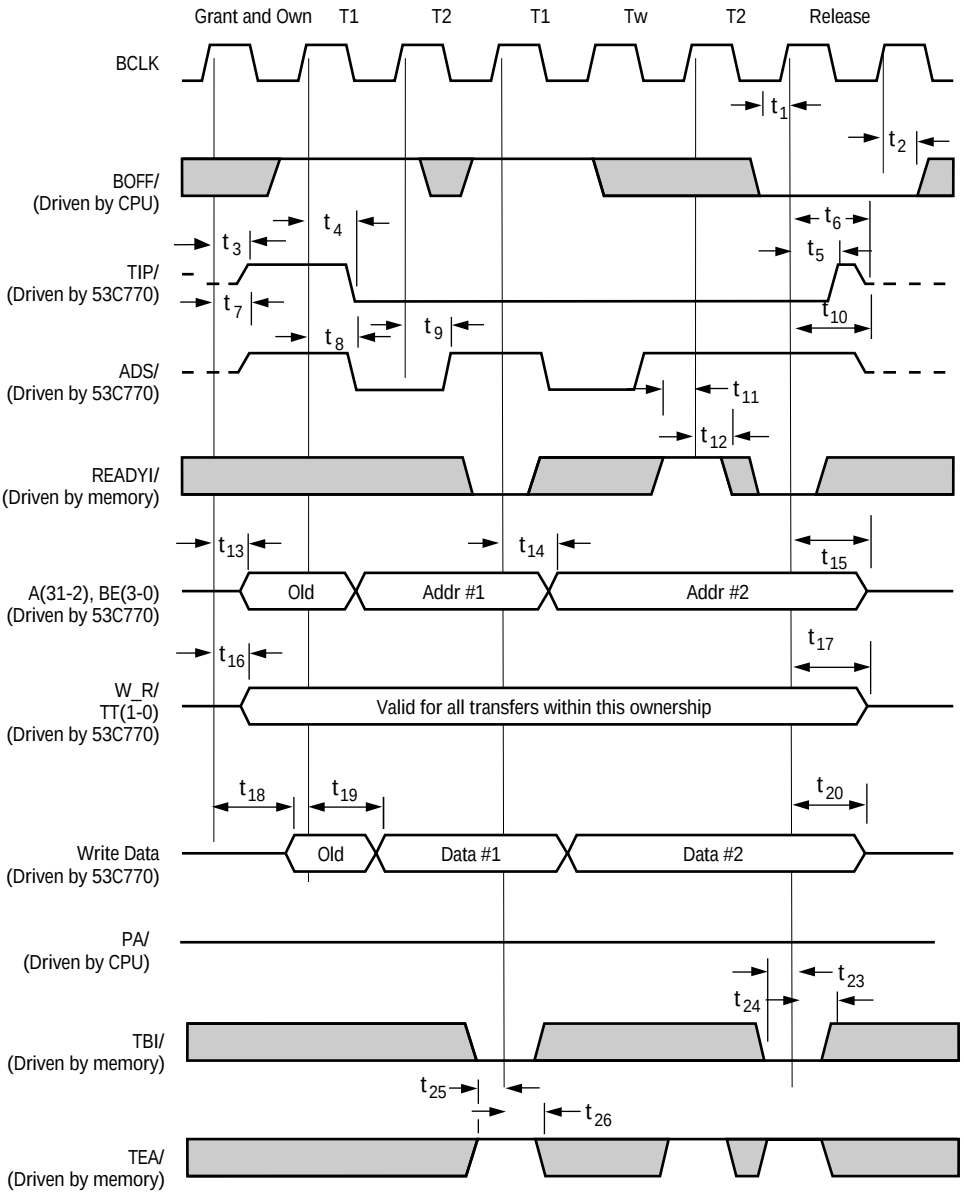
1. The waveforms in these sections show the address/byte enable signals for Bus Mode 4, A(31-2), BE(3-0). These waveforms also apply to the bus Mode 3 address/byte enable lines, A(31-0), BHE/.
2. See note 1 above.
3. See note 1 above.

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Bus Mode 3 and 4 Bus Master Write Sequence

1. The SYM53C770 has attained bus mastership.
2. The SYM53C770 asserts the W_R/, Transfer Modifier, and Transfer Type lines.
3.
   a. The SYM53C770 asserts Transfer in Progress.
   b. The SYM53C770 asserts the Address Status and Byte Enable signals, and the Address and Data lines.
4. The SYM53C770 deasserts Address Status.
5. The SYM53C770 waits for Ready In, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.
   - If Transfer Error Acknowledge is asserted and Ready In is not asserted and the SYM53C770 requires more cycles, then return to step 3b.
6. Upon acknowledge of the last bus cycle, the SYM53C770 deasserts Master, Busy, and Transfer in Progress.
7. The SYM53C770 floats the Control, Address, and Data Lines.

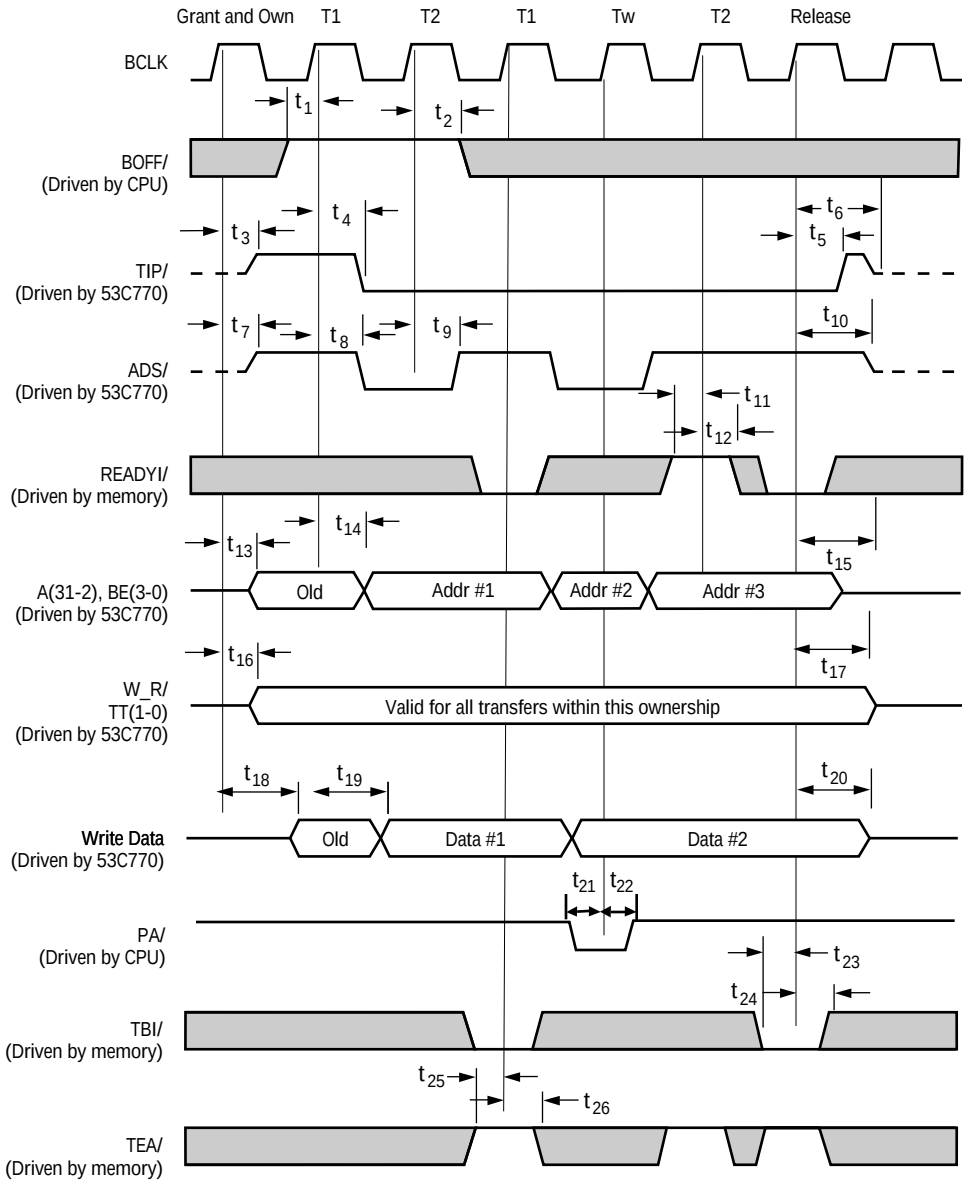
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Note: this diagram shows two back-to-back transfers for a transfer size of two.

Figure 6-35: Bus Mode 3 and 4 Bus Master Write (Non-Preview of Address)

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Note: this diagram shows two back-to-back transfers for a burst size of two.

Figure 6-36: Bus Mode 3 and 4 Bus Master Write (Preview of Address)

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Table 6-36: Bus Mode 3 and 4 Bus Master Write Timings

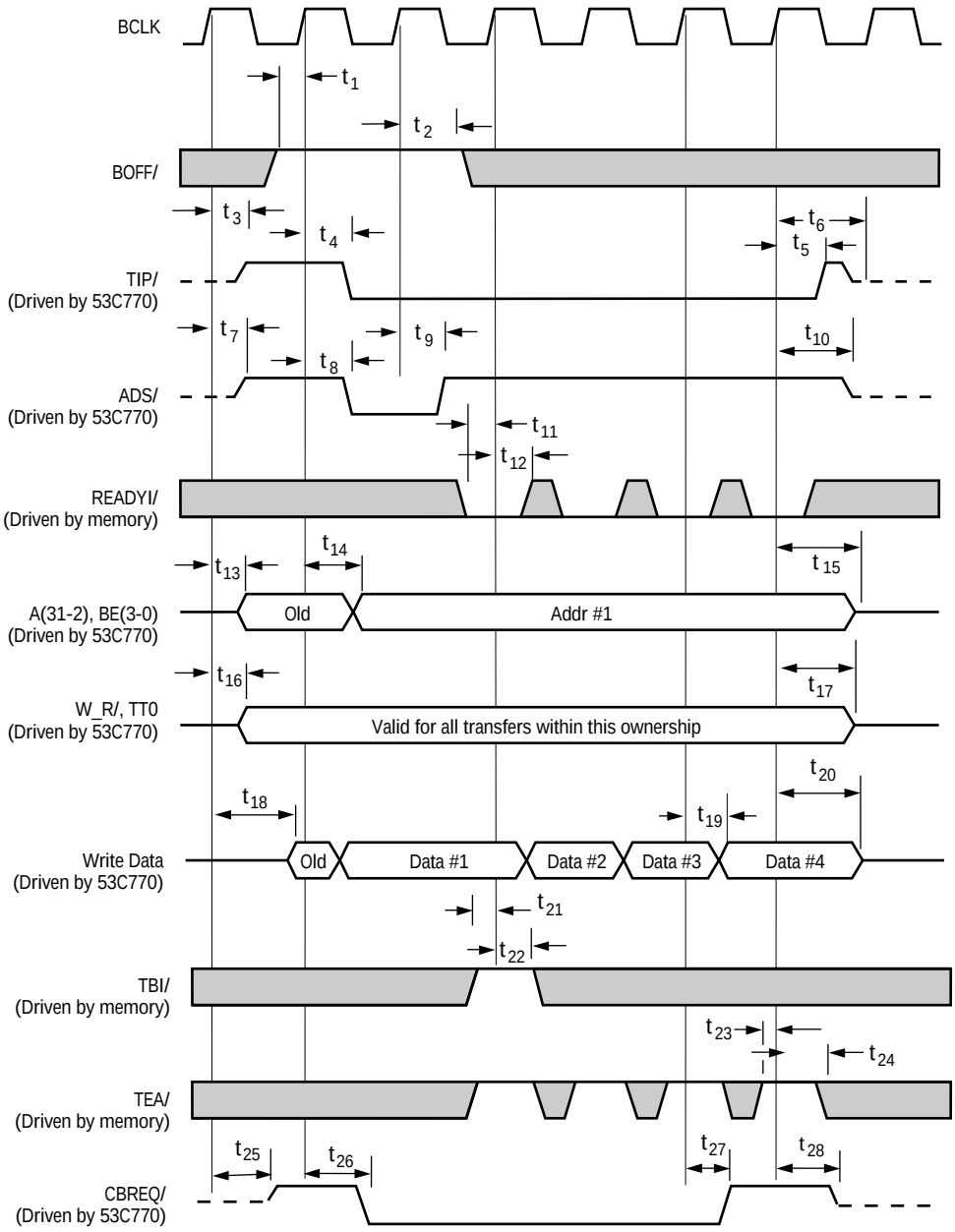
Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	4	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READY/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), BE(3-0) driven[1]	t_{13}	5	28	ns
BCLK high to A(31-2), BE(3-0) valid[2]	t_{14}	3	20	ns
BCLK high to A(31-2), BE(3-0) high-Z[3]	t_{15}	7	32	ns
BCLK high to W_R/, TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to Write Data driven	t_{18}	5	34	ns
BCLK high to Write Data valid	t_{19}	5	24	ns
BCLK high to Write Data high-Z	t_{20}	5	30	ns
PA/ setup to BCLK high	t_{21}	5	-	ns
PA/ hold from BCLK high	t_{22}	5	-	ns
TBI/ setup to BCLK high	t_{23}	6	-	ns
TBI/ hold from BCLK high	t_{24}	4	-	ns
TEA/ setup to BCLK high	t_{25}	9	-	ns
TEA/ hold from BCLK high	t_{26}	5	-	ns

1. The waveforms in these sections show the address/byte enable signals for Bus Mode 4, A(31-2), BE(3-0). These waveforms also apply to the bus Mode 3 address/byte enable lines, A(31-0), BHE/.

2. See note 1 above.

3. See note 1above.

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Note: this diagram shows one cache line burst of four.

Figure 6-37: Bus Mode 4 Bus Master Write (Cache Line Burst)

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Table 6-37: Bus Mode 4 Bus Master Write Timings (Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), BE(3-0) driven[1]	t_{13}	5	28	ns
BCLK high to A(31-2), BE(3-0) valid[2]	t_{14}	3	20	ns
BCLK high to A(31-2), BE(3-0) high-Z[3]	t_{15}	7	32	ns
BCLK high to W_R/, TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to Write Data driven	t_{18}	5	34	ns
BCLK high to Write Data valid	t_{19}	5	24	ns
BCLK high to Write Data high-Z	t_{20}	5	30	ns
TBI/ setup to BCLK high	t_{21}	6	-	ns
TBI/ hold from BCLK high	t_{22}	4	-	ns
TEA/ setup to BCLK high	t_{23}	9	-	ns
TEA/ hold from BCLK high	t_{24}	5	-	ns
BCLK high to CBREQ/ driven	t_{25}	5	28	ns
BCLK high to CBREQ/ low	t_{26}	5	20	ns
BCLK high to CBREQ/ high	t_{27}	5	20	ns
BCLK high to CBREQ/ high-Z	t_{28}	7	32	ns

1. The waveforms in these sections show the address/byte enable signals for Bus Mode 4, A(31-2), BE(3-0). These waveforms also apply to the bus Mode 3 address/byte enable lines, A(31-0), BHE/.

2. See note 1 above.

3. See note 1 above.

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SCSI Timings

Initiator Asynchronous Send

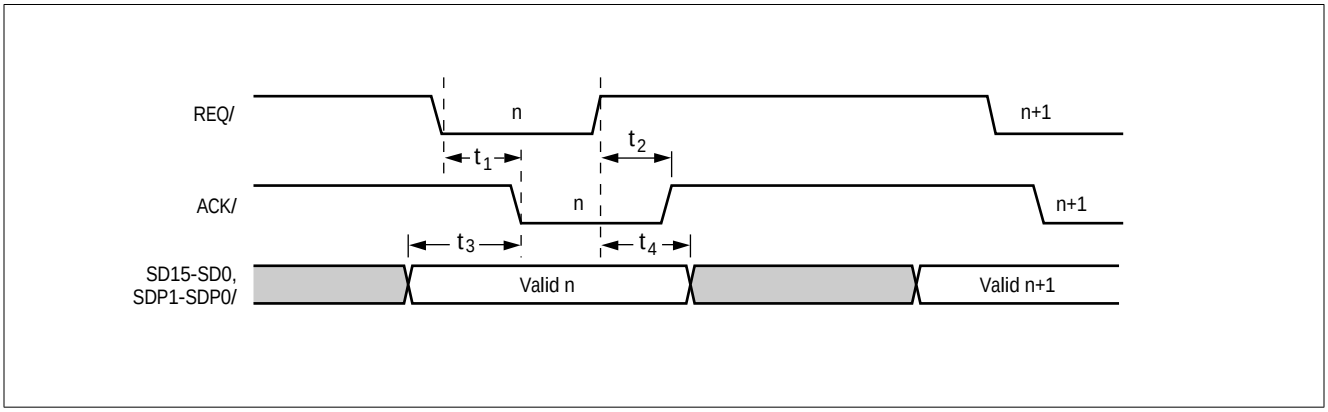


Figure 6-38: Initiator Asynchronous Send

Table 6-38: Initiator Asynchronous Send Timings

Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	55	-	ns
Data hold from ACK/ asserted	t_4	20	-	ns

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Initiator Asynchronous Receive

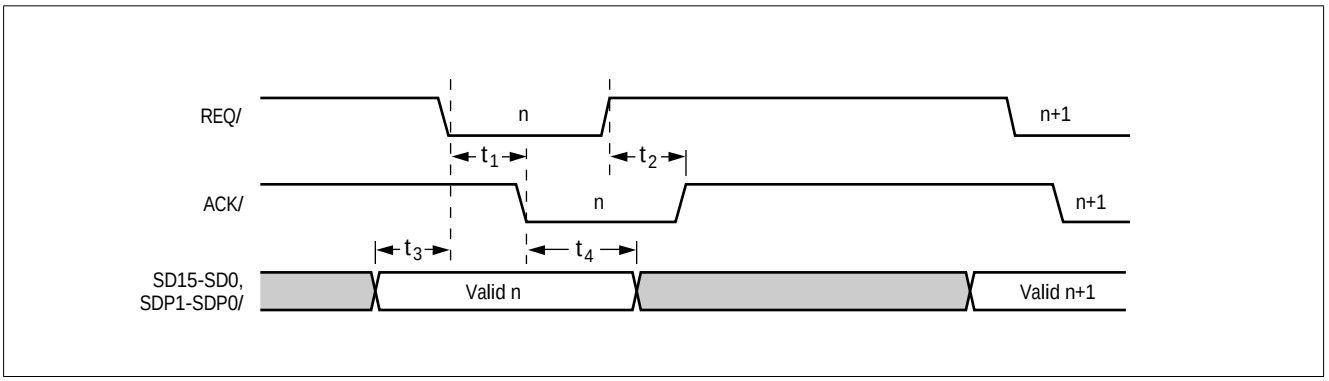


Figure 6-39: Initiator Asynchronous Receive

Table 6-39: Initiator Asynchronous Receive Timings

Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to REQ/ asserted	t_3	0	-	ns
Data hold from ACK/ asserted	t_4	0	-	ns

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Target Asynchronous Send

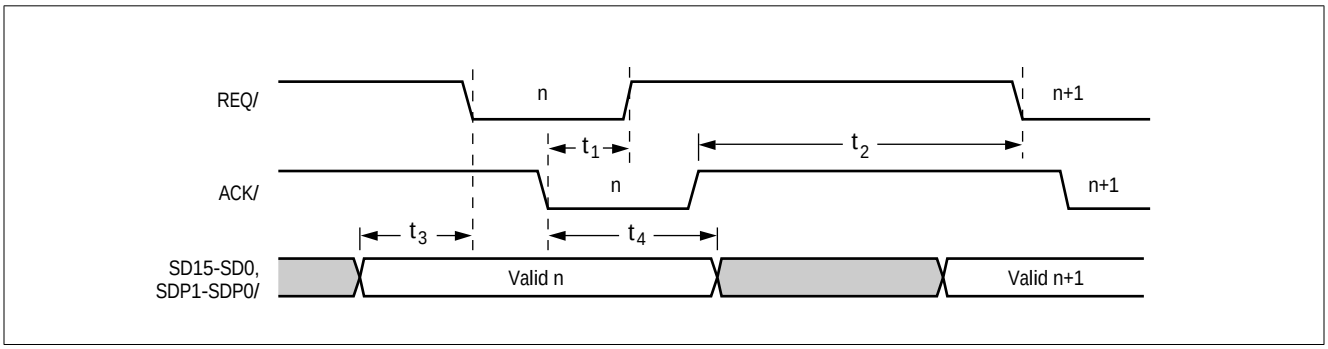


Figure 6-40: Target Asynchronous Send Waveforms

Table 6-40: Target Asynchronous Send Timings

Parameter	Symbol	Min	Max	Units
REQ/ deasserted from ACK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	10	-	ns
Data setup to REQ/ asserted	t_3	55	-	ns
Data hold from ACK/ asserted	t_4	20	-	ns

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Target Asynchronous Receive

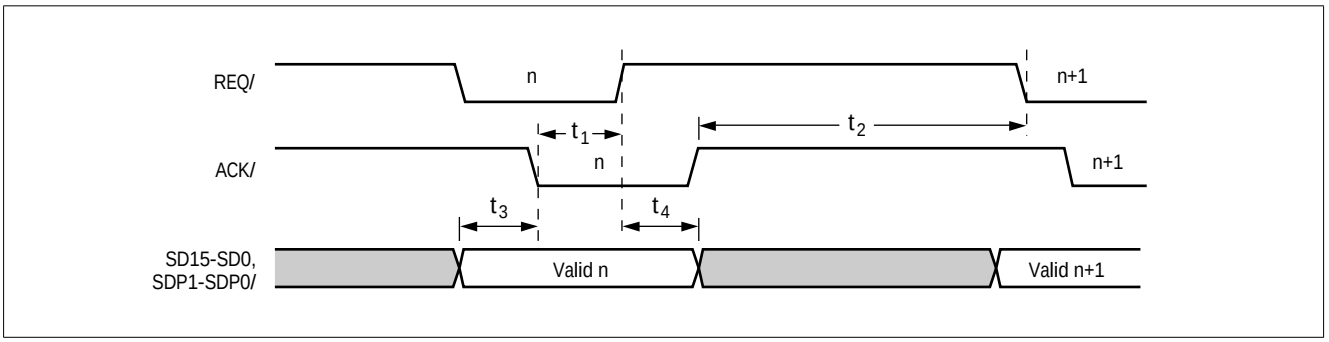


Figure 6-41: Target Asynchronous Receive

Table 6-41: Target Asynchronous Receive Timings

Parameter	Symbol	Min	Max	Units
REQ/ deasserted from CK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	0	-	ns
Data hold from REQ/ deasserted	t_4	0	-	ns

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Initiator and Target Synchronous Transfers

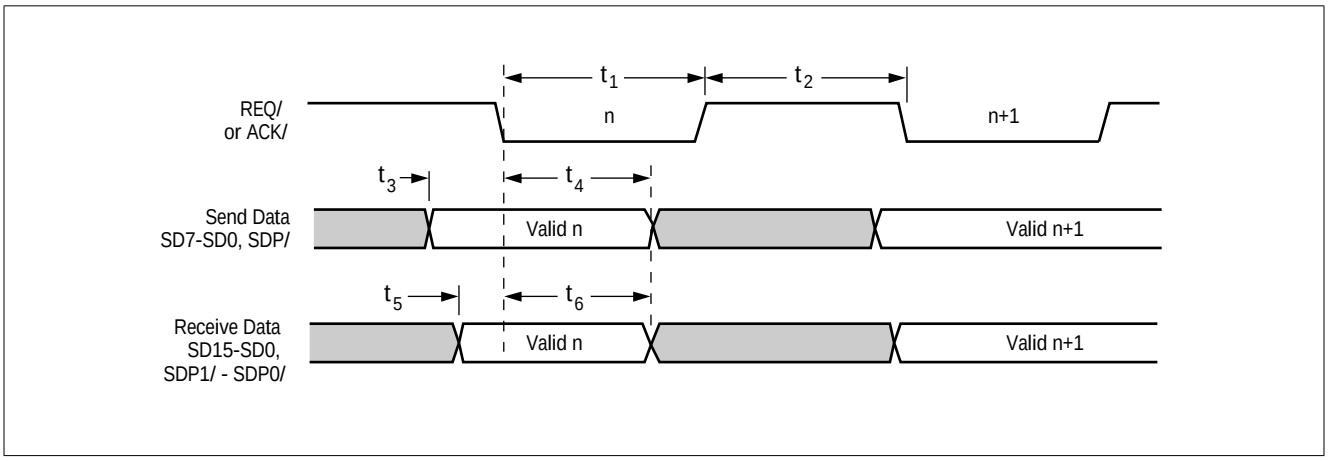


Figure 6-42: Initiator and Target Synchronous Transfers

Table 6-42: SCSI-1 Transfers (Single-ended, 5.0 MB/s)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	90	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	90	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	90	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	90	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	55	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	100	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	45	-	ns

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Table 6-43: SCSI-1 Transfers (Differential, 4.17 MB/s)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	96	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	96	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	84	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	84	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	65	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	110	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	45	-	ns

Table 6-44: SCSI-2 Fast Transfers (10.0 MB/s, 40 MHz clock)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	35	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	35	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	20	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	20	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	33	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	45	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	10	-	ns

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Table 6-45: SCSI-2 Fast Transfers (10.0 MB/s, 50 MHz clock)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	35	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	35	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	20	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	20	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	33	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	40**	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	10	-	ns

**Transfer Period bits (bits 6-4 in the SXFER register) are set to zero and the extra Clock Cycle of Data Setup bit (bit 7 in SCNTL) is set.*

*** Analysis of system configuration is recommended due to reduced driver skew margin in differential systems.*

Note: for fast SCSI, the TolerANT Enable bit (STEST3 bit 7) should be set.

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Table 6-46: Ultra SCSI Single-Ended Transfers (20.0 MB/s (8-bit transfers) or 40.0 MB/s (16-bit transfers), 80 or 100 MHz clock)

Symbol	Parameter	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	16	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	12	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	17	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	6	-	ns

**Transfer period bits (bits 6-4 in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.*

Note: for fast SCSI, set the TolerANT Enable bit (bit 7 in STEST3). During Fast-20 transfers, the value of the Extend REQ/ACK Filtering bit (STEST2, bit 1) has no effect.

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Table 6-47: Ultra SCSI Differential Transfers (20.0 MB/s (8-bit transfers) or 40.0 MB/s (16-bit transfers), 80 or 100 MHz clock)

Symbol	Parameter	MIn	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	16	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	16	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	21	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	6	-	ns

**Transfer period bits (bits 6-4 in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.*

Note: for fast SCSI, set the TolerANT Enable bit (bit 7 in STEST3). During Fast-20 transfers, the value of the Extend REQ/ACK Filtering bit (STEST2, bit 1) has no effect.

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Appendix A
Register Summary

Register 00 (03)
SCSI Control Zero (SCNTL0)
Read/Write

ARB1	ARB0	START	WATN/	EPC	EPG	AAP	TRG
7	6	5	4	3	2	1	0
Default>>							
1	1	0	0	0	0	0	0

Bit 7 **ARB1 (Arbitration mode bit 1)**
Bit 6 **ARB0 (Arbitration mode bit 0)**

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection or reselection

Bit 5 **START (Start sequence)**
Bit 4 **WATN (Select with ATN/ on a start sequence)**
Bit 3 **EPC (Enable parity checking)**
Bit 2 **EPG (Enable parity generation/parity through)**
Bit 1 **AAP (Assert ATN/ on parity error)**
Bit 0 **TRG (Target mode)**

Register 01 (02)
SCSI Control One (SCNTL1)
Read/Write

EXC	ADB	DHP	CON	RST	AESP	IARB	SST
7	6	5	4	3	2	1	0
Default >>>							
0	0	0	0	0	0	0	0

Bit 7 **EXC (Extra clock cycle of data setup)**
Bit 6 **ADB (Assert SCSI data bus)**
Bit 5 **DHP (Disable Halt on Parity Error or ATN) (Target Only)**
Bit 3 **RST (Assert SCSI RST/ signal)**
Bit 2 **AESP (Assert even SCSI parity (force bad parity))**
Bit 1 **IARB (Immediate Arbitration)**
Bit 0 **SST (Start SCSI Transfer)**

Register 02 (01)
SCSI Control Register Two (SCNTL2)
Read/Write

SDU	CHM	SLPMD	SLPHBEN	WSS	VUE1	VUE0	WSR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **DU (SCSI Disconnect Unexpected)**
Bit 6 **CHM (Chained Mode)**
Bit 5 **SLPMD (SLPAR Mode Bit)**
Bit 4 **SLPHBEN (SLPAR High Byte Enable)**
Bit 3 **WSS (Wide SCSI Send)**
Bit 2 **VUE1 (Vendor Unique Enhancements bit 1)**
Bit 1 **UE0 (Vendor Unique Enhancements bit 0)**
Bit 0 **WSR (Wide SCSI Receive)**

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Register 03 (00)
SCSI Control Three (SCNTL3)
Read/Write

Ultra	SCF2	SCF1	SCF0	EWS	CCF2	CCF1	CCF0
7	6	5	4	3	2	1	0
Default>>							
0	0	0	0	0	0	0	0

Bit 7 **Ultra (Ultra Enable)**
Bits 6-4 **SCF2-0 (Synchronous Clock Conversion Factor)**
Bit 3 **EWS (Enable Wide SCSI)**
Bits 2-0 **CCF2-0 (Clock Conversion Factor)**

Register 04 (07)
SCSI Chip ID (SCID)
Read/Write

RES	RRE	SRE	RES	ID3	ID2	ID1	ID0
7	6	5	4	3	2	1	0
Default>>							
X	0	0	X	0	0	0	0

Bit 7 **Reserved**
Bit 6 **RRE (Enable Response to Reselection)**
Bit 5 **SRE (Enable Response to Selection)**
Bit 4 **Reserved**
Bits 3-0 **Encoded Chip SCSI ID**

Register 05 (06)
SCSI Transfer (SXFER)
Read/Write

TP2	TP1	TP0	MO4	MO3	MO2	MO1	MO0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-5 **TP2-0 (SCSI Synchronous Transfer Period)**
Bits 4-0 **MO4-MO0 (Max SCSI synchronous offset)**

Register 06 (05)
SCSI Destination ID (SDID)
Read/Write

RES	RES	RES	RES	ID3	ID2	ID1	ID0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	0	0	0

Bits 7-4 **Reserved**
Bits 3-0 **Encoded Destination SCSI ID bits 3-0**

Register 07 (04)
General Purpose (GPREG)
Read/Write

RES	RES	RES	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	0	1	1	1	1

Bits 7-5 **Reserved**
Bits 4-0 **GPIO4-0 (General Purpose Inputs/Outputs)**

Register 08 (0B)
SCSI First Byte Received (SFBR)
Read/Write

7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-0 **1B7-0 (First byte received)**

Register 09 (0A)
SCSI Output Control Latch (SOCL)
Read /Write

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **REQ (Assert SCSI REQ/ signal)**
Bit 6 **ACK (Assert SCSI ACK/ signal)**
Bit 5 **BSY (Assert SCSI BSY/ signal)**
Bit 4 **SEL (Assert SCSI SEL/ signal)**
Bit 3 **ATN (Assert SCSI ATN/ signal)**
Bit 2 **MSG (Assert SCSI MSG/ signal)**
Bit 1 **C/D (Assert SCSI C_D/ signal)**
Bit 0 **I/O (Assert SCSI I_O/ signal)**

Register 0A (09)
SCSI Selector ID Register (SSID)
Read Only

VAL	Reserved			Encoded SCSI Destination ID			
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

Bit 7 **VAL (SCSI Valid Bit)**
Bits 6-4 **Reserved**
Bits 3-0 **Encoded Destination SCSI ID**

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Register 0B (08)
SCSI Bus Control Lines (SBCL)
Read Only

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

Bit 7 **REQ (REQ/ status)**
Bit 6 **ACK (ACK/ status)**
Bit 5 **BSY (BSY/ status)**
Bit 4 **SEL (SEL/ status)**
Bit 3 **ATN (ATN/ status)**
Bit 2 **MSG (MSG/ status)**
Bit 1 **C/D (C_D/ status)**
Bit 0 **I/O (I_O/ status)**

Register 0C (0F)
DMA Status (DSTAT)
Read Only

DFE	HPE	BF	ABRT	SSI	SIR	WTD	IID
7	6	5	4	3	2	1	0
Default>>>							
1	0	0	0	0	0	0	0

Bit 7 **DFE (DMA FIFO empty)**
Bit 6 **HPE (Host Parity Error)**
Bit 5 **BF (Bus fault)**
Bit 4 **ABRT (Aborted)**
Bit 3 **SSI (SCRIPTS step interrupt)**
Bit 2 **SIR (SCRIPTS interrupt instruction received)**
Bit 1 **WTD (Watchdog time-out detected)**
Bit 0 **IID (Illegal instruction detected)**

Register 0D (0E)
SCSI Status Zero (SSTAT0)
Read Only

ILF	ORF	OLF	AIP	LOA	WOA	RST/	SDP/
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **ILF (SIDL least significant byte full)**
Bit 6 **ORF (SODR least significant byte full)**
Bit 5 **OLF (SODL least significant byte full)**
Bit 4 **AIP (Arbitration in progress)**
Bit 3 **LOA (Lost arbitration)**
Bit 2 **WOA (Won arbitration)**
Bit 1 **RST/ (SCSI RST/ signal)**
Bit 0 **SDP0/ (SCSI SDP0/ parity signal)**

Register 0E (0D)
SCSI Status One (SSTAT1)
Read Only

FF3	FF2	FF1	FF0	SDP	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	X	X	X	X

Bits 7-4 **FF3-0 (FIFO flags)**
Bit 3 **SDP0 (Latched SCSI parity)**
Bit 2 **MSG (SCSI MSG/ signal)**
Bit 1 **C/D (SCSI C_D/ signal)**
Bit 0 **I/O (SCSI I_O/ signal)**

Register 0F (0C)
SCSI Status Two (SSTAT2)
Read Only

ILF1	ORF1	OLF1	FF4	SPL1	DIFF	LDSC	SDP1
7	6	5	4	3	2	1	0
Default: >>>							
0	0	0	0	X	0	1	X

Bit 7 **ILF1 (SIDL most significant byte full)**
Bit 6 **ORF1 (SODR most significant byte full)**
Bit 5 **OLF1 (SODL most significant byte full)**
Bit 4 **FF4 (FIFO Flags bit 4)**
Bit 3 **Latched SCSI parity for SD15-8**
Bit 2 **DIFFSENSE SENSE**
Bit 1 **LDSC (Last Disconnect)**
Bit 0 **SDP1 (SCSI SDP1 Signal)**

Registers 10-13 (10-13)
Data Structure Address (DSA)
Read/Write

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Register 14 (17)
Interrupt Status (ISTAT)
Read/Write

ABRT	RST	SIGP	SEM	CON	INTF	SIP	DIP
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **ABRT (Abort operation)**
Bit 6 **RST (Software reset)**
Bit 5 **SIGP (Signal process)**
Bit 4 **SEM (Semaphore)**
Bit 3 **CON (Connected)**
Bit 2 **INTF (Interrupt on the Fly)**
Bit 1 **SIP (SCSI interrupt pending)**
Bit 0 **DIP (DMA interrupt pending)**

Register 18 (1B)
Chip Test Zero (CTEST0)
Read/Write

CDIS	SC1	SC0	GRP	DFP	EHP	TT1	C386E
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	X	0	0	0

Bit 7 **CDIS (Cache burst disable)**
Bits 6-5 **SC1-0 (Snoop control)**
Bit 4 **GRP (Generate Receive Parity)**
Bit 3 **DFP (DMA FIFO parity)**
Bit 2 **EHP (Even host parity)**
Bit 1 **TT1 (Transfer type bit)**
Bit 0 **C386E (Cache 386 Enable)**

Register 19 (1A)
Chip Test One (CTEST1)
Read Only

FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFl0
7	6	5	4	3	2	1	0
Default >>>							
1	1	1	1	0	0	0	0

Bits 7-4 **FMT3-0 (Byte Empty in DMA FIFO)**
Bits 3-0 **FFL3-0 (Byte Full in DMA FIFO)**

Register 1A (19)
Chip Test Two (CTEST2)
Read Only

DDIR	SIGP	RES	RES	DFP	TEOP	DREQ	DACK
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	X	0	0	0	1

Bit 7 **DDIR (Data Transfer Direction)**
Bit 6 **SIGP (Signal process)**
Bit 5 **Reserved**
Bit 4 **Reserved**
Bit 3 **DFP (DMA FIFO parity)**
Bit 2 **TEOP (SCSI true end of process)**
Bit 1 **DREQ (Data request status)**
Bit 0 **DACK (Data acknowledge status)**

Register 1B (18)
Chip Test Three (CTEST3)
Read/Write

V3	V2	V1	V0	FLF	CLF	FM	SM
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	0	0	0

Bits 7-4 **V3-0 (Chip revision level)**
Bit 3 **FLF (Flush DMA FIFO)**
Bit 2 **CLF (Clear DMA FIFO)**
Bit 1 **FM (Fetch pin mode)**
Bit 0 **SM (Snoop pins mode)**

Registers 1C-1F (1C-1F)
Temporary Stack (TEMP)
Read/Write

Register 20 (23)
DMA FIFO (DFIFO)
Read/Write

RES	BO6	BO5	BO4	BO3	BO2	BO1	BO0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bit 7 **Reserved**
Bits 6-0 **BO6-0 (Byte offset counter)**

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Register 21 (22)
Chip Test Four (CTEST4)
Read/Write

MUX	ZMOD	ZSD	SRTM	EHPC	FBL2	FBL1	FBL0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **MUX (Host bus multiplex mode)**
Bit 6 **ZMOD (High impedance mode)**
Bit 5 **ZSD (SCSI DMA High Impedance Mode)**
Bit 4 **SRTM (Shadow Register Test Mode)**
Bit 3 **EHPC (Enable Host Parity Check)**
Bits 2-0 **FBL2-0 (FIFO byte control**

Register 22 (21)
Chip Test Five (CTEST5)
Read/Write

ADCK	BBCK	RES	MASR	DDIR	RAM0	RAM1	RAMEN
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	0	0	0	0	0

Bit 7 **ADCK (Clock address incrementor)**
Bit 6 **BBCK (Clock byte counter)**
Bit 5 **Reserved**
Bit 4 **MASR (Master control for set or reset pulses)**
Bit 3 **DDIR (DMA direction)**
Bit 2-1 **RAM1-0 (SCRIPTS RAM bits 1-0)**
Bit 0 **RAMEN (RAM Base Address Enable)**

Register 23 (20)
Chip Test Six (CTEST6)
Read/Write

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DMA Byte Counter (DBC)
Read/Write

Register 27 (24)
DMA Command (DCMD)
Read/Write

Registers 28-2B (28-2B)
DMA Next Data Address (DNAD)
Read/Write

Registers 2C-2F (2C-2F)
DMA SCRIPTS Pointer (DSP)
Read/Write

Registers 30-33(30-33)
DMA SCRIPTS Pointer Save (DSPS)
Read/Write

Registers 34-37 (34-37)
Scratch Register A (SCRATCHA)
Read/Write

Register 38 (3B)
DMA Mode (DMODE)
Read/Write

BL1	BL0	FC2	FC1	PD	FAM	UO	MAN
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7-6 **BL1-0 (Burst length)**
Bit 5-4 **FC2-1 (Function code) (Bus Modes 1, 3 and 4), or TM2-1 (Transfer Modifier) (Bus Mode 2)**
Bit 3 **PD (Program/data)**
Bit 2 **FAM (Fixed address mode)**
Bit 1 **UO/TT0 (User programmable transfer type)**
Bit 0 **MAN (Manual start mode)**

Register 39 (3A)
DMA Interrupt Enable (DIEN)
Read/Write

RES	HPED	BF	ABRT	SSI	SIR	WTD	IID
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bit 7 **Reserved**
Bit 6 **HPED (Host parity error detected during DMA read or Slave write)**
Bit 5 **BF (Bus fault)**
Bit 4 **ABRT (Aborted)**
Bit 3 **SSI (SCRIPTS step interrupt)**
Bit 2 **SIR (SCRIPTS interrupt instruction received)**
Bit 1 **WTD (Watchdog time-out detected)**
Bit 0 **IID (Illegal instruction detected)**

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Register 3A (39)
DMA Watchdog Timer (DWT)
Read/Write

7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Register 3B (38)
DMA Control (DCNTL)
Read/Write

STE	BSM	EA	SSM	BW16	STD	FA	COM
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **STE (Size Throttle Enable)**
Bit 6 **BSM (Bus Mode)**
Bit 5 **EA (Enable ACK)**
Bit 4 **SSM (Single-step mode)**
Bit 3 **BW16 (Host Bus Width Equal to 16)**
Bit 2 **STD (Start DMA operation)**
Bit 1 **FA (Fast arbitration)**
Bit 0 **COM (53C700 compatibility)**

Register 3C-3F (3C-3F)
Adder Sum Output (ADDER)
Read Only

Register 40 (43)
SCSI Interrupt Enable Zero (SIEN0)
Read/Write

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **M/A (SCSI Phase Mismatch - Initiator Mode; SCSI ATN Condition - Target Mode)**
Bit 6 **CMP (Function Complete)**
Bit 5 **SEL (Selected)**
Bit 4 **RSL (Reselected)**
Bit 3 **SGE SCSI Gross Error)**
Bit 2 **UDC (Unexpected Disconnect)**
Bit 1 **RST (SCSI Reset Condition)**
Bit 0 **PAR (SCSI Parity Error)**

Register 41 (42)
SCSI Interrupt Enable One (SIEN1)
Read/Write

RES	RES	RES	RES	RES	STO	GEN	HTH
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	0	0	0

Bits 7-3 **Reserved**
Bit 2 **STO (Selection or Reselection Time-out)**
Bit 1 **GEN (General Purpose Timer Expired)**
Bit 0 **HTH (Handshake to Handshake Timer Expired)**

Register 42 (41)
SCSI Interrupt Status Zero (SIST0)
Read Only

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **M/A (Initiator Mode: Phase Mismatch; Target Mode: ATN/ Active)**
Bit 6 **CMP (Function Complete)**
Bit 5 **SEL (Selected)**
Bit 4 **RSL (Reselected)**
Bit 3 **SGE (SCSI Gross Error)**
Bit 2 **UDC (Unexpected Disconnect)**
Bit 1 **RST (SCSI RST/ Received)**
Bit 0 **PAR (Parity Error)**

Register 43 (40)
SCSI Interrupt Status One (SIST1)
Read Only

RES	RES	RES	RES	RES	STO	GEN	HTH
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	0	0	0

Bits 7-3 **Reserved**
Bit 2 **STO (Selection or Reselection Time-out)**
Bit 1 **GEN (General Purpose Timer Expired)**
Bit 0 **HTH (Handshake to Handshake timer Expired)**

Register 44 (47)
SCSI Longitudinal Parity (SLPAR)
Read/Write

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Register 45 (46)
SCSI Wide Residue Data (SWIDE)
Read Only

Register 46 (45)
Memory Access Control (MACNTL)
Read/Write

TYP3	TYPE2	TYP1	TYP0	DataWR	DataRD	PSCRIPT	SCRIPT
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	0	0	0

Bits 7-4 **TYP3-0 (Chip Type)**
Bits 3-0

Register 47 (44)
General Purpose Control (GPCNTL)
Read/Write

RES	RES	RES	GPIO_en4	GPIO_en3	GPIO_en2	GPIO_en1	GPIO_en0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	0	1	1	1	1

Bits 7-5 **Reserved**
Bit 4 **GPIO_en4 (General Purpose Output Enable 4)**
Bits 3-0 **GPIO_en3-0 (General Purpose Output Enable 3-0)**

Register 48 (4B)
SCSI Timer Register 0 (STIME0)
Read /Write

HTH3	HTH2	HTH1	HTH0	SEL3	SEL2	SEL1	SEL0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-4 **HTH (Handshake-to-Handshake Timer Period)**
Bits 3-0 **SEL (Selection Time-out Period)**

Register 49 (4A)
SCSI Timer Register One (STIME1)
Read/Write

RES	HTHBA	GENSF	HTHSF	GEN3	GEN2	GEN1	GEN0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bits 7 **Reserved**
Bit 6 **Handshake-to-Handshake Timer Bus Activity Enable Bit (HTHBA)**
Bit 5 **General Purpose Timer Scale Factor Bit (GENSF)**
Bit 4 **Handshake-to-Handshake Timer Scale Factor Bit (HTHSF) Bit (HTHSF)**
Bits 3-0 **GEN3-0 (General Purpose Timer Period)**

Register 4A (49)
Response ID Zero (RESPID0)
Read/Write

Register 4B (48)
Response ID One (RESPID1)
Read/Write

Register 4C (4F)
SCSI Test Register Zero (STEST0)
Read Only

SSAID	SSAID	SSAID	SSAID	SLT	ART	SOZ	SOM
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	X	1	1

Bits 7-4 **SSAID (SCSI Selected ASID)**
Bit 3 **SLT (Selection Response Logic Test)**
Bit 2 **ART (Arbitration Priority Encoder Test)**
Bit 1 **SOZ (SCSI Synchronous Offset Zero)**
Bit 0 **SOM (SCSI Synchronous Offset Maximum)**

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Register 4D (4E)
SCSI Test Register One (STEST1)
Read Only

RES 7	RES 6	RES 5	RES 4	DBLEN 3	DBLSEL 2	SFP1 1	SFP0 0
Default >>>							
X	X	X	X	0	0	X	X

Bits 7-4 **Reserved**
Bit 3 **SCLK Doubler Enable (DBLEN)**
Bit 2 **SCLK Doubler Select (DBLSEL)**
Bits 1-0 **SFP1-0 (SCSI FIFO Parity)**

Register 4E (4D)
SCSI Test Register Two (STEST2)
Read/Write

SCE 7	ROF 6	DIF 5	SLB 4	SZM 3	AWS 2	EXT 1	LOW 0
Default >>>							
0	0	0	0	0	0	0	0

Bit 7 **SCE (SCSI Control Enable)**
Bit 6 **ROF (Reset SCSI Offset)**
Bit 5 **DIF (SCSI Differential Mode)**
Bit 4 **SLB (SCSI Loopback Mode)**
Bit 3 **SZM (SCSI High-Impedance Mode)**
Bit 2 **AWS (Always Wide SCSI)**
Bit 1 **EXT (Extend REQ/ACK Filtering)**
Bit 0 **LOW (SCSI Low level Mode)**

Register 4F (4C)
SCSI Test Register Three (STEST3)
Read/Write

TE 7	STR 6	HSC 5	DSI 4	S16 3	TTM 2	CSF 1	FTM 0
Default>>>							
X	X	0	0	0	0	0	0

Bit 7 **TE (TolerANT Enable)**
Bit 6 **STR (SCSI FIFO Test Read)**
Bit 5 **HSC (Halt SCSI Clock)**
Bit 4 **DSI (Disable Single Initiator Response)**
Bit 3 **S16 (16-bit System)**
Bit 2 **TTM (Timer Test Mode)**
Bit 1 **CSF (Clear SCSI FIFO)**
Bit 0 **STW (SCSI FIFO Test Write)**

Registers 50-51 (52-53)
SCSI Input Data Latch (SIDL)
Read Only

Registers 54-55 (56-57)
SCSI Output Data Latch (SODL)
Read/Write

Registers 58-59 (5A-5B)
SCSI Bus Data Lines (SBDL)
Read Only

Registers 5C-5F
Scratch Register B (SCRATCHB)
Read/Write

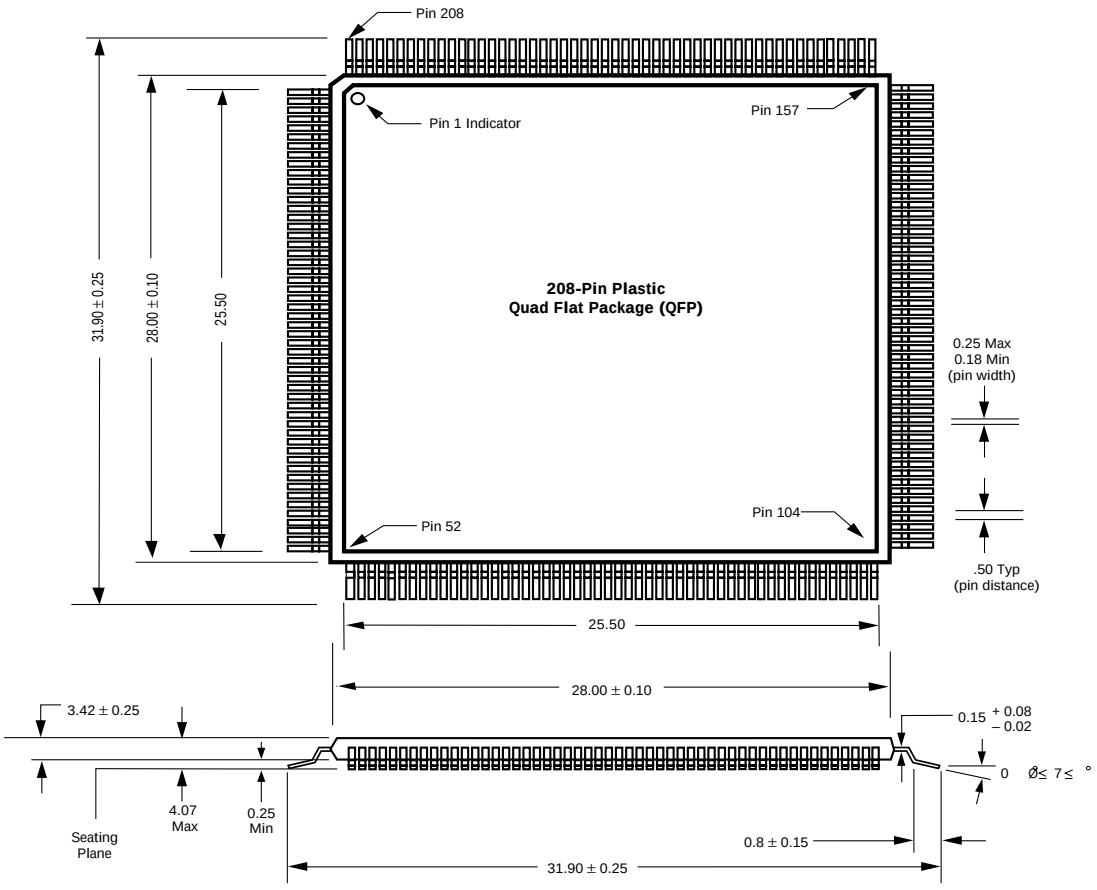
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Appendix B

Mechanical Drawings

SYM53C770 Mechanical Drawing



** All dimensions are in millimeters.*

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Appendix C
Application Notes

SEN 833	SYM53C720 to 68030 Interface
SEN 836	SYM53C720 to 80386SX Interface
SEN 848	SYM53C720 to 80486 Interface
SEN 849	SYM53C720 to VESA Local Bus Interface

Note: these application notes for the SYM53C720 also apply to the SYM53C770.

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Printed in the U.S.A.
T18962I
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Appendix B: Texas Instruments TL16C550A Asynchronous Communications Element

B.1 The following Pages contain the Texas Instruments TL16C550A Asynchronous Communications Element Manual.

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- **Capable of Running With All Existing TL16C450 Software**
- **After Reset, All Registers Are Identical to the TL16C450 Register Set**
- **In the FIFO Mode, Transmitter and Receiver Are Each Buffered With 16-Byte FIFOs to Reduce the Number of Interrupts to the CPU**
- **In the TL16C450 Mode, Holding and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data**
- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to (2^{16} – 1) and Generates an Internal 16× Clock**
- **Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream**
- **Independent Receiver Clock Input**
- **Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (dc to 256 Kbit/s)**
- **False-Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **3-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, Framing Error Simulation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$)**
- **Faster Plug-In Replacement for National Semiconductor NS16550A**

description

The TL16C550A is a functional upgrade of the TL16C450 asynchronous communications element (ACE). Functionally identical to the TL16C450 on power up (character mode†), the TL16C550A can be placed in an alternate mode (FIFO) to relieve the CPU of excessive software overhead.

In this mode, internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two of the TL16C450 terminal functions (terminals 24 and 29 on the N package and terminals 27 and 32 on the FN package) have been changed to allow signalling of direct memory address (DMA) transfers.

The TL16C550A performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE at any point in the ACE's operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C550A ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to (2^{16} – 1) and producing a 16× clock for driving the internal transmitter logic. Provisions are included to use this 16× clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

† The TL16C550A can also be reset to the TL16C450 mode under software control.



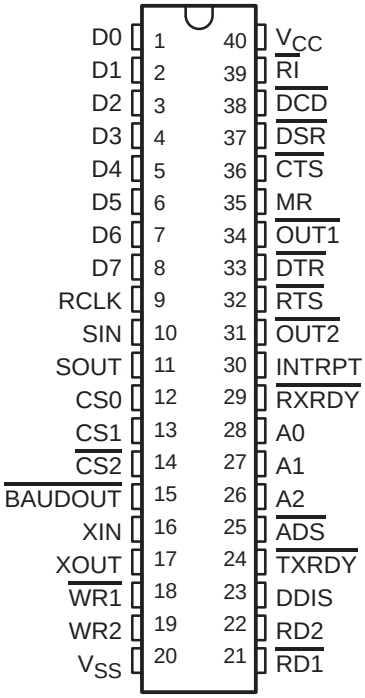
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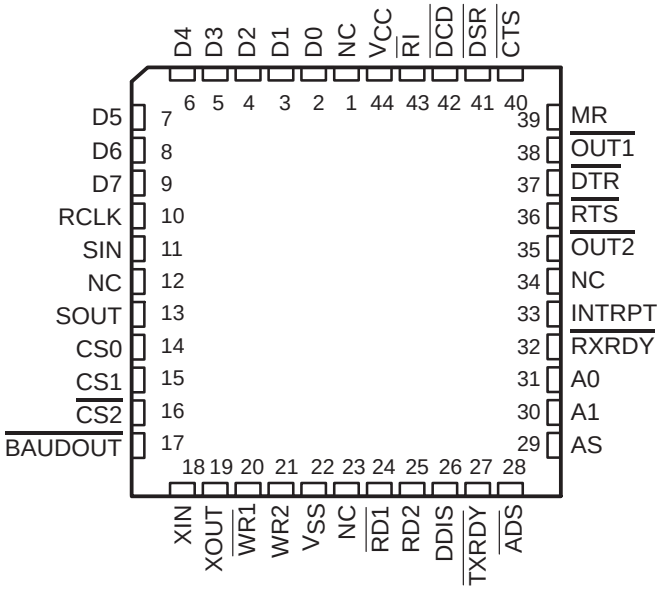
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N PACKAGE
(TOP VIEW)



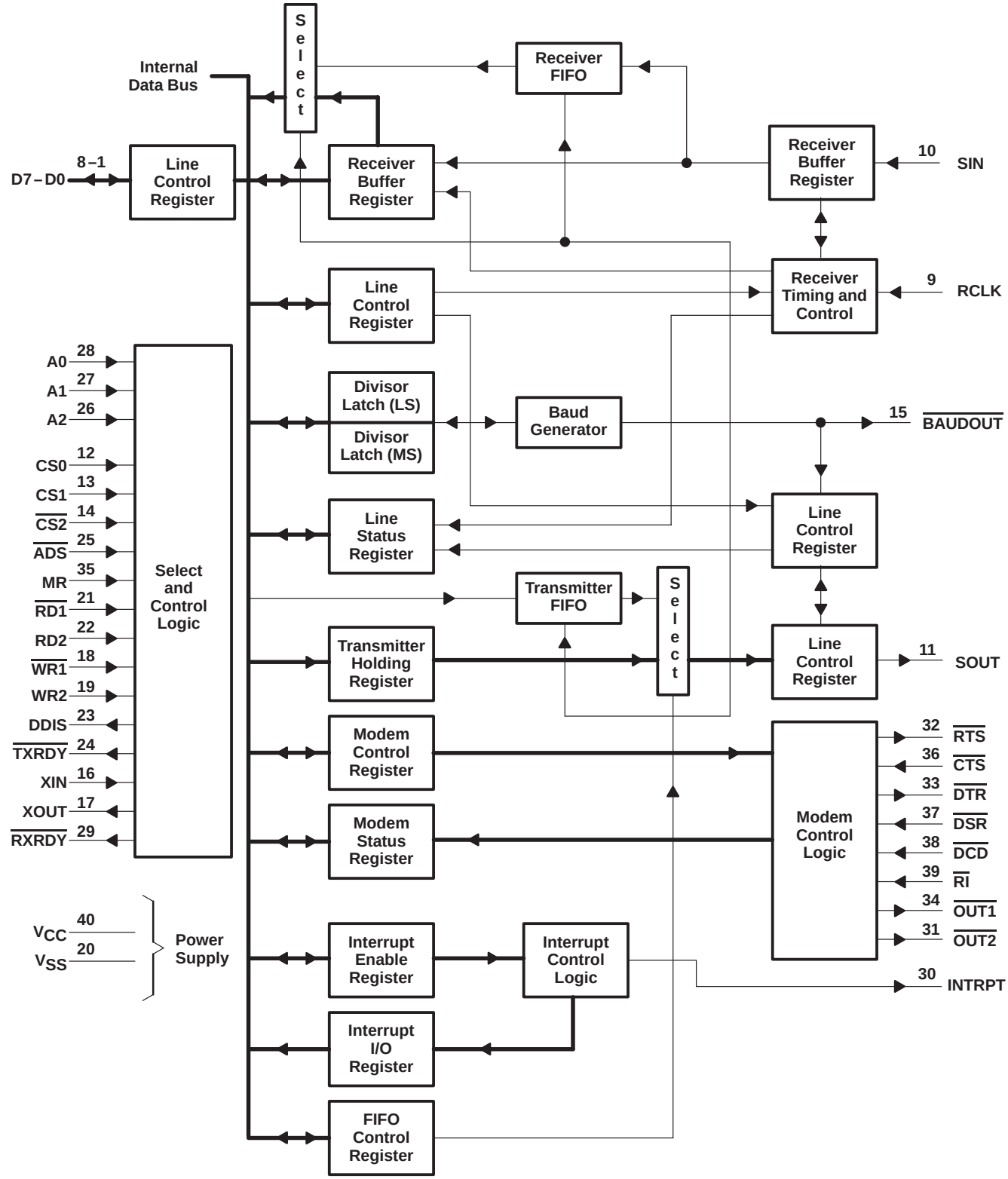
FN PACKAGE
(TOP VIEW)



NC – No internal connection

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block diagram



NOTE A: Terminal numbers shown are for the N package.

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Terminal Functions

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
A0 A1 A2	28 [31] 27 [30] 26 [29]	I	Register select. A0, A1, and A2 are used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the address strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25 [28]	I	Address strobe. When $\overline{ADS}$ is active (low), the register select signals (A0, A1, and A2) and chip select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the register select and chip select signals are held in the state they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15 [17]	O	Baud out. $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
CS0 $\overline{CS1}$ $\overline{CS2}$	12 [14] 13 [15] 14 [16]	I	Chip select. When CSx is active (high, high, and low respectively), the ACE is selected. If any of these inputs are inactive, the ACE remains inactive. Refer to the $\overline{ADS}$ (address strobe) signal description.
$\overline{CTS}$	36 [40]	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 – D7	1 – 8 [2 – 9]	I/O	Data bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38 [42]	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (DDCD) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	23 [26]	O	Driver disable. This output is active (high) when the CPU is not reading data. When active, this output can disable an external transceiver.
$\overline{DSR}$	37 [41]	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33 [37]	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a master reset or during loop mode operation or clearing bit 0 (DTR) of the modem control register.
INTRPT	30 [33]	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data is available or timeout (FIFO mode only), transmitter holding register empty, or an enabled modem status interrupt. The INTRPT output is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35 [39]	I	Master reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2.
$\overline{OUT1}$ $\overline{OUT2}$	34 [38] 31 [35]	O	Outputs 1 and 2. $\overline{OUT1}$ and $\overline{OUT2}$ are user-designated output terminals that are set to their active states by setting their respective modem control register bits (OUT1 and OUT2) high. $\overline{OUT1}$ and $\overline{OUT2}$ are set to their inactive (high) states as a result of master reset or during loop mode operations or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the modem control register.
RCLK	9 [10]	I	Receiver clock. RCLK is the 16× baud rate clock for the receiver section of the ACE.
$\overline{RD1}$ RD2	21 [24] 22 [25]	I	Read inputs. When either $\overline{RD1}$ or RD2 are active (high or low respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., RD2 tied low or $\overline{RD1}$ tied high).

† Terminal numbers shown in brackets are for the FN package.

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Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
$\overline{RI}$	39 [43]	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32 [36]	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to transmit data. $\overline{RTS}$ is set to its active state by setting the RTS modem control register bit, and is set to its inactive (high) state either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the modem control register.
$\overline{RXRDY}$	29 [32]	O	Receiver ready output. Receiver direct memory access (DMA) signalling is available with $\overline{RXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected with FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR0 = 0 or FCR0 = 1, FCR3 = 0), if there is at least 1 character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ is active (low). When RXRDY has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). In DMA mode 1 (FCR0 = 1, FCR3 = 1), when the trigger level or the timeout has been reached, $\overline{RXRDY}$ goes active (low); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (high).
SIN	10 [11]	I	Serial input. SIN is a serial data input from a connected communications device.
SOUT	11 [13]	O	Serial output. SOUT is a composite serial data output to a connected communication device. SOUT is set to the marking (high) state as a result of master reset.
$\overline{TXRDY}$	24 [27]	O	Transmitter ready output. Transmitter DMA signalling is available with $\overline{TXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected with FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	40 [44]		5-V supply voltage
V_{SS}	20 [22]		Supply common
$\overline{WR1}$ WR2	18 [20] 19 [21]	I	Write inputs. When either $\overline{WR1}$ or WR2 are active (high or low respectively) while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., WR2 tied low or $\overline{WR1}$ tied high).
XIN XOUT	16 [18] 17 [19]	I/O	External clock. XIN and XOUT connect the ACE to the main timing reference (clock or crystal).

† Terminal numbers shown in brackets are for the FN package.

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absolute maximum ratings over free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range at any input, V_I . . . . . –0.5 V to 7 V
Output voltage range, V_O . . . . . –0.5 V to 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	–0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = –1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			±10	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kbit/s			10	mA
C_{XIN}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, All other terminals grounded, f = 1 MHz, T_A = 25°C		15	20	pF
C_{XOUT}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XOUT.

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system timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC		175		ns
t_{w5}	Pulse duration, $\overline{ADS}$ low	t_{ADS}	2, 3	15		ns
t_{w6}	Pulse duration, write strobe	t_{WR}	2	80		ns
t_{w7}	Pulse duration, read strobe	tRD	3	80		ns
t_{w8}	Pulse duration, master reset	t_{MR}		1		µs
t_{su1}	Setup time, address valid before $\overline{ADS}\uparrow$	t_{AS}	2, 3	15		ns
t_{su2}	Setup time, CS before $\overline{ADS}\uparrow$	t_{CS}	2, 3	15		ns
t_{su3}	Setup time, data valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{DS}	2	15		ns
t_{h1}	Hold time, address low after $\overline{ADS}\uparrow$	t_{AH}	2, 3	0		ns
t_{h2}	Hold time, CS valid after $\overline{ADS}\uparrow$	t_{CH}	2, 3	0		ns
t_{h3}	Hold time, CS valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WCS}	2	20		ns
t_{h4}§	Hold time, address valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WA}	2	20		ns
t_{h5}	Hold time, data valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{DH}	2	15		ns
t_{h6}	Hold time, CS valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RCS}	3	20		ns
t_{h7}§	Hold time, address valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RA}	3	20		ns
t_{d4}§	Delay time, CS valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{CSW}	2	15		ns
t_{d5}§	Delay time, address valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{AW}	2	15		ns
t_{d6}§	Delay time, write cycle, $\overline{WR1}\uparrow$ or WR2$\downarrow$ to $\overline{ADS}\downarrow$	t_{WC}	2	80		ns
t_{d7}§	Delay time, CS valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{CSR}	3	15		ns
t_{d8}§	Delay time, address valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{AR}	3	15		ns
t_{d9}	Delay time, read cycle, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to $\overline{ADS}\downarrow$	tRC	3	80		ns

§ Applicable only when $\overline{ADS}$ is tied low.

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high	t_{XH}	1	f = 9 MHz maximum	50		ns
t_{w2}	Pulse duration, clock low	t_{XL}	1	f = 9 MHz maximum	50		ns
t_{d10}	Delay time, $\overline{RD1}\downarrow$ or RD2$\uparrow$ to data valid	t_{RVD}	3	C_L = 100 pF		60	ns
t_{d11}	Delay time, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to floating data	t_{HZ}	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Disable time, $\overline{RD1}\downarrow\uparrow$ or RD2$\uparrow\downarrow$ to DDIS$\uparrow\downarrow$	t_{RDD}	3	C_L = 100 pF		60	ns

NOTE 2: Charge and discharge time is determined by V_{OL}, V_{OH}, and external loading.

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	t_{LW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	80		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	t_{HW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	100		ns
t_{d1}	Delay time, XIN$\uparrow$ to $\overline{BAUDOUT}\uparrow$	t_{BLD}	1	C_L = 100 pF		125	ns
t_{d2}	Delay time, XIN$\uparrow\downarrow$ to $\overline{BAUDOUT}\downarrow$	t_{BHD}	1	C_L = 100 pF		125	ns

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receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample clock	t_{SCD}	4			100	ns
t_{d13}	Delay time, stop to set RCV error interrupt or read RBR to LSI interrupt or stop to $\overline{\text{RXRDY}}\downarrow$	t_{SINT}	4,5,6,7,8			1	RCLK cycles
t_{d14}	Delay time, read RBR/LSR to reset interrupt	t_{RINT}	4,5,6,7,8	C_L = 100 pF		150	ns

NOTE 3: In FIFO mode RC = 425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, INTRPT to transmit start	t_{IRS}	9		8	24	baudout cycles
t_{d16}	Delay time, start to interrupt	t_{STI}	9		8	8	baudout cycles
t_{d17}	Delay time, WR THR to reset interrupt	t_{HR}	9	C_L = 100 pF		140	ns
t_{d18}	Delay time, initial write to interrupt (THRE)	t_{SI}	9		16	32	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	t_{IR}	9	C_L = 100 pF		140	ns
t_{d20}	Delay time, write to TXRDY inactive	t_{WXI}	10,11	C_L = 100 pF		195	ns
t_{d21}	Delay time, start to TXRDY active	t_{SXA}	10,11	C_L = 100 pF		8	baudout cycles

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d22}	Delay time, WR MCR to output	t_{MDO}	12	C_L = 100 pF		100	ns
t_{d23}	Delay time, modem interrupt to set interrupt	t_{SIM}	12	C_L = 100 pF		170	ns
t_{d24}	Delay time, RD MSR to reset interrupt	t_{RIM}	12	C_L = 100 pF		140	ns

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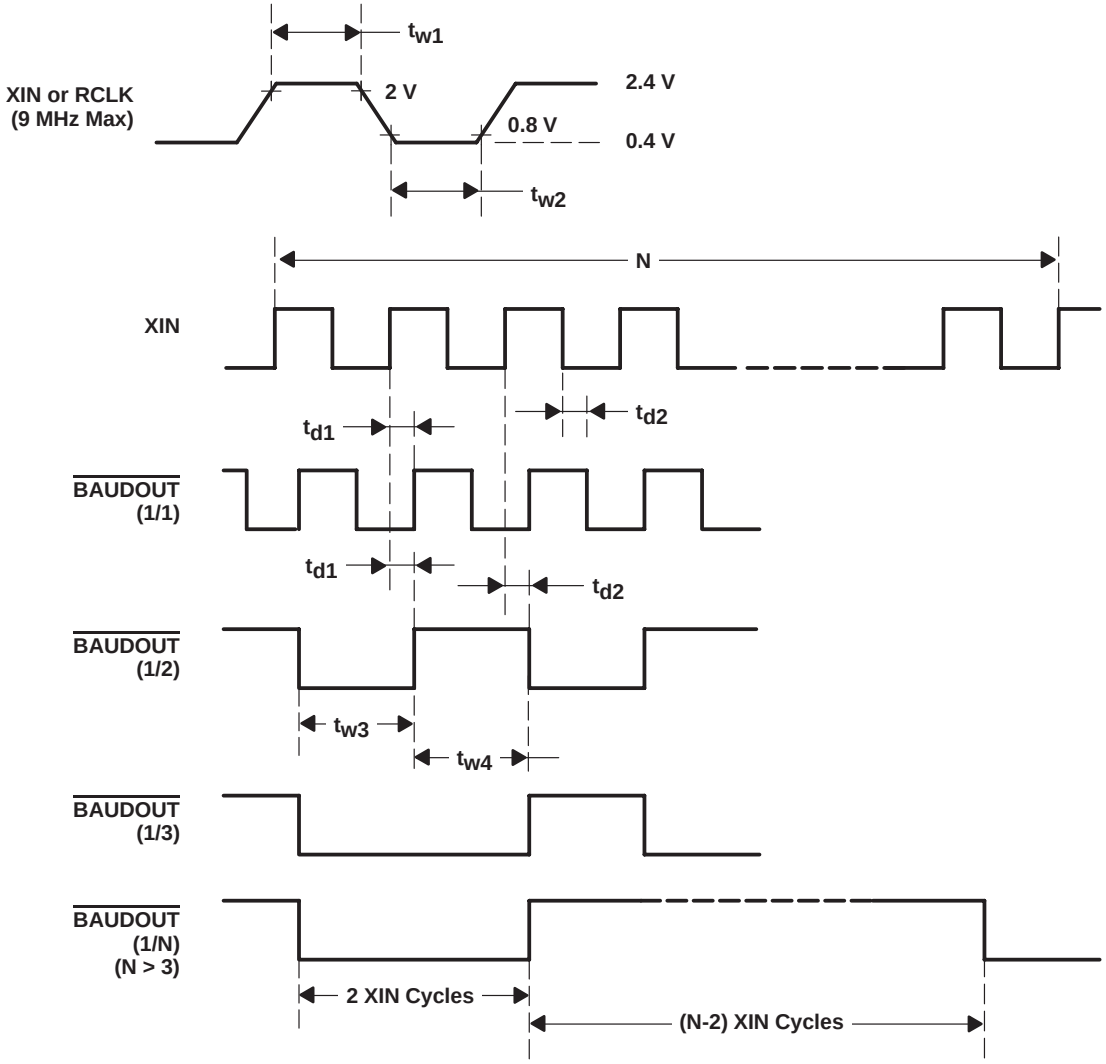
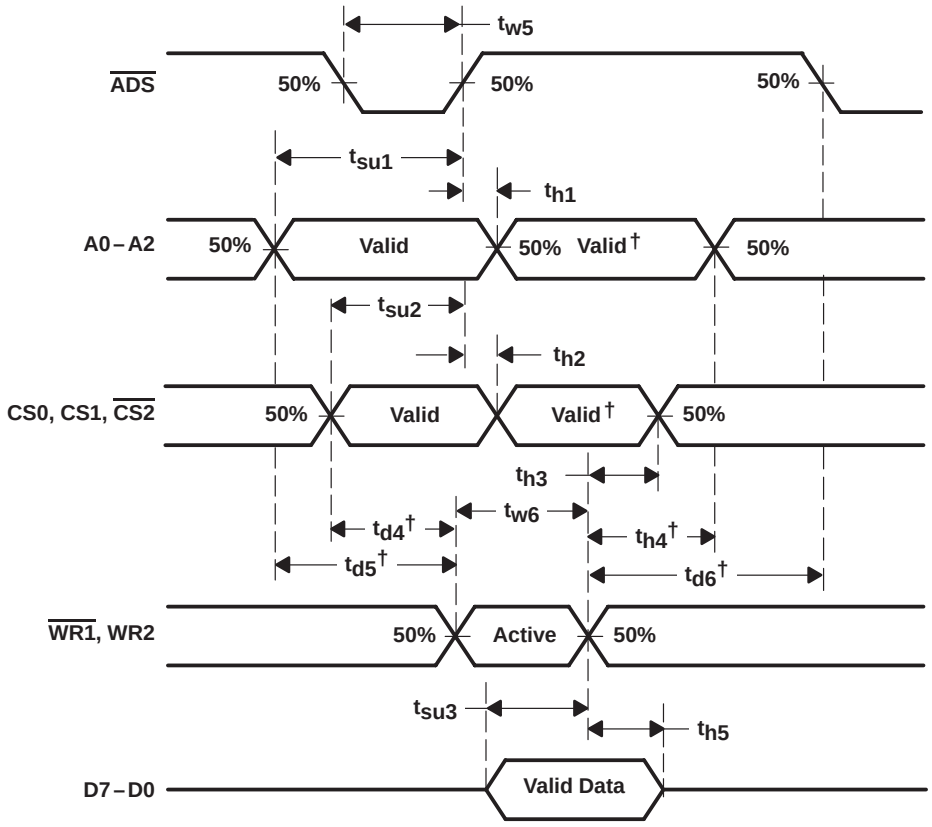


Figure 1. Baud Generator Timing Waveforms

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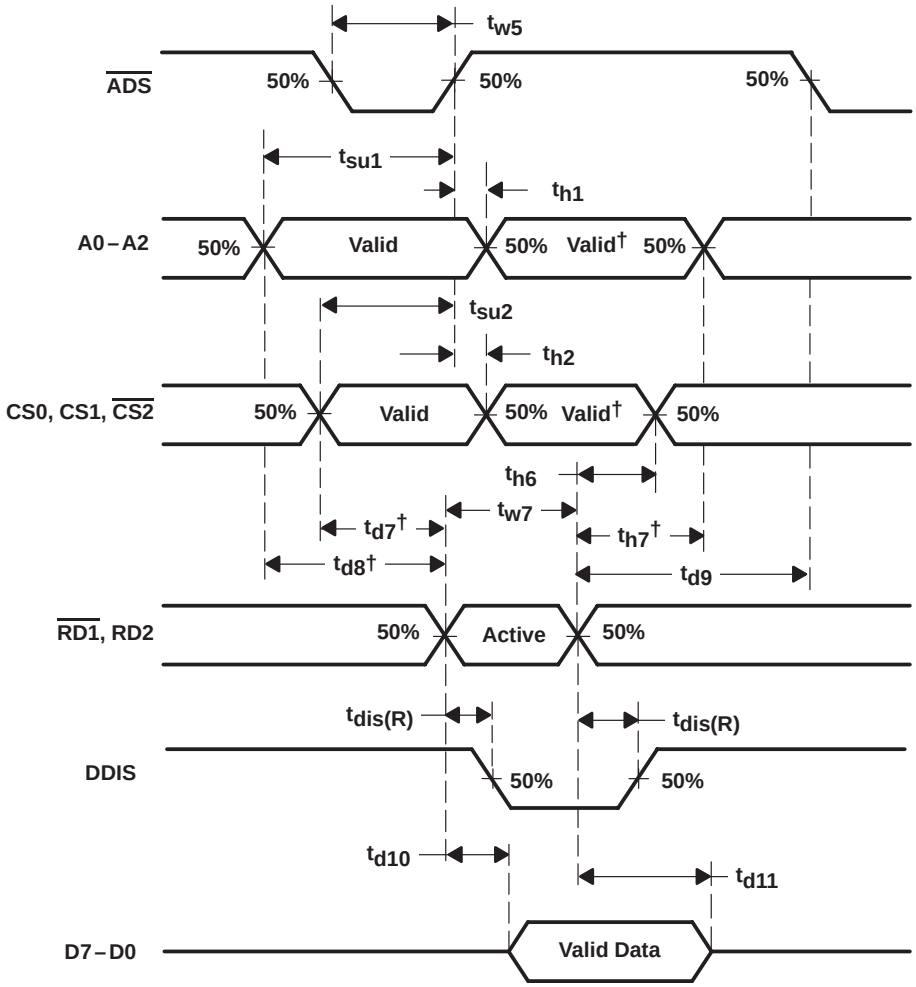


† Applicable only when $\overline{\text{ADS}}$ is tied low.

Figure 2. Write Cycle Timing Waveforms

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† Applicable only when $\overline{\text{ADS}}$ is tied low.

Figure 3. Read Cycle Timing Waveforms

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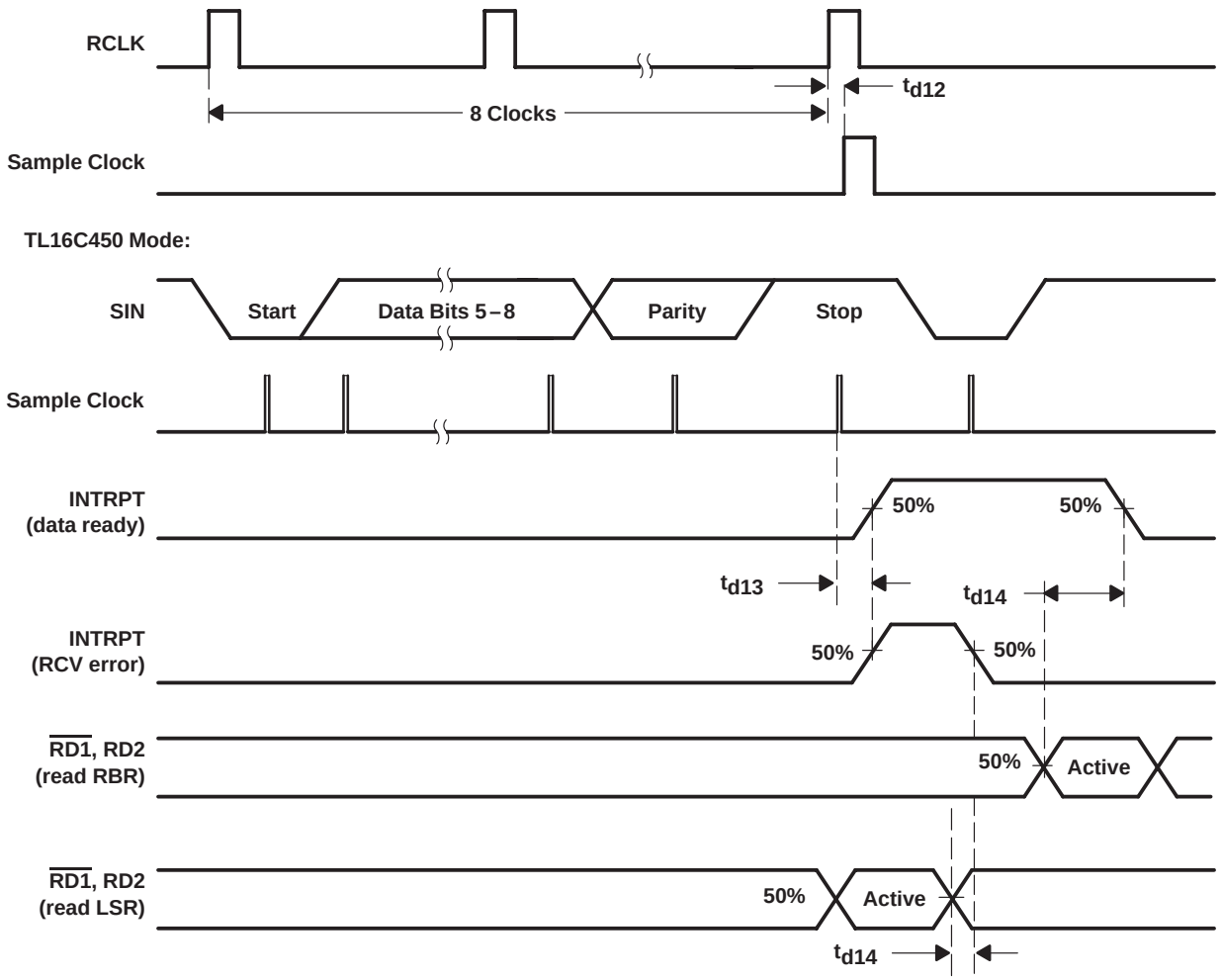
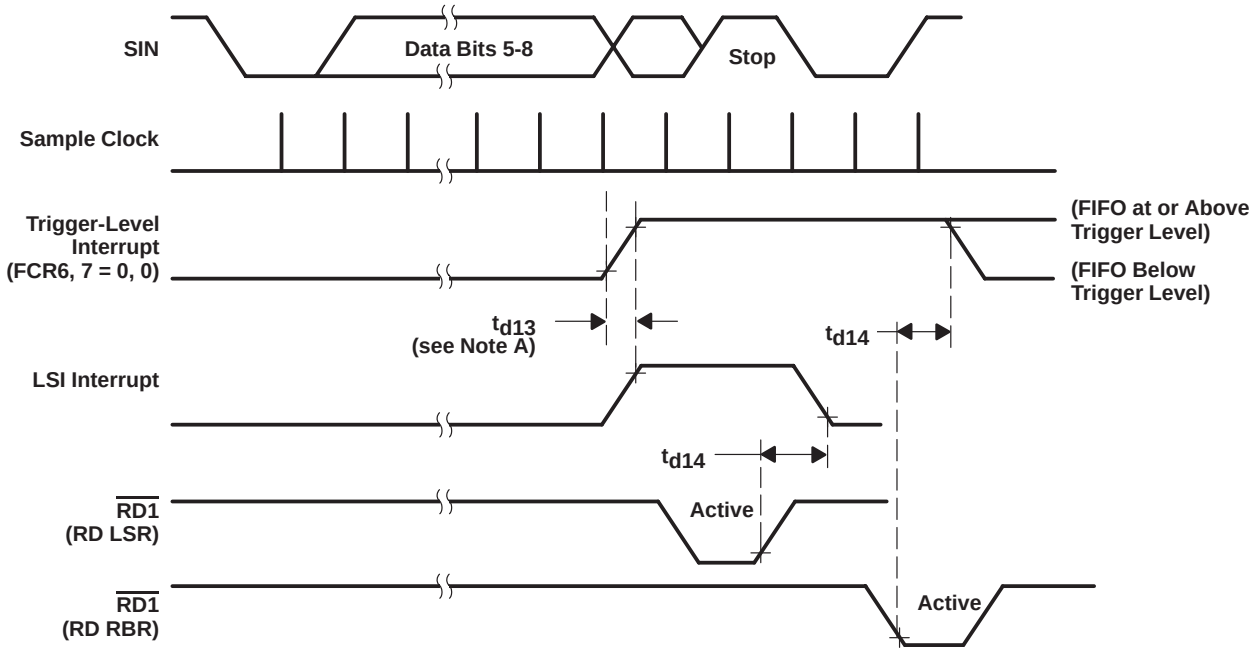


Figure 4. Receiver Timing Waveforms

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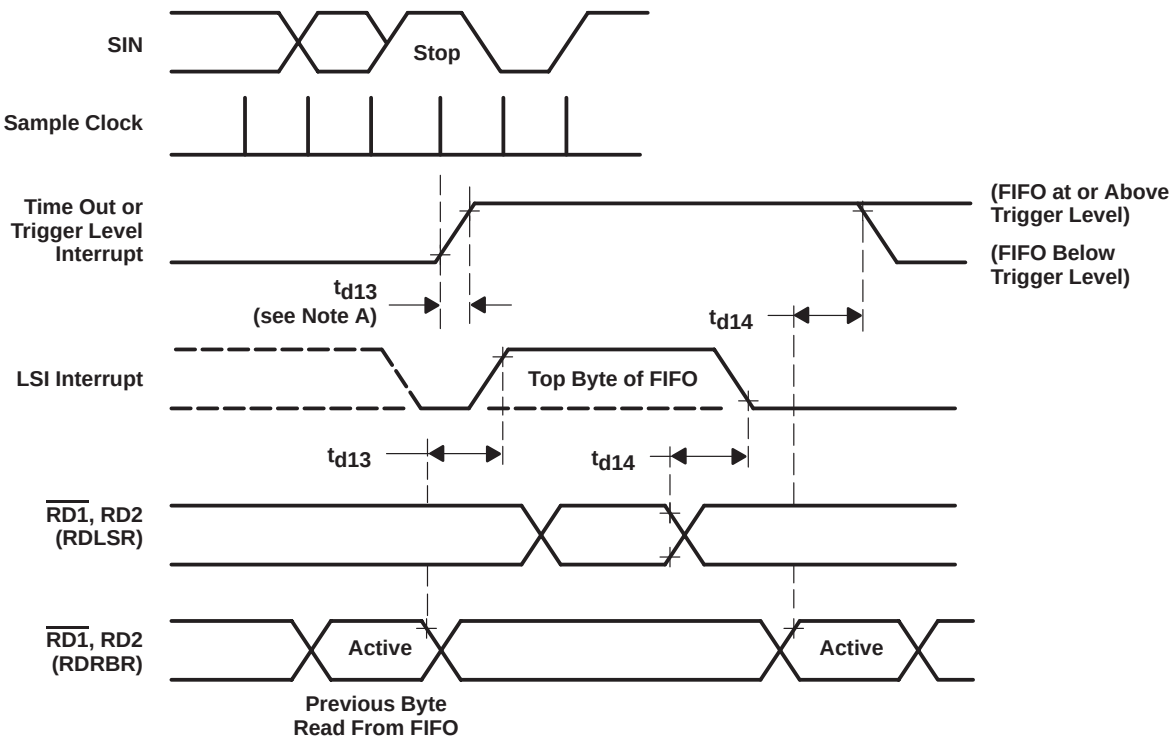
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NOTE A: For a timeout interrupt, t_{d13} = 8 RCLKs.

Figure 5. Receiver FIFO First Byte (Sets DR Bit) Waveforms

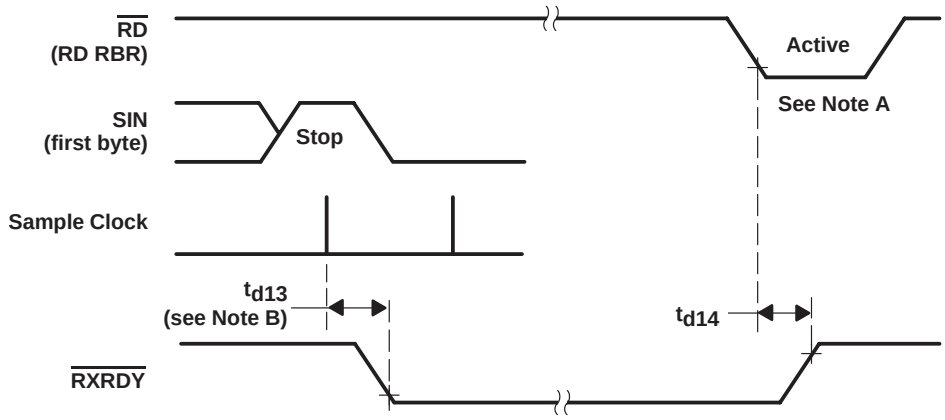


NOTE A: For a timeout interrupt, t_{d13} = 8 RCLKs.

Figure 6. Receiver FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

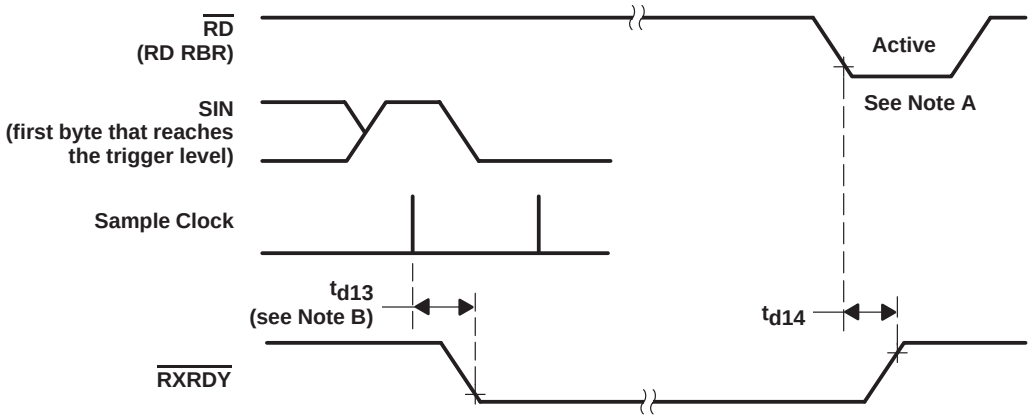
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NOTES: A. This is the reading of the last byte in the FIFO.
B. For a timeout interrupt, t_{d13} = 8 RCLKs.

Figure 7. Receiver Ready ($\overline{\text{RXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (mode 0)



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a timeout interrupt, t_{d13} = 8 RCLKs.

Figure 8. Receiver Ready ($\overline{\text{RXRDY}}$) Waveforms, FCR = 1 or FCR3 = 1 (mode 1)

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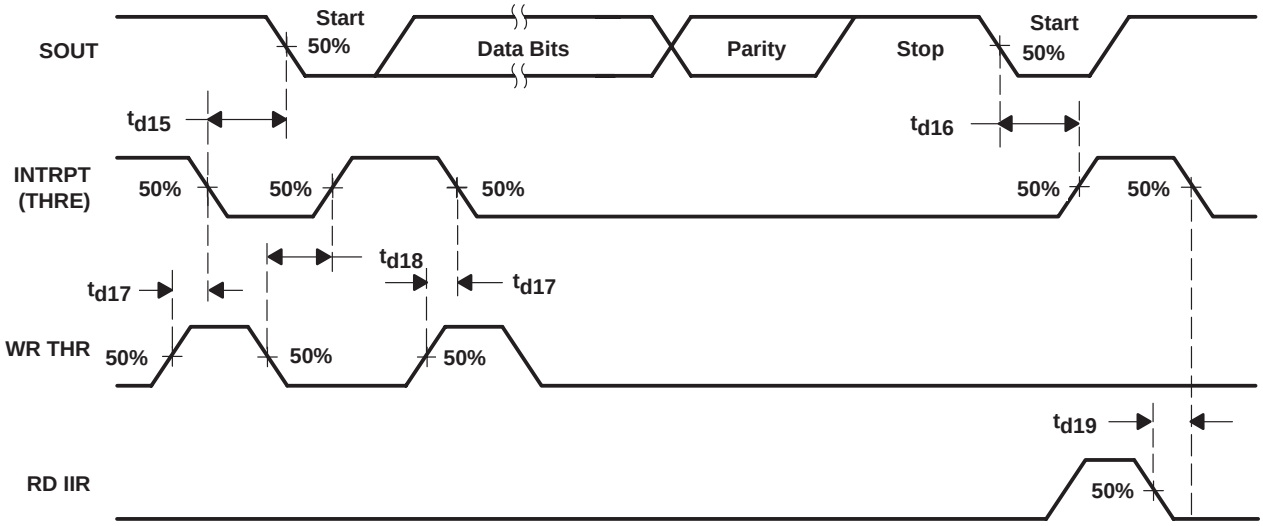


Figure 9. Transmitter Timing Waveforms

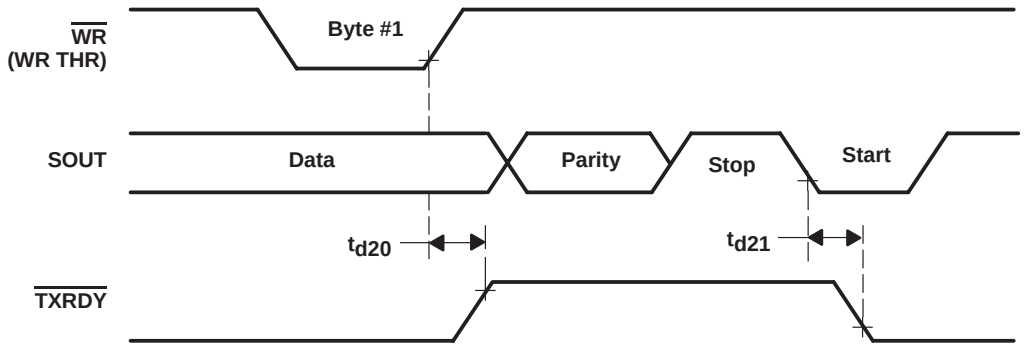


Figure 10. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (mode 0)

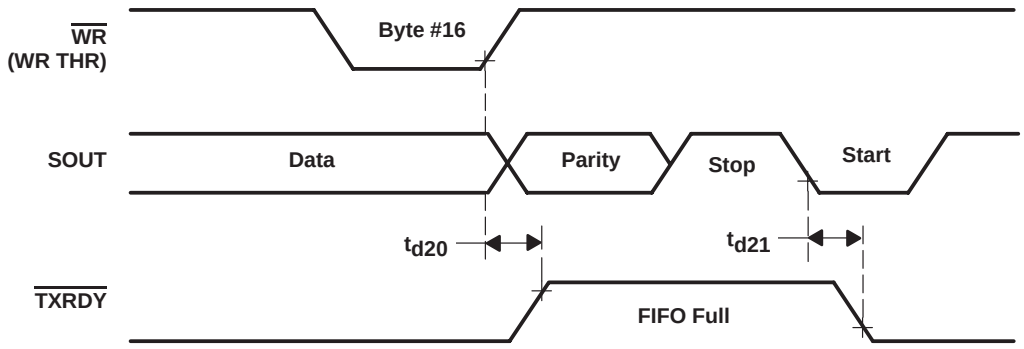


Figure 11. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 1 and FCR3 = 1 (mode 1)

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PARAMETER MEASUREMENT INFORMATION

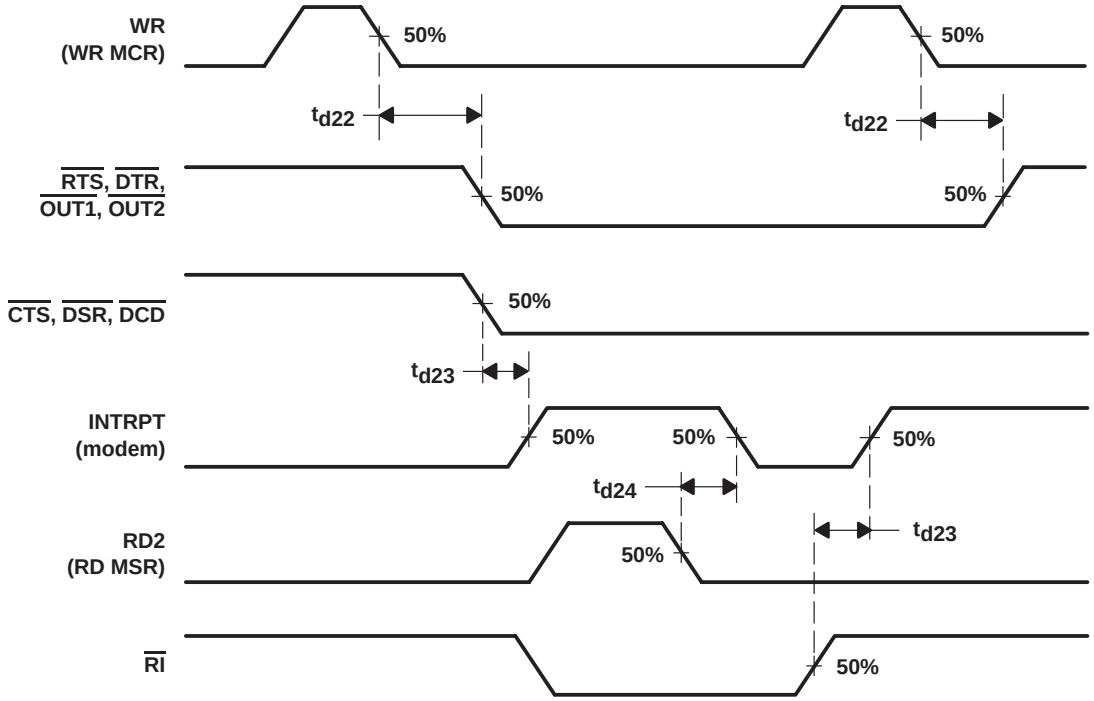


Figure 12. Modem Control Timing Waveforms

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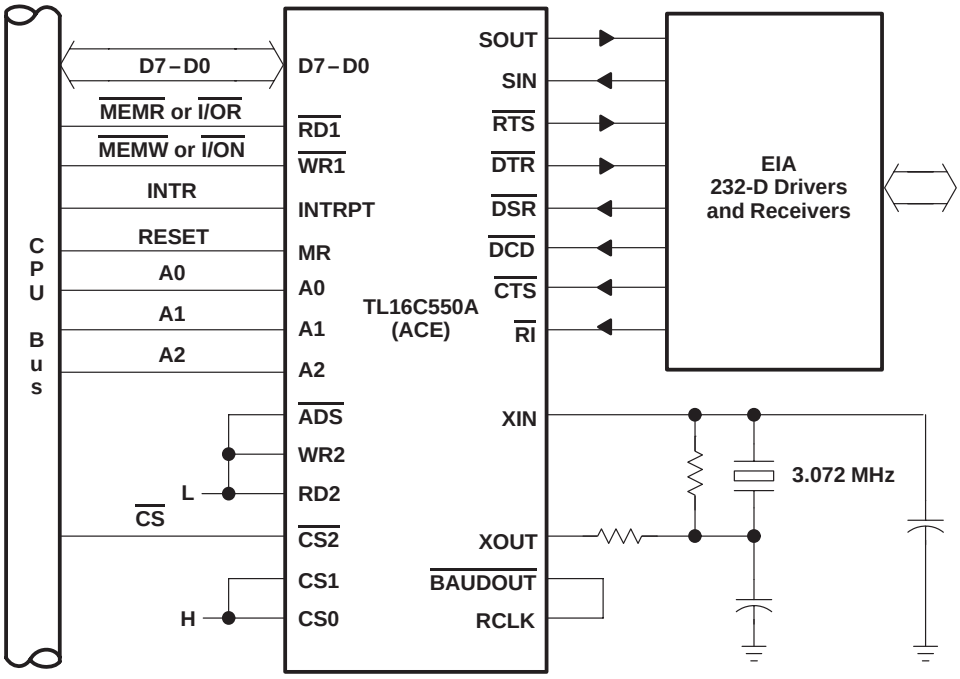


Figure 13. Basic TL16C550A Configuration

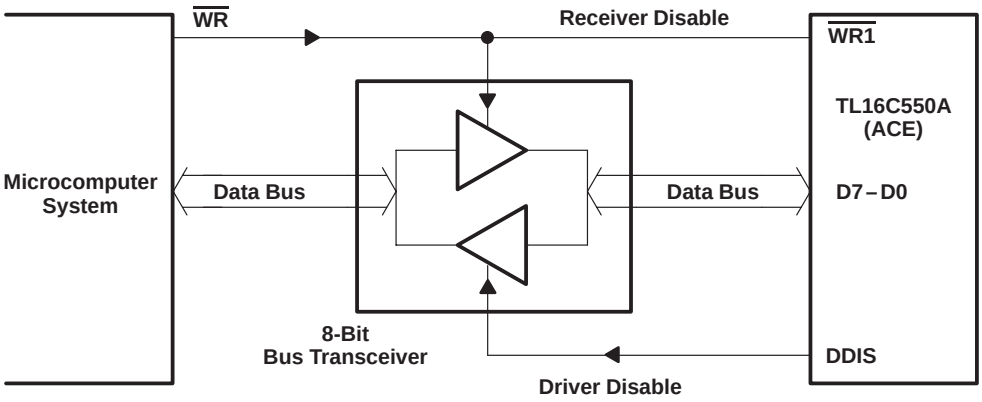
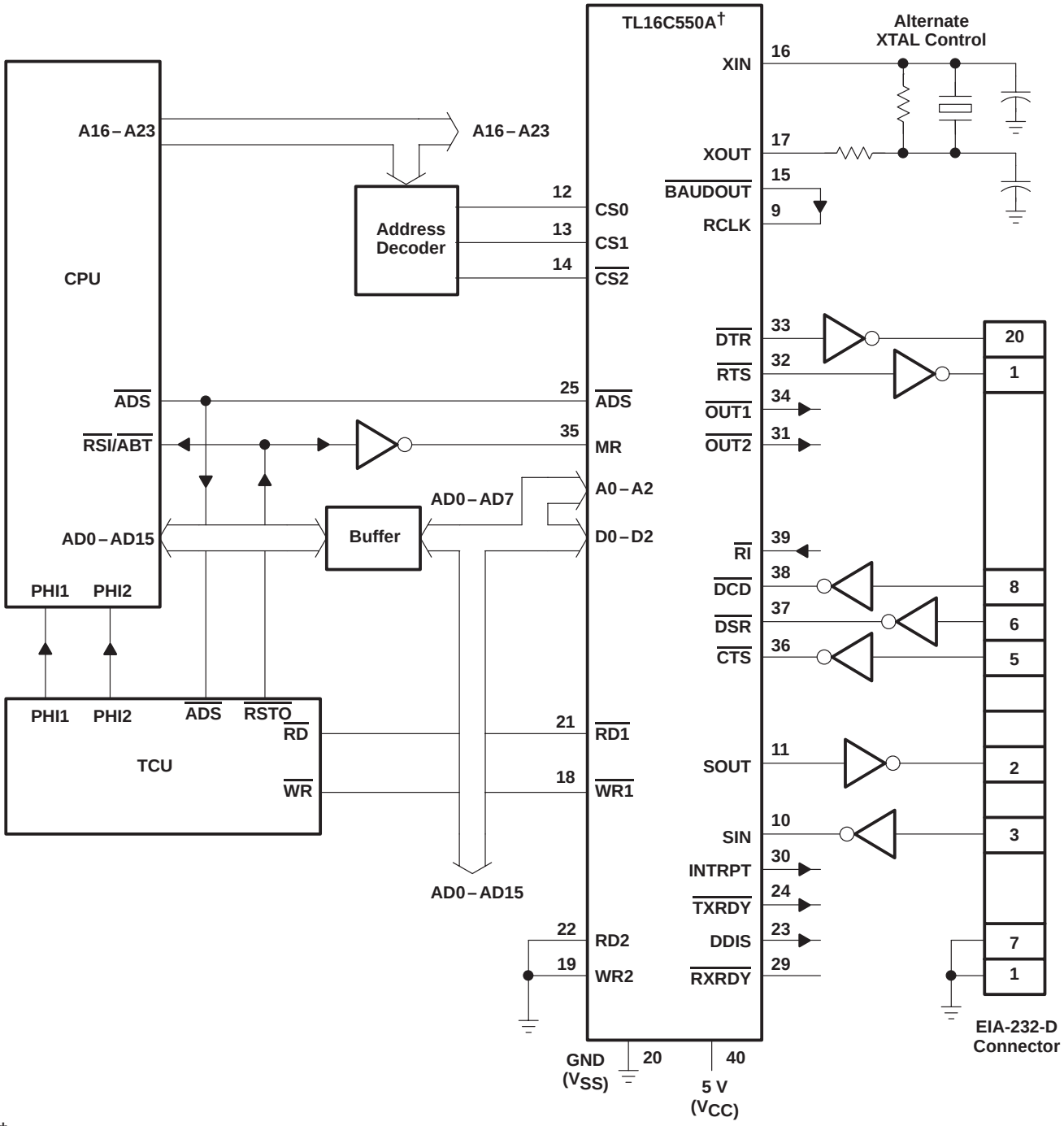


Figure 14. Typical Interface for a High-Capacity Data Bus

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† Terminal numbers for the TL16C550A are for the N package.

Figure 15. Typical TL16C550A Connection to a CPU

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PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is set, bits 1–3 are cleared, and bits 4–7 are permanently cleared
FIFO Control Register	Master Reset	All bits cleared
Line Control Register	Master Reset	All bits cleared
Modem Control Register	Master Reset	All bits cleared (5–7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are set, all other bits are cleared
Modem Status Register	Master Reset	Bits 0–3 are cleared, bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{\text{OUT2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT1}}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Registers	Master Reset	No effect
Transmitter Holding Registers	Master Reset	No effect
RCVR FIFO	MR/FCR1-FCR0/ ΔFCR0	All bits low
XMIT FIFO	MR/FCR2-FCR0/ ΔFCR0	All bits low

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PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERB)	”0“ If Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Transmitter FIFO Reset	Number of Stop Bits (STB)	Out1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 4)	DMA Mode Select	Parity Enable (PEN)	Out2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 4)	Receiver Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 4)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 4)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
NOTE 4: These bits are always cleared in the TL16C450 mode.

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PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables the FIFOs, clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

- Bit 0: This bit (FCR0), when set, enables the transmit and receive FIFOs. Bit 0 must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: This bit (FCR1), when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 2: This bit (FCR2), when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 3: When this bit (FCR0) and FCR3 are set, $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ change from mode 0 to mode 1.
- Bits 4 and 5: These two bits (FCR4 and FCR5) are reserved for future use.
- Bits 6 and 7: These two bits (FCR6 and FCR7) set the trigger level for the receiver FIFO interrupt. Table 4 shows the trigger level for the receiver FIFO interrupt.

Table 4. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1) receiver interrupts occur as follows:

1. The receive data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared as soon as the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and, like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled, receiver FIFO timeout interrupts occur as follows:

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FIFO interrupt mode operation (continued)

1. FIFO timeout interrupt occurs when the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character received was longer than 4 continuous character times ago (when 2 stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO was longer than 4 continuous character times ago. This causes a maximum character received to interrupt issued delay of 160 ms at 300 baud with 12-bit characters.
2. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
3. When a timeout interrupt has occurred, it is cleared and the timer reset when the microprocessor reads one character from the receiver FIFO.
4. When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The THR interrupt (02) occurs when the transmit FIFO is empty. It is cleared as soon as the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmit FIFO empty indications are delayed 1 character time minus the last stop bit time when the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate, if it is enabled.

Character timeout interrupt and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt. The transmit FIFO empty interrupt has the same priority as the current THRE interrupt.

FIFO polled mode operation

When FCR0 is set, clearing IER0, IER1, IER2, IER3, or all four puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks the receiver and transmitter status using the LSR.

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 – LSR4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode and the IIR is not affected since IER2 = 0.
- LSR5 indicates when the transmit FIFO is empty.
- LSR6 indicates that both the transmit FIFO and shift registers are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or timeout conditions indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

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interrupt enable register (IER)

The IER enables each of the four types of interrupts (refer to Table 5) and the INTRPT output signal in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit, when set, enables the received data available interrupt.
- Bit 1: This bit, when set, enables the THRE interrupt.
- Bit 2: This bit, when set, enables the receiver line status interrupt.
- Bit 3: This bit, when set, enables the modem status interrupt.
- Bits 4 – 7: These bits in the IER are not used and are always cleared.

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and the type of interrupt is defined by the interrupt's three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4. Details of each bit are as follows:

- Bit 0: This bit can be used either in a hardwire prioritized or polled interrupt system. When this bit is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 5.
- Bit 3: This bit is always cleared in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a timeout interrupt is pending.
- Bits 4 thru 5: These two bits are not used and are always cleared.
- Bits 6 and 7: These two bits are always cleared in the TL16C450 mode. They are set when bit 0 of the FCR is set.

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interrupt identification register (IIR) (continued)

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER (IIR)				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	–
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Reading the line status register (LSR)
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode.	Reading the receiver buffer register (RBR)
1	1	0	0	2	Character timeout indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time	Reading the receiver buffer register (RBR)
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt identification register (IIR) (if source of interrupt) or writing into the transmitter holding register (THR)
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register (MSR)

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 6.

Table 6. Serial Character Word Length

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks the first stop bit only, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in Table 7.

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line control register (LCR) (continued)

Table 7. Number of Stop Bits Generated

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in the transmitted data between the last data word bit and the first stop bit. In received data, when bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic 1's in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. When bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition, i.e., a condition where the serial output (SOUT) terminal is forced to the spacing (low) state. When bit 6 is cleared, the break condition is disabled. The break condition has no affect on the transmitter logic; it only affects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are described in the following bulleted list and summarized in Table 3.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. Bit 0 is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO and is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: This bit is the overrun error (OE) indicator. When bit 1 is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. The OE indicator is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten but is not transferred to the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment
‡ Bits 1 through 4 are the error conditions that produce a receiver line status Interrupt.

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line status register (LSR)† (continued)

- Bit 2‡: This bit is the parity error (PE) indicator. When bit 2 is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). The PE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3‡: This bit is the framing error (FE) indicator. When bit 3 is set, it indicates that the received character did not have a valid (set) stop bit. The FE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE then samples this start bit twice and then accepts the input data.
- Bit 4‡: This bit is the break interrupt (BI) indicator. When bit 4 is set, it indicates that the received data input was held clear for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only the 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. Bit 5 is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is set, then an interrupt is generated. THRE is set when the contents of the THR are transferred to the transmitted shift register. This bit is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. Bit 6 is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, the TEMT bit is cleared. In the FIFO mode, this bit is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550A, this bit is always cleared. In the TL16C450 mode, this bit is cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the data terminal ready ($\overline{\text{DTR}}$) output. Setting bit 0 forces the $\overline{\text{DTR}}$ output to its low state. When bit 0 is cleared, $\overline{\text{DTR}}$ goes high.
- Bit 1: This bit (RTS) controls the request to send ($\overline{\text{RTS}}$) output in a manner identical to bit 0's control over the $\overline{\text{DTR}}$ output.
- Bit 2: This bit (OUT1) controls the output 1 ($\overline{\text{OUT1}}$) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{\text{DTR}}$ output.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

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modem control register (MCR) (continued)

- Bit 3: This bit (OUT2) controls the output 2 ($\overline{OUT2}$) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When bit 4 is set, the following occurs:

  1. The SOUT is set high.
  2. The SIN is disconnected.
  3. The output of the TSR is looped back into the RSR input.
  4. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
  5. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs.
  6. The four modem control output terminals are forced to their inactive states (high).

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

- Bit 5 – 7: These bits are permanently cleared.

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the change in clear to send (ΔCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input has changed states since the last time it was read by the CPU . When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 1: This bit is the change in data set ready (ΔDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of ring indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 3: This bit is the change in data carrier detect (ΔDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the compliment of the clear to send ($\overline{CTS}$) input. When bit 4 (loop) of the MCR is set, bit 4 is equivalent to the MCR bit 1 (RTS).
- Bit 5: This bit is the compliment of the data set ready ($\overline{DSR}$) input. When bit 4 (loop) of the MCR is set, bit 5 is equivalent to the MCR bit 1 (DTR).

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modem status register (MSR) (continued)

- Bit 6: This bit is the compliment of the ring indicator ($\overline{RI}$) input. When bit 4 (loop) of the MCR is set, bit 6 is equivalent to the MCR bit 2 (OUT1).
- Bit 7: This bit is the compliment of the data carrier detect ($\overline{DCD}$) input. When bit 4 (loop) of the MCR is set, bit 7 is equivalent to the MCR bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 8 MHz and divides it by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16× the baud rate. The formula for the divisor is:

divisor # = XIN frequency input ÷ (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 8 and 9, which follow, illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively For baud rates of 38.4 kbit/s and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 16 for examples of typical clock circuits.

Table 8. Baud Rates Using a 1.8432-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

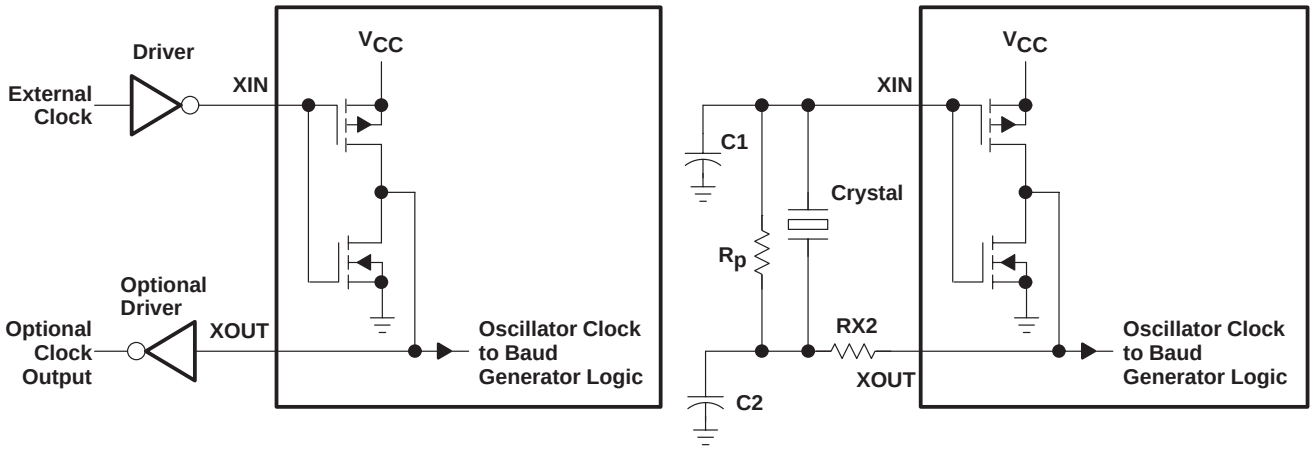
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programmable baud generator (continued)

Table 9. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	R_P	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 16. Typical Clock Circuits

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receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACEs RSR receives serial data from the SIN terminal. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. in the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

scratch register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is suppled by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off the internal data bus and, when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at the serial output (SOUT). In the TL16C450 mode, when the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

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