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Model 4261

12-bit 10 MHz, or 14-bit 5 MHz A/D Converter VME Board



Features

- 12-bit resolution at 10 MHz, or 14-bit resolution at 5 MHz
- 2 or 8 Msample buffer memory
- Programmable sample rate
- Parallel digital output interface

Ordering Information

Model	Description
4261	12-bit 10 MHz A/D, 2 Msample RAM
Options:	
-001	Same with Tag RAM
-002	8 Msample RAM
-010	14-bit 5 MHz A/D, 2 Msample RAM

General Information

The Model 4261 is a wideband high performance A/D converter board for VMEbus. It may be used either as a front end for Pentek's VMEbus MIX subsystems or as a standalone general purpose data acquisition board for VMEbus.

High-speed Conversion

Model 4261 provides an integrated sample-and-hold and A/D converter delivering 12-bit resolution at 10 MHz. Option -010 provides 14-bit resolution at 5 MHz.

Flexible Buffer Memory

Two SRAM data buffers are arranged in a "swinging buffer" configuration. One buffer accepts data from the A/D converter, while the other delivers data to the VMEbus. When both buffers have completed their cycles, they are swapped for the next cycle.

The output buffer may also be directed to provide sequential samples to a front-panel 16-bit parallel TTL digital interface, delivering data at a rate compatible with the target device.

Two buffer memory sizes are available: 2 Msample (std) or 8 Msample (optional). The buffer size is programmable in steps of four samples.

Address Tag

An optional Tag RAM (Option -001) allows the user to "tag" variable-length blocks of output samples with a 4-bit address field specifying the destination device.

Sampling Rate Control

Sampling rates are derived from either the internal 10 MHz crystal oscillator or an external TTL clock into a front panel BNC. A programmable divide-by-N counter can be used with either clock source. An external TTL trigger can be used to start conversion.

Specifications

Input signal: single-ended, ±1.0 V full scale; 50 ohms input impedance

A/D conversion: 10 MHz/12 bits, or 5 MHz/14 bits; in-band harmonics –72 dBc typ.; SNR 65/70 dB typ.; THD –68 dBc typ.; 2-tone IM distortion –75 dBc typ.

Sample rate generator: plug-in DIP oscillator or external TTL clock (front panel BNC); programmable divide-by-N, where N = integer from 1 to 65,535

Data buffer: 2 Msamples standard, or 8 Msamples optional

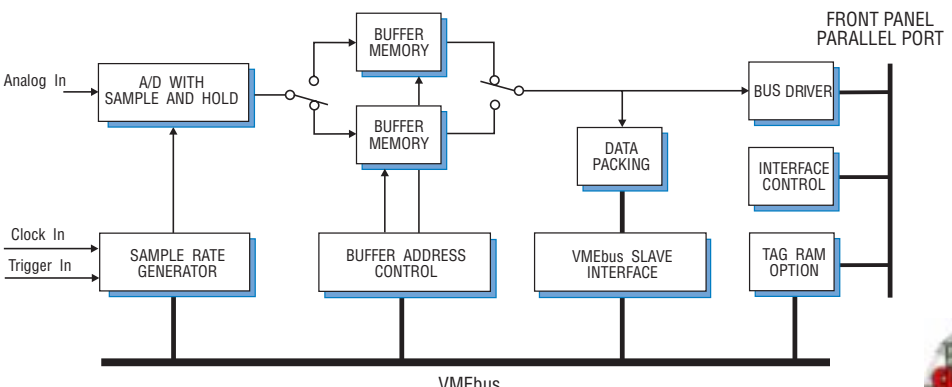
VMEbus interface: slave D32 A32, I(1-7); base address jumper selectable on any 2 MB boundary; A16 address space used for control/status registers and FIFO mode data output

Parallel interface: data output 16 bits TTL; Tag output 4 bits TTL; handshake lines 2 bits (NRFD and DAV); 50-pin DIL connector, front panel

Power: 3.9 A at +5 V; 0.3 A at +12 V; 0.6 A at –12 V; with option -001: 4.6 A at +5 V; 0.3 A at +12 V; 0.6 A at –12 V

Size: 6U board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide

Block Diagram, Model 4261



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