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OPERATING MANUAL

MODELS 4261 and 4261A

10 MHz, 12 bit and 5 MHz, 14 bit
A/D Converters for VMEbus Systems
with TAG RAM (4261A)

PENTEK

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Pentek Model 4261 Operating Manual - Revision History

Date	Rev	Applicable Serial #'s	Comments
12/12/91	A	9150001 - 9301001	Initial product release
06/15/92	B	9150001 - 9301001	Clarifications and error corrections. Around this time, separate manuals were also produced for the 4261A and the 4261 optioon 002.
04/29/94	C	9301001 - Forward	Unify all 4261 Manuals into one. Add JP8 jumper info and update Parallel Port info to include Free Run mode. Clarify RAM size table.
06/21/94	C.1	9301001 - Forward	Expand Tables 2-6 and 3-17 (identical tables - Block Size Jumpers) to include all available settings. Re-numbered pages in Appendices.
01/11/95	D	9301001 - Forward	Discourage direct RAM access. Move Parallel Port Operations Section from 3.4.8 (subsection of A16 registers) to new Section 3.8. Indicate that clock must be stopped before writing to FIFO (Section 3.4.10.2.) Changes to Figures 1-1 and 3-1 to show output FIFO. RAM is Read-Only in A24 and A32. New code examples in Appendix A. Move memory manipulation App Note to Appendix C. Add new Appendix B, 82C54 Data Sheet. Correct labeling of JP4 and JP5 in Fig. 2-1.
08/16/95	E	9301001 - Forward	Add documantation of new Option 019 - Direct front-panel output of A/D data. Material added as follows: Change to Fig. 1-1 (Block Diagram) to show direct data path; New Section (1.1.6) in Chapter 1; Option added to Ordering Info in Specs (Sec. 1.2); New Section in Chapter 2 (2.10), including 2 new tables (2-12 & 2-13) and 2 new Figures (2-11 and 2-12); Detailed Block Diagram (Fig 3-1) updated.
07/25/96	E.1	9301001 - Forward	Change Tables 2-10 and 2-12 such that pin 1 is at lower right of table, to match connector pinout. Change wording of last paragraph in Section 2.9.3 - $\overline{\text{NRFD}}$ can FLOAT high, pull-up not necessary. Change Sec. 2.10.1 and Fig. 2-12 - MUST drive A inputs of 4272-019 - pinout not compatible w/ Channel B. Add sections on inserting & Removing card from cage. Add Tables & Figures to Table of Contents.

The material presented in Appendix B of this manual is excerpted from Intel Corporation's data sheet for the 82C54 Programmable Interval Timer, Intel publication number 231244-005. A complete copy of this data sheet may be ordered from Intel Literature Sales., P. O. Box 7641, Mt. Prospect, IL, 60056-7641 (Phone: (800) 548-4725. Pentek gratefully extends its thanks to Intel for their permission to use this copyrighted material.

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Chapter 1: General Information

1.1 Introduction

Pentek's Model 4261 A/D Converter for VMEbus is a general purpose, high-speed data acquisition system with applications in digital signal processing, process control, FFT spectrum analysis, digital waveform capture, digital receivers, transient recording, and radar analysis. Depending upon the options ordered, the main features of the Model 4261 include either a 10 MHz, 12 bit or a 5.12 MHz, 14-bit A/D Converter, a 2, 8 or 32 Megasample Data Buffer, the VMEbus interface, and the Parallel Output Port.

The unit consists of a single 6U VMEbus board which occupies a single slot in the card cage and is fully compliant with a VMEbus specifications.

The Model 4261 is completely programmable over the VMEbus, including sampling rate, memory block length, interrupt mode, and output mode. Each of the operational sections of the unit will now be presented in some detail.

1.1.1 A/D Converter and Sample & Hold

The front end of a 10 MHz, 12-bit Model 4261 consists of a Burr Brown Model ADC603 integrated A/D Converter and Sample & Hold. The 5.12 MHz, 14-bit model uses the Burr-Brown Model ADC614. These are both complete hybrid devices which have been well characterized for ± ½ bit accuracy at sample rates up to their maximums.

The analog input is accepted by a front panel BNC connector. The input impedance is a 50Ω resistive load, with a full scale input voltage of ±1.00 V. A high performance wide-band amplifier (Burr Brown OPA620) buffers the signal before it is applied to the input of the ADC.

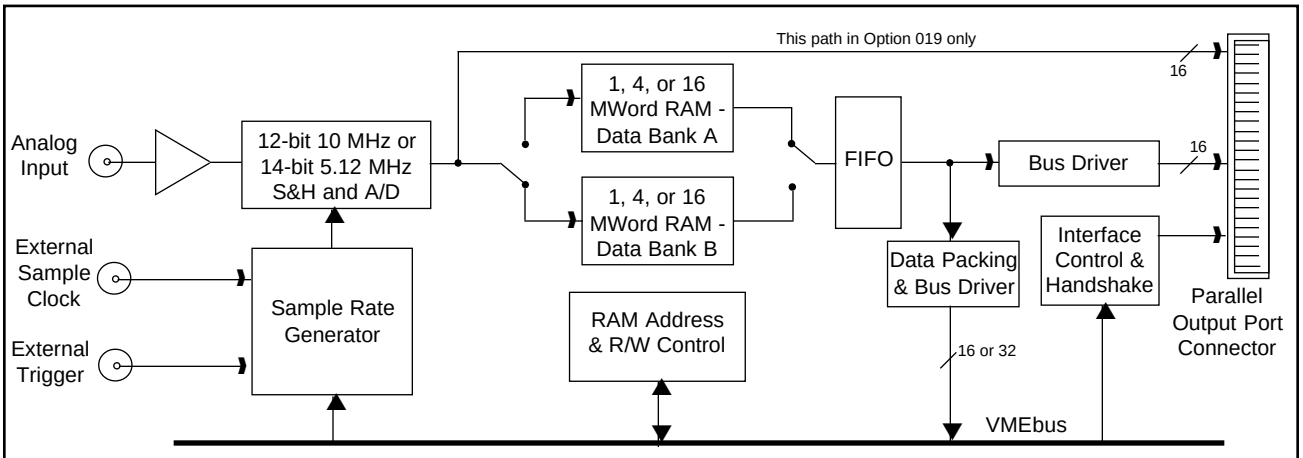


Figure 1-1: Model 4261A Block Diagram

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1.1 Introduction (continued)

1.1.1 A/D Converter and Sample & Hold (continued)

The sampling clock for the Model 4261 can come from any of four sources:

- Internal 10 MHz Oscillator (the 5.12 MHz unit uses 10.24 MHz ÷ 2)
- Internal 10 MHz Oscillator divided by N
- External TTL Clock Input
- External TTL Clock Input divided by N

The internal 10 MHz oscillator is in the form of a standard 14-pin DIP with a frequency stability of ±100 ppm. This device is socketed and can be replaced in the field with an oscillator at another frequency. These devices are quite readily available from numerous vendors in many off-the-shelf standard frequencies. Custom frequency units are very reasonably priced.

A front panel BNC accepts the external TTL sampling clock which can be used instead of the internal oscillator. The maximum input frequency is 10 MHz. Either the internal oscillator or the external sampling clock can be divided by an integer value (1 to 65,536) by a programmable divider circuit.

For synchronization of multiple 4261's, the external sampling clocks of each unit can be driven from a common source.

1.1.2 External Triggering

If selected, sampling can be controlled by a trigger generator which accepts an external TTL pulse. Either edge of this pulse can be used to start the sampling process. Alternately, the external trigger input can be used as a gate for the sampling clock.

1.1.3 Data RAM Memory

The Data RAM Memory in a standard Model 4261 consists of two independent and identical memory blocks, each consisting of twelve 1M x 1 DRAM's. This provides a total of 2 Megasamples of storage. In the Model 4261 option 002 (8 Megasample memory), uses 4M x 1 DRAMs, and the option 003 (32 Megasample memory) uses 16M x 1 DRAMs.

As is shown in the block diagram on the previous page, the two memory banks are arranged in the form of a "swinging buffer" or "ping-pong memory" configuration. One bank, acting as the input memory, is tied to the A/D converter output, accepting samples at the A/D sampling rate. The other bank, the output memory, is connected to either the Parallel Port or the VMEbus Interface, depending on the output mode. Data can be read out from the output bank at any rate up to 10 MHz.

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1.1 Introduction (continued)

1.1.3 Data RAM Memory (continued)

The control circuitry for the Data RAM is quite extensive and flexible. The Data RAM can be configured as a single-shot transient recorder. In this case, the banks are cleared under software control and sampling is started by an external (or programmed) trigger signal. Data collection continues until the bank is full or until a pre-programmed number of samples has been collected. Data can then be read out over the VMEbus for further processing.

For continuous data collection, the average data output rate must be equal to the sampling rate of the A/D converter. In this case, the Data RAM can be programmed to swap automatically when the input bank is full and the output bank is empty, without losing any data.

Some applications require bank sizes smaller than the full bank. In this case, the size of each block can be configured in software to be any size from 4 samples up to 1 Megasample for a unit with 2 MS of RAM. For an 8 MS unit, the minimum block size is 16 samples, amd in a 32 MS unit, a block may be as small as 64 samples. In both cases, a block may be as large as desired (up to half of the total memory size), and in all three cases, the block size resolution is equal to the minimum block size. This feature is useful in satisfying minimum latency requirements typical of many process control loops.

1.1.4 VMEbus Interface

The VMEbus interface provides access to the Model 4261 by a VMEbus Bus Master for control of all programmable board functions and for reading data out to any bus device or to disk. The control functions supported include:

Selection of Data Output Mode (VME or Parallel Port)
VMEbus Data Bus Width (16 or 32 bits)
Start Command
Reset Control
Block Size (see last paragraph of Section 1.1.3, above)
Bank Swap
Bank Clear
Interrupt Mask
Interrupt and Operating Status
Tag RAM Setup

The acquired data is read from the Model 4261 via its FIFO output buffer. The FIFO mode allows the user to empty (or fill) the Data RAM from a single VME address. Sequential addressing of the DRAM's is performed automatically using the internal address counter. This is a very efficient method of moving a block of data onto the bus.

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1.1 Introduction (continued)

1.1.5 Parallel Port

The Parallel Port allows data to be delivered to a general purpose device with a parallel TTL input port. A simple two-wire handshake consists of an output line indicating data is ready and an input line indicating data has been accepted.

The Parallel Port looks like a FIFO output where the FIFO is as deep as the output memory bank. In this way, data can be delivered in bursts or with variable output rates completely independent of the A/D rate at the input. The only constraint is that the average output rate must be greater than or equal to the average input rate to avoid overruns and loss of input data.

The Parallel Port is delivered through a front panel 50-pin flat cable connector. The data bus is 16-bits wide and the top 12 bits are used for sampled data. It is compatible with the Pentek Model 4241 Digital I/O MIX Module.

1.1.6 Direct A/D Output - Option 019 Only

An optional configuration supplements the front panel parallel port described above by also making the data output from the A/D converter directly available to the user, bypassing the RAM banks. There are no handshaking signals associated with this output data stream, whose output rate will be exactly equal to the sampling clock rate. On units equipped with Option 019, the front panel port connector contains 80 pins, and carries the direct A/D output data as well as the RAM bank data and its handshake signals. The pinout of this connector is compatible with Option 019 of the Pentek Model 4272 Multiband Digital Receiver MIX Module.

1.1.7 Tag RAM

On the Model 4261A, an adjunct feature of Parallel Port is the Tag RAM. Four lines of the parallel port connector are used as the Tag field, for the purpose of steering output data to one of 16 destination devices. The ribbon cable can be connected in a daisy-chain fashion to several receivers. Each receiver can decode the 4-bit tag address and accept data only when the address matches. This decoding scheme is supported on the Model 4241 Digital I/O module.

During setup, the tags are loaded from the VMEbus into the Tag RAM. The RAM is arranged as 8 pages of 256 x 8 bytes each. The four least significant bits of each byte is the tag and the seventh bit is set to '1' to designate the last tag in the list. This set bit causes the list to be recycled. The list can contain any number of tags up to 256. Three control bits specify which one of the 8 pages is to be used. This supports fast switching between lists for applications where multiple output patterns are required.

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1.1 Introduction (continued)

1.1.7 Tag RAM (continued)

A Group Counter determines the number of samples sent per tag. If the Group Counter is set to 1, then each output sample is sent with successive tags from the Tag RAM. If blocks of 1k samples are to be sent to each device, then the Group Counter is set to 1k. The maximum count for the Group Counter is 16 Megasamples.

1.1.8 Interrupts

The VMEbus can be interrupted on several different operating conditions including:

- Bank Swap
- Bank Full
- Input Overload
- Input Overrun

Each interrupt source is enabled by a bit in the interrupt mask register. Jumpers configure the interrupt to any one of seven interrupt levels on the bus. An interrupt ID vector register is provided so that the VME Bus Master can interrogate the Model 4261 to determine the interrupt source.

1.2 Specifications

A/D Converter and Sample & Hold:

Standard Unit:

Type:	Burr Brown ADC603
Resolution:	12 bits
Conversion Rate:	Up to 10 MSample/sec
Sample & Hold:	Integral, 12-bit accuracy
Full Scale Input:	+ 1 V
Spur Free Dyn Range:	-72 dBc, typical
SINAD:	65 dB
Total Harm. Distortion:	-69 dBc, typical
Signal/Noise:	-65 dBc, typical
Aperture Jitter:	9 ps

Option 010:

Type:	Burr Brown ADC614
Resolution:	14 bits
Conversion Rate:	Up to 5.12 MSample/sec
Sample & Hold:	Integral, 14-bit accuracy
Full Scale Input:	+ 1 V
Spur Free Dyn Range:	-82 dBc, typical
SINAD:	70 dB
Signal/Noise:	-71 dBc, typical
Aperture Jitter	10 ps

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1.2 Specifications (continued)

Sample Rate Generator:

Type:	Programmable divider
Divisor Range:	1 to 65,535
Clock Range:	150 Hz to 10 MHz
Resolution:	16 bits
External Clock:	TTL Input, DC - 10 MHz, Front Panel BNC
External Trigger:	TTL Input, Front Panel BNC

Data RAM:

Size:	
Standard Unit:	2,097,152 12-bit samples
Option 002:	8,388,608 12-bit samples
Option 003:	33,554,432 12-bit samples
Configuration:	Two swinging banks, each bank:
Standard Unit:	1,048,576 samples max. 4 samples min.
Option 002:	4,194,304 samples max. 16 samples min.
Option 003:	16,777,216 samples max. 64 samples min.
Input Data Rate:	10 MHz maximum
VMEbus Access:	Each bank mapped as a memory region in A24 and A32 Address Space. Size of region:
Standard Unit:	2 MByte
Option 002:	8 Mbyte
Option 003:	32 Mbyte
VMEbus Base Address:	DIP switch selectable

Parallel Port:

Data Field:	16 bits, 2's complement (high true)
Tag Field:	4 or 6 bits, user programmed (high true)
Control Line Out:	DAV - Data Available (low true)
Control Line In:	NRFD - Not Ready For Data (low true)
Levels:	TTL, single-ended
Connector:	50-pin IDC Flat Cable

TAG Section (Model 4261A):

Tag Field:	4 or 6 bits, user programmed (high true)
Tag Page Size:	256 entries
Number of Tag Pages:	8

VMEbus Interface:

Bus Device Class:	Slave D32 A32 I(1-7)
Memory Space:	DRAM Size
Base Address:	DIP Switch Selectable.
Standard Unit:	on any 2 MByte boundary
Option 002:	on any 8 Mbyte boundary
Option 003:	on any 32 Mbyte boundary

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1.2 Specifications (continued)

Power Requirements:

+5V	3.9 A typ. (4.6 A typ w/ Tag Ram [4261A])
+12V	0.3 A typ
–12V	0.3 A typ (0.6 A typ w/ Tag Ram [4261A])

Physical:

Dimensions:	6U (160 mm x 233.35 mm) Single (4HP) 0.8" slot width
Airflow:	100 Linear ft/min at 0.5" from component surface

Ordering Information:

Model 4261:	10 MHz, 12 bit A/D Converter, 2 MSample Data Ram
Model 4261A:	Same as above, with Tag Ram
Option 002:	8 MSample Data Ram
Option 003:	32 MSample Data Ram
Option 010:	5.12 MHz, 14 bit A/D Converter
Option 019:	Direct A/D Output available at Parallel Port Connector

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Chapter 2 - Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If you discover any damage, please contact Pentek immediately, at the phone number shown on this manual's title page. Please save the original shipping container and packing material, in case re-shipment is required.

2.2 Introduction

The Model 4261 fits in a standard 6U double-high VMEbus card cage and occupies 4HP units of width or 0.8". Before the unit is installed in the VMEbus card cage, configuration jumpers must be installed for proper operation.

Table 2-1, below, presents a list of jumpers and their functions. **DO NOT CHANGE THE SETTINGS OF ANY JUMPERS NOT MENTIONED IN THIS TABLE.**

Table 2-1: Model 4261 - Jumper Functions

PC Board	Jumper	Function
Main	JP2 - 1 thru 7, 11 thru 17	Interrupter Request Level - IRQ Line
	JP2 - 8 thru 10, 18 thru 20	Interrupter Request Level - Vector Level
	JP3 - 1 thru 16	A32 VMEbus Slave Base Address
	JP4 - 1 thru 16	A24 and A32 VMEbus Slave Base Address
	JP5 - 1 thru 16	A16 VMEbus Slave Base Address
	JP6 - 1 thru 16	Block Size - RAM A
	JP7 - 1 thru 16	Block Size - RAM B
	JP8 - 1 thru 3	Parallel Port Control
	JP9 - 1 thru 3	Parallel Port Signal Select (Option 019 Only)
A/D	JP1 - 1 thru 3	Test Counter Enable / Disable
Tag RAM	JP1, JP2	Tag Bits 5 & 6 Enable

2.3 Separating the PC Board Assemblies

The Model 4261 consists of three separate printed circuit (PC) board assemblies:

Main Board	Contains VMEbus Interface, RAM Buffers	# 004.42610
A/D Module	Contains A/D Converter	# 004.42611
TAG RAM	Contains TAG Section (4261A Only)	# 004.42612

In order to set certain jumpers, these PC assemblies must be separated from each other. The boards are held together by nylon screws and threaded standoffs and by pin & socket connectors. Drawings of these boards, showing jumper and screw locations, are presented as Figures 2-1 through 2-3, on the following pages.

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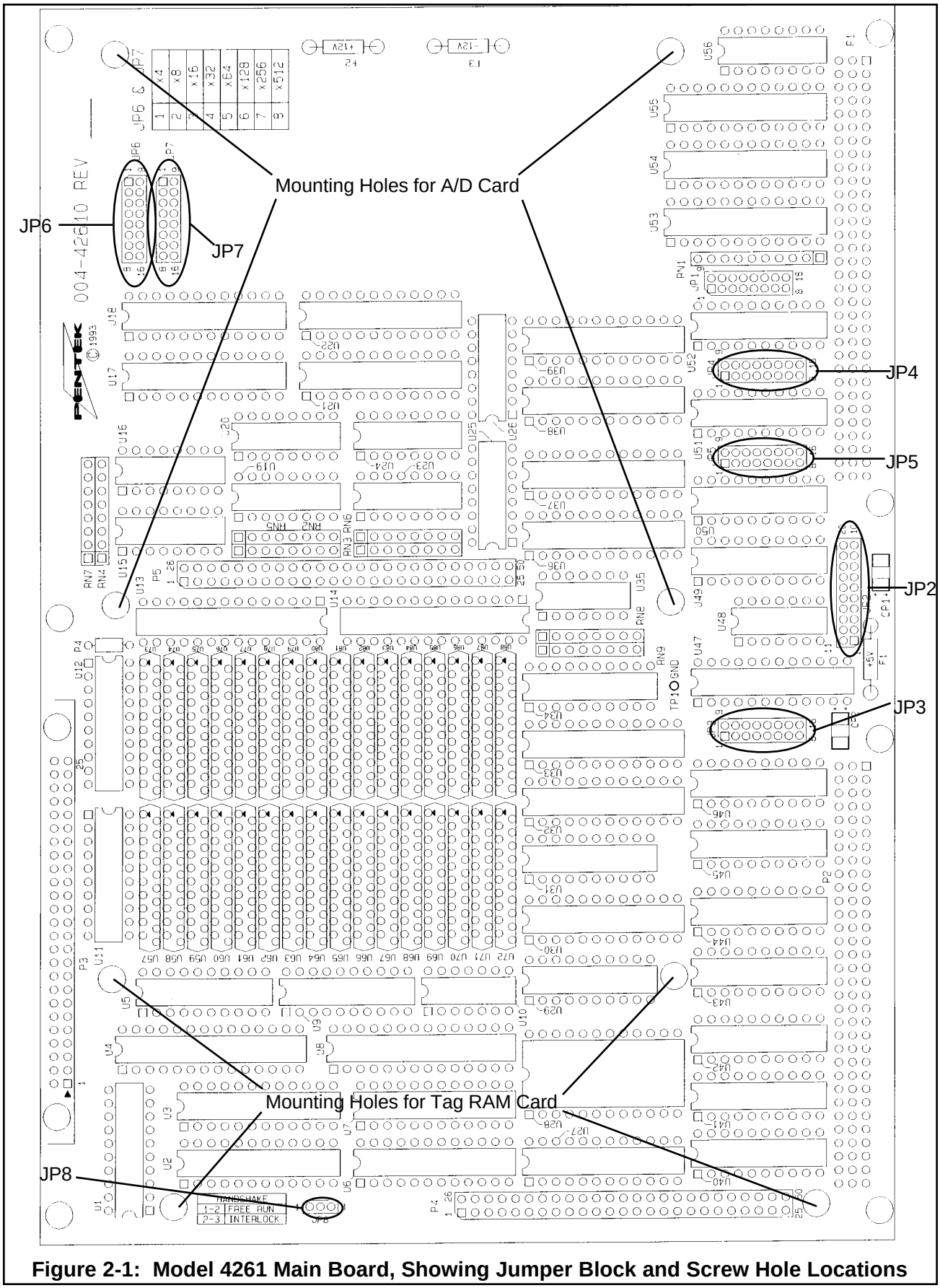


Figure 2-1: Model 4261 Main Board, Showing Jumper Block and Screw Hole Locations

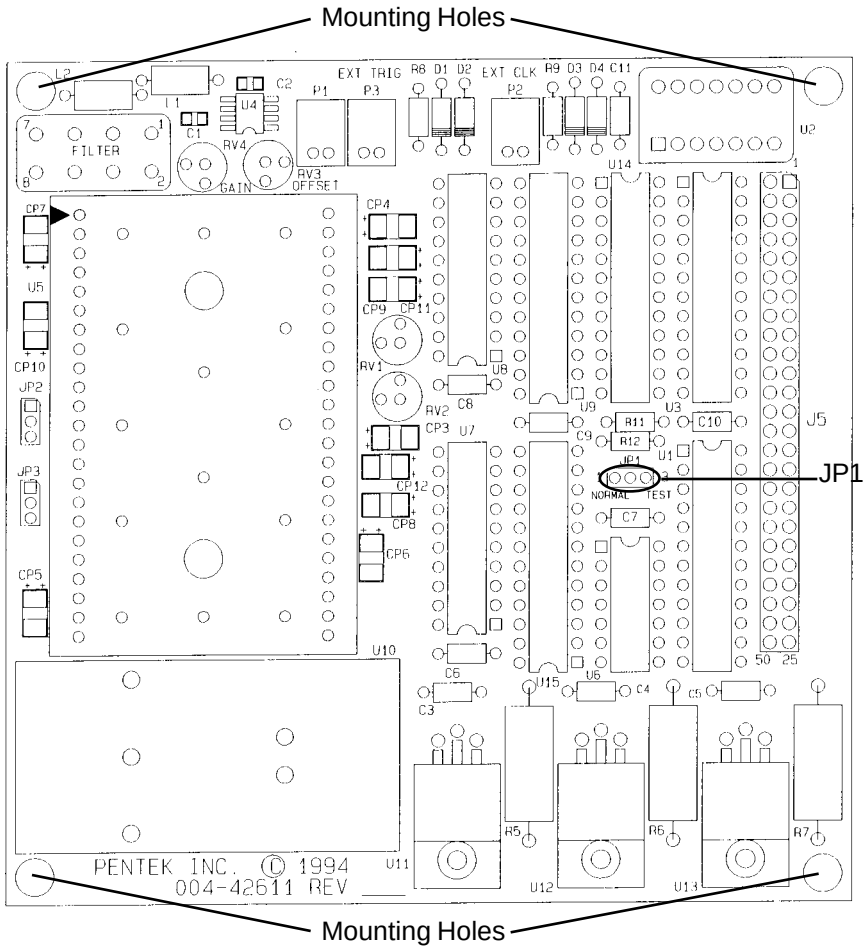


Figure 2-2: Model 4261 A/D Module, Showing Jumper Block and Screw Hole Locations

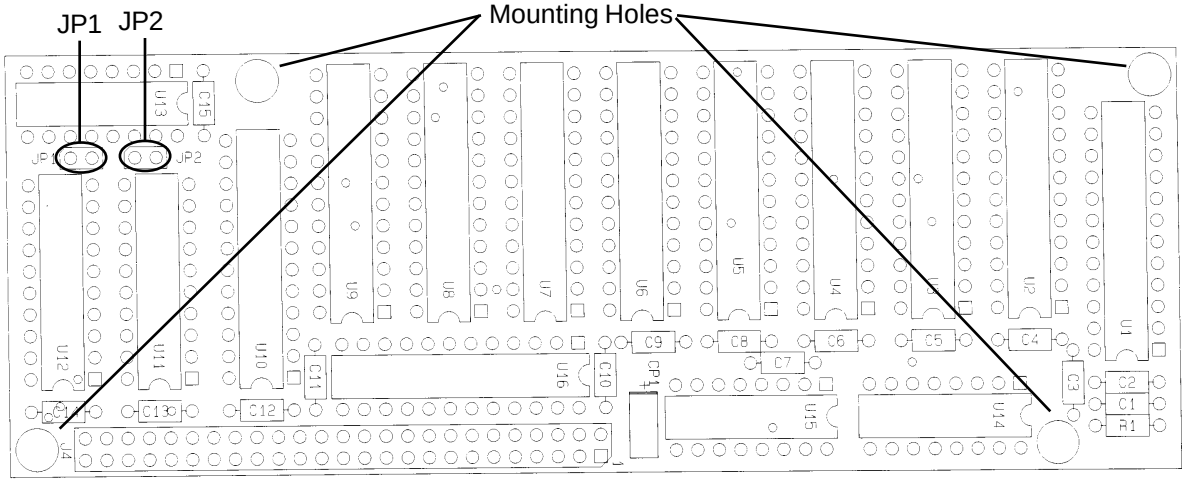


Figure 2-3: Model 4261A Tag Section, Showing Jumper Block and Screw Hole Locations

2.3 Separating the PC Board Assemblies (continued)

CAUTION:

When replacing the modules, be sure the pin & socket connectors are aligned.

First place the Model 4261 on a static-controlled work surface with the Main Board down. Remove the four nylon screws securing the board to be separated. For the TAG Section module, gently separate the pin & socket connector and pull the module straight up. For the A/D Converter module, gently separate the pin & socket connector and then swing the module over the front panel, using the wires to the front panel BNC connectors as a 'hinge'.

2.4 VMEbus Base Address Jumpers - Main Board JP3, JP4 and JP5

The Model 4261 is a VMEbus slave device. This means that it appears as a memory resource to the VMEbus and can be addressed for reading and writing performed by any VMEbus master. In order to locate the base of the Model 4261's memory in the VMEbus address space, jumpers JP3, JP4 and JP5 on the Main Board must be set. This address will be referred to throughout this manual as the **Base Address.**

The Model 4261 responds to three addressing modes: A16, A24 and A32 each with its own address modifier (AM) codes. These address modes are described in Table 2-2, below.

Table 2-2: Model 4261 Addressing Modes

Mode	Address Lines	Function	Resolution	Jumpers	AM Codes
A16	A01 thru A15	Counter / Timer Registers	256 bytes	JP5	2D, 29
		Interrupt ID and Mask Registers			
		Trigger Command Register			
		Command Register			
		TAG RAM Input / Output			
		Data VME FIFO Input / Output			
A24	A01 thru A23	Data VME RAM	Std: 2 Mbytes	JP4, JP3	3E, 3D, 3A, 39
			Opt.002: 8 Mbytes		
			Opt.003: 32 Mbytes		
A32	A01 thru A31	Data VME RAM	Std: 2 Mbytes	JP4, JP3	0E, 0D, 0A, 09
			Opt.002: 8 Mbytes		
			Opt.003: 32 Mbytes		

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2.4 VMEbus Base Address Jumpers (continued)

2.4.1 A16 Base Address Jumpers

Data access to either the VME FIFO or the PAR PORT (Front Panel Parallel Output Port), is performed in A16 VMEbus address space. If you intend to read the data out over the VMEbus, the FIFO is much more efficient than direct RAM access and is therefore the recommended method. For A16 address space, the Base Address (A16_base) may be set on any multiple of 256 bytes as determined by jumper block JP5. Table 2-3, below, describes the settings.

Table 2-3: A16 Base Address Jumpers - Jumper Block JP5

JP5 Jumper Pins	1 - 9	2 - 10	3 - 11	4 - 12	5 - 13	6 - 14	7 - 15	8 - 16
Address Line	A15	A14	A13	A12	A11	A10	A09	A08
Hex Weight	0x8000	0x4000	0x2000	0x1000	0x0800	0x0400	0x0200	0x0100
Jumper IN	0	0	0	0	0	0	0	0
Jumper OUT	1	1	1	1	1	1	1	1

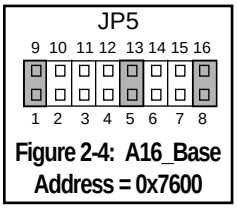


Figure 2-4: A16_Base Address = 0x7600

For example, for an A16 base address of 7600H (equivalent to decimal 30208), install jumpers JP5, 1-9, JP5, 5-13, and JP5, 8-16 and omit the other five jumpers. This jumper pattern is shown in Figure 2-4, at the left, with the darkened positions indicating an installed jumper.

2.4.2 A24 and A32 Base Address Jumpers

If your application requires direct access to the VME RAM, this is accomplished in A24 or A32 VMEbus address space. As noted above, the FIFO provides a far more efficient method of reading data out of the 4261, over the VMEbus, than does direct RAM access. We recommend that the VME RAM accesses be used only to "skip over" initial, uninteresting samples that may have been taken, by performing a single read at a particular address. This will advance the FIFO's pointer to that RAM address, after which the remainder of the data can be read from the FIFO.

The RAM containing the output data is memory-mapped to the VMEbus and must be located on a 2 Mbyte address boundary if you have a standard 4261 or 4261A. It must be located on an 8 Mbyte boundary if your 4261 is equipped with memory option 002, or on a 32 Mbyte boundary if you have memory option 003.

If A24 addressing is used then jumper block JP4 determines the location of the base of the VME RAM (A24_base). If A32 addressing is used, then both jumper blocks JP4 and JP3 are used.

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2.4 VMEbus Base Address Jumpers (continued)

2.4.2 A24 and A32 Base Address Jumpers (continued)

Table 2-4: Model 4261 - A24 and A32 Base Address Jumper Functions

Address Space	A32 Space								A24 Space		
Jumper Block Pins	JP3 1-9	JP3 2-10	JP3 3-11	JP3 4-12	JP3 5-13	JP3 6-14	JP3 7-15	JP3 8-16	JP4 1-9	JP4 2-10	JP4 3-11
Address Line	A31	A30	A29	A28	A27	A26	A25*	A24	A23†	A22	A21
Hex Weight	0x8000 0000	0x4000 0000	0x2000 0000	0x1000 0000	0x0800 0000	0x0400 0000	0x0200 0000	0x0100 0000	0x0080 0000	0x0040 0000	0x0020 0000
Jumper IN	0	0	0	0	0	0	0	0	0	0	0
Jumper OUT	1	1	1	1	1	1	1	1	1	1	1

NOTES: Jumper JP1, 1-9 must always be installed in units with 8 MSample or 2 MSample DRAM
Additionally, JP1, 2-10 and JP1, 3-11 must always be installed in units with 2 MSample DRAM.
* - Least Significant Base Address bit for Option 003 (32 MSample DRAM)
† - Least Significant Base Address bit for Option 002 (8 MSample DRAM)

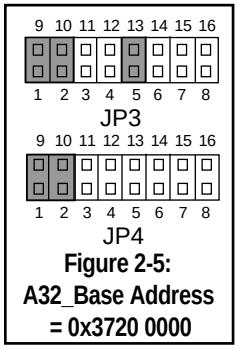


Figure 2-5: A32_Base Address = 0x3720 0000

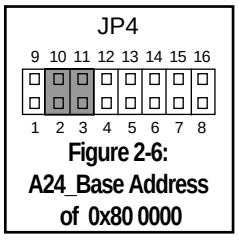


Figure 2-6: A24_Base Address of 0x80 0000

Table 2-4, above, describes the A24 and A32 base address jumper settings. Note that a Model 4261 with memory option 003 can only mapped to address 0x00 0000 in A24 space, and it occupies the entire 16 Mbytes provided by A24. For these units, jumper positions listed to the right of JP3 pins 7 and 15 in the table above are not used, and must be set for '0' (in A24 or A32 space). By the same token, 4261s with memory option 002 can reside at only two locations in A24 space, (0x00 0000 and 0x80 0000). For these units, jumper positions listed to the right of JP4, pins 1 and 9 in Table 2-4 are not used, and must be set to '0'. (Again, this applies to A32 space as well as A24 space.)

For example, to set a Base Address of 0x3720 0000 in A32 address space, then jumpers JP3, 1-9; JP3, 2-10; JP3, 5-13; JP4, 1-9; and JP4, 2-10 must be installed and the others removed. See Figure 2-5, to the left, above.

To set a Base Address of 0x80 0000 in A24 address space, jumpers JP4, 2-10 and JP4, 3-11 must be installed. See Figure 2-6, to the left, below.

2.4.3 VME RAM Size

The size of the active VME RAM memory array is 2 Mbytes (1 MSample) in a standard Model 4261, 8 Mbytes (4 MSamples) in units equipped with memory option 002, and 32 Mbytes (16 MSamples) in units equipped with option 003. This is because only half of the installed memory is available to the VMEbus at any given time, while the ADC fills the other half. The 4261's VME RAM region starts at the Base Address, set by jumpers as described in the section above. In some cases, it may be desirable to reduce the size of the VMEbus 'window' or view of the VME RAM. There are two common reasons for wanting to use less VMEbus memory space First, the VME RAM Block Size may be smaller than the amount of memory in your ADC unit. Secondly, since the VME RAM mode is seldom used, then the A24 or A32 adddress space occupied by the 4261 is underutilized.

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2.4 VMEbus Base Address Jumpers (continued)

2.4.3 VME RAM Size (continued)

Table 2-5: Model 4261 - VME RAM Size Jumpers

RAM Size	JP1 1-9	JP1 2-10	JP1 3-11	JP1 4-12	JP1 5-13	JP1 6-14	JP1 7-15	JP1 8-16	JP4 1-9	JP4 2-10	JP4 3-11	JP4 4-12	JP4 5-13	JP4 6-14	JP4 7-15	JP4 8-16
16 M	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
8 M	X	-	-	-	-	-	-	-	A	-	-	-	-	-	-	-
4 M	X	X	-	-	-	-	-	-	A	A	-	-	-	-	-	-
2 M	X	X	X	-	-	-	-	-	A	A	A	-	-	-	-	-
1 M	X	X	X	X	-	-	-	-	A	A	A	A	-	-	-	-
512 k	X	X	X	X	X	-	-	-	A	A	A	A	A	-	-	-
256 k	X	X	X	X	X	X	-	-	A	A	A	A	A	A	-	-
128 k	X	X	X	X	X	X	X	-	A	A	A	A	A	A	A	-
64 k	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A

NOTES: 'X' indicates jumpers that MUST be installed to set the indicated VMEbus DRAM window size.
'-' indicates jumpers that MUST be removed for the indicated VMEbus DRAM window size.
'A' indicates jumpers that MAY be installed to set the DRAM Base Address

Table 2-5, above, shows the jumpers necessary for configuring the 4261's VME RAM region to various sizes. Jumper block JP1 actually determines the size of the VME's memory window on the 4261, and jumper block JP4 is used in determining the base address. An 'X' in the table indicates a jumper that MUST be installed on JP1 to set the desired memory window size. A '-' in the table indicates a jumper that MUST be omitted on either jumper block for the indicated configuration . An 'A' indicates a jumper that MAY be installed on JP4 to set the base address of the DRAM.

As can be seen from Table 2-5, each pair of jumpers installed reduces the VME RAM size by a factor of two. The minimum VME RAM Size is 64 kbytes, selected when all jumpers are installed.

2.5 Block Size Jumpers

The Block Size refers to the effective size of each RAM bank. The size is expessed in words where each word is a 16-bit value containing a 12-bit sample from the A/D converter. The maximum Block Size is 1 MWord in units with standard memory, 4 MWords in units with memory option 002, and 16 MWords in units with memory option 003. The minimum Block Size is 8 words. (Each word is represented as two 8-bit bytes on the VMEbus.)

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2.5 Block Size Jumpers (continued)

The Block Size is set using two facilties on the board: the Block Size Jumpers and the Block Size Counter. The Block Size Jumpers are used to select the Word Clock for use as the input to the Block Size Counter. This is represented schematically in Figure 2-7, below.

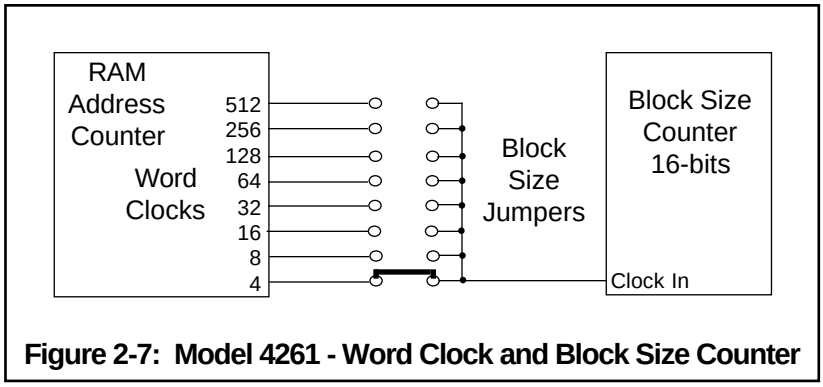


Figure 2-7: Model 4261 - Word Clock and Block Size Counter

The RAM Address Counter generates RAM addresses and supplies the eight Word Clocks for the Block Size Jumpers. Each Word Clock corresponds to a number of words accessed in the RAM and ranges from a 4-word clock to a 512-word clock.

The Block Size Counter is a software programmable, 16-bit down counter which can be preset to any value between 2 and 65,535. By using various combinations of the Word Clocks and counter divisors, the Block Size can range from 8 words (4 x 2) to 4,194,240 words (64 x 65,535). There are two RAM Address Counters and two Block Size Counters, one for each bank.

Both sections should be set for the same Block Size under normal circumstances, although they may be set differently for unusual applications. The jumper descriptions are shown in Table 2-6, below. The maximum block size available in your unit is, of course, a function of the amount of DRAM installed. Be aware that not all the settings listed in the table below may be available for your memory configuration. Examples of programming various Block Sizes are presented in Section 3.4.9.2.

Table 2-6: Model 4261 - DRAM Block Size Jumper Settings

Word Clock	Minimum Block Size (N = 2)	Maximum Block Size (N = 65,535)	Divisor (N) Resolution	Block Size Resolution	RAM Bank A Jumper	RAM Bank B Jumper
4	8	2^{18} - 8 = 262,136	2	8	JP7-1,9	JP6-1,9
8	16	2^{19} - 8 = 524,280	1	8	JP7-2,10	JP6-2,10
16	32	2^{20} - 16 = 1,048,560	1	16	JP7-3,11	JP6-3,11
32	64	2^{21} - 32 = 2,097,120	1	32	JP7-4,12	JP6-4,12
64	128	2^{22} - 64 = 4,194,240	1	64	JP7-5,13	JP6-5,13
128	256	2^{23} - 128 = 8,388,480	1	128	JP7-6,14	JP6-6,14
256	512	2^{24} - 256 = 16,776,960	1	256	JP7-7,15	JP6-7,15
512	1024	2^{25} - 512 = 33,553,920	1	512	JP7-8,16	JP6-8,16

NOTES: 1) One, and only one, jumper per bank may (and must) be installed.
2) For Word Clock = 4, Divisor (N) MUST be an even integer.
3) This table applies to 4261 Main Board (320-42610) Revisions C and higher.

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2.6 Interrupt Jumpers

The Model 4261 can generate interrupts on any of the seven VMEbus interrupt levels. The interrupt level is determined by setting jumpers as described in Table 2-7, below. Figure 2-8, beneath the table, shows jumper block JP2 configured such that the 4261 is a VMEbus interruptor on level 7.

Table 2-7: Model 4261 - VME Interrupt Level Jumpers

Interrupt Level	IRQ Line Jumper	Interrupt Vector Jumpers Installed
none	none	none
1	JP2,7-17	JP2,10-20
2	JP2,6-16	JP2, 9-19
3	JP2, 5-15	JP2,10-20 JP2, 9-19
4	JP2, 4-14	JP2, 8-18
5	JP2, 3-13	JP2,10-20 JP2, 8-18
6	JP2, 2-12	JP2, 9-19 JP2, 8-18
7	JP2, 1-11	JP2,10-20 JP2, 9-19 JP2, 8-18

NOTE: **ONLY ONE** IRQ Line Jumper may be installed

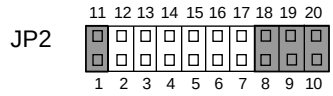


Figure 2-8: Model 4261 - JP2 Configuration for a Level 7 Interruptor

2.7 A/D Test Counter Jumper

In order to provide a digital test pattern at the output of the Model 4261, the output of the A/D converter can be replaced by the bits of a 12-bit binary counter. The counter advances once every sample clock and provides a linear digital ramp of 4096 levels which wraps around to zero after the end count.

To enable this counter (and disable the ADC), a shorting jumper is placed at jumper block JP1 between pins 2 and 3. To enable the A/D converter, place the jumper between pins 1 and 2 of JP1. These settings are summarized in Table 2-8, below.

Table 2-8: Model 4261 - A/D Test Counter Jumper

Enable A/D Converter	Enable Test Counter
Install Jumper JP1, 1-2	Install Jumper JP1, 2-3

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2.8 TAG RAM Bit Jumpers (Model 4261A Only)

The Model 4261A's TAG RAM normally supplies 4 bits to the parallel digital output port. Two additional tag bits are available in the TAG RAM and can be brought out to the Parallel Port by installing jumpers on the TAG RAM module.

These bits are designated TA5 and TA6 and are the two next higher bits above TA1 thru TA4. The jumpers and output pins are shown in Table 2-9, below:

Table 2-9: Model 4261A - TAG RAM Bits TA5 and TA6

TAG RAM Bit Designation	Install Jumper To Enable	Parallel Port Output Pin
TA5	JP1	P3-30
TA6	JP2	P3-31

2.9 Parallel Port Connector - Standard Units

The Parallel Port on a standard Model 4261 or 4261A (i. e., one **NOT** equipped with Option 019) is a general purpose TTL interface for supplying output data from the Output FIFO to an external device. It provides of a 16-bit data field, a 4-bit Tag field, and a 2-wire handshake system.

The front panel Parallel Port connector is a 50-pin dual in-line header connector with 0.025" square male pins. The pins are arranged as two rows of 25 pins with 0.1" spacing betwen the pins and between the rows. The 3M part number for this connector is #3433-5302.

The mating connector is a standard 50-position ribbon cable socket. Sockets from a wide variety of manufacturers can be used. The preferred socket style is one which accepts a strain relief, such as the 3M #3425-7050 with strain relief #3448-3050. Ejector-latch handles on the front panel connector will lock this style socket into place and make it easy to eject.

The pin assignments for the Parallel Port connector are shown in Table 2-10, on the next page, along with a pin orientation drawing. Note that the triangular arrow on the front panel near the bottom of the connector marks pin #1. **When installing the socket, be sure to align pin #1 of the socket with pin #1 of the front panel connector.** Most sockets have a triangular arrow embossed on the socket body to designate pin #1.

The logic levels for all signals are TTL-compatible, with logic '0' = 0.0 to 0.8 V and logic '1' = 2.0 to 5.0 V relative to Digital Ground (GND). The 16 data lines PD0 through PD15 and the 4 (optionally 6) Tag lines TA1 thorugh TA4 (or TA6) are all high-true logic levels. The two handshake lines, $\overline{\text{DAV}}$ and $\overline{\text{NRFD}}$ are low true logic levels.

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2.9 Parallel Port Connector - Standard Units (continued)

Table 2-10: Model 4261- Front Panel Parallel Port Connector Pin Assignment

Pin #	Signal	Function	Pin #	Signal	Function
50	GND	Digital Ground	25	$\overline{\text{NRFD}}$	Not Ready For Data*
49	GND	Digital Ground	24	$\overline{\text{DAV}}$	Data Valid*
48	GND	Digital Ground	23	GND	Digital Ground
47	TA4	Tag Bit 4	22	TA2	Tag Bit 2
46	TA3	Tag Bit 3	21	TA1	Tag Bit 1 - LSB
45	GND	Digital Ground	20	PD15	Data Bit 15 - MSB
44	GND	Digital Ground	19	PD14	Data Bit 14
43	GND	Digital Ground	18	GND	Digital Ground
42	GND	Digital Ground	17	PD13	Data Bit 13
41	GND	Digital Ground	16	PD12	Data Bit 12
40	GND	Digital Ground	15	PD11	Data Bit 11
39	GND	Digital Ground	14	PD10	Data Bit 10
38	GND	Digital Ground	13	GND	Digital Ground
37	GND	Digital Ground	12	PD9	Data Bit 9
36	GND	Digital Ground	11	PD8	Data Bit 8
35	GND	Digital Ground	10	PD7	Data Bit 7
34	GND	Digital Ground	9	PD6	Data Bit 6
33	GND	Digital Ground	8	GND	Digital Ground
32	GND	Digital Ground	7	PD5	Data Bit 5
31	TA6	Tag Bit 6[1]	6	PD4	Data Bit 4
30	TA5	Tag Bit 5[1]	5	PD3	Data Bit 3
29	GND	Digital Ground	4	PD2	Data Bit 2
28	GND	Digital Ground	3	GND	Digital Ground
27	GND	Digital Ground	2	PD1	Data Bit 1
26	GND	Digital Ground	1	PD0	Data Bit 0 - LSB

* Low true logic signals

[1] Optional Tag Bits - see section 2.8

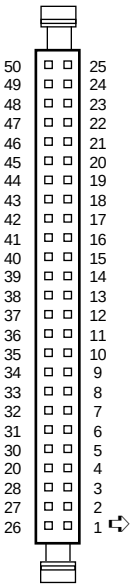


Figure 2-9: Model 4261 - Front Panel Parallel Port Connector Pin Numbering

2.9.1 Parallel Port Mode Control Jumper

The Model 4261's Parallel port can be operated in two different modes, Interlocked mode or Free-Run Mode. The operating mode is selected by the placement of a shorting jumper on Jumper Block JP8. Placing the jumper between pins 1 & 2 selects Free Run mode, and positioning it between pins 2 & 3 chooses Interlocked operation. Table 2-11, below, summarizes the jumper settings. Descriptions of the port's handshaking and timing can be found in Section 2.9.2, beginning on the next page.

Table 2-11: Model 4261 - Parallel Port Mode Select

Free Run Mode	Interlocked Mode
Install Jumper JP8-1,2	Install Jumper JP8-2,3

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2.9 Parallel Port Connector - Standard Units (continued)

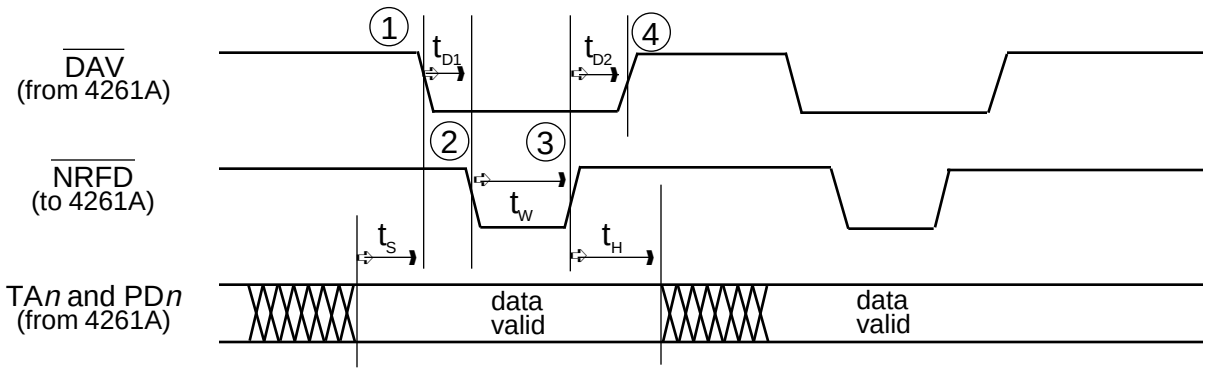
2.9.2 Parallel Port Timing - Interlocked Mode

In Interlocked mode, two handshake lines are used to deliver data samples to the Parallel Port. The $\overline{DAV}$ line is driven as an output line by the Model 4261 to indicate that data is ready on the data lines. The $\overline{NRFD}$ line is an input line to the Model 4261 indicating that data is being stored and accepted by the receiving device. The timing diagram shown in Figure 2-10, below, illustrates the operation.

The time sequence for a transfer is also given below, referenced to the numbers shown in the diagram.

1) The 4261 sends $\overline{DAV}$ low when it has placed valid output data on the PD bus and a valid Tag on the TA bus.

2) The receiver sends $\overline{NRFD}$ low indicating that it has acknowledged $\overline{DAV}$ and is busy loading data.



NOTES:

1) The receiving device can implement the $\overline{NRFD}$ generator with a simple one-shot circuit. The minimum logic '0' pulse width of $\overline{NRFD}$ is t_W = 30 nsec.

2) At the 4261 connector, the $\overline{NRFD}$ line is a TTL input with a 330 ohm pull-up resistor to +5V. If more than one receiver device is to be used, the $\overline{NRFD}$ line should be driven by open collector drivers. The last device to become ready for data will then release the line so the pull-up resistor can pull the line to logic '1'.

3) Timing parameters are defined as:

Parameter	Description	min	typ	max	
t_S	data valid setup time before $\overline{DAV}$ low	15	20	–	nsec
t_{D1}	delay from $\overline{DAV}$ low to $\overline{NRFD}$ low	0	30	∞	nsec
t_W	low pulse width of $\overline{NRFD}$	30	–	–	nsec
t_{D2}	delay from $\overline{NRFD}$ high to $\overline{DAV}$ high	10	20	40	nsec
t_H	data valid hold time from $\overline{NRFD}$ high	15	25	–	nsec

Figure 2-10: Parallel Port Timing - Interlocked Mode

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2.9 Parallel Port Connector - Standard Units (continued)

2.9.2 Parallel Port Timing - Interlocked Mode (continued)

3) The receiver sends $\overline{\text{NRFD}}$ high when it has finished loading the data and is ready for more data.

4) The 4261 acknowledges the $\overline{\text{NRFD}}$ going high by returning $\overline{\text{DAV}}$ to the high state and fetching the next data sample

2.9.3 Parallel Port Timing - Free Run Mode

In Free Run mode, data is transferred in bursts whose length is equal to the Block Size. See Section 2.5 for details about setting the Block Size Jumpers. Data is transferred at a 10 MWord/sec rate, regardless of the ADC's Sample Rate setting. If the Sample Rate is below 10 MHz, the data will begin to be transferred out the port after the filling of the first block. The entire block is sent, and no further transfers occur until the next block is filled.

In this mode, the $\overline{\text{DAV}}$ line toggles as in Interlocked mode (low when a sample is ready, high between samples), but no handshake with the $\overline{\text{NRFD}}$ line occurs. Simply let $\overline{\text{NRFD}}$ float to a high level to allow transfers, or take it low to stop the flow of data.

2.10 Parallel Port Connector - Option 019

The Parallel Port on a Model 4261 or 4261A equipped with Option 019 is a general purpose TTL interface that supplys output data direct from the A/D converter, in addition to all of the signals provided by the port on the standard units. This option was designed to interface with the Pentek Model 4272 Multiband Digital Receiver MIX Module, when that unit is also equipped with Option 019.

The front panel Parallel Port connector for Option 019 is an 80-pin dual in-line header connector with .016" x 0.0125" male pins. The pins are arranged as two rows of 40 pins with 0.05" spacing betwen the pins and 0.1" spacing between the rows. The 3M part number for this connector is #81080-620203.

The mating connector is an 80-position ribbon cable socket. The preferred socket style is one which accepts a strain relief, such as the 3M #82080-6006, with strain relief #3858-080. Ejector-latch handles on the front panel connector will lock this style socket into place and make it easy to eject.

The pin assignments for the Parallel Port connector are shown in Table 2-12, on the next page, along with a pin orientation drawing, Figure 2-11. Note that the triangular arrow on the front panel near the bottom of the connector marks pin #1. **When installing the socket, be sure to align pin #1 of the socket with pin #1 of the front panel connector.** The socket has a triangular arrow embossed on the socket body to designate pin #1.

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2.10 Parallel Port Connector - Option 019 (continued)

Table 2-12: Model 4261, Option 019 - Front Panel Parallel Port Connector Pin Assignment

Pin #	Signal	Function	Pin #	Signal	Function
80	GND	Digital Ground	79	DAD3	Direct A/D Data Bit 3
78	GND	Digital Ground	77	DAD2	Direct A/D Data Bit 2
76	GND	Digital Ground	75	DAD1	Direct A/D Data Bit 1
74	GND	Digital Ground	73	GND	Digital Ground
72	GND	Digital Ground	71	DAD0	Direct A/D Data Bit 0 (LSB)
70	GND	Digital Ground	69	$\overline{\text{SEND}}$	A/D Send*
68	GND	Digital Ground	67	TA4	Tag Bit 4
66	GND	Digital Ground	65	TA3	Tag Bit 3
64	GND	Digital Ground	63	DAD15	Direct A/D Data Bit 15 (MSB)
62	GND	Digital Ground	61	DAD14	Direct A/D Data Bit 14
60	GND	Digital Ground	59	DAD13	Direct A/D Data Bit 13
58	GND	Digital Ground	57	DAD12	Direct A/D Data Bit 12
56	GND	Digital Ground	55	DAD11	Direct A/D Data Bit 11
54	GND	Digital Ground	53	DAD10	Direct A/D Data Bit 10
52	GND	Digital Ground	51	DAD9	Direct A/D Data Bit 9
50	GND	Digital Ground	49	DAD8	Direct A/D Data Bit 8
48	GND	Digital Ground	47	DAD7	Direct A/D Data Bit 7
46	GND	Digital Ground	45	DAD5	Direct A/D Data Bit 6
44	GND	Digital Ground	43	DAD5	Direct A/D Data Bit 5
42	GND	Digital Ground	41	DAD4	Direct A/D Data Bit 4
40	GND	Digital Ground	39	GND	Digital Ground
38	GND	Digital Ground	37	RD0/ $\overline{\text{NRFD}}$	RAM Bit 0 (LSB)/ Not Ready For Data*†
36	GND	Digital Ground	35	$\overline{\text{DAV}}$	Data Valid*
34	GND	Digital Ground	33	TA2	Tag Bit 2
32	GND	Digital Ground	31	TA1	Tag Bit 1 - LSB
30	GND	Digital Ground	29	RD15	RAM Data Bit 15 (MSB)
28	GND	Digital Ground	27	RD14	RAM Data Bit 1
26	GND	Digital Ground	25	RD13	RAM Data Bit 1
24	GND	Digital Ground	23	RD12	RAM Data Bit 1
22	GND	Digital Ground	21	RD11	RAM Data Bit 1
20	GND	Digital Ground	19	RD10	RAM Data Bit 1
18	GND	Digital Ground	17	RD9	RAM Data Bit 1
16	GND	Digital Ground	15	RD8	RAM Data Bit 1
14	GND	Digital Ground	13	RD7	RAM Data Bit 1
12	GND	Digital Ground	11	RD6	RAM Data Bit 1
10	GND	Digital Ground	9	RD5	RAM Data Bit 1
8	GND	Digital Ground	7	RD4	RAM Data Bit 1
6	GND	Digital Ground	5	RD3	RAM Data Bit 1
4	GND	Digital Ground	3	RD2	RAM Data Bit 1
2	GND	Digital Ground	1	RD1	RAM Data Bit 1

* - Low true logic signals

† - RD0 out or $\overline{\text{NRFD}}$ in must be selected by setting of jumper block JP9

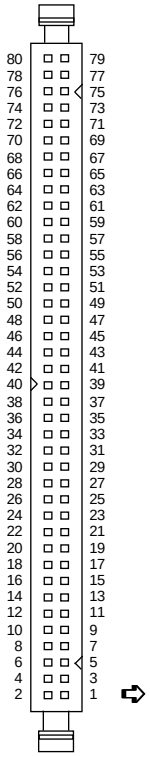


Figure 2-11: Model 4261, Option 019 - Front Panel Parallel Port Connector Pin Numbering

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2.10 Parallel Port Connector - Option 019 (continued)

The logic levels for all signals are TTL-compatible, with logic '0' = 0.0 to 0.8 V and logic '1' = 2.0 to 5.0 V relative to Digital Ground (GND). The 32 data lines, RD0 through RD15 and DAD0 through DAD15 and the 4 Tag lines TA1 thorugh TA4 are all high-true logic levels. (Note that Option 019 cannot support 6-bit Tag data.) The three handshake lines, $\overline{\text{DAV}}$, $\overline{\text{NRFD}}$ and $\overline{\text{SEND}}$ are low true logic levels.

Aside from the re-arrangement of the connector pins, all timing and handshaking for the RAM data is identical to that in the standard units. When using the 4261(A) Option 019 as a front end for the Model 4272 Option 019, the $\overline{\text{DAV}}$ signal is used as the clock input for the RAM data. This data will generally be applied to the 4272's narrow-band channel(s). The clock signal for the Direct A/D data, which will usually be connected to the wideband channel of the 4272, is the $\overline{\text{SEND}}$ signal.

In this implementation, the $\overline{\text{NRFD}}$ input handshake signal shares a connector pin with the RD0 RAM data output. Jumper Block JP9 must be set properly dependent upon which of these signals will be carried by this pin. As shown in Table 2-13, below, if the pin is to carry $\overline{\text{NRFD}}$ in, the jumper must be placed between pins 1 and 2. If the pin is to carry the LSB of the RAM data, the jumper must be placed between pins 2 and 3.

NOTE: The $\overline{\text{NRFD}}$ input handshake signal, which is not generally used when interfacing a 4261 to a 4272, is not useable on the earliest units produced with Option 019. For PC artwork with part number 320-42617, Rev. A, pin 37 of the parallel port connector is driven by the output of a data buffer. Therefore, no externally driven signal should be connected to this pin.

Table 2-13 - Model 4261 Option 019 - RD0/NRFD Jumper Selection - JP9

Signal to be carried	Jumper Position
RD0 Out	1 - 2
NRFD In	2 - 3

2.10.1 Interfacing with the Model 4272 Option 019

When used with the Model 4272 Option 019, the direct A/D output from the 4261 will generally be used to drive the wideband (channel C) input of the receiver, and used to determine which band(s) of the delayed data (from the memory buffers) will be focused on by the narrowband channel(s) (i. e., channels A and/or B).

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2.10 Parallel Port Connector - Option 019 (continued)

2.10.1 Interfacing with the Model 4272 Option 019 (continued)

Figure 2-12, right, shows the cabling arrangement for using the Model 4261 Option 019 as a front end for the Model 4272 Option 019 in the manner described above. As the figure shows, the 80-line ribbon cable connected to the 4261's front panel port must be split down the middle (i. e., between pins 40 and 41). The upper 40 (pins 41 - 80) wires carry the direct, unbuffered A/D data, and should be connected to the wideband (channel C) input port of the 4272 (pins 41 - 80 of the 4272's upper connector). The lower 40 pins 0f the 4261's output port carry the delayed data from the swinging memory buffers. These pins must be connected to the A input port of the 4272, as shown in the figure. (The pinout of the cable will not allow for connection to the channel B input.) The input data may then be directed to the other receiver channel as well, by programming the multiplexer (see Section B.2.1 of the 4272 Operating Manual).

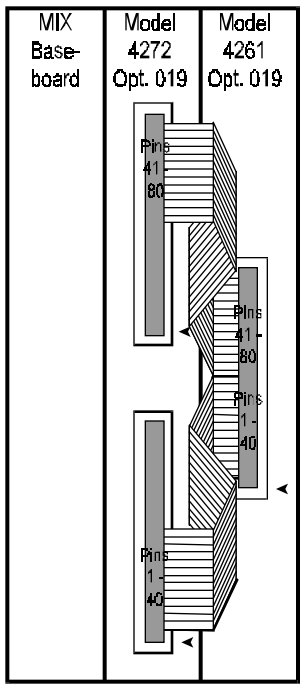


Figure 2-12: Model 4261 Option 019 - Cabling for Interface with Model 4272 Option 019

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2.11 Front Panel BNC Connectors

The following sections describe the functions of the BNC connectors on the Model 4261's front panel. Figure 2-13, right, shows the front panel of the Model 4261.

2.11.1 A/D INPUT Connector

The A/D Input connector accepts an analog signal with a voltage range of +1.00 V to -1.00 V. The input impedance is 50Ω, and is resistive. It is recommended that 50Ω coaxial cable (such as type RG-58/U) be used and the signal source have an output impedance of 50Ω. This will optimize the matching of the source and the cable to the Model 4261 input.

2.11.2 EXT TRIG Connector

The EXT TRIG connector is used to accept the External Trigger Input signal. The input must be a TTL-compatible signal with a logic '0' level between 0.0 V and 0.8 V and a logic '1' level between 2.0 V and 5.0 V. The input is terminated with a TTL-compatible PAL input and represents a load equivalent to one standard TTL input.

The input must be free of overshoot and undershoot in order to avoid false triggering. If possible, the signal should be terminated at the front panel with an in-line resistive termination which matches the characteristics of the driving signal and the cable.

2.11.3 EXT CLK Connector

The EXT CLK connector is used to accept the External Sample Clock Input signal. The input must be a TTL compatible signal with a logic '0' level between 0.0 V and 0.8 V and a logic '1' level between 2.0 V and 5.0 V. The input is terminated with a TTL-compatible PAL input and represents a load equivalent to one standard TTL input.

The input must be free of over shoot and under shoot in order to avoid false clocking. If possible, the signal should be terminated at the front panel with an in-line resistive termination which matches the characteristics of the driving signal and the cable.

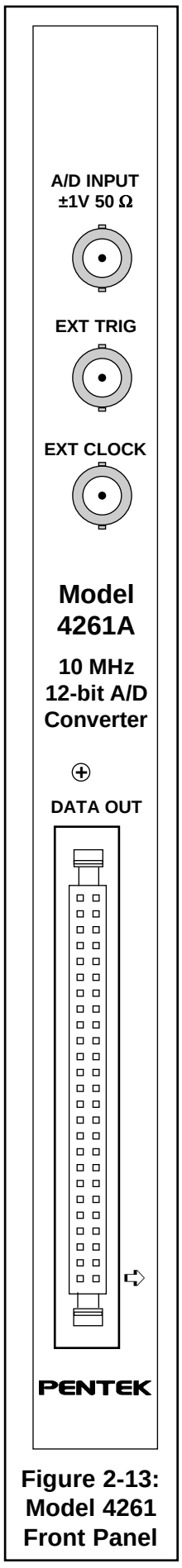


Figure 2-13: Model 4261 Front Panel

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2.11 Front Panel BNC Connectors (continued)

2.11.3 EXT CLK Connector (continued)

The External Sample Clock frequency range is from DC to 10 MHz. The duty cycle of the input signal is not critical, but it should have minimum logic '0' and logic '1' durations of 40 nsec. A TTL square wave is ideal over the frequency range.

2.12 Inserting the Model 4261(A) in the VMEbus Card Cage

Align the Model 4261 card edge with the card cage guides and push evenly on both ejector handles until the front panel seats against the upper and lower rails. Secure the unit to the cage by tightening the upper and lower retainer screws in the front panel.

CAUTION!!

Never insert or remove the Model 4261(A) while power is applied in the card cage.

2.13 Removing the Model 4261(A) from the VMEbus Card Cage

Loosen the upper and lower retaining screws; they are captive screws and will remain part of the panel assembly. Gently push both ejector handles apart (away from the center of the panel) until the unit unseats itself from the cage connectors. Then pull outward to remove the unit.

2.14 Air Flow and Thermal Considerations

Because of the high-speed A/D Converter circuitry, the Model 4261(A) generates a significant amount of heat as part of its normal operating mode. For this reason it is essential that sufficient airflow (at least 300 linear ft./min.) be maintained in the card cage.

CAUTION!!

The Model 4261(A) Must Be Operated With Forced Air Cooling of 300 Linear Feet/Min At ALL Times To Avoid Excessive Heat Buildup.

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Chapter 3 - Memory Maps, Registers and Operating Procedures

3.1 Introduction

The Model 4261 is controlled primarily by configuration jumpers and commands sent over the VMEbus to memory-mapped control registers. Each of these registers will be described in detail in this section. A more detailed block diagram of the Model 4261 Wideband A to D Converter for VMEbus systems is shown in Figure 3-1, below.

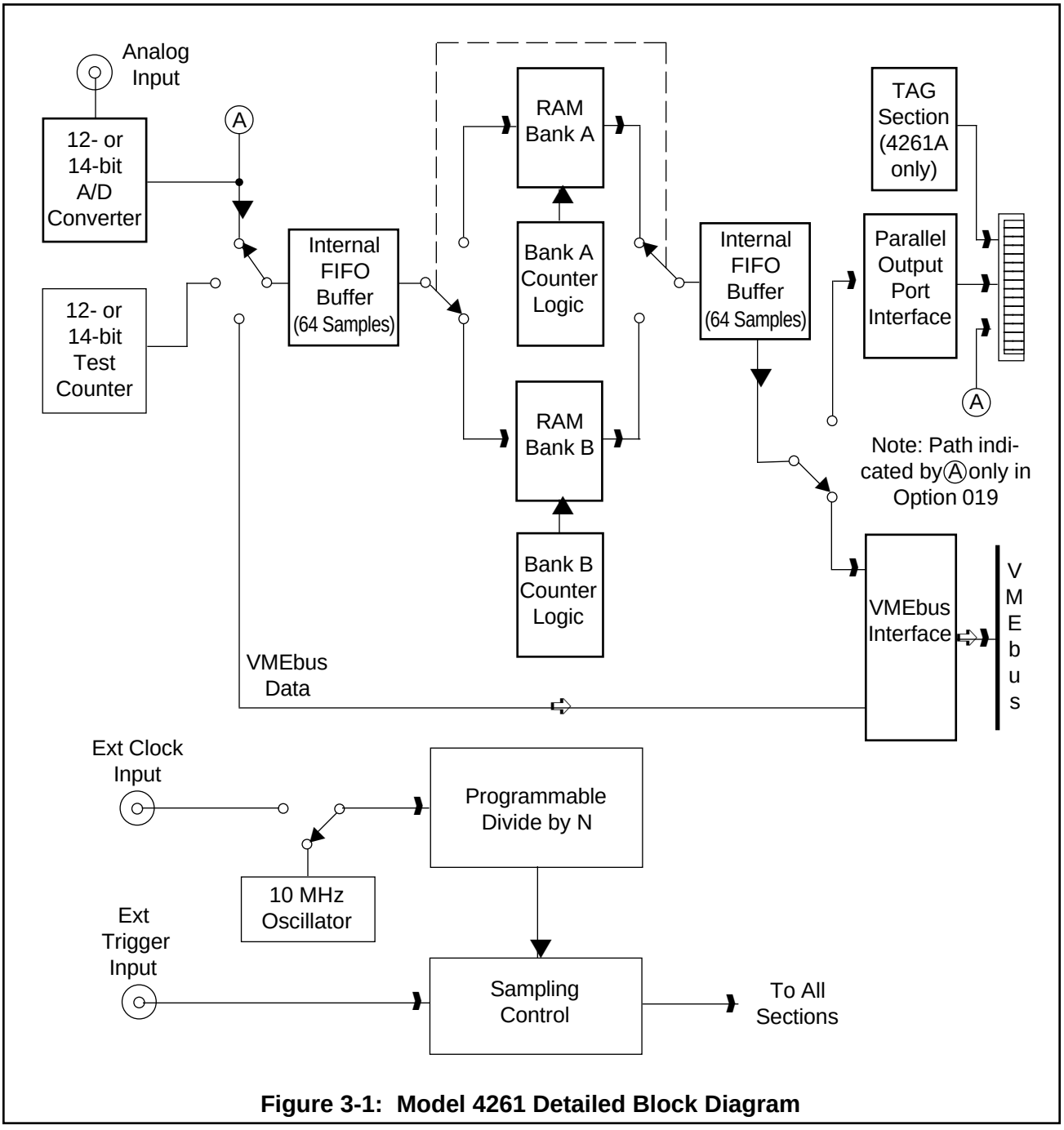


Figure 3-1: Model 4261 Detailed Block Diagram

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3.2 VMEbus Memory Tutorial

The Model 4261 acts as a VMEbus Slave device. Each of the control registers and the VME FIFO is mapped into the VMEbus A16 memory space. Access to this address space is determined by the A16 Base Address Jumpers which are described in Section 2.4.1.

VMEbus address bits A01 through A31 are implemented as 31 separate bus lines. These lines are used to explicitly address 2^{31} 16-bit words.

VME address bit A0 does not actually correspond to an address line on the bus, but is used in the control of two data strobe lines: $\overline{DS0}$ and $\overline{DS1}$. $\overline{DS0}$ becomes active for the lower byte of the 16-bit word, and $\overline{DS1}$ for the upper byte. For single byte transfers, only one of the $\overline{DSn}$ strobes is active. For 16-bit transfers, both data strobes become active at the same time. For 32-bit transfers, in addition to both strobes active, the $\overline{LWORD}$ (longword) bus line is also asserted.

3.2.1 Address Modifier Codes

There are three addressing modes defined for VMEbus transfers: 32-bit, 24-bit, and 16-bit modes. The modes are provided to support a variety of bus devices ranging from simple I/O functions with only a few memory locations to large RAM arrays with hundreds of Megabytes of storage. The addressing mode is determined by a special 6-bit code which is placed on 6 dedicated VMEbus lines by the current VMEbus Master and is known as the Address Modifier Code, or AM Code.

The VMEbus specification defines the usage of certain AM codes as shown in Table 3-1. The Model 4261 responds only to the AM codes shown in ***italic*** type. Other codes may be included by modifying the AM Code PROM (U56 on the VMEbus board, type 82S129).

Table 3-1: Model 4261 - VME Address Modifier Codes

HEX Code	Addr Space	Function	HEX Code	Addr Space	Function
3F	A24	Standard Supervisory Block Transfer	0F	A32	Extended Supervisory Block Transfer
3E	***A24***	***Standard Supervisory Program Access***	***0E***	***A32***	***Extended Supervisory Program Access***
3D	***A24***	***Standard Supervisory Data Access***	***0D***	***A32***	***Extended Supervisory Data Access***
3B	A24	Standard Nonpriviledged Block Transfer	0B	A32	Extended Nonpriviledged Block Transfer
3A	***A24***	***Standard Nonprivileged Program Access***	***0A***	***A32***	***Extended Nonprivileged Program Access***
39	***A24***	***Standard Nonprivileged Data Access***	***09***	***A32***	***Extended Nonprivileged Data Access***
2D	***A16***	***Short Supervisory Access***	10 thru 1F		User-Defined
29	***A16***	***Short Nonprivileged Access***	all others		RESERVED

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3.3 VMEbus Memory Map

The VMEbus sees the Model 4261 as two regions of memory:

1) A16 memory space is used for the Control Registers, TAG Section and VME FIFO. Most of your programming operations will be performed in this region.

2) A24 or A32 memory space for the VME RAM. This region is seldom used in most applications.

3.3.1 A16 Address Space Memory Map

The A16 address space memory map, for both reads and writes, is shown in Table 3-2, below. Note that most of the registers are read/write access with the exceptions of the Interrupt ID Vector Register (write only), the Status Register (read only) and the Interrupt Status Register (read only). All addresses shown are expressed in hexadecimal notation.

To access these registers the VMEbus master device which conducts the read or write cycle must select A16 address space by using AM codes 2D or 29 (see Section 3.2.1, previous page).

The A16 Base Address for the Model 4261 is determined by the jumpers described in Section 2.4.1. The A16 memory space occupied by the Model 4261 is a 256 byte block starting at this base address. All accesses within this block will handshake with the VMEbus, and **no other VMEbus device should be mapped within this same 256 byte region of A16 address space.** If more than one Model 4261 is used per card cage, arrange the base address jumper assignments to provide a unique address for each board.

Table 3-2: Model 4261 - A16 Address Space Memory Map

Address (hex)	WRITE Access	READ Access
A16_base+0x0000	CTC # 0 - Block Size A	CTC # 0 - Block Size A
A16_base+0x0002	CTC # 1 - Block Size B	CTC # 1 - Block Size B
A16_base+0x0004	CTC # 2 - Sample Clk Divider	CTC # 2 - Sample Clk Divider
A16_base+0x0006	CTC Control	CTC Control
A16_base+0x0010	Interrupt ID Vector	Status Register
A16_base+0x0012	Interrupt Mask Register	Interrupt Mask Register
A16_base+0x0014	Command Register	Command Register
A16_base+0x0016	Trigger Register	Trigger Register
A16_base+0x0018	(Reserved)	(Reserved)
A16_base+0x001A	Tag Command Register	Tag Command Register
A16_base+0x001C	Tag Data Register	Tag Data Register
A16_base+0x001E	–	Interrupt Status Register
A16_base+0x0030	VME FIFO Write Port	VME FIFO Read Port

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3.4 A16 Address Space Registers

Each of the registers shown in the A16 Address Space Memory Map will be described in detail in the subsections below.

3.4.1 **Command Register** - Read/Write @ A16_base+0x0014

The Command Register is an 8-bit read/write register which is used to control RAM Bank assignment, data mode, reset, and start/stop control.

Table 3-3: Model 4261 Command Register - A16_base+0x0014 - R/W Access

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	**VME Enable**	**Word Size**	**Start Mode**	**Reset Mode**	**Bank Load**	**Bank B Top Count**	**Bank A Top Count**	**Bank Select**
'0' Level Function	VME Data Path OFF	16-bit VME Transfers	START Mode OFF	RESET Mode ON	Bank Load Release	Bank B Top Count OFF	Bank A Top Count OFF	Bank A In Bank B Out
'1' Level Function	VME Data Path ON	32-bit VME Transfers	START Mode ON	RESET Mode OFF	Bank Load Setup	Bank B Top Count ON	Bank A Top Count ON	Bank A Out Bank B In
Power On or Reset Condition: All Bits Cleared to '0' state								

3.4.1.1 VME Enable - Bit D7

The VME Enable bit is used to establish the data path between the VMEbus and the VME RAM or the VME FIFO, whichever is selected. When this bit is set to logic '1' and bit D7 of the Interrupt Mask Register (Parallel Port Enable) is cleared to logic '0', the VMEbus path is enabled. When the VME Enable bit is cleared to logic '0', the VMEbus data path is disabled. The relationship between the VME Enable bit and the Parallel Port Enable bit is shown in Table 3-4, below. Normally, the two bits will be set as complements, selecting one path or the other.

Table 3-4: Model 4261 - VMEbus/ Front Panel Parallel Port Selection

Active Path	VME Enable Bit	Parallel Port Enable Bit
None	0	0
VMEbus	1	0
Parallel Port	0	1
Illegal Setting	1	1

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3.4 A16 Address Space Registers (continued)

3.4.1 Command Register (continued)

3.4.1.2 VMEbus Word Size - Bit D6

When the VME data path is enabled, the data transfer word width on the VMEbus is specified by this bit. When this bit is cleared to logic '0', 16-bit transfers are enabled (D16 transfers) and when it is set to logic '1', 32-bit transfers are enabled (D32 transfers).

For D16 transfers each sample from the A/D converter is a 12-bit value, top justified in a 16-bit field. VMEbus data bus bits D00 through D15 are used.

For D32 transfers, two 16-bit words are presented in parallel, each with 12-bit A/D samples top justified within each 16-bit field. The less significant 16-bit word (VMEbus data bits D00 through D15) contains the lower address sample and the more significant 16-bit word (D16 through D31) contains the higher address sample. From a time line perspective, the lower order word contains the earlier sample. See sections 3.4.11 and 3.5 for for details.

3.4.1.3 Start Mode - Bit D5

The Start Mode bit is used to enable all the read and write functions of the Data RAM. This includes writes by the A/D Converter, VMEbus reads and writes, and Parallel Port reads. This bit is provided to allow the programmer to 'freeze' all Data RAM activity for the purpose of monitoring status and changing control functions such as bank selection.

When the Start Mode bit is cleared logic '0', the Start Mode is OFF, i. e., Data RAM operations are disabled. When the bit is set to logic '1', the Start Mode is ON, i. e., Data RAM operations are enabled.

3.4.1.4 Reset Mode - Bit D4

The Reset Mode bit is used to reset all functions on the board. When the Reset Mode is ON, the circuits listed in Table 3-5, on the following page, are affected in the manner indicated in the table. When the Reset Mode bit is cleared to logic '0', the Reset Mode is ON, i. e., the 4261 is held in the reset state. When the bit is set to logic '1', the Reset Mode is OFF, and the 4261 is free to acquire data.

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3.4 A16 Address Space Registers (continued)

3.4.1 Command Register (continued)

3.4.1.4 Reset Mode (continued)

Table 3-5: Model 4261 Reset Mode Operation	
Section Affected	**Reset Mode Action**
DATA RAM Counters	Cleared to zero count
DATA RAM I/O Buffers	Cleared to Empty
Bank Select Flip Flop (FF)	Bank A = Input, Bank B = Output
Bank A Top Count FF	Cleared to OFF
Bank B Top Count FF	Set to ON
RUN Flip Flop	Cleared to OFF
Interrupt Status Register	Cleared to '0's
Interrupt Mask Register	Cleared to '0's
Parallel Port Enable Bit	Cleared to '0'
Interrrupt Flip Flop	Cleared to OFF

3.4.1.5 Bank Load - Bit D3

The Bank Load provides a programmed means to change the state of three flip-flops which control the Data RAM operation. These three flip-flops are the Bank A Top Count FF, Bank B Top Count FF, and the Bank Select FF. The states of these flip-flops are normally controlled by the Sample Control logic and Data RAM Counter logic and support the automatic buffer swapping features of the Data RAM.

It may be desirable in some applications to force the states of these flip-flops by software control to achieve a particular function. The Bank Load bit is used to 'clock in' the three logic levels in bits D2, D1, and D0 of this register into the three flip-flops.

Normally, the Bank Load bit is cleared to logic '0'. In order to change the state of the three flip-flops, first set the Start Mode bit to OFF (i. e., clear bit D5 of this register to logic '0') and set the desired bit pattern in bits D2, D1, and D0 of this register. Then pulse the Bank Load bit high, i. e., first set D3 to logic '1' and then clear it back to logic '0'. The process above is usually referred to as a Bank Load sequence.

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3.4 A16 Address Space Registers (continued)

3.4.1 Command Register (continued)

3.4.1.6 Bank B and Bank A Top Count Bits - Bits D2 and D1

These bits allow the programmer to change the state of the Top Count flip-flops for Bank A and Bank B. Generally, the states of these flip-flops are controlled by the Sample Control logic and Data RAM Counter hardware. The hardware sets these flip-flops when the associated data bank is full. In general, there is no need for the user to set them directly.

However, should the user feel the need to intervene, the Top Count flip-flops will be set to the logic levels programmed in bits D2 and D1 of this register, respectively, after the Bank Load bit (bit D3) is toggled from logic '0' to logic '1' and then back to logic '0' as described in Section 3.4.1.5.

When bit D1 or D2 is cleared to logic '0', that bank's Top Count flip-flop will be set OFF following a Bank Load sequence. When bit D1 or D2 is set to logic '1', that bank's Top Count flip-flop will be set ON following a Bank Load sequence.

3.4.1.7 Bank Select - Bit D0

This bit allows the programmer to change the state of the Bank Select flip-flop. Again, this flip-flop is usually controlled by hardware, without user intervention. The flip-flop will be set to the logic level programmed in bit D0 of this register after the Bank Load bit is toggled from logic '0' to logic '1' and then back to logic '0' as described in section 3.4.1.5.

When bit D0 is cleared to logic '0', the Bank Select mode will be changed for Bank A = Input and Bank B = Output following a Bank Load sequence. When bit D0 is set to logic '1', the Bank Select mode will be changed for Bank B = Input and Bank A = Output following a Bank Load sequence.

3.4.2 **Status Register** - Read Only @ A16_base+0x0010

The Status Register is used to interrogate the board for operational conditions of the Data RAM and its control logic. All of the conditions represented by the bits in the Status Register are monitored in 'real time' and follow any instantaneous changes that may occur during data collection and distribution. Table 3-6, at the top of the next page, gives the bit definition of the Model 4261's Status Register.

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3.4 A16 Address Space Registers (continued)

3.4.2 Status Register (continued)

Table 3-6: Model 4261 - Status Register - A16_base+0x0010 - Read Only Access

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	**Output Ready**	**Input Ready**	**Bank A Top Count**	**Bank B Top Count**	**Bank A Write**	**Bank B Write**	**Bank A Read**	**Bank B Read**
'0' Level Function	***Output Data NOT READY***	NOT Ready for Input Data	***NOT At Top Count***	NOT At Top Count	***Bank A Write NOT ACTIVE***	***Bank B Write NOT ACTIVE***	***Bank A Read NOT ACTIVE***	***Bank B Read NOT ACTIVE***
'1' Level Function	Output Data READY	***READY for Input Data***	At Top Count & Stopped	***At Top Count & Stopped***	Bank A Write ACTIVE	Bank B Write ACTIVE	Bank A Read ACTIVE	Bank B Read ACTIVE
Power On and Reset Conditions Shown In ***Italic*** Type								

3.4.2.1 Output Ready - Bit D7

When the Output Ready bit is at logic '0', no data is available at the output of the Data RAM regardless of its destination: the VME FIFO, VME RAM, or Parallel Port. When this bit is at logic '1', at least one sample is available at the output.

3.4.2.2 Input Ready - Bit D6

When the Input Ready bit is at logic '0', the input to the Data RAM can not accept new data. This status applies both to inputs from the A/D converter and from the VMEbus. If a sample is entered in spite of a NOT READY condition, it will be lost. When this bit is at logic '1', at least one sample can be accepted by the Data RAM.

3.4.2.3 Bank A Top Count and Bank B Top Count - Bits D5 and D4

The Bank A and Bank B Top Count bits indicate the status of the Top Count flip-flops in the RAM Counter control circuitry. The bits will be at logic '1' when the number of samples written into the input Data RAM buffer or read out from the output Data RAM buffer equals the programmed Block Size -AND- the buffer has not yet 'flipped' to the opposite mode. For example, this will occur in the input buffer if it becomes full and the output buffer has not yet emptied.

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3.4 A16 Address Space Registers (continued)

3.4.2 Status Register (continued)

3.4.2.4 Bank A Write and Bank B Write - Bits D3 and D2

When the Sample Control logic has set up Bank A or Bank B for write operation, the associated bit will be appropriately set to logic '1'. As long as this bank is capable of accepting data, the bit will remain set.

When one of these bits becomes a logic '0', the associated bank is not able to accept data. These bits may be monitored as part of diagnostic or control routines to determine the operating state of the unit.

3.4.2.5 Bank A Read and Bank B Read - Bits D1 and D0

When the Sample Control logic has set up Bank A or Bank B for read operation, the associated bit will be appropriately set to logic '1'. As long as this bank is capable of reading data, the bit will remain set.

When one of these bits becomes a logic '0', the associated bank is not capable of delivering output data. These bits may be monitored as part of diagnostic or control routines to determine the operating state of the unit.

3.4.3 Interrupt Mask Register - Read/Write @ A16_base+0x0012

The Interrupt Mask Register allows the programmer to determine the which of the resources on the Model 4261 may issue interrupts to the VMEbus. When a bit in the mask register is set to logic '1', the interrupt source is enabled and when the bit is cleared to logic '0', the interrupt source is 'masked' or blocked from asserting an interrupt.

The interrupt sources may be OR'ed by setting more than one interrupt mask bit to logic '1'. In this case, the Interrupt Status Register (at address A16_base+0x001E, see Section 3.4.4) may be polled to determine the source of the interrupt.

NOTE: Bit D7 of this register is different from bits D0 through D6 in that is **NOT** an interrupt mask bit. Instead it is a control bit used to enable the front panel Parallel Port. See the discussion in Section 3.4.3.1.

The bit definition for the Interrupt Mask Register is shown in Table 3-7, at the top of the next page.

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3.4 A16 Address Space Registers (continued)

3.4.3 Interrupt Mask Register (continued)

Table 3-7: Model 4261 - Interrupt Mask Register - A16_base+0x0012 - R/W Access								
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	**Parallel Port Enable**	**End of RUN**	**Start of RUN**	**Bank Swap**	**Bank A Top Count**	**Bank B Top Count**	**A/D Overrrun**	**A/D Overload**
'0' Level Function	Parallel Port NOT Enabled	NOT Enabled	NOT Enabled	NOT Enabled	NOT Enabled	NOT Enabled	NOT Enabled	NOT Enabled
'1' Level Function	Parallel Port Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
Power On or Reset Condition: All Bits Cleared to '0' state								

3.4.3.1 Parallel Port Enable - Bit D7

The Front Panel Parallel Port is enabled by setting this bit to logic '1' and clearing the VME Enable bit (Command Register, bit D7) to logic '0'. Normally, the two bits will be set as complements, selecting one path or the other. See the discussion in section 3.4.1.1. Note again that this bit is different from the other bits in the Interrupt Mask register. Below, we repeat the table describing the relationship between the path enable bits.

Table 3-8: Model 4261 - VMEbus/ Front Panel Parallel Port Selection		
Active Path	**VME Enable Bit**	**Parallel Port Enable Bit**
None	0	0
VMEbus	1	0
Parallel Port	0	1
Illegal Setting	1	1

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3.4 A16 Address Space Registers (continued)

3.4.3 Interrupt Mask Register (continued)

3.4.3.2 End of RUN - Bit D6

The RUN flip-flop controls the writing of data into the input bank. When RUN is true, data is being collected and when when it is false data collection halts. When the End of RUN bit is set to logic '1', the transition of the RUN flip-flop from true to false will assert a VMEbus interrupt.

When this bit is cleared to logic '0', this interrupt source is masked off.

3.4.3.3 Start of RUN - Bit D5

The RUN flip-flop controls the writing of data into the input bank. When RUN is true, data is being collected and when when it is false data collection halts. When the Start of RUN bit is set to logic '1', the transition of the RUN flip-flop from false to true will assert a VMEbus interrupt.

When this bit is cleared to logic '0', this interrupt source is masked off.

3.4.3.4 Bank Swap - Bit D4

When both Bank A and Bank B buffers reach Top Count, they are automatically 'swapped' making the previous input bank (now filled with new data) the output bank, and making the previous output bank (now empty) the input bank. This is a very common choice for interrupt since it tells the VMEbus when new data is ready to be taken. When the Bank Swap bit is set to logic '1', the swapping of banks will assert a VMEbus Interrupt.

When this bit is cleared to logic '0', this interrupt source is masked off.

3.4.3.5 Bank A and Bank B Top Count - Bits D3 and D2

The Top Count flip-flops for each bank become true when the number of data transfers for that bank equal the programmed block size. When one of the Top Count bits is set to logic '1', the transition of the associated Top Count flip-flop from from false to true will assert a VMEbus interrupt.

When one these bit is cleared to logic '0', that interrupt source is masked off.

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3.4 A16 Address Space Registers (continued)

3.4.3.6 A/D Overrun - Bit D1

When the A/D converter attempts to write data into the input bank and cannot do so because the bank is full or otherwise unavailable, data will be lost. This is called an A/D overrun. If this interrupt mask bit is set to logic '1', then an interrupt will be generated when an A/D overrun occurs.

When this bit is cleared to logic '0', this interrupt source is masked off.

3.4.3.7 A/D Overload - Bit D0

The digital output of the A/D converter is sent to a digital code detector which looks for both positive and negative full scale values. This corresponds to full scale analog voltage present at the input and typically represents an error condition. By setting this interrupt mask bit to logic '1', an interrupt is generated when an overload occurs.

When this bit is cleared to logic '0', this interrupt source is masked off.

3.4.4 Interrupt Status Register - Read Only @ A16_base+0x001E

The Interrupt Status Register allows interrogation of the bits which contribute to VMEbus interrupts. This is a read only register and writes to this address will have no effect. The bit definition is shown in Table 3-9, below.

Table 3-9: Model 4261 - Interrupt Status Register - A16_base+0x001E - Read ONLY Access

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	not used	not used	Bank A Top Count	Bank B Top Count	RUN Flip Flop	Latched Bank Swap	Latched Overrun	Latched Overload
'0' Level Function	-	-	FALSE	FALSE	FALSE	FALSE	FALSE	FALSE
'1' Level Function	-	-	TRUE	TRUE	TRUE	TRUE	TRUE	TRUE
Power On or Reset Condition: All Bits Cleared to '0' state								

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3.4 A16 Address Space Registers (continued)

3.4.4 Interrupt Status Register (continued)

When reading the Interrupt Status Register, bits D7 and D6 will be indeterminate and should be ignored. Bits D5, D4, and D3 reflect the instantaneous status of the conditions shown in Table 3-9.

Bits D2, D1, and D0 are latched and remain true even after the condition which caused the bit to be set has become false. The three latched bits are cleared to logic '0' following a read of the Interrupt Status Register.

3.4.4.1 Bank A and Bank B Top Count - Bits D5 and D4

The Bank A and Bank B Top Count bits indicate the instantaneous status of the Top Count flip-flops in the RAM Counter control circuitry. The bits will be at logic '1' when the number of samples written into the input Data RAM buffer or read out from the output Data RAM buffer equals the programmed Block Size -AND- the buffer has not yet 'flipped' to the opposite mode. For example, this will occur in the input buffer if it becomes full and the output buffer has not yet emptied.

3.4.4.2 Run Flip Flop - Bit D3

This bit tracks the actual, instantaneous status of the RUN flip-flop. In other words, this bit will be at logic '1' if the RUN flip-flop is set, and at logic '0' if the RUN flip-flop is cleared.

3.4.4.3 Latched Bank Swap - Bit D2

When both Bank A and Bank B buffers have reached Top Count, the banks are automatically 'swapped'. Since this is a momentary event, it is latched into D2 of this register for proper identification in an interrupt service routine. This bit will remain set until cleared by an Interrupt Status Register read.

3.4.4.4 Latched Overrun - Bit D1

When the A/D converter attempts to write data into the input bank and cannot do so because the bank is full or otherwise unavailable, data will be lost. This is called an A/D overrun. Since this is a momentary event, it is latched into D1 of this register for proper identification in an interrupt service routine. This bit will remain set until cleared by an Interrupt Status Register read.

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3.4 A16 Address Space Registers (continued)

3.4.4 Interrupt Status Register (continued)

3.4.4.5 Latched Overload - Bit D0

The digital output of the A/D converter is sent to a digital code detector which looks for both positive and negative full scale values. This corresponds to full scale analog voltage present at the input and typically represents an error condition. Since this is a momentary event, it is latched into D0 of this register for proper identification in an interrupt service routine. This bit will remain set until cleared by an Interrupt Status Register read.

3.4.5 Trigger Register - Read/Write @ A16_base+16

The Trigger Register allows the user to capture data by using timing information from external signals. The key hardware element involved is the RUN Flip-Flop (or FF). When the RUN FF is set (true or '1' state), the A/D converter is enabled and data can flow into the input bank. When the RUN FF is cleared (false or '0' state), the A/D converter is disabled and data acquisition ceases. The various bits in the Trigger Register provide several means for setting and clearing the RUN FF. Table 3-10, below, summarizes the functions of this register's bits.

Table 3-10: Model 4261 - Trigger Register - A16_base+0x0016 - R/W Access

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	**not used**	**Auto Arm Mode**	**Trigger Polarity**	**Trigger Mode**	**Sample Clk Select**	**Ext Trigger Enable**	**Clear RUN FF**	**Set RUN FF**
'0' Level Function	-	RUN FF Not Cleared on Bank Swap	Low True or Neg Edge	EDGE Mode ON	Internal Sample Clock	External Trigger Disabled	-	-
'1' Level Function	-	RUN FF Cleared on Bank Swap	High True or Pos Edge	LEVEL Mode ON	External Sample Clock	External Trigger Enabled	Force RUN FF to '0' state	Force RUN FF to '1' state
Power On or Reset Condition: All Bits Cleared to '0' state								

3.4.5.1 Auto Arm Mode - Bit D6

By setting this bit to logic '1', the RUN Flip-Flop is turned off (cleared) at every Bank Swap and is turned on (set) by a new trigger event. This permits triggered data collecting for each block of data.

If this bit is cleared to logic '0', then the RUN Flip Flop will not be cleared at the Bank Swap.

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3.4 A16 Address Space Registers (continued)

3.4.5 Trigger Register (continued)

3.4.5.2 Trigger Polarity - Bit D5

The External Trigger input can be used as an edge sensitive trigger or as a level sensistive 'gate', as determined by the Trigger Mode bit in this register (see Section 3.4.5.3, below.) The External Trigger Enable bit (see Section 3.4.5.5, below) must be set to logic '1' for the external trigger to function. This bit determines the active level or direction of transition that will be recognized as a trigger. Table 3-11, below, shows the relationship between the Trigger Polarity bit and the Trigger Mode bit.

Table 3-11: Model 4261 - Trigger Mode and Polarity

Trigger Polarity (D5)	Trigger Mode (D4)	Mode	RUN Flip Flop Response to External Trigger	
			RUN FF SET	RUN FF CLEARED
0	0	Negative Edge	'1' to '0' edge ↓	–
1	0	Positive Edge	'0' to '1' edge ↑	–
0	1	Negative Level	0	1
1	1	Positive Level	1	0

NOTE: External Trigger Enable bit (D2) must be at logic '1'

3.4.5.3 Trigger Mode - Bit D4

The Trigger Mode bit determines how the External Trigger input signal is used. When this bit is at logic '0' and the External Trigger Enable bit (see Section 3.4.5.5) is set to logic '1', the External Trigger signal is used as an edge-sensitive input, setting the RUN FF on either positive or negative-going edges, determined by the Trigger Polarity bit (see Section 3.4.5.2).

When this bit is at logic '1', the External Trigger input is used as a level sensistive input much like a 'gate' for the sampling clock. The RUN FF follows the level of the External Trigger either inverted or not, as determined by the Trigger Polarity bit. The relationship between the Trigger Mode and the Trigger Polarity bits is shown in Table 3-11, in Section 3.4.5.2, above.

3.4.5.4 Sample Clock Select - Bit D3

The Sample Clock Select bit determines the source of the sample clock. When this bit is cleared to logic '0', the internal sample clock is used. When it is set to logic '1', the External Sample Clock is used. For a discussion of the sample clock operation see Section 3.4.8.

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3.4 A16 Address Space Registers (continued)

3.4.5 Trigger Register (continued)

3.4.5.5 External Trigger Enable - Bit D2

To enable the External Trigger input as a edge- or level-sensitive control signal for the RUN FF, this bit must be set to logic '1'. See the discussions above in sections 3.4.5.2 and 3.4.5.3. When this bit is set to logic '0', the External Trigger input signal is disabled and is ignored entirely.

3.4.5.6 Clear RUN Flip Flop - Bit D1

The Clear RUN FF bit is an overriding reset signal to the RUN Flip-Flop. When this bit is set to logic '1', the RUN FF is reset unconditionally and will not respond to any external trigger commands. This bit also overrides the Set RUN FF bit.

When this bit is cleared to logic '0', the RUN FF is released to respond to trigger signals and the Set RUN FF bit.

3.4.5.7 Set RUN Flip Flop - Bit D0

The Set RUN FF bit is a set signal which overrides any external trigger commands. When this bit is set to logic '1', the RUN FF will be set unless the Clear RUN FF is set to logic '1' (in which case the RUN FF will be cleared).

When this bit is at logic '0', the RUN FF is released to respond to trigger signals.

NOTE: When both the Clear RUN FF and Set RUN FF bits are at logic '1', the RUN FF will be cleared. When both bits are taken from logic '1' to logic '0' simultaneously, the state of the RUN FF is indeterminate. Under normal operation, to guarantee a known state, let only one of these two bits be at logic '1' at a time.

3.4.6 Tag Command Register

- Read/Write @A16_base+0x001A (Model 4261A Only)

The Tag Command Register controls the operation of the 4261A's Tag section which allows the user to supply a 4- or 6-bit address field or 'tag' with every sample delivered to the front panel Parallel Port. This supports the distribution of data to multiple destination devices, each one associated with a specific Tag. The Tags are stored as a table in the Tag RAM which may contain up to 256 entries. Each Tag entry can be used for any number of consecutive samples (Group Size) as determined by the Group Counter.

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3.4 A16 Address Space Registers (continued)

3.4.6 Tag Command Register (continued)

Each bit in the Tag Command Register is shown in Table 3-12, below.

Table 3-12: Model 4261A - Tag Command Register - A16_base+0x001A - R/W Access

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Diagnotic Mode	Tag Page Address 2	Tag Page Address 1	Tag Page Address 0	Tag Output Reg Clear	Tag Reg Select 2	Tag Reg Select 1	Tag Reg Select 0
'0' Level Function	Normal Mode	Selects Tag RAM Page Address (One of eight pages)			CLEAR Tag Output Reg to '0's	Selects Data Path used by Tag Data Buffer for Reading and Writing to:		
'1' Level Function	Diagnostic Mode				Release Tag Output Register	Tag RAM Tag RAM Address Group Preset & Group Counter		
Power On or Reset Condition: All Bits Cleared to '0' state								

The Tag Page Address bits select which one of the eight pages of the Tag RAM is to be used. The Tag Register Select bits 'steer' the Tag Data Buffer to the various elements shown in the block diagram below, Figure 3-2. All data is transferred over an 8-bit data bus which corresponds to bits D0 through D7 of the VMEbus. Data transfers consist of first setting up the Tag Register Select bits of the Tag Command Register and then performing reads and writes on the Tag Data Register directed to the selected element.

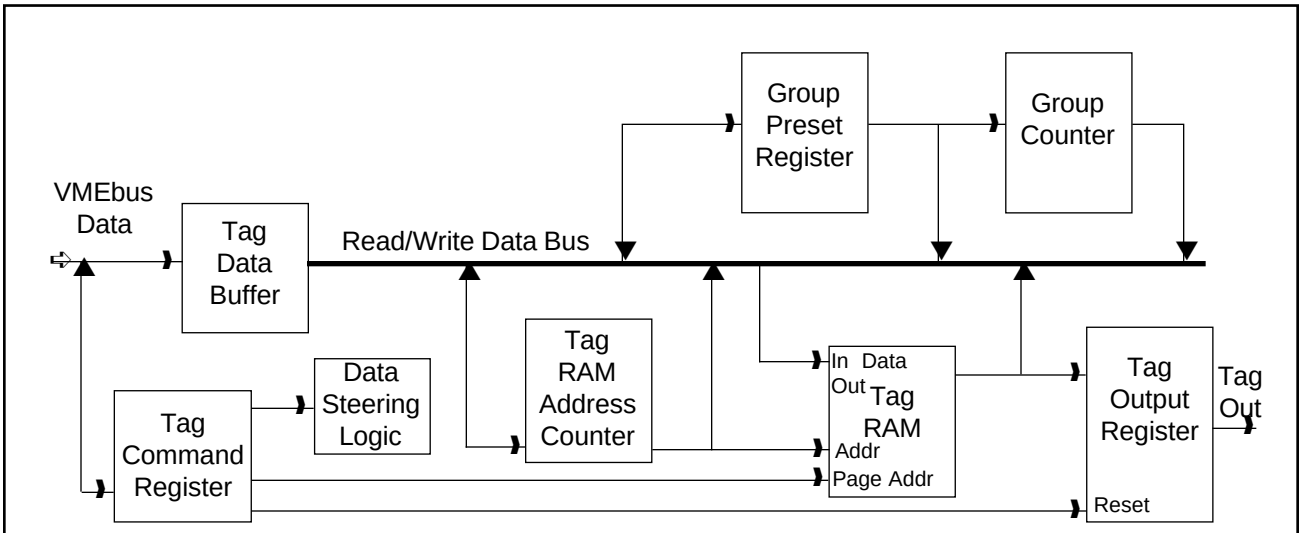


Figure 3-2: Model 4261A Tag Memory and Logic Block Diagram

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3.4 A16 Address Space Registers (continued)

3.4.6 Tag Command Register (continued)

3.4.6.1 Diagnostic Mode - Bit D7

The Diagnostic Mode bit is used for testing at the factory. The user should always leave this bit cleared to logic '0'.

3.4.6.2 Tag RAM Page Address - Bits D6, D5 and D4

These three bits select one of eight pages of Tag RAM, where each page contains 256 entries. This allows eight different setups of Tag patterns to be stored during initialization with fast switching between setups during operation. These bits should be changed prior to accessing the Tag RAM for all reads and writes to the Tag RAM. During operation, these bits may be changed to substitute a new page for the current one. To ensure a coherent transisiton between pages, the following procedure is recommended:

1) CLEAR the RUN Flip-Flop (see Section 3.4.5.6)
2) Change the Tag RAM Page Address (i. e., these bits)
3) Set the Tag RAM Address Counter to zero (see Section 3.4.7.1)
4) Release the RUN FF (see Section 3.4.5.6)

3.4.6.3 Tag Output Register Reset - Bit D3

When this bit is cleared to logic '0', the Tag Output Register, which drives the front panel Tag Bit lines, will be cleared to all '0's. When this bit is set to logic '1', the register is released and may be loaded with the output from the Tag RAM.

3.4.6.4 Tag Data Register Select - Bits D2, D1 and D0

These three bits select which of the elements in the Tag Section are used for reading and writing when using the Tag Data Register. The settings are descrbed in Table 3-13, at the top of the next page.

3.4.7 Tag RAM Data Buffer - Read/Write @ A16_base+0x001C

The Tag Data Buffer is the data path for reading and writing to the various elements in the Tag Section. The Tag Data Buffer is steered by the three Tag Register Select bits (D2, D1 and D0) in the Tag Command Register. The bit definition of this register is shown in Table 3-13, at the top of the next page.

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3.4 A16 Address Space Registers (continued)

3.4.7 Tag RAM Data Buffer (continued)

Table 3-13: Model 4261A Tag Data Buffer - A16_base+0x001C - R/W Access

Tag Reg Select 2	Tag Reg Select 1	Tag Reg Select 0	Select Code	READ Access	WRITE Access
0	0	0	0	Group Counter - 2^0 thru 2^7	Group Counter & Preset Reg - 2^0 thru 2^7
0	0	1	1	Group Counter - 2^8 thru 2^{15}	Group Counter & Preset Reg - 2^8 thru 2^{15}
0	1	0	2	Group Counter - 2^{16} thru 2^{23}	Group Counter & Preset Reg - 2^{16} thru 2^{23}
0	1	1	3	Tag RAM Data	Tag RAM Data
1	0	0	4	Tag RAM Address Counter	Tag RAM Address Counter
1	0	1	5	Group Preset Reg - 2^0 thru 2^7	–
1	1	0	6	Group Preset Reg - 2^8 thru 2^{15}	–
1	1	1	7	Group Preset Reg - 2^{16} thru 2^{23}	–

NOTES: 1) Write Access Requires Start Mode Bit (D5 in Command Register, at A16_base+0x0014) = 0
2) Tag Reg Select bits are D2, D1 and D0 in Tag Command Register, at A16_base+0x001A

3.4.7.1 Tag RAM Address Counter

The Tag RAM Address Counter is an 8-bit binary up counter which addresses the bottom eight bits of the Tag RAM covering a 256 byte page. The Tag RAM Address Counter is a read/write register. It is accessed by setting the Tag Data Register Select bits in the Tag Command Register to 4 (D2 = 1, D1 = D0 = 0.) Writes to this register are enabled only when the Start Mode bit (D5 in the Command Register at A16_base+0x0014) is OFF (at logic '0'). The counter may be read back at any time during operation without interfering with data transfers, although the counter value may be changing during data transfers to the Parallel Port.

This counter is used in the count mode (Start Mode ON) to automatically step through the Tag RAM during normal operation. It is used in the setup mode (Start Mode OFF) as an address register for accessing individual locations in the Tag RAM. See Section 3.4.1.3 for more information about Start Mode.

3.4.7.2 Tag RAM Data

The Tag RAM can be written to and read from by setting up the Tag Register Select bits in the Tag Command Register to 3 (D2 = 0, D1 = D0 = 1.) The address of the Tag RAM is determined by the setting of the Tag RAM Address Counter and the Page Address bits (D6, D5 and D4) in the Tag Command Register. Each address to be accessed must be first explicitly written to the Tag RAM Address Counter.

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3.4 A16 Address Space Registers (continued)

3.4.7 Tag RAM Data Buffer (continued)

3.4.7.2 Tag RAM Data (continued)

Writes to the Tag RAM are enabled only when the Start Mode bit (D5 in the Command Register at A16_base+0x0014) is OFF (at logic '0'). Reads to the Tag RAM are enabled at all times, but the the Tag RAM may be changing if reads are performed during Parallel Port data transfers while the Tag Address Counter is counting. For this reason, it is recommended that transfers be stopped by setting the RUN FF to the OFF state (see Section 3.4.5.6) or the Start Mode to OFF prior to reading.

The format for the bits used by the Tag RAM is shown in Table 3-14, below.

Table 3-14: Model 4261A - Tag RAM Buffer Data Format

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N/U	Last Tag Flag	TA6	TA5	TA4	TA3	TA2	TA1

The six TA bits are the bits which are sent out as the Tag field. The Last Tag Flag is used to denote the last Tag in the tag table. When a byte is encountered in the Tag RAM with this bit is set to logic '1', the Tag RAM Counter resets to zero for the next Tag RAM Address.

For example, suppose four Tags are to be stored in the Tag RAM, for Tag values of 2, 3, 6, and 8. The entries to the Tag RAM would be as shown in Table 3-15, below.

Table 3-15: Model 4261A - Tag RAM Data Example

Tag RAM Address	Desired Tag RAM Data	D6 (Last Tag)	D5 (TA6)	D4 (TA5)	D3 (TA4)	D2 (TA3)	D1 (TA2)	D0 (TA1)	Actual Tag RAM Data
00	02	0	0	0	0	0	1	0	02
01	03	0	0	0	0	0	1	1	03
02	06	0	0	0	0	1	1	0	06
03	08	1	0	0	1	0	0	0	48
NOTE: RAM Addresses and Data are in Hexadecimal, bit values in Binary									

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3.4 A16 Address Space Registers (continued)

3.4.7 Tag RAM Data Buffer (continued)

3.4.7.2 Tag RAM Data (continued)

In this case, the Tag RAM Address counter will continually cycle through the addresses 00, 01, 02, and 03 and then repeat.

Up to 256 Tag entries can be made per page. By setting the Tag Page Address bits to a different page, another seven pages of Tags can be setup for different Tag patterns at the output.

3.4.7.3 Group Preset Register

The Group Size is defined as the number of consecutive data samples sent out of the front panel Parallel Port for each Tag value stored in the Tag RAM. For example, if the Group Size is set for 16, then the first 16 samples are sent out with the first Tag in the Tag RAM, the second 16 are sent out with the second Tag, etc.

The Group Preset Register consists of three 8-bit read/write registers which make up a 24-bit binary Group Size value. The range of allowed settings for the Group Size is from 1 to 2^{23} in steps of 1. Each 8-bit field is separately addressable by first setting up the Tag Register Select bits (D2, D1 and D0 at A16_base+0x001A) in the Tag Command Register to 5, 6 or 7, as shown in Table 3-13, on the page before the previous. Reads and writes performed to A16_base+0x001C will access the field selected by the Tag Register Select bits. For write operations, the START bit in the Command Register (D5 at A16_base+0x0014) must be cleared to logic '0'.

A write to the Group Preset Register also causes a write to the Group Counter. The data stored in these sections is always identical. Reads, however, can be conducted individually for each section.

The Group Size is equal to the 24-bit value programmed in the Group Preset Register + 1. For example, to set a Group Size of 16, the Group Preset Register would be programmed for 15.

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3.4 A16 Address Space Registers (continued)

3.4.7 Tag RAM Data Buffer (continued)

3.4.7.4 Group Counter

The Group Counter is a 24-bit binary down counter. When the count reaches a value of zero, the value of the Group Preset Register is automatically loaded into the Group Counter and the counter begins counting down. The number of counts in a load/count cycle is equal to the number in the Group Preset Register + 1. For example, if the Group Preset Register is programmed to 3, the Group Counter would cycle with 4 states: 3, 2, 1, 0, 3, 2, 1, 0, etc.

Like the Group Preset Register, the Group Counter is viewed from the VMEbus as three 8-bit registers. **The Group Counter is programmed simultaneously with the Group Preset Register.** Writes are enabled only when the Start Mode bit (D5 in the Command Register at A16_base+0x0014) is OFF (at logic '0').

The Group Counter alone can be read back by selecting the appropriate Tag Register Select bits. Reads are enabled at all times, but the counter value may be changing during transfers to the Parallel Port.

3.4.7.5 Operation of the Tag Section

There are two modes of operation of the Tag Section: Start Mode bit OFF (D5 in the Command Register at A16_base+0x0014 = 0, used for setup) and Start Mode bit ON (D5 at A16_base+0x0014 = 1, used for Parallel Port data transfers).

When Start Mode is OFF, all Tag Section devices are accessable for both reading and writing. The Group Preset Register and the Tag RAM should be configured in this mode as described in the preceding sections.

Even though the Group Preset Register does not change as a result of Parallel Port operation, each time the setup mode is entered, the Group Preset Register & Group Counter should be reprogrammed to guarantee a known initial state of the Group Counter. At the end of setup mode, the Tag RAM Address Counter should normally be set to zero so the first Tag is ready to be presented to the Tag Output Register.

When the Start Mode bit is changed from OFF to ON, the following sequence of events occurs:

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3.4 A16 Address Space Registers (continued)

3.4.7 Tag RAM Data Buffer (continued)

3.4.7.5 Operation of the Tag Section (continued)

1) The Group Counter is decremented by one.
2) The Tag Output Register is loaded with the Tag stored at the current Tag RAM Address Counter address.
3) The Tag RAM Address Counter is then incremented by one.
4) The next data sample is presented at the Parallel Port output lines.
5) The Group Counter is enabled to decrement for every Parallel Port output sample.
6) The Tag RAM Address Counter is enabled to increment every time the Group Counter reaches zero and reloads the Group Preset Register count value.

When the Start Mode is changed from ON to OFF, the data transfers out of the Parallel Port are halted and the current state of the Tag Section is held. All elements can now be accessed for both reads and writes.

3.4.8 Counter Timer Circuit

The Counter Timer Circuit (CTC) is used for controlling the Block Size of the RAM Banks and for generating the sample clock. The CTC is an Intel 82C54 device which contains three independent 16-bit programmable counters, each controlled by registers memory mapped to 8-bit locations in A16 address space. The memory map appears as four locations: one for control of the CTC and three for loading parameters for each of the three counter sections.

The three counter sections of the 82C54 are assigned functionally in the Model 4261 as shown in Table 3-2, in Section 3.3.1:

CTC #0: Block Size - RAM Bank A - address A16_base+0x0000

CTC #1: Block Size - RAM Bank B - address A16_base+0x0002

CTC #2: Sample Clock Divider - address A16_base+0x0004

For all three sections, it is recommended that the Mode 2 Rate Generator Mode is used. This produces a single pulse when the initial count has elapsed and then reloads the initial count for another count down cycle. A complete description of the 82C54 is presented in Appendix B of this manual, the 82C54 data sheet.

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3.4 A16 Address Space Registers (continued)

3.4.8 Counter Timer Circuit (continued)

3.4.8.1 CTC Control Section - Read/Write @ A16_base+0x0006

The Control Word format is shown in Table 3-16, below, for reference. The SC bits are used to select the counter to be controlled and the remaining bits define the modes for the selected counter. Typically the counters can be all set for RW1, RW2 = 1,1 for LSB and MSB operation; M2, M1, and M0 = 0,1,0 for Mode 2 Rate Generator; and BCD = 0 for binary mode operation.

Table 3-16: Model 4261 - CTC Control Section - A16_base+0x0006 - R/W Access

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	**SC1**	**SC0**	**RW1**	**RW0**	**M2**	**M1**	**M0**	**BCD**
Settings	Select Counter 0 0 Select CTC #0 0 1 Select CTC #1 1 0 Select CTC #2 1 1 Read Back Cmd		Read/Write Mode 0 0 Counter Latch 0 1 LSB Only 1 0 MSB Only 1 1 LSB & MSB		Mode Select 0 1 0 Mode 2			BCD Set to '0'

Once the Control Word is written for each counter section, the initial count can be sent to each counter by addressing it explicitly, as described in the sections that follow. For example, if all three CTC counters are to be set up for 16-bit divisors (LSB & MSB programming) in binary mode 2 operation, the following three hexadecimal bytes can be sent to the Control Word: 0x34, 0x74, and 0xB4 for CTC counters 0, 1, and 2, respectively.

3.4.8.2 Block Size Counters (CTC #0 and CTC #1) - Read/Write @ A16_base+0x0000 (Counter A) and A16_base+0x0002(Counter B)

The Block Sizes for Bank A and Bank B are determined by the Block Size Counter A and Block Size Counter B implemented in sections CTC #0 and CTC #1, respectively. The formula for the Block Size is expressed as:

Block Size = N times Word Clock

where: N = programmed CTC divisor . . . $2 \leq N \leq 65{,}535$

The Word Clock is determined by the Block Size Jumpers described in Section 2.5. The range of values is presented in Table 3-17, at the top of the next page, reproduced from Table 2-6 in Section 2.5.

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3.4 A16 Address Space Registers (continued)

3.4.8 Counter Timer Circuit (continued)

3.4.8.2 Block Size Counters (CTC #0 and CTC #1) (continued)

Table 3-17: Model 4261 - DRAM Block Size Jumper Settings

Word Clock	Minimum Block Size (N = 2)	Maximum Block Size (N = 65,535)	Divisor (N) Resolution	Block Size Resolution	RAM Bank A Jumper	RAM Bank B Jumper
4	8	2^{18} - 8 = 262,136	2	8	JP7-1,9	JP6-1,9
8	16	2^{19} - 8 = 524,280	1	8	JP7-2,10	JP6-2,10
16	32	2^{20} - 16 = 1,048,560	1	16	JP7-3,11	JP6-3,11
32	64	2^{21} - 32 = 2,097,120	1	32	JP7-4,12	JP6-4,12
64	128	2^{22} - 64 = 4,194,240	1	64	JP7-5,13	JP6-5,13
128	256	2^{23} - 128 = 8,388,480	1	128	JP7-6,14	JP6-6,14
256	512	2^{24} - 256 = 16,776,960	1	256	JP7-7,15	JP6-7,15
512	1024	2^{25} - 512 = 33,553,920	1	512	JP7-8,16	JP6-8,16

NOTES: 1) One, and only one, jumper per bank may (and must) be installed.
2) For Word Clock = 4, Divisor (N) MUST be an even integer.
3) This table applies to 4261 Main Board (320-42610) Revisions C and higher.

The first step in determining which setting to use is to find out which settings bracket the desired value with minimum and maximum limits. The second step is to determine which of those settings permits the resolution required to achieve the exact setting. There may be more than one valid combination of jumper settings and divisor values.

For example, for a Block Size of 400 samples, the Minimum and Maximum Block Size columns show that using any Word Clock from 4 through 128 is acceptable. Since 400 is multiple of 4, 8 and 16, Word Clocks of 4, 8 or 16 could be used (with N = 100, 50, or 25 respectively). However, since 400 is not a multiple of 32, 64 or 128, these Word Clocks cannot be used. Here, there are three equally valid choices for a word clock / divisor combination: 4 x 100, 8 x 50, and 16 x 25.

When programming the CTC divisor values in the 16-bit divisor mode, two sequential bytes are sent to the appropriate CTC section address: **the first byte sent is the least significant byte and the second is the most significant byte.**

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3.4 A16 Address Space Registers (continued)

3.4.8 Counter Timer Circuit (continued)

3.4.8.2 Block Size Counters (CTC #0 and CTC #1) (continued)

Suppose we select the first case for a Word Clock of 4. After setting the Block Size Jumpers for JP7, 1-9 and JP6, 1-9, we program a divisor of 100 by sending two successive hexadecimal divisor bytes of 64_{16} and 00_{16}, first to address A16_base+0x0000 (for CTC #0) and then to address A16_base+0x0002 (for CTC #1), a total of four transfers. This programs both Bank A and Bank B Block Size Counters for a divisor of 100. The 16-bit hex divisor is $0064_{16} = 100_{10}$.

As another example, suppose that a Block Size of exactly 1 million samples is required. In this case, the min/max limits require a Word Clock of 16 or greater. Since 1,000,000 is exactly divisible only by 16, 32 and 64, there are three choices: Word Clocks of 16, 32 or 64, with N = 62,500, 31,250 or 15,625 respectively.

Suppose we select a Word Clock = 32. After setting the Block Size Jumpers for JP7, 8-16 and JP6, 8-16, we program a divisor of 31,250 by sending two succesive hexadecimal divisor bytes of 12_{16} and $7A_{16}$, first to address A16_base+0x0000, and then to address A16_base+0x0002. The 16-bit hex divisor is $7A12_{16} = 31{,}250_{10}$.

3.4.8.3 Sample Clock Divider (CTC #2) - Read/Write @ A16_base+0x0004

The Sample Clock is generated by selecting either the internal 10 MHz crystal oscillator or the External Sample Clock from the front panel BNC (using bit D3 of the Trigger Register at A16_Base+0x0016, as described in Section 3.4.5.4) and using the selected source as the input to the 16-bit programmable divider implemented as CTC #2.

The formula for the effective sampling clock frequency is expressed as:

$$\text{Sample Clock} = \frac{\text{Input Clock}}{N}$$

where: N = programmed CTC #2 divisor . . . $1 \leq N \leq 65{,}535$

When programming the CTC #2 divisor values in the 16-bit divisor mode, two sequential bytes are sent to address A16_base+0x0004: **the first byte sent is the least significant byte and the second is the most significant byte.**

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3.4 A16 Address Space Registers (continued)

3.4.8 Counter Timer Circuit (continued)

3.4.8.3 Sample Clock Divider (CTC #2) (continued)

For example, to program a sampling rate of 80 kHz using the internal 10 MHz oscillator, the required divisor is 125. First clear bit D3 of the Trigger Register (at A16_base+0x0016) to logic '0', to select the internal oscillator. Then program a divisor of 125 by sending two successive hexadecimal divisor bytes of $7D_{16}$ and 00_{16} to address A16_base+0x0004. The 16-bit hex divisor is $007D_{16} = 125_{10}$.

NOTE: There is no mechanism in the Model 4261, option 010 (14-bit, 5 MHz) to prevent the setting of the sample rate divider to 1. This amounts to an attempt to operate the unit at twice its specified maximum sampling frequency. On these units, the divider **MUST** be programmed for 2 or more.

3.4.9 Interrupt ID Vector Register - Write Only @ A16_base+0x0010

The Interrupt ID Vector Register stores the interrupt acknowledge ID byte vector which the VMEbus uses to identify the source of an interrupt. This vector is an 8-bit value which is placed on the VMEbus data lines D0 through D7 in response to an interrupt acknowledge (IACK) cycle. The ID Vector Register is a write only register. See section 3.6 for a discussion of interrupts. Table 3-18, below, summarizes the bits in this regster.

Table 3-18: Model 4261- Interrupt ID Vector Register - A16_base+0x0010 - Write Only Access

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

3.4.10 VME FIFO Read/Write Port - Read/Write @ A16_base+0x0030

The most efficient method available in the Model 4261 for delivering data to the VMEbus is via its FIFO. The FIFO appears as a single memory location in A16 memory space, at A16_base+0x0030. In order to facilitate this mode, the following configuration settings must be made:

1) Clear the Parallel Port Enable bit (D7) in the Interrupt Mask Register (A16_base+0x0012) to logic '0' (see Section 3.4.3.1.)

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3.4 A16 Address Space Registers (continued)

3.4.10 VME FIFO Read/Write Port (continued)

2) Set the VME Enable bit (D7) in the Command Register (A16_base+0x0014) to logic '1' (see Section 3.4.1.1.)

3) Clear the Word Size bit (D6) in the Command Register (A16_base+0x0014) to logic '0', for 16-bit bus transfers, or set it to '1' for 32-bit bus transfers (see Section 3.4.1.2.)

Note that there are actually two FIFO registers included on the Model 4261 (see the block diagram on page 29), one at the input side of the RAM array, and the other at the output side of the RAM array. The input FIFO provides a place store data while the banks are being switched, and the output FIFO provides a cache of available data that may be read during the bank switch process. Each FIFO is 64 samples deep, and data is moved in and out of the FIFOs four samples at a time.

3.4.10.1 VME FIFO Read Operation

As soon as a memory bank is 'swapped' from the input path to the output path, the data in the bank becomes available to the VMEbus for reads at location A16_base+0x0030. The first sample written into the bank by the A/D Converter during its input mode will be the first sample available at the output.

The number of samples available equals the Block Size. After the last sample has been read, one of two events occur. If the input bank is full, the banks will swap and the new buffer will be available for reads. If the input bank is not full, the unit will wait for it to fill and in the meantime, the Output Ready bit in the Status Register will be at logic '0'.

The data format for output data is shown in Table 3-19, below, for both 16-bit and 32-bit modes. The format presented in this table assumes a unit equipped with a 12-bit ADC. If a 14-bit A/D is installed, then D2 (and D18 in 32-bit mode) are the lsbs of the 14-bit samples, and D3 (and D19) are active data bits.

Table 3-19: Model 4261 - VME FIFO Data Format - Read Operation

Bits	D31 - - - - - D20	D19* D18* D17 D16	D15 - - - - D4	D3* D2* D1 D0
16-bit	not driven	not driven	msb ----Sample(n)---- lsb	0* 0* 0 0
32-bit	msb ----Sample(n+1)---- lsb	0* 0* 0 0	msb ----Sample(n)---- lsb	0* 0* 0 0

*NOTE: for 14-bit units, D2 (and D18, in 32-bit output mode) are sample lsb's, and D3 (and D19) are not always 0.

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3.4 A16 Address Space Registers (continued)

3.4.10 VME FIFO Read/Write Port (continued)

3.4.10.1 VME FIFO Read Operation (continued)

In 16-bit data mode, with a 12-bit A/D Converter, the 12-bits of each sample are top justified with the D15 - D4 VME data bus and bits D3 through D0 are set to zero. For a 14-bit ADC in 16-bit data mode, the data is justified in bits D15 - D2, and only bits D1 and D0 will be constant zeros. Bits D31 through D16 are not driven in 16-bit data mode.

In 32-bit data mode, VME bus data bits D15 - D0 are the same as for 16-bit mode. With a 12-bit ADC, bits D31 - D20 contain the next data sample, top justified with bits D19 through D16 set to zero. With a 14-bit A/D Converter, the next sample is contained in bits D31 - D18, with bits D17 and D16 set to zero.

3.4.10.2 VME FIFO Write Operation

Although not optimized for this function, the design of the Model 4261 permits its use as a FIFO-based VME memory array. As soon as a memory bank is 'swapped' from the output path to the input path, the bank is empty and becomes available to the VMEbus for writes to location A16_base+0x0030. Before attempting to write any data, the RUN Flip-Flop should be set to OFF, by setting the D2 bit of the Trigger Register, at A16_base+0x0016, to a logic '1'.

The number of samples which will be accepted equals the Block Size. As data is written into the bank, it passes first through a staging section which transfers data in blocks of 8 samples into the bank. If the number of samples written from the VMEbus is not equal to a multiple of 8, then the excess 1 to 7 samples will be lost if the banks are prematurely swapped by software control.

Data formatting is shown in Table 3-20, at the top of the next page. For 16-bit transfers on a 12-bit unit, data in bits D0 through D3 and D16 through D31 are ignored. For 16-bit transfers on a 14-bit unit, data in bits D0, D1, and D16 - D31 are ignored. For 32-bit transfers on a 12-bit device, data in bit positions D0 through D3 and D16 through D19 will be ignored. For 32-bit transfers on a 14-bit 4261, data in bit positions D0, D1, D16 and D17 will be ignored.

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3.4 A16 Address Space Registers (continued)

3.4.10 VME FIFO Read/Write Port (continued)

3.4.10.2 VME FIFO Write Operation (continued)

Table 3-20: Model 4261 - VME FIFO Data Format - Write Operation

Bits	D31 - - - - - D20	D19* D18* D17 D16	D15 - - - - D4	D3* D2* D1 D0
16-bit	x - - - - - x	x x x x	msb ----Sample(n)---- lsb	y y x x
32-bit	msb ----Sample(n+1)---- lsb	y y x x	msb ----Sample(n)---- lsb	y y x x

x = don't care, bit values are ignored . . . y = active bits on 14-bit units, don't care on 12-bit units
* - lsbs for 14-bit units

3.5 VME RAM Data Access - A24 and A32 Address Space - Read Only

Direct VMEbus access to the RAM array on the Model 4261 is a process that requires several microseconds per access. Also, before accessing the RAM array, the Block Size Counters must be disabled (refer to the source code examples in Appendix A or the 82C54 Data Sheet in Appendix B for details). For these reasons, we recommend that the FIFO port be used as the primary mode of reading A/D data out of this device.

The only condition that makes direct access to the 4261's RAM array truly useful is when a large number of "uninteresting" samples have been taken, and these samples precede the desired data in the FIFO. This may occur if there is a long delay between the trigger and the significant portion of the waveform being sampled. In this case, a **single**, direct VMEbus read operation, at the address where the "good" samples begin, will cause the FIFO's pointer to advance to that memory location. After this **ONE** direct RAM read, the remainder of the data may be read from the FIFO.

In order to facilitate this mode, the following configuration settings must be made:

1) Set the A24 and A32 Base Address Jumpers (see Section 2.4.2.)
2) Set the VME RAM Size jumpers (see Section 2.4.3.)
3) Clear the Parallel Port Enable bit (D7) in the Interrupt Mask Register (A16_base+0x0012) to logic '0' (see Section 3.4.3.1.)
4) Set the VME Enable bit (D7) in the Command Register (A16_base+0x0014) to logic '1' (see Section 3.4.1.1.)
5) Clear the Word Size bit (D6) in the Command Register (A16_base+0x0014) to logic '0', for 16-bit bus transfers, or set it to '1' for 32-bit bus transfers (see Section 3.4.1.2.)

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3.5 **VME RAM Data Access** - A24 and A32 Address Space (continued)

The RAM bank assigned to the output function is available for random reads from the VMEbus. **The RAM bank assigned to the input function is unavailable to the VME-bus.**

Control of which bank is used for input and which for output is accomplished under program control through the Bank Select bit of the Command Register (see Section 3.3.1.) Bank 'swapping' also occurs automatically when the input bank is full and the output bank is empty.

Status of the banks is revealed by reading the Status Register (see Section 3.2.2.) It is recommended that the Status Register be polled prior to accessing the VME RAM to ensure that the banks are ready for the transfer.

The base address of the memory region is determined by the A24 and A32 Base Address Jumpers and the size of the memory region is determined by the VME RAM Size Jumpers. Refer to the previous sections shown above for details regarding the setting of these jumpers.

The data format for both 16-bit and 32-bit read operations is shown in Table 3-21, below.

Table 3-21: Model 4261 - VME RAM Data Format - Read Operation

Bits	D31 - - - - - D20	D19* D18* D17 D16	D15 - - - - D4	D3* D2* D1 D0
16-bit	not driven	not driven	msb ----Sample(n)---- lsb	0* 0* 0 0
32-bit	msb ----Sample(n+1)---- lsb	0* 0* 0 0	msb ----Sample(n)---- lsb	0* 0* 0 0

*NOTE: for 14-bit units, D2 (and D18, in 32-bit output mode) are sample lsb's, and D3 (and D19) are not always 0.

The first sample at the bottom of the VME RAM is located at the A24 or A32 Base Address. When 16-bit mode transfers are selected, **all accesses must be specified with even addresses**, so that the 16-words are aligned on 2-byte boundaries. When 32-bit mode transfers are selected, **all accesses must be done with addresses which are multiples of four,** so that the 32-bit words are aligned on 4-byte boundaries.

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3.6 Interrupt Operation

The Model 4261 can be used to generate an interrupt an the VMEbus in response to various conditions on the board. Interrupts are setup as follows:

1) Use the Interrupt Jumpers at JP2 and JP7 to set the interrupt level for the VMEbus as described in Section 2.5.

2) Set the Interrupt Mask Register (A16_base+0x0012) to enable any combination of interrupt sources as described in Section 3.4.3

3) The VMEbus interrupt handler should be configured for responding to interrupts on the interrupt level selected by the jumpers in step (1).

4) The VMEbus interrupt handler must load the Interrupt ID Vector Register as described in section 3.4.9.

5) The VMEbus interrupt service routine should perform two functions:

   a) Conduct an interrupt acknowledge (IACK) cycle to retrieve the Interrupt ID Vector to determine which board in the card cage caused the interrupt. The IACK cycle also clears the interrupt flip-flop.

   b) Read the Interrupt Status Register (A16_base+0x001E) to determine the source of the interrupt as described in Section 3.4.4. This will also clear the three latched bits in this register.

3.7 Parallel Port Operation

The Parallel Port electrical interface is described in Section 2.9. The bit definition for the 16-bit Parallel Data bus is shown in Table 3-22, below.

Table 3-22: Model 4261 - Parallel Port Output Data Format

Bit	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Data	msb	- - - - - - - - - - - - - - - -				Sample(n)			- - - - - - - - - - - - - - - -			lsb (12-bit)	–	lsb (14-bit)	0	0

The following steps should be followed when setting up for Parallel Port operation:

1) Set the Parallel Port Enable bit (D7) in the Interrupt Mask Register (A16_base+0x0012) to logic '1' (see Section 3.4.3.1.)

2) Clear the VME Enable bit (D7) in the Command Register (A16_base+0x0014) to logic '0' (see Section 3.4.1.1.)

3) Select the Parallel Port operating mode, Interlocked or Free Run, using the jumper block JP8 (see Section 2.9.1.)

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3.7 **Parallel Port Operation** (continued)

4) Setup the Tag Section as required. After setup, set the Tag Address Counter to zero. If no tags are required, no setup of the Tag Section is required (see Sections 3.4.6 and 3.4.7.)

5) Start the data collection and enable the receiver

The output bank contains the number of samples equal to the Block Size. When the last sample from the output bank is read from the Parallel Port, one of two events will occur:

1) If the input bank is full, the banks will swap automatically and the new bank will be available for reads. The $\overline{\text{DAV}}$ line will indicate that new sam-ples are available and data transfers will continue. This will occur if the average Parallel Port output transfer rate is lower than the input (A/D) sampling rate. Of necessity, during the time between the input bank becoming full and the output bank becoming empty, **input data will be lost.**

2) If the input bank is not full, the unit will wait for it to fill. This will occur if the average output rate is faster than the A/D input sampling rate. While waiting for the input bank to fill, the Output Ready bit in the Status Register will be at logic '0' and the $\overline{\text{DAV}}$ line will remain at logic '1'. As soon as the input bank fills, the banks will swap and $\overline{\text{DAV}}$ will go to logic '0' indicating the first sample from the swapped bank is ready at the output. In this case, **no input data loss will occur.**

During Parallel Port output transfers, the Status Register and the Tag Section can be freely polled by the VMEbus to monitor bank and sample count activity without interfering with the transfers.

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Appendix A: Programming Examples

A.1 Introduction

This Appendix presents two sample C language programs for working with the Pentek Model 4261 A/D Converter. The first example, **p4261.c**, was written to use the Bit3 Model 403 PC-VMEbus Adaptor as the VMEbus Master. The second, **4283_61.c**, was written to use Pentek's Model 4283 TMS320C30 Digital Signal Processor as the VMEbus master. Both examples provide routines that initialize the various sections of the 4261, begin the sampling process, and read data from the FIFO.

A.2 p4261.c

```
#include <stdio.h>
#include <dos.h>

/* The 4261 has the capability of storing data into a FIFO to be read
   from VME in A16 mode, or sending the data to the parallel port */

#define     VME_FIFO_MODE     1
#define     A16BASE 0x8000                  /* 4261 A16 Base Address */
#define     ADOFF 2                                 /* Sets RUN off */
#define     ADCTL 1       /* Sets internal sampling clock and RUN on */
#define     TAG1  0                 /* Sample tag for parallel port */
#define     TAG2  1                 /* Sample tag for parallel port */

void BufSize(unsigned size);                /* Selects Buffer Size */
void initsampling(unsigned div);        /* Initializes sampling rate */
void setup(void);                       /* Initializes BIT-3 Adapter */
void ReadInit(void);        /* Swaps current READ buffer after reset */
void WriteInit(void);   /* Allows VMEbus WRITES into buffer with RUN off */
void Reset(void);               /* Disables buffer address counters */
void FifoInit(void);          /* Allows sequential access to buffer */
void ParInit(void);                     /* Initializes Parallel port */
void TagInit(void);  /* Initialzes TAG RAM circuit for parallel port */
void a16();            /* Bit3 routine for setting A16 Address Modifier */
void setup();                                /* Bit3 Setup routine */
unsigned adctl = ADCTL;
unsigned int vme_seg = 0xd000;              /* Bit3 Window into VME */


void main(void)
{
   unsigned data;

   setup();                    /* Initialize Bit3 PC to VME Adapter */
   a16();                              /* Set A16 Address Modifier */

   initsampling(1);                          /* Sample rate = 10 MHz */
   BufSize(1000);        /* Buffer size = wordclk*100 (default=400) */
```

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A.2 **p4261.c** (continued)

```
   #if VME_FIFO_MODE
      FifoInit();                          /* Initialize FIFO Interface */
      while (1)
      {
         /* Wait for FIFO Not Empty */
         while ((peek(A16BASE, 0x10) & 0x80) == 0);
         data = peek(A16BASE, 0x30);
         printf("data = %lx\n", data);
      }

   #else
      ParInit();                           /* Initialize Parallel Port */

   #endif
}


void ReadInit(void)
{
   poke(vme_seg,A16BASE+0x14,0);                    /* Master reset */
   poke(vme_seg,A16BASE+0x14,0x10);                /* Release Reset */
   poke(vme_seg,A16BASE+0x16,ADOFF);
   poke(vme_seg,A16BASE+0x14,0x93);              /* Input Buffer = B */
   poke(vme_seg,A16BASE+0x14,0x9b);               /* Pulse Bankload */
   poke(vme_seg,A16BASE+0x14,0x93);               /* Reset Bankload */
   poke(vme_seg,A16BASE+0x14,0xb3);                    /* Set Start */
}


void WriteInit(void)
{
   poke(vme_seg,A16BASE+0x14,0);                    /* Master reset */
   poke(vme_seg,A16BASE+0x14,0x10);                /* Release Reset */
   poke(vme_seg,A16BASE+0x16,ADOFF);
   poke(vme_seg,A16BASE+0x14,0xb3);                    /* Set Start */
}


void FifoInit(void)
{
   poke(vme_seg,A16BASE+0x14,0);                    /* Master reset */
   poke(vme_seg,A16BASE+0x14,0x10);                /* Release Reset */
   poke(vme_seg,A16BASE+0x14,0xb0);                    /* Set Start */
   poke(vme_seg,A16BASE+0x16,adctl);
}

void ParInit(void)
{
   poke(vme_seg,A16BASE+0x14,0);                    /* Master reset */
   poke(vme_seg,A16BASE+0x14,0x10);                /* Release Reset */
   poke(vme_seg,A16BASE+0x16,adctl);
   poke(vme_seg,A16BASE+0x12,0x80);                  /* Set pbus on */
   poke(vme_seg,A16BASE+0x14,0x35);                    /* Set Start */
}
```

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A.2 **p4261.c** (continued)

```
void TagInit(void)
{
   poke(vme_seg,A16BASE+0x1a,0);         /* Select block counter lsb */
   poke(vme_seg,A16BASE+0x1c,0x5);           /* Write block size lsb */
   poke(vme_seg,A16BASE+0x1a,1);         /* Select block counter mid */
   poke(vme_seg,A16BASE+0x1c,0);             /* Write block size mid */
   poke(vme_seg,A16BASE+0x1a,2);         /* Select block counter msb */
   poke(vme_seg,A16BASE+0x1c,0);             /* Write block size msb */

   poke(vme_seg,A16BASE+0x1a,4);   /* Select Tag RAM Address counter */
   poke(vme_seg,A16BASE+0x1c,0);            /* Write Tag RAM Address */
   poke(vme_seg,A16BASE+0x1a,3);        /* Select Tag RAM Data input */
   poke(vme_seg,A16BASE+0x1c,1);             /* Write Tag to Tag RAM */

   poke(vme_seg,A16BASE+0x1a,4);   /* Select Tag RAM Address counter */
   poke(vme_seg,A16BASE+0x1c,1);            /* Write Tag RAM Address */
   poke(vme_seg,A16BASE+0x1a,3);        /* Select Tag RAM Data input */

   poke(vme_seg,A16BASE+0x1c,(2 | 0x40));    /* Write Last Tag to Tag RAM */

   poke(vme_seg,A16BASE+0x1a,4);   /* Select Tag RAM Address counter */
   poke(vme_seg,A16BASE+0x1c,0);    /* Write Initial Tag RAM Address */

   poke(vme_seg,A16BASE+0x1a,8);      /* Put Tag circuit in Run Mode */
}


void Reset(void)
{
   /* Disable counters */
   poke(vme_seg,A16BASE+0x6,0x14);   /* Select buffer A mode control */
   poke(vme_seg,A16BASE+0x6,0x54);   /* Select buffer B mode control */
}


void BufSize(unsigned size)
{
   poke(vme_seg,A16BASE+0x6,0x34);   /* Select buffer A mode control */
   poke(vme_seg,A16BASE+0x0,(size & 0xff));      /* set divisor  lsb */
   poke(vme_seg,A16BASE+0x0,(size >> 8));        /* set divisor  msb */

   poke(vme_seg,A16BASE+0x6,0x74);   /* Select buffer B mode control */
   poke(vme_seg,A16BASE+0x2,(size & 0xff));      /* set divisor  lsb */
   poke(vme_seg,A16BASE+0x2,(size >> 8));        /* set divisor  msb */
}
```

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A.2 **p4261.c** (continued)

```
void initsampling(unsigned div)
{
   if(div!=1)                                   /* If less than 10 MHz */
   {
      poke(vme_seg,A16BASE+0x6,0xb4);     /* select 8254 command reg */
      poke(vme_seg,A16BASE+0x4,(div & 0xff));    /* set divisor  lsb */
      poke(vme_seg,A16BASE+0x4,(div >> 8));      /* set divisor  msb */
   }
   else                                              /* 10 MHZ clock */
      poke(vme_seg,A16BASE+0x6,0x90);
}


void setup(void)
{
   int   stat;

   inportb(0x202);
   inportb(0x208);

   if((inportb(0x202) & 1)!=0)
   {
      printf("power cable off\n");
      exit(0);
   }

   outportb(0x200,0x90);
   stat=inportb(0x202) & 0xc5;

   if(stat!=0)
      printf("setup status error\n");

   if((stat & 0x80)!=0)
      printf("parity error\n");

   if((stat & 0x40)!=0)
      printf("bus error\n");

   if((stat & 0x1)!=0)
      printf("power off error\n");

   if(stat==0)
      printf("setup looks good\n\n");

   outportb(0x20d,0x2d);                    /* A16 address modifiers */
   outportb(0x208,0x8);                /* use address page  register */
   outportb(0x20a,0x0);                          /* use bottom page */
   }


void a16()                             /* changes addr modifers to A16 */
{
   outportb(0x20d, 0x2d);                    /* Short Address AM Code */
}
```

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A.3 4283_61.c

```
/* 4283_61.c - This program intializes the 4261 from the 4283 Baseboard */

#define VME_READ   1

/****************** 4261 Globals ***************************************/
volatile unsigned int *PageAddressReg,*AddressModifierReg,*ControlRegister;
volatile unsigned int *DataBuffer,*Status,*DramBuffer,*VMEpointer,data;
/***********************************************************************/

#define A16BASE    0x8000                       /* A16 Base Address */
#define A16        0x29                      /* A16 Address Modifier */


/* 4261 Registers */
#define CTC_0        (A16BASE + 0x00)         /* CTC #0 Block Size A */
#define CTC_1        (A16BASE + 0x02)         /* CTC #1 Block Size B */
#define CTC_2        (A16BASE + 0x04) /* CTC #2 Sample Clock Divider */
#define CTC_CNTL     (A16BASE + 0x06)                /* CTC Control */
#define INTR_ID      (A16BASE + 0x10) /* Intr. ID Vector - Write Only */
#define STATUS       (A16BASE + 0x10) /* Status Register - Read Only */
#define INTR_MASK    (A16BASE + 0x12)             /* Interrupt Mask */
#define COMMAND      (A16BASE + 0x14)                /* Command Reg */
#define TRIGGER      (A16BASE + 0x16)                /* Trigger Reg */
#define TAG_CMD      (A16BASE + 0x1A)                /* Tag Command */
#define TAG_DATA     (A16BASE + 0x1C)                   /* Tag Data */
#define INTR_STATUS  (A16BASE + 0x1E)           /* Interrupt Status */
#define FIFO_PORT    (A16BASE + 0x30)                  /* FIFO Port */


main()
{
   unsigned int i,temp;

   /* Initialize Pointers to 4283 VME Interface Registers */
   ControlRegister = (unsigned int *) 0x800000u;
   PageAddressReg = (unsigned int *) 0x800002u;
   AddressModifierReg = (unsigned int *) 0x800001u;

   /* Set Pointers to 4261 Address Space */
   VMEpointer = (unsigned int *) 0xC00000u + (A16BASE / 4);
   DataBuffer = (unsigned int *) 0xC00000u + (FIFO_PORT / 4);
   Status = (unsigned int *) 0xC00000u + (STATUS / 4);

   /* Initialize pointer to Data Buffer on 4283 */
   DramBuffer = (unsigned int *) 0x201000u;

   /* Set A16 Address Modifier */
   *AddressModifierReg=A16;

   BufSize(1000);                              /* Set Buffer Size */
   initsampling(1);                    /* Set Sampling Rate Divisor */
```

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A.3 4283_61.c (continued)

```
   #if VME_READ
      FifoInit();                        /* Initialize FIFO Interface */
      SetCtl(0x0120);              /* Set Low Order 16 bit Word Cycle */

      while ((*Status & 0x80) == 0);     /* wait for input FIFO half-full */
      for (i=0;i<1024;i++)
      {
         data=*DataBuffer;
         DramBuffer[i]=(data & 0xffff) << 16;
      }

   #else
      ParInit();                          /* Initialize Parallel Port */
   #endif

   while (1);
}


void FifoInit(void)
{
   SetCtl(0x120);                /* Set Low Order 16 bit Word Cycle */
   VMEpointer[5] = 0;                              /* Master reset */
   VMEpointer[5] = 0x10;                          /* Release Reset */
   VMEpointer[5] = 0xb0;                              /* Set Start */
   SetCtl(0x320);               /* Set High Order 16 bit Word Cycle */
   VMEpointer[5] = 0x100b0;                     /* Set Start and Run */
}


void ParInit(void)
{
   SetCtl(0x120);                /* Set Low Order 16 bit Word Cycle */
   VMEpointer[5] = 0;                             /* Master reset  */
   VMEpointer[5] = 0x10;                          /* Release Reset */
   SetCtl(0x320);               /* Set High Order 16 bit Word Cycle */
   VMEpointer[5] = 0x10010;                       /* Release Reset */
   VMEpointer[4] = 0x800000;                        /* Set Pbus ON */
   SetCtl(0x120);                /* Set Low Order 16 bit Word Cycle */
   VMEpointer[5] = 0x35;                              /* Set Start */
}
```

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A.3 **4283_61.c** (continued)

```
void BufSize(unsigned size)
{
   SetCtl(0x320);                /* Set High Order 16 bit Word Cycle */
   VMEpointer[1] = 0x340000;         /* Select buffer A mode control */
   SetCtl(0x120);                 /* Set Low Order 16 bit Word Cycle */
   VMEpointer[0] = (size & 0xff);               /* set divisor  lsb */
   VMEpointer[0] = (size >> 8);                 /* set divisor  msb */

   SetCtl(0x320);                /* Set High Order 16 bit Word Cycle */
   VMEpointer[1] = 0x740000;         /* Select buffer B mode control */
   VMEpointer[0] = ((size & 0xff) << 16);       /* set divisor  lsb */
   VMEpointer[0] = ((size >> 8) << 16);         /* set divisor  msb */
}


void initsampling(unsigned div)
{
   if(div!=1)                           /* If Sample Rate is < 10 MHz */
   {
      SetCtl(0x320);             /* Set High Order 16 bit Word Cycle */
      VMEpointer[1] = 0xb40000;  /* select 8254 command reg and point to ch0 */
      SetCtl(0x120);              /* Set Low Order 16 bit Word Cycle */
      VMEpointer[1] = (div & 0xff);             /* set divisor  lsb */
      VMEpointer[1] = (div >> 8);               /* set divisor  msb */
   }

   else                                 /* Else Sample Rate is 10 MHz */
    {
      SetCtl(0x320);             /* Set High Order 16 bit Word Cycle */
      VMEpointer[1] = 0x900000;
   }
}


SetCtl(int code)
{
   *ControlRegister = code;
}
```

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Appendix B: Intel 82C54 Data Sheet

B.1 Introduction

The Intel 82C54 is a high-performance, CHMOS version of the industry standard 8254 counter/timer, which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 82C54 is pin compatible with the HMOS 8254, and is a superset of the 8253.

Six programmable timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications.

The 82C54 is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent HMOS product. The 82C54 is available in 24-pin DIP and 28-pin plastic leaded chip carrier (PLCC) packages.

B.1.1 Key Features

- ❑ Compatible with all Intel and most other microprocessors
- ❑ High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188
- ❑ Handles Inputs from DC to 8 MHz
- ❑ 10 MHz for 82C54-2
- ❑ Three independent 16-bit counters
- ❑ Completely TTL Compatible
- ❑ Six Programmable Counter Modes
- ❑ Binary or BCD counting
- ❑ Status Read Back Command

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B.2 Functional Description

The 82C54 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

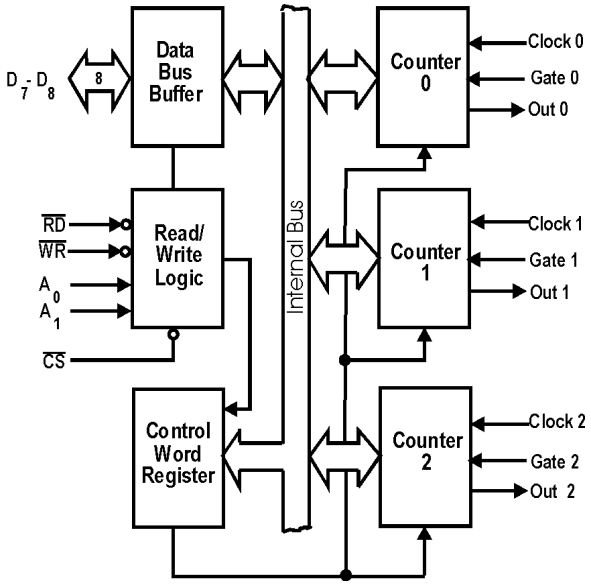


Figure B-1: 82C54 Block Diagram

Some of the other counter/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real Time Clock
- Digital One-shot
- Square Wave Generator
- Complex Waveform Generator
- Event Counter
- Programmable Rate Generator
- Binary Rate Multiplier
- Complex Motor Controller

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B.3 Block Diagram

B.3.1 Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus.

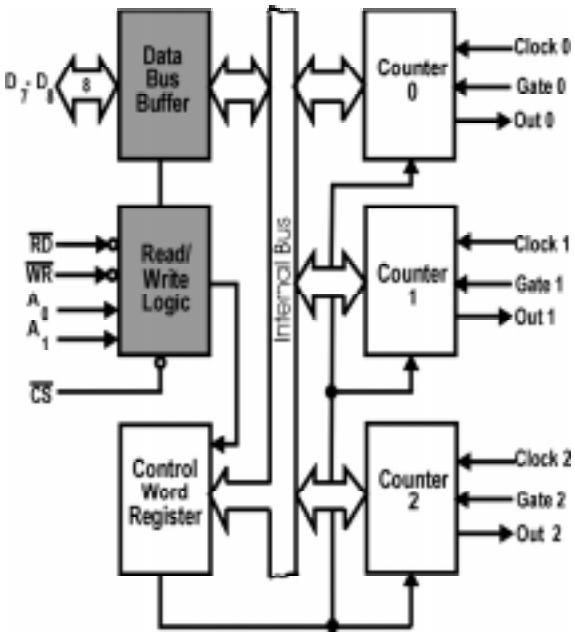


Figure B-2: 82C54 - Block Diagram Showing Data Bus Buffer and Read/Write Logic

B.3.2 Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A_1 and A_0 select one of the three counters or the Control Word Register to be read from or written to. A "low" on the $\overline{RD}$ input tells the 82C54 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 82C54 has been selected by holding $\overline{CS}$ low.

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B.3 Block Diagram (continued)

B.3.3 Control Word Register

The Control Word Register, Figure B-3 below, is selected by the Read/Write Logic when A_1, A_0 = 11. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

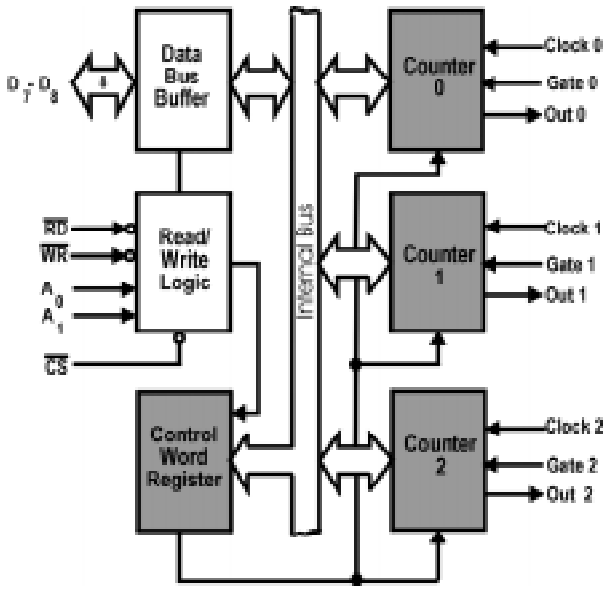


Figure B-3: 82C54 - Block Diagram Showing Control Word Register and Counter

B.3.4 Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure B-4, page 5. The Counters are fully independent. Each Counter may operate in a different mode.

The Control Word Register is also shown in Figure B-4, page 5; it is not part of the Counter itself, but its contents determine how the Counter operates.

The status register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

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B.3 Block Diagram (continued)

B.3.4 Counter 0, Counter 1, Counter 2 (continued)

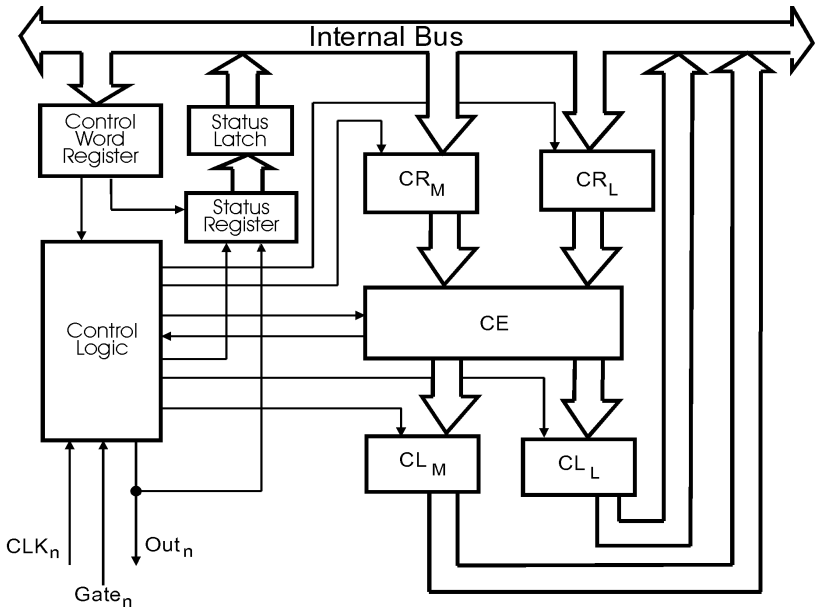


Figure B-4: 82C54 - Internal Block Diagram of a Counter

The actual counter is labelled CE (for "Counting Element"). It is a 16-bit presettable synchronous down counter.

OLM and OLL are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L stand for "Most significant byte" and "Least significant byte" respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CRM and CRL (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CRM and CRL are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

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B.3 Block Diagram (continued)

B.3.4 Counter 0, Counter 1, Counter 2 (continued)

The Control Logic is also shown in the diagram. CLKn, GATEn, and OUTn are all connected to the outside world through the Control Logic.

B.4 82C54 System Interface

The 82C54 is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.

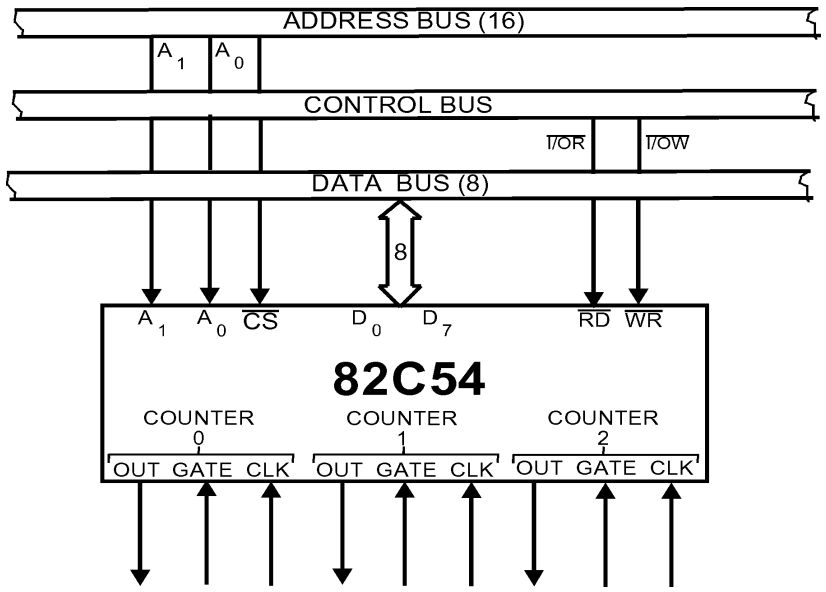


Figure B-5: 82C54 - System Interface

B.5 Operational Description

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

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B.5 Operational Description (continued)

B.5.1 Programming the 82C54

Counters are programmed by writing a Control Word and then an initial count. The control word format is shown in Table B-1, below.

Table B-1: Control Word Format

Control Word Format

A_1, A_0 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	MO	BCD

SC - Select Counter:

SC1	SC2	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read Back Command (See Read Operations)

M - Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW - Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write Least Significant Byte Only
1	0	Read/Write Most Significant Byte Only
1	1	Read/Write; Least Significant Byte Byte First, Then Most Significant Byte

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

All Control Words are written to the Control Word Register, which is selected when A1, A0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1, A0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

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B.5 Operational Description (continued)

B.5.2 Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1) For each Counter, the Control Word must be written before the initial count is written.

2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte.)

Since the Control Word Register and the three Counters have separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: a program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

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B.5 Operational Description (continued)

B.5.2 Write Operations (continued)

Table B-2: A Few Possible Programming Sequences

		A_1	A_0			A_1	A_0
Control Word	Counter 0	1	1	Control Word	Counter 2	1	1
LSB of Count	Counter 0	0	0	Control Word	Counter 1	1	1
MSB of Count	Counter 0	0	0	Control Word	Counter 0	1	1
Control Word	Counter 1	1	1	LSB of Count	Counter 2	1	0
LSB of Count	Counter 1	0	1	MSB of Count	Counter 2	1	0
MSB of Count	Counter 1	0	1	LSB of Count	Counter 1	0	1
Control Word	Counter 2	1	1	MSB of Count	Counter 1	0	1
LSB of Count	Counter 2	1	0	LSB of Count	Counter 0	0	0
MSB of Count	Counter 2	1	0	MSB of Count	Counter 0	0	0

		A_1	A_0			A_1	A_0
Control Word	Counter 0	1	1	Control Word	Counter 1	1	1
Control Word	Counter 1	1	1	Control Word	Counter 0	1	1
Control Word	Counter 2	1	1	LSB of Count	Counter 1	0	1
LSB of Count	Counter 2	1	0	Control Word	Counter 2	1	1
LSB of Count	Counter 1	0	1	LSB of Count	Counter 0	0	0
LSB of Count	Counter 0	0	0	MSB of Count	Counter 1	0	1
MSB of Count	Counter 0	0	0	LSB of Count	Counter 2	1	0
MSB of Count	Counter 1	0	1	MSB of Count	Counter 0	0	0
MSB of Count	Counter 2	1	0	MSB of Count	Counter 2	1	0

Note: In all four examples, all counters are programmed to read/write two byte counts. These are only four of many possible programming sequences.

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B.5 Operational Description (continued)

B.5.3 Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the counters: a simple read operation, the Counter Latch Command, and the Read-Back Command. Each is explained below. The first method is to perform a simple read operation. To read the Counter, which is selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

B.5.3.1 Counter Latch Command

The second method uses the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A1, A0 = 11. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

Table B-3: 82C54 - Counter Latching Command Format

A_1, A_0 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - Specify Counter to be Latched

X - don't care

Note:
Don't care bits(X) should be set to logic state '0' to insure compatibility with future Intel products.

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

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B.5 Operational Description (continued)

B.5.3 Read Operations (continued)

B.5.3.1 Counter Latch Command (continued)

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until it is read; Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1) Read least significant byte.

2) Write new least significant byte.

3) Read most significant byte.

4) Write new most significant byte.

If a Counter is programmed to read/write two-byte counts, the following precaution applies; a program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

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B.5 Operational Description (continued)

B.5.3 Read Operations (continued)

B.5.3.2 Read-Back Command

The third method uses the Read-Back command. This command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Table B-4, below. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 = 1.

Table B-4: Read-Back Command Format

A_1, A_0 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D_5: 0 = Latch Count of Selected Counter(s)
D_4: 0 = Latch Status of Selected Counter(s)
D_3: 0 = Select Counter 2
D_2: 0 = Select Counter 1
D_1: 0 = Select Counter 0
D_0: Reserved for Future Expansion; Must be set to Logic State '0'

The read-back command may be used to latch multiple counter output latches (OL) by setting the N bit D5=0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i. e., the count which will be read is the count at the time the first read-back command was issued.

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B.5 Operational Description (continued)

B.5.3 Read Operations (continued)

B.5.3.2 Read-Back Command (continued)

The read-back command may also be used to latch status information of selected counter(s) by setting $\overline{\text{STATUS}}$ bit 04=0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Table B-5, at the top of the next page. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

Table B-5: Status Byte

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output	Null Count	RW1	RW0	M2	M1	M0	BCD

D_7: 1 = Out Pin is 1
0 = Out Pin is 0
D_6: 1 = Null Count
0 =Count Available for Reading
D_5 - D_0: Counter Programmed Mode (see Figure B-7)

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Table B-6, page 14.

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B.5 Operational Description (continued)

B.5.3 Read Operations (continued)

B.5.3.2 Read-Back Command (continued)

Table B-6: Null Count Operation		
A.	Write to Control Word Register[1]	Null Count =1
B.	Write to the Count Register (CR)[2]	Null Count =1
C.	New Count is Loaded Into CE (CR → CE)	Null Count =0
[1]	Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected	
[2]	If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to '1' when the second byte is written.	

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i. e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both $\overline{\text{COUNT}}$ and $\overline{\text{STATUS}}$ bits D5, D4=0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Table B-7, below.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

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B.5 Operational Description (continued)

B.5.3 Read Operations (continued)

B.5.3.2 Read-Back Command (continued)

Table B-7: 82C54 - Read-Back Command Example

Command									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Description	Result
1	1	0	0	0	0	1	0	Read Back Count and Status of Counter 0	Count and Status Latched for Counter 0
1	1	1	0	0	1	0	0	Read Back Status of Counter 1	Status Latched for Counter 1
1	1	1	0	1	1	0	0	Read Back Status of Counters 2, 1	Status Latched for Counter 2, not for Counter 1
1	1	0	1	1	0	0	0	Read Back Count of Counter 2	Count Latched for Counter 2
1	1	0	0	0	1	0	0	Read Back Count and Status of Counter 1	Count Latched for Counter 1, but not Status
1	1	1	0	0	0	1	0	Read Back Status of Counter 1	Command Ignored, Status Already Latched for Counter 1

Table B-8: 82C54 -Read/Write Operations Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	Description
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read From Counter 0
0	0	1	0	1	Read From Counter 1
0	0	1	1	0	Read From Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

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B.5 Operational Description (continued)

B.5.4 Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE:	A rising edge, then a falling edge, in that order, of a Counter's CLK input.
TRIGGER:	A rising edge of a Counter's GATE input.
COUNTER LOADING:	The transfer of a count from the CR to the CE (refer to the "Functional Description")

B.5.4.1 Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N+1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

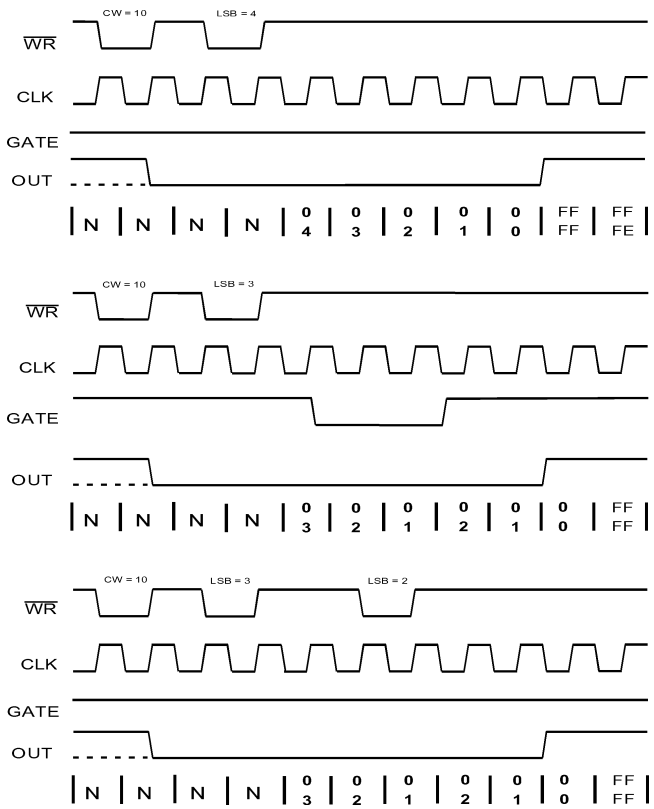
1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).

2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

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NOTE: The Following Conventions Apply To All Mode Timing Diagrams:

1) Counters are programmed for binary (not BCD) counting and for Reading/Writing least significant byte (LSB) only.

2) The counter is always selected ($\overline{CS}$ always low).

3) CW stands for "Control Word"; CW = 10 means a control word of 10, hex is written to the counter.

4) LSB stands for "Least Significant Byte" of count.

5) Numbers below diagrams are count values.

The lower number is the least significant byte.
The upper number is the most significant byte. Since the counter is programmed to Read/Write LSB only, the most significant byte cannot be read.
N stands for an undefined count.
Vertical lines show transitions between count values.

Figure B-6: 82C54 - Mode 0

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B.5 Operational Description (continued)

B.5.4 Mode Definitions (continued)

B.5.4.1 Mode 0: Interrupt on Terminal Count (continued)

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N+1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).

2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

B.5.4.2 Mode 1: Hardware Retriggerable One-shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

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B.5 Operational Description (continued)

B.5.4 Mode Definitions (continued)

B.5.4.2 Mode 1: Hardware Retriggerable One-shot (continued)

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

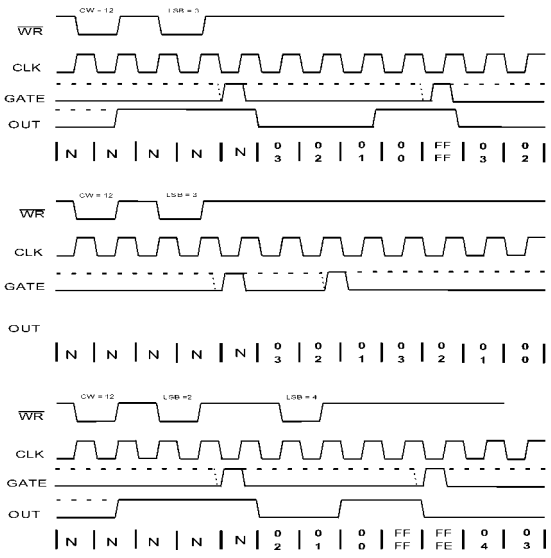
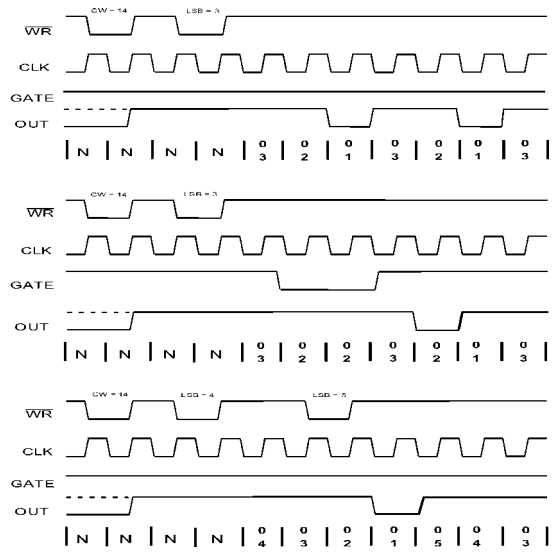


Figure B-7: 82C54 - Mode 1



NOTE: A GATE transition should not occur one clock prior to terminal count.

Figure B-8: 82C54 - Mode 2

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B.5 Operational Description (continued)

B.5.4 Mode Definitions (continued)

B.5.4.3 Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

B.5.4.4 Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

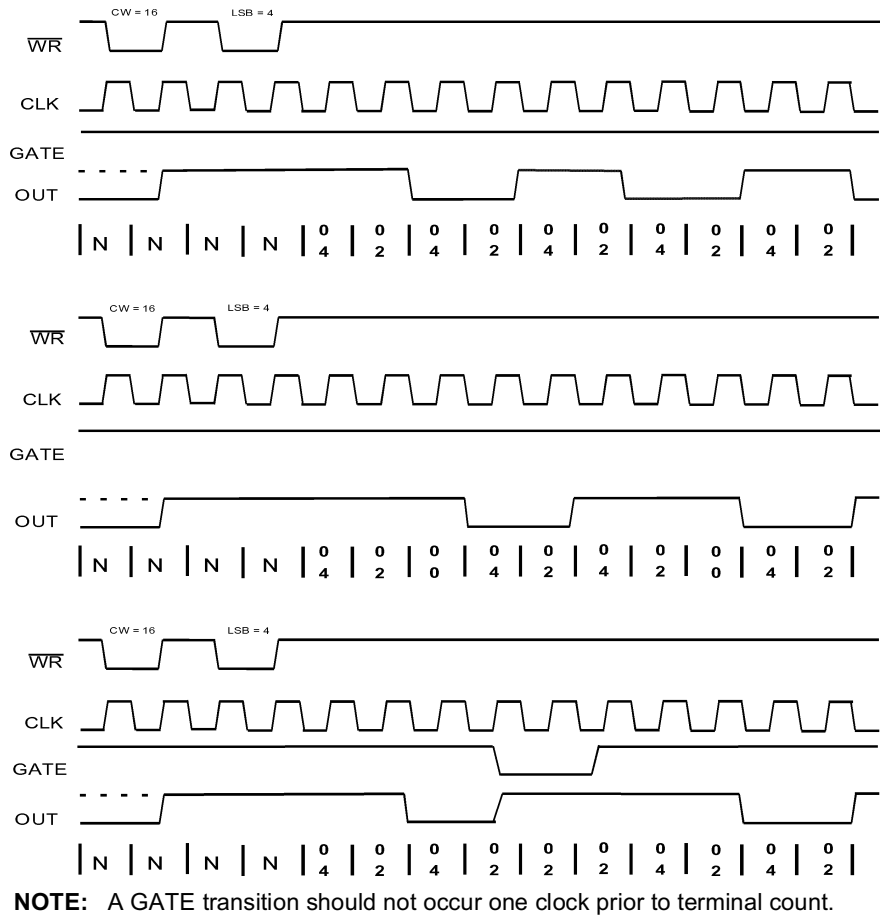
GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

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B.5 Operational Description (continued)

B.5.4 Mode Definitions (continued)

B.5.4.4 Mode 3: Square Wave Mode (continued)



NOTE: A GATE transition should not occur one clock prior to terminal count.

Figure B-9: 82C54 - Mode 3

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

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B.5 Operational Description (continued)

B.5.4 Mode Definitions (continued)

B.5.4.4 Mode 3: Square Wave Mode (continued)

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N+1)/2 counts and low for (N–1)/2 counts.

B.5.4.5 Mode 4: Software Triggered Strobe

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.

2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

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B.5 Operational Description (continued)

B.5.4 Mode Definitions (continued)

B.5.4.5 Mode 4: Software Triggered Strobe (continued)

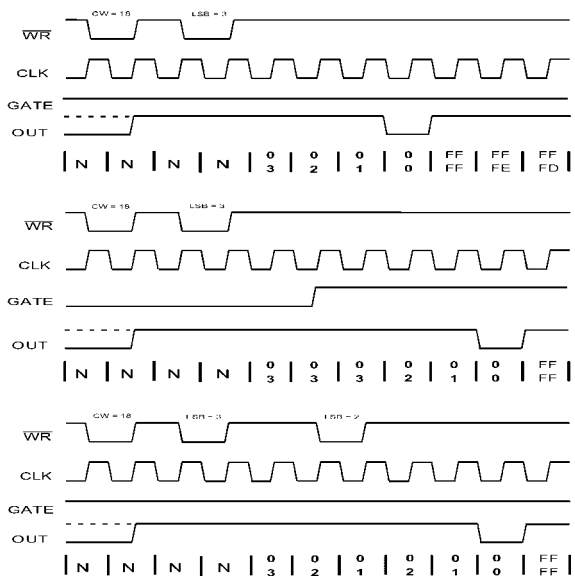


Figure B-10: 82C54 - Mode 4

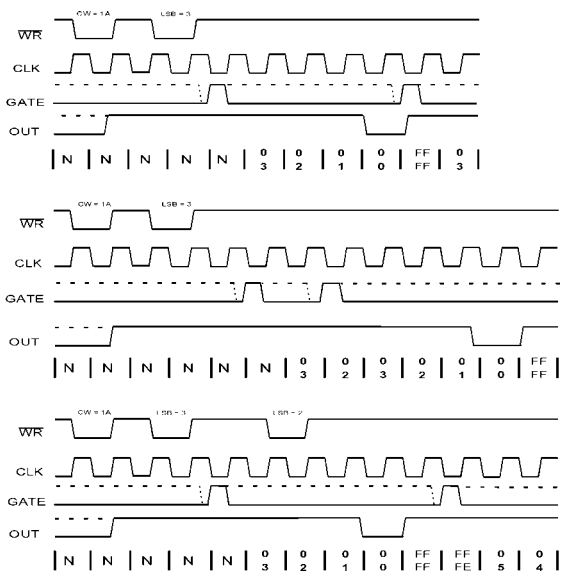


Figure B-11: 82C54 - Mode 5

This allows the sequence to be "retriggered" by software. OUT strobes low N+1 CLK pulses after the new count of N is written.

B.5.4.6 Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again. After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after a trigger. A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N+1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

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B.6 Operation Common to All Modes

B.6.1 Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

B.6.2 GATE

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK; the flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive. In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following $\overline{WR}$ of a new count value.

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B.6 Operation Common to All Modes (continued)

B.6.3 Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

Table B-9: Gate Pin Operations Summary

Signal Status Modes	Low or Going Low	Rising	High
0	Disables Counting	_____	Enables Counting
1	_____	1) Initiates Counting 2) Resets Output after next Clock	_____
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	_____	Enables Counting
5	_____	Initiates Counting	_____

Table B-10: Minimum and Maximum Initial Counts

Mode	Min Count	Max Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0

Note: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting

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Appendix C: Application Note

Manipulating RAM Buffer Addresses in the Model 4261 A/D Converter

C.1 Overview

This note describes a technique for explicitly setting the memory buffer starting address for input data collection from the A/D converter.

C.2 Background

The data memory of the Pentek Model 4261A provides a very flexible data storage facility satisfying many different applications. It is divided into two completely identical and symmetrical 'banks', each with its own address counter.

The data memory is arranged in a 'ping-pong' or 'swinging buffer' configuration: one bank is associated with the A/D converter for receiving input data and the other bank is associated with the VMEbus or parallel port for output data. The banks can be 'swapped' under various conditions so that the data collected from the A/D can be made available for output. The bank previously used for output has typically been emptied and is ready for new data.

C.3 Bank Address Counters

The address counter for each bank is a 24-bit binary device which is incremented automatically during input operation for writing sequential data from the A/D converter.

When a bank is set for output mode, it is available for random access read/write commands from the VMEbus. In this mode, when a read or write is performed, the VMEbus address is 'preset' or loaded into the address counter.

C.4 Bank Block Counters

Completely separate from the bank address counters are two other counters called the Block Counters. These are implemented with two sections of a programmable counter timer circuit (CTC) type 82C54.

These block counters are 16-bit binary devices which can be used to terminate data collection after a certain number of input samples have been collected or output samples delivered. The input clocks to these counters, called 'word clocks' are 'taps' from the bottom bits of the bank address counters. The taps available correspond to one clock every 4 samples to one clock every 512 samples, and all binary steps in between. When the input counter reaches 'top count', the Run bit is turned off stopping input samples from being written into the input bank.

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C.5 Bank Swapping

Bank swapping can be controlled in one of two ways:

1) Automatically when both block counters have reached 'top count', indicating that all input points have been collected and all output points have been delivered
2) Explicitly under VMEbus software control by setting the Bank Select bit in the Command Register. In this way, the VMEbus can gain access to either bank.

We can exploit the second case to achieve writing input data records of a programmed length to specific addresses within the input bank.

C.6 Example

For example, suppose we have the 32 MSample memory version of the 4261 and wish to collect 8 discrete time records each 3 MSamples in length, with each time record beginning at 4 MSample address boundaries. Each input bank contains 16 MSamples which we will divide into four 4 MSample regions.

1) The first step is to reset the board to initialize functions. This sets up bank A for input and bank B for output, both of which are now empty.
2) Then disable automatic bank swapping and set the block counter for 3 MSamples record length.
3) The START bit is set ON, and then the RUN bit is set ON and the input record is written into bank A. After 3 MSamples are collected, the top count bit from block counter A goes true, turning off the RUN bit and stopping data collection. The bank A address counters are now stopped at the 3 MSample address.
4) At this point, the START bit must be set OFF and the Bank Select bit set for bank A output mode.
5) A read is performed at VMEbus address corresponding to the 4 MSample boundary to force the bank A address counters to the 4 MSample address.
6) Now the Bank Select bit is set for bank A input mode, the bank A block counter is re-loaded for 3 MSamples, and the START is set ON and then the RUN bit is set ON, starting data collection for the second record.
7) Steps (3) through (6) are repeated until all four 3 MSample records are collected in bank A.
8) Now bank B can be filled in exactly the same way, repeating steps (3) through (7).
9) The 8 time records can be read out over the VMEbus, one bank at a time, until all data is delivered. Data will remain intact indefinitely and can be read in any order.

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