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OPERATING MANUAL

PENTEK MODEL 4265

16-Channel, 16-bit, 48 kHz, Σ–Δ
A/D and D/A Converter VMEbus Board

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Pentek Model 4265 Operating Manual - Revision History

Date	Rev	Applicable Serial #'s	Comments
12/31/93	A	9401004 - Forward	Initial product release - Preliminary Manual
03/10/94	A.1	9401004 - Forward	A24/A32 jumper descriptions corrected, Frequency Synthesizer range limitation note added.
06/27/95	B	9441054 - Forward	Completely revised and expanded. Synthesizer now optional (Opt. 002). More details about operating characteristics of the CS4215s in body of manual. Enhanced discussion of Comm Port usage. New Sample Code in Appendix A.
08/06/99	B.1	9441054 - Forward	Corrected Figure 1-1; now refers to Banks as A, B, C & D and Channels as 1, 2, 3 & 4, now agrees with nomenclature used throughout the rest of the manual. Section 2.3.1 now refers to the 16-pin Comm Port connectors as Pentek Part Number 2104.

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The material presented in Appendix B of this manual is excerpted from Crystal Semiconductor Corporation's data sheet for the CS4215 16-Bit Multimedia Audio Codec, Crystal publication number DS76F2. A complete copy of this data sheet may be ordered from Crystal Semiconductor Corp., P. O. Box 17847, Austin, TX 78760 (Phone: (512) 445-7222; FAX: (512) 445-7581. Pentek gratefully extends its thanks to Crystal for their permission to use this copyrighted material.

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Chapter 1: General Description

1.1 Introduction

The Model 4265 is a complete 16-channel A/D and D/A converter for digital audio applications. As a standard 6U VMEbus card, its control and configuration registers are memory mapped into VMEbus slave address space. Sampled input and output data streams are tailored to directly interface with the communications ports of the Texas Instruments TMS320C40 DSP. Front panel communication port (Comm Port) connectors match those found on Pentek's family of 'C40 based DSP products, providing flexible interconnections and the ability to change data paths quickly and easily.

1.1.1 Four 4-Channel A/D - D/A Banks

The Model 4265 contains four identical banks of circuitry each providing four channels of 16-bit A/D conversion, four channels of 16-bit D/A conversion, two 'C40-compatible Comm Port interfaces, and a control section driven from the VMEbus. Each bank can operate in A/D mode, D/A mode, or a combination of both and utilize either one or two 'C40-compatible Comm Ports. Each bank also features an independent programmable sample rate generator which determines the sampling rate for all A/D and D/A channels within that bank.

1.1.2 Input Section

The 4-channel input (A/D) section of each bank is implemented with the Crystal Semiconductor CS4215, a highly-integrated sigma-delta (Σ–Δ) converter. Each input features a programmable gain amplifier with a 0 to 22.5 dB range with 1.5 dB resolution. The 16-bit Σ–Δ A/D's provide inherent anti-aliasing digital filters with sharp cutoff characteristics and linear phase response. The 16-bit linear A/D output can be used directly or converted to 8-bit A-law or μ-law coding for digital voice applications.

1.1.3 Output Section

Like the input section, the 4-channel output (D/A) section of each bank also employs the Σ–Δ technology devices. Either 16-bit linear, or 8-bit A-law or μ-law samples are handled by the decoder section and then passed on to integral digital reconstruction filters, eliminating the need for external output filters. An output attenuator provides a 0 to 94.5 dB range with 1.5 dB resolution.

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1.1 Introduction (continued)

1.1.4 Sampling Rate Section

Each of the four 4-channel banks can operate at independent sample rates. The sampling rate for each bank is determined by a local programmable divider, within each bank, operating from any one of four master frequency sources: two socketed DIP crystal oscillators, a programmable frequency synthesizer, and an external TTL clock input.

The ratio between the selected frequency source and the sample rate is programmable in 8 steps from 384 to 3072. When the internal frequency synthesizer is used as the source, any sampling rate between 4 kHz and 48 kHz can be set with a resolution of 200 Hz or better. See the specifications section for a complete listing of frequencies available.

1.1.5 Comm Port Data Interface

One TMS320C40-compatible Comm Port within each 4-channel bank is used for outputting sampled data from the A/D converters. Any one, two, three or four of the A/D converters can be connected to this output Comm Port. This channel assignment is software programmable, providing very flexible arrangements. Samples are interleaved by channel in sequential order.

Data is delivered in byte-serial fashion, and can be formatted as either two bytes per sample for 16-bit linear operation, or one byte per sample for the 8-bit A-law or μ-law coding function.

The second Comm Port is used for input data for control functions and for sampled data to the D/A converters. Like the output Comm Port, any one, two, three or four of the D/A converters can be connected to the input Comm Port under software configuration. All 8-bit and 16-bit coding formats are available.

1.1.6 VMEbus Control Interface

All control and configuration data for the Model 4265 is programmed over the VMEbus via simple memory mapped registers. These functions include setting up the Comm Port-to-channel assignment, the input gain and output attenuation, the linear/companding coding functions, and the number of active channels. Provisions for setting the sampling rate and internal/external sampling modes is also included.

The Model 4265 is a VMEbus slave device that can decode A24 and A32 addresses, and can participate in D16 data transfers. Note that the use of the VMEbus interface is required to initialize the unit even though subsequent control information may be sent over the input Comm Port.

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1.1 Introduction (continued)

1.1.7 Comm Port Control Interface

The input Comm Ports for any of the four channel banks can be used to control gain and attenuation within that bank. Other control functions such as sampling rates, channel assignments, etc., must be programmed over the VMEbus.

1.1.8 Software Support

C language software driver code is included in the last section of this manual for Pentek's 'C40-compatible products and for generic VMEbus devices.

VMEbus drivers include routines for initializing the control sections of the board including the number of active channels, sampling rates, gain, and attenuation. These will allow any VMEbus Master to control the overall operation of the board.

The 'C40-compatible Comm Port drivers include routines for moving data between 'C40-compatible memory resources and the A/D and D/A converters and for setting attenuation and gain.

1.1.9 Block Diagram

A block diagram of the Pentek Model 4265, 16-Channel, 16-bit, 48 kHz, Σ–Δ, A/D - D/A Converter VMEbus board is presented in Figure 1-1 on page 12.

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1.1 Introduction (continued)

1.1.9 Block Diagram (continued)

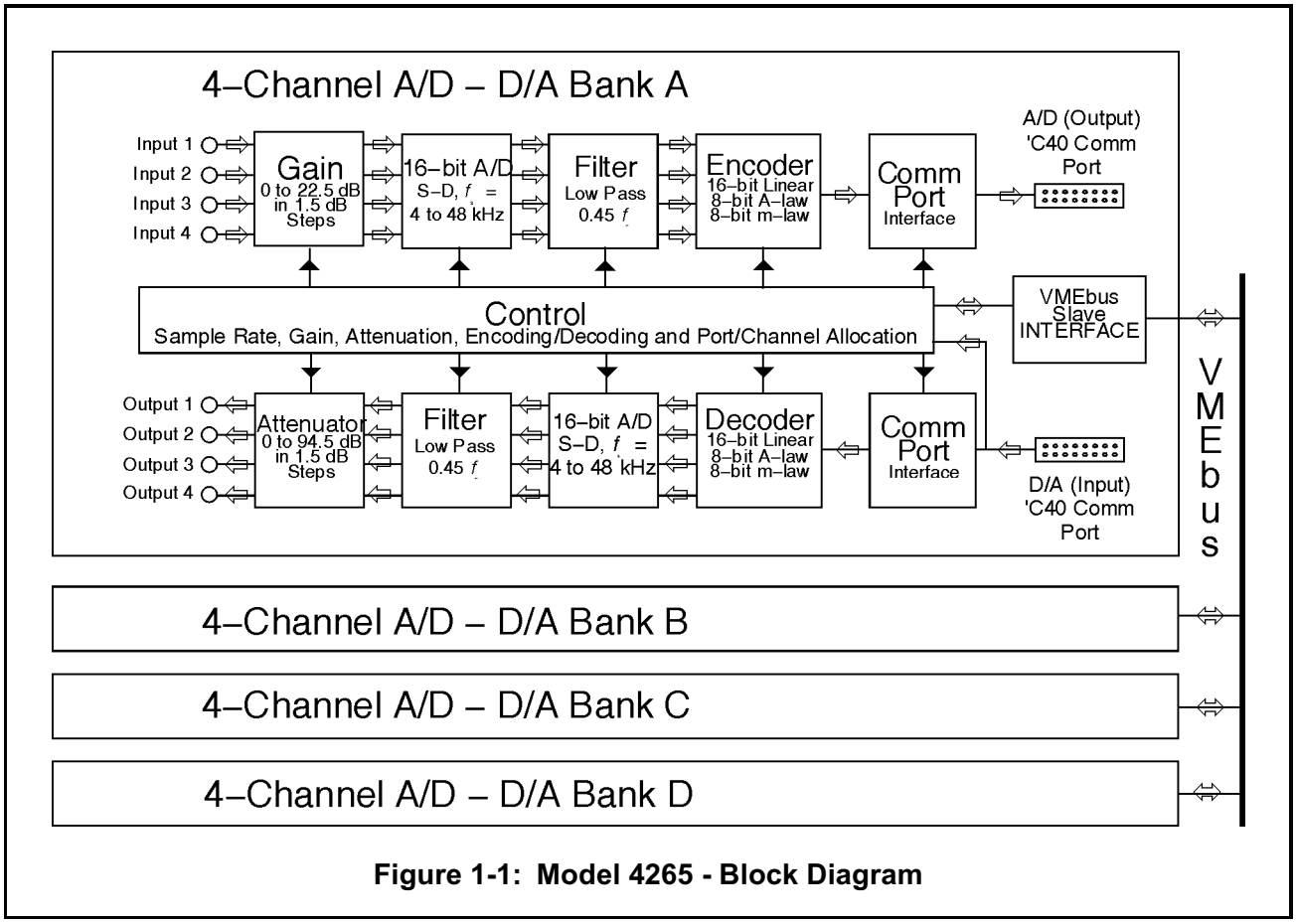


Figure 1-1: Model 4265 - Block Diagram

1.2 Specifications

Input Channels and A/D Converters:

Input Type:	Single-ended
Input Impedance:	100 kΩ
Full Scale Input:	2.0 V_{RMS} ±0.5 dB
Input Gain Range:	0 to 22.5 dB
Input Gain Steps:	1.5 dB
A/D Resolution:	16 bits
Sampling Rate (f_S):	4 kHz to 48 kHz
Frequency Response:	±0.5 dB

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1.2 Specifications (continued)

Input Channels and A/D Converters (continued):

Input Digital Channels

Passband:	0 to 0.45 f_S
Passband Ripple:	±0.1 dB
Transition Band:	0.45 f_S to 0.55 f_S
Stop Band:	≥0.55 f_S
Stop Band Rejection:	74 dB min
Group delay Variation:	0 µs
Encoder:	16-bit linear, 8-bit A-law or µ-law

Output Channels and D/A Converters:

Output Type:	Single-ended
Output Impedance:	600 Ω
Full Scale Output:	2.0 V_{RMS} ±0.5 dB
Output Atten Range:	0 to 94.5 dB
Output Atten Steps:	1.5 dB
D/A Resolution:	16 bits
Sampling Rate ():	4 kHz to 48 kHz
Frequency Response:	±0.5 dB

Output Digital Interpolation Filter (for Analog Output from D/A):

Passband:	0 to 0.45 f_S
Passband Ripple:	±0.1 dB
Transition Band:	0.45 f_S to 0.55 f_S
Stop Band:	≥0.55 f_S
Stop Band Rejection:	74 dB min
Group Delay Variation:	0 µs
Decoder:	16-bit linear, 8-bit A-law or µ-law

VMEbus Interface:

Type:	A24/A32, D16 Slave Interface
Base Address:	Set with Jumpers

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1.2 Specifications (continued)

Sample Rate Synthesizer (Option 002 only):

Output Frequency: DC to 25 MHz with 0.0058 Hz resolution
Effective Sample Rates:

- ÷ 384 Mode - DC to 65.10 kHz* with 15.16×10^{-6} Hz resolution
- ÷ 448 Mode - DC to 55.80 kHz* with 12.99×10^{-6} Hz resolution
- ÷ 512 Mode - DC to 48.83 kHz* with 11.37×10^{-6} Hz resolution
- ÷ 768 Mode - DC to 32.55 kHz with 7.58×10^{-6} Hz resolution
- ÷ 896 Mode - DC to 27.90 kHz with 6.50×10^{-6} Hz resolution
- ÷ 1536 Mode - DC to 16.28 kHz with 3.79×10^{-6} Hz resolution
- ÷ 2560 Mode - DC to 9.77 kHz with 2.27×10^{-6} Hz resolution
- ÷ 3072 Mode - DC to 8.14 kHz with 1.89×10^{-6} Hz resolution

* NOTE: These sample rates are above the CS4215's specified maximum sampling rate - operation above 48 kHz is NOT guaranteed.

Sampling Rate Selection (each bank)

Sampling Rate Generator:
Internal Rates (kHz):

5.5125	22.05
6.615	27.42857
8.0	32.0
9.6	33.075
11.025	37.8
16.0	44.1
18.9	48.0

All frequencies are shown in kHz. Frequencies are software selectable and crystal controlled to an accuracy of ± 0.01%

External Sample Rates:
Ext. TTL sample clock divided by:
384, 448, 512, 768, 896, 1536, 2560 or 3072

Synthesized (Internal) Rates (Option 002 only):
Synthesizer output divided by:
384, 448, 512, 768, 896, 1536, 2560 or 3072 (see synthesizer specs)

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1.2 Specifications (continued)

Front Panel Connectors:

A/D - D/A Input and Output:	Two 34-pin DIL headers, one for 4-channel banks A & B and the other for C & D. Each connector provides 8 single-ended analog inputs and 8 single-ended analog outputs.
'C40-compatible Comm Ports (8):	16-pin DIL ribbon cable, plug-to-plug compatible with all of Pentek's TMS320C40 based products.
External Sample Clock (in/out):	BNC, female, front panel, TTL levels
Dimensions: Width	Single 6U VMEbus board 20.3mm (0.8-in.)

Power:

+ 5.0 V_{DC}:	3.70 A typ.
+ 12.0 V_{DC}:	0.15 A typ.
– 12.0 V_{DC}:	0.20 A typ.

Ordering Information:

Model 4265:	16 channels A/D and D/A with 8 Comm Ports
Option 001:	8 channels A/D and D/A with 4 Comm Ports
Option 002:	Internal Frequency Synthesizer for Sample Clock

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Chapter 2: Installation

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If you discover any damage, please contact Pentek immediately, at (201) 818-5900. Please save the original shipping container and packing material, in case re-shipment is required.

2.2 Configuration Jumpers

Before installing the Model 4265, the unit must be configured for proper operation. This is accomplished by setting configuration jumpers which are described in the subsections that follow. The Model 4265 consists of two PC assemblies: the VME Board and the Mezzanine Board. All of these jumpers are located between the two VMEbus connectors, P1 and P2. The two boards do not need to be separated to set these jumpers.

For reference purposes, the component layout drawings for both the VME and Mezzanine boards are shown in Figures 2-2 and Figures 2-3. A magnified view of the jumper blocks is shown in Figure 2-1, below.

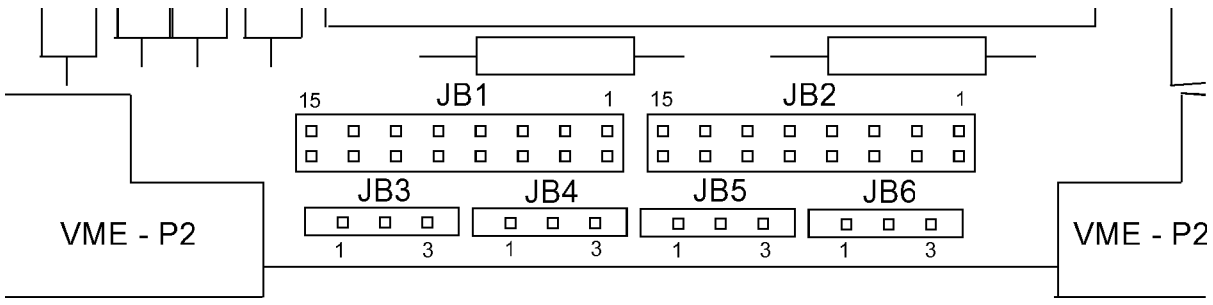


Figure 2-1: Model 4265 - Jumper Blocks Magnified View

The shorting jumpers used on these jumper blocks have 2 mm spacing between pins. Pentek's part number for these jumpers is 356.00010. Should you require additional jumpers, call us at (201) 818-5900, and request that part number.

The jumper settings for JB1 and JB2 are described in Section 2.2.1, and are used to set the VMEbus base address.

Jumper setting for JB3 through JB6 are described in Section 2.2.2 and are used to select the operating mode for the front panel EXT CLK reference clock connector.

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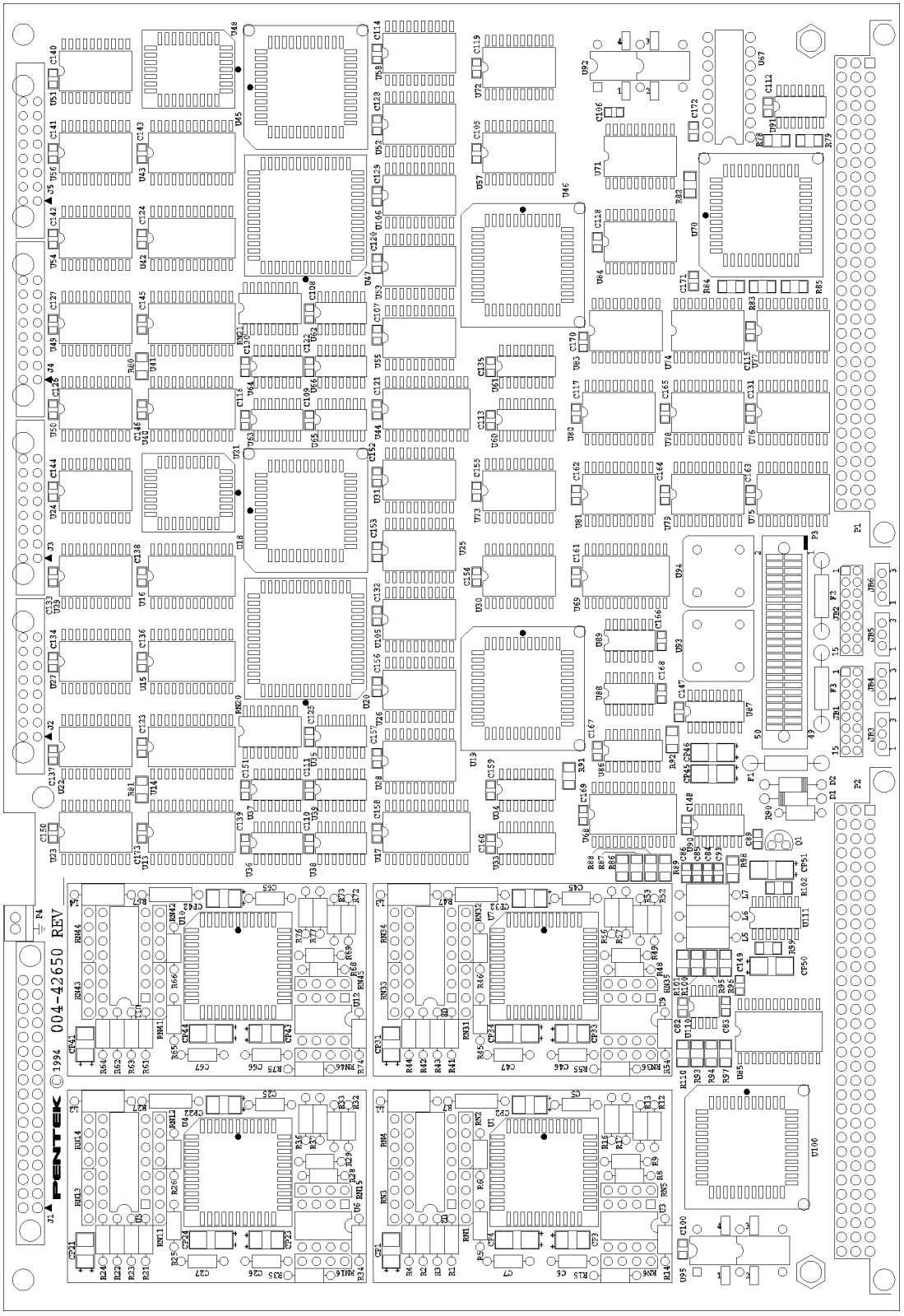


Figure 2-2: Model 4265 - VME Board Component Layout

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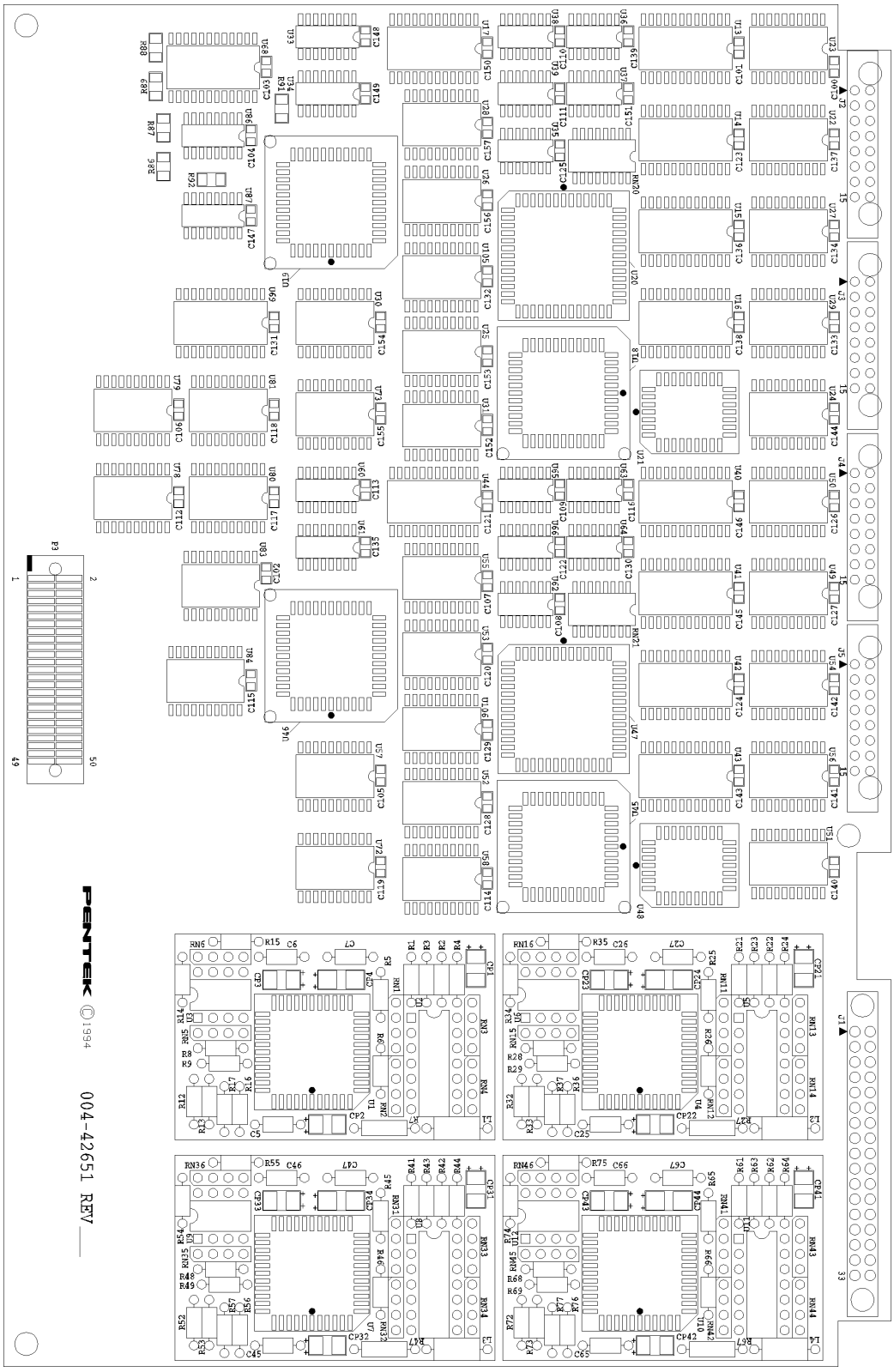


Figure 2-3: Model 4265 - Mezzanine Board Component Layout

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2.2 Configuration Jumpers (continued)

2.2.1 A32 and A24 VMEbus Base Address Jumper Blocks - JB1 and JB2

Resource locations on the Model 4265 within the A24 or A32 VMEbus address space are determined by setting jumper blocks JB1 and JB2. This address is referred to as the VMEbus Base address (VME_base) and it appears as an offset to all other addresses used for board resources. Jumper blocks JB1 and JB2 are located on the VME board between the two VMEbus connectors, P1 and P2.

For A32 addressing, jumper block JB1 sets the most significant 8 bits and jumper JB2 sets the 8 next most significant bits. A32 addresses are conventionally expressed 8 hexadecimal digits.

For A24 addressing, jumper block JB1 is not used, and jumper block JB2 sets the 8 most significant A24 bits. A24 addresses are conventionally expressed with 6 hexadecimal digits.

The entire address space for the Model 4265 is thus mapped within a single 64k byte block of VMEbus address space. There are 256 such blocks available in A24 space and 65,536 such blocks available in A32 space.

The jumpers are small black shorting plugs which are pushed onto two adjacent pins of the jumper block header. In Figure 2-4, below, and Figure 2-5, on the next page, the address weights shown to the right of each jumper position indicates the weight of that jumper. If the jumper is left open (not installed) the indicated weight is added to the base address value. If the jumper is installed, the weight does not add to the address value.

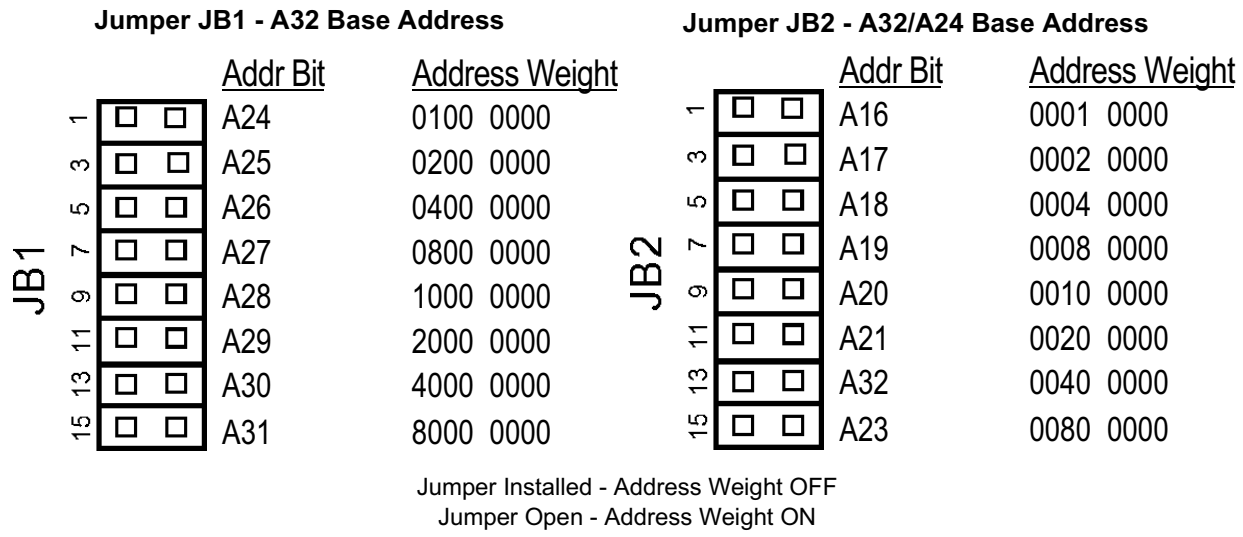


Figure 2-4: Model 4265 - A32 and A24 Base Address Jumper Weights

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2.2 Configuration Jumpers (continued)

2.2.1 A32 & A24 VMEbus Base Address Jumper Blocks - JB1 & JB2 (cont.)

As an example, suppose you wish to set an A32 VMEbus base address of 0x5A12 0000. The jumpers would be installed as shown In Figure 2-5, below. The installed jumpers are indicated as shaded blocks

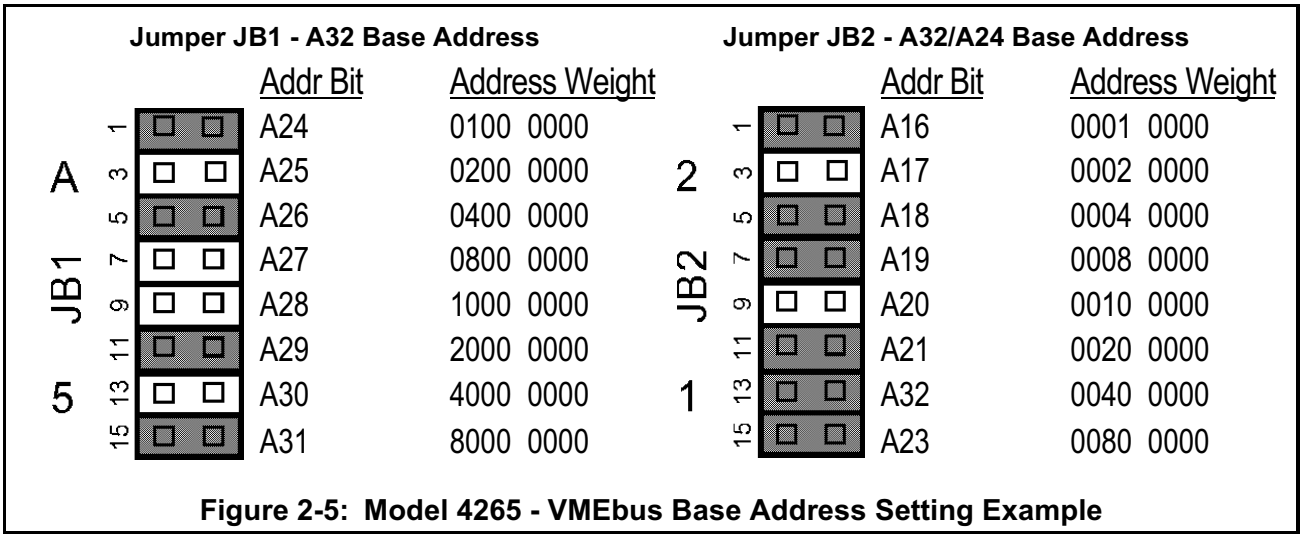


Figure 2-5: Model 4265 - VMEbus Base Address Setting Example

The same jumper setting would be valid for an A24 VMEbus base address of 0x12 0000.

2.2.2 External Reference Clock Input/Output Jumper Blocks - JB3 thru JB6

Each of the four 4-channel banks can be configured to use an external reference clock supplied to the front panel BNC connector. Alternately, the reference clock for any one of the 4-channel banks can be selected as an output to the front panel BNC connector. Configuring the mode of operation for the external reference clock (input or output) is determined by four jumper blocks, JB3, JB4, JB5 and JB6. The location of these jumper blocks is shown in Figure 2-1.

Each of these jumper blocks is a three pin, single-in line header, where a jumper may be installed between pins 1 & 2 or pins 2 & 3. The connectivity of these jumper blocks is shown in Figure 2-6, on page 22. Normally, all four jumpers are installed between pins 1 & 2, which allows an external clock signal, connected to the front panel EXT CLK BNC, to be accepted by any of the four reference clock MUX's using Control Register bits CS1 and CS0 (see Section 3.5.1).

If one reference clock from one of the MUX outputs needs to be delivered as an output to the front panel BNC, then the jumper for that bank **ONLY** is installed in the 2-3 position. This method may also be employed to use one channel's reference as a common clock for all channels. ***Note that only one of the reference clock jumpers may be installed in the 2-3 position.***

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2.2 Configuration Jumpers (continued)

2.2.2 External Reference Clock Input/Output Jumper Blocks (continued)

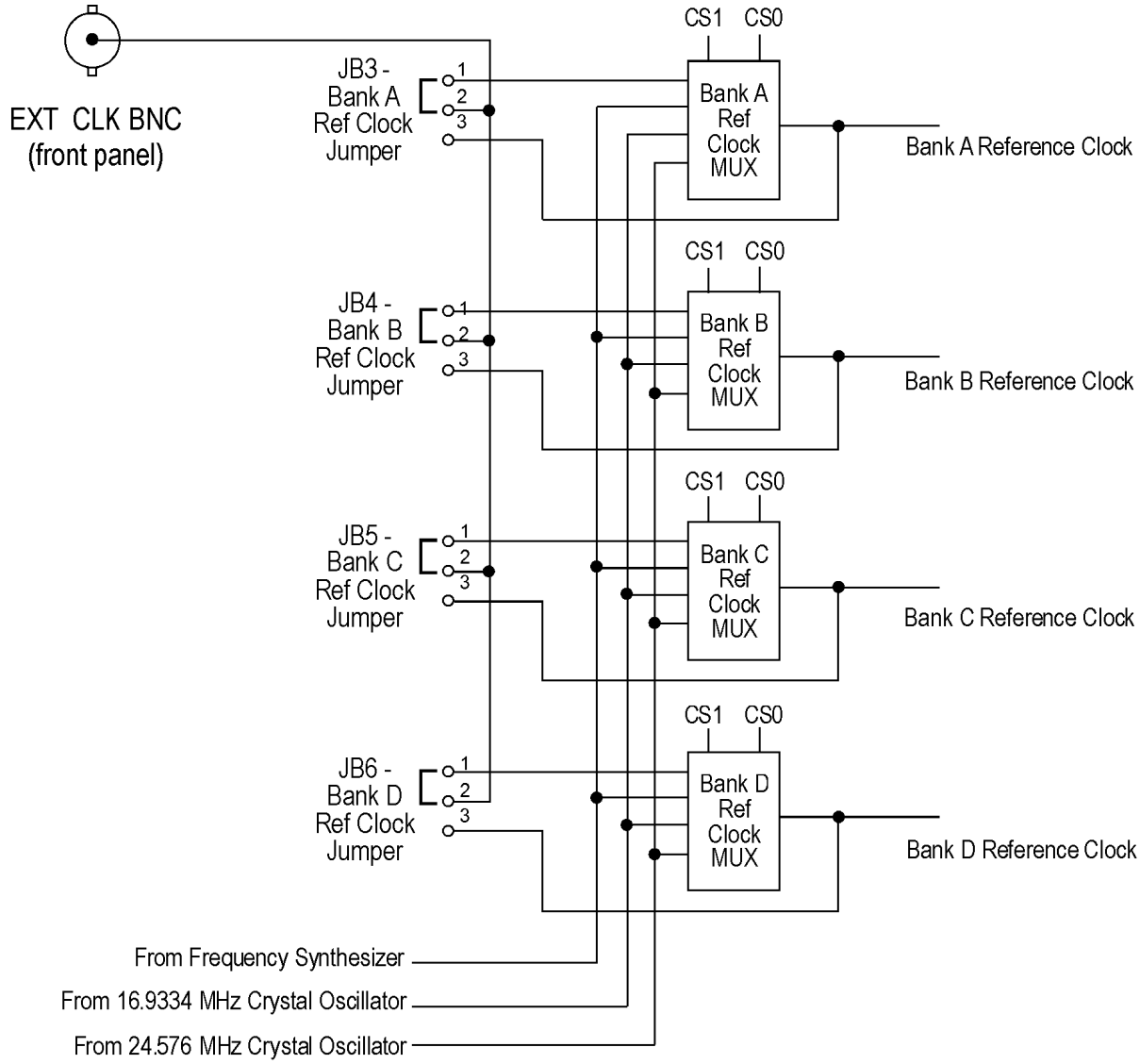


Figure 2-6: Model 4265 - External Reference Clock Input/Output Jumper Setting

2.3 Front Panel Connectors

A view of the front panel is shown in Figure 2-7, on the next page. Three different connector types are provided: Analog Input/Output connectors, Comm Port connectors, and a Reference Clock connector.

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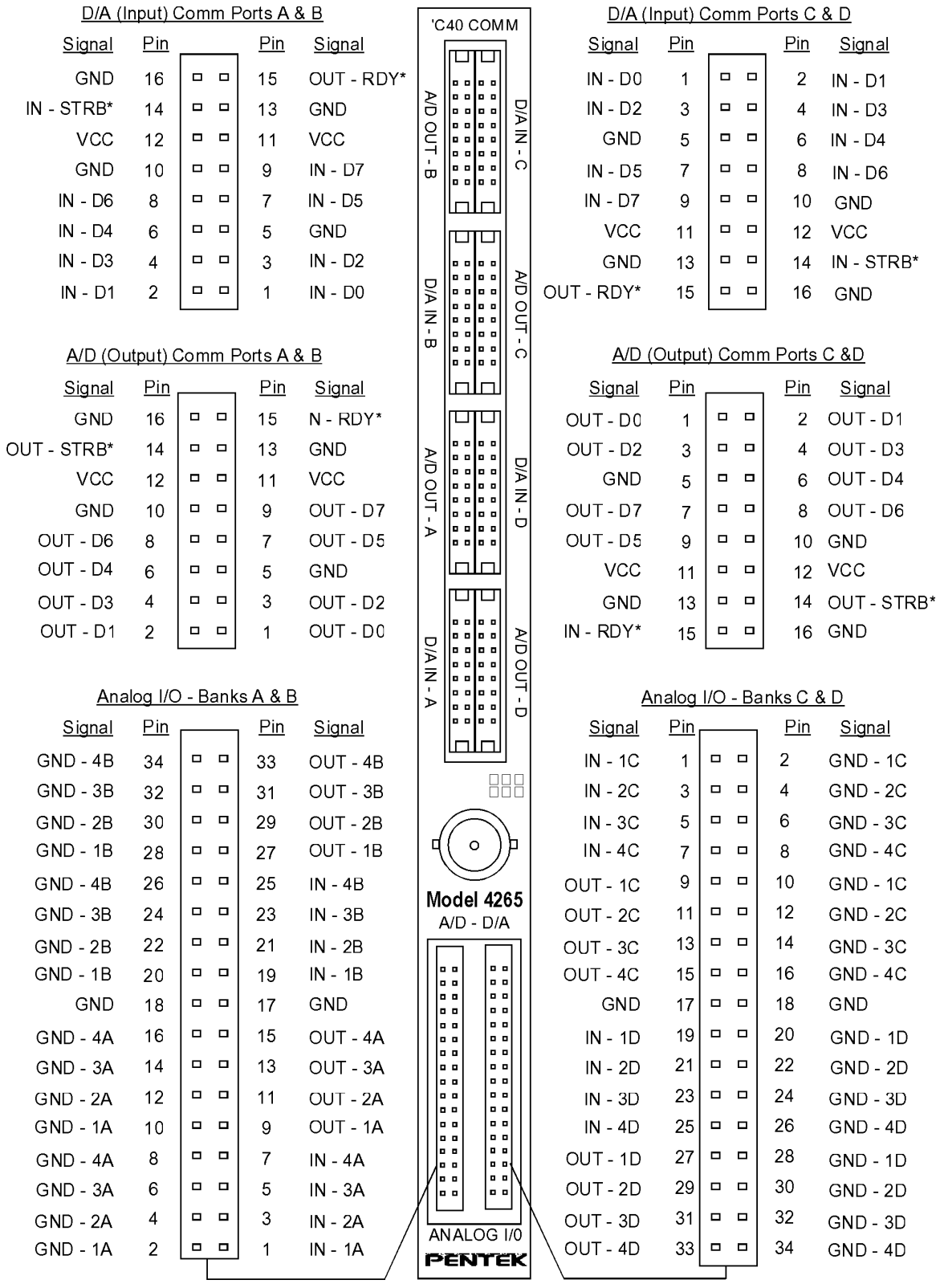


Figure 2-7: Model 4265 - Front Panel View, Showing Connector Pinouts

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2.3 Configuration Jumpers (continued)

2.3.1 'C40-compatible Comm Port Connectors

Eight 16-pin Comm Port connectors are provided at the top of the panel. These connectors mate directly with the standard 3M plugs used with all of Pentek's TMS320C40 based products. The plugs and connectors are keyed to prevent incorrect insertion. Note that the left and right rows of Comm Port connectors are rotated 180° with respect to each other, with pin 1 always on the inside row of pins, as shown in Figure 2-7 on page 23.

Unlike the Comm Ports of the TMS320C40, the Model 4265's Comm Ports are dedicated as inputs or outputs only. A Model 4265 input Comm Port cannot be programmed to operate as an output Comm Port, and vice versa. Each of the Comm Port lines is terminated with a series resistor to match cable impedance and to prevent excess current flow in the case of two outputs being connected together.

Comm Port cables can be easily assembled by using a 3M hand press with locator plate #3443-110 and standard 16-conductor, 0.050 pitch flat ribbon cable such as 3M #3365/16. Every Model 4265 is shipped with eight mating connectors (3M #50116-B000) and the optional strain relief (3M #3448-50116). The use of these standard components allows the user to easily configure the Comm Port cables to minimize excess cable length for any given interconnect pattern. A pre-assembled Comm Port cable is available from Pentek as Model 2104. This cable is compatible with all Comm Port equipped devices except the Models 4285, 7110 and 6223. To interface with those devices, use the Model 2115 cable, also available from Pentek.

A complete description of the operation of the 'C40 Comm Ports is contained in Chapter 8 the Texas Instruments' **TMS320C4x User's Guide**.

2.3.2 Analog Input/Output Signal Connectors

Two 34-pin, dual-inline connectors provide access to the 16 analog input signals and the 16 analog output signals. These are single-ended signals and each signal line is accompanied by an adjacent ground pin. The mating connector is a standard 34-pin dual-inline socket connector which accepts two rows of 0.025" square pins arranged on 0.100" centers between pins and between rows.

This style is compatible with all standard ribbon cable sockets as well as crimp style loaded contact connectors available from various distributors (such as the 3M #3414-7006, which would use strain relief #3448-2034). The pin headers on the Model 4265 are open headers which are not shrouded. If you prefer to use discrete pairs of wires, each pair with its own connector, 2-pin connectors from 3M (#CHG-1002-001010) or Berg (#650389-035), may be utilized.

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2.3 Configuration Jumpers (continued)

2.3.2 Analog Input/Output Signal Connectors (continued)

2.3.2.1 Analog Input Circuitry

Each analog input signal is connected to a resistive divider circuit, as shown in Figure 2-8, below. The impedance of each input, with respect to ground, is 100 kΩ. The full scale input voltage is 2.00 V_{RMS}, or 5.6 V_{P-P}. The input signal is centered around 0 V_{DC}.

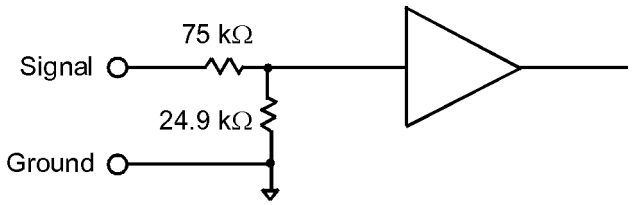


Figure 2-8: Model 4265 - Analog Input Signal Schematic

2.3.2.2 Analog Output Circuitry

Each analog output signal is driven from an output amplifier through a 600Ω series resistor. The full scale open circuit output voltage is 2.00 V_{RMS} or 5.6 V_{P-P}. The output signal is centered around 0 V_{DC}.

2.3.3 External Clock Connector

The Model 4265's front panel BNC connector, labeled EXT CLK, can function either as an input or an output signal connector, depending upon jumper settings (see Section 2.2.2). The subsections below describe the signals that should be applied if the connector is used as an input, and that which will be available if it is used as an output.

2.3.3.1 External Clock Input Signal

The Model 4265 can accept an external reference clock which can be used to derive the sample clock for any or all of the four 4-channel banks. This is provided through the front panel BNC connector.

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2.3 Front Panel Connectors (continued)

2.3.3 **External Clock Connector** (continued)

2.3.3.1 External Clock Input Signal (continued)

When configured as an input, the External Sample Clock requires that TTL logic signal '0' = 0.0 to 0.8 V and logic '1' = 2.0 to 5.0 V. The input will also accommodate 5V CMOS logic signals.

See Section 3.5.1 and Section 3.7.3 for more details concerning the EXT CLK signal.

2.3.3.2 External Reference Clock Output

The EXT CLK front panel BNC connector can also be used as a reference clock output from the Model 4265 for use as a reference clock input to one or more additional Model 4265s, which can then be slaved to a single reference. As an output, the signal is TTL compatible, capable of driving the clock inputs of nine additional Model 4265s.

See Section 3.5.1 and Section 3.7.3 for more details concerning the EXT CLK signal.

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Chapter 3: VMEbus Interface and Operations

3.1 Introduction

There are two methods of interfacing data and control to the Model 4265:

the VMEbus interface	- used for initializing the board
the 'C40 Compatible Comm Ports	- used for sending A/D data, D/A data attenuation and gain settings

This chapter deals with the VMEbus interface. Chapter 4 deals with the Comm Port interface.

This chapter describes the view of the Model 4265 from the VMEbus, which has access to two types of resources: the Dual-Ported RAM's and the Control Registers.

3.2 VMEbus Data and Addressing

The VMEbus is a byte-addressed bus. Each address increment corresponds to specific 8-bit byte location. The VMEbus address bits are designated A0 (for the least significant address bit) thru A31 (for the most significant address bit). VMEbus address bits A1 through A31 are implemented as 31 separate bus lines. These lines are used to explicitly address 2^{31} 16-bit words.

VME address bit A0 does not actually correspond to an address line on the bus, but is used in the control of two data strobe lines: $\overline{DS0}$ and $\overline{DS1}$. $\overline{DS0}$ becomes active for the lower byte of the 16-bit word, and $\overline{DS1}$ for the upper byte. For single byte transfers, only one of the DS strobes is active. For 16-bit transfers, both data strobes become active at the same time. For 32-bit transfers, in addition to both strobes active, the LWORD (long-word) bus line is also asserted.

Each of the Model 4265's resources are 8-bit (byte) locations, mapped on long-word address boundaries (characterized by A0 = 0 and A1 = 0). The Model 4265 will respond to word (16 bit) and long-word (32-bit) transfers. However, for both word and long-word transfers, only the least significant byte is used. D8 transfers are not supported in the Model 4265.

Many DSP boards (like Pentek's 4283 and 4284) are inherently 32-bit data devices, thus using 32-bit transfers is much easier. Many 680x0 based CPU boards (like Pentek's 4283, 4284, 4285 and 4290) are inherently byte-oriented devices, so users must make sure that such devices are properly programmed for word or longword transfers.

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3.3 Address Modifier (AM) Codes

There are three addressing modes defined for VMEbus transfers: 32-bit, 24-bit, and 16-bit modes. The modes are provided to support a variety of bus devices ranging from simple I/O functions with only a few memory locations to large RAM arrays with hundreds of megabytes of storage. The addressing mode is determined by a special 6-bit code which is placed on 6 dedicated VMEbus lines by the current VMEbus Master and is known as the Address Modifier Code, or AM Code.

The Model 4265 responds ONLY to the following eight AM codes for A24 and A32 accesses:

A24 AM Codes: 3E, 3D, 3A, and 39
A32 AM Codes: 0E, 0D, 0A, and 09

3.4 VMEbus Memory Map

There are four Dual Port RAM's and four Control Registers, one for each of the 4-channel banks. There is also a frequency synthesizer (for sample clock generation), controllable over the VMEbus. Each of these resources is addressed over the VMEbus as an offset from the VME_base address, as shown in Table 3-1, below. The VME_base address is determined by the settings of jumper blocks JB1 and JB2, as described in Section 2.2.1.

Table 3-1: Model 4265 - VMEbus Slave Memory Map

Resource	Dual Port RAM Base	Control Register
Bank A	VME Base + 0x0000	VME Base + 0x0800
Bank B	VME Base + 0x0400	VME Base + 0x0C00
Bank C	VME Base + 0x1000	VME Base + 0x1800
Bank D	VME Base + 0x1400	VME Base + 0x1C00
Load Synth (W. O.)	-	VME Base + 0x2020
Synth Freq Reg (W. O.)	-	VME Base + 0x2040
Synth Control Reg	-	VME Base + 0x2044

3.5 Control Register Description

The Control Register is used to the initialize the CS4215's, set the sampling clock source, and set the operating modes for the Comm Port and VMEbus interface. There are four control Registers, one for each bank. The Control Registers are located at the VMEbus addresses indicated in Table 3-1, above. The Control Register's bits are identified in Table 3-2 on page 29 and their functions are described in the subsections that follow the table. Note that upon VME reset, all Control Registers are initialized to 0x00.

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3.5 Control Register Description (continued)

Table 3-2: Model 4265 - Control Registers - Read/Write								
Bit No.	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Ref_Clk_ Src_1	Ref_Clk_ Src_0	DPR Offset	Bank Reset	DPR Master	CS4215 D/C Mode	CS4215 SClk	CS4215 FSync
Bit Function	Reference Clock Source Select - see Section 3.5.1		0 = Run 1 = Setup	0 = Reset 1 = Run	0 = VME 1 = Comm	0 = Cmd 1 = Data	See Section 3.5.6	
Note: All bits cleared to logic '0' by VME Reset.								

3.5.1 Reference Clock Source Select - Bits D7 and D6

The reference clock is a signal whose frequency is divided to determine the sample rate of the A/D and D/A converters in the Model 4265. The reference clock signal may be taken from one of three sources in a standard Model 4265. The available reference sources are the two crystal oscillators included for each channel bank (16.9334 MHz and 24.576 MHz) and the front panel EXT CLK connector. A fourth reference source is added in units equipped with Option 002, a frequency synthesizer.

The reference clock source is selected by the settings of these two bits, according to Table 3-3, below. Note that if the external clock is selected, it must be connected to the multiplexer's input by the reference clock jumper blocks (this is the factory default state of these jumpers). See Section 2.2.2 for more information about the reference clock jumpers.

Table 3-3: Model 4265 -Reference Clock Source Bits - Control Register bits D7 and D6			
Bit No.	**D7**	**D6**	**Reference Clock Source**
Bit Name	**CS1**	**CS0**	
Bit Definitions	0	0	24.576 MHz Internal Oscillator
	0	1	16.9344 MHz Internal Oscillator
	1	0	Frequency Synthesizer Clock*
	1	0	External Reference Clock Input
* Frequency Synthesizer Clock Selection Only Valid for Option 002			

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3.5 Control Register Description (continued)

3.5.2 Dual Port RAM Offset - Bit D5

This bit must be set to the logic '1' state during VME initialization and setup of the Model 4265. This bit is connected to the highest-order address line on the CS4215's side of the Dual-Port RAM. Setting the bit points the CS4215 away from the areas of the Dual-Port RAM that the VMEbus needs to access to initialize the board.

After VME initialization is complete, for normal A/D and D/A converter operation, this bit must be cleared to the logic '0' state.

3.5.3 Bank Reset - Bit D4

The Bank Reset bit provides a general software-controlled reset function for the CS4215's. This bit is connected to the RESET pin of both of the CS4215's in the bank, and both devices will be held in the reset state for as long as this bit remains in the '0' state. Setting the Reset bit to the '1' state releases the CS4215's for signal acquisition and generation. The reset operation of the CS4215 is described fully in Appendix B.

3.5.4 Dual-Port RAM Master Select - Bit D3

When this bit is cleared to the logic '0' state, the Dual-Port RAM for the bank in question is under the control of the current VMEbus Master. When this bit is set to the logic '1' state, the bank's DPR is controlled by the 'C40-compatible Comm Port. Thus, this bit must also be cleared during initialization, and set to collect data.

3.5.5 CS4215 Data/Control Mode Select - Bit D2

The D/C bit is a control bit for the CS4215 that is used to select between the Data and Control mode operation. These operating modes are described in Section 3.6 and in Appendix B. When this bit is cleared to the logic '0' state, the Control Mode is selected, allowing initialization and settings changes. When it is set to the logic '1' state, the Data Mode is selected, enabling data conversion in both directions.

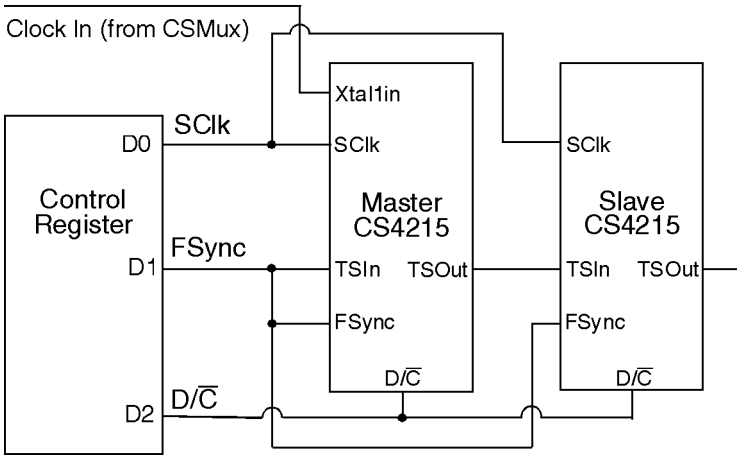
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3.5 Control Register Description (continued)

3.5.6 CS4215 SClk and FSync - Bits D1 and D0

These bits are used as timing signals during the initialization of the CS4215's in the Control Mode. These operations are described in the Control Mode section of the CS4215 manual in Appendix B.

Mode control data is first loaded into the Control Section of the Dual Port RAM (see Section 3.6.1, below) and then the Data/Control bit in this register (D2, see Section 3.5.5) is cleared to the logic '0' state. This places the CS4215's in Control Mode, where the SCLK input on the CS4215's (driven by the SClk bit, D1) is used as the clock signal instead of the CLK or XTL inputs. The FSync bit (D0 in this register) drives the Frame Synchronization input of both CS4215's in the bank, and the Time Slot Sync (TSIN) input of the Master CS4215. The Time Slot Sync output (TSOUT) of the Master CS4215 is connected to TSIN on the slave CS4215. This is illustrated in Figure 3-1, below.



D/C = 0: Control Mode - SClk and FSync are inputs on all CS4215's, driven by Setup Reg
D/C = 1: Data Mode - Xtal1In is clock input to Master, Master's SClk is an output that drives Slave's SClk inputs; FSync is an output on the Master and an input on the Slaves

Figure 3-1: Model 4265 - Clock & Sync Signals

When shifting setup data into the CS4215's, the FSync bit is set to the logic '1' state for the first serial bit of the Control Mode data stream and then cleared to logic '0' state for all the remaining bits. The SClk bit is toggled from the logic '1' state to logic '0' state for each bit in the serial Control Mode data stream. The states of these two bits are changed by writing to the Control Register.

Control Mode and initialization are discussed further in Section 4.1 of this manual, and in Appendix B (the CS4215 manual).

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3.6 Dual Port RAM Description

Each Analog I/O bank on the Model 4265 contains two Crystal Semiconductor CS4215 Dual Channel Σ–Δ A/D - D/A Converters. Each of these devices provides two channels of A/D conversion, input gain, input filtering, and optional compression. One of the devices acts as a master and the other as a slave.

Each of these devices also provides two channels of D/A conversion, output smoothing filters, output attenuation and optional expansion. Therefore, each bank provides four channels of A/D and D/A conversion.

Control of the CS4215's is accomplished by a combination of writing to the Dual Port RAM and to the Control Register. Data in the Dual Port RAM is circulated through the serial/parallel interface to the CS4215. Half of the data in the Dual Port RAM is for control functions such as operating mode, clock source, etc., and the other half of the data in the Dual Port RAM is for A/D and D/A data and for gain and attenuation settings.

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3.6 Dual Port RAM Description (continued).

Table 3-4: Model 4265 - Dual Port RAM Address Map - CS4215 Control Functions					
VME Address Offset from DPR_Base (Byte Address)	**Offset from DPR_Base for 32-bit DSP's (32-bit Address)**	**CS4215 Device**	**Channel**	**CS4215 Register**	**Read/Write**
0x0000	0x0000	Master	1 & 2	Status Register	Write
0x0004	0x0001	Master	1 & 2	Data Format Register	Write
0x0008	0x0002	Master	1 & 2	Serial Port Control Register	Write
0x000C	0x0003	Master	1 & 2	Test Register	Write
0x0010	0x0004	Master	1 & 2	Parallel Port Register	Write
0x0014	0x0005	Master	1 & 2	Reserved	Write
0x0018	0x0006	Master	1 & 2	Revision Level Register	Write
0x001C	0x0007	Master	1 & 2	Reserved	Write
0x0020	0x0008	Slave	3 & 4	Status Register	Write
0x0024	0x0009	Slave	3 & 4	Data Format Register	Write
0x0028	0x000A	Slave	3 & 4	Serial Port Control Register	Write
0x002C	0x000B	Slave	3 & 4	Test Register	Write
0x0030	0x000C	Slave	3 & 4	Parallel Port Register	Write
0x0034	0x000D	Slave	3 & 4	Reserved	Write
0x0038	0x000E	Slave	3 & 4	Revision Level Register	Write
0x003C	0x000F	Slave	3 & 4	Reserved	Write
0x0040	0x0010	Master	1 & 2	Status Register	Read
0x0044	0x0011	Master	1 & 2	Data Format Register	Read
0x0048	0x0012	Master	1 & 2	Serial Port Control Register	Read
0x004C	0x0013	Master	1 & 2	Test Register	Read
0x0050	0x0014	Master	1 & 2	Parallel Port Register	Read
0x0054	0x0015	Master	1 & 2	Reserved	Read
0x0058	0x0016	Master	1 & 2	Revision Level Register	Read
0x005C	0x0017	Master	1 & 2	Reserved	Read
0x0060	0x0018	Slave	3 & 4	Status Register	Read
0x0064	0x0019	Slave	3 & 4	Data Format Register	Read
0x0068	0x001A	Slave	3 & 4	Serial Port Control Register	Read
0x006C	0x001B	Slave	3 & 4	Test Register	Read
0x0070	0x001C	Slave	3 & 4	Parallel Port Register	Read
0x0074	0x001D	Slave	3 & 4	Reserved	Read
0x0078	0x001E	Slave	3 & 4	Revision Level Register	Read
0x007C	0x001F	Slave	3 & 4	Reserved	Read

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3.6 Dual Port RAM Description (continued)

In Table 3-4, page 33 and Table 3-5, below, the first column shows the VMEbus address offset for accessing each location in the Dual-Port RAM. The offset must be applied to the Dual-Port RAM Base address given in Table 3-1, on page 28. Each location corresponds to an 8-bit byte.

Table 3-5: Model 4265 - Dual Port RAM Address Map - CS4215 Data and Amplitude Functions

VME Address Offset from DPR_Base (Byte Address)	Offset from DPR_Base for 32-bit DSP's (32-bit Address)	CS4215 Device	Channel	CS4215 Register	Read/Write
0x0080	0x0020	Master	1	Left (Odd) MSB Data	Write
0x0084	0x0021	Master	1	Left (Odd) LSB Data	Write
0x0088	0x0022	Master	2	Right (Even) MSB Data	Write
0x008C	0x0023	Master	2	Right (Even) LSB Data	Write
0x0090	0x0024	Master	1	Left (Odd) Output Attenuation	Write
0x0094	0x0025	Master	2	Right (Even) Output Attenuation	Write
0x0098	0x0026	Master	1	Left (Odd) Input Gain	Write
0x009C	0x0027	Master	2	Right (Even) Input Gain	Write
0x00A0	0x0028	Slave	3	Left (Odd) MSB Data	Write
0x00A4	0x0029	Slave	3	Left (Odd) LSB Data	Write
0x00A8	0x002A	Slave	4	Right (Even) MSB Data	Write
0x00AC	0x002B	Slave	4	Right (Even) LSB Data	Write
0x00B0	0x002C	Slave	3	Left (Odd) Output Attenuation	Write
0x00B4	0x002D	Slave	4	Right (Even) Output Attenuation	Write
0x00B8	0x002E	Slave	3	Left (Odd) Input Gain	Write
0x00BC	0x002F	Slave	4	Right (Even) Input Gain	Write
0x00C0	0x0030	Master	1	Left (Odd) MSB Data	Read
0x00C4	0x0031	Master	1	Left (Odd) LSB Data	Read
0x00C8	0x0032	Master	2	Right (Even) MSB Data	Read
0x00CC	0x0033	Master	2	Right (Even) LSB Data	Read
0x00D0	0x0034	Master	1	Left (Odd) Output Attenuation	Read
0x00D4	0x0035	Master	2	Right (Even) Output Attenuation	Read
0x00D8	0x0036	Master	1	Left (Odd) Input Gain	Read
0x00DC	0x0037	Master	2	Right (Even) Input Gain	Read
0x00E0	0x0038	Slave	3	Left (Odd) MSB Data	Read
0x00E4	0x0039	Slave	3	Left (Odd) LSB Data	Read
0x00E8	0x003A	Slave	4	Right (Even) MSB Data	Read
0x00EC	0x003B	Slave	4	Right (Even) LSB Data	Read
0x00F0	0x003C	Slave	3	Left (Odd) Output Attenuation	Read
0x00F4	0x003D	Slave	4	Right (Even) Output Attenuation	Read
0x00F8	0x003E	Slave	3	Left (Odd) Input Gain	Read
0x00FC	0x003F	Slave	4	Right (Even) Input Gain	Read

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3.6 Dual Port RAM Description (continued)

The four channels within each bank are designated 1, 2, 3, and 4. Half of the locations are used for writing to the Dual Port RAM and the other half of the locations are for reading from the Dual Port RAM. The Write and Read addresses of the Control and Data sections of the Dual Port RAM are separated by a heavy line in Table 3-4 and Table 3-5. After byte has been written into an address in either section of the Dual Port RAM, it must be clocked through the device before it is available at the read address. See the programming example in Appendix A, or the CS4215 data sheet in Appendix B for further information.

As an example, suppose we wish to write to the bank C channel 2 output attenuation control byte. Assume A32 addressing mode and a VME_base address of 0x5A12 0000. The VMEbus address is given by:

	5A12	0000	(VME_base)
+		1000	(Bank C Offset - from Table 3-1)
+		0094	(Write Address for Ch 2 Output Attenuation - from Table 3-5)
	5A12	1094	(VME Address)

3.6.1 Control Section of the DPR - Control Mode Operation

Each of the four CS4215's contained in the Model 4265 requires eight 8-bit bytes (or 64 bits) of control information to be sent and retrieved during Control Mode initialization. These 8 bytes are sent bit-serially to the CS4215's in sequential 'time slots', identified as Time Slots 1 through 8. On-board hardware interfaces the DPR to these serial channels and maintains an easy to use memory-mapped image of each input byte and output byte. With eight CS4215's per Model 4265 (or four CS4215's in the eight-channel model), there are a total of 64 write bytes and 64 readback bytes contained in the Control Section of the DPR (32 of each in the eight-channel model). The DPR is organized as a byte-wide device so that each location corresponds to one of these bytes and therefore, one time slot.

Table 3-4, on page 33, gives the addresses for each register in the Control Section of the DPR. Table 3-6, on page 36, shows the bit definition for each of the 64 bits in the Control Mode data stream for each CS4215. These bits are arranged according to Time Slots that correspond exactly to bytes in the DPR. Each byte is addressed over the VMEbus as a unique VME address, using the bottom (least significant) 8 bits of the 16-bit word (D16) or the 32-bit longword (D32) data. The most significant bits of the word or longword are not used. Only 26 of the 64 control bits are actually used and the read/write capability of each bit varies with the bit's function. Bits in Table 3-6 identified with a logic state ('1' or '0'), rather than a symbolic name, **MUST** be written with the indicated state. Brief descriptions of these control bits can be found in Section 3.6.1.1 through Section 3.6.1.5 beginning on page 37. More information about these control bits may be found in the CS4215 manual in Appendix B.

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3.6 Dual Port RAM Description (continued)

3.6.1 Control Section of the DPR - Control Mode Operation (continued)

Table 3-6: Model 4265 - Control Mode Time Slot Bit Definitions for Each CS4215

DPR Address	Function	Time Slot	Bit D7	Bit D6	Bit D5	Bit D4	Bit D3	Bit D2	Bit D1	Bit D0
Cbase + 0	Status Register	1	0	0	1	MLB	OLB	DCB	0	0
Cbase + 4	Data Format Register	2	HPF	0	DFR2	DFR1	DFR0	ST	DF1	DF0
Cbase + 8	Serial Port Control Register	3	ITS	MCK2	MCK1	MCK0	BSEL1	BSEL0	XCLK	XEN
Cbase + C	Test Register	4	0	0	0	0	0	0	ENL	DAD
Cbase + 10	Parallel Port Register	5	PIO1	PIO2	0	0	0	0	0	0
Cbase + 14	Reserved	6	0	0	0	0	0	0	0	0
Cbase + 18	Revision Level Register	7	0	0	0	0	RV3	RV2	RV1	RV0
Cbase + 1C	Reserved	8	0	0	0	0	0	0	0	0

Note that the DPR addresses in Table 3-6, above, were given as Cbase+offset, where Cbase is the Control Base Address for a specific CS4215. The Cbase address for a given device is simply the lowest register address within that device, i. e. the Status Register address. Referring again to Table 3-4, note that the Cbase address used for read operations from a given device differs from the address used for write operations to the same device. For example, the Cbase address for write operations to the device containing channels 1 and 2 of Analog I/O Bank A would be the VME_base address. The Cbase address for read operations from the same device would be VME_base+0x40.

One must also be aware that the offsets given from the Cbase address in Table 3-6 assume that byte addressing is used, as would be the case for a VME Master using a 68000 series processor, such as Pentek's 4200 series. If a Pentek DSP board, such as the Models 4283, 4284, 4285 and/or 4290, which use long-word addressing, the offsets from Cbase given in Table 3-12 must be divided by a factor of 4, which results in an offset range for a given channel pair of 0 - 7.

For example, suppose we wish to read the revision level for the Slave CS4215 in Analog I/O Bank B, contained in the 4-bit field RV3 through RV0. We will again assume A32 addressing mode, a byte-addressing VME Master, and a VME_base address of 0x5A12 0000. This would be available by performing a read operation at the following address:

```
    5A12   0000  (VME_base)
+          0400  (Bank B Offset - from Table 3-1)
+          0078  (Slave Revision Level Readback Register - from Table 3-4)
    5A12   0478  (VME Address)
```


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3.6 Dual Port RAM Description (continued)

3.6.1 Control Section of the DPR - Control Mode Operation (continued)

In the example at the bottom of page 36, the four least significant bits of the word returned by the read operation at the calculated address would represent the encoded revision level. See Section 3.6.1.15, page 43 for information about associating the returned code with a revision level.

The flowchart in Figure 3-2, on page 38, illustrates the sequence of operations in Control Mode.

3.6.1.1 Data/Control Bit (DCB) - CS4215 Status Register (Time Slot 1), Bit D2

This bit is referred to as the CLB (Control Latch Bit) in the CS4215 Manual in Appendix B. It should be cleared to the logic '0' state for all control mode operations, and set to the logic '1' state for all data mode operations. During initialization, the readback registers are polled to see when this bit cleared to the logic '0' state. When it does, we reset it to the logic '1' state, and then send two additional frames of valid control information. A reset sets this bit to the logic '1' state.

3.6.1.2 Output Level Bit (OLB) - CS4215 Status Register (Time Slot 1), Bit D3

When this bit is cleared to the logic '0' state, the full scale voltage at the CS4215's Line Outputs is 2.8 V_{P-P}. When this bit is set to the logic '1' state, the full scale voltage at the CS4215's Line Outputs is 2.0 V_{P-P}. A reset clears this bit to the logic '0' state.

3.6.1.3 Microphone Level Bit (MLB) - CS4215 Status Register (Time Slot 1), Bit D4

This bit controls the full-scale input level at the Microphone inputs, which are unused in the Model 4265. The state of this bit is therefore trivial in this implementation.

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3.6 Dual Port RAM Description (continued)

3.6.1 Control Section of the DPR - Control Mode Operation (continued)

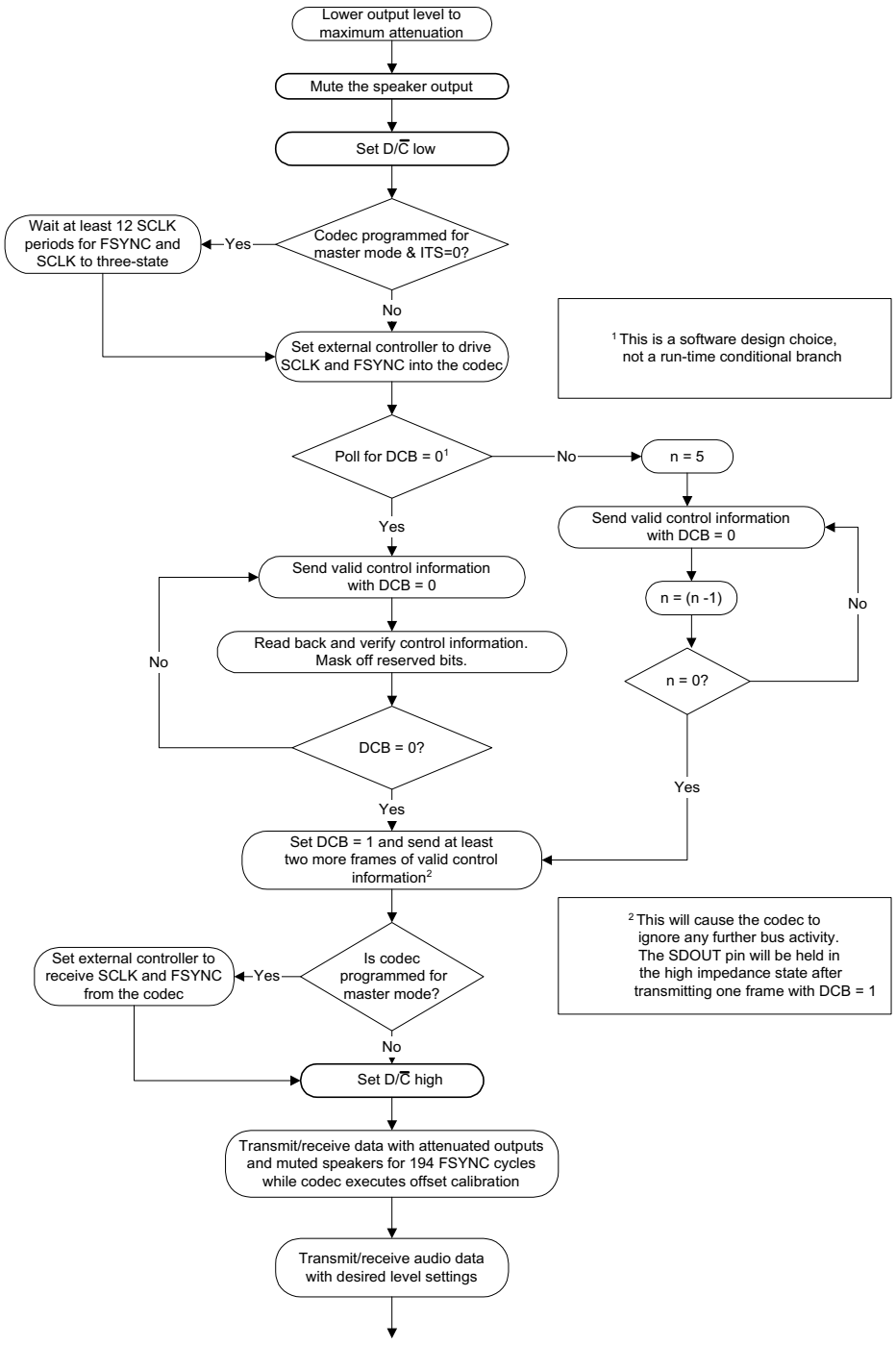


Figure 3-2: CS4215 Control Mode Operation Flow Chart

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3.6 Dual Port RAM Description (continued)

3.6.1 Control Section of the DPR - Control Mode Operation (continued)

3.6.1.4 Data Format Selection Bits (DF1 & DF0)

- CS4215 Data Format Register (Time Slot 2), Bits D1 & D0

The format for data to be output from the CS4215's A/D converters, and for data to be input to the CS4215's D/A converters, is selected by these two bits, according to Table 3-7, below.

Table 3-7: Model 4265 - CS4215 Data Format Selection Bits (DF1 & DF0) - Data Format Register, Bits D1 and D0

DF1 (D1)	DF0 (D0)	Selected Data Format
0	0	Linear - 16-bit 2's complement
0*	1*	Compressed - 8-bit μ-Law*
1	0	Compressed - 8-bit A-Law
1	1	Linear - 8-bit unsigned
* - state after reset		

3.6.1.5 Stereo Bit (ST)

- CS4215 Data Format Register (Time Slot 2), Bit D2

In Mono mode, digital and analog inputs to the "right" channels of the CS4215 chips (these are the even-numbered channels of the 4265) are disabled. The analog signal presented to the "left" (odd) A/D input of a given CS4215 is digitally output for both channels (the odd input channel and next higher even channel). Digital data presented to the "left" (odd) D/A input of a given CS4215 will generate identical analog outputs on both of that chip's channels (i. e., that odd channel and the next higher even channel). In stereo mode, all digital output channels from the CS4215's track the identically numbered A/D inputs, and all analog CS4215 outputs track the identically numbered D/A inputs.

Stereo mode is selected by setting this bit to the logic '1' state. Clearing this bit to the logic '0' state selects Mono mode, which is the state after reset.

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3.6 Dual Port RAM Description (continued)

3.6.1 Control Section of the DPR - Control Mode Operation (continued)

3.6.1.6 Data Conversion Frequency Selection Bits (DFR2 - DFR0) - CS4215 Data Format Register (Time Slot 2), Bits D5 - D3

These three bits are used to select the quantity by which the selected input clock signal, selected by the Clock Source Select Bits (D7 and D6 in the 4265's Control Register, see Section 3.5.1) will be divided, to determine the sampling rate for both A/D and D/A Conversion. Table 3-8, below, gives the divisors that can be obtained by the programming of these bits, and the sample rates that will result if either of the internal crystal oscillators is selected as the clock source.

Table 3-8: Model 4265 - CS4215 Data Conversion Frequency Bits(DFR2 thru DFR0) - Data Format Register Bits D5 thru D3

DFR2 (D5)	DFR1 (D4)	DFR0 (D3)	Clock Divisor	Sample Frequency	
				With 24.576 MHz Crystal Oscillator	With 16.9344 MHz Crystal Oscillator
0*	0*	0*	3072*	8.000 kHz	5.5125 kHz
0	0	1	1536	16.000 kHz	11.025 kHz
0	1	0	896	27.429 kHz	18.900 kHz
0	1	1	768	32.000 kHz	22.050 kHz
1	0	0	448	54.857 kHz†	37.800 kHz
1	0	1	384	64.000 kHz†	44.100 kHz
1	1	0	512	48.000 kHz	33.075 kHz
1	1	1	2560	9.600 kHz	6.615 kHz

* - state after reset

† - these sample rates are above the CS4215's specified maximum sampling rate - operation above 48 kHz is not guaranteed

3.6.1.7 High Pass Filter Bit (HPF) - CS4215 Data Format Register (Time Slot 2), Bit D7

When this bit is set to the logic '1' state, a digital high-pass filter is inserted following the A/D Converter, to minimize the DC offset. The filter is removed from the ADC path when this bit is cleared to the logic '0' state, which is the condition after reset.

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3.6 Dual Port RAM Description (continued)

3.6.1 Control Section of the DPR - Control Mode Operation (continued)

3.6.1.8 Transmitter Enable Bit (XEN)

- CS4215 Serial Port Control Register (Time Slot 3), Bit D0

This bit must be cleared to the logic '0' state to enable the serial data output from the ADC. A reset sets this bit to the logic '1' state, which tri-states serial data output.

3.6.1.9 Transmit Clock Bit (XCLK)

- CS4215 Serial Port Control Register (Time Slot 3), Bit D1

When this bit is cleared to the logic '0' state, the CS4215's SCLK and FSYNC pins are programmed as inputs, placing the device in Slave Mode. This is the condition after a reset. To place a CS4215 in Master mode, set this bit to the logic '1' state. The Master CS4215 generates the SCLK and FSYNC signals to drive the Slaves' inputs.

3.6.1.10 Bit Rate Select Bits (BSEL1 & BSEL0)

- CS4215 Serial Port Control Register (Time Slot 3), Bits D3 & D2

The number of bits that comprise a data frame is determined by the settings of these two bits, according to Table 3-9, below. As implemented in the Model 4265, ONLY the 128 bits/frame setting should be used. The reset state is 256 bits/frame.

Table 3-9: Model 4265 - CS4215 Bit Rate Select Bits (BSEL1 & BSEL0) - Serial Port Control Register, Bits D3 and D2

BSEL1 (D3)	BSEL0 (D2)	Selected Frame Length
0	0	64 bits/frame
0*	1*	128 bits/frame*
1†	0†	256 bits/frame†
1	1	Reserved - Do Not Use
* - **only** usable setting for 4265		† - state after reset

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3.6 Dual Port RAM Description (continued)

3.6.1 Control Section of the DPR - Control Mode Operation (continued)

3.6.1.11 Clock Source Select Bits (MCK2 - MCK0)

- CS4215 Serial Port Control Register (Time Slot 3), Bits D6 - D4

The CS4215's internal clock select multiplexer is not utilized in the Model 4265. An external MUX, controlled by the Clock Source Select bits in the 4265's Control Register (see Section 3.5.1) is used instead, to select between one of the two on-board crystal oscillators (24.567 MHz and 16.9344 MHz), the signal applied to the front panel's EXT CLK connector, or, on units equipped with Option 002, the Frequency Synthesizer.

The output of the external MUX drives the XTAL1 input on the Master CS4215, and the Master's SCLK (programmed as an output by setting the XCLK bit to the logic state '1', D1 in this register) drives the SCLK on the Slaves (programmed as inputs by clearing their XCLK bits to the logic '0' state). These Clock Source Select Bits must therefore be programmed to select the XTAL1 input on the Master and the SCLK input on the slaves. Table 3-10, below, describes these settings.

Table 3-10: Model 4265 - CS4215 Clock Source Select Bits (MCK2 thru MCK0) - Serial Port Control Register - Bits D6 thru D4

MCK2 (D6)	MCK1 (D5)	MCK0 (D4)	Selected Clock Source	Comments
0*	0*	0*	SCLK input*	Use this setting for slaves. 128 bits /frame (BSEL(1,0) = 0,1) and XCLK = 0
0	0	1	XTAL1 input	Use this setting for Master. 128 bits /frame (BSEL(1,0) = 0,1) and XCLK =1
* - state after reset				

3.6.1.12 Immediate Tri-State Bit (ITS)

- CS4215 Serial Port Control Register (Time Slot 3), Bit D7

When this bit is cleared to the logic '0' state (the condition following a reset), the SCLK and FSYNC pins may require up to 12 clock periods to switch to the high-impedance state after the D/$\overline{C}$ input goes low. To force SCLK and FSYNC to tri-state immediately when D/$\overline{C}$ goes low, set this bit to the logic '1' state.

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3.6 Dual Port RAM Description (continued)

3.6.1 Control Section of the DPR - Control Mode Operation (continued)

3.6.1.13 Loopback Mode Bit (DAD) and Loopback Enable Bit (ENL) - CS4215 Test Register (Time Slot 4), Bits D0 and D1

In the normal operating and initialization cases, all bits in this register are cleared to the logic '0' state. These two bits are used to enable and select testing modes. D1, the ENL bit, enables loopback testing when set to the logic '1' state. D0, the DAD bit, is significant only when D1 is set. The digital-digital loopback mode is selected by clearing DAD to the logic '0' state, and the digital-analog-digital loopback mode is selected when DAD is set to the logic '1' state. See the CS4215 Manual in Appendix B for definitions of these loopback modes.

3.6.1.14 Parallel I/O Bits (PIO1 & PIO0) - CS4215 Parallel Port Register (Time Slot 5), Bits D7 & D6

In the normal operating and initialization cases, all bits in this register are cleared to the logic '0' state. A reset sets these two bits to the logic '1' state. These bits reflect the states present at the CS4215's PIO1 and PIO0 pins, which are pulled high on the Model 4265. See the CS4215 Manual in Appendix B for further details.

3.6.1.15 CS4215 Hardware Revision Level Bits (VER3 - VER0) - CS4215 Version Register (Time Slot 7), Bits D3 - D0

In the normal operating and initialization cases, all bits in this register are cleared to the logic '0' state. The hardware revision level of the CS4215 can be read in the four LSB's of this register, as shown in Table 3-11, below. See the CS4215 Manual in Appendix B for information about the differences between the three revisions of this device. Pentek has built Model 4265s with all three revisions of the CS4215, but (except in the case of units that have had parts replaced) any given unit will have parts that are all of the same revision. To date, all new revisions of the CS4215 have been backward compatible.

Table 3-11: Model 4265 - CS4215 Hardware Revision Level Bits (VER3 - VER0) - Version Register - Bits D3 - D0

VER3 (D3)	VER2 (D2)	VER1 (D1)	VER0 (D0)	CS4215 Revision
0	0	0	0	Rev. C
0	0	0	1	Rev. D
0	0	1	0	Rev. E

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3.6 Dual Port RAM Description (continued)

3.6.2 Data Section of the DPR - Data Mode Operation

Each CS4215 utilizes eight bytes of input data and eight bytes of output data for write and readback operations once every sampling period. Half of this data consists of A/D and D/A sampled data and the other half consists of 'static' data such as gain, attenuation and other channel setup information. The A/D and D/A sampled data typically changes every sampling period, but the static, setup data typically changes only occasionally.

Because of the differing requirements of these data types, the Model 4265 provides two separate facilities for handling these two types of data:

- A/D and D/A data are handled by Comm Ports
- Static Data is stored in the Data Section of the DPR.

The first feature allows the 'C40-compatible Processor to efficiently send data to the D/A and read data from the A/D converters in block mode (DMA) transfers, with a FIFO to absorb the discrepancy between the regular sampling rate and the burst operation of the processor.

The second feature allows the VMEbus Master to write the static bytes once and then not have to write this information again unless a change is required. The DPR 'refreshes' the static data automatically every sampling period from the data stored in it, thus saving a significant amount of data flow over the VMEbus.

A convenient feature of the Model 4265's DPR operation is that when a data sample is delivered to a D/A converter (i. e., is sent over the Comm Port), it is also automatically stored in the DPR in its natural time slot position. If no subsequent samples are sent, on-board circuitry automatically reuses the last data point written to the DPR as the next data point for the D/A converter. This provides two very useful features:

- Following conversion of the last sample received over the Comm Port, the DAC output is held at the last programmed DC level. This is preferable to having it suddenly change to 0 volts or become undefined.
- The DPR can be used as an alternate path for delivering data to the D/A converter. This may be useful in some applications where the output voltage need not change frequently.

Similarly, the A/D operation takes advantage of the DPR by writing each A/D sample both to the input of the A/D FIFO (which precedes the Comm port in the data path) and to the natural time slot location in the DPR. This allows the A/D output data in the Model 4265 to be fetched from either the Comm Port or the DPR.

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3.6 Dual Port RAM Description (continued)

3.6.2 Data Section of the DPR - Data Mode Operation (continued)

As a result of these features, the data section of the DPR contains both A/D and D/A data as well as static input gain and output attenuation data. Just as in the Control section of the DPR, for a 16 channel unit, there are 64 write bytes and 64 readback bytes in the Data section of the DPR.

The CS4215 Manual, in Appendix B, refers to the two channels within each chip as 'left' and 'right' channels. On the Model 4265, this 'left' and 'right' designation translates into odd and even channel numbers, respectively. For example, the left channel in the first CS4215 is channel 1, and the right channel is channel 2.

In Table 3-12, below, the bit definition of each of the eight time slots in the Data section of each CS4215 is shown. Note that the Data section DPR addresses in Table 3-12 (like the Control section DPR addresses in Table 3-6) are expressed as Dbase+offset, where Dbase is the Data section base address for a specific CS4215. The Dbase address is simply the lowest address in a given device's data section, i. e., the left (odd) MSB location. Also note that, as in the Control section, different Dbase addresses are used for write operations (data being sent into the CS4215) and readback operations (data being retrieved from the CS4215).

Table 3-12: Model 4265 - Data Mode Time Slot Bit Definitions for Each CS4215

DPR Address	Function	Time Slot	Bit D7	Bit D6	Bit D5	Bit D4	Bit D3	Bit D2	Bit D1	Bit D0
Dbase+ 0	Left (Odd) Channel Signal	1	Most Significant 8 bits of 16-bit Sample							
Dbase+ 4	Left (Odd) Channel Signal	2	Least Significant 8 bits of 16-bit Sample							
Dbase+ 8	Right (Even) Channel Signal	3	Most Significant 8 bits of 16-bit Sample							
Dbase+ C	Right (Even) Channel Signal	4	Least Significant 8 bits of 16-bit Sample							
Dbase+ 10	Left (Odd) Output Attenuation	5	HE	LE	LO5	LO4	LO3	LO2	LO1	LO0
Dbase+ 14	Right (Even) Output Attenuation	6	0	SE	RO5	RO4	RO3	RO2	RO1	RO0
Dbase+ 18	Left (Odd) Input Gain	7	PIO1	PIO0	OVR	IS	LG3	LG2	LG1	LG0
Dbase+ 1C	Right (Even) Input Gain	8	MA3	MA2	MA1	MA0	RG3	RG2	RG1	RG0

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3.6 Dual Port RAM Description (continued)

3.6.2 Data Section of the DPR - Data Mode Operation (continued)

Note that the left (odd) and right (even) channel audio time slot descriptions in Table 3-12, above, apply to data for both the A/D and the D/A: the A/D data is readback data and the D/A data is write data.

The nomenclature used for the bits shown in Table 3-12 is identical to that used in the CS4215 Manual in Appendix B. The functions of these bits are described briefly in the subsections that follow, and also in the CS4215 Manual.

For example, suppose we wish to set output attenuation level for Bank D, channel 2. Since channel 2 is an even (i. e., right) channel, this would be available by performing a write at address Dbase+14. The six least significant bits of the data word written would be used as the attenuation data. See Section 3.6.2.2 for details about attenuation settings. A sample calculation for the actual address to write is shown below, again assuming a VME_base address of 0x5A12 0000, and byte addressing.

```
      5A12  0000 (VME_base)
+           1400 (Bank D Offset - from Table 3-1)
+           0080 (Master Dbase Address for Writes - from Table 3-5)
+           0014 (Right Output Attenuation Address - from Table 3-12)
      5A12  1494 (VME Address)
```

3.6.2.1 Signal Data - CS4215 Data RAM (Time Slots 1-4), Bits D0 - D7

The first four time slots in the Data Section of the 4265's Dual-Port RAM are used for actual signal data. Output samples are serially shifted out of the CS4215 and converted into two 8-bit parallel words. Then, they are sent to both the DPR readback address corresponding to the appropriate time slots (see Table 3-12) and to the A/D FIFO, which precedes the Output Comm Port. The data written to the DPR by the A/D is overwritten every sample period, while the samples delivered to the A/D FIFO remain there until they are read via the Comm Port. If the A/D FIFO should become full, subsequent samples will still be written to the appropriate DPR time slot addresses, but will be overwritten every frame until room becomes available in the FIFO.

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3.6 Dual Port RAM Description (continued)

3.6.2 Data Section of the DPR - Data Mode Operation (continued)

3.6.2.1 Signal Data - CS4215 Data RAM (Time Slots 1-4), Bits D0 - D7

Signal generation data samples for the CS4215's D/A section that are written to the 4265's D/A (Input) Comm Port are written to a Dual-Port RAM buffer external to the CS4215, and are also, simultaneously, written into the DPR write addresses corresponding to appropriate time slots, internal to the CS4215. If the external buffer becomes empty, the last samples written into the DPR for each enabled channel are retained and used as the data for any subsequent output samples, until more data is delivered via the Comm Port. If the external buffer becomes full, the Comm Port's READY signal is de-asserted until room becomes available.

3.6.2.2 Output Attenuation Bits (LO5 - LO0 and RO5 - RO0) - CS4215 Data RAM (Time Slots 5 & 6), Bits D5 - D0

These two six-bit groups set the output attenuation level for the CS4215's D/A section. Time slot 5 sets the attenuation for the odd (left) channels, and time slot 6 sets it for the even (right) channels.

The attenuation is adjustable from 0 dB (all six bits cleared to the logic '0' state) to –94.5 dB (all six bits set to the logic '1' state) in 1.5 dB steps. These correspond to full scale output voltage ranges from 2.0 V_{RMS} (at 0 dB attenuation) to approximately 0.71 nV_{RMS} (at –94.5 dB attenuation). D0 is the Least Significant Bit (weighted at –1.5 dB attenuation) and D5 is the Most Significant Bit (weighted at –48 dB attenuation).

Table 3-13, below, gives the weights of each bit in these fields. Resetting the CS4215 sets all six of these bits to the logic '1' state, resulting in the minimum output voltage range (i. e., maximum attenuation).

Table 3-13: Model 4265 - CS4215 Output Attenuation Bits (LO5 thru LO0 & RO5 thru RO0) - Dual-Port RAM Data Section - Time Slots 5 & 6 - Bits D5 thru D0 - Bit Weights When Set ('1')

Bit	D5 (L/RO5)	D4 (L/RO4)	D3 (L/RO3)	D2 (L/RO2)	D1 (L/RO1)	D0 (L/RO0)
Attenuation	-48 dB	-24 dB	-12 dB	-6 dB	-3 dB	-1.5 dB

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3.6 Dual Port RAM Description (continued)

3.6.2 Data Section of the DPR - Data Mode Operation (continued)

3.6.2.3 Line Output Enable Bit (LE)

- CS4215 Data RAM (Time Slot 5), Bit D6

This bit must be set to the logic '1' state to enable the CS4215's Line Outputs. These outputs are buffered and delivered to the 4265's front panel as the D/A outputs. Resetting the CS4215 clears this bit to the logic '0' state, thus disabling the 4265's analog outputs.

3.6.2.4 Headphone Output Enable Bit (HE)

- CS4215 Data RAM (Time Slot 5), Bit D7

The CS4215's Headphone outputs are unused on the 4265, which makes the state of this bit trivial. After a reset, this bit is cleared to the logic '0' state, which disables the Headphone outputs.

3.6.2.5 Speaker Output Enable Bit (SE)

- CS4215 Data RAM (Time Slot 6), Bit D6

The CS4215's Speaker output is unused on the 4265, which makes the state of this bit trivial. After a reset, this bit is cleared to the logic '0' state, which disables the Speaker output.

3.6.2.6 A/D Data Invalid Bit (ADI)

- CS4215 Data RAM (Time Slot 6), Bit D7

In the readback portion of the CS4215's DPR Data section, this bit is set to the logic '1' state to indicate that the CS4215 is in self-calibration. This means that any data samples that may appear at the A/D output are invalid. Self-calibration is initiated immediately after reset and also immediately after the transition from Control Mode to Data Mode operation. This bit should always be cleared to the logic '0' state in the write section of the DPR.

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3.6 Dual Port RAM Description (continued)

3.6.2 Data Section of the DPR - Data Mode Operation (continued)

3.6.2.7 Input Gain Bits (LG3 - LG0 and RG3 - RG0) - CS4215 Data RAM (Time Slots 7 & 8), Bits D3 - D0

These two four-bit groups set the input gain level for the CS4215's A/D section. Time slot 7 sets the gain for the odd (left) channels, and time slot 8 sets it for the even (right) channels. The gain is adjustable from 0 dB (all four bits cleared to the logic '0' state) to +22.5 dB (all four bits set to the logic '1' state) in 1.5 dB steps. These correspond to full scale input voltage ranges from 2.0 V_{RMS} (at 0 dB gain) to approximately 11.25 mV_{RMS} (at +22.5 dB gain). D0 is the Least Significant Bit (weighted at +1.5 dB gain) and D5 is the Most Significant Bit (weighted at +12 dB gain). Table 3-14, below, gives the weights of each bit in these fields. Resetting the CS4215 clears all four of these bits to the logic '0' state, resulting in the maximum input voltage range (i. e., minimum gain).

Table 3-14: Model 4265 - CS4215 Input Gain Bits (LG3 thru LG0 & RG3 thru RG0) - Dual-Port RAM Data Section - Time Slots 7 & 8 - Bits D3 thru D0 - Bit Weights When Set ('1')

Bit	D3 (L/RG3)	D2 (L/RG2)	D1 (L/RG1)	D0 (L/RG0)
Gain	+12 dB	+6 dB	+3 dB	+1.5 dB

On the Model 4265 Option 003, the Full Scale Input Range is from 20.0 V_{P-P} (at 0 dB gain) to approximately 112.5 mV_{P-P} (at +22.5 dB gain).

3.6.2.8 Input Select Bit (IS) - CS4215 Data RAM (Time Slot 7), Bit D4

When cleared to the logic '0' state (the condition after resetting the CS4215), this bit selects the Line input pin as the input for the A/D converter. Setting this bit to the logic '1' state causes the CS4215 to use the microphone input pin at the A/D stage's input. Since the mic input is unconnected on the Model 4265, this bit should always be cleared to the logic '0' state.

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3.6 Dual Port RAM Description (continued)

3.6.2 Data Section of the DPR - Data Mode Operation (continued)

3.6.2.9 Overrange Bit (OVR) - CS4215 Data RAM (Time Slot 7), Bit D5

When this bit is set to the logic '1' state in the readback section of the CS4215's Data RAM, it indicates that an overrange condition has occurred at the A/D input. The indicator remains set until cleared by writing a '0' to this bit in the write section of Data RAM. This bit must be set to the logic '1' state in the write section of Data RAM to enable overrange detection. After an overrange has been detected, therefore, this bit must be written with a '0' to clear the overrange, and set to the logic '1' state in the next frame to re-enable detection. A reset clears this bit to the logic '0' state.

3.6.2.10 Parallel I/O Bits (PIO1 and PIO0) - CS4215 Data RAM (Time Slot 7), Bits D7 and D6

These bits may be used as parallel I/O bits in some implementations of the CS4215. However, the pins with which this feature is associated are unconnected (except for being pulled up) on the Model 4265. These bits should always be cleared to the logic '0' state, and their readback states ignored.

3.6.2.11 Monitor Path Attenuation Bits (MA3 - MA0) - CS4215 Data RAM (Time Slot 8), Bits D7 - D4

These bits may be used to set the attenuation of the signal at the CS4215's monitor outputs. Since these outputs are unused on the Model 4265, it is good practice to set all these bits to the logic '1' state for maximum attenuation (i. e., minimum signal) at these outputs. That is also the reset condition for these bits.

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3.7 Sample Clock Generator

The sample clock generation system for the Model 4265 is quite flexible. Each of the four 4-channel Analog I/O banks can operate at a different sample clock frequency, but all four channels of A/D and D/A conversion within a given bank must use the same sample clock.

The CS4215 utilizes a high speed oversampling clock to achieve the sigma delta A/D and D/A conversion and digital filtering. This oversampling clock operates at 256 times the effective sample rate. Within each CS4215 is an oversampling clock generator which is derived from the reference clock by using an internal clock divider. The relationship between the sample rate, the oversampling clock and the reference clock are given by the formulas:

$$\text{Sample Clock} = \text{Oversampling Clock} \div 256$$
$$\text{Sample Clock} = \text{Reference Clock} \div N$$

where N is the division ratio of the clock divider in the CS4215.

3.7.1 Selecting the Reference Clock

Depending upon the options included in your Model 4265, there are either three or four independent selections for the reference clock source for each of the 4-channel banks. These are:

- 24.576 MHz Crystal Oscillator
- 16.9344 MHz Crystal Oscillator
- External Reference Clock Input (Front Panel EXT CLK BNC)
- Frequency Synthesizer (in Option 002 only)

The reference clock for a given I/O bank is selected by setting the two bits (D7 and D6) in the Control Register for that bank. See Table 3-3, in Section 3.5.1, for details.

3.7.2 Setting the CS4215 Clock Divisor - 24.576 and 16.9334 MHz Oscillators

The CS4215 clock divider can be programmed to operate at any of eight fixed division ratios, N. Therefore, the relationship between the reference clock and the sampling clock is constrained to eight ratios, given by the formula:

$$\text{Sample Clock} = \text{Reference Clock} \div N$$

Three bits in the Data Format Registers (one of the CS4215 control registers) are used to select one of the eight division ratios. These bits are DFR2, DFR1, and DFR0. See Table 3-8, and Section 3.6.1.6 for the bit definitions and addressing. Note that both CS4215's (master and slave devices) in one bank must have the same setting for these DFR bits.

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3.7 Sample Clock Generator (continued)

3.7.3 Setting the CS4215 Clock Divisor - External Reference Clock Operation

The signal applied to them front panel EXT CLK connector can be used as the reference clock for internal sample clock generation. In this case, both CS1 bits (CS1 and CS0) in the Control Register (see Section 3.5.1) must be set to the logic '1' state. The DFR bits can then be set to divide the external clock frequency by any of the eight division ratios shown in Table 3-8, in Section 3.6.1.6 on page 40.

For example, if a frequency of 15 kHz is required and an external clock frequency of 7.68 MHz is available, the DFR bits can be set to '110' to select a division ratio of 512. Another combination which would produce the same 15 kHz sample rate is an external clock of 13.44 MHz and a divisor of 896 (DFR setting is '010').

The maximum sampling rate at which the Model 4265 is guaranteed to meet the specifications listed in Section 1.2 is 48 kHz. The maximum frequency for an external clock signal is 24.576 MHz.

3.7.4 Setting the CS4215 Clock Divisor - Frequency Synthesizer Clock Operation (Option 002 ONLY)

On units equipped with Option 002 (and only on such units), a Phase-Locked Loop-based frequency synthesizer can be substituted for the crystal oscillators used for internal sample clock generation. In this case, the CS1 bit must be set to logic '1' state and the CS0 bit must be cleared to logic '0' state in the Control Register (see Section 3.5.1).

The frequency synthesizer has an output frequency range of DC to 25 MHz with resolution of 0.0058 Hz. The sample frequency is determined by the synthesizer frequency and the division ratio, N, according to the following formula:

$$\text{Sample Clock} = \text{Synthesizer Clock} \div N$$

Three bits in the Data Format Registers (one of the CS4215 control registers) are used to select one of the eight division ratios. These bits are DFR2, DFR1, and DFR0. See Table 3-8, in Section 3.6.1.6 for the bit definitions and Section 3.6 for addressing information. Note that both CS4215's (master and slave devices) in one bank must have the same setting for these DFR bits.

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3.8 **Operation of the Frequency Synthesizer** - Option 002 ONLY

The Frequency Synthesizer, provided as Option 002 on the Model 4265, utilizes Direct Digital Synthesis to generate a clock between 0 and 25.0 MHz. Although the Model 4265 contains only one frequency synthesizer, the synthesizer's output clock can be used as the reference clock for any or all of the four 4-channel Analog I/O banks. This reference clock is used by the CS4215's to determine the sample frequency for the A/D and D/A converters. The operation of the CS4215 clock generator and selection of the reference clock are described in Section 3.7. Note that the clock select bits CS1 and CS0 must be set as described in Section 3.7.4, or in Table 3-3 in Section 3.5.1 to utilize the frequency synthesizer's output as the reference clock.

In general, once the frequency synthesizer is selected as the clock source, the sample frequency is determined by the synthesizer frequency and the division ratio, N, according to the following formula:

$$\text{Sample Clock} = \text{Synthesizer Clock} \div N$$

Three bits in the Data Format Registers (one of the CS4215 control registers) are used to select one of the eight division ratios. These bits are DFR2, DFR1, and DFR0. See Table 3-8, in Table 3.6.1.6 for the bit definitions and addressing. Note that both CS4215's (master and slave devices) in any given Analog I/O bank must have the same setting for these DFR bits. The relationship between the DFR bit values and the resultant range of synthesized sampling frequencies is given in Table 3-8, on page 40.

Once the correct divisor is determined and the DFR bits are set, the operating frequency of the frequency synthesizer must be set. First, one must assure that the synthesizer is not being held in the reset state (which holds all of its internal registers at a value of zero) by writing a '1' to address VME_base+0x2044. The desired frequency is set using a 32-bit binary value programmed in the Frequency Synthesizer. This 32-bit word is written as four bytes, with the most significant byte (D31 - D24) written first, and the remaining bytes in order of decreasing significance (i. e., least significant byte last). As is the case for all data transfers, the data must always be placed in the Least Significant bits (D7 - D0) of the VME data bus. These four bytes are all written to a register that is accessed from the VMEbus at location VME_base+0x2040. The 32-bit synthesizer data word (Synth_data in the equation presented below), as a function of the desired synthesizer output frequency ($f_{OUT} \leq 25$ MHz) is calculated as follows:

$$\text{Synth_Data} = 2^{32} \frac{f_{out}}{50\ \text{MHz}}$$

These four writes place the frequency data, in proper order, in a parallel assembly register within the synthesizer. This transfer scheme is illustrated in Figure 3-3 on page 54. The contents of the parallel assembly register are passed on to the phase accumulator (where they are actually used to generate the output frequency) when a load pulse is delivered to the synthesizer. In the Model 4265, this pulse is created when a dummy write operation (the data is unused and therefore trivial) is performed at address VME_base+0x2020.

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3.8 **Operation of the Frequency Synthesizer** - Option 002 ONLY (continued)

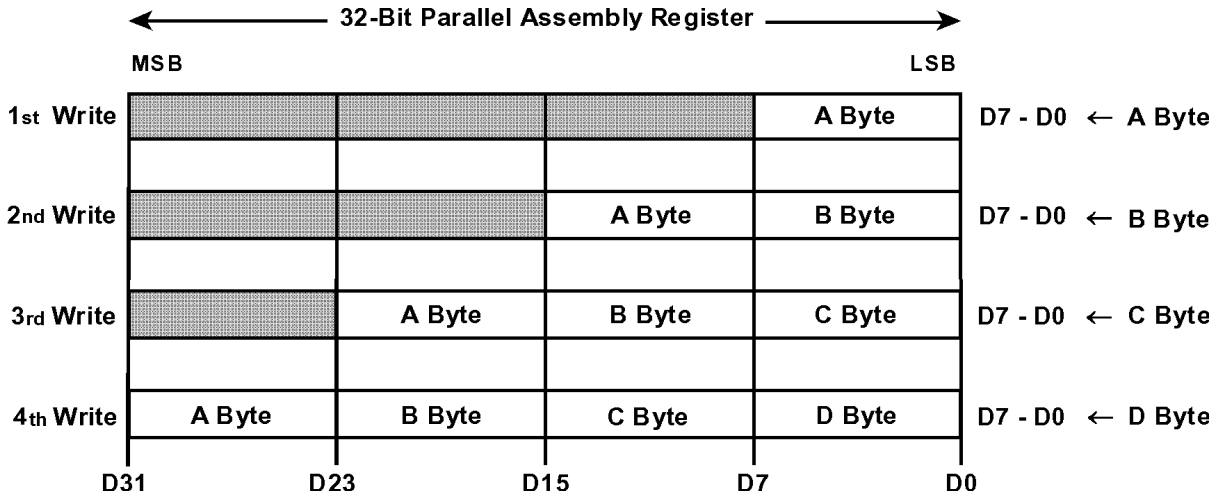


Figure 3-3: Model 4265 - Frequency Synthesizer Data Loading Sequence

Table 3-15, below, summarizes the VMEbus addresses associated with the Model 4265's synthesizer section, and the functions of the registers at those addresses.

Table 3-15: Model 4265, Option 002 - VMEbus Registers for Frequency Synthesizer

VMEbus Address	Address	Register Name	Function
VME_base+0x2044	R/W	DDS_Control	Set to logic '1' to release Synth reset, clear to '0' to assert reset
VME_base+0x2040	W.O.	Synth_Data	32-bit frequency control word written here as 4 bytes, MSB first
VME_base+0x2020	W.O.	Synth_Load	After Synth_data is written, dummy write here loads data into Synth

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Chapter 4: Comm Port Interface

4.1 Introduction

There are two methods of interfacing data and control to the Model 4265:

VMEbus interface	- used for initializing the board
'C40-compatible Comm Ports	- used for A/D and D/A data I/O, attenuation and gain settings

Chapter 3 deals with the VMEbus interface and this chapter deals with the Comm Port interface. It describes how to access the CS4215's from the 'C40-compatible Comm Ports.

There are four pairs of 'C40-compatible Comm Ports on the front panel of the Model 4265: four for input and four for output. The input Comm Ports (labeled **D/A IN - X** on the front panel, where X is the channel designation (A, B, C or D)) can be used to set gain and attenuation and to deliver data to the D/A converters. The output Comm Ports (labeled **A/D OUT - X**) can be used to read back gain and attenuation settings, and to acquire data from the A/D converters. The locations and pinouts of the front panel Comm Port connectors.

Each of the transfers to and from the Comm Ports is conducted on a 32-bit word basis using four consecutive 8-bit bytes. Two bytes of the 32-bit transfer are used for data and two bytes are used for control. One of the two control bytes is used for controlling input Comm Port functions and one is used for controlling output Comm Port functions.

4.2 Input Comm Port Description

The four bytes utilized for each 32-bit input Comm Port transfer are grouped as shown in Table 4-1, below.

Table 4-1: Model 4265 - Input Comm Port Data Transfer Formats

Byte Field	D/A Data Transfer Format	Atten/Gain Transfer Format
D31 - D24	Most Sig. byte of D/A Data	(not used)
D23 - D16	Least Sig. byte of D/A Data	Atten/Gain Settings
D15 - D8	Input Control Byte	Input Control Byte
D7 - D0	Output Control Byte	Output Control Byte

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4.2 Input Comm Port Description (continued)

4.2.1 D/A Data Transfer Format

The two most significant bytes (D31 - D24 and D23 - D16) are used for input data (data to be delivered to the D/A converters). The most significant data bit is D31 and the least significant bit is D16. Data for the D/A converters is written in 2's complement format.

4.2.2 Attenuation/Gain Settings Transfer Format

Only the second byte (D23-D16) is used for sending the attenuation and gain settings (for the A/D and D/A converters). The most significant data bit is D23 and the least significant bit is D16. See Section 3.6.2.2 and Section 3.6.2.7 for information about gain and attenuation settings.

4.2.3 Input Control Byte Description

Table 4-2, below, gives the bit definition of each bit in used in the Input Control Byte, bits D15 - D8 of the 32-bit Input Comm Port transfer. These bits are used to steer the upper two bytes (data bytes) to the appropriate destinations and are also used to control various functions of the unit.

Table 4-2: Model 4265 - Input Comm Port - Input Control Byte (D15 - D8)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Clear_ Error	Error_ Control	N/U	O/P FIFO Reset	D/C Mode Select	Attn/Gain Select	Chan_ Select_1	Chan_ Select_0
Bit Function	0 = No Clear 1 = Clear Err Bit	0=Err Bits Off 1=Err Bits On	Not Used	0 = Reset 1 = Run	0 = Data 1 = Control	0 = Atten 1 = Gain	See Table 4-3 in Section 4.2.3.5	

4.2.3.1 Error Bits - D15 (Clear) and D14 (Control)

Bits D15 and D14 of the 32-bit Input Comm Port data word are concerned with error handling. Error bits, which indicate that data for a given channel has been lost, are located in the Output (A/D) Comm Port's Status Byte. Setting the D14 bit in this byte to the logic '1' state enables operation of the error bits. Clearing D14 to the logic '0' state disables the error bits. To clear an enabled error bit, set the D15 bit in this byte to the logic '1' state. D15 should be cleared to the logic '0' state for normal operation.

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4.2 Input Comm Port Description (continued)

4.2.3 Input Control Byte Description (continued)

4.2.3.2 Output FIFO Reset - Bit D12

Clearing the D12 bit in the Input Control byte to the logic '0' state resets the Output (A/D) FIFO, clearing any data it may contain. For normal operation of the Output FIFO, D12 in this byte should be set to the logic '1' state.

4.2.3.3 Data/Control Mode Select - Bit D11

When the D11 bit in the Input Control Byte is cleared to the logic '0' state, the D31 - D16 bits of the Input Comm Port carry 16 bits of D/A input data to be placed in CS4215 time slots 1, 2, 3 or 4. The channel that the data is intended for is indicated by the channel select bits, D9 & D8 (see Section 4.2.3.5, below).

When D11 of the Input Control Byte is set to the logic '1' state, D31 - D24 of the Input Comm Port are unused, and D23 - D16 carry 8 bits of settings information bound for CS4215 time slot 5 or 6 (if it is an attenuation setting) or 7 or 8 (if it is a gain setting). The D10 bit in this byte indicates whether the setting is for attenuation or gain (see Section 4.2.3.4, below), and the D9 & D8 bits determine which channel the setting information is intended for (see Section 4.2.3.5 on page 58).

4.2.3.4 Attenuation/Gain Select - Bit D10

This bit only has meaning when the D11 bit (see Section 4.2.3.3, above) is set to the logic '1' state, indicating that the D23 - D16 bits of the Input Comm Port carry settings information rather than data for the D/A converter. If D10 of the Input Control Byte is cleared to the logic '0' state, the data in D23 - D16 will be treated as an attenuation setting, and delivered to CS4215 time slot 5 or 6, depending upon the channel selected. If D10 of the Input Control Byte is set to the logic '1' state, the data in D23 - D16 will be treated as a gain setting, and delivered to CS4215 time slot 7 or 8, again depending upon the channel selected by bits D9 and D8 in this byte (see Section 4.2.3.5 on page 58).

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4.2 Input Comm Port Description (continued)

4.2.3 Input Control Byte Description (continued)

4.2.3.5 Channel Selection Bits - D9 and D8

The settings of these two bits determine which of the four analog I/O channels in the bank will receive the data being sent by the Comm Port, according to Table 4-3, below.

Table 4-3: Model 4265 - Comm Port Interface - Input Control Byte - Channel Select Bits

D9	D8	Selected Channel
0	0	Channel 1 (Master, Left)
0	1	Channel 2 (Master, Right)
1	0	Channel 3 (Slave, Left)
1	1	Channel 4 (Slave, Right)

4.2.3.6 Output Control Byte Description

Table 4-4, below, gives the bit definition of each bit in the Output Control Byte, D7 - D0 of the 32-bit Input Comm Port transfer. These bits are used to enable the various types of data capable of being delivered to the Output Comm Ports.

Table 4-4: Model 4265 - Input Comm Port - Output Control Byte (D7 - D0)

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Status_ Chan_4	Data_ Chan_4	Status_ Chan_3	Data_ Chan_3	Status_ Chan_2	Data_ Chan_2	Status_ Chan_1	Data_ Chan_1
Bit Function	0 = Disable delivery of Channel Status or Data to Output Comm Port 1 = Enable delivery of Channel Status or Data to Output Comm Port							

In Table 4-4, Status refers to the readback of gain and attenuation settings for a given I/O channel, while Data refers to the 16 bits of sampled output data from the channel's A/D Converter.

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4.3 Output Comm Port Description

The four bytes utilized for each 32-bit Output Comm Port transfer are grouped as shown in Table 4-5, below.

Table 4-5: Model 4265 - Output Comm Port Data Transfer Formats

Byte Field	D/A Data Transfer Format	Atten/Gain Transfer Format
D31 - D24	Most Sig. Byte of A/D Data	(not used)
D23 - D16	Least Sig. Byte of A/D Data	Atten/Gain Readback
D15 - D18	Channel Address	Channel Address
D7 - D0	Comm Port Status	Comm Port Status

4.3.1 A/D Data Transfer Format

The two most significant bytes (D31-D24 and D23-D16) are used for output data (data produced by the A/D converters). The most significant data bit is D31 and the least significant bit is D16. Data from the A/D converters is delivered in 2's complement format.

4.3.2 Attenuation/Gain Readback Transfer Format

Only the second byte (D23 - D16) is used for reading back the attenuation and gain settings (for the A/D and D/A converters). The most significant data bit is D23 and the least significant bit is D16. See Section 3.6.2.2 and Section 3.6.2.7 for information about interpreting the data read back as a gain or attenuation setting.

4.3.3 Channel Address Byte Description

Table 4-6, below, gives the a definition of each bit used in the Channel Address Byte, bits D15 - D8 of the 32-bit Output Comm Port transfer. These bits are used to identify the upper two bytes (data bytes) as the type of transfer (either A/D data, gain or attenuation settings) and which channel the data represents.

Table 4-6: Model 4265 - Output Comm Port - Channel Address Byte (D15 - D8)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Not Used				D/C Mode Identify	Attn/Gain Identify	Chan_ Identify_1	Chan_ Identify_0
Bit Function	Always cleared to logic '0' state				0 = Data 1 = Control	0 = Atten 1 = Gain	See Table 4-7 in Section 4.3.3.3	

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4.3 Output Comm Port Description (continued)

4.3.3 Channel Address Byte Description (continued)

4.3.3.1 Data/Control Mode Identify - Bit D11

When the D11 bit in the Channel Address Byte is cleared to the logic '0' state, the D31 - D16 bits of the Output Comm Port carry 16 bits of A/D output data from CS4215 time slots 1, 2, 3 or 4. The channel that the data came from is indicated by the channel identify bits, D9 & D8 (see Section 4.3.3.3, below).

When D11 of the Channel Address Byte is set to the logic '1' state, D31 - D24 of the Output Comm Port are unused, and D23 - D16 carry 8 bits of settings readback information from CS4215 time slot 5 or 6 (if it is an attenuation setting) or 7 or 8 (if it is a gain setting). The D10 bit in this byte indicates whether the setting is for attenuation or gain (see Section 4.3.3.2, below), and the D9 & D8 bits determine which channel the setting was read back from (see Section 4.3.3.3, below).

4.3.3.2 Attenuation/Gain Identify - Bit D10

This bit only has meaning when the D11 bit (see Section 4.3.3.1, above) is set to the logic '1' state, indicating that the D23 - D16 bits of the Output Comm Port carry settings readback information rather than data from the A/D converter. If D10 of the Channel Address Byte is cleared to the logic '0' state, the data in D23 - D16 is an attenuation setting readback, from CS4215 time slot 5 or 6 (depending upon the channel identified). If D10 of the Channel Address Byte is set to the logic '1' state, the data in D23 - D16 is a gain setting readback, from CS4215 time slot 7 or 8, again depending upon the channel identified by bits D9 and D8 in this byte (see Section 4.3.3.3, below).

4.3.3.3 Channel Identification Bits - D9 and D8

The settings of these two bits identify which of the four analog I/O channels in the bank the data being sent by the Comm Port came from, according to Table 4-7, below.

Table 4-7: Model 4265 - Comm Port Interface - Channel Address Byte - Channel ID Bits

D9	D8	Identified Channel
0	0	Channel 1 (Master, Left)
0	1	Channel 1 (Master, Right)
1	0	Channel 3 (Slave, Left)
1	1	Channel 4 (Slave, Right)

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4.3 Output Comm Port Description (continued)

4.3.4 Comm Port Status Byte Description

Table 4-8, below, gives a definition of each bit in used in the Comm Port Status Byte, bits D7 - D0 of the 32-bit Output Comm Port transfer. These bits are used to indicate that data from a given channel has been lost due to FIFO overflow.

Table 4-8: Model 4265 - Output Comm Port - Comm Port Status Byte (D7 - D0) - Read Only

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	O/P_FIFO _Full	Error_ Enable	Not Used		Chan_4_ Error_Status	Chan_3_ Error_Status	Chan_2_ Error_Status	Chan_1_ Error_Status
Bit Function	0 = OK (No Err) 1 = FIFO Full	0 = Disabled 1 = Enabled	Always Cleared to Logic '0' State		0 = O.K. (No Error) 1 = Error (Data Lost)			

4.3.4.1 Output FIFO Full - Bit D7

This bit reflects the state of the state of the FULL flag on the FIFO that is located between the A/D Converter output of the CS4215 and the Output Comm Port. When this bit of the Comm Port Status Byte is set to the logic '1' state, the FIFO for that bank has been filled and data has been lost from at least one channel. The lower bits in the Status byte will tell which channels have actually been affected. A logic '0' in this bit indicates that the FIFO is not full, and no data has been lost.

4.3.4.2 Error Enable - Bit D6

This bit is essentially a readback of the Error Control Bit (D14) in the Input Control Byte. It will read back as a logic stat '1' when the error bits (D3 - D0 in this byte) are enabled, or as a logic state '0' when the error bits are disabled.

4.3.4.3 Channel Error Status Bits - D3 thru D0

These four bits in the Channel Status Byte indicate which channel(s) in the bank have actually lost data when the Fifo Full Bit (D7 in this byte) is set to the logic '1' state. Each of these four bits corresponds to one channel in the Comm Port's four-channel group. For all four of these bits, a logic state '1' indicates that the channel has lost data, and a logic state '0' indicates that no data has been lost. The D0 bit is for Channel 1 (the Master CS4215, left channel), D1 is for Channel 2 (Master CS4215, right channel), D2 is for Channel 3 (Slave CS4215, left channel) and D3 is for Channel 4 (Slave CS4215, right channel).

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AppendixA: Programming Examples

A.1 Introduction

Two sample programs are included in the following pages of this Appendix. The first, port65.c, allows a Pentek Model 4284 (TMS320C40 DSP-based VME/MIX Baseboard) to initialize the Model 4265 over the VMEbus, and then exchange Analog I/O data with it over the Comm Ports. The second, init65.c, allows the 4265 to be initialized by a Heurikon Model HKV3D (68030-based VME computer board), running the VxWorks operating system.

A.2 Program Code

The sample program code can be found on the following pages:

port65.c code - Page 1

init65.c code - Page 5

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```
/*********************************************************************
/* PORT65.C
/* 4270 using a 4265
*********************************************************************/

typedef volatile unsigned int uint;


/* Processor NUmbers */
#define PROC_A            0
#define PROC_B            1
#define PROC_C            2
#define PROC_D            3

/* Size of Input and Output Buffers */
#define BUF_SIZE          0x2000

/* functions and pointers for the 4270 */
uint in_comm_port(uint port_no, uint *data);
uint out_comm_port(uint port_no, uint data);

uint *datain, *dataout, *out_in, *cntrl, *channel;

main()
{
    void init_ptrs(uint proc, uint **InBuf, uint **OutBuf,
                   uint **BufStart, uint **BufEnd );
    void init_70(uint *OutBuf);
    void user_cntrl(void);

    uint i, o, port, control;
    uint *c40_reg;
    uint proc;
    int  inport, outport;
    uint *OutBuf, *InBuf;
    uint *BufStart, *BufEnd;

    /* Turn off Bus Timeouts */
    *(unsigned int *) 0x34000d = 0xff;

    /* Determine Which Processor this is */
    c40_reg = (uint *)0x340000u;

    proc = (*c40_reg & 0x300000u) >> 20;
```

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```
    /*  Based on the Processor Number Determine which Com Ports */
    if (proc == PROC_A )
    {
        inport = 5;
        outport = 2;
    }
    else if (proc == PROC_B)
    {
        inport = 5;
        outport = 2;
    }
    else if (proc == PROC_C)
    {
        inport = 5;
        outport = 2;
    }
    else   /* proc == PROC_D */
    {
        inport = 5;
        outport = 2;
    }


    /* Initialize 4270 */

    init_ptrs(proc, &InBuf, &OutBuf, &BufStart, &BufEnd);
    init_70(OutBuf);

    while(1){
        /* make sure buffers don't overlap */
        if( OutBuf != InBuf ){
           /* test and see if out comm port function worked */
           if(out_comm_port(outport, *OutBuf) == 1){
               ++OutBuf;

               /* if the end of buffer has been reached reset
               pointer */
               if( OutBuf == BufEnd)
                   OutBuf  = BufStart;
           }
        }

        /* test and see if out comm port function worked */
       if(in_comm_port(inport, InBuf) == 1){
           ++InBuf;

           /* if the end of buffer has been reached reset
              pointer */
           if( InBuf == BufEnd )
               InBuf = BufStart;
       }
       user_cntrl();
    }
}
```


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```
/* if the user changes data in the control buffer */
/* pass the information onto the 4265 bank */
void user_cntrl(void)
{
    uint control, port;

    if((*cntrl) != 0xffff0000u){
        port = ((*cntrl) & 0x03000000u) >> 24;
        control = (*cntrl) & 0xffffffu;
        out_comm_port(port, control);
        *cntrl = 0xffff0000u;
    }
}

/* Function to set up pointers and their initial values */
void init_ptrs(uint proc, uint **InBuf, uint **OutBuf,
               uint **BufStart, uint **BufEnd)
{
    /* 4270 pointers */
    datain  = (uint *)0x40001000;
    dataout = (uint *)0x40001001;
    out_in  = (uint *)0x40001002;
    cntrl   = (uint *)0x40001003;
    channel = (uint *)0x40001004;

    /* Buffers for storing comm port data */
    /* one is used for input data to c40 */
    /* while the other is used for output data */
    switch (proc)
    {
        case PROC_A:
            *OutBuf = (uint *)0x40002000u;
            *InBuf  = (uint *)0x40003000u;
            break;
        case PROC_B:
            *OutBuf = (uint *)0x40004000u;
            *InBuf  = (uint *)0x40005000u;
            break;
        case PROC_C:
            *OutBuf = (uint *)0x40006000u;
            *InBuf  = (uint *)0x40007000u;
            break;
        case PROC_D:
            *OutBuf = (uint *)0x40008000u;
            *InBuf  = (uint *)0x40009000u;
            break;
    }
    *BufStart = *OutBuf;
    *BufEnd = *OutBuf + BUF_SIZE;

}
```

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```
/* Function to initial 4270 pointers  */
void init_70(uint *OutBuf)
{
    uint i, j;

    *datain  = 0;
    *dataout = 0;
    *out_in = 0x7055u;    /* the control for in and out c40 comm ports */
                          /* 0x70 = input control, 0x55 = output control */
    *cntrl = 0xffff0000u; /* dual port ram - user control - flag */

    /* set up ramp test function in output buffers */
    for(i = 0; i < BUF_SIZE; i = i + 4){
        for(j = 0; j < 4; j++)
            *(OutBuf + (i+j)) = (i << 18) | (j << 8);
    }
}

/* C40 input comm port function */
uint in_comm_port(uint port_no, uint *data)
{
    uint *comm_port_address, i;

    comm_port_address =(uint *)((port_no * 16) + 0x100040u);
    if(((*comm_port_address) & 0x1e00u) != 0){
        *data = *(comm_port_address + 1);
        return(1);
    }
    else return(0);
}

/* C40 output comm port function */
uint out_comm_port(uint port_no, uint data)
{
    uint *comm_port_address;

    comm_port_address =(uint *)((port_no * 16) + 0x100040u);
    if (((*comm_port_address) & 0x1e0u) != 0x1e0u){
        *(comm_port_address + 2) = (data & 0xffff0f00u) | (*out_in);
        return(1);
    }
    else{
        return(0);
    }
}
```


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```
/*************************************************************************
/* init65.c
/* This program initializes the 4265 over VME from HKV3D running VxWorks
*************************************************************************/


#include "vxWorks.h"
#include "sysLib.h"
#include "msgQLib.h"
#include "iv.h"
#include "vme.h"
#include "taskLib.h"
#include "usrLib.h"

#define CHAN_16        1

/* 4265 Memory and Register locations */
#define DPR_A          0x0000
#define DPR_B          0x0400
#define DPR_C          0x1000
#define DPR_D          0x1400

#define REG_A          0x0800
#define REG_B          0x0c00
#define REG_C          0x1800
#define REG_D          0x1c00

#define PLL            0x2000

/* 4265 control register bit positions and values */
#define FSYNC          0x01
#define FCLK           0x02
#define DATA_CMND      0x04
#define VME_COMM       0x08
#define RESET          0x10
#define DPR_OFFSET     0x20
#define CLK24M         0x00
#define CLK16M         0x40
#define CLKSYN         0x80
#define CLKEXT         0xc0

/* The 4265 can be access in A24 or A32 Address Modes */
#define A24_BASE         0x00120000L
#define A32_BASE         0x5a120000L
#define A24_ACCESS_MODE  VME_AM_STD_SUP_DATA    /* 0x3d */
#define A32_ACCESS_MODE  VME_AM_EXT_SUP_DATA    /* 0x0d */


/* Current Address Mode Selected */
#define ACCESS_MODE      A24_ACCESS_MODE
#define BASE_ADDRESS     A24_BASE


/* Declare Forward and External Declarations */
extern void init_bank(UINT32 Dpr, UINT32 Reg);
extern void jumpstart(UINT32 Dpr, UINT32 Reg);
extern STATUS Pokew(UINT32 Addr, UINT16 Data);
extern STATUS Peekw(UINT32 Addr, UINT16 *Data);
extern void   delay (UINT16 cnt);
```

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```
STATUS
Init65()
{
    /* Pointer for the 4265 */
    UINT32 DprPtrA, Reg_A;
    UINT32 DprPtrB, Reg_B;
    UINT32 DprPtrC, Reg_C;
    UINT32 DprPtrD, Reg_D;

    /* Pointers for the 4265 */
    DprPtrA = (UINT32)(BASE_ADDRESS | DPR_A);
    DprPtrB = (UINT32)(BASE_ADDRESS | DPR_B);
    DprPtrC = (UINT32)(BASE_ADDRESS | DPR_C);
    DprPtrD = (UINT32)(BASE_ADDRESS | DPR_D);

    Reg_A = (UINT32)(BASE_ADDRESS | REG_A);
    Reg_B = (UINT32)(BASE_ADDRESS | REG_B);
    Reg_C = (UINT32)(BASE_ADDRESS | REG_C);
    Reg_D = (UINT32)(BASE_ADDRESS | REG_D);

    /* Initialize the 4265 banks (memory) */

    init_bank(DprPtrA, Reg_A);
    init_bank(DprPtrB, Reg_B);
#if CHAN_16
    init_bank(DprPtrC, Reg_C);
    init_bank(DprPtrD, Reg_D);
#endif

    /* Jump start each of the banks so that */
    /* the banks 4215 a/d and d/a start running */

    jumpstart(DprPtrA, Reg_A);
    jumpstart(DprPtrB, Reg_B);
#if CHAN_16
    jumpstart(DprPtrC, Reg_C);
    jumpstart(DprPtrD, Reg_D);
#endif

    printf("Init65 Completed\n");

}

/* Initialize the banks dual port memory */
void init_bank(UINT32 Dpr, UINT32 Reg)
{
    UINT16 i;
    UINT16 data;
```

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```
/********************** CONTROL MODE  ***********************************/
    /* set the Dpr offset bit high */
    if (Pokew(Reg, 0x0020) != OK)     /* reset to 4215, send D/C bit low  */
    {
        printf("Error Writing to 4265\n");
        return;
    }
    if (Peekw(Reg, &data) != OK)
    {
        printf("Error Reading to 4265\n");
        return;
    }
    printf("Data = %x\n", data);
    /* From Here On Assume Pokew and Peekw are OK */

    /* First do the Master chip */
    Pokew(Dpr+0x0,0x0);  /* time slot 1: Status Register with DCB bit low */
    Pokew(Dpr+0x4,0x4);  /* time slot 2: Data Format Register */
    Pokew(Dpr+0x8,0x16); /* time slot 3: Serial Port Control Register */
    Pokew(Dpr+0xc,0x0);  /* time slot 4: Test Register */
    Pokew(Dpr+0x10,0x0);  /* time slot 5: Parallel Port Register */
    Pokew(Dpr+0x14,0x0);  /* time slot 6: Reserved Register */
    Pokew(Dpr+0x18,0x0);  /* time slot 7: 4215 Revision Register */
    Pokew(Dpr+0x1c,0x0);  /* time slot 8: Reserved Register */

/* Then do the Slave chips */

    Pokew(Dpr+0x20, 0x0); /* time slot 1: Status Register with DCB bit low */
    Pokew(Dpr+0x24, 0x4); /* time slot 2: Data Format Register */
    Pokew(Dpr+0x28, 0x34);/* time slot 3: Serial Port Control Register */
    Pokew(Dpr+0x2c, 0x0); /* time slot 4: Test Register */
    Pokew(Dpr+0x30, 0x0); /* time slot 5: Parallel Port Register */
    Pokew(Dpr+0x34, 0x0); /* time slot 6: Reserved Register */
    Pokew(Dpr+0x38, 0x0); /* time slot 7: 4215 Revision Register */
    Pokew(Dpr+0x3c, 0x0); /* time slot 8: Reserved Register */

/************************** DATA MODE  ***********************************/

/* First do the Master chip */

    Pokew(Dpr+0x80, 0x0);  /* time slot 1: Left  Audio Output Data MS 8 bits */
    Pokew(Dpr+0x84, 0x0);  /* time slot 2: Left  Audio Output Data LS 8 bits */
    Pokew(Dpr+0x88, 0x0);  /* time slot 3: Right Audio Output Data MS 8 bits */
    Pokew(Dpr+0x8c, 0x0);  /* time slot 4: Right Audio Output Data LS 8 bits */
    Pokew(Dpr+0x90, 0x40); /* time slot 5: Left  Channel Output Control */
    Pokew(Dpr+0x94, 0x0);  /* time slot 6: Right Channel Output Control */
    Pokew(Dpr+0x98, 0x0);  /* time slot 7: Left  Channel Input Control */
    Pokew(Dpr+0x9c, 0xf0); /* time slot 8: Right Channel Input Control */

/* Then do the Slave chips */

    Pokew(Dpr+0xa0, 0x0);  /* time slot 1: Left  Audio Output Data MS 8 bits */
    Pokew(Dpr+0xa4, 0x0);  /* time slot 2: Left  Audio Output Data LS 8 bits */
    Pokew(Dpr+0xa8, 0x0);  /* time slot 3: Right Audio Output Data MS 8 bits */
    Pokew(Dpr+0xac, 0x0);  /* time slot 4: Right Audio Output Data LS 8 bits */
    Pokew(Dpr+0xb0, 0x40); /* time slot 5: Left  Channel Output Control  */
    Pokew(Dpr+0xb4, 0x0);  /* time slot 6: Right Channel Output Control */
    Pokew(Dpr+0xb8, 0x0);  /* time slot 7: Left  Channel Input  Control */
    Pokew(Dpr+0xbc, 0xf0); /* time slot 8: Right Channel Input  Control */
}
```


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```
void jumpstart( UINT32 Dpr, UINT32 Reg)
{
    void SendCtl(UINT32 reg);
    UINT16 i;
    UINT16 data;

    Pokew(Reg, 0x0010);       /* Release reset to 4215, send D/C bit low */

    Pokew(Dpr+0x40, 0xff);    /* "Zero" out 4215 #1 return data destination */
    Pokew(Dpr+0x60, 0xff);    /* "Zero" out 4215 #2 return data destination */

    Peekw(Dpr+0x40, &data);
    printf("dpr = %lx\n", Dpr+0x40);
    while((data & 4)!=0){ /* Wait for 4215 #1 to set DCB bit low */
       SendCtl( Reg );
       Peekw(Dpr+0x40, &data);
    }

    Peekw(Dpr+0x60, &data);
    while((data & 4)!=0){ /* Wait for 4215 #2 to set DCB bit low */
       SendCtl( Reg );
       Peekw(Dpr+0x60, &data);
    }

    Pokew(Reg, 0x0030);      /* Move 4215 out of the way to access dpr */

    Pokew(Dpr+0x0,0x4);      /* Set chip #1 DCB bit high, data mode */
    Pokew(Dpr+0x20,0x4);     /* Set chip #2 DCB bit high, data mode */

    Pokew(Reg, 0x0010);      /* Release reset to 4215, send D/C bit low */

    SendCtl( Reg );          /* 2 more frames */
    SendCtl( Reg );

    Pokew(Reg, 0x001c);      /* data mode and comm port enable */
}


void SendCtl( UINT32 reg)
{
    UINT16 i;
    UINT16 data;

    Peekw(reg, &data);
    Pokew(reg, data | 0x3);  /* Send fsync high and sclk high */
    delay(10);
    Peekw(reg, &data);
    Pokew(reg, data & 0xfd); /* Send fsync high and sclk low */
    delay(10);

    for(i = 0; i < 128; i++) {
        Peekw(reg, &data);
        Pokew(reg, (data & 0xfe) | 0x2); /* Send fsync low and sclk high */
        delay(10);
        Peekw(reg, &data);
        Pokew(reg, data & 0xfc);         /* Send fsync low and sclk low */
        delay(10);
    }
}
```


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```
void delay(UINT16 cnt)   /* Length of delay does not need to be exact */
{
    INT16  i;

    for (i = 0; i < cnt; ++i);
}

STATUS
Pokew(UINT32 Addr, UINT16 Data)
{
    UINT32  pokeAddr;

    sysBusToLocalAdrs(ACCESS_MODE, Addr, &pokeAddr);
    if (vxMemProbe(pokeAddr, WRITE, 2, &Data) == -1)
      return (ERROR);
    return (OK);
}

STATUS
Peekw(UINT32 Addr, UINT16 *Data)
{
    UINT32  peekAddr;

    sysBusToLocalAdrs(ACCESS_MODE, Addr, &peekAddr);
    if (vxMemProbe(peekAddr, READ, 2, Data) == -1)
      return (ERROR);
    return (OK);
}
```


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Appendix B: Crystal Semiconductor Corporations CS4215 16-bit Multimedia Audio Codec Data Sheet

B.1 *CS4215 Data Sheet*

The following pages contain a reprint of Crystal Semiconductor's CS4215 Data Sheet.

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Semiconductor Corporation

CS4215

16-Bit Multimedia Audio Codec

Features

- Sample Frequencies from 4 kHz to 50 kHz
- 16-bit Linear, 8-bit Linear, μ-Law, or A-Law Audio Data Coding
- Programmable Gain for Analog Inputs
- Programmable Attenuation for Analog Outputs
- On-chip Oscillators
- +5V Power Supply
- Microphone and Line Level Analog Inputs
- Headphone, Speaker, and Line Outputs
- On-chip Anti-Aliasing/Smoothing Filters
- Serial Digital Interface

General Description

The CS4215 is an Mwave™ audio codec.

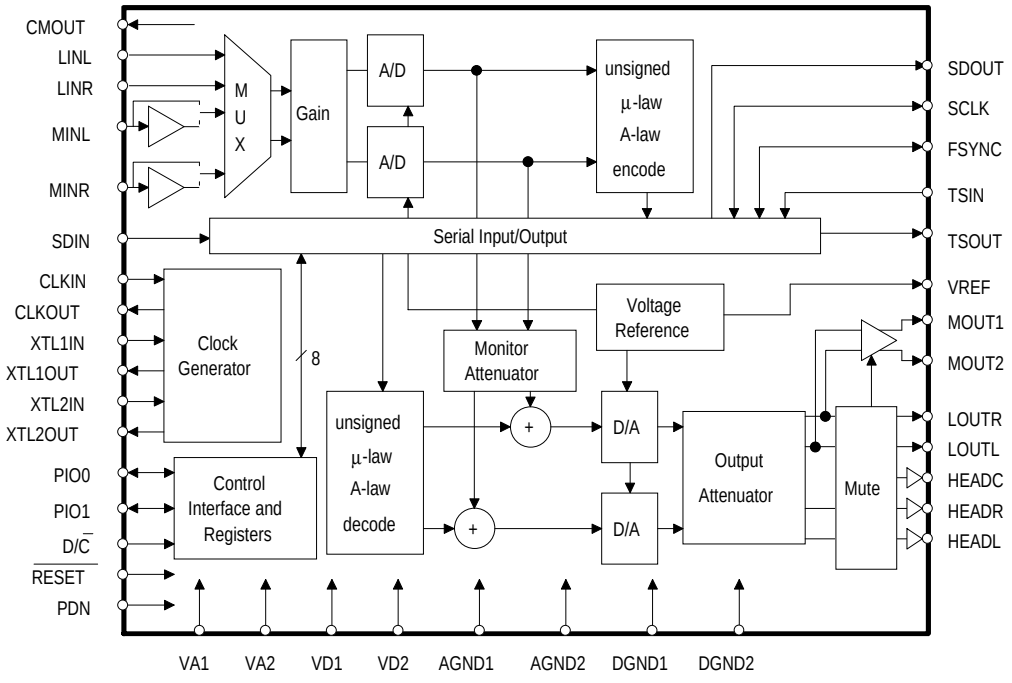
The CS4215 is a single-chip, stereo, CMOS multimedia codec that supports CD-quality music, FM radio-quality music, telephone-quality speech, and modems. The analog-to-digital and digital-to-analog converters are 64×oversampled delta-sigma converters with on-chip filters which adapt to the sample frequency selected.

The +5V only power requirement makes the CS4215 ideal for use in workstations and personal computers.

Integration of microphone and line level inputs, input and output gain setting, along with headphone and monitor speaker driver, results in a very small footprint.

Ordering Information:

CS4215-KL	0°C to 70°C	44-pin PLCC
CS4215-KQ	0°C to 70°C	100-pin TQFP
CDB4215	Evaluation Board	



This data sheet was written for Revision E CS4215 codecs and later. For differences between Revision E and previous versions, see *Appendix A*.

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ANALOG CHARACTERISTICS(T_A = 25°C; VA1, VA2, VD1, VD2 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1, VD2; Full Scale Input Sine wave, No Gain, No Attenuation 1 kHz; Conversion Rate = 48 kHz; No Gain, No Attenuation, SCLK = 3.072 MHz; Measurement Bandwidth is 10 Hz to 20 kHz; Slave mode; Unless otherwise specified.)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution			16	-	-	Bits
ADC Differential Nonlinearity			-	-	±0.9	LSB
Instantaneous Dynamic Range	Line Inputs Mic Inputs	IDR	80 72	84 78	- -	dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD	- -	- -	0.012 0.032	% %
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs		- -	80 60	- -	dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs		- -	- -	0.5 0.5	dB dB
Frequency Response (Note 1)	(0 to 0.45 Fs)		-0.5	-	+0.2	dB
Programmable Input Gain	Line Inputs Mic Inputs		-0.2 19.8	- -	23.5 44	dB dB
Gain Step Size			-	1.5	-	dB
Absolute Gain Step Error			-	-	0.75	dB
Offset Error with HPF = 0 (No Gain)	Line Inputs (AC Coupled) Line Inputs (DC Coupled) Mic Inputs		- - -	±150 ±10 ±400	±400 ±150 -	LSB
Offset Error with HPF = 1 (Notes 1,2) (No Gain)	Line Inputs (AC Coupled) Line Inputs (DC Coupled) Mic Inputs		- - -	0 0 0	±5 ±5 ±5	LSB
Full Scale Input Voltage:	(MLB=0) Mic Inputs (MLB=1) Mic Inputs Line Inputs		0.250 2.50 2.50	0.28 2.8 2.8	0.310 3.10 3.10	Vpp V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Input Resistance	(Note 3)		20	-	-	kΩ
Input Capacitance			-	-	15	pF
CMOUT Output Voltage (Maximum output current = 400 µA)	(Note 4)		1.9	2.1	2.3	V

Notes:
1. This specification is guaranteed by characterization, not production testing.
2. Very low frequency signals will be slightly distorted when using the HPF.
3. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance.
4. DC current only. If dynamic loading exists, then CMOUT must be buffered or the performance of ADC's and DAC's may be degraded.

***** Parameter definitions are given at the end of this data sheet.

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ANALOG CHARACTERISTICS (Continued)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation; Unless Otherwise Specified.						
DAC Resolution			16	-	-	Bits
DAC Differential Nonlinearity			-	-	±0.9	LSB
Total Dynamic Range		TDR	-	95	-	dB
Instantaneous Dynamic Range (OLB = 1)	(All Outputs)	IDR	80	85	-	dB
Total Harmonic Distortion (OLB = 1)	Line Out (Note 5) Headphone Out (Note 6) Speaker Out (Note 6)	THD	- - -	- - -	0.025 0.2 0.32	% % %
Interchannel Isolation	Line Out (Note 5) Headphone Out (Note 6)		- -	80 40	- -	dB dB
Interchannel Gain Mismatch	Line Out Headphone		- -	- -	0.5 0.5	dB dB
Frequency Response (Note 1)	(0 to 0.45 Fs)		-0.5	-	+0.2	dB
Programmable Attenuation	(All Outputs)		0.2	-	-94.7	dB
Attenuation Step Size			-	1.5	-	dB
Absolute Attenuation Step Error			-	-	0.75	dB
Offset Voltage	Line Out		-	10	-	mV
Full Scale Output Voltage with OLB = 0	Line Output (Note 5) Headphone Output (Note 6) Speaker Output-Differential (Note 6)		2.55 3.6 7.3	2.8 4.0 8.0	3.08 4.4 8.8	V_{pp} V_{pp} V_{pp}
Full Scale Output Voltage with OLB = 1	Line Output (Note 5) Headphone Output (Note 6) Speaker Output-Differential (Note 6)		1.8 1.8 3.6	2.0 2.0 4.0	2.2 2.2 4.4	V_{pp} V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Deviation from Linear Phase			-	-	1	Degree
Out of Band Energy	(22 kHz to 100 kHz) Line Out		-	-60	-	dB
Power Supply						
Power Supply Current (Note 7)	Operating Power Down		- -	110 0.5	140 2	mA mA
Power Supply Rejection	(1 kHz)		-	40	-	dB

Notes: 5. 10 kΩ, 100 pF load. Headphone and Speaker outputs disabled.
6. 48 Ω, 100 pF load. For the headphone outputs, THD with 10kΩ, 100pF load is 0.02%.
7. Typically, 50% of the power supply current is supplied to the analog power pins (VA1, VA2) and 50% is supplied to the digital power pins (VD1, VD2). Values given are for unloaded outputs.

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A/D Decimation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.0	µs

D/A Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.1/Fs	s

DIGITAL CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = 5V)

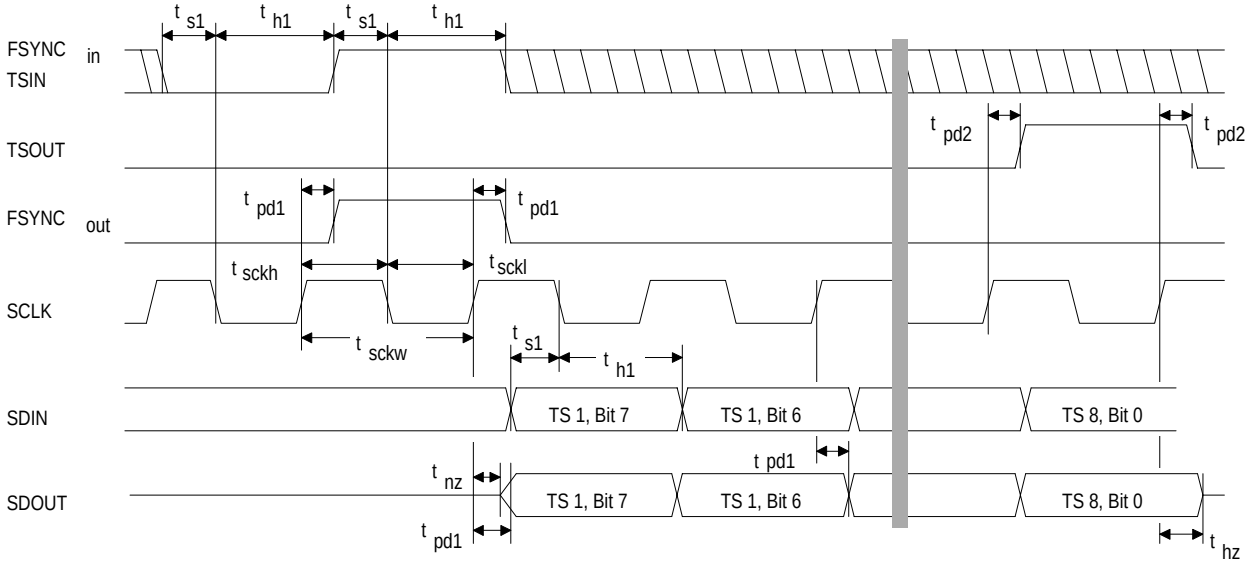
Parameter	Symbol	Min	Max	Units
High-level Input Voltage	V_{IH}	(VD1,VD2)-1.0	(VD1,VD2)+0.3	V
Low-level Input Voltage	V_{IL}	-0.3	1.0	V
High-level Output Voltage at I_0 = -2.0 mA	V_{OH}	(VD1,VD2)-0.2	-	V
Low-level Output Voltage at I_0 = 2.0 mA	V_{OL}	-	0.1	V
Input Leakage Current (Digital Inputs)		-	10	µA
Output Leakage Current (High-Z Digital Outputs)		-	10	µA

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SWITCHING CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = +5V, outputs loaded with 30 pF; Input Levels: Logic 0 = 0V, Logic 1 = VD1, VD2)

Parameter		Symbol	Min	Typ	Max	Units
SCLK period	Master Mode, XCLK = 1 (Note 8) Slave Mode (XCLK = 0)	t_{sckw} tsckw	- 80	1/(Fs*bpf) -	- -	s ns
SCLK high time	Slave Mode, XCLK = 0 (Note 9)	tsckh	25	-	-	ns
SCLK low time	Slave Mode, XCLK = 0 (Note 9)	tsckl	25	-	-	ns
Input Setup Time		t_{s1}	15	-	-	ns
Input Hold Time		t_{h1}	10	-	-	ns
Input Transition Time	10% to 90% points		-	-	10	ns
Output delay		tpd1	-	-	28	ns
SCLK to TSOUT		tpd2	-	-	30	ns
Output to Hi-Z state	Timeslot 8, bit 0	t_{hz}	-	-	12	ns
Output to non-Hi-Z	Timeslot 1, bit 7	t_{nz}	15	-	-	ns
Input Clock Frequency	Crystals CLKIN (Note 10)		- 1.024	- -	27 13.5	MHz MHz
Input Clock (CLKIN) low time			30	-	-	ns
Input Clock (CLKIN) high time			30	-	-	ns
Sample rate		Fs	4	-	50	kHz
$\overline{\text{RESET}}$ low time	(Note 11)		500	-	-	ns

Notes:
8. In Master mode with BSEL1,0 set to 64 or 128 bits per frame (bpf), the SCLK duty cycle is 50%. When BSEL1,0 is set to 256 bpf, SCLK will have the same duty cycle as CLKOUT. See Internal Clock Generation section.
9. In Slave mode, FSYNC and SCLK must be derived from the master clock running the codec (CLKIN, XTAL1, XTAL2).
10. Sample rate specifications must not be exceeded.
11. After powering up the CS4215, RESET should be held low for 50 ms to allow the voltage reference to settle.



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ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital Analog	VD1,VD2 VA1,VA2	-0.3 -0.3	6.0 6.0	V V
Input Current	(Except Supply Pins)		-	±10.0	mA
Analog Input Voltage			-0.3	(VA1, VA2)+0.3	V
Digital Input Voltage			-0.3	(VD1, VD2)+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

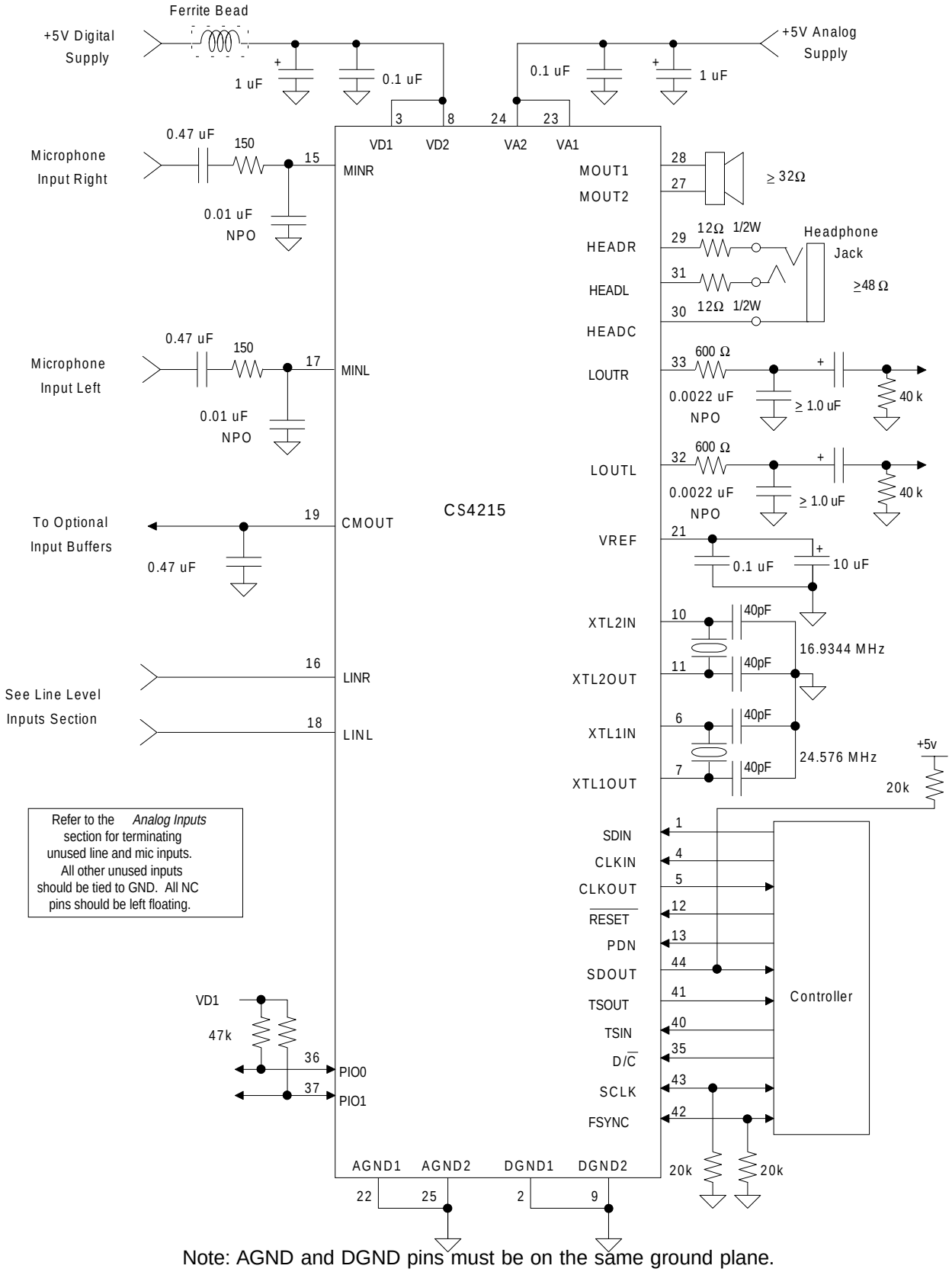
Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital (Note 8) Analog (Note 8)	VD1,VD2 VA1,VA2	4.75 4.75	5.0 5.0	5.25 5.25	V V
Operating Ambient Temperature		T_A	0	25	70	°C

Note: 8. $|VD - VA|$ must be less than 0.5 Volts (one diode drop).

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Note: AGND and DGND pins must be on the same ground plane.

Figure 1. Recommended Connection Diagram

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FUNCTIONAL DESCRIPTION

Overview

The CS4215 has two channels of 16-bit analog-to-digital conversion and two channels of 16-bit digital-to-analog conversion. Both the ADCs and the DACs are delta-sigma converters. The ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation. Special features include a separate microphone input with a 20 dB programmable gain block, an optional 8-bit μ-law or A-law encoder/decoder, pins for two crystals to set alternative sample rates, direct headphone drive and mono speaker drive.

Control for the functions available on the CS4215, as well as the audio data, are communicated to the device over a serial interface. Separate pins for input and output data are provided, allowing concurrent writing to and reading from the device. Data must be continually written for proper operation. Multiple CS4215 devices may be attached to the same data lines.

Analog Inputs

Figure 1, the recommended connection diagram, shows examples of the external analog circuitry recommended around the CS4215. An internal multiplexer selects between line level inputs and microphone level inputs.

Input filters using a 150 Ω resistor and a .01 μF NPO capacitor to ground are required to isolate the input op-amps from, and provide a charge reserve for, the switched-capacitor input of the codec. The RC values may be safely changed by a factor of two.

The HPF bit in Control Time Slot 2 provides a high pass filter that will reduce DC offset on the analog inputs. Using the high pass filter will cause slight distortions at very low frequencies.

Unused analog inputs that are not selected have a very high input impedance, so they may be tied to AGND directly. Unused analog inputs that are selected should be tied to AGND through a 0.1uF capacitor. This prevents any DC current flow.

Line Level Inputs

LINL and LINR are the line level input pins. These pins are internally biased to the CMOUT voltage. Figure 2 shows a dual op-amp buffer which combines level shifting with a gain of 0.5 to attenuate the standard line level of 2 V_{rms} to

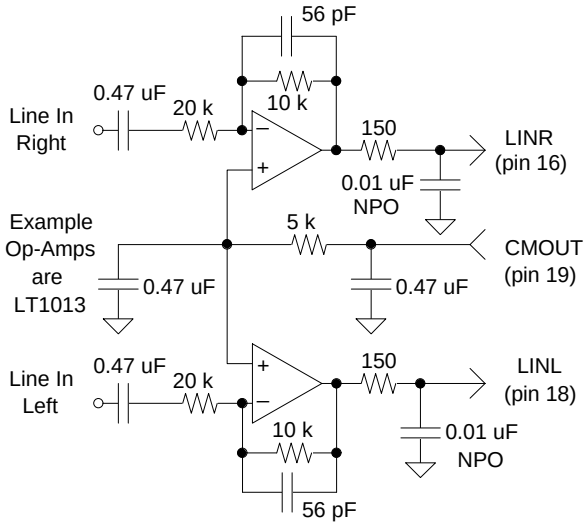


Figure 2. DC Coupled Input.

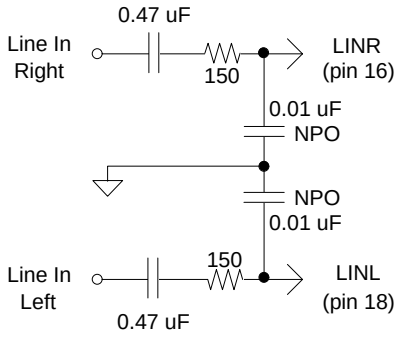


Figure 3. AC Coupled Input.

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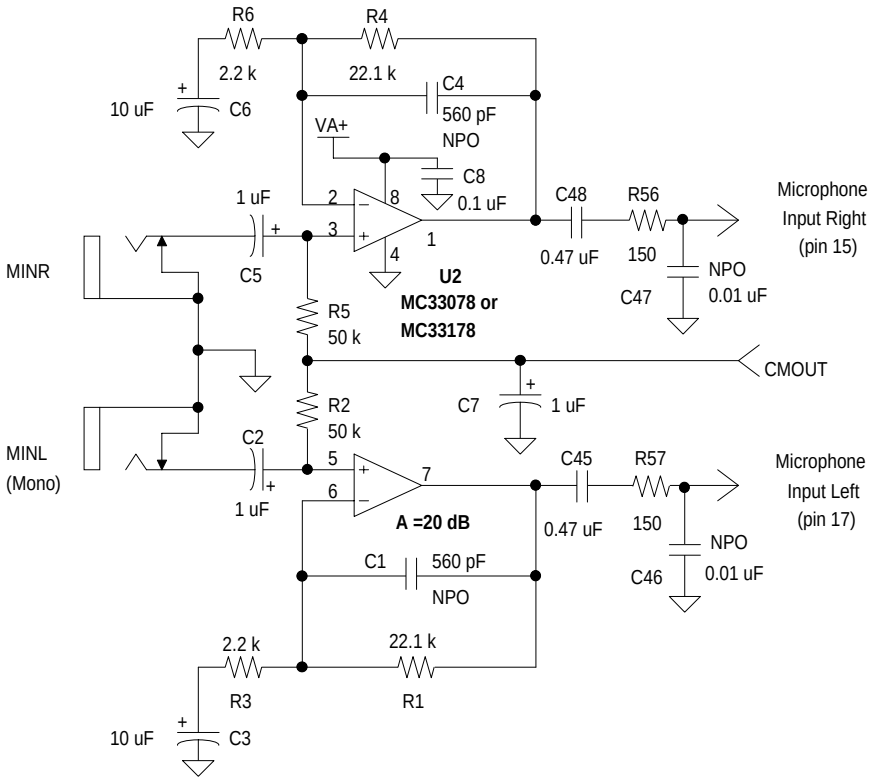


Figure 4. Optional Microphone Input Buffer

1 V_{rms}. The CMOUT reference level is used to level shift the signal. This level shifting allows the line inputs to be DC coupled into the CS4215. Minimum ADC offset results when the line inputs are DC coupled (see Analog Characteristics Table).

Figure 3 shows an AC coupled input circuit for signals centered around 0 Volts. The anti-aliasing RC filter presents a low impedance at high frequencies and should be driven by a low impedance source.

Microphone Level Inputs

Internal amplifiers with a programmable 20 dB gain block are provided for the microphone level inputs, MINR and MINL. Figure 4 shows a single-ended input microphone pre-amplifier stage with a gain of 23 dB. AC coupling is mandatory for these inputs since any DC offset on the input will be amplified by the codec.

The 20 dB gain block may be disabled using the MLB bit in Control Time Slot 1. When disabled, the inputs become line level with full scale inputs of 1 Vrms.

Adjustable Input Gain

The signals from the microphone or the line inputs are routed to a programmable gain circuit which provides up to 22.5 dB of gain in 1.5 dB steps. Level changes only take effect on zero crossings to minimize audible artifacts, often referred to as "zipper noise". The requested level change is forced if no zero crossing is found after 511 frames (10.6 ms at a 48 kHz frame rate). A separate zero crossing detector exists for each channel.

Analog Outputs

The analog outputs of the DACs are routed via an attenuator to a pair of line outputs, a pair of

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headphone outputs and a mono monitor speaker output.

Output Level Attenuator

The DAC outputs are routed through an attenuator, which provides 0 dB to 94.5 dB of attenuation, adjustable in 1.5 dB steps. Level changes are implemented using both analog and digital attenuation techniques. Level changes only take effect on zero crossings to minimize audible artifacts. The requested level change is forced if an analog zero crossing does not occur within 511 frames (10.6 ms at a 48 kHz frame rate). A separate zero crossing detector exists for each channel.

Line Outputs

LOUTR and LOUTL output an analog signal, centered around the CMOUT voltage. The minimum recommended load impedance is 8 kΩ. Figure 1 shows the recommended 1.0 µF DC blocking capacitor with a 40 kΩ resistor to ground. When driving impedances greater than 10 kΩ, this provides a high pass corner of 20 Hz. These outputs may be muted.

Headphone Outputs

HEADR and HEADL output an analog signal, centered around the HEADC voltage. The default headphone output level (OLB = 0) contains an optional 3 dB gain over the line outputs which provides reasonable listening levels, even with small amplitude digital sources. These outputs have increased current drive capability and can drive a load impedance as low as 48 Ω. External 12 Ω series resistors reduce output level variations with different impedance headphones. The common return line from driving headphones should be connected to HEADC, which is biased to the CMOUT voltage. This removes the need for AC coupling, and also controls where the return currents flow. All three headphone output lines are short-circuit protected. These outputs may be muted.

Speaker Output

MOUT1 and MOUT2 differentially drive a small loudspeaker, whose impedance should be greater than 32 Ω. The signal is a summed version of the right and left line output, tapped off prior to the mute function, but after the attenuator. The speaker output may be independently muted. With OLB = 0, the speaker output also contains a 3 dB gain over the line outputs. When OLB = 1, the speaker outputs are driven at the same level as the line outputs.

Some small speakers distort heavily when presented with low frequency energy. A high-pass filter helps eliminate the low frequency energy and can be implemented by AC coupling both speaker terminals with a resistor to ground, on the speaker side of the DC blocking capacitors. The values selected would depend on the speaker chosen, but typical values would be 22 µF for the capacitors, with the positive side connected to the codec, and 50 kΩ resistors. This circuit is contained on the CDB4215 evaluation board as shown in the end of this data sheet.

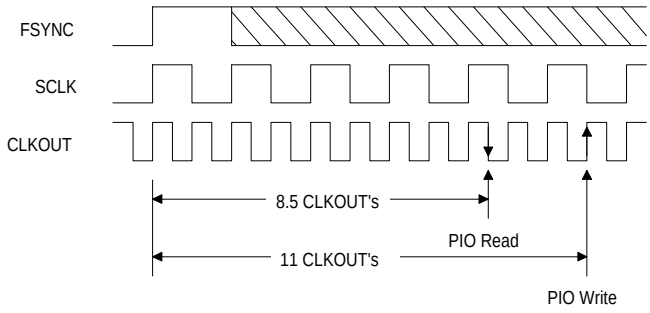
Input Monitor Function

To allow monitoring of the input audio signal, the output of the ADCs can be routed through a monitor path attenuator, then digitally mixed into the input data for the DACs (see the front page block diagram). Changes in the input gain or output level settings directly affect the monitor level. If full scale data from the ADCs is added to full scale digital data from the serial interface, clipping will occur.

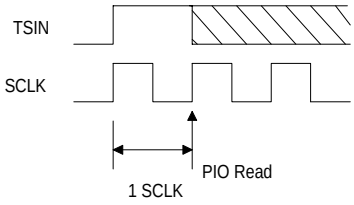
Calibration

Both output offset voltage and input offset error are minimized by an internal calibration cycle. At least one calibration cycle must be invoked

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Data Mode -Read and Write



Control Mode - Read Only

Notes:
1. DATA MODE READ - The data is sent out via SDOUT on the next frame.
2. CONTROL MODE READ - The data is sent out, via SDOUT, the same frame.
3. DATA MODE READ, WRITE - are tied to the rising edge of FSYNC and CLKOUT. They are independent of SCLK.
4. CONTROL MODE READ - The PIO pins are sampled by a rising edge of SCLK.

Figure 5. PIO Pin Timing

after power up. A calibration cycle will occur immediately after leaving the reset state. A calibration cycle will also occur immediately after going from control mode to data mode ($D/\overline{C}$ going high). When powering up the CS4215, or exiting the power down state, a minimum of 50 ms must occur, to allow the voltage reference to settle, before initiating a calibration cycle. This is achieved by holding $\overline{RESET}$ low or staying in control mode for 50 ms after power up or exiting power down mode. The input offset error will be calibrated for whichever input channel is selected (microphone or line, using the IS bit). Therefore, the IS bit should remain steady while the codec is calibrating, although the other bits input to the codec are ignored. Calibration takes 194 FSYNC cycles and SDOUT data bits will be zero during this period. The A/D Invalid bit, ADI (bit 7 in data time slot 6), will be high during calibration and will go low when calibration is finished.

Parallel Input/Output

Two pins are provided for parallel input/output. These pins are open drain outputs and require external pull-up resistors. Writing a zero turns on the output transistor, pulling the pin to ground; writing a one turns off the output transistor, which allows an external resistor to pull the pin high. When used as an input, a one must be written to the pin, thereby allowing an external device to pull it low or leave it high. These pins can be read in control mode and their state is recorded in Control Register 5. These pins can be written to and read back in data mode using Data Register 7. Figure 5 shows the Parallel Input/Output timing.

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Clock Generation

The master clock operating the CS4215 may be generated using the on-chip crystal oscillators, or by using an external clock source. In all data modes SCLK and FSYNC must be synchronous to the selected master clock.

If the master clock source stops, the digital filters will power down after 5 µs to prevent overheating. If FSYNC stops, the digital filters will power down after approximately 1 FSYNC period. The CS4215 will not enter the total power down state.

Internal Clock Generation

Two external crystals may be attached to the XTL1IN, XTL1OUT, XTL2IN and XTL2OUT pins. Use of an external crystal requires additional 40 pF loading capacitors to digital ground (see Figure 1). XTAL1 oscillator is intended for use at 24.576 MHz and XTAL2 oscillator is intended for use at 16.9344 MHz, although other frequencies may be used. The gain of the internal inverter is slightly higher for XTAL1, ensuring proper operation at >24 MHz frequencies. The crystals should be parallel resonant, fundamental mode and designed for 20 pF loading (equivalent to a 40 pF capacitor on each leg). If XTAL1 or XTAL2 is not selected as the master clock, that particular crystal oscillator is powered down to minimize interference. If a crystal is not needed, the XTL-IN pin should be grounded. An example crystal supplier is CAL Crystal, telephone number (714) 991-1580.

FSYNC and SCLK must be synchronous to the master clock. When using the codec in slave mode with one of the crystals as master clock, the controller must derive FSYNC and SCLK from the crystals, i.e. via CLKOUT. Note that CLKOUT will stop in a low condition within two periods after D/$\overline{C}$ goes low.

An internally generated clock which is 256 times the sample rate (FSYNC rate) is output (CLKOUT) for potential use with an external AES/EBU transmitter, or another CS4215. No glitch occurs on CLKOUT when selecting alternate clock sources. CLKOUT will stop in a low condition within two periods after D/$\overline{C}$ goes low, assuming one of the crystal oscillators is selected, or either CLKIN or SCLK is the master clock source and is continuous. The duty cycle of CLKOUT is 50% if the master clock is one of the crystal oscillators and the DFR bits are 0, 1, 2, 6 or 7. If the DFR bits are 3 or 5, the duty cycle is 33% (high time). If the DFR bits are 4 then CLKOUT has the timing shown in Figure 6. If the master clock is SCLK or CLKIN, the duty cycle of CLKOUT will be the same as the master clock source.

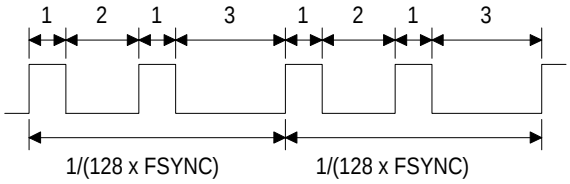


Figure 6. CLKOUT duty cycle using the on-chip crystal oscillator when DFR = 4 (typically FSYNC = 37.8 kHz)

External Clock

An external clock input pin (CLKIN) is provided for potential use with an external AES/EBU receiver, or an already existing system clock. When MCK2 = 0, the input clock must be exactly 256 times the sample rate, and FSYNC and SCLK must be synchronous to CLKIN. When MCK2 = 1 the DFR bits allow various divide ratios off the CLKIN frequency.

Alternatively, an external high frequency clock may be driven into XTL1IN or XTL2IN. The correct clock source must be selected using the MCK bits. Manipulating DFR bits will allow various divide ratios from the clock to be se-

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lected. SCLK and FSYNC must be synchronous to the external clock.

As a third alternative, SCLK may be programmed to be the master clock input. In this case, it must be 256 times Fs.

Serial Interface

The serial interface of the CS4215 transfers digital audio data and control data into and out of the device. Multiple CS4215 devices may share the same data lines. DSP's supported include the Motorola 56001 in network mode and a subset of the 'CHI' bus from AT&T/Intel.

Serial Interface Signals

Figure 7 shows an example of two CS4215 devices connected to a common controller. The Serial Data Out (SDOUT) and Serial Data In (SDIN) lines are time division multiplexed between the CS4215s.

The serial interface clock, SCLK, is used for transmitting and receiving data. SCLK can be generated by one of the CS4215s, or it can be input from an external SCLK source. When generated by an external source, SCLK must be synchronous to the master clock. Data is transmitted on the rising edge of SCLK and is received on the falling edge of SCLK. The SCLK frequency is always equal to the bit rate.

The Frame Synchronizing signal (FSYNC) is used to indicate the start of a frame. It may be output from one of the CS4215s, or it may be generated from an external controller. If FSYNC is generated externally, it must be high for at least 1 SCLK period, and it must fall at least 2 SCLKs before the start of a new frame (see Figure 8). It must also be synchronous to the master clock. The frequency of FSYNC is equal to the system sample rate (see Figure 8). Each CS4215 requires 64 SCLKs to transfer all the data. The SCLK frequency can be set to 64, 128, or 256 bits per frame, thereby allowing for 1, 2 or 4 CS4215s connected to the same bus.

In a typical multi-part scenario, one CS4215 (the master) would generate FSYNC and SCLK, while the other CS4215s (the slaves) would receive FSYNC and SCLK. The CLKOUT of the master would be connected to the CLKIN of each slave device as shown in Figure 7. Then, the master device would be programmed for the desired sample frequency (assuming one of the crystals is selected as the clock source), the number of bits per frame, and for SCLK and FSYNC to be outputs. The slave devices would be programmed to use CLKIN as the clock source, the same number of bits per frame, and for SCLK and FSYNC to be inputs. Since CLKOUT is al-

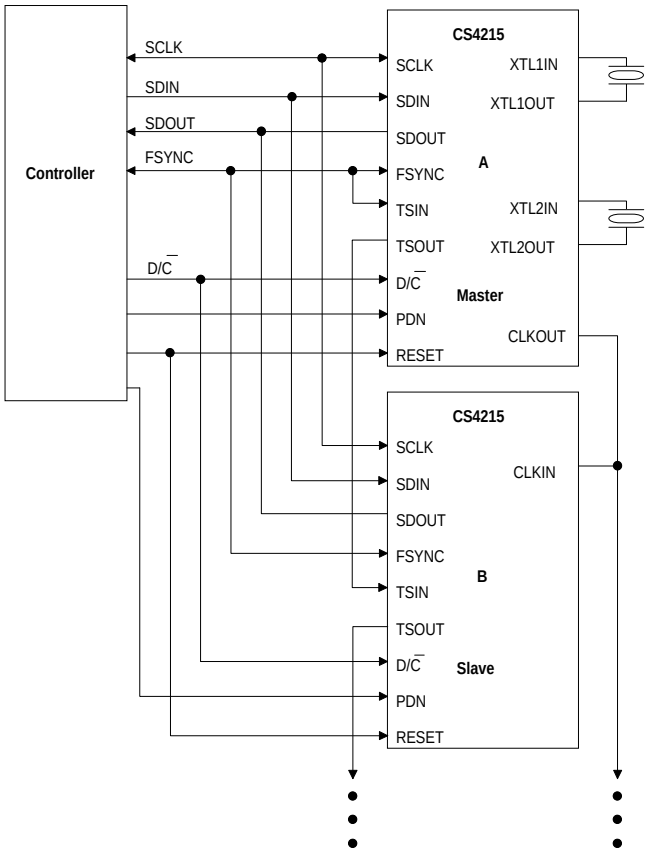


Figure 7. Multiple CS4215's

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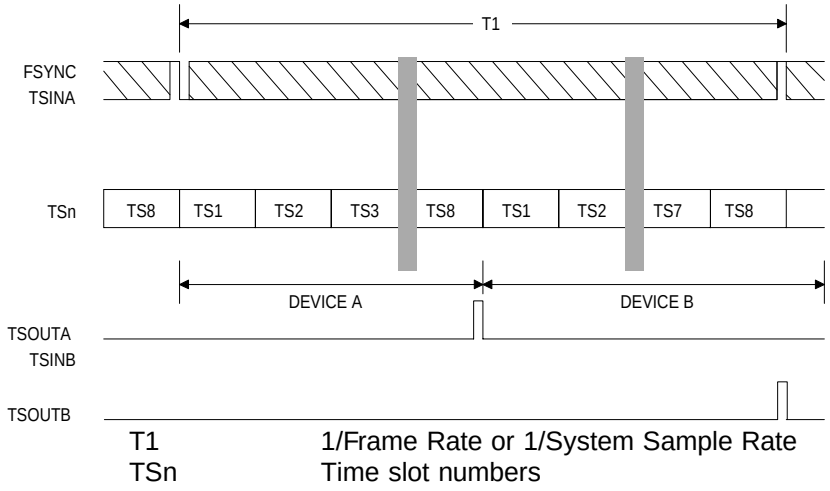


Figure 8. Serial Interface Timing for 2 CS4215's

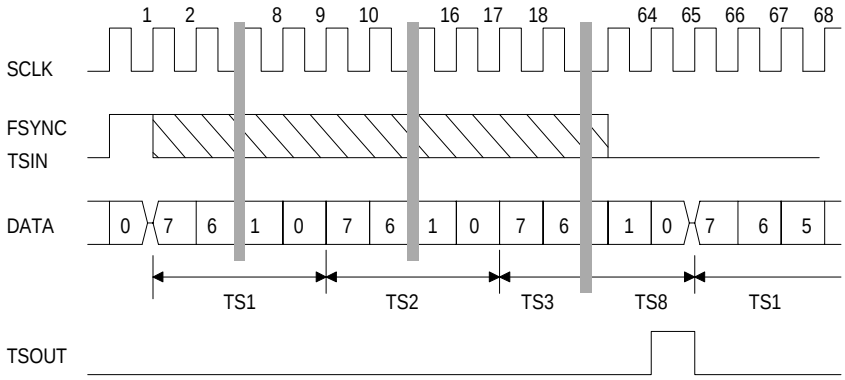


Figure 9. Frame Sync and Bit Offset Timing

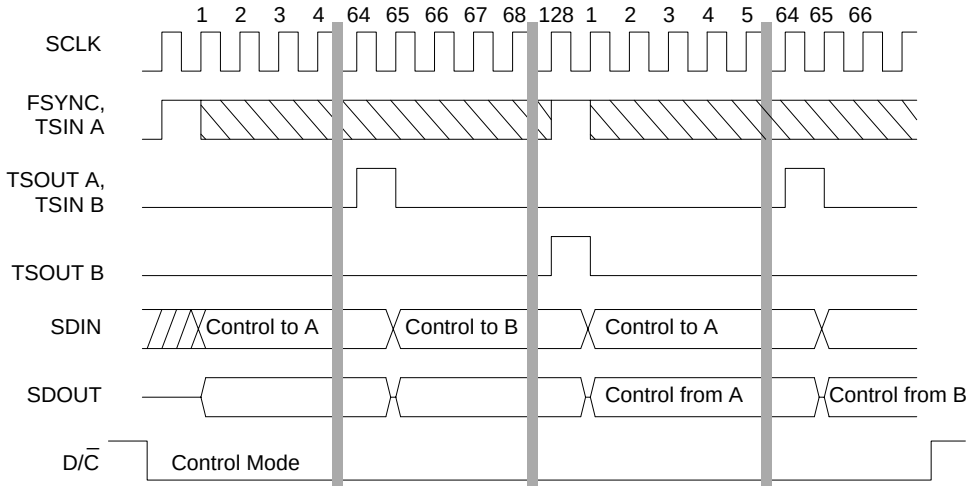


Figure 10. Control Mode Timing for 2 CS4215's

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ways 256 times the sample frequency and scales with the selected sample frequency on the master, the slave devices will automatically scale with changes in the master codec's sample frequency.

CS4215s are time division multiplexed onto the bus using the Time Slot Out (TSOUT) and Time Slot In (TSIN) signals. TSOUT is an output signal that is high for one SCLK bit time, and indicates that the CS4215 is about to release the bus. TSIN is an input signal that informs the CS4215 that the next time slot is available for it to use. The first device in the chain uses FSYNC as its TSIN signal. All subsequent devices use the TSOUT of the previous device as its TSIN input. TSIN must be high for at least 1 SCLK period and fall at least 2 SCLKs before start of a new frame.

Serial Interface Operation

The serial interface format has a variable number of time slots, depending on the number of CS4215s attached to the bus. All time slots have 8 bits. Each CS4215 requires 8 time slots (64 bits) to communicate all data (see Figure 9).

CONTROL MODE

The Control Mode is used to set up the CS4215 for subsequent operation in Data Mode by loading the internal control registers. Control mode is asserted by bringing D/$\overline{C}$ low. If D/$\overline{C}$ is low during power up, then the CS4215 will enter control mode immediately. The SCLK and FSYNC pins are tri-stated, and the CS4215 will receive SCLK and FSYNC from an external source. If the CS4215 is in master mode (SCLK and FSYNC are outputs) and D/$\overline{C}$ is brought low, then SCLK & FSYNC will continue to be driven for a minimum of 4 and a maximum of 12 SCLKs, if the ITS bit = 0. If ITS is 1, SCLK and FSYNC will three-state immediately after D/$\overline{C}$ goes low. If D/$\overline{C}$ is brought low when the codec is programmed as master with ITS=0, the codec will timeout and release FSYNC and SCLK within 100µs. The values in the control registers for control of the serial ports are ignored in control mode. The data received on SDIN is stored into the control registers which have addresses matching their time slots. The data in the registers is transmitted on SDOUT with the time slot equal to the register number (see Figure 10).

The steps involved when going from data mode to control mode and back are shown in the flow chart in Figure 11.

Control Formats

The CS4215 control registers have the functions and time slot assignments shown in Table 1. The register address is the time slot number when D/$\overline{C}$ is 0. Reserved bits should be written as 0 and could be read back as 0 or 1. When comparing data read back, reserved bits should be masked. The SDOUT pin goes into a high-impedance state prior to Time Slot 1 and after Time Slot 8. The data listed below the register is its reset state.

The parallel port register is used to read and write the two open-drain input/output pins. The outputs are all set to 1 on RESET. PIO bits are read only in control mode. Note that, since PIO signals are open drain signals, an external device

Time slot	Description
1	Status
2	Data Format
3	Serial Port Control
4	Test
5	Parallel Port
6	RESERVED
7	Revision
8	RESERVED

Table 1. Control Registers

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may drive them low even when they have been programmed as highs. Therefore, the value read back may differ from the value written. In the data mode, (D/$\overline{C}$=1), this register can be read and written to through the serial port as part of the Input Settings Registers. In control mode, (D/$\overline{C}$=0) these bits can only be read.

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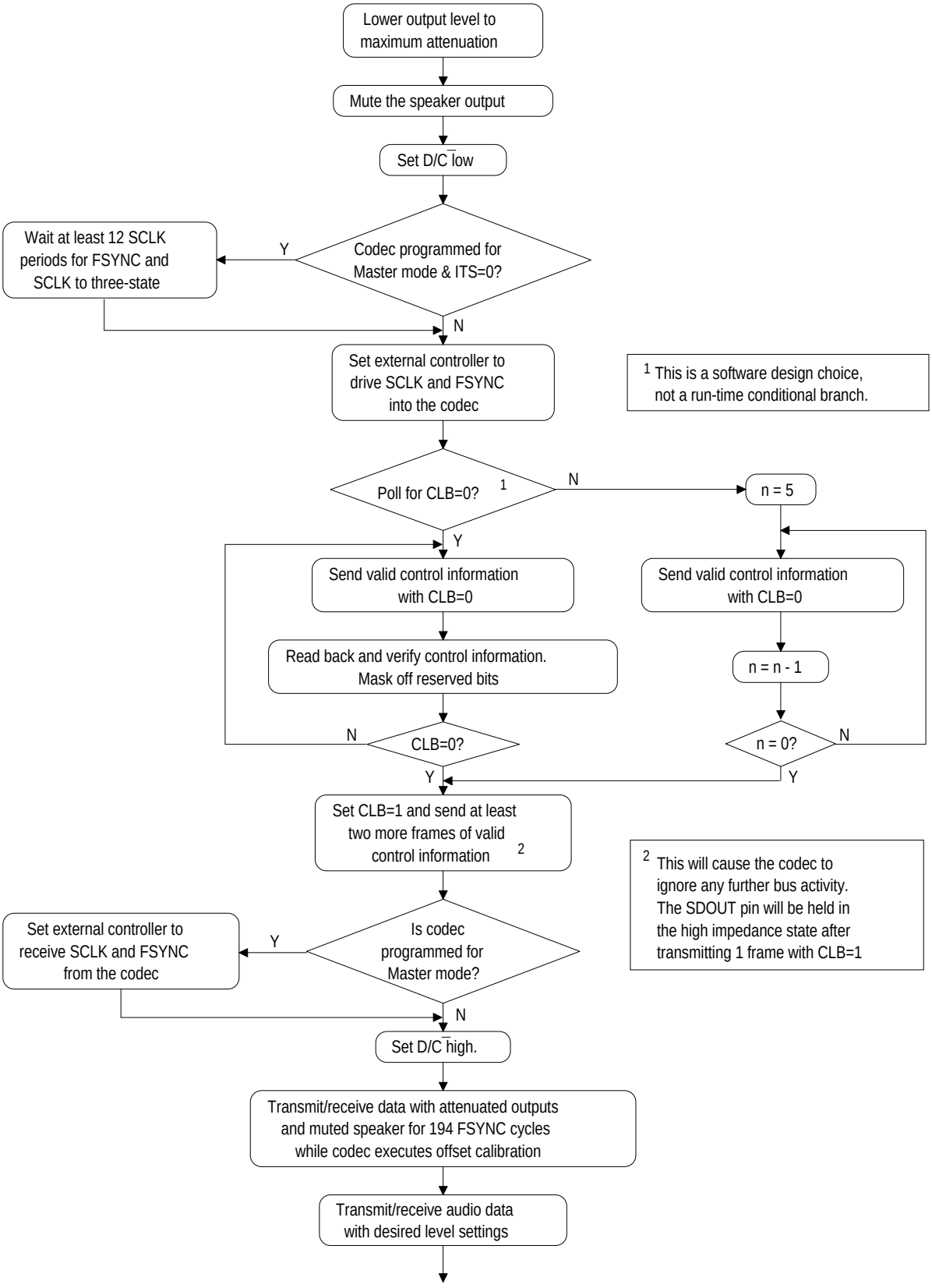


Figure 11. Control Mode Flow Chart

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Control Time Slot 1, Status Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**0**	**0**	**1**	**MLB**	**OLB**	**CLB**	**RSRV**	
Reset (R)	0	0	1	0	0	1	X	X

BIT	NAME	VALUE		FUNCTION
RSRV	Reserved Bits			Must be written as 0.
CLB	Control Latch Bit	1	*R*	Ensures proper transition between control and data mode.
OLB	Output Level Bit	0	*R*	Line full scale outputs are 2.8 Vpp (1Vrms) Headphone full scale output is 4.0 Vpp. Speaker full scale output is 8.0 Vpp.
		1		Line and Headphone full scale outputs are 2.0 Vpp. Speaker full scale output is 4.0 Vpp.
MLB	Microphone Level	0	*R*	20 dB Fixed Gain Enabled Full scale microphone inputs are 0.288 Vpp.
		1		20 dB Fixed Gain Disabled Full scale inputs are 2.88 Vpp.

Control Time Slot 2, Data Format Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**HPF**	**RSRV**	**DFR2**	**DFR1**	**DFR0**	**ST**	**DF1**	**DF0**
Reset (R)	0	X	0	0	0	0	0	1

BIT	NAME	VALUE		FUNCTION
DF1-0	Data Format Selection	0 0	0	16-bit $2^{'s}$-complement linear.
		0 1	1 *R*	8-bit μ–Law.
		1 0	2	8-bit A-Law.
		1 1	3	8-bit unsigned linear.
ST	Stereo Bit	0	*R*	Mono Mode.
		1		Stereo Mode.
DFR2-0	Data Conversion Frequency Selection			

			XTAL1(kHz)	XTAL2 (kHz)
		CLKIN (÷)	24.576 MHz	16.9344 MHz
0 0 0	0 *R*	3072	8	5.5125
0 0 1	1	1536	16	11.025
0 1 0	2	896	27.42857	18.9
0 1 1	3	768	32	22.05
1 0 0	4	448	NA	37.8
1 0 1	5	384	NA	44.1
1 1 0	6	512	48	33.075
1 1 1	7	2560	9.6	6.615

RSRV	Reserved Bit			Must be written as 0
HPF	High Pass Filter	0	*R*	Disabled.
		1		Enabled. A Digital High Pass Filter is used to force the ADC DC offset to zero.

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Control Time Slot 3, Serial Port Control Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**ITS**	**MCK2**	**MCK1**	**MCK0**	**BSEL1**	**BSEL0**	**XCLK**	**XEN**
Reset (R)	0	0	0	0	1	0	0	1

BIT	NAME	VALUE			FUNCTION
XEN	Transmitter Enable	0 1		*R*	Enable the serial data output. Disable (high-impedance state) serial data output.
XCLK	Transmit Clock	0 1		*R*	Receive SCLK and FSYNC from external source SLAVE Mode Generate SCLK and FSYNC MASTER Mode
BSEL1-0	Select Bit Rate	0 0 0 1 1 0 1 1	0 1 2 3	 *R* 	64 bits per frame. 128 bits per frame. 256 bits per frame. Reserved.
MCK2-0	Clock Source Select	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0	0 1 2 3 4	*R* 	SCLK is master clock, 256 bits per frame. BSEL must equal 2, and XCLK must equal 0. XTAL1, 24.576 MHz, is clock source. XTAL2, 16.9344 MHz, is clock source. CLKIN is clock source, and must be 256xFs. CLKIN is clock source, DFR2-0 select sample frequency.
ITS	Immediate Three-State	0 1		*R* 	SCLK and $\overline{\text{FSYNC}}$ three-state up to 12 clocks after D/$\overline{\text{C}}$ goes low. SCLK and $\overline{\text{FSYNC}}$ three-state immediately after D/$\overline{\text{C}}$ goes low.

Control Time Slot 4, Test Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**TEST**						**ENL**	**DAD**
Reset (R)	0	0	0	0	0	0	0	0

BIT	NAME	VALUE		FUNCTION
DAD	Loopback Mode	0 1	*R*	Digital-Digital Loopback. Digital-Analog-Digital Loopback.
ENL	Enable Loopback Testing	0 1	*R*	Disable. Enable.
TEST	Test bits			The TEST bits must be written as zero, otherwise special factory test modes may be invoked.

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Control Time Slot 5, Parallel Port Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**PIO1**	**PIO0**	**RSRV**					
Reset (R)	1	1	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.
PIO1-0	Parallel I/O Bits	1 1 3 *R*	See the Parallel Input/Output Section.

Control Time Slot 6, Reserved Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**RSRV**							
Reset (R)	X	X	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.

Control Time Slot 7, Version Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**RSRV**				**VER3**	**VER2**	**VER1**	**VER0**
Reset (R)	X	X	X	X	0	0	1	0

BIT	NAME	VALUE	FUNCTION
VER3-0	Device Version Number	0 0 0 0 0 0 0 0 1 1 0 0 1 0 2 *R*	"C". See *Appendix A.* "D". See *Appendix A.* "E". This Data Sheet
RSRV	Reserved Bits		Must be written as 0.

Control Time Slot 8, Reserved Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**RSRV**							
Reset (R)	X	X	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.

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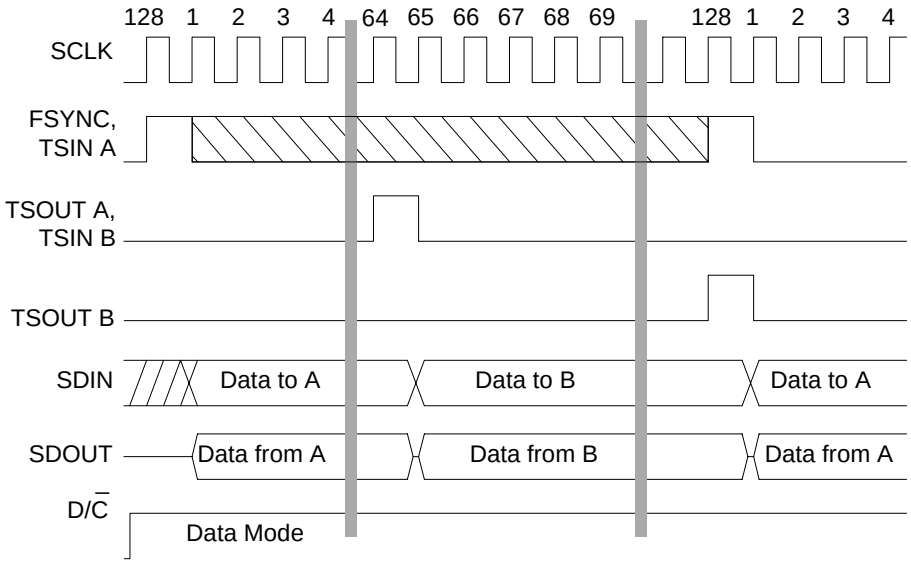


Figure 12. Data Mode Timing for 2 CS4215's

DATA MODE

The data mode is used during conversions to pass digital data between the CS4215 and external devices. The frame sync rate is equal to the value of the conversion frequency set by the DFR2-DFR0 bits of the Data Format register. Each frame has either 64, 128, or 256 bit times depending on the BSEL bits in the Serial Control register. Control of gain, attenuation, input selection and output muting are embedded in the data stream.

Time slot	Description
1	Left Audio MS8 bits
2	Left Audio LS8 bits
3	Right Audio MS8 bits
4	Right Audio LS8 bits
5	Output Setting
6	Output Setting
7	Input Setting
8	Input Setting

Table 2. Data Registers

Data Formats

All time slots contain 8 bits. The MSB of the data is transmitted/received first. The CS4215 data registers have the functions and time slot assignments shown in Table 2. The register address is the time slot number when D/$\overline{C}$ is 1. The SDOUT pin goes into a high-impedance state prior to time slot 1 and after Time Slot 8 (see Figure 12).

The CS4215 supports four audio data formats: 16-bit 2's-complement linear, 8-bit unsigned linear, 8-bit A-Law, and 8-bit µ-Law. Figure 13 illustrates the transfer characteristic for 16-bit and 8-bit linear formats. Note that a digital code

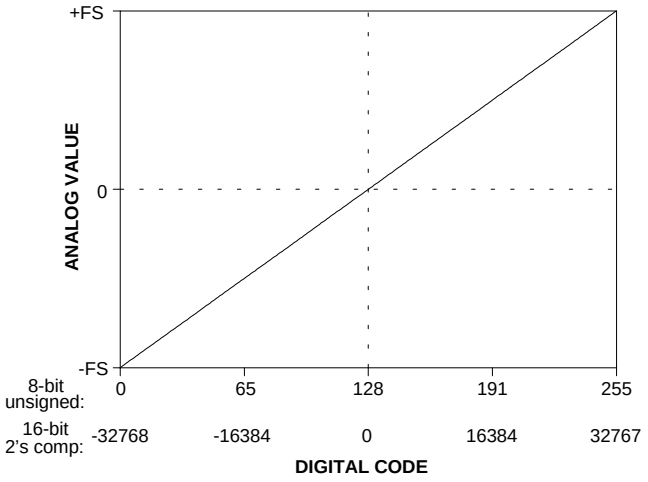


Figure 13. Linear Data Formats

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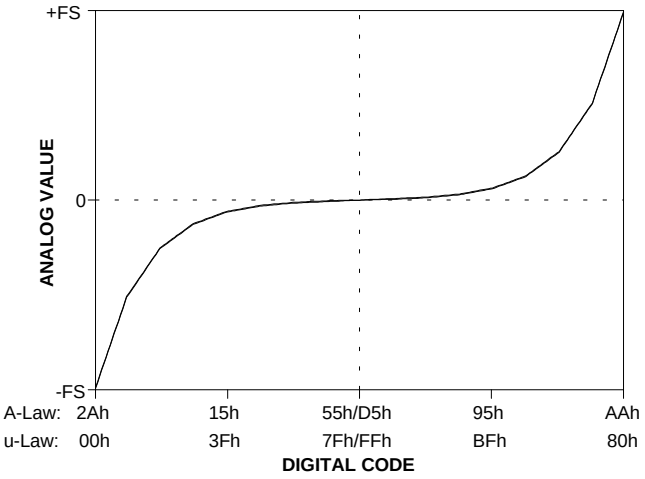


Figure 14. Companded Data Formats

of 128 (80 Hex) is considered analog zero for the 8-bit unsigned format.

A non-linear coding scheme is used for the companded formats as shown in Figure 14. This scheme is compatible with CCITT G.711. Companding uses more precision at lower amplitudes at the expense of less precision at higher amplitudes. µ-Law is equivalent to 13 bits at low signal levels and A-Law is equivalent to 12 bits. This low-level dynamic range is obtained at the expense of large-signal dynamic range which, for both µ-Law and A-Law, is equivalent to 6 bits. The CS4215 internally operates at 16 bits. The companded data is expanded to the upper 13 (12) bits for the DACs and compressed from the upper 13 (12) bits to 8 bits for the ADCs.

Data Time Slot 1&2, Left Channel Audio Data

Time slot 1 and 2 contain audio data for the left channel. In mono modes, only the left channel data is used, however both the right and left output DACs are driven. In 8-bit modes, only time slot 1 is used for the data.

Data Time Slot 3&4, Right Channel Audio Data

Time slot 3 and 4 contains audio data for the right channel. In mono modes, the right ADC outputs zero and the right DAC uses the left digital data. In 8-bit modes, only time slot 3 is used for the data.

Figure 15 summarizes all the time slot bit allocations for the 4 data modes and for control mode.

Reset

$\overline{\text{RESET}}$ going low causes all the internal control registers to be set to the states shown with each register description. $\overline{\text{RESET}}$ must be brought low and high at least once after power up. $\overline{\text{RESET}}$ returning high causes the CS4215 to execute an offset calibration cycle. $\overline{\text{RESET}}$ or D/$\overline{\text{C}}$ returning high should occur at least 50 ms after the power supply has stabilized to allow the voltage reference to settle.

Data Time Slot 5, Output Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**HE**	**LE**	**LO5**	**LO4**	**LO3**	**LO2**	**LO1**	**LO0**
Reset (R)	0	0	1	1	1	1	1	1

BIT	NAME	VALUE		FUNCTION
LO5-0	Left Channel Output Attenuation Setting	1 1 1 1 1 1 63	*R*	1.5dB attenuation steps. LO5 is the MSB. 0 = no attenuation. 111111 = -94.5dB
LE	Line Output Enable	0 1	*R*	Analog line outputs off (muted). Analog line outputs on.
HE	Headphone Output Enable	0 1	*R*	Headphone output off (muted). Headphone output on.

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Data Time Slot 6, Output Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**ADI**	**SE**	**RO5**	**RO4**	**RO3**	**RO2**	**RO1**	**RO0**
Reset (R)	1	0	1	1	1	1	1	1

BIT	NAME	VALUE	FUNCTION
RO5-0	Right Channel Output Attenuation Setting	1 1 1 1 1 1 63 *R*	1.5dB attenuation steps. RO5 is the MSB. 0 = no attenuation. 111111 = -94.5dB Not used in mono modes.
SE	Speaker Enable	0 *R* 1	Speaker off (muted). Speaker on.
ADI	A/D Data Invalid	0 1 *R*	A/D data valid. A/D data invalid. Busy in calibration.

Data Time Slot 7, Input Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**PIO1**	**PIO0**	**OVR**	**IS**	**LG3**	**LG2**	**LG1**	**LG0**
Reset (R)	1	1	0	0	0	0	0	0

BIT	NAME	VALUE	FUNCTION
LG3-0	Left Channel Input Gain Setting	0 0 0 0 *R*	1.5dB gain steps. LG3 is the MSB. 0 = no gain, 1111 = 22.5dB gain.
IS	Input Select	0 *R* 1	Line level inputs (LINL, LINR). Microphone level inputs (MINL, MINR).
OVR	Overrange	0 *R*	When read as 1, this bit indicates that an input over-range condition has occurred. The bit remains set until cleared by writing 0 into the register. Writing a 1 enables the overrange detection. The bit will remain 0 until an over-range occurs. Serial port clear has priority over internal settings.
PIO1-0	Parallel I/O	1 1 3 *R*	Parallel input/output bits.

Data Time Slot 8, Input Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**MA3**	**MA2**	**MA1**	**MA0**	**RG3**	**RG2**	**RG1**	**RG0**
Reset (R)	1	1	1	1	0	0	0	0

BIT	NAME	VALUE	FUNCTION
RG3-0	Right Channel Input Gain Setting	0 0 0 0 *R*	1.5dB gain steps. RG3 is the MSB. 0 = no gain, 1111 = 22.5dB gain.
MA3-0	Monitor Path Attenuation	1 1 1 1 15 *R*	6dB attenuation steps. MA3 is the MSB. 0 = no attenuation, 1111 = mute.

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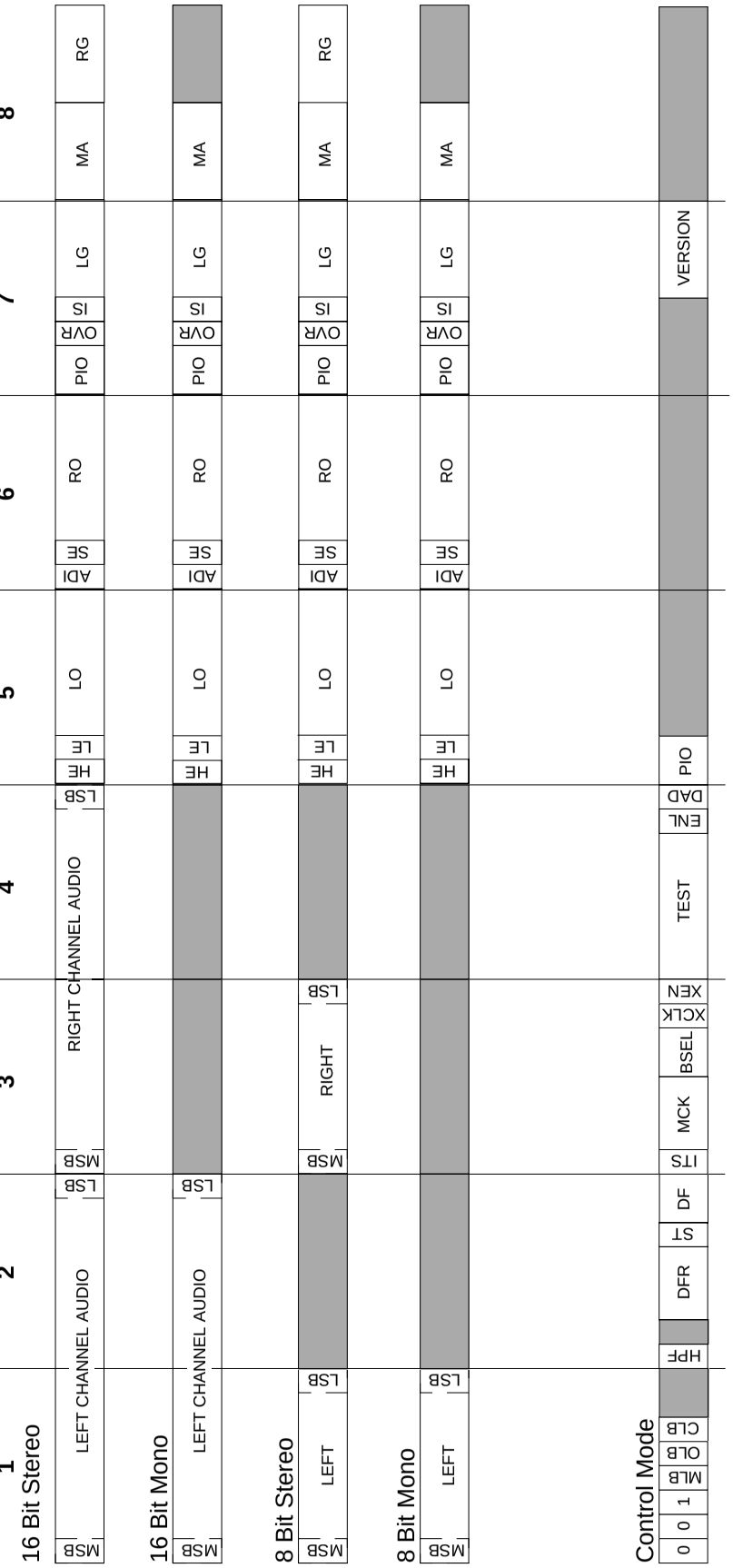


Figure 15. Time Slot/Register Overview

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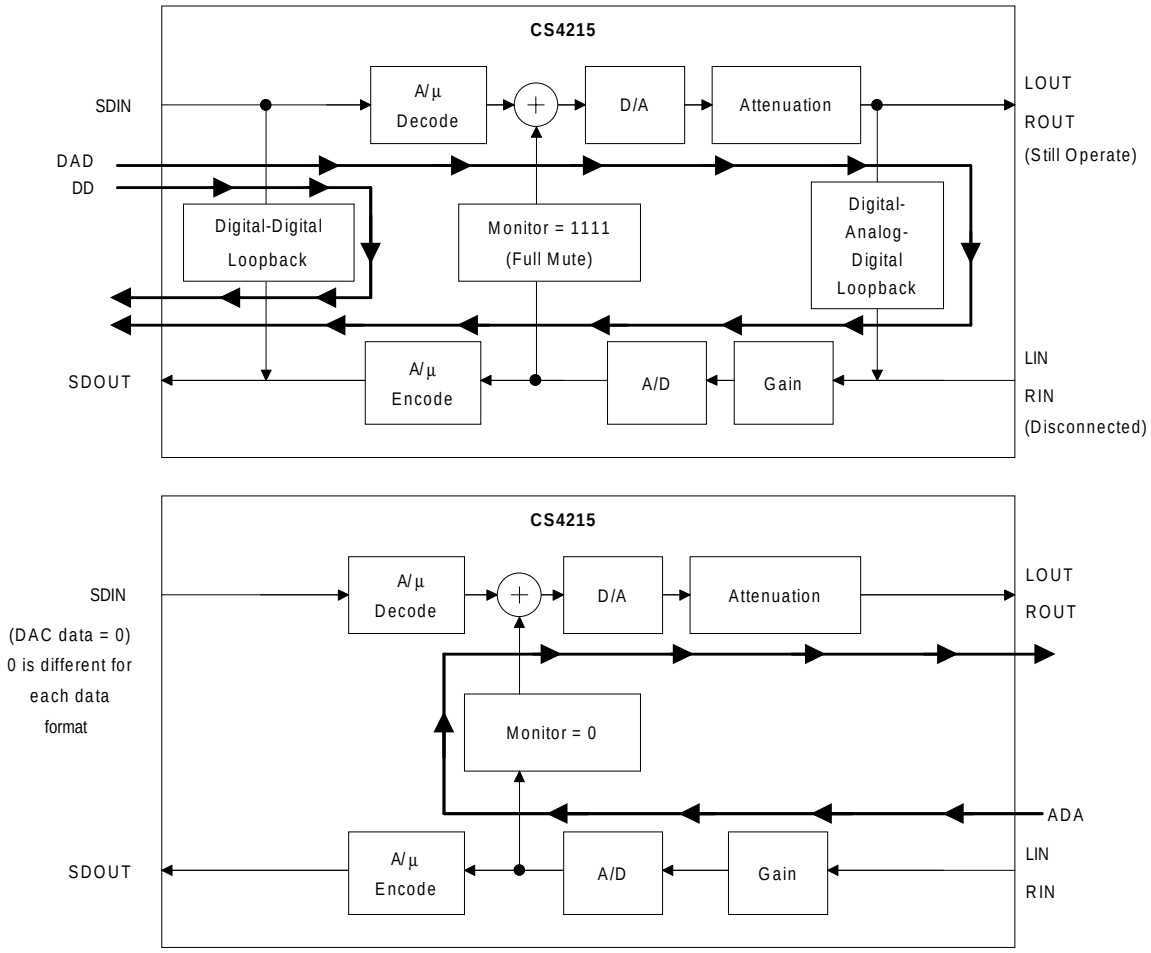


Figure 16. DD, DAD & ADA Loopback Paths

Power Down Mode

Bringing the PDN pin high puts the CS4215 into the power down mode. In this mode HEADC and CMOUT will not supply current. Power down will change all the control registers to the reset state shown under each Control Time Slot register. In the power down mode, the TSOUT pin will follow the TSIN state with less than 10 ns delay.

After returning to normal operation from power down, an offset calibration cycle must be executed. Either bringing $\overline{\text{RESET}}$ low then high, or updating the control registers, will cause an offset calibration cycle. In either case, a delay of 50 ms must occur after PDN goes low before executing the offset calibration. This allows the internal voltage reference time to settle.

LOOPBACK TEST MODES

The CS4215 contains three loopback modes that may be used to test the codec. Two of the loopback test modes are designed to allow the host to perform a self-test on the CS4215. The third mode allows laboratory testing using external equipment.

Host Self-Test Loopback Modes

Since the CS4215 is a mixed-signal device, it is equipped with an internal register that will enable the host to perform a two-tiered test on power-up or as needed. The loopback test is enabled by setting the Enable Loopback bit, ENL, in control register 4. The first tier of loopback is a digital-digital loopback, DD, which is selected by clearing the DAD bit in control register 4 (see

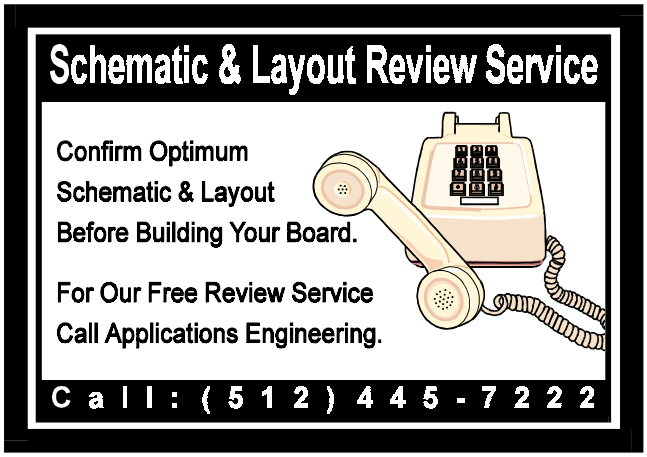
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Figure 16). DD loopback checks the interface between the host and the CS4215 by taking the data on SDIN and looping it back onto SDOUT, with the data on SDOUT being one frame delayed from the data on SDIN. The host can verify that the data received is exactly the same as the data sent, thereby indicating the interface between the two devices and the digital interface on the CS4215 are operating properly. The output DAC's are functional in DD loopback. Now that the interface has been verified, the rest of the CS4215 can be tested using the second tier of loopback.

The second tier of loopback is a digital-analog-digital loopback, DAD, which is selected by setting the DAD bit in control register 4. DAD loopback checks the analog section of the CS4215 by connecting the right and left analog outputs, after the output attenuator, to the analog inputs of the gain stage. This allows testing of most of the CS4215 from the host by sending a known digital signal to the DACs and monitoring the digital signal from the ADCs. During DAD loopback, the monitor attenuator must be set at maximum (full mute), and the analog outputs may be individually muted. The analog inputs are disconnected internally. The flow of test data for both DD and DAD loopback modes is illustrated in the top portion of Figure 16.

Analog-to-Analog Loopback Mode

A third loopback mode is achieved by setting the monitor attenuator to zero attenuation and sending the DACs digital zero via SDIN. This loopback is termed analog-digital-analog, ADA, since the selected analog input will now appear on the enabled analog outputs. Since this test is controlled by external stimulus and the host is not involved (except to send the DACs zeros), it is generally considered a laboratory test as opposed to a self test. The bottom portion of Figure 16 illustrates the ADA signal flow through the CS4215. Note that this test requires the host send analog zeros to the DAC. Each data format has a different code for zero. See Figures 13 and 14.



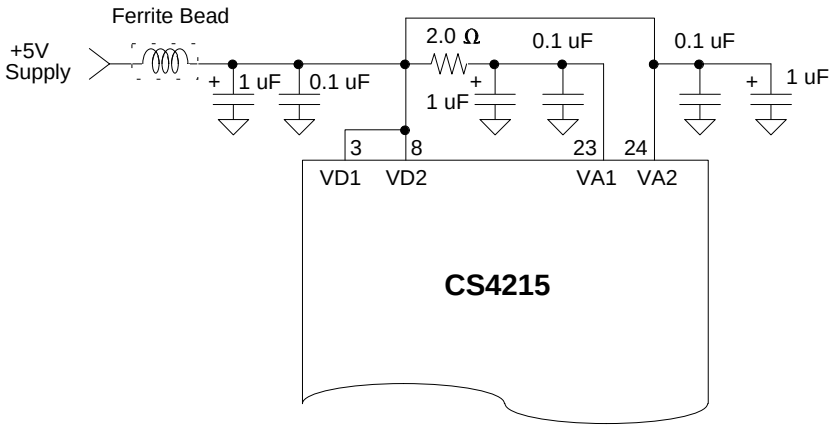


Figure 17. Optional Power Supply Arrangement

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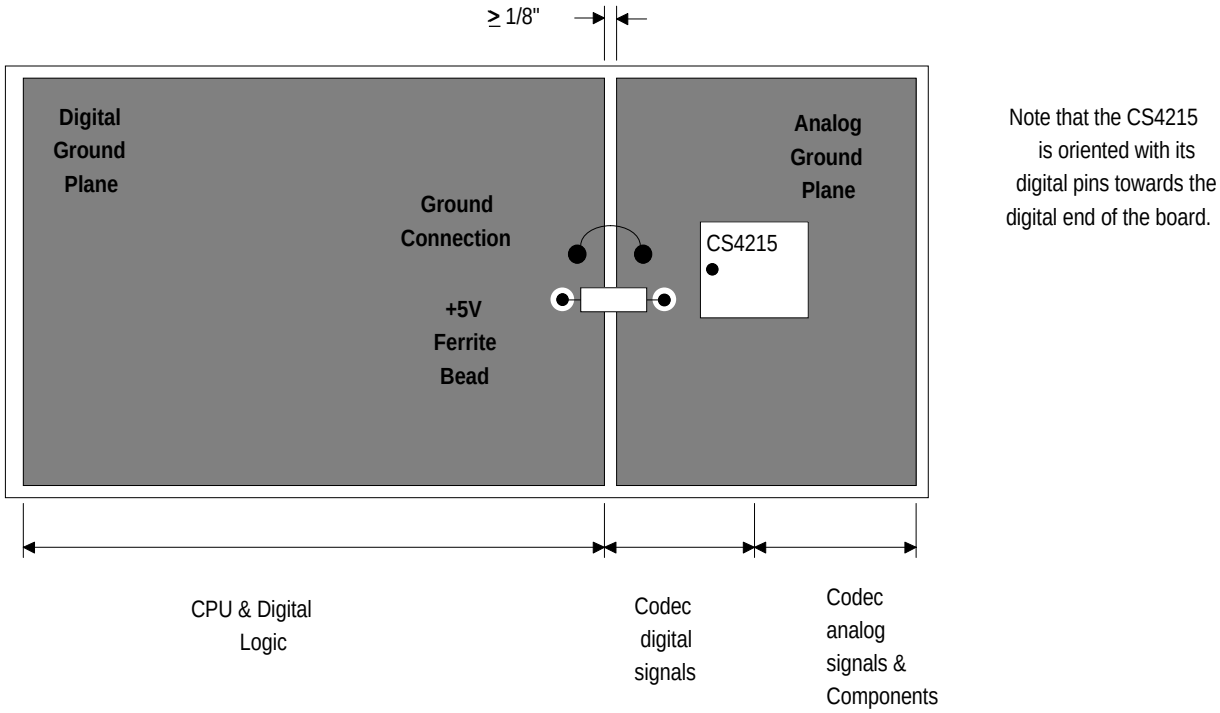


Figure 18. Suggested Layout Guideline

POWER SUPPLY AND GROUNDING

When using separate supplies, the digital power should be connected to the CS4215 via a ferrite bead, positioned closer than 1" to the device (see Figure 1). The codec VA1, VA2 pins should be derived from the cleanest power source available. If only one supply is available, use the suggested arrangement in Figure 17. VA1 supplies analog power to the ADCs and DACs while VA2 supplies power to the output power drivers (headphones and speaker). The large currents necessary for VA2 are not flowing through the 2.0 Ω resistor, and therefore do not corrupt the VA1 converter supply.

The CS4215 along with associated analog circuitry, should be positioned near to the edge of the circuit board, and have its own, separate, ground plane. On the CS4215, the analog and digital grounds are internally connected; therefore, the four ground pins must be externally connected with zero impedance between ground pins. The best solution is to place the entire chip on a solid ground plane as shown in Figure 18. Preferably, it should also have its own power plane. A single connection between the CS4215 ground and the board ground should be positioned as shown in Figure 18.

Figure 19 illustrates the optimum ground and decoupling layout for the CS4215 assuming a surface-mount socket and leaded decoupling capacitors. Surface-mount sockets are useful since the pad locations are exactly the same as the actual chip; therefore, given that space for the socket is left on the board, the socket can be optional for production. Figure 19 depicts the top layer containing signal traces and assumes the bottom or inter-layer contains a solid analog ground plane. The important points with regards to this diagram are that the ground plane is SOLID under the codec and connects all codec ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors are placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor is

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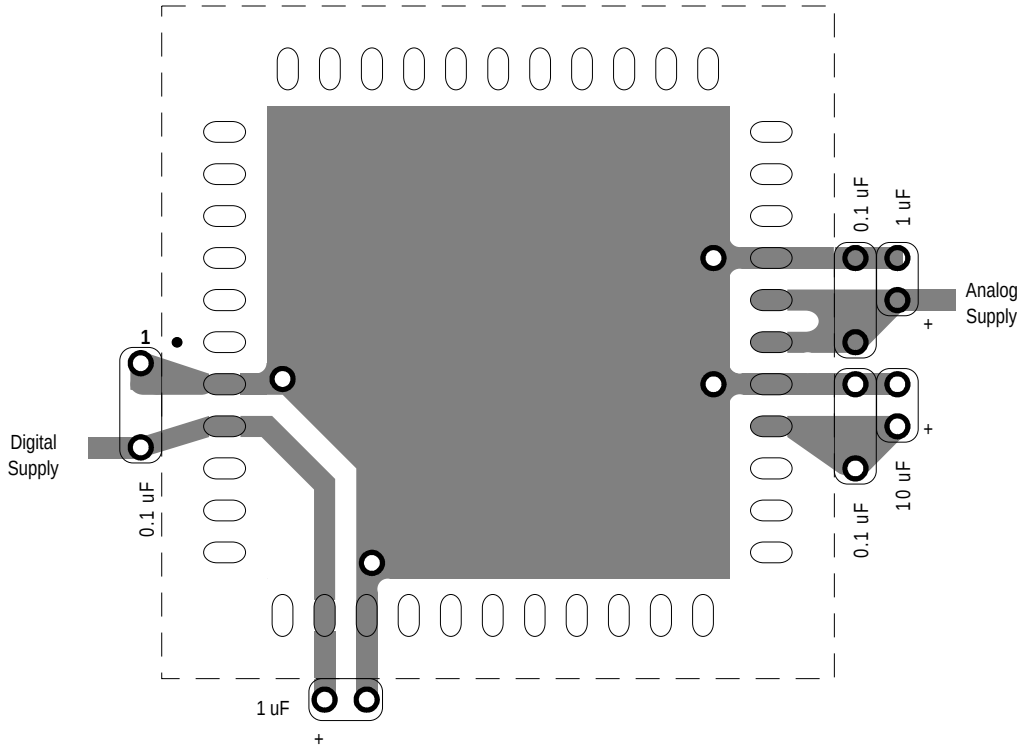


Figure 19. CS4215 Decoupling Layout Guideline

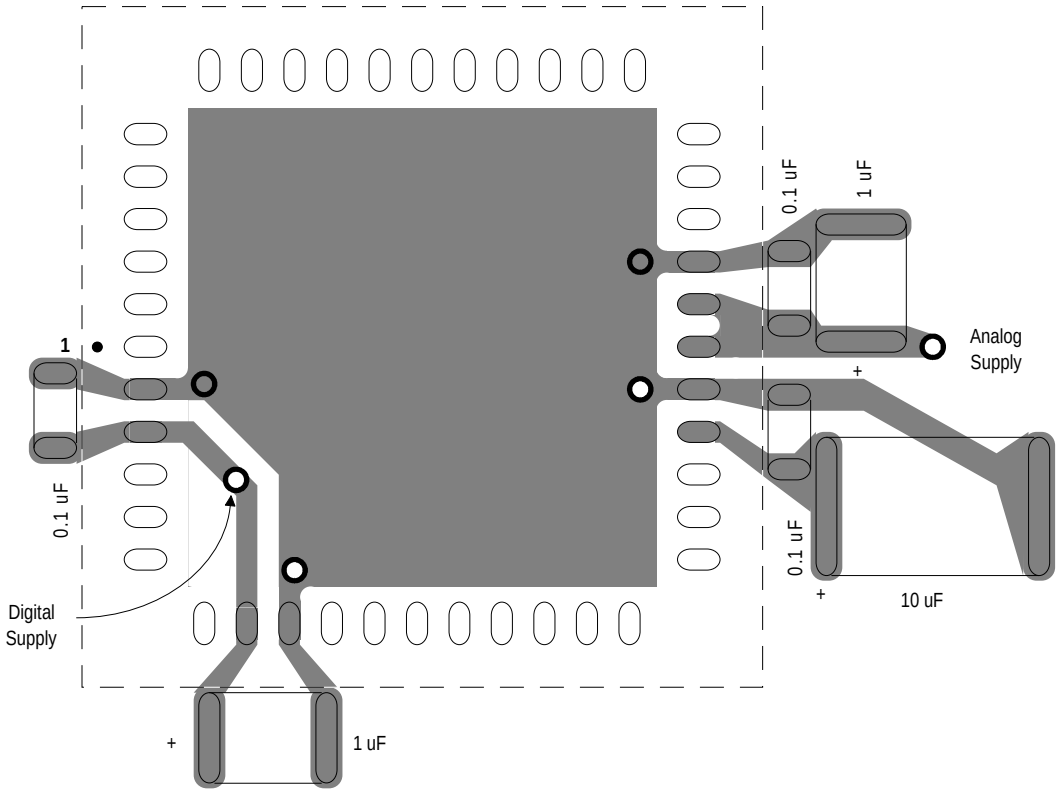


Figure 20. CS4215 Surface Mount Decoupling Layout

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placed closest to the codec. Vias are placed near the AGND and DGND pins, under the IC, and should be attached to the solid analog ground plane on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces bringing the power to the codec should be wide thereby keeping the impedance low.

Although not shown in the figures, the trace layers (top layer in the figures) should have ground plane fill in-between the traces to minimize coupling into the analog section. See the CDB4215 evaluation board data sheet for an example layout.

If using all surface-mount components, the decoupling capacitors should still be placed on the layer with the codec and in the positions shown in Figure 20. The vias shown are assumed to attach to the appropriate power and analog ground layers. Traces bringing power to the codec should be as wide as possible to keep the impedance low. For the same reason, vias should be large for power and ground runs.

If using through-hole sockets, effort should be made to find a socket with the minimum height which will minimize the socket impedance. When using a through-hole socket, the vias under the codec in Figure 19 are not needed since the pins serve the same function.

ADC and DAC Filter Response Plots

Figures 21 through 27 show the overall frequency response, passband ripple and transition band for the CS4215 ADCs and DACs. Figure 27 shows the DACs' deviation from linear phase. Fs is the selected sample frequency. Since the sample frequency is programmable, the filters will adjust to the selected sample frequency. Fs is also the FSYNC frequency.

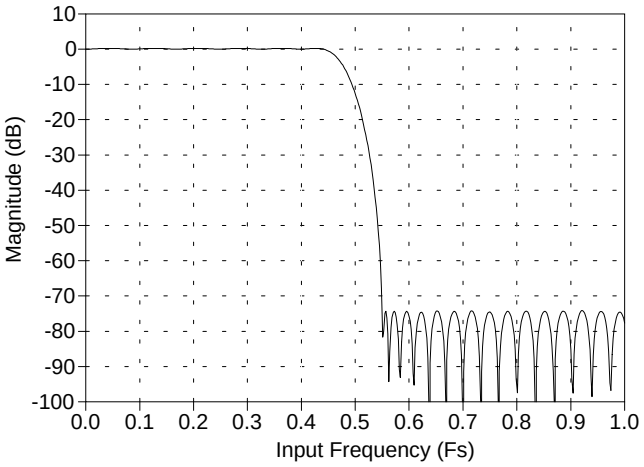


Figure 21. ADC Frequency Response

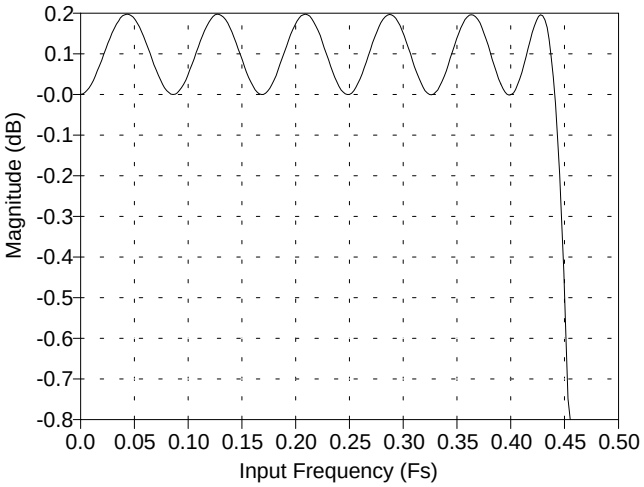


Figure 22. ADC Passband Ripple

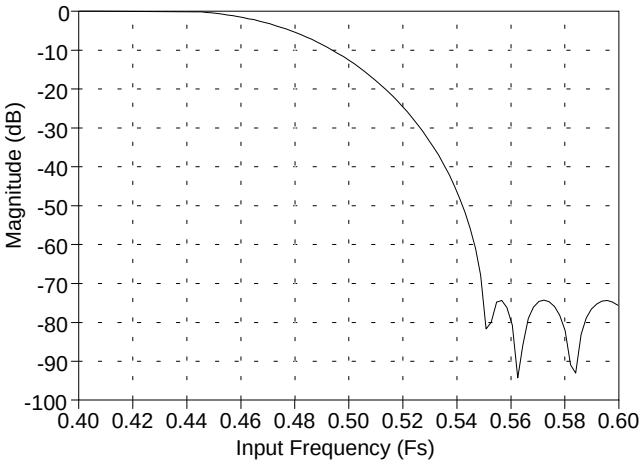


Figure 23. ADC Transition Band

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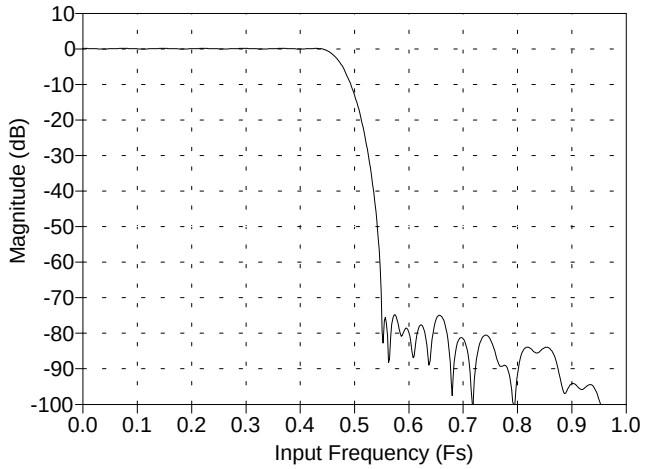


Figure 24. DAC Frequency Response

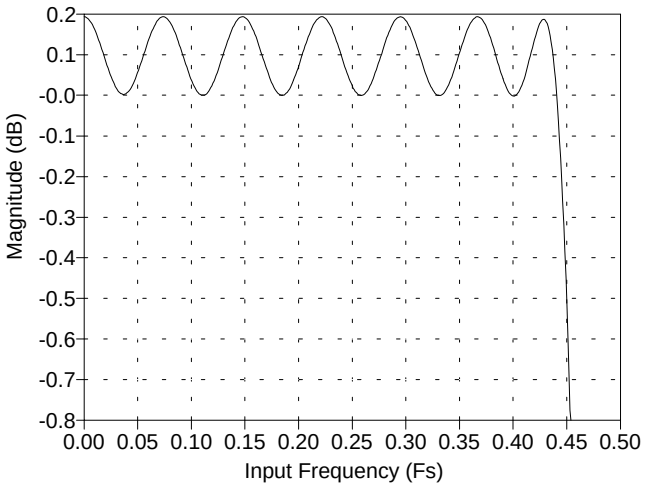


Figure 25. DAC Passband Ripple

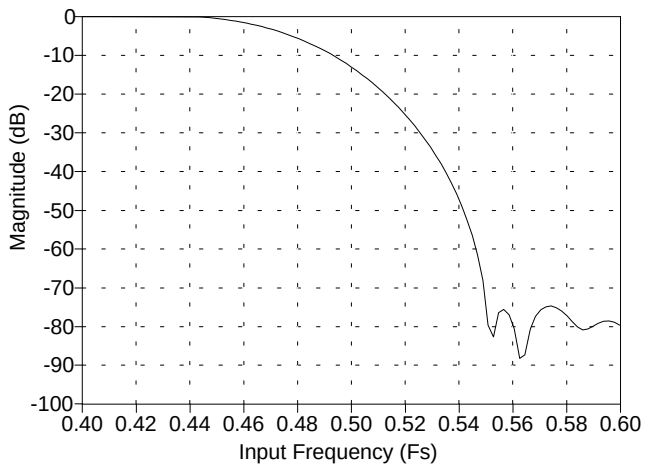


Figure 26. DAC Transition Band

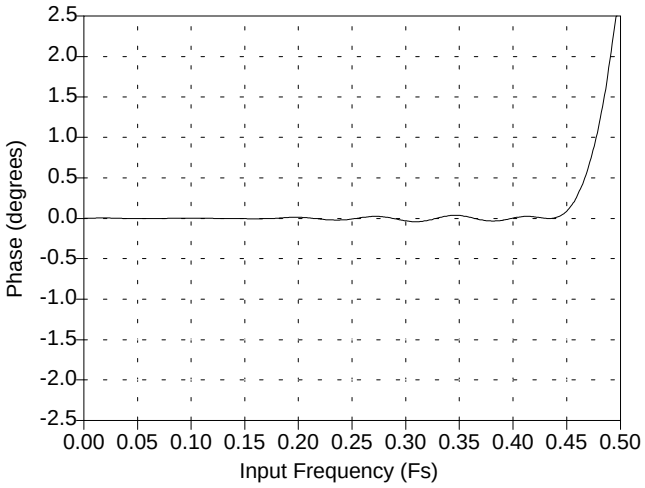
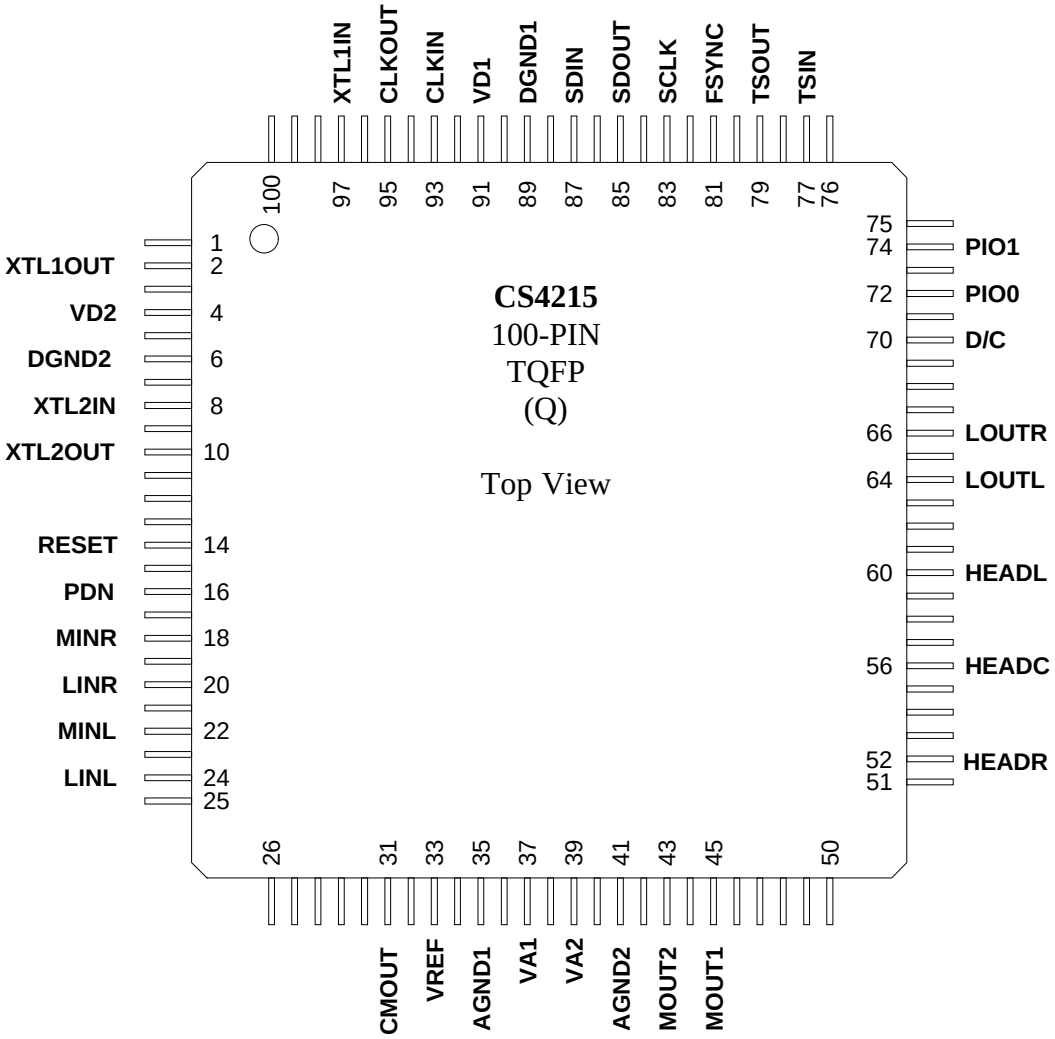


Figure 27. DAC Deviation from Linear Phase

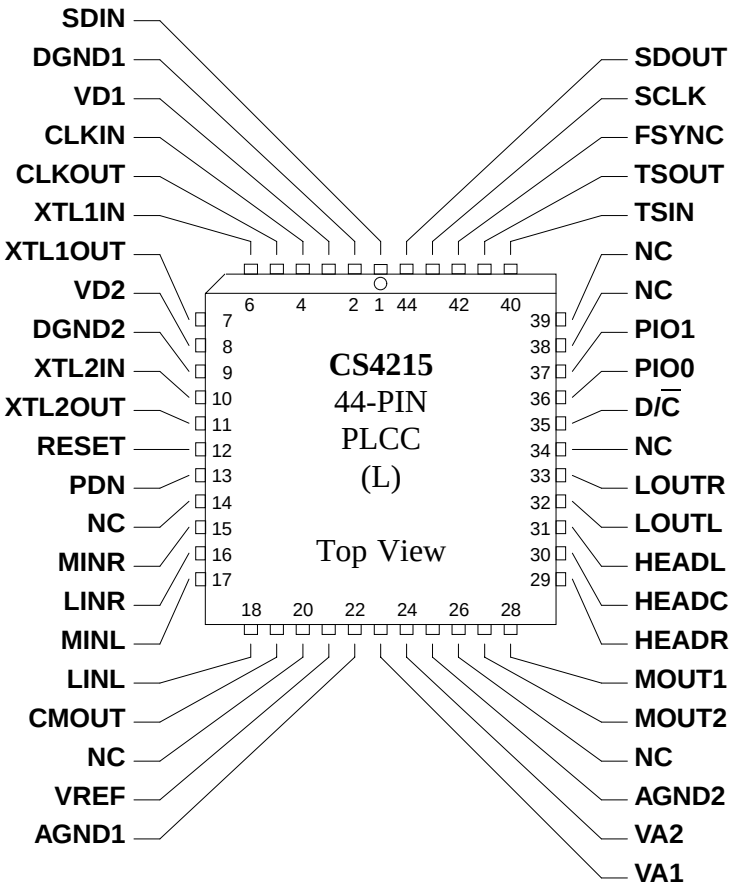
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PIN DESCRIPTIONS



Note: All unlabeled pins are No Connects

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Power Supply

VA1, VA2 - Analog Power Input, Pins 23(L), 24(L), 37(Q), 39 (Q)

+5 V analog supply.

AGND1, AGND2 - Analog Ground, Pins 22(L), 25(L), 35(Q), 41(Q)

Analog ground. Must be connected to DGND1, DGND2 with zero impedance.

VD1, VD2 - Digital Power Input, Pins 3(L), 8(L), 91(Q), 4(Q)

+ 5 V digital supply.

DGND1, DGND2 - Digital Ground, Pin 2(L), 9(L), 89(Q), 6(Q)

Digital ground. Must be connected to AGND1, AGND2 with zero impedance.

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Analog Inputs

LINL, LINR - Left and Right Channel Line Level Inputs, Pins 18(L), 16(L), 24(Q), 20(Q)

Line level input connections for the right and left channels.

MINL, MINR - Left and Right Channel Microphone Inputs, Pins 17(L), 15(L), 22(Q), 18(Q)

Microphone level input connections for the right and left channels.

Analog Outputs

LOUTR, LOUTL - Line Level Outputs, Pins 33(L), 32(L), 66(Q), 64(Q)

One pair of line level outputs are provided. The output level for right and left outputs can be independently varied. These outputs can be muted.

HEADR, HEADL - Headphone Outputs, Pins 29(L), 31(L), 52(Q), 60(Q)

HEADR and HEADL are intended to drive a pair of headphones. Additional current drive, along with an optional +3 dB of gain, ensures reasonable listening levels. These outputs can be muted.

HEADC - Common Return for Headphone Outputs, Pin 30(L), 56(Q)

HEADC is the return path for large currents when driving headphones from the HEADR and HEADL outputs. This pin is nominally at 2.1 V.

CMOUT - Common Mode Output, Pin 19(L), 31(Q)

Common mode voltage output. This signal may be used for level shifting the analog inputs. The load on CMOUT must be DC only, with an impedance of not less than 10kΩ. CMOUT should be bypassed with a 0.47 µF to AGND. CMOUT is nominally at +2.1V.

MOUT1, MOUT2 - Mono Speaker Outputs, Pins 28(L), 27(L), 45(Q), 43(Q)

Mono external loudspeaker differential output connections. The loudspeaker output is a mix of left and right line outputs. Independent muting of the speaker is provided. MOUT1 and MOUT2 output voltage is nominally at 2.1 V with no signal.

VREF - Voltage Reference Output, Pin 21(L), 33(Q)

The on-chip generated ADC/DAC reference voltage is brought out to this pin for decoupling purposes. This output must be bypassed with a 10 µF capacitor in parallel with a 0.1 µF capacitor to the adjacent AGND1 pin. No other external load may be connected to this output.

Digital Interface Signals

SDIN - Serial Data Input, Pin 1(L), 87(Q)

Audio data for the DACs and control information for all functions is presented to the CS4215 on this pin.

SDOUT - Serial Data Output, Pin 44(L), 85(Q)

Audio data from the ADCs and status information concerning all functions is written out by the CS4215 onto this pin.

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SCLK - Serial Port Clock, Pin 43(L), 83(Q)

SCLK rising causes the data on SDOUT to be updated. SCLK falling latches the data on SDIN into the CS4215. The SCLK signal can be generated off-chip, and input into the CS4215. Alternatively, the CS4215 can generate and output SCLK in data mode.

FSYNC - Frame Sync Signal, Pin 42(L), 81(Q)

The Frame Synchronizing Signal is sampled by SCLK, with a rising edge indicating a new frame is about to start. FSYNC frequency is always the system sample rate. Each frame may have 64, 128 or 256 data bits, allowing for 1, 2 or 4 CS4215s connected to the same bus. FSYNC may be input to the CS4215, or may be generated and output by the CS4215 in data mode. When FSYNC is an input, it must be high for at least 1 SCLK period. FSYNC can stay high for the rest of the frame, but must return low at least 2 SCLKs before the next frame starts.

TSIN - Time Slot Input, Pin 40(L), 77(Q)

TSIN high for at least 1 SCLK cycle indicates to the CS4215 that the next time slot is allocated for it to use. TSIN is normally connected to the TSOUT pin of the previous device in the chain. TSIN should be connected to FSYNC for the 1st (or only) CS4215 in the chain.

TSOUT - Time Slot Output, Pin 41(L), 79(Q)

TSOUT goes high for 1 SCLK cycle, indicating that the CS4215 is about to release the data bus. Normally connected to the TSIN pin on the next device in the chain.

D/$\overline{C}$ - Data/Control Select Input, Pin 35(L), 70(Q)

When D/$\overline{C}$ is low, the information on SDIN and SDOUT is control information. When D/$\overline{C}$ is high, the information on SDIN and SDOUT is data information.

PDN - Power Down Input, Pin 13(L), 16(Q)

When high, the PDN pin puts the CS4215 into the power down mode. In this mode HEADC and CMOUT will not supply current. Power down causes all the control registers to change to the default reset state. In the power down mode, the TSOUT pin remains active, and follows TSIN delayed by less than 10 ns.

$\overline{\text{RESET}}$ - Active Low Reset Input, Pin 12(L), 14(Q)

Upon reset, the values of the control information (when D/$\overline{C}$ = 0) will be initialized to the values given in the Reset Description section of this data sheet.

Clock and Crystal Pins

XTL1IN, XTL1OUT, XTL2IN, XTL2OUT - Crystals 1 and 2 Inputs and Outputs, Pins 6(L), 7(L), 10(L), 11(L), 97(Q), 2(Q), 8(Q), 10(Q)

Input and output connections for crystals 1 and 2. One of these oscillators may provide the master clock to run the CS4215.

CLKIN - External Clock Input, Pin 4(L), 93(Q)

External clock input optionally used to clock the CS4215. The CLKIN frequency must be 256 times the maximum sample rate (FSYNC frequency).

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CLKOUT - Master Clock Output, Pin 5(L), 95(Q)

Master clock output, whose frequency is always 256 times the system sample rate (FSYNC frequency). CLKOUT is active only in data mode and is low during control mode.

Miscellaneous Pins

PIO0, PIO1 - Parallel Input/Output, Pins 36(L), 37(L), 72(Q), 74(Q)

These pins are provided as general purpose digital parallel input/output and have open drain outputs. An external pull-up resistor is required. They can be read in control mode, and read and written to in data mode.

Note: All unlabeled pins are No Connects which should be left floating.

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PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth. Units in LSB.

Total Dynamic Range

The rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (ie. attenuation bits for the DACs at full attenuation.) Units in dB.

Instantaneous Dynamic Range

The dynamic range available at any instant in time. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces to harmonic distortion components of the noise to insignificance. Units in dB.

Total Harmonic Distortion

THD is the ratio of the rms value of a signal's first five harmonic components to the rms value of the signals fundamental component. THD is calculated for the ADCs using an input signal which is 3dB below typical full-scale, and is referenced to typical full-scale. A digital full-scale output is used to calculate THD for the DACs.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Frequency Response

Worst case variation in output signal level versus frequency over 10 Hz to 20 kHz. Units in dB.

Step Size

Typical delta between two adjacent gain or attenuation values. Units in dB.

Absolute Step Error

The deviation of a gain or attenuation step from a straight line passing through the no-gain/attenuation value and the full-gain/attenuation value (i.e. end points). Units in dB.

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Out-of-Band Energy

The ratio of the rms sum of the energy from 0.46xFs to 2.1xFs compared to the rms full-scale signal value. Tested with 48kHz Fs giving an out-of-band energy range of 22kHz to 100kHz.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input at CMOUT. For the DACs, the deviation of the output from CMOUT with mid-scale input code. Units in volts.

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APPENDIX A

This data sheet describes version 2 of the CS4215. Therefore, this appendix is included to describe the differences between versions 0,1 and version 2. This information is only useful for users that still have version 0 and version 1 devices since version 2 devices will supplant the earlier versions. The version number can be found in control mode, time slot 7. The version can also be identified by the revision letter stamped on the top of the actual chip. The revision letter immediately precedes the data code on the second line of the package marking (See *General Information* section of the Crystal Data Book). Version 0 corresponds to chip revision C, version 1 corresponds to chip revision D, and version 2 corresponds to chip revision E. Future chip revisions (ie. F, G, H) may still be version 2 since the version number only changes if there is a register change to the part that will affect driver software.

The Functional Differences Between Version 0(Rev. C) and Version 1(Rev. D)

1. FSYNC on version 0 must be ONLY one SCLK period high, whereas on version 1 FSYNC must be AT LEAST one SCLK period high.

2. When driving an external CMOS clock into one of the XTL-IN pins, version 0 devices must have a series resistor of at least 1kΩ between the CS4215 and the clock source. The resistor is needed because the codec will put XTL-IN to ground (on version 0 only) when that crystal is not selected, as is the case on power-up. In version 1 the XTL-IN pins are floated when not selected; therefore, the series resistor is not needed on version 1. Version 1 will work properly if the resistor is included.

3. The OLB and ITS bits do not exist on version 0. Writing these bits as zero makes both versions function identically; therefore, version 1 is backwards compatible with version 0.

4. When entering control mode, CLKOUT stops 4 to 12 clocks later and may start up briefly when switching master clock sources on version 0. On version 1 CLKOUT stops within two clocks and doesn't start up until data mode is entered.

5. In version 0 the headphone and speaker outputs are not short-circuit protected, whereas in version 1 they are short-circuited protected.

The functional differences between Version 1(Rev. D) and Version 2(Rev. E)

1. The MLB, HPF, and MCK2 bits in control mode do not exist in version 0 or version 1. Writing these bits as zero makes all versions functionally identical; therefore, version 2 is backwards compatible with previous versions.

2. The A/D invalid bit, ADI, in data mode does not exist in version 0 or version 1.

3. The 8-bit unsigned data format (DF1,0=3) does not exist in version 0 or version 1.

4. SDOUT contained random data during calibration in versions 0 and 1. SDOUT outputs zeros during calibration in version 2.

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