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OPERATING MANUAL

PENTEK MODEL 4272

Multiband Digital Receiver
MIX Module for VMEbus Systems

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Pentek Model 4272 Operating Manual - Revision History

Date	Rev	Applicable Serial #'s	Comments
10/28/94	Preliminary	9443001 - Forward	Initial Product Release - Revised from 4271 Manual
10/31/94	Preliminary	9443001 - Forward	Added Sample Code in Appendix A
11/10/94	Preliminary	9443001 - Forward	Change to Sample Code - sense of comparison of status register for FIFO Half-Full condition corrected.
11/17/94	Preliminary	9443001 - Forward	Figure 2-1: Specified that Sync signal on Wideband I/O connector is an Output. Added description to Section 2.6.
02/01/95	Preliminary	9443001 - Forward	Remove signal routing scheme showing common data w/separate strobes from Fig. 1-2. Re-move 4-ch. reference from page 9. Input Termination Resistors (Sec. 2.3.2) - 12 devices, not 16. Remove Ch. D rows from Table 2-1. Corrections to Table 3-2: D1 & D9 (Harris Reset), 1 = Reset; D4, D12 & D18 (Pack Mode), 1 = Disable. Same changes to text descriptions of these bits, Secs. 3.3.2 & 3.3.5. Corrections to Table 3-4: Q samples in upper word, I in lower. Same change to accompanying text, Sec. 3.5
08/28/95	A	9443001 - Forward	Remove references to Options 010 and 013 from Specs and Appendix B, and add Option 019 (16-bit TTL input interface for 6410 and 4261 Option 019). Minor corrections to Figs. 1-2 and 1-3, pgs. 8 & 9. Separate Address Maps added for each MIX Baseboard. Indicate that Command Shift Mode for Harris chips takes about 1 msec, (Sec 3.3.4). Data Type bits in Status Register are dependent on which DDR chip and state of Packing, so new table is added to explain all of that. Correct info about where good data can be found in Real Mode. Table describing Packed Data Mode Addressing in Sec. 3.5 (Table 3-4 in last rev., 3-9 in this one) corrected with respect to where I & Q bytes are found in Non-Packed Mode. New Sample Code in Appendix A.
08/05/96	B	9443001 - Forward	Change pinout tables in Figures 2-1 and B-1 and B-3, such that pin 1 is listed at lower right of tables, to agree with connector orientations. Use symbolic addresses from sample code in Memory Maps. Correct text in Section 3.3.8 (GC Sync Source) to agree with bit setting listed in Table 3-6 (0=int, 1=ext). Sec. B.2.2 - Change all 6410 references to 64xx. Correction to Figure B-6 & accompanying text - MUST connect 4261 to A input, NOT B! Update MIX Appendix. Add all Figures & Tables to Table of Contents.
04/26/99	C	9443001 - Forward	Changes to Specs (Sec. 1.5): sample rate for wideband channel is 50 MHz w/ ECL option; lowest decimation for wideband channel is 4; added reference to option 021 which allows a wideband decimation of 2. Changed Sec. 3.5 and Table 3.7: for channel C bit D21 is not used and bit D22 is used to enable the time-out clock. Deleted App. E, F and G, now covered by separate MIX Tutorial manual.
5/11/99	C.1	9443001 - Forward	Table 3-6; changed all references from 4252 to 4272; corrected typographical errors.

The material presented in Appendix C of this manual is excerpted from Harris Semiconductor Corp.'s Data Sheet for the HSP50016 Digital Down Converter. The material presented in Appendix D of this manual is excerpted from Graychip, Inc.'s Data Sheet for the GC1012 Digital Tuner. Pentek gratefully extends its thanks to both Harris and Graychip for their permission to use these copyrighted materials.

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Chapter 1: General Description

1.1 General Information

The Model 4272 is a general-purpose, multiband digital receiver MIX module that accepts 12-bit digitized data at sampling rates up to 70 MHz. It contains two narrowband receivers and one wideband receiver, which perform frequency down-conversion (i. e., translation to baseband), low-pass filtering and decimation of the sampled output. The receiver output signals can be delivered through the MIX bus to one of Pentek's VMEbus MIX baseboards, such as the Models 4283, 4284, 4285 (Options 031 and 036), 4200, 4201, and 4202, which can provide DSP functions and/or DMA transfers to the VMEbus. A front panel digital output from the wideband receiver allows data to be sent to a DSP subsystem over a dedicated parallel cable.

1.2 Operating Principle

The Model 4272 uses the GC1012, a highly-integrated digital receiver chip manufactured by Graychip, Inc., as the wideband receiver. The narrowband receiver chips are HSP50016's, manufactured by Harris Semiconductor Corp. All of these devices contain tunable local oscillators, mixers and tunable low pass output filters, all implemented in digital logic. The local oscillator frequency and the output filter cutoff frequency in each section are independently programmable over the MIX interface providing extremely flexible and agile operation.

1.3 Flexible Input and Output Connections

All input data is accepted on front panel parallel connectors, with either TTL or ECL level compliance An input multiplexer at the narrowband receivers allows data to be taken either from independent input connectors or from the wideband receiver input connector, so that all receivers can process the same input signal. Operating modes and receiver frequencies are programmable over the MIX bus.

The output data from each receiver is delivered to a separate FIFO buffer for output over the MIX bus. Output data from the wideband channel is also delivered to the front panel connector. A full complement of FIFO interrupt flags is provided for efficient transfers. All control of operating modes and tuning frequency is programmable over the MIX bus.

The Model 4272 is ideal as a general purpose digital receiver for VMEbus workstations and embedded systems.

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1.4 Block Diagram and Circuit Description

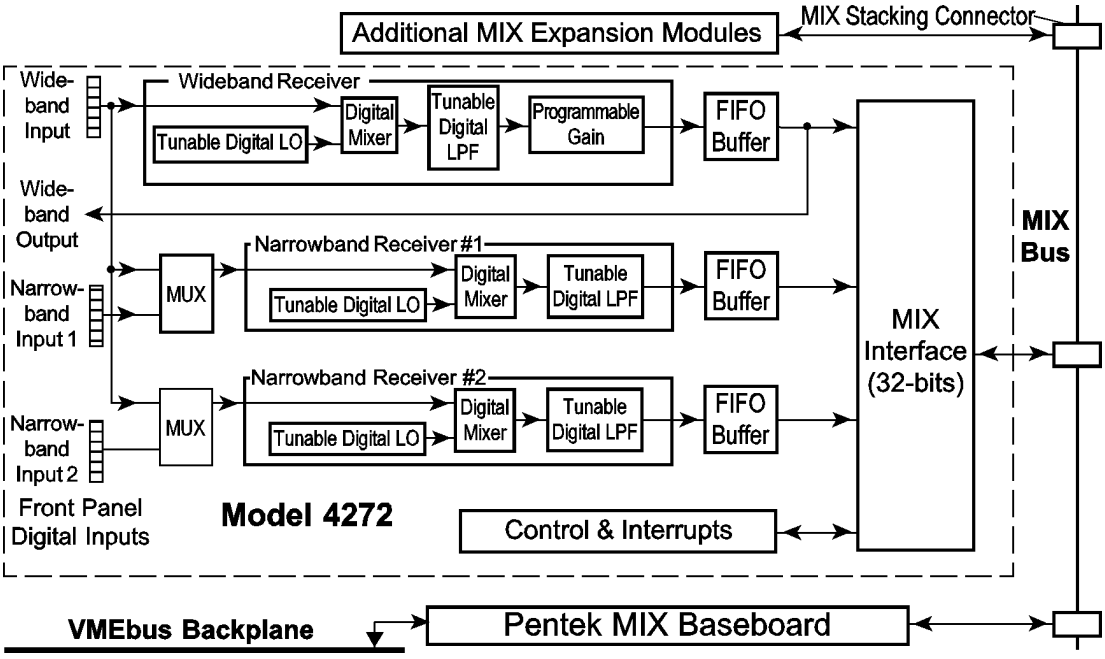


Figure 1-1: Model 4272 - Block Diagram

Figure 1-1, above, shows a block diagram of the Model 4272. The front end of the Model 4272 consists of an input section capable of accepting digital data from a variety of sources including single-ended TTL, differential TTL (RS-422), single-ended and differential ECL. These input varieties are supported by a family of daughtercards available as options. The standard input is single-ended TTL, and the pinout of the narrowband channels is compatible with the output connectors of Pentek's Model 64XX Series of A/D Converters.

Once the data is received, it can be routed through one of two paths: the data from the wideband I/O connector can be used for all channels, or each channel can receive its own data stream. Likewise, the clocks and timing signals from the wideband channel can be routed to all channels, or separate signals can be used for each channel.

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1.4 Block Diagram and Circuit Description (continued)

These arrangements allow the user to configure the Model 4272 to process a single input sequence with three separate receivers, each tuned to a different local oscillator frequency. Alternately, the three receivers can be used completely asynchronously, with different clock and data signals. One popular configuration is to use two data streams for I and Q channels using a common clock.

Because the three receiver chips are completely independent, each one can be programmed for a different local oscillator frequency and filter characteristics. On the other hand, provisions are included for synchronizing all three devices so that the local oscillator signals in all receivers are operating with the same phase angle.

Because the Model 4272 is a MIX module, it can be combined very effectively with other MIX-compatible products for VMEbus from Pentek, to create powerful signal processing and analysis systems. For example, the 21.4 MHz IF output from a VHF receiver can be connected to the analog input of the Pentek Model 6472 70 MHz 10-bit A/D converter. Digital samples from the Model 6472 are delivered to all three inputs of the Model 4272.

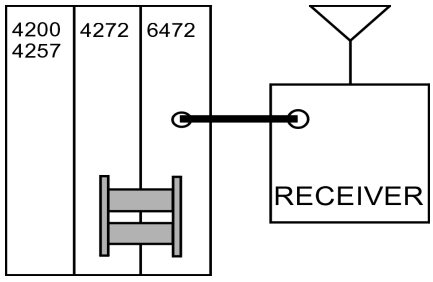


Figure 1-2: Model 4272 in a Signal Acquisition and Processing System

If the Model 4272 is attached to a Pentek Model 4200 MIX baseboard equipped with a Model 4257 Dual TMS320C40 co-processor MIX module, a very powerful multiband, 550 mega-op signal processing receiver can be assembled in three VMEbus slots.

Three independent tuning bands can be selected with the Model 4272. The three selected signals are sent from the Model 4272 through the MIX bus to the 'C40 processors in the Model 4257. The DSP's can then perform FFT or signal classification functions, and report results to the VMEbus through the Model 4200.

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1.5 Model 4272 Specifications

General:

Receiver Chips:

Wideband:	Graychip GC1012
Narrowband:	Harris HSP50016 (two channels)

Digital Inputs:

Standard Unit:

Input Data:	12 bits, 2's complement, single-ended TTL
Input Strobe:	1 line per channel
Connectors:	Two, front-panel 68-pin flat ribbon cable connectors, 0.025-in. pitch cable. The narrowband connector carries 12-bit input data, clocks and strobes for the two narrowband channels.The wideband connector carrys 12-bit input data, clocks, strobes, 16-bit output data and FIFO Flags for the wideband channel.

Option 012:

Input Data:	12 bits, 2's complement, differential ECL
Input Strobe:	1 line per channel
Connectors:	Same signal arrangement as standard unit, but complementary input signals replace grounds on connector.

Option 019:

Input Data:	16 bits, 2's complement, single-ended TTL
Input Strobe:	1 line per channel
Connectors:	Two, front-panel 80-pin flat ribbon cable connectors, 0.025-in. pitch cable. Narrowband connector carries 16-bit input data, clocks and strobes for the two narrowband channels. Wideband connector caries 16-bit input data, clocks, strobes, 16-bit output data and FIFO Flags for the wideband channel.

Sampling Rate:

TTL Inputs:	DC to 30 MHz max
ECL Inputs:	
Narrowband Channels:	DC to 70 MHz max
Wideband Channel:	DC to 50 MHz max

Input Levels:

Standard:	TTL, Single-Ended
Option 012:	ECL, Differential
Option 019:	TTL, Single-Ended

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1.5 Model 4272 Specifications (continued)

Tunable Digital Local Oscillators

Type: Direct Digital Synthesizer
Programming: 28-bit Binary Word (FREQ)

$$\text{Frequency} = \frac{\text{Sample Rate}}{2^{28}} \times \text{FREQ}$$

Resolution: Sample Rate / 2^{28}
Format: Four bytes
Outputs: 12-bits, sine and cosine, to Mixer

Digital Mixer

Inputs: 12-bit front panel input word (16 bits for Option 019)
12-bit sine and cosine from digital Local Oscillator
Output: 16-bits to Digital Low Pass Filter

Tunable Low Pass Filters:

Narrowband Channels:

Type: Decimating FIR, > 90dB stopband rejection
Programming: 14-bit integer, D
Operation: Sampling rate and bandwidth at the output are reduced by a factor of 4D for Complex Mode and 2D for Real Mode
Range: 16 < D < 16,384

Wideband Channel:

Type: Decimating FIR, > 75 dB stopband rejection
Programming: 14-bit integer, D
Operation:
Standard: Sampling rate and bandwidth at the output are reduced by a factor of 4, 8, 16 or 32 for Real Mode and 8, 16, 32 or 64 for Complex Mode.
Option 021: Sampling rate and bandwidth at the output are reduced by a factor of 2, 4, 8, 16 or 32 for Real Mode and 4, 8, 16, 32 or 64 for Complex Mode.

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1.5 Model 4272 Specifications (continued)

FIFO Buffers:

Number: One per channel

Size:
- Narrowband Channels: 1k samples x 16 bits (Standard)
  8k samples x 16 bits (Option 020)
- Wideband Channel: 16k samples x 16 bits

Interrupts: MIX interrupts for full, half-full, and empty conditions

Output Data: Programmable, Real or Complex

Real Mode: Consecutive 16-bit, 2's complement real samples
Complex: Interleaved 16-bit, 2's complement I and Q samples

MIX Interface:

Baseboard: Mounts directly to any of Pentek MIX baseboards using MIX expansion bus.

Memory Map: Control registers and FIFO data output for each digital receiver section are memory mapped at specific MIX bus address locations

Interrupts: FIFOs can interrupt MIX bus on Empty, Full and Half-Full conditions

Power: 3.0 A @ 5 V^{DC} max

Dimensions: Each module occupies one 0.8" VMEbus slot position and has its own front panel

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If you discover any damage, please contact Pentek immediately, at (201) 818-5900. Please save the original shipping container and packing material, in case re-shipment is required.

2.2 Front Panel Digital Input and Output Connectors - Standard TTL I/O

The Model 4272's front panel contains two flat cable connectors. The connector at the bottom of the panel carries the data, clock and strobe inputs for the two narrowband receivers, which we will often refer to as receiver channels A and B. The pin assignments for this connector are shown in the table on the right in Figure 2-1, on page 24. The connector at the top of the panel carries the data, clock and strobe inputs, and the data and FIFO flag outputs, for the wideband receiver, which we often refer to as receiver channel C. The pin assignments for this connector are shown to the left of Figure 2-1.

The 4272 can accommodate different types of input signals. The input circuitry is contained on a daughter card inside the module, called the Mezzanine board. The description below applies to the standard, single-ended, TTL option. For other input options, refer to information in Appendix B.

The standard TTL input connector is a 68-pin flat ribbon cable header manufactured by 3M. The part number for the header is 3M #81068-620203. The mating flat cable socket connector is 3M #82068-6006, and the strain relief is 3M #3858-068. Two of each of these items are supplied with the Model 4272. The recommended cable is 3M #3756-068.

For each of the narrowband input channels, the input signals consist of 12 data lines (D0 - D11), a data strobe (CK), and two sync control lines (SS and AS). The wideband input channel also accepts a third sync signal (GS), and provides connections for the 16-bit output from the drop receiver, the output FIFO flags, and FIFO read and clear inputs.

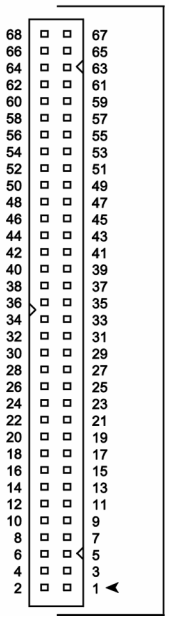
Note that each input line has an associated GND line opposite it (see the tables in Figure 2-1). This translates to an alternating GND/signal line sequence in the flat ribbon cable, very desirable in controlling crosstalk and impedance. It is recommended that the driving end of the cable have all of the GND lines connected to signal ground to help maintain signal integrity.

The nominal impedance of the 3M flat cable listed above is 85Ω. All input lines can be terminated with either pullup resistors to +5V, pulldown resistors to GND, or both. These resistors are described in Section 2.4. The type of line driver to use depends on the length of the cable, clock frequency and termination chosen.

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Top Input/Output Connector Wideband Channel (C)			
68	GND	67	GND
66	GND	65	Ch C - $\overline{GS}$ in
64	GND	63	Ch C - CK in
62	GND	61	Ch C - $\overline{AS}$ in
60	GND	59	Ch C - $\overline{SS}$ in
58	GND	57	Ch C - D11 in (MSB)
56	GND	55	Ch C - D10 in
54	GND	53	Ch C - D9 in
52	GND	51	Ch C - D8 in
50	GND	49	Ch C - D7 in
48	GND	47	Ch C - D6 in
46	GND	45	Ch C - D5 in
44	GND	43	Ch C - D4 in
42	GND	41	Ch C - D3 in
40	GND	39	Ch C - D2 in
38	GND	37	Ch C - D1 in
36	GND	35	Ch C - D0 in (LSB)
34	$\overline{GND}$	33	$\overline{GND}$
32	$\overline{FRST}$	31	$\overline{FRD}$
30	GND	29	$\overline{GND}$
28	Sync Out	27	$\overline{FF}$
26	$\overline{HF}$	25	$\overline{EF}$
24	GND	23	GND
22	GND	21	GND
20	Ch C - D15 out (MSB)	19	Ch C - D14 out
18	Ch C - D13 out	17	Ch C - D12 out
16	Ch C - D11 out	15	Ch C - D10 out
14	Ch C - D9 out	13	Ch C - D8 out
12	GND	11	GND
10	GND	9	GND
8	Ch C - D7 out	7	Ch C - D6 out
6	Ch C - D5 out	5	Ch C - D4 out
4	Ch C - D3 out	3	Ch C - D2 out
2	Ch C - D1 out	1	Ch C - D0 out (LSB)

Bottom Input Connector Channels A and B			
68	GND	67	GND
66	GND	65	N/C
64	GND	63	Ch B - CK
62	GND	61	Ch B - $\overline{AS}$
60	GND	59	Ch B - $\overline{SS}$
58	GND	57	Ch B - D11 in (MSB)
56	GND	55	Ch B - D10 in
54	GND	53	Ch B - D9 in
52	GND	51	Ch B - D8 in
50	GND	49	Ch B - D7 in
48	GND	47	Ch B - D6 in
46	GND	45	Ch B - D5 in
44	GND	43	Ch B - D4 in
42	GND	41	Ch B - D3 in
40	GND	39	Ch B - D2 in
38	GND	37	Ch B - D1 in
36	GND	35	Ch B - D0 in (LSB)
34	GND	33	GND
32	GND	31	N/C
30	GND	29	Ch A - CK
28	GND	27	Ch A - $\overline{AS}$
26	GND	25	Ch A - $\overline{SS}$
24	GND	23	Ch A - D11 in (MSB)
22	GND	21	Ch A - D10 in
20	GND	19	Ch A - D9 in
18	GND	17	Ch A - D8 in
16	GND	15	Ch A - D7 in
14	GND	13	Ch A - D6 in
12	GND	11	Ch A - D5 in
10	GND	9	Ch A - D4 in
8	GND	7	Ch A - D3 in
6	GND	5	Ch A - D2 in
4	GND	3	Ch A - D1 in
2	GND	1	Ch A - D0 in (LSB)



The mating flat cable socket connector is 3M #82068-6006 and the strain relief is 3M #3858-068.

Two each of these items are supplied with the Model 4272.

The recommended 0.025" pitch flat cable is 3M # 3756/068.

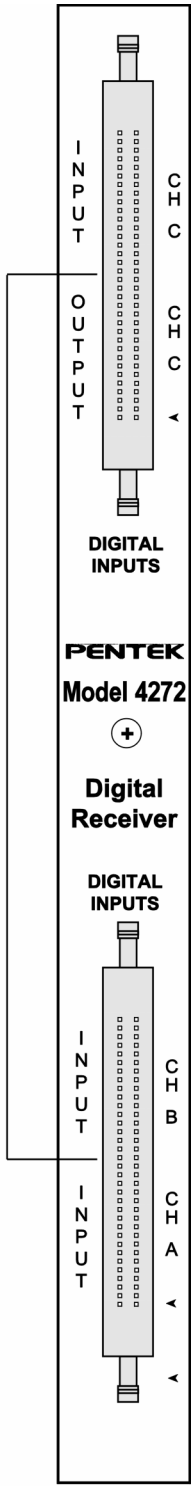


Figure 2-1: Front Panel Input Connector Pin Assignment - Standard TTL Input

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2.2 Front Panel Digital Input and Output Connectors (continued)

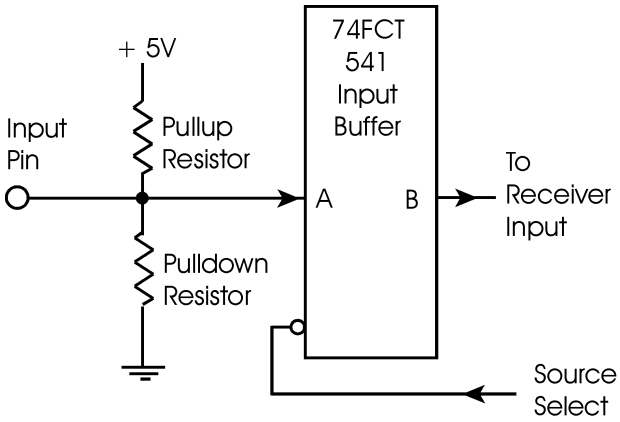


Figure 2-2: Typical Input Signal Circuitry

The input circuitry for the data, clock and strobe signals is shown schematically in Figure 2-2, above. The data buffer is a type 74FCT541. FCT is a high-performance, TTL compatible CMOS logic family manufactured by Integrated Device Technology (IDT). The source select signal comes from a programmable register bit that determines whether the input for a narrowband receiver comes from its own connector or from the wideband connector. The enable input on the wideband receiver's input buffers are grounded (i. e., they are always enabled).

2.3 Setup Information - Standard TTL I/O

The Model 4272 consists of two PC assemblies: the MIX Board and the Mezzanine Board. The MIX board contains the receiver circuitry, FIFOs and MIX bus interface.

The Mezzanine board contains the digital interface circuitry between the front panel connectors and the input to the receiver chips. Different mezzanine boards are used for the various input options. The standard, single-ended TTL option is described in this section of the manual. For other interface options, see Appendix B.

The MIX and Mezzanine boards are connected mechanically and electrically, and must be separated to change the termination resistors. There are no user configurable jumpers on the MIX board or the Mezzanine board. For reference purposes, the component layout drawings for both the MIX and Mezzanine boards are shown in Figure 2-3 and Figure 2-4.

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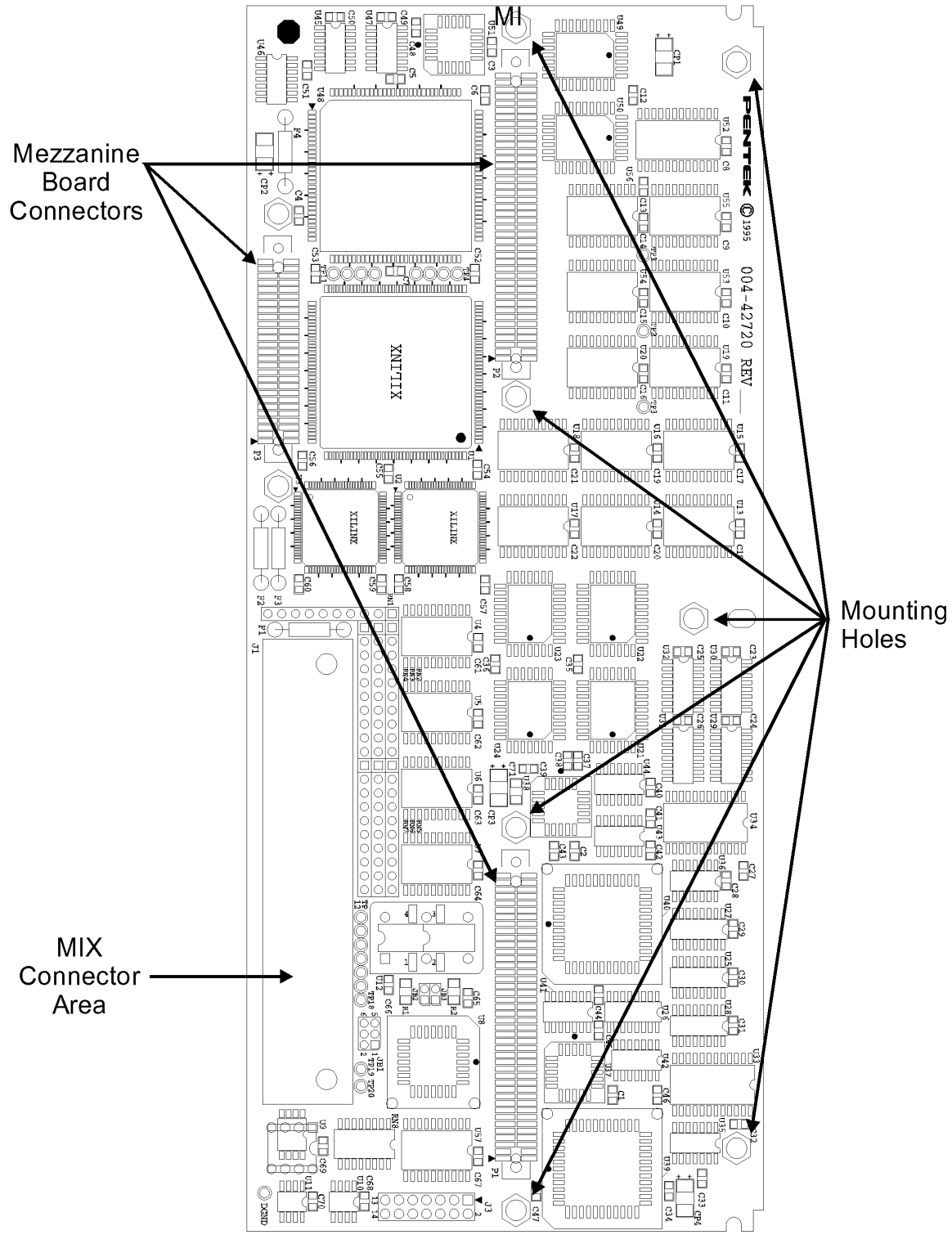


Figure 2-3: Model 4272 MIX Board Connector and Mounting Hole Locations

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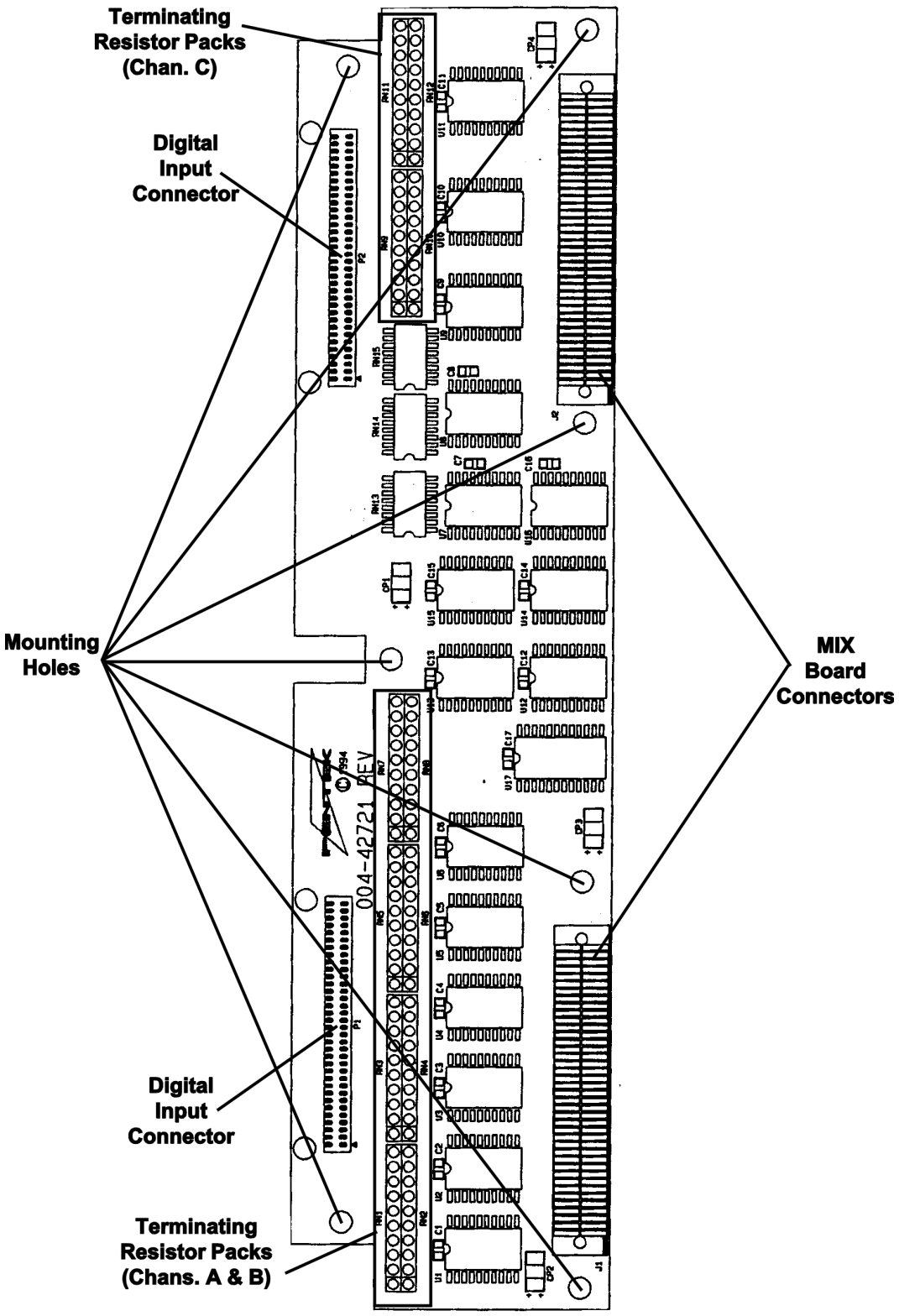


Figure 2-4: Model 4272 Mezzanine Board Component, Connector and Mounting Hole Locations - Standard TTL I/O

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2.3 Setup Information - Standard TTL I/O (continued)

2.3.1 Separating the MIX and Mezzanine Boards

Follow the procedure below to separate the two boards.

CAUTION!!

Perform all assembly steps in a static controlled work environment

---

1) Place the Model 4272 on the work surface with the MIX board down.
2) Remove the seven nylon Philips head screws from the solder side of the Mezzanine board.
3) Close the ejectors on the front panel digital I/O connectors.
4) Separate the two boards by gently and evenly separating the two connectors at the rear of the Mezzanine board.
5) Lift out the Mezzanine board by slipping the ejector ears through the holes in the front panel.

To re-attach the MIX and Mezzanine boards, reverse the above procedure.
Be careful to properly align the headers in their sockets during the mating operation.

2.3.2 Input Termination Resistors - Standard TTL I/O

All three input channels can have user-replaceable termination resistors installed on all input lines. These resistors are in the form of SIP (single in-line package) resistor networks. The resistor networks required are 10-pin devices with one common pin and 9 resistors as shown physically and schematically in Figure 2-5, at the top of the page 23.

There are four resistor networks per channel: two for pulldown and two for pullup for a total of 12 devices. All are socketed so they can be removed or changed easily. The location of these resistor networks is on the Mezzanine board, and is shown in Figure 2-4, on page 21.

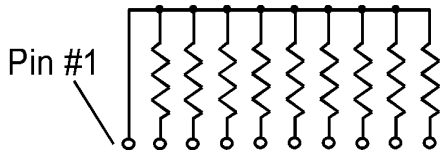
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2.3 Setup Information - Standard TTL I/O (continued)

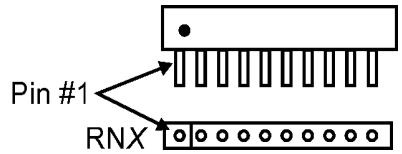
2.3.2 Input Termination Resistors - Standard TTL I/O (continued)

Figure 2-5: Model 4272 -Terminating Resistor Networks

(a) Schematic



(b) Package & Silk Screen Marking



The recommended part numbers from four manufacturers are given below:

Allen-Bradley	110A-ddm
Bournes	4310R-101-ddm (molded package)
Bournes	10X-1-ddm (conformally coated package)
Sprague	420CH-ddm-X2P2
Beckman	L10-1C-ddm

where dd is the two-digit resistor value and m is the multiplier (power of 10). For example, a 330 Ω molded Bournes network would have the following number: 4310R-101-331.

Table 2-1 tells which resistor network location provides what function for which signals. Note that the Model 4272 is shipped with factory-installed resistor networks as shown in this table.

When installing the resistor networks, be sure to install pin #1 of the resistor network (usually indicated by a dot on the package) in socket pin #1 designated by a square silk screen marking. Refer to Figure 2-5, above.

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2.3 Setup Information - Standard TTL I/O (continued)

Table 2-1: Model 4272 - Input Termination Resistor Network Definition - Standard TTL I/O

Channel	Input Signals	Pullup Location	Installed Pullup Network	Pulldown Location	Installed Pulldown Network
A	D0 - D7	RN1	330 ohm	RN9	390 ohm
A	D8-D11,CK,SS,AS	RN2	330 ohm	RN10	390 ohm
B	D0 - D7	RN3	330 ohm	RN11	390 ohm
B	D8-D11,CK,SS,AS	RN4	330 ohm	RN12	390 ohm
C	D0 - D7	RN5	330 ohm	RN13	390 ohm
C	D8-D11,CK,SS,AS	RN6	330 ohm	RN14	390 ohm

2.4 Installing the Model 4272 on the MIX Baseboard

See the MIX Tutorial for VMEBus Systems (Manual Part Number 800.00001) for MIX module stack assembly instructions.

2.5 Installing the Assembly into the VMEbus Card Cage

See the MIX Tutorial for VMEBus Systems (Manual Part Number 800.00001) for MIX module stack installation instructions.

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2.6 Signal Description

Below is a list of each I/O signal along, with a description.

Signal	Description
D0 - D11 in	**Digital Input Data:** These 12 input data lines are used to deliver the 2's complement digital input. Bit D0 is the least significant bit and D11 is the most significant bit. Levels are coded as follows:

Positive Full Scale	0111 1111 1111
:	:
+1 LSB	0000 0000 0001
Zero (center of range):	0000 0000 0000
-1 LSB	1111 1111 1111
:	:
Negative Full Scale	1000 0000 0000

CK	**Input Data Clock:** This input line is buffered in the same manner as the data lines. The buffered clock signal is used to clock the incoming data into the receiver chips.
$\overline{SS}$	**System Sync:** This input line is used as a reset signal for all timers, accumulators and control counters within the receiver chips. Use of this signal for the narrowband receivers is described in the HSP50016 manual in Appendix C. Use of this signal for the wideband receiver is described in the GC1012 manual in Appendix D.
$\overline{AS}$	**Accumulator Sync**: This input line supports synchronization of tuning frequency changes within the GC1012. The narrowband channels do not use this input. Use of this signal is described in the GC1012 manual in Appendix D.
D0 - D15 out	**Digital Output Data:** Available only from the wideband receiver (Channel C). Coding of the output data is 16-bit 2's complement, similar to the input coding.
$\overline{EF}$	**FIFO Empty Flag:** The 4272 drives this line low when no output data is available in the channel C output FIFO.
$\overline{HF}$	**FIFO Half-Full Flag:** The 4272 drives this line low while the channel C output FIFO is half-full or more.
$\overline{FF}$	**FIFO Full Flag:** The 4272 drives this line low there is no more room for data in the channel C output FIFO.
$\overline{FRD}$	**FIFO Read:** Drive this line low to read data from the 4272's channel C output FIFO via the front panel connector.
$\overline{FRST}$	**FIFO Reset:** Drive this line low to reset the channel C output FIFO.
SYNCOUT	**Sync Output:** In Unpacked mode, this output is high when a real sample is at the output connector, and low when the output sample is imaginary. In Packed mode, this output is always high.

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2.7 Input Selection - Standard Input

The Model 4272 allows data delivered to the channel C input connector to be distributed to any or all of the three channels. In addition, the input clock (CK) and sync signals ($\overline{AS}$ and $\overline{SS}$) delivered to Channel C input connector can be delivered to any or all of the three channels.

As shown in Figure 2-6, below, selection of the input signals is accomplished by programming register bits to enable the appropriate tri-state buffers.

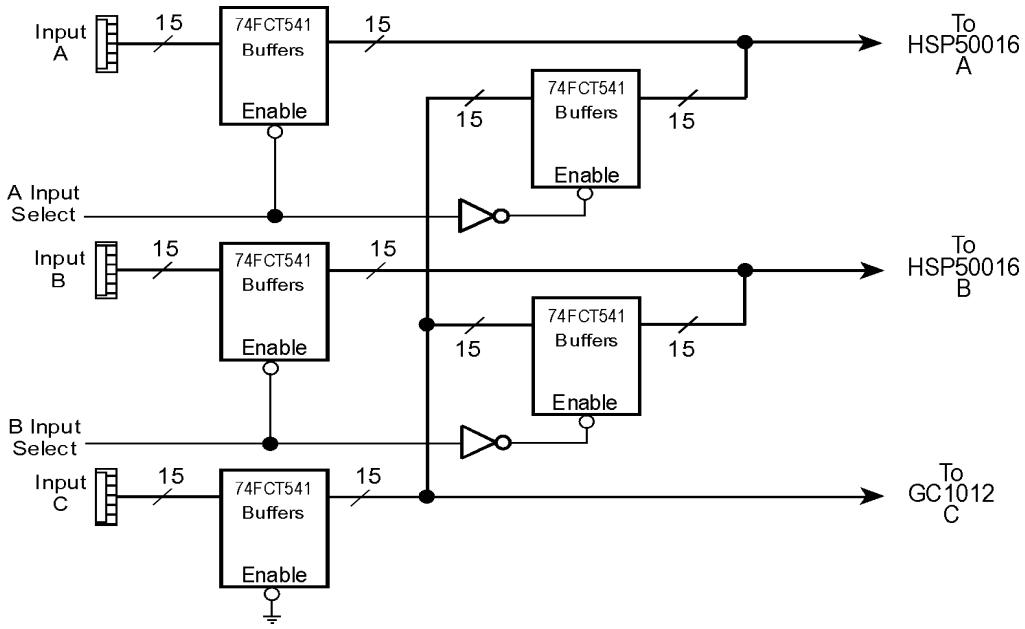


Figure 2-6: Model 4272 - Input Source Selection

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Chapter 3: Memory Maps and Register Descriptions

3.1 Programming Overview

The following sections cover access to the Model 4272 from the MIX Baseboard and the issuing of commands for module control and data transfers. There are two cases to be considered, dependent upon the type of Baseboard used. This chapter gives details for Baseboards that use direct MIX addressing, such as Pentek's Models 4200, 4200A, 4201, 4201A, 4284 and 4285 (with Option 031 or 036). General information on the use of these Baseboards is given in the MIX Tutorial for VMEBus Systems (Manual Part Number 800.00001). The Memory Map for the Model 4283 is also included in this chapter.

3.2 Address Maps

The sections below will present address maps for the twenty-seven resources available on the Model 4272, for each type of MIX Baseboard available from Pentek. These resources are assigned a symbolic name that are referrenced in subsequent sections of the manual.

For Models 4200, 4200A, 4201 or 4201A, use the address map in Section 3.2.1. If you will be using your Model 4272 with a Model 4202 Baseboard, use the address map in Section 3.2.2. If the Model 4283 will be the MIX Baseboard for your Model 4272, skip to Section 3.2.3, and use the address map found there. If your 4272 will be mounted on a Model 4284 Baseboard, use the address map in Section 3.2.4. Finally, if the Model 4285 is the baseboard that will control your MIX, refer to the address map in Section 3.2.5.

By convention, the MIX addresses given in this manual are generally given as 8-digit hexadecimal codes, with a space between the first and second four digits, simply for notational convenience. The form is MIX_base+0xYYYY ZZZZ. The leading '0x' is common notation for a hex value in the 'C' programming language.

Since each hex digit represents 4 bits, the 8-digit MIX address represents 32 bits of address. The MIX_base part of the address is dependent upon the Baseboard in use, and is used to select each module by its stack position. This geographical addressing scheme avoids the need for address jumpers and possible conflicts, but requires that software must accommodate the physical placement of modules in the MIX stack.

The exception to this convention will be for the Model 4283 Baseboard, whose TMS320C30 processor only has a 24-bit address bus on the port it uses for the MIX bus. In this case, a page register is used for module selection (as opposed to different base addresses for each module), and the addresses are given as 6-digit hexadecimal codes, of the form 0xYY ZZZZ.

A final point must now be made about MIX nomenclature. Module 0 (or MIX position 0) refers to the closest module to the Baseboard, whether or not it is nested. Module 1 (or MIX position 1) is the module that may be mounted above Module 0, and Module 2 is the device that may be stacked above Module 1.

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3.2 Address Maps (continued)

3.2.1 Model 4272 Address Map for the 4200/01 Series Baseboards

Table 3-1: Model 4272 Memory Map for Use with Models 4200, 4200A, 4201 and 4201A MIX Baseboards- 68030 View

4200/01 68030 Address	Symbolic Name	Resource
MIX_base+0x0000 0000	Control_Reg	Control Register
MIX_base+0x0000 0004	Status_Reg	Status Register (Read Only Access)
MIX_base+0x0000 0008	Harris_CntlA_MSB	Harris Channel A Control Register (MSB)
MIX_base+0x0000 000C	Harris_CntlA_LSB	Harris Channel A Control Register (LSB)
MIX_base+0x0000 0010	Harris_CntlB_MSB	Harris Channel B Control Register (MSB)
MIX_base+0x0000 0014	Harris_CntlB_LSB	Harris Channel B Control Register (LSB)
MIX_base+0x0000 0018	Mezz_Cntl_1	Mezz Control 1 Register
MIX_base+0x0000 001C	Mezz_Cntl_2	Mezz Control 2 Register
MIX_base+0x0000 0020	Harris_A_FIFO	Output FIFO Channel A (Read Only Access)
MIX_base+0x0000 0024	Harris_B_FIFO	Output FIFO Channel B (Read Only Access)
MIX_base+0x0000 0028	Graychip_FIFO	Output FIFO Channel C (Read Only Access)
MIX_base+0x0000 0040	GCC_Freq_Byte_0	Graychip Channel C Frequency Byte 0
MIX_base+0x0000 0044	GCC_Freq_Byte_1	Graychip Channel C Frequency Byte 1
MIX_base+0x0000 0048	GCC_Freq_Byte_2	Graychip Channel C Frequency Byte 2
MIX_base+0x0000 004C	GCC_Freq_Byte_3	Graychip Channel C Frequency Byte 3
MIX_base+0x0000 0050	GCC_Sync_Mode	Graychip Channel C Sync Mode Register
MIX_base+0x0000 0054	GCC_Filter_Mode	Graychip Channel C Filter Mode Register
MIX_base+0x0000 0058	GCC_Gain_Control	Graychip Channel C Gain Fraction Register
MIX_base+0x0000 005C	GCC_Gain_Exponent	Graychip Channel C Gain Exponent Register
MIX_base+0x0000 0060	GCC_Output_Mode	Graychip Channel C Output Mode Register
MIX_base+0x0000 0064	GCC_Output_Status	Graychip Channel C Output Status Register
MIX_base+0x0000 0068	GCC_One_Shot	Graychip Channel C One Shot Register
MIX_base+0x0000 006C	GCC_Checksum	Graychip Channel C Checksum Register
MIX_base+0x0000 0070	GCC_I_Output_Byte_0	Graychip Channel C **I** Output Byte 0 Register
MIX_base+0x0000 0074	GCC_I_Output_Byte_1	Graychip Channel C **I** Output Byte 1 Register
MIX_base+0x0000 0078	GCC_Q_Output_Byte_0	Graychip Channel C **Q** Output Byte 0 Register
MIX_base+0x0000 007C	GCC_Q_Output_Byte_1	Graychip Channel C **Q** Output Byte 1 Register

MIX base Address:
If 4272 is in MIX position 0, MIX_base=0xC000 0000
If 4272 is in MIX position1, MIX_base=0xD000 0000
If 4272 is in MIX position 2, MIX_base=0xE000 0000

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3.2 Address Map (continued)

3.2.1 Model 4272 Address Map for the 4200/01 Baseboards (continued)

Pentek's Models 4200 and 4201 Baseboards use a 16 MHz 68030 processor as the MIX bus controller. The 4200A and 4201A use a 40 MHz 68030. From the 68030's viewpoint, the MIX bus is mapped identically for all four of these Baseboards. The MIX_base address for Module 0 (which may either be nested, sharing the Baseboard's VMEbus slot, or stacked in the adjacent VMEbus slot), is 0xC000 0000. For the next device in the stack, Module 1, the base address is 0xD000 0000. Finally for the last MIX Module in the stack, Module 2, the MIX_base address is 0xE000 0000. Table 3-1, page 28, gives the physical addresses, in the memory space of the 68030 processor on any of these four Baseboards, that correspond to the symbolic names used to represent the Model 4272's resources in subsequent sections of this manual.

Note that the 4200 series of VME/MIX Baseboards also support mastering of the MIX bus by Upper MIX Bus Masters (UMBMs), and by VMEbus Masters. For further information about MIX Bus access on these Baseboards in this manner, please refer to the MIX Tutorial for VMEBus Systems (Manual Part Number 800.00001).

3.2.2 Model 4272 Address Map for the Model 4202 Baseboard

The Model 4202 is a VMEbus slave-only Baseboard, and contains no processor. This device maps the resources connected to its MIX Bus into VMEbus A32, A24 or A16 slave address space. The VMEbus A32 or A24 base address is programmed into a register in the 4202's A16 interface by a VMEbus Master (the A16 base address is set by switches on the board). This register is cleared at power-up, resulting in a default base address of 0x0000 0000 in A32 space, or 0x00 0000 in A24 space.

In direct addressing mode, the two most significant bits of the VMEbus address (i. e., A31 and A30 in A32 space, A23 and A22 in A24 space or A15 and A14 in A16 space) select a particular 4202 Baseboard, by comparison with the two Least Significant Bits (D1 and D0) of the VMEbus Address Register. The next two VMEbus address bits (i. e., A29 and A28 in A32 space, A21 and A20 in A24 space, or A13 and A12 in A16 space) select among the MIX modules stacked on the 4202. Thus, assuming A32 operation and that the VMEbus Address Register is NOT written to, the MIX_base address for Module 0 is 0x0000 0000. Making the same assumptions, Module 1's MIX_base address is 0x1000 0000 and the MIX_base address for Module 2 is 0x2000 0000.

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3.2 Address Map (continued)

3.2.2 Model 4272 Address Map for the Model 4202 Baseboard (continued)

Table 3-2: Model 4272 Memory Map for Use with Model 4202 MIX Baseboard

VMEbus Address	Symbolic Name	Resource
MIX_base+0x0000 0000	Control_Reg	Control Register
MIX_base+0x0000 0004	Status_Reg	Status Register (Read Only Access)
MIX_base+0x0000 0008	Harris_CntlA_MSB	Harris Channel A Control Register (MSB)
MIX_base+0x0000 000C	Harris_CntlA_LSB	Harris Channel A Control Register (LSB)
MIX_base+0x0000 0010	Harris_CntlB_MSB	Harris Channel B Control Register (MSB)
MIX_base+0x0000 0014	Harris_CntlB_LSB	Harris Channel B Control Register (LSB)
MIX_base+0x0000 0018	Mezz_Cntl_1	Mezz Control 1 Register
MIX_base+0x0000 001C	Mezz_Cntl_2	Mezz Control 2 Register
MIX_base+0x0000 0020	Harris_A_FIFO	Output FIFO Channel A (Read Only Access)
MIX_base+0x0000 0024	Harris_B_FIFO	Output FIFO Channel B (Read Only Access)
MIX_base+0x0000 0028	Graychip_FIFO	Output FIFO Channel C (Read Only Access)
MIX_base+0x0000 0040	GCC_Freq_Byte_0	Graychip Channel C Frequency Byte 0
MIX_base+0x0000 0044	GCC_Freq_Byte_1	Graychip Channel C Frequency Byte 1
MIX_base+0x0000 0048	GCC_Freq_Byte_2	Graychip Channel C Frequency Byte 2
MIX_base+0x0000 004C	GCC_Freq_Byte_3	Graychip Channel C Frequency Byte 3
MIX_base+0x0000 0050	GCC_Sync_Mode	Graychip Channel C Sync Mode Register
MIX_base+0x0000 0054	GCC_Filter_Mode	Graychip Channel C Filter Mode Register
MIX_base+0x0000 0058	GCC_Gain_Control	Graychip Channel C Gain Fraction Register
MIX_base+0x0000 005C	GCC_Gain_Exponent	Graychip Channel C Gain Exponent Register
MIX_base+0x0000 0060	GCC_Output_Mode	Graychip Channel C Output Mode Register
MIX_base+0x0000 0064	GCC_Output_Status	Graychip Channel C Output Status Register
MIX_base+0x0000 0068	GCC_One_Shot	Graychip Channel C One Shot Register
MIX_base+0x0000 006C	GCC_Checksum	Graychip Channel C Checksum Register
MIX_base+0x0000 0070	GCC_I_Output_Byte_0	Graychip Channel C **I** Output Byte 0 Register
MIX_base+0x0000 0074	GCC_I_Output_Byte_1	Graychip Channel C **I** Output Byte 1 Register
MIX_base+0x0000 0078	GCC_Q_Output_Byte_0	Graychip Channel C **Q** Output Byte 0 Register
MIX_base+0x0000 007C	GCC_Q_Output_Byte_1	Graychip Channel C **Q** Output Byte 1 Register

MIX base Address:
If 4272 is in MIX position 0, MIX_base=0x0000 0000 for A32, or 0x00 0000 for A24
If 4272 is in MIX position1, MIX_base= 0x1000 0000 for A32, or 0x10 0000 for A24
If 4272 is in MIX position 2, MIX_base=0x2000 0000 for A32, or 0x20 0000 for A24

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3.2 Address Map (continued)

3.2.2 Model 4272Address Map for the Model 4202 Baseboard (continued)

Table 3-2, page 30, presents the memory map for a Model 4272 installed on a Model 4202 Baseboard, assuming direct addressing, A32 or A24 operation, and that nothing has been written to the 4202's VME Address Register. For information about using the Model 4202's Paged Addressing Mode, A16 MIX access, multiple 4202's in the same card cage or Upper MIX Bus Masters, please refer to the Operating Manual for the Model 4202 Baseboard or the UMBM.

3.2.3 Model 4272 Address Map for the Model 4283 Baseboard

On the Model 4283 Baseboard, there are two levels of addressing: 1) selection of the particular expansion module by its stack position and 2) selection of one of the resources within the module.

3.2.3.1 Module Selection

The TMS320C30 selects among MIX Modules by using a two bit field in the Model 4283 Page Register, located at 'C30 address 0x0080 0002. These two bits select one of the three possible MIX stack positions according to Table 3-3, below.

Access to some resources on certain MIX modules may require that either or both of the MIX bus A27 (MX_A27) and A21 (MX_A21) bits be set to the logic '1' state. On the 4283 Baseboard, these bits are also contained in the Address Page Register. MX_A27 is the D17 bit of this register, and MX_A21 is the D14 bit. Table 3-3 also shows these bits.

Table 3-3: Model 4272 - Module Selection
-Model 4283 Page Register - 'C30 Address 0x0080 0002

Page Register Bits	D31-D38	D17	D16	D15	D14	D13-D0	Example
Stack Position 0	X	MX_A27	1	1	MX_A21	X	0x00001 8000
Stack Position 1	X		1	0		X	0x00001 0000
Stack Position 2	X		0	1		X	0x00000 8000
X = other functions							

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3.2 Address Map (continued)

3.2.3 Model 4272 Address Map for the Model 4283 Baseboard (continued)

3.2.3.2 Register Selection Within the Module

Once the module has been selected, all resources of the Model 4272 appear in the TMS320C30 address map according to Table 3-4. Accessing these registers is accomplished by simply reading and writing these locations.

The 24-bit addressing scheme accesses 32-bit data locations for the TMS320C30, even though many of the elements correspond to 8-bit or 16-bit devices.

Table 3-4: Model 4272 Memory Map for Use with Model 4283 MIX Baseboard

4283 'C30 Address	Symbolic Name	Resource
0x0080 4000	Control_Reg	Control Register
0x0080 4001	Status_Reg	Status Register (Read Only Access)
0x0080 4002	Harris_CntlA_MSB	Harris Channel A Control Register (MSB)
0x0080 4003	Harris_CntlA_LSB	Harris Channel A Control Register (LSB)
0x0080 4004	Harris_CntlB_MSB	Harris Channel B Control Register (MSB)
0x0080 4005	Harris_CntlB_LSB	Harris Channel B Control Register (LSB)
0x0080 4006	Mezz_Cntl_1	Mezz Control 1 Register
0x0080 4007	Mezz_Cntl_2	Mezz Control 2 Register
0x0080 4008	Harris_A_FIFO	Output FIFO Channel A (Read Only Access)
0x0080 4009	Harris_B_FIFO	Output FIFO Channel B (Read Only Access)
0x0080 400A	Graychip_FIFO	Output FIFO Channel C (Read Only Access)
0x0080 4010	GCC_Freq_Byte_0	Graychip Channel C Frequency Byte 0
0x0080 4011	GCC_Freq_Byte_1	Graychip Channel C Frequency Byte 1
0x0080 4012	GCC_Freq_Byte_2	Graychip Channel C Frequency Byte 2
0x0080 4013	GCC_Freq_Byte_3	Graychip Channel C Frequency Byte 3
0x0080 4014	GCC_Sync_Mode	Graychip Channel C Sync Mode Register
0x0080 4015	GCC_Filter_Mode	Graychip Channel C Filter Mode Register
0x0080 4016	GCC_Gain_Control	Graychip Channel C Gain Fraction Register
0x0080 4017	GCC_Gain_Exponent	Graychip Channel C Gain Exponent Register
0x0080 4018	GCC_Output_Mode	Graychip Channel C Output Mode Register
0x0080 4019	GCC_Output_Status	Graychip Channel C Output Status Register
0x0080 401A	GCC_One_Shot	Graychip Channel C One Shot Register
0x0080 401B	GCC_Checksum	Graychip Channel C Checksum Register
0x0080 401C	GCC_I_Output_Byte_0	Graychip Channel C **I** Output Byte 0 Register
0x0080 401D	GCC_I_Output_Byte_1	Graychip Channel C **I** Output Byte 1 Register
0x0080 401E	GCC_Q_Output_Byte_0	Graychip Channel C **Q** Output Byte 0 Register
0x0080 401F	GCC_Q_Output_Byte_1	Graychip Channel C **Q** Output Byte 1 Register

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3.2 Address Map (continued)

3.2.4 Model 4272 Address Map for the Model 4284 Baseboard

The Model 4284 Baseboard uses a TMS320C40 Digital Signal Processor to master transactions with the MIX bus. The three MIX module locations are each mapped into separate, 64 M-Longword regions of the 'C40's memory space. Module 0's MIX_base address in the 'C40 memory map is 0x2000 0000. The MIX_base address for Module 1 is 0x2400 0000, and the 'C40's MIX_base address for Module 2 is 0x2800 0000. Table 3-5, below, presents the memory map for the twenty-seven resources on the Model 4272, as seen by the 'C40 processor on the Model 4284 Baseboard.

Table 3-5: Model 4272 Memory Map for Use with the Model 4284 MIX Baseboard

4284 'C40 Address	Symbolic Name	Resource
MIX_base+0x0000 0000	Control_Reg	Control Register
MIX_base+0x0000 0001	Status_Reg	Status Register (Read Only Access)
MIX_base+0x0000 0002	Harris_CntlA_MSB	Harris Channel A Control Register (MSB)
MIX_base+0x0000 0003	Harris_CntlA_LSB	Harris Channel A Control Register (LSB)
MIX_base+0x0000 0004	Harris_CntlB_MSB	Harris Channel B Control Register (MSB)
MIX_base+0x0000 0005	Harris_CntlB_LSB	Harris Channel B Control Register (LSB)
MIX_base+0x0000 0006	Mezz_Cntl_1	Mezz Control 1 Register
MIX_base+0x0000 0007	Mezz_Cntl_2	Mezz Control 2 Register
MIX_base+0x0000 0008	Harris_A_FIFO	Output FIFO Channel A (Read Only Access)
MIX_base+0x0000 0009	Harris_B_FIFO	Output FIFO Channel B (Read Only Access)
MIX_base+0x0000 000A	Graychip_FIFO	Output FIFO Channel C (Read Only Access)
MIX_base+0x0000 0010	GCC_Freq_Byte_0	Graychip Channel C Frequency Byte 0
MIX_base+0x0000 0011	GCC_Freq_Byte_1	Graychip Channel C Frequency Byte 1
MIX_base+0x0000 0012	GCC_Freq_Byte_2	Graychip Channel C Frequency Byte 2
MIX_base+0x0000 0013	GCC_Freq_Byte_3	Graychip Channel C Frequency Byte 3
MIX_base+0x0000 0014	GCC_Sync_Mode	Graychip Channel C Sync Mode Register
MIX_base+0x0000 0015	GCC_Filter_Mode	Graychip Channel C Filter Mode Register
MIX_base+0x0000 0016	GCC_Gain_Control	Graychip Channel C Gain Fraction Register
MIX_base+0x0000 0017	GCC_Gain_Exponent	Graychip Channel C Gain Exponent Register
MIX_base+0x0000 0018	GCC_Output_Mode	Graychip Channel C Output Mode Register
MIX_base+0x0000 0019	GCC_Output_Status	Graychip Channel C Output Status Register
MIX_base+0x0000 001A	GCC_One_Shot	Graychip Channel C One Shot Register
MIX_base+0x0000 001B	GCC_Checksum	Graychip Channel C Checksum Register
MIX_base+0x0000 001C	GCC_I_Output_Byte_0	Graychip Channel C **I** Output Byte 0 Register
MIX_base+0x0000 001D	GCC_I_Output_Byte_1	Graychip Channel C **I** Output Byte 1 Register
MIX_base+0x0000 001E	GCC_Q_Output_Byte_0	Graychip Channel C **Q** Output Byte 0 Register
MIX_base+0x0000 001F	GCC_Q_Output_Byte_1	Graychip Channel C **Q** Output Byte 1 Register
If 4272 is in MIX position 0, MIX_base = 0x2000 0000 If 4272 is in MIX position 1, MIX_base = 0x2400 0000 If 4272 is in MIX position 2, MIX_base = 0x2800 0000		

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3.2 Address Map (continued)

3.2.4 Model 4272 Address Map for the Model 4284 Baseboard (continued)

This Baseboard also supports mastering of the MIX bus by processor modules in the MIX stack, known as UMBM's (Upper MIX Bus Masters). For further details on this type of transaction, please refer to the MIX Tutorial for VME-Bus Systems (Manual Part Number 800.00001).

3.2.5 Model 4272 Address Map for the Model 4285 MIX Baseboard Adapter

When the Model 4285 is equipped with one of the MIX Expansion Bus Adapters (Options 031 or 036) all eight of its 'C40 processors can access modules on the MIX bus via the 4285's Main Bus. Additionally, four of the processors (A, B, E and F) have a separate access path to devices on the MIX bus via their Global I/O expansion ports. Separate control registers are provided for each of these five interfaces to the MIX bus. Two addressing modes, Normal and Compressed, are available for any of these access paths.

Table 3-6, page 35, presents the memory map for the slave resources on the Model 4272, as seen by the 'C40 processors on the Model 4285 Baseboard. The table also provides the MIX_Base addresses, in the memory spaces of the 'C40 processors, for the Expansion bus and Global I/O access paths. For further information on the use of the 4285 as a MIX baseboard, including VME access to MIX resources on the 4285, please refer to the Model 4285 MIX Baseboard Adapter Operating Manual, Pentek part #800.42851.

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3.2 Address Map (continued)

3.2.5 Model 4272 Address Map for the Model 4285 MIX Baseboard Adapter (continued)

Table 3-6: Model 4272 Memory Map for Use with the Model 4285 MIX Baseboard

4285 'C40 Address	Symbolic Name	Resource
MIX_base+0x0000 0000	Control_Reg	Control Register
MIX_base+0x0000 0001	Status_Reg	Status Register (Read Only Access)
MIX_base+0x0000 0002	Harris_CntlA_MSB	Harris Channel A Control Register (MSB)
MIX_base+0x0000 0003	Harris_CntlA_LSB	Harris Channel A Control Register (LSB)
MIX_base+0x0000 0004	Harris_CntlB_MSB	Harris Channel B Control Register (MSB)
MIX_base+0x0000 0005	Harris_CntlB_LSB	Harris Channel B Control Register (LSB)
MIX_base+0x0000 0006	Mezz_Cntl_1	Mezz Control 1 Register
MIX_base+0x0000 0007	Mezz_Cntl_2	Mezz Control 2 Register
MIX_base+0x0000 0008	Harris_A_FIFO	Output FIFO Channel A (Read Only Access)
MIX_base+0x0000 0009	Harris_B_FIFO	Output FIFO Channel B (Read Only Access)
MIX_base+0x0000 000A	Graychip_FIFO	Output FIFO Channel C (Read Only Access)
MIX_base+0x0000 0010	GCC_Freq_Byte_0	Graychip Channel C Frequency Byte 0
MIX_base+0x0000 0011	GCC_Freq_Byte_1	Graychip Channel C Frequency Byte 1
MIX_base+0x0000 0012	GCC_Freq_Byte_2	Graychip Channel C Frequency Byte 2
MIX_base+0x0000 0013	GCC_Freq_Byte_3	Graychip Channel C Frequency Byte 3
MIX_base+0x0000 0014	GCC_Sync_Mode	Graychip Channel C Sync Mode Register
MIX_base+0x0000 0015	GCC_Filter_Mode	Graychip Channel C Filter Mode Register
MIX_base+0x0000 0016	GCC_Gain_Control	Graychip Channel C Gain Fraction Register
MIX_base+0x0000 0017	GCC_Gain_Exponent	Graychip Channel C Gain Exponent Register
MIX_base+0x0000 0018	GCC_Output_Mode	Graychip Channel C Output Mode Register
MIX_base+0x0000 0019	GCC_Output_Status	Graychip Channel C Output Status Register
MIX_base+0x0000 001A	GCC_One_Shot	Graychip Channel C One Shot Register
MIX_base+0x0000 001B	GCC_Checksum	Graychip Channel C Checksum Register
MIX_base+0x0000 001C	GCC_I_Output_Byte_0	Graychip Channel C **I** Output Byte 0 Register
MIX_base+0x0000 001D	GCC_I_Output_Byte_1	Graychip Channel C **I** Output Byte 1 Register
MIX_base+0x0000 001E	GCC_Q_Output_Byte_0	Graychip Channel C **Q** Output Byte 0 Register
MIX_base+0x0000 001F	GCC_Q_Output_Byte_1	Graychip Channel C **Q** Output Byte 1 Register

MIX base Address for Expansion Bus	**MIX base Address for Global I/O Bus**
If 4272 is in MIX position 0, MIX_base = 0x9000 0000	If 4272 is in MIX position 0, MIX_base = 0xC800 0000
If 4272 is in MIX position 1, MIX_base = 0x9020 0000	If 4272 is in MIX position 1, MIX_base = 0xC820 0000
If 4272 is in MIX position 2, MIX_base = 0x9040 0000	If 4272 is in MIX position 2, MIX_base = 0xC840 0000

Note: MXA27 is asserted via page bit 2 in Normal addressing mode, or via 'C40 address bit GA20 in Compressed addressing mode

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3.3 Control Register - Read/Write @ Address Control_Reg

The Model 4272 Control Register contains interrupt mask bits, reset control bits, and data packing bits for each receiver channel. It also has bits that launch the command shift cycle for the Harris chips, and overflow and sync control bits for the Graychip. Table 3-7, below, shows the function of each bit.

Table 3-7: Model 4272 - Control Register - Read/Write @ Control_Reg

Ch. C Bits	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**
Function	N/U	Harris B Input Source	Harris C Input Source	N/U	Graychip Software Gain Sync	Graychip Software Sys Sync	Graychip Software Accum Sync	Graychip Sync Source
Logic '1' **Logic '0'**	- -	C Input B Input	C Input A Input	- -	Run Set Gain	Run Sync	Run Set Freq.	Front Panel Software
Ch. C Bits	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
Function	Interrupt Mask Bits					Packed Data Mode	Front Panel Output	Graychip FIFO Reset
	FIFO FULL	FIFO Half Full	FIFO Not Empty	Overflow Flag	Graychip Interrupt			
Logic '1' **Logic '0'**	Enabled Disabled	Enabled Disabled	Enabled Disabled	Enabled Disabled	Enabled Disabled	Disabled Enabled	Enabled Disabled	Release Reset
Ch. B Bits	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Ch. A Bits	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Function	Interrupt Mask Bits			Packed Data Mode	Command Shift Mode	Harris Reset Source	Harris Internal Reset	Harris FIFO Reset
	FIFO FULL	FIFO Half Full	FIFO Not Empty					
Logic '1' **Logic '0'**	Enabled Disabled	Enabled Disabled	Enabled Disabled	Disabled Enabled	Start Shift Release	External Internal	Reset Release	Release Reset

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3.3 **Control Register** (continued)

The Control Register is cleared to logic '0' in all bit positions after reset.

The Control Register is a read/write device, and uses all bits of the 32-bit MIX bus word. Two identically-arranged 8-bit groups, D0 - D7 and D8 - D15, are concerned with functions of the Harris Chips in channels A and B. The upper 16 bits mainly pertain to the Graychip in channel C. Each of the bits of the Control Register will be described below.

3.3.1 **FIFO Reset -** Bits D0 (Ch. A), D8 (Ch. B), and D16 (Ch. C)

These bits are used to reset all functions within the associated FIFO memories. This is useful when initializing the module and in recovering from any error condition. When this bit is cleared to the logic '0' state, the associated FIFO is cleared of all data. Also, in the Status Register (see XREF) the Empty flag for the associated FIFO is set true (i. e., cleared to the logic '0' state), and the Half-Full and Full flags for the associated FIFO are set false (i. e., set to the logic '1' state). When this bit is set to the logic '1' state, the FIFO is released for accepting data.

3.3.2 **Harris Chip Internal Reset -** D1 (Ch. A) and D9 (Ch. B)

Setting either of these bits to the logic '1' state causes the indicated Harris chip to execute an internal reset cycle. The chip will be held in the reset state as long as the bit remains high. Clear the bit back to the logic '0' state to release the Harris drop receiver chip for operation.

Note that a channel's Reset Source bit (see Section 3.3.3, below) must be programmed for Internal Reset (i. e., cleared to logic '0') for that channel's internal reset bit to function.

3.3.3 **Harris Chip Reset Source** - D2 (Ch. A) and D10 (Ch. B)

These two bits determine whether the Harris Chips will generate their own (software) reset, or will respond to an externally generated reset signal. This reset synchronously initializes all of the chip's internal functions. Clearing either of these bits to the logic '0' state enables the software reset function for the indicated device. In this case, clearing the Internal Reset bit (see Section 3.3.2, above) will initiate a reset in the Harris chip. If either of these bits is set to the logic '1' state, that Harris chip will be reset by an external signal applied at that channel's front panel System Sync (SS) input pin.

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3.3 **Control Register** (continued)

3.3.4 **Harris Command Shift Mode** - D3 (Ch. A) and D11 (Ch. B)

The operating modes of the Harris chips are determined by the contents of their internal control registers (refer to Appendix C of this manual, which is the Harris HSP50016 manual, for further details). Each Harris chip contains seven 40-bit control registers. The desired control words are loaded into the chip's registers via a serial interface, and are shifted in MSB first. The control word address occupies the three MSBs of the control word.

On the Model 4272, the desired control word is written by the MIX bus Master into a pair of registers (for Channel A, symbolic address Harris_CntlA_MSB holds the 8 MSBs of the control word, and Harris_CntlA_LSB holds the 32 LSBs; for Channel B, the 8 MSBs go in Harris_CntlB_MSB, and the 32 LSBs in Harris_CntlB_LSB). After loading the proper registers with the desired control word, set this bit to the '1' state and poll the Shift Mode bit in the Status Register (D4 for Ch. A, D12 for Ch. B at symbolic address Status_Reg) to determine when the shift process is complete.

The status bit will remain in the '1' state while the serial shift is in progress, and will return to the '0' state when the shift is completed and the device is ready for operation. (These bits must remain in the '0' state for normal drop receiver operation in their respective channels.) The shift process takes around one millisecond (1 msec) to complete. When trying to modify settings while acquiring data, waiting for the shift to complete will result in a loss of data. The wait may be bypassed in this case.

3.3.5 **Packed Data Mode** - Bits D4 (Ch. A), D12 (Ch. B), and D18 (Ch. C)

In Packed Data Mode, the 16-bit I (In-phase or Real) and Q (Quadrature or Imaginary) output data samples are placed in the same 32-bit word in the output FIFO. This operating mode is enabled for a given channel by clearing the indicated bit to the '0' state. This is the state that this bit is left in after a reset.

The data samples are actually formatted for either packed or unpacked mode in registers that follow the FIFO in the output data path. For details on the format in which the data will appear when the FIFO is read, please refer to Section 3.4.7 (Reading the Output Data FIFOs).

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3.3 **Control Register** (continued)

3.3.6 **Front Panel Output** - Bit D17 (Ch. C only)

For the Model 4272's wideband channel (channel C) only, the output data delivered by the FIFO may be output either on the front panel connector, or on the MIX bus. Front panel output is enabled when this bit is set to the logic '1' state. The FIFO Full, Half-Full and Empty flag outputs are also available at the front panel connector in this mode.

When front panel output is enabled, the FIFO Read and Reset inputs are delivered from the front panel connector, rather than over the MIX bus.

When this bit is cleared to the logic '0' state, FIFO output data and flags are only available over the MIX bus, and the MIX bus Master has control of the FIFO Read and Reset inputs.

3.3.7 **Interrupt Mask Bits**

The bits described in the subsections below are all used to allow certain events or status flags to generate an interrupt to a MIX bus Baseboard or Upper MIX bus Master. In all cases, set the indicated bit to the '1' state to allow the stated condition to cause an interrupt. (Interrupts generated by this module are cleared by reading the Status Register, see Section 3.4.) Leaving these bits in their default (cleared or logic '0') state will prevent (or mask) these events from creating interrupts.

3.3.7.1 Graychip Interrupt - Bit D19 (Ch. C only)

When this bit is set to the logic '1' state, the GC1012's Interrupt output is passed along as a MIX bus Interrupt. Refer to Appendix D of this manual (the GC1012 Manual) for information about enabling this output on the Graychip, and circumstances that will cause the chip's Interrupt output to go true.

3.3.7.2 Graychip Overflow Flag -Bit D20 (Ch. C only)

When this bit is set to the logic '1' state, a MIX bus Interrupt will be generated when the GC1012's Overflow output goes true. Refer to Appendix D of this manual (the GC1012 Manual) for information about enabling this output on the Graychip, and circumstances that will cause the chip's Overflow output to go true.

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3.3 Control Register (continued)

3.3.7 Interrupt Mask Bits (continued)

3.3.7.3 FIFO Not Empty- Bits D5 (Ch. A), D13 (Ch. B) and D21 (Ch. C)

When one of these bits is set to the logic '1' state, a MIX bus Interrupt will be generated whenever data becomes available in the indicated channel's output FIFO (i. e., when the FIFO Empty flag goes FALSE). It indicates that at least one sample is available for readout.

3.3.7.4 FIFO Half Full - Bits D6 (Ch. A), D14 (Ch. B) and D22 (Ch. C)

When one of these bits is set to the logic '1' state, a MIX bus Interrupt will be generated when the output FIFO's Half-full flag for the indicated channel goes true. This interrupt is often used to trigger the FIFO readout routine.

3.3.7.5 FIFO Full - Bits D7 (Ch. A), D15 (Ch. B) and D23 (Ch. C)

When one of these bits is set to the logic '1' state, a MIX bus Interrupt will be generated when the output FIFO's Full flag for the indicated channel goes true. This implies a strong probability that data has been lost.

3.3.8 Graychip Sync Source - Bit D24 (Ch. C only)

This bit is used to select the source for the SS, GS and AS signals for the GC1012 to be either the software sync bits (bits D27 - D25 in this register, see below) or the signals presented to the front panel digital input connector pins. A logic '0' in this bit selects the software (internal) mode, and a logic '1' selects the hardware (external) path.

3.3.9 Graychip Software Accumulator Sync - Bit D25 (Ch. C only)

This bit can be used as the source for the AS signal for the GC1012 when the Sync Source bit (see Section 3.3.8) is set to the logic '1' state. This bit is presented with an inversion to the AS pin of the GC1012, and is registered by a rising clock edge. The function of this input is described in the GC1012 Manual in Appendix D.

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3.3 Control Register (continued)

3.3.10 Graychip Software System Sync - Bit D26 (Ch. C only)

This bit can be used as the source for the SS signal for the GC1012 when the Sync Source bit (see Section 3.3.8) is set to the logic '1' state. This bit is presented with an inversion to the SS pin of the GC1012, and is registered by a rising clock edge. The function of this input is described in the GC1012 Manual in Appendix D.

3.3.11 Graychip Software Gain Sync - Bit D27 (Ch. C only)

This bit can be used as the source for the GS signal for the GC1012 when the Sync Source bit (see Section 3.3.8) is set to the logic '1' state. This bit is presented with an inversion to the GS pin of the GC1012, and is registered by a rising clock edge. The function of this input is described in the GC1012 Manual in Appendix D.

3.3.12 Harris Input Source Selects - Bits D29 (Ch. A) and D30 (Ch. B)

When one of these bits is set to the logic '1' state, the indicated channel will use the channel C front panel input connector as its input data source. When these bits are in their default (cleared or logic '0') states, the channels obtain their input signals from their own front panel connectors.

3.4 Status Register - Read Only @ Address Status_Reg

The Status Register is a read-only register used to monitor various conditions within the Model 4272. It is useful in servicing interrupts and in software routines for polled operations. Reading the Status Register clears any pending interrupt from this module. Table 3-8, below, shows the function of each bit.

Table 3-8: Model 4272 - Status Register - Read Only @ Status_Reg

Ch. C Bits	D23	D22	D21	D20	D19	D18	D17	D16
Function	Not Used	Timeout Clock	Not Used	Overflow	FIFO FULL	FIFO Half Full	FIFO Empty	Data Type
Logic '1'	-	Timeout	-	False				
Logic '0'	-	OK	-	True				
Ch. B Bits	D15	D14	D13	D12	D11	D10	D9	D8
Ch. A Bits	D7	D6	D5	D4	D3	D2	D1	D0
Function	Not Used		Timeout Clock	Shift Mode	FIFO FULL	FIFO Half Full	FIFO Empty	Data Type
Logic '1'	-		Timeout	Shifting	False			
Logic '0'	-		OK	Ready	True			

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3.4 **Status Register** (continued)

The Status Register uses 18 bits of the 32-bit MIX bus word. It is arranged as three nearly identical 6-bit groups, each group pertaining to one of the three channels. Note that the corresponding bit numbers for each group are shown in columns above the function description. The upper byte of this register (D24 - D31) is unused.

All of the bits in the Status Register reflect the current state of each condition and are determined by the logic levels on the corresponding pins of the FIFOs and the receiver chips. None of these bits is latched in hardware external to these devices.

Each of the Status Register bits will be described in the subsections below.

3.4.1 **Data Type** - Bits D0 (Ch. A), D8 (Ch. B) and D16 (Ch. C)

When operating in the complex mode, the drop receiver chip produces inter-leaved samples for real and imaginary values. The Data Type bit can be used to determine whether the most recent write to the FIFO was a Real (In-Phase or 'I') sample or an Imaginary (Quadrature or 'Q') sample.

Unfortunately, the interpretation of these bits is not as straightforward as one might hope. The state of these bits depends not only on whether the last sample written to the FIFO was real or Imaginary, but also on whether or not the module is operating in Packed Data mode, and on whether the bit in question is for the Graychip or a Harris chip. Table 3-9, below, tells how the contents of these bits are interpreted. See the drop receiver chip manuals in Appendices C and D for more details.

Table 3-9: Model 4272 -Data Type Bits

Harris Chips **D0 (ch. A) & D8 (ch. B)**	**Non-Packed** **Data Mode**	**Packed** **Data Mode**
Real (I) Sample	0	1
Imaginary (Q) Sample	1	0
Graychip **D16 (Ch.C)**	**Non-Packed** **Data Mode**	**Packed** **Data Mode**
Real (I) Sample	0	1
Imaginary (Q) Sample	1	0

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3.4 **Status Register** (continued)

3.4.2 **FIFO Empty** - Bits D1 (Ch. A), D9 (Ch. B) and D17 (Ch. C)

These bits reflect the current levels of their channels' FIFO Empty Flags. When one of these bits is in the logic '0' (true) state, its FIFO is empty. When one of these bits is in the logic '1' state, there is at least one sample in that FIFO.

Note that in Packed Mode, if there is only one sample in the FIFO, the read will not complete until a second sample is placed in the FIFO. (Remember that in Packed mode, one read delivers two samples.)

3.4.3 **FIFO Half Full** - Bits D2 (Ch. A), D10 (Ch. B) and D18 (Ch. C)

These bits reflect the current levels of their channels' FIFO Half Full Flags. When one of these bits is in the logic '0' (true) state, its FIFO is at least half full. When one of these bits is in the logic '1' state, that FIFO is less than half full. These bits can be used to insure that a data read from the FIFO for up to half the FIFO depth is possible. For example, for a 1k sample FIFO, if this bit is at logic '0', at least 512 samples can be read.

3.4.4 **FIFO Full** - Bits D3 (Ch. A), D11 (Ch. B) and D19 (Ch. C)

These bits reflect the current levels of their channels' FIFO Full Flags. When one of these bits is in the logic '0' (true) state, its FIFO is full. When one of these bits is in the logic '1' state, that FIFO is not full. These bits can be used to insure that data reads from the FIFO for the entire FIFO depth are allowed.

3.4.5 **Harris Shift Mode** - Bits D4 (Ch. A) and D12 (Ch. B)

When one of these bits is in the logic '1' state, the Harris receiver in the indicated channel is in process of shifting in one or more control word(s), to change the device's operating parameters. Shift Mode is initiated by writing a '1' to bit D3 of the Control Register (address Control_Reg 0x0000 0000) for channel A, or bit D11 for channel B. When the bit returns to the logic '0' state, the Harris receiver is ready for operation. The shift operation takes about 1 msec. If you are trying change settings 'on the fly' (i. e., while acquiring data), waiting for the shift to complete will result in a loss of data. In such a case, start the shift and resume data taking without polling this bit.

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3.4 Status Register (continued)

3.4.6 Graychip Overflow - Bit D20 (Ch. C only)

This bit reflects the current level of the GC1012's Overflow Flag. When this bit is in the logic '0' (true) state, an overflow condition has occurred (see Appendix D of this manual, the GC1012 Manual, for further details). When this bit is in the logic '1' (false) state, no overflow has occurred.

3.4.7 Timeout Clock Status - Bits D5 (Ch. A), D13 (Ch. B) and D22 (Ch. C)

A logic '1' in any of these bits indicates that the drop receiver in the channel in question can no longer detect the clock signal applied to the front panel for that channel. A logic '0' in any of these bits means that the associated receiver can see its clock.

3.5 Reading the Output Data FIFOs

The Packed Data Mode bits in the Control Register (D4, D12, and D18 for channels A, B and C, respectively) determine how the output data appears on the MIX bus. See Section 3.3.5 for a description of the use of these bits. As shown in Table 3-10, below, the most significant bit (msb) of each output word appears in D31 or D15 bit position, and the least significant bit (lsb) appears in the D16 or D0 bit position.

When you are reading Complex data in packed mode, each 32-bit FIFO read produces a 16-bit 'I' sample in the high word (D31 - D16) and a 16-bit 'Q' sample in the low word (D15 - D0). When reading complex data in non-packed mode, the first 32-bit read (and all subsequent odd reads) will deliver a 16 bit 'I' sample in the low word, and the second read (and all subsequent even reads) will deliver a 16-bit 'Q' sample in the low word. Table 3-10, summarizes the above information. In Complex, Non-packed mode, data in the high word should be ignored.

Table 3-10: Model 4272 - Packed Mode Data Addressing, Complex Mode

Packed Mode			Non-Packed Mode	
Symbolic Address	D31 ------- D16 msb lsb	D15 ------- D0 msb lsb	Next Read D15 ------- D0	1st Read D15 ------- D0
Graychip_FIFO	Channel C (I)	Channel C (Q)	Channel C (Q)	Channel C (I)
Harris_B_FIFO	Channel B (I)	Channel B (Q)	Channel B (Q)	Channel B (I)
Harris_A_FIFO	Channel A (I)	Channel A (Q)	Channel A (Q)	Channel A (I)

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3.5 Reading the Output Data FIFOs (continued)

When the 4272 is operating in Real mode (i. e., taking only 'I' samples), the distribution of data samples is dependent upon both the state of data packing and which type of receiver chip is delivering the data. When reading real data from the Graychip in Packed mode, all 32 bits contain valid data, and the earlier sample is in the high word (D31 - D16). When reading real data from the Graychip in Non-packed mode, the upper 16 bits of each read will contain a valid sample, and the lower 16 bits should be discarded. When reading real data from a Harris chip in Packed mode, the upper 16 bits of each read will contain a valid sample, and the lower 16 bits should be discarded. When reading real data from a Harris chip in Non-packed mode, the upper 16 bits of the first read (and all subsequent odd reads) will contain a valid sample. Data contained in the lower 16 bits of each odd read, and in all 32 bits of each even read, should be discarded. The above information is summarized in Table 3-11, below.

Table 3-11: Model 4272 - Packed Mode Data Addressing, Real Mode

	Packed Mode		Non-Packed Mode	
Mix Address	D31 ------- D16 msb lsb	D15 ------- D0 msb lsb	Next Read D31 ------- D16	1st Read D31 ------- D16
Graychip_FIFO	Ch. C, Sample 0	Ch. C, Sample 1	Ch. C, Sample 1	Ch. C, Sample 0
Harris_B_FIFO	Ch. B Sample	Discard	Discard (D31 - D0)	Ch. B Sample
Harris_A_FIFO	Ch. A Sample	Discard	Discard (D31 - D0)	Ch. A Sample

It is worth noting at this point that the actual process of formatting the output data in Packed or Non-packed mode occurs in registers that follow the FIFOs in the output data path. Samples are placed in these 32-bit registers by separate 16-bit FIFOs. Each FIFO has its own Full, Half-Full and Empty flags that can be polled by reading the Status Register (see Section 3.4), or can trigger an interrupt when true if enabled by the Interrupt Mask bits in the Control Register (see Section 3.3.7). If the Empty flag for a given channel is true, and an attempt is made to read data from that channel's FIFO over the MIX bus, a MIX_Wait will hold off the read operation until a sample is available. If the Full Flag for a given channel goes true, then it is likely that some data has been lost in that channel. These registers cannot be read consecutively in less than 240 nanoseconds. FIFO access can be slowed down by placing some NOP commands after each FIFO read or by using repeated register stores to the same location between FIFO reads.

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3.6 HSP50016 Registers - R/W @ Harris_CntlA_MSB through Harris_CntlB_LSB

The HSP50016 Narrowband Drop Receiver chips in the Model 4272 are programmed by serially shifting in up to seven 40-bit control words via the control input. For any given control word, the three most significant bits indicate which of the seven HSP50016 control registers the word is meant for. Please refer to the HSP50016 Manual, in Appendix C of this manual, for details about the seven control registers in these devices and their functions.

On the Model 4272, the desired control word(s) for a given channel are written to a pair of registers. The contents of these registers are then transferred to a parallel-input shift register for transfer to the receiver chip. For Channel A, the 8 MSBs of a control word are written to MIX_base+0x0000 0008 (addresses given in this section assume that a byte-addressed baseboard is in use), and the 32 LSBs of a Channel A control word are written to MIX_base+0x0000 000C. For Channel B, the 8 MSBs go in MIX_base+0x0000 0010, and the 32 LSBs go in MIX_base+0x0000 0014. The shift process takes around 1 msec to complete. The Shift Mode bits in the Status Register (D4 for ch. A and D12 for ch. B, at MIX_base+0x0000 0004, see Section 3.4.5) can be polled to determine when the shift operation is finished. When trying to modify settings while acquiring data, waiting for the shift to complete will result in a loss of data. The polling operation may be bypassed in this case.

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3.7 GC1012 Registers - Read/Write @ GCC_Freq_Byte_0 through GCC_Q_Output_Byte_1

The GC1012 wideband receiver has 16 internal registers for control and status of this device. Each register is mapped into a separate MIX address in a contiguous region from MIX_base+0x0000 0040 through MIX_base+0x0000 007C (assuming a byte-addressed baseboard, see the MIX Address Maps in Section 3.2). Note again that each register is mapped on 4-byte address boundaries (last digit of MIX address is 0, 4, 8, or C).

The address of each of these registers (again, assuming a byte-addressed baseboard) is shown in Table 3-12, below. A complete description of each register and its functions is given in the GC1012 Manual in Appendix D.

Table 3-12: Model 4272 - GC1012 Register Addressing Map

Mix_base +	Reg #	Register Description
0x0000 007C	15	Q-Output Byte1
0x0000 0078	14	Q-Output Byte 0
0x0000 0074	13	I-Output Byte 1
0x0000 0070	12	I-Output Byte 0
0x0000 006C	11	Checksum Register
0x0000 0068	10	One-Shot Address
0x0000 0064	9	Output Status Register
0x0000 0060	8	Output Mode Register
0x0000 005C	7	Gain Exponent Register
0x0000 0058	6	Gain Control Register
0x0000 0054	5	Flitter Mode Register
0x0000 0050	4	Sync Mode Register
0x0000 004C	3	Frequency Byte 3 (most sig byte)
0x0000 0048	2	Frequency Byte 2
0x0000 0044	1	Frequency Byte 1
0x0000 0040	0	Frequency Byte 0 (least sig byte)

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Appendix A: Programming Examples

A.1 Introduction

The sections that follow present nine program segments that allow a Model 4272, mounted on any of Pentek's MIX Baseboards, to acquire real or complex data from an input source. Once data has been acquired a radix 4 complex FFT is computed and formatted for display.

Two header files are included, 4272.h, which defines constants specific to the 4272, and mod.h, which determines the MIX Module's base address based on the processor which is running the program, the MIX Baseboard, and the MIX stack position(s) of the 4272 (and the processor module that may be in use). Two different main programs are included; p4272r.c, for acquiring and processing real data, and p4272c.c, for acquiring and processing complex data. Each of these contains routines for initialization and synchronization of the receiver module, in addition to the data acquisition routines. The data transfer process may controlled be by one of two methods, polling or interrupts. If interrupts are used, intr.c decides from the information contained in mod.h which MIX Interrupt should be enabled by the processor.

The function process.c performs the FFT, by making calls to the assembly language routines fft_c4.asm and util.asm. Finally, the function display.c performs scaling on the data returned by the FFT routine.

A.2 Model 4272 Programming Examples

The remainder of this appendix contains programming examples for the Model 4272 which include:

- ❑ 4272.h Page A-3
- ❑ mod.h Page A-6
- ❑ p4272c.c Page A-9
- ❑ p4272r.c Page A-23
- ❑ process.c Page A-37
- ❑ display.c Page A-39
- ❑ intr.c Page A-40
- ❑ fft_c4.asm Page A-45
- ❑ util.asm Page A-51

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```
/* 4272.h  - This file contains 4272 module specific information */

#ifndef P4272_H
#define P4272_H

#define P4272_NB_FIFO_SIZE         (1 * 1024)     /* Narrowband */
#define P4272_WB_FIFO_SIZE         (16 * 1024)    /* Wideband   */

/* 4272 Mix Module Register Offsets */
#define P4272_CONTROL_REG       0x00000000L
#define P4272_STATUS_REG        0x00000001L
#define P4272_HARRIS_CNTLA_MSB  0x00000002L
#define P4272_HARRIS_CNTLA_LSB  0x00000003L
#define P4272_HARRIS_CNTLB_MSB  0x00000004L
#define P4272_HARRIS_CNTLB_LSB  0x00000005L
#define P4272_MEZZ_CNTL_1       0x00000006L
#define P4272_MEZZ_CNTL_2       0x00000007L
#define P4272_HARRIS_A_FIFO     0x00000008L
#define P4272_HARRIS_B_FIFO     0x00000009L
#define P4272_GRAYCHIP_FIFO     0x0000000aL
#define P4272_GRAYCHIP_REG_0    0x00000010L  /* 1st of 16 Registers */

/* Definitions of Gray Chip Channel Registers - Each channel has 16 Registers
*/
/* The Constant are offsets from P4272_GRAYCHIP_REG_0
*/
#define CH_FREQ_BYTE_0          0x00000000L  /* LSB */
#define CH_FREQ_BYTE_1          0x00000001L
#define CH_FREQ_BYTE_2          0x00000002L
#define CH_FREQ_BYTE_3          0x00000003L  /* MSB */
#define CH_SYNC_MODE            0x00000004L
#define CH_FILTER_MODE          0x00000005L
#define CH_GAIN_CONTROL         0x00000006L
#define CH_GAIN_EXPONENT        0x00000007L
#define CH_OUTPUT_MODE          0x00000008L
#define CH_OUTPUT_STATUS        0x00000009L
#define CH_ONE_SHOT             0x0000000aL
#define CH_CHECKSUM             0x0000000bL
#define CH_I_OUTPUT_BYTE_0      0x0000000cL
#define CH_I_OUTPUT_BYTE_1      0x0000000dL
#define CH_Q_OUTPUT_BYTE_0      0x0000000eL
#define CH_Q_OUTPUT_BYTE_1      0x0000000fL

/* Constants specific to each 4272 Register */

/* Status Register */

#define SR_DATA_TYPE_A          0x00000001L
#define SR_FIFO_EMPTY_A         0x00000002L
#define SR_FIFO_HALF_FULL_A     0x00000004L
#define SR_FIFO_FULL_A          0x00000008L
#define SR_SHIFT_MODE_A         0x00000010L
#define SR_TIMEOUT_CLOCK_A      0x00000020L
```

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```
#define SR_DATA_TYPE_B          0x00000100L
#define SR_FIFO_EMPTY_B         0x00000200L
#define SR_FIFO_HALF_FULL_B     0x00000400L
#define SR_FIFO_FULL_B          0x00000800L
#define SR_SHIFT_MODE_B         0x00001000L
#define SR_TIMEOUT_CLOCK_B      0x00002000L

#define SR_DATA_TYPE_C          0x00010000L
#define SR_FIFO_EMPTY_C         0x00020000L
#define SR_FIFO_HALF_FULL_C     0x00040000L
#define SR_FIFO_FULL_C          0x00080000L
#define SR_OVERFLOW             0x00100000L
#define SR_TIMEOUT_CLOCK_C      0x00200000L

/* Possible Data Types */

#define HR_PACKED_REAL_I_DATA_A     SR_DATA_TYPE_A
#define HR_PACKED_IMAG_Q_DATA_A     0L

#define HR_UNPACKED_REAL_I_DATA_A   0L
#define HR_UNPACKED_IMAG_Q_DATA_A   SR_DATA_TYPE_A

#define HR_PACKED_REAL_I_DATA_B     SR_DATA_TYPE_B
#define HR_PACKED_IMAG_Q_DATA_B     0L

#define HR_UNPACKED_REAL_I_DATA_B   0L
#define HR_UNPACKED_IMAG_Q_DATA_B   SR_DATA_TYPE_B

#define GC_PACKED_REAL_I_DATA_C     0L
#define GC_PACKED_IMAG_Q_DATA_C     SR_DATA_TYPE_C

#define GC_UNPACKED_REAL_I_DATA_C   SR_DATA_TYPE_C
#define GC_UNPACKED_IMAG_Q_DATA_C   0L

/* Control Register  */

#define CR_FIFO_RELEASE_A       0x00000001L
#define CR_HR_INT_RST_A         0x00000002L
#define CR_HR_RST_SRC_A         0x00000004L
#define CR_HR_SHIFT_MD_A        0x00000008L
#define CR_HR_UNPACK_DATA_A     0x00000010L
#define CR_HR_FIFO_NOT_EMPTY_A  0x00000020L
#define CR_HR_FIFO_HALF_FULL_A  0x00000040L
#define CR_HR_FIFO_FULL_A       0x00000080L

#define CR_FIFO_RELEASE_B       0x00000100L
#define CR_HR_INT_RST_B         0x00000200L
#define CR_HR_RST_SRC_B         0x00000400L
#define CR_HR_SHIFT_MD_B        0x00000800L
#define CR_HR_UNPACK_DATA_B     0x00001000L
#define CR_HR_FIFO_NOT_EMPTY_B  0x00002000L
#define CR_HR_FIFO_HALF_FULL_B  0x00004000L
#define CR_HR_FIFO_FULL_B       0x00008000L
```

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```
#define CR_FIFO_RELEASE_C        0x00010000L
#define CR_GC_FR_PANEL_OUTPUT_C  0x00020000L
#define CR_GC_UNPACK_DATA_C      0x00040000L
#define CR_GC_INTR_ENA_C         0x00080000L
#define CR_GC_OVERFLOW__C        0x00100000L
#define CR_GC_FIFO_NOT_EMPTY_C   0x00200000L
#define CR_GC_FIFO_HALF_FULL_C   0x00400000L
#define CR_GC_FIFO_FULL_C        0x00800000L

#define CR_GC_SFTW_SYNC_SLCT_C   0x01000000L
#define CR_GC_SFTW_AS_SYNC_C     0x02000000L
#define CR_GC_SFTW_SS_SYNC_C     0x04000000L
#define CR_GC_SFTW_GAIN_SYNC_C   0x08000000L

#define CR_HRA_INPUT_SRC_C       0x20000000L
#define CR_HRB_INPUT_SRC_C       0x40000000L

#define GRAY_CTL_MASK            0x0fff0000
#define HARRIS_A_CTL_MASK        0x200000ff
#define HARRIS_B_CTL_MASK        0x4000ff00

#endif
```

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```
/* mod.h - This file determines the MIX Module's base address based on the
           processor which is running the program, the MIX Baseboard, and
           the MIX stack position being addressed.

 Note: This file only supports the following DSP processor boards:
        4283            4254         4257
        4284            4270

 Defining the Baseboard:
    Set the appropriate BB_42XX constant to a 1 and the others to 0

 Running programs on a 4270, 4254, or 4257 Mix Module
    Set the MM_4270 constant if processor is on the 4270
    Set the MM_425X constant if processor is on the 4257

 Running program on the 4284 or 4283
    Clear the MM_4270 and MM_425X constants

 Specifying the MIX Module stack position of Mix Module being addressed
    For Mix stack position 0, set MOD to MOD0_ADDR
    For Mix stack position 1, set MOD to MOD1_ADDR
    For Mix stack position 2, set MOD to MOD2_ADDR

 Running programs on the 4283 Mix Baseboard(Setting the Page Register)
    To select Mix stack position 0, set MOD_SELECT to MOD0_SELECT
    To select Mix stack position 1, set MOD_SELECT to MOD1_SELECT
    To select Mix stack position 2, set MOD_SELECT to MOD2_SELECT
*/

/* Define BaseBoard Type */
#define BB_4283        0
#define BB_4284        0
#define BB_4200        0
#define BB_4201        1
#define BB_4202        0

/* Define Mix Module Type - Only if program is to be executed
                            on a Mix Module Processor               */
#define MM_4270        1
#define MM_425X        0

/* Specify Mix Module Position of module being addressed */
#define MOD            MOD1_ADDR

#if MM_4270 | MM_425X
/* Specify MIX STACK Position for the 4270 or 425X processor boards */
#define MIX_POS        0
#endif

#if BB_4283
/* The 4283 Selects the Mix Module being addressed with a Page Register */
#define MOD_SELECT     MOD0_SELECT
#else
#define MOD_SELECT     MOD          /* Only being set to keep code similar  */
#endif
```

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```
/* BaseBoard = 4283 - This BaseBoard does not support Upper Mix Bus Masters */
#if BB_4283

/* The 4283 Baseboard uses a page register to select which Mix Module */
/* is being accessed                                                  */
#define  MOD0_SELECT      0x18000
#define  MOD1_SELECT      0x10000
#define  MOD2_SELECT      0x8000

#define  MOD0_ADDR        0x00804000
#define  MOD1_ADDR        0x00804000
#define  MOD2_ADDR        0x00804000

/* Some Mix Modules require the setting of Address Bit 27   */
/* This is selected in the Page Register for this baseboard */
#define D17_DATA_BIT      0x00020000

/* Address Bit in address which corresponds to A27 - This is unused by 4283 */
#define A27_ADDR_BIT      0x00000000

#endif

/* BaseBoard = 4284 */
#if BB_4284

#if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257  */

#define  MOD0_ADDR        0xC0000000
#define  MOD1_ADDR        0xC4000000
#define  MOD2_ADDR        0xC8000000

/* Address Bit in address which corresponds to A27 */
#define A27_ADDR_BIT      0x02000000

#else                   /* No Mix Module             */

#define  MOD0_ADDR        0x20000000
#define  MOD1_ADDR        0x24000000
#define  MOD2_ADDR        0x28000000

/* Address Bit in address which corresponds to A27 */
#define A27_ADDR_BIT      0x02000000
#endif


#endif

/* BaseBoard = 4200 or 4201 */
#if BB_4200 | BB_4201

#if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257  */

#define  MOD0_ADDR        0xF0000000
#define  MOD1_ADDR        0xF4000000
#define  MOD2_ADDR        0xF8000000
```

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```
/* Address Bit in address which corresponds to A27 */
#define A27_ADDR_BIT      0x02000000
#else            /* No Mix Module             */

#define  MOD0_ADDR        0xC0000000
#define  MOD1_ADDR        0xD0000000
#define  MOD2_ADDR        0xE0000000

/* Address Bit in address which corresponds to A27 */
#define A27_ADDR_BIT      0x02000000
#endif

#endif

/* BaseBoard = 4202  */
#if BB_4202

#if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257  */

#define  MOD0_ADDR        0xC0000000
#define  MOD1_ADDR        0xC4000000
#define  MOD2_ADDR        0xC8000000

/* Address Bit in address which corresponds to A27 */
#define A27_ADDR_BIT      0x02000000
#endif

#endif


/************************** End of File ****************************/
```

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```
/*********************************************************************
 * FILE: p4272c.c
 * Description: This example program demonstrates how to setup and
 * acquire complex data on a Pentek Model 4272.  Once data has been
 * acquired a radix 4 complex FFT is computed and formatted
 * for display.
 *********************************************************************/

#include "mod.h"
#include "4272.h"
#include "math.h"

#define PROCESS_DATA  0
#define DISPLAY_DATA  0

#define POLLING       1
#define INTERRUPTS    0

/* Data Source - This Selection determines which input connector   */
/* contains the clock and data.  The Graychip always gets it's     */
/* data from connector C, but the Harris Chips can get their data  */
/* from their own connector or from input connector C              */
#define CHANNEL_A     0
#define CHANNEL_B     1
#define CHANNEL_C     2

#define DATA_SOURCE   CHANNEL_C

/* Channel select */
#define CHAN_SELECT   CHANNEL_C

/* Data Modes */
#define PACKED        1
#define UNPACKED      0

/* Tuning Frequency */
#define TUNING_FREQ        (float) 3.0e6

/* Decimation Factor - The range of values for this control differs */
/* between the Harris and Gray Chips.                               */
#define DEC_FACTOR         64

/* Input clock frequency - This clock is provided by the source of the
                    data
*/
#define INPUT_CLOCK_FREQ   50.0e6

/* Number of Samples to acquire - In complex Mode, this program refers to */
/* one sample as one real plus one imaginary sample.                      */
#define NUM_SAMPLES        1024

#if BB_4283
/* 4283 Specific Registers */
unsigned int *PageAddressReg, *ExpBusControlReg;
#endif
```

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```
/* 4272 Registers */
volatile unsigned int *HarrisA_LSB, *HarrisA_MSB;
volatile unsigned int *HarrisB_LSB, *HarrisB_MSB;
volatile unsigned int *GrayC;
volatile unsigned int *Status, *Control, *Fifo;

int           Samples[NUM_SAMPLES*2];
int           half_fifo_size;
char          data_ready;
int           samples_needed;
unsigned      int intr_mask;
int           *samplesP;

extern double  data_buf[];  /* This is defined in fft_c4.asm.  This buffer is
*/
                     /* allocated in it's own data section(.databuf)   */
                     /* The FFT routine uses circular addressing which */
                     /* requires the N LSBs to be zero. N is an        */
                     /* integer such that 2**N > R.  R is the size of  */
                     /* data buffer.                                   */

extern void enableInterrupts();
extern void clearInterrupts();
extern float fdiv();
extern void ProcessAndDisplayData();
extern void InitFFTTables();
double determineScaleMult();
int   *ReadSamples();

main()
{
    register int i;
    register int j;
    unsigned int cntl_mask;
    unsigned int status_mask;
    int          temp;
    int          num_samples;
    int          dec_factor;

#if BB_4283
    ExpBusControlReg = (unsigned int *) 0x808060u;
    PageAddressReg   = (unsigned int *) 0x800002u;

    *ExpBusControlReg = 0x0;             /* Remove MIX bus wait states */
    *PageAddressReg = MOD_SELECT;        /* Select module */
#endif
#if BB_4284
    *(unsigned int *) 0x100020 = 0;     /* Turn off timer */
#endif
#if MM_4270
    *(unsigned int *) 0x34000d = 0xff;   /* Disable NMI generation     */
#endif
```

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```
    Status      = (unsigned int *) (MOD | P4272_STATUS_REG);
    Control     = (unsigned int *) (MOD | P4272_CONTROL_REG);
    HarrisA_LSB = (unsigned int *) (MOD | P4272_HARRIS_CNTLA_LSB);
    HarrisA_MSB = (unsigned int *) (MOD | P4272_HARRIS_CNTLA_MSB);
    HarrisB_LSB = (unsigned int *) (MOD | P4272_HARRIS_CNTLB_LSB);
    HarrisB_MSB = (unsigned int *) (MOD | P4272_HARRIS_CNTLB_MSB);
    GrayC       = (unsigned int *) (MOD | P4272_GRAYCHIP_REG_0);

#if PROCESS_DATA
    /* Initialize tables for fft processing */
    InitFFTTables(NUM_SAMPLES);
#endif

#if INTERRUPTS
      i = *Status;         /* Clear any pending interrupts   */
      enableInterrupts();  /* Enable Mix Interrupt           */
#endif

    dec_factor = DEC_FACTOR;
    while (1)
    {
      /* Reset the Gray and Harris Chips */
      *Control = CR_HR_INT_RST_A | CR_HR_INT_RST_B;
      /* Reset Data Ready Flag */
      data_ready = 0;

      if (CHAN_SELECT == CHANNEL_A)
      {
          Fifo       = (unsigned int *) (MOD | P4272_HARRIS_A_FIFO);
          half_fifo_size = P4272_NB_FIFO_SIZE / 2;
          intr_mask  = CR_HR_FIFO_HALF_FULL_A;
          cntl_mask  = CR_FIFO_RELEASE_A;
          status_mask = SR_FIFO_HALF_FULL_A;

          InitHarrisA(TUNING_FREQ, dec_factor);  /* Initialize Harris A */
      }
      else if (CHAN_SELECT == CHANNEL_B)
      {
          Fifo       = (unsigned int *) (MOD | P4272_HARRIS_B_FIFO);
          half_fifo_size = P4272_NB_FIFO_SIZE / 2;
          intr_mask  = CR_HR_FIFO_HALF_FULL_B;
          cntl_mask  = CR_FIFO_RELEASE_B;
          status_mask = SR_FIFO_HALF_FULL_B;

          InitHarrisB(TUNING_FREQ, dec_factor);  /* Initialize Harris B */
      }
      else   /*  CHAN_SELECT = CHANNEL_C */
      {
          Fifo       = (unsigned int *) (MOD | P4272_GRAYCHIP_FIFO);
          half_fifo_size = P4272_WB_FIFO_SIZE / 2;
          intr_mask  = CR_GC_FIFO_HALF_FULL_C;
          cntl_mask  = CR_FIFO_RELEASE_C;
          status_mask = SR_FIFO_HALF_FULL_C;
          InitGray(TUNING_FREQ, dec_factor);   /* Initialize the Graychip */
      }
```

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```
      /* Enable Interrupt Mask */
      *Control |= intr_mask;

      ResetFifo(CHAN_SELECT);                    /* Reset and Release Fifo */

      /* Calculate the number of samples to read.  Each complex */
      /* sample requries a real and an imaginary part           */
      samples_needed = NUM_SAMPLES * 2;
      samplesP = Samples;
#if POLLING
      if (CHAN_SELECT == CHANNEL_C)
      {
          while (*Status & status_mask);         /* wait FIFO half-full    */

          /* Since this example only requires 1K samples, turn off clock to */
          /* Graychip.  This will prevent fifo from a narrow write pulse    */
          /* when fifo fills up during data read out.                       */
          temp = GrayC[CH_FILTER_MODE];
          GrayC[CH_FILTER_MODE] = 0x0;

          /* Read out the data samples */
          (void) ReadSamples(samplesP, samples_needed);

          /* Restore Graychip Setting */
          GrayC[CH_FILTER_MODE] = temp;
      }
      else     /* Channels A or B */
      {
          while (samples_needed > 0)
          {
            /* wait FIFO half-full */
            while(*Status & status_mask);

            /* Determine how many samples left to read */
            if (samples_needed <= half_fifo_size)
                num_samples = samples_needed;
            else
                num_samples = half_fifo_size;

            /* Read the data from the fifo */
            samplesP = ReadSamples(samplesP, num_samples);

            /* Decrement number of samples needed */
            samples_needed -= num_samples;
          }
      }
#else
      while (!data_ready);
#endif

#if PROCESS_DATA
       /* Perform Complex FFT */
       ProcessData(Samples, data_buf, NUM_SAMPLES);
#endif
```

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```
#if DISPLAY_DATA
       /* Scale Data for display */
       DisplayData(data_buf, NUM_SAMPLES);
#endif

    }
}
int *ReadSamples(register int *samplesP, register int num_samples)
{
    register int i;
    register int temp;

    /* Read out data from the fifo */
    for (i = 0; i < num_samples / 2; i++)
    {
#if PACKED
      temp = *(int *)Fifo;        /* store real and imaginary */
      *samplesP++ = temp >> 16;   /* Real(I) D31-D16          */
      *samplesP++ = (temp << 16) >> 16; /* Imag(Q) D15-D0     */
#else
      temp = *(int *)Fifo;        /* store real and imaginary */
      *samplesP++ = temp >> 16;   /* Real(I) Value            */
      temp = *(int *)Fifo;
      *samplesP++ = temp >> 16;   /* Imag(Q) Value            */
#endif
    }
    return(samplesP);
}

InitGray(float center, unsigned int dec_factor)
{
    unsigned int freq;
    int          power;
    double       temp;

    freq = (pow(2.0, 28) / INPUT_CLOCK_FREQ) * center;
    GrayC[CH_FREQ_BYTE_0] = freq & 0x000000ff;
    GrayC[CH_FREQ_BYTE_1] = (freq >> 8) & 0x000000ff;
    GrayC[CH_FREQ_BYTE_2] = (freq >> 16) & 0x000000ff;
    GrayC[CH_FREQ_BYTE_3] = (freq >> 24) & 0x000000ff;
    GrayC[CH_SYNC_MODE] = 0x09;/* Disable SS, load center freq always */
    GrayC[CH_FILTER_MODE] = 0x20 | determineDecimationMode(dec_factor);
    GrayC[CH_GAIN_CONTROL] = 0x00;  /* unity gain */
    GrayC[CH_GAIN_EXPONENT] = 0x2;  /* unity gain, immediately */
    GrayC[CH_OUTPUT_MODE] = 0x85;   /* I and Q mux, WS is low true pulse, */
                           /* 16 bit rounding                    */
}

/* determineDecimationMode - This routine determines the Graychip settings */
/*                           for a given decimation factor                 */
determineDecimationMode(unsigned int dec_factor)
{
    int dec_mode;
```

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```
    switch (dec_factor)
    {
       case 0:                          /* Output Rate = Input Rate   */
       case 1:
            dec_mode = 0;
            break;
       case 2:                          /* Output Rate = Input Rate/2  */
            dec_mode = 2;
            break;
       case 4:                          /* Output Rate = Input Rate/4  */
            dec_mode = 3;
            break;
       case 8:                          /* Output Rate = Input Rate/8  */
            dec_mode = 4;
            break;
       case 16:                         /* Output Rate = Input Rate/16 */
            dec_mode = 5;
            break;
       case 32:                         /* Output Rate = Input Rate/32 */
            dec_mode = 6;
            break;
       case 64:                         /* Output Rate = Input Rate/64 */
            dec_mode = 7;
            break;
       default:                         /* Output Rate = Input Rate/64 */
            dec_mode = 7;
    }

    return(dec_mode);
}

InitHarrisA(float center, unsigned int dec_factor)
{
    unsigned int freq;
    unsigned int scaling;
    double       scaleMult;

    /* Calculate the Minimum Phase Increment                            */
    /* Phase Incr = ((2**33) / Input Clock Rate) * Desired LO / 2       */
    /* Center Freq is scaled by 2 to prevent overflow on real-int       */
    /* conversion                                                       */
    freq = fdiv(pow(2.0, 33), INPUT_CLOCK_FREQ) * center / 2;
    freq *= 2;

    /* Control Register 1: Normal Mode (CW), */
    *HarrisA_LSB =(freq << 4) | 0x1;
    *HarrisA_MSB = 0x30 | (freq >> 28);
    SendA();

    /* Control Register 2: max phase increment - Only used during Chirp Modes
*/
    *HarrisA_LSB = 0x0;
    *HarrisA_MSB = 0x50;
    SendA();
```

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```
    /* Control Register 3: phase offset = 0 */
    *HarrisA_LSB = 0x0;
    *HarrisA_MSB = 0x70;
    SendA();

    /* Control Register 4: adjust gain for HDF decimation , offset and flip */
    *HarrisA_LSB = determineHDFDataShift(dec_factor);
    *HarrisA_MSB = 0x91;

    SendA();

    /* Control Register 5: HDF decimation  */
    scaleMult = determineScaleMult(dec_factor);
    scaling = scaleMult * pow(2.0, 20);
    scaling &= 0x001fffe0;
    *HarrisA_LSB = scaling | (dec_factor - 1) << 21;
    *HarrisA_MSB = 0xb0 | (dec_factor - 1) >> 12;
    SendA();

    /* Control Register 6: This value is hardware specific and should  */
    /*                     never be modified                           */
    *HarrisA_LSB = 0x0d126002;
    *HarrisA_MSB = 0xd0;
    SendA();

    /* Control Register 7: Force input to 0x8000 when enabled in control */
    /*                     reg 1                                          */
    *HarrisA_LSB = 0x00002000;
    *HarrisA_MSB = 0xF0;
    SendA();
}

InitHarrisB(float center, unsigned int dec_factor)
{
    unsigned int freq;
    unsigned int scaling = 0;
    double       scaleMult;

    /* Calculate the Minimum Phase Increment                          */
    /* Phase Incr = ((2**33) / Input Clock Rate) * Desired LO / 2     */
    /* Center Freq is scaled by 2 to prevent overflow on real-int     */
    /* conversion                                                     */
    freq = (pow(2.0, 33) / INPUT_CLOCK_FREQ) * center / 2;
    freq *= 2;

    /* Control Register 1: Normal Mode (CW), */
    *HarrisB_LSB =(freq << 4) | 0x1;
    *HarrisB_MSB = 0x30 | (freq >> 28);
    SendB();

    /* Control Register 2: max phase increment - Only used during Chirp Modes
*/
    *HarrisB_LSB = 0x0;
    *HarrisB_MSB = 0x50;
    SendB();
```

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```
    /* Control Register 3: phase offset = 0 */
    *HarrisB_LSB = 0x00000;
    *HarrisB_MSB = 0x70;
    SendB();

    /* Control Register 4: adjust gain for HDF decimation , offset and flip */
    *HarrisB_LSB = determineHDFDataShift(dec_factor);
    *HarrisB_MSB = 0x91;
    SendB();

    /* Control Register 5: HDF decimation  */
    scaleMult = determineScaleMult(dec_factor);
    scaling = scaleMult * pow(2.0, 20.0);
    scaling &= 0x001fffe0;
    *HarrisB_LSB = scaling | (dec_factor - 1) << 21;
    *HarrisB_MSB = 0xb0 | (dec_factor - 1) >> 12;
    SendB();

    /* Control Register 6: This value is hardware specific and should  */
    /*                     never be modified                           */
    *HarrisB_LSB = 0x0d126002;
    *HarrisB_MSB = 0xd0;
    SendB();

    /* Control Register 7: Force input to 0x8000 when enabled in control */
    /*                     reg 1                                         */
    *HarrisB_LSB = 0x00002000;
    *HarrisB_MSB = 0xF0;
    SendB();
}


SendA()
{
    /* Send Shift command to harris chip - This operation takes about */
    /* 1 Millisecond to complete the transfer to the Harris Control   */
    /* Buffer.  When modifing settings during data acquisition,       */
    /* waiting for operation to complete will result in loss of data. */
    /* Bypass the wait for completion in this case.                   */

    *Control = (*Control & ~HARRIS_A_CTL_MASK) | CR_HR_SHIFT_MD_A |
             CR_FIFO_RELEASE_A;

    /* Wait for Shifting to be started */
    while(!(*Status & SR_SHIFT_MODE_A));

    /* Wait for Shifting to be completed */
    while(*Status & SR_SHIFT_MODE_A);

    /* Clear the Command Shift bit in control register */
    *Control = (*Control & ~HARRIS_A_CTL_MASK) |
             CR_FIFO_RELEASE_A; /* release fifo */
}
```

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```
SendB()
{
    /* Send Shift command to harris chip - This operation takes about */
    /* 1 Millisecond to complete the transfer to the Harris Control   */
    /* Buffer.  When modifing settings during data acquisition,       */
    /* waiting for operation to complete will result in loss of data. */
    /* Bypass the wait for completion in this case.                   */

    *Control = (*Control & ~HARRIS_B_CTL_MASK) | CR_HR_SHIFT_MD_B |
            CR_FIFO_RELEASE_B;

    /* Wait for Shifting to be started */
    while(!(*Status & SR_SHIFT_MODE_B));

    /* Wait for Shifting to be completed */
    while(*Status & SR_SHIFT_MODE_B);

    /* Clear the Command Shift bit in control register */
    *Control = (*Control & ~HARRIS_B_CTL_MASK) |
            CR_FIFO_RELEASE_B; /* release fifo */
}

/* determineHDFDataShift - This routine determines the HDF Data Shift
                    which is used by the Harris Chip to compensate
                    for the truncation due to the 5 stage decimation
                    filter
*/
unsigned int determineHDFDataShift(unsigned int dec_factor)
{
    unsigned int dataShift;
    int          power;
    double       temp;

    /* Determine the Log2(dec_factor) */
    temp = frexp(dec_factor, &power);

    /* Decrement the exponent by 1 and Multiply the fraction by 2 */
    /* frexp always rounds up                                     */
    --power;

    /* Data shift = 75 - Ceiling(5*Log2(R))   */
    /*    R = Decimation Factor               */
    temp = 5 * power;
    dataShift = 75 - ceil(temp);
    if ((int)dataShift < 0)
      dataShift = 0;
    dataShift = dataShift << 1;

    return(dataShift);
}
```

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```
/* determineScaleMult - This routine determines the scaling multiplier
                        which is used by the Harris Chip to compensate
                        for HDF Gain.
*/
double determineScaleMult(unsigned int dec_factor)
{
    int          power;
    double       temp;
    double       fraction;
    double       ScaleMult;

    /* Determine the Log2(dec_factor) */
    fraction = frexp((double) dec_factor, &power);

    /* Decrement the exponent by 1 and Multiply the fraction by 2 */
    /* frexp always rounds up                                     */
    --power;

    fraction *= 2.0;

    /* If decimation is a power of 2, then the scale multiplier is 1 */
    /* otherwise calculate the Scale Multiplier                      */
    /*     Scale Multiplier = 2**(Ceiling(5Log2(R))) / R**5          */
    /*           where R = decimation factor                         */
    if (fraction != 1.0)
    {
      temp = 5 * power;
      temp = ceil(temp);

      ScaleMult = pow(2.0, temp) / pow((double) dec_factor, 5.0);
    }
    else
      ScaleMult = 1.0;

    return(ScaleMult);
}

void ResetFifo(unsigned int chan_select)
{
    unsigned int temp;
    unsigned int temp1;
    unsigned int iq_mask;
    unsigned int status_mask;
    unsigned int iq_state;

    /* Reset the Fifos */
    *Control = 0;

    /* Select the data source.  For the Harris Chips, Data can be */
    /* received from the channel C                                */
    if (DATA_SOURCE == CHANNEL_C)
      *Control |= CR_HRA_INPUT_SRC_C | CR_HRB_INPUT_SRC_C;
```

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```
    if (chan_select == CHANNEL_C)
    {
      /* Save previous Filter Mode setting and turn off decimated clock.    */
      /* When the Fifo is Released, It is important that no Fifo writes are */
      /* occuring at the same time. A narrow write pulse may cause the fifo */
      /* to lose it's memory.  The same condition can occur after the fifo  */
      /* reaches a full condition and a sample is read from the fifo. For   */
      /* either case, it is recommended that the Filter Mode Register is    */
      /* cleared before releasing the fifo reset and reading samples from   */
      /* a full fifo.                                                       */

      temp = GrayC[CH_FILTER_MODE];
      GrayC[CH_FILTER_MODE] = 0x0;
    }

    /* Release Reset and Set non-packed data mode.  Data packing is  */
    /* a method of reading out the data from the fifo in an efficient */
    /* manner.  It does not affect how the data is acquired or stored */
    /* within the fifo.  In complex output mode, I and Q positioning  */
    /* must be determined before entering packed data mode.           */
    if (chan_select == CHANNEL_A)
    {
      /* Set Mask for determining IQ Ordering */
      iq_mask = SR_DATA_TYPE_A;
#if PACKED
      iq_state = HR_PACKED_IMAG_Q_DATA_A;
#else
      iq_state = HR_UNPACKED_IMAG_Q_DATA_A;
#endif

      /* Set Status Mask for Fifo Empty Flag  */
      status_mask = SR_FIFO_EMPTY_A;

      *Control |= (CR_FIFO_RELEASE_A | CR_HR_UNPACK_DATA_A | intr_mask);
    }
    else if (chan_select == CHANNEL_B)
    {
      /* Set Mask for determining IQ Ordering */
      iq_mask = SR_DATA_TYPE_B;
#if PACKED
      iq_state = HR_PACKED_IMAG_Q_DATA_B;
#else
      iq_state = HR_UNPACKED_IMAG_Q_DATA_B;
#endif

      /* Set Status Mask for Fifo Empty Flag  */
      status_mask = SR_FIFO_EMPTY_B;

        led_on();

      *Control |= (CR_FIFO_RELEASE_B | CR_HR_UNPACK_DATA_B | intr_mask);
    }
```

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```
    else
    {
      /* Set Mask for determining IQ Ordering */
      iq_mask = SR_DATA_TYPE_C;
#if PACKED
      iq_state = GC_PACKED_IMAG_Q_DATA_C;
#else
      iq_state = GC_UNPACKED_IMAG_Q_DATA_C;
#endif

      /* Set Status Mask for Fifo Empty Flag  */
      status_mask = SR_FIFO_EMPTY_C;

      *Control |= (CR_FIFO_RELEASE_C | CR_GC_UNPACK_DATA_C | intr_mask);

      /* Restore decimated clock and output mode */
      GrayC[CH_FILTER_MODE] = temp;
    }

    /* Wait for Fifo to have at least one sample */
    while ((*Status & status_mask) == 0);

    /* Read the first sample, this is necessary to update the Data */
    /* Type flag in the status register                            */
    temp1 = *Fifo;

    /* Read data until a first Real Sample */
    while (1)
    {
      /* Wait for Fifo to have at least one sample */
      while ((*Status & status_mask) == 0);

      /* While Status indicates next sample is Imaginary */
      /* Read the next sample and discard it             */
      if ((*Status & iq_mask) == iq_state)
         temp1 = *Fifo;
      else
         break;
    }
#if PACKED
    /* Now that the proper sample order has been determined,  */
    /* Enter Packed Mode if selected                          */
    if (chan_select == CHANNEL_A)
      *Control &= ~CR_HR_UNPACK_DATA_A;
    else if (chan_select == CHANNEL_B)
      *Control &= ~CR_HR_UNPACK_DATA_B;
    else
      *Control &= ~CR_GC_UNPACK_DATA_C;
#endif
}
```

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```
c_int01()
{
    unsigned int temp;
    int          num_samples;

    if (CHAN_SELECT == CHANNEL_C)
    {
      /* Since this example only requires 1K samples, turn off clock to */
      /* Graychip.  This will prevent fifo from a narrow write pulse    */
      /* when fifo fills up during data read out.                       */
      temp = GrayC[CH_FILTER_MODE];
      GrayC[CH_FILTER_MODE] = 0x0;

      /* Read out the data samples */
      (void) ReadSamples(Samples, samples_needed);

      /* Indicate to the main program that data is ready */
      data_ready = 1;

      /* Disable Interrupt */
      *Control &= ~intr_mask;
    }
    else     /* Channels A or B */
    {
      /* Determine how many samples left to read */
      if (samples_needed <= half_fifo_size)
          num_samples = samples_needed;
      else
          num_samples = half_fifo_size;
      /* Read the data from the fifo */
      samplesP = ReadSamples(samplesP, num_samples);

      /* Decrement number of samples needed */
      samples_needed -= num_samples;

      /* If all the samples have been gathered */
      if (samples_needed == 0)
      {
          /* Set Data Ready Flag */
          data_ready = 1;

          /* Disable Interrupt */
          *Control &= ~intr_mask;
      }
    }

    temp = *Status;           /* Clear interrupt latch */

    /* Clear Processor Interrupt */
    clearInterrupt();
}

unsigned int *timer1_address = (unsigned int *)0x100030;
led_on()
{
```

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```
      *timer1_address = 0x302u;              /* led ON  */
}

led_off()
{
      *timer1_address = 0x306u;              /* led OFF  */
}

toggle_led()
{
      *timer1_address = ((*timer1_address & 0x306u) ^ 0x4);
}
```

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```
/*********************************************************************
 * FILE: P4272r.c
 * Description: This example program demonstrates how to setup and
 * acquire real data on a Pentek Model 4272.  Once data has been
 * acquired a radix 4 complex FFT is computed and formatted
 * for display.
 *********************************************************************/

#include "mod.h"
#include "4272.h"
#include "math.h"

#define PROCESS_DATA  0
#define DISPLAY_DATA  0

#define POLLING       1
#define INTERRUPTS    0

/* Data Source - This Selection determines which input connector   */
/* contains the clock and data.  The Graychip always gets it's    */
/* data from connector C, but the Harris Chips can get their data */
/* from their own connector or from input connector C             */
#define CHANNEL_A     0
#define CHANNEL_B     1
#define CHANNEL_C     2

#define DATA_SOURCE   CHANNEL_C

/* Channel select */
#define CHAN_SELECT   CHANNEL_C

/* Data Modes */
#define PACKED        0
#define UNPACKED      1

/* Tuning Frequency */
#define TUNING_FREQ        (float) 3.0e6

/* Decimation Factor - The range of values for this control differs */
/* between the Harris and Gray Chips.                              */
#define DEC_FACTOR         32

/* Input clock frequency - This clock is provided by the source of the
                    data
*/
#define INPUT_CLOCK_FREQ   50.0e6

/* Number of Samples to acquire - In complex Mode, this program refers to */
/* one sample as one real plus one imaginary sample.                      */
#define NUM_SAMPLES        1024

#if BB_4283
/* 4283 Specific Registers */
unsigned int *PageAddressReg, *ExpBusControlReg;
#endif
```

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```
/* 4272 Registers */
volatile unsigned int *HarrisA_LSB, *HarrisA_MSB;
volatile unsigned int *HarrisB_LSB, *HarrisB_MSB;
volatile unsigned int *GrayC;
volatile unsigned int *Status, *Control, *Fifo;

int           Samples[NUM_SAMPLES*2];
int           half_fifo_size;
char          data_ready;
int           samples_needed;
unsigned      int intr_mask;
int           *samplesP;

extern double  data_buf[];  /* This is defined in fft_c4.asm.  This buffer is
*/
                     /* allocated in it's own data section(.databuf)   */
                     /* The FFT routine uses circular addressing which */
                     /* requires the N LSBs to be zero. N is an        */
                     /* integer such that 2**N > R.  R is the size of  */
                     /* data buffer.                                   */

extern void enableInterrupts();
extern void clearInterrupts();
extern float fdiv();
extern void ProcessAndDisplayData();
extern void InitFFTTables();
double determineScaleMult();
int   *ReadSamples();

main()
{
    register int i;
    register int j;
    unsigned int cntl_mask;
    unsigned int status_mask;
    int          temp;
    int          num_samples;
    int          dec_factor;

#if BB_4283
    ExpBusControlReg = (unsigned int *) 0x808060u;
    PageAddressReg   = (unsigned int *) 0x800002u;

    *ExpBusControlReg = 0x0;             /* Remove MIX bus wait states */
    *PageAddressReg = MOD_SELECT;        /* Select module */
#endif
#if BB_4284
    *(unsigned int *) 0x100020 = 0;     /* Turn off timer */
#endif
#if MM_4270
    *(unsigned int *) 0x34000d = 0xff;   /* Disable NMI generation     */
#endif
```

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```
    Status      = (unsigned int *) (MOD | P4272_STATUS_REG);
    Control     = (unsigned int *) (MOD | P4272_CONTROL_REG);
    HarrisA_LSB = (unsigned int *) (MOD | P4272_HARRIS_CNTLA_LSB);
    HarrisA_MSB = (unsigned int *) (MOD | P4272_HARRIS_CNTLA_MSB);
    HarrisB_LSB = (unsigned int *) (MOD | P4272_HARRIS_CNTLB_LSB);
    HarrisB_MSB = (unsigned int *) (MOD | P4272_HARRIS_CNTLB_MSB);
    GrayC       = (unsigned int *) (MOD | P4272_GRAYCHIP_REG_0);

#if PROCESS_DATA
    /* Initialize tables for fft processing */
    InitFFTTables(NUM_SAMPLES);
#endif

#if INTERRUPTS
      i = *Status;         /* Clear any pending interrupts   */
      enableInterrupts();  /* Enable Mix Interrupt           */
#endif

    dec_factor = DEC_FACTOR;
    while (1)
    {
      /* Reset the Gray and Harris Chips */
      *Control = CR_HR_INT_RST_A | CR_HR_INT_RST_B;
      /* Reset Data Ready Flag */
      data_ready = 0;

      if (CHAN_SELECT == CHANNEL_A)
      {
          Fifo       = (unsigned int *) (MOD | P4272_HARRIS_A_FIFO);
          half_fifo_size = P4272_NB_FIFO_SIZE / 2;
          intr_mask  = CR_HR_FIFO_HALF_FULL_A;
          cntl_mask  = CR_FIFO_RELEASE_A;
          status_mask = SR_FIFO_HALF_FULL_A;

          InitHarrisA(TUNING_FREQ, dec_factor);  /* Initialize Harris A */
      }
      else if (CHAN_SELECT == CHANNEL_B)
      {
          Fifo       = (unsigned int *) (MOD | P4272_HARRIS_B_FIFO);
          half_fifo_size = P4272_NB_FIFO_SIZE / 2;
          intr_mask  = CR_HR_FIFO_HALF_FULL_B;
          cntl_mask  = CR_FIFO_RELEASE_B;
          status_mask = SR_FIFO_HALF_FULL_B;

          InitHarrisB(TUNING_FREQ, dec_factor);  /* Initialize Harris B */
      }
      else   /*  CHAN_SELECT = CHANNEL_C */
      {
          Fifo       = (unsigned int *) (MOD | P4272_GRAYCHIP_FIFO);
          half_fifo_size = P4272_WB_FIFO_SIZE / 2;
          intr_mask  = CR_GC_FIFO_HALF_FULL_C;
          cntl_mask  = CR_FIFO_RELEASE_C;
          status_mask = SR_FIFO_HALF_FULL_C;
          InitGray(TUNING_FREQ, dec_factor);   /* Initialize the Graychip */
      }
```

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```
      /* Enable Interrupt Mask */
      *Control |= intr_mask;

      ResetFifo(CHAN_SELECT);                    /* Reset and Release Fifo */

      /* Calculate the number of samples to read.  Each complex */
      /* sample requries a real and an imaginary part           */
      samples_needed = NUM_SAMPLES;
      samplesP = Samples;
#if POLLING
      if (CHAN_SELECT == CHANNEL_C)
      {
          while (*Status & status_mask);         /* wait FIFO half-full    */

            led_off();

          /* Since this example only requires 1K samples, turn off clock to */
          /* Graychip.  This will prevent fifo from a narrow write pulse    */
          /* when fifo fills up during data read out.                       */
          temp = GrayC[CH_FILTER_MODE];
          GrayC[CH_FILTER_MODE] = 0x0;

          /* Read out the data samples */
          (void) ReadSamples(samplesP, samples_needed);

          /* Restore Graychip Setting */
          GrayC[CH_FILTER_MODE] = temp;
      }
      else     /* Channels A or B */
      {
          while (samples_needed > 0)
          {
            /* wait FIFO half-full */
            while(*Status & status_mask);

                led_off();

            /* Determine how many samples left to read */
            if (samples_needed <= half_fifo_size)
                num_samples = samples_needed;
            else
                num_samples = half_fifo_size;

            /* Read the data from the fifo */
            samplesP = ReadSamples(samplesP, num_samples);

            /* Decrement number of samples needed */
            samples_needed -= num_samples;
          }
      }
#else
      while (!data_ready);
#endif
```

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```
#if PROCESS_DATA
       /* Perform Complex FFT */
       ProcessData(Samples, data_buf, NUM_SAMPLES);
#endif
#if DISPLAY_DATA
       /* Scale Data for display */
       DisplayData(data_buf, NUM_SAMPLES);
#endif

    }
}
int *ReadSamples(register int *samplesP, register int num_samples)
{
    register int i;
    register int temp;
    register int num_reads;

    if (CHAN_SELECT == CHANNEL_C)
        num_reads = num_samples/2;
    else
        num_reads = num_samples;

    /* Read out data from the fifo */
    for (i = 0; i < num_reads; i++)
    {
#if PACKED
      temp = *(int *)Fifo;        /* store real and imaginary */
      *samplesP++ = temp >> 16;   /* Real(I) D31-D16          */
        if (CHAN_SELECT == CHANNEL_C)
            *samplesP++ = (temp << 16) >> 16; /* Imag(Q) D15-D0     */
#else
        if (CHAN_SELECT == CHANNEL_C)
        {
          temp = *(int *)Fifo;        /* store real and imaginary */
          *samplesP++ = temp >> 16;   /* Real(I) Value            */
          temp = *(int *)Fifo;
          *samplesP++ = temp >> 16;   /* Real(I) Value            */
        }
        else
        {
          temp = *(int *)Fifo;
            *samplesP++ = temp >> 16;   /* Real(I) Value            */
          temp = *(int *)Fifo;        /* Make Dummy Read          */
        }
#endif
    }
    return(samplesP);
}
```

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```
InitGray(float center, unsigned int dec_factor)
{
    unsigned int freq;
    int          power;
    double       temp;

    freq = (pow(2.0, 28) / INPUT_CLOCK_FREQ) * center;
    GrayC[CH_FREQ_BYTE_0] = freq & 0x000000ff;
    GrayC[CH_FREQ_BYTE_1] = (freq >> 8) & 0x000000ff;
    GrayC[CH_FREQ_BYTE_2] = (freq >> 16) & 0x000000ff;
    GrayC[CH_FREQ_BYTE_3] = (freq >> 24) & 0x000000ff;
    GrayC[CH_SYNC_MODE] = 0x09;/* Disable SS, load center freq always */
    GrayC[CH_FILTER_MODE] = 0x50 | determineDecimationMode(dec_factor);
    GrayC[CH_GAIN_CONTROL] = 0x00;  /* unity gain */
    GrayC[CH_GAIN_EXPONENT] = 0x2;  /* unity gain, immediately */
    GrayC[CH_OUTPUT_MODE] = 0x85;   /* I and Q mux, WS is low true pulse, */
                           /* 16 bit rounding                    */
}

/* determineDecimationMode - This routine determines the Graychip settings */
/*                            for a given decimation factor                */
determineDecimationMode(unsigned int dec_factor)
{
    int dec_mode;

    switch (dec_factor)
    {
       case 0:                          /* Output Rate = Input Rate   */
       case 1:
            dec_mode = 2;
            break;
       case 2:                          /* Output Rate = Input Rate/2  */
            dec_mode = 3;
            break;
       case 4:                          /* Output Rate = Input Rate/4  */
            dec_mode = 4;
            break;
       case 8:                          /* Output Rate = Input Rate/8  */
            dec_mode = 5;
            break;
       case 16:                         /* Output Rate = Input Rate/16 */
            dec_mode = 6;
            break;
       case 32:                         /* Output Rate = Input Rate/32 */
            dec_mode = 7;
            break;
       default:                         /* Output Rate = Input Rate/32 */
            dec_mode = 7;
    }

    return(dec_mode);
}
```

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```
InitHarrisA(float center, unsigned int dec_factor)
{
    unsigned int freq;
    unsigned int scaling;
    double       scaleMult;

    /* Calculate the Minimum Phase Increment                              */
    /* Phase Incr = ((2**33) / Input Clock Rate) * Desired LO / 2         */
    /* Center Freq is scaled by 2 to prevent overflow on real-int         */
    /* conversion                                                         */
    freq = fdiv(pow(2.0, 33), INPUT_CLOCK_FREQ) * center / 2;
    freq *= 2;

    /* Control Register 1: Normal Mode (CW), */
    *HarrisA_LSB =(freq << 4) | 0x1;
    *HarrisA_MSB = 0x30 | (freq >> 28);
    SendA();

    /* Control Register 2: max phase increment - Only used during Chirp Modes
*/
    *HarrisA_LSB = 0x0;
    *HarrisA_MSB = 0x50;
    SendA();

    /* Control Register 3: phase offset = 0 */
    *HarrisA_LSB = 0x0;
    *HarrisA_MSB = 0x70;
    SendA();

    /* Control Register 4: adjust gain for HDF decimation , offset and flip */
    *HarrisA_LSB = 0x80000000 | determineHDFDataShift(dec_factor);
    *HarrisA_MSB = 0x90;

    SendA();

    /* Control Register 5: HDF decimation  */
    scaleMult = determineScaleMult(dec_factor);
    scaling = scaleMult * pow(2.0, 20);
    scaling &= 0x001fffe0;
    *HarrisA_LSB = scaling | (dec_factor - 1) << 21;
    *HarrisA_MSB = 0xb0 | (dec_factor - 1) >> 12;
    SendA();

    /* Control Register 6: This value is hardware specific and should  */
    /*                     never be modified                           */
    *HarrisA_LSB = 0x0d126002;
    *HarrisA_MSB = 0xd0;
    SendA();

    /* Control Register 7: Force input to 0x8000 when enabled in control */
    /*                     reg 1                                          */
    *HarrisA_LSB = 0x00002000;
    *HarrisA_MSB = 0xF0;
    SendA();
}
```

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```
InitHarrisB(float center, unsigned int dec_factor)
{
    unsigned int freq;
    unsigned int scaling = 0;
    double       scaleMult;

    /* Calculate the Minimum Phase Increment                          */
    /* Phase Incr = ((2**33) / Input Clock Rate) * Desired LO / 2     */
    /* Center Freq is scaled by 2 to prevent overflow on real-int     */
    /* conversion                                                     */
    freq = (pow(2.0, 33) / INPUT_CLOCK_FREQ) * center / 2;
    freq *= 2;

    /* Control Register 1: Normal Mode (CW), */
    *HarrisB_LSB =(freq << 4) | 0x1;
    *HarrisB_MSB = 0x30 | (freq >> 28);
    SendB();

    /* Control Register 2: max phase increment - Only used during Chirp Modes
*/
    *HarrisB_LSB = 0x0;
    *HarrisB_MSB = 0x50;
    SendB();

    /* Control Register 3: phase offset = 0 */
    *HarrisB_LSB = 0x00000;
    *HarrisB_MSB = 0x70;
    SendB();

    /* Control Register 4: adjust gain for HDF decimation , offset and flip */
    *HarrisB_LSB = 0x80000000 | determineHDFDataShift(dec_factor);
    *HarrisB_MSB = 0x90;
    SendB();

    /* Control Register 5: HDF decimation  */
    scaleMult = determineScaleMult(dec_factor);
    scaling = scaleMult * pow(2.0, 20.0);
    scaling &= 0x001fffe0;
    *HarrisB_LSB = scaling | (dec_factor - 1) << 21;
    *HarrisB_MSB = 0xb0 | (dec_factor - 1) >> 12;
    SendB();

    /* Control Register 6: This value is hardware specific and should  */
    /*                     never be modified                           */
    *HarrisB_LSB = 0x0d126002;
    *HarrisB_MSB = 0xd0;
    SendB();

    /* Control Register 7: Force input to 0x8000 when enabled in control */
    /*                     reg 1                                          */
    *HarrisB_LSB = 0x00002000;
    *HarrisB_MSB = 0xF0;
    SendB();
}
```

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```
SendA()
{
    /* Send Shift command to harris chip - This operation takes about */
    /* 1 Millisecond to complete the transfer to the Harris Control   */
    /* Buffer.  When modifing settings during data acquisition,       */
    /* waiting for operation to complete will result in loss of data. */
    /* Bypass the wait for completion in this case.                   */

    *Control = (*Control & ~HARRIS_A_CTL_MASK) | CR_HR_SHIFT_MD_A |
            CR_FIFO_RELEASE_A;

    /* Wait for Shifting to be started */
    while(!(*Status & SR_SHIFT_MODE_A));

    /* Wait for Shifting to be completed */
    while(*Status & SR_SHIFT_MODE_A);

    /* Clear the Command Shift bit in control register */
    *Control = (*Control & ~HARRIS_A_CTL_MASK) |
            CR_FIFO_RELEASE_A; /* release fifo */
}

SendB()
{
    /* Send Shift command to harris chip - This operation takes about */
    /* 1 Millisecond to complete the transfer to the Harris Control   */
    /* Buffer.  When modifing settings during data acquisition,       */
    /* waiting for operation to complete will result in loss of data. */
    /* Bypass the wait for completion in this case.                   */

    *Control = (*Control & ~HARRIS_B_CTL_MASK) | CR_HR_SHIFT_MD_B |
            CR_FIFO_RELEASE_B;

    /* Wait for Shifting to be started */
    while(!(*Status & SR_SHIFT_MODE_B));

    /* Wait for Shifting to be completed */
    while(*Status & SR_SHIFT_MODE_B);

    /* Clear the Command Shift bit in control register */
    *Control = (*Control & ~HARRIS_B_CTL_MASK) |
            CR_FIFO_RELEASE_B; /* release fifo */
}

/* determineHDFDataShift - This routine determines the HDF Data Shift
                    which is used by the Harris Chip to compensate
                    for the truncation due to the 5 stage decimation
                    filter
*/
```

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```
unsigned int determineHDFDataShift(unsigned int dec_factor)
{
    unsigned int dataShift;
    double       power;
    double       temp;

    /* Determine the Log2(dec_factor) */
    power = log10((double)dec_factor) / log10(2.0);

    /* Data shift = 75 - Ceiling(5*Log2(R))   */
    /*    R = Decimation Factor               */
    temp = 5.0 * power;
    dataShift = 75.0 - ceil(temp);
    if ((int)dataShift < 0)
      dataShift = 0;
    dataShift = dataShift << 1;

    return(dataShift);
}

/* determineScaleMult - This routine determines the scaling multiplier
                        which is used by the Harris Chip to compensate
                        for HDF Gain.
*/
double determineScaleMult(unsigned int dec_factor)
{
    double       power;
    int          power1;
    double       temp;
    double       fraction;
    double       ScaleMult;


    /* Determine the Log2(dec_factor) */
    power = log10((double)dec_factor) / log10(2.0);

    /* Determine if dec_factor is a factor of 2 */
    fraction = frexp((double) dec_factor, &power1);
    fraction *= 2.0;

    /* If decimation is a power of 2, then the scale multiplier is 1 */
    /* otherwise calculate the Scale Multiplier                      */
    /*     Scale Multiplier = 2**(Ceiling(5Log2(R))) / R**5          */
    /*           where R = decimation factor                         */
    if (fraction != 1.0)
    {
      temp = 5.0 * power;
      temp = ceil(temp);
      ScaleMult = pow(2.0, temp) / pow((double) dec_factor, 5.0);
    }
    else
      ScaleMult = 1.0;

    return(ScaleMult);
}
```

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```
void ResetFifo(unsigned int chan_select)
{
    unsigned int temp;
    unsigned int temp1;
    unsigned int iq_mask;
    unsigned int status_mask;
    unsigned int iq_state;

    /* Reset the Fifos */
    *Control = 0;

    /* Select the data source.  For the Harris Chips, Data can be */
    /* received from the channel C                                */
    if (DATA_SOURCE == CHANNEL_C)
      *Control |= CR_HRA_INPUT_SRC_C | CR_HRB_INPUT_SRC_C;

    if (chan_select == CHANNEL_C)
    {
      /* Save previous Filter Mode setting and turn off decimated clock.    */
      /* When the Fifo is Released, It is important that no Fifo writes are */
      /* occuring at the same time. A narrow write pulse may cause the fifo */
      /* to lose it's memory.  The same condition can occur after the fifo  */
      /* reaches a full condition and a sample is read from the fifo. For   */
      /* either case, it is recommended that the Filter Mode Register is    */
      /* cleared before releasing the fifo reset and reading samples from   */
      /* a full fifo.                                                       */

      temp = GrayC[CH_FILTER_MODE];
      GrayC[CH_FILTER_MODE] = 0x0;
    }

    /* Release Reset and Set non-packed data mode.  Data packing is  */
    /* a method of reading out the data from the fifo in an efficient */
    /* manner.  It does not affect how the data is acquired or stored */
    /* within the fifo.  In complex output mode, I and Q positioning  */
    /* must be determined before entering packed data mode.           */
    if (chan_select == CHANNEL_A)
    {
      /* Set Mask for determining IQ Ordering */
      iq_mask = SR_DATA_TYPE_A;
#if PACKED
      iq_state = HR_PACKED_IMAG_Q_DATA_A;
#else
      iq_state = HR_UNPACKED_IMAG_Q_DATA_A;
#endif

      /* Set Status Mask for Fifo Empty Flag  */
      status_mask = SR_FIFO_EMPTY_A;

        led_on();

      *Control |= (CR_FIFO_RELEASE_A | CR_HR_UNPACK_DATA_A | intr_mask);
    }
```

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```
    else if (chan_select == CHANNEL_B)
    {
      /* Set Mask for determining IQ Ordering */
      iq_mask = SR_DATA_TYPE_B;
#if PACKED
      iq_state = HR_PACKED_IMAG_Q_DATA_B;
#else
      iq_state = HR_UNPACKED_IMAG_Q_DATA_B;
#endif

      /* Set Status Mask for Fifo Empty Flag  */
      status_mask = SR_FIFO_EMPTY_B;

      *Control |= (CR_FIFO_RELEASE_B | CR_HR_UNPACK_DATA_B | intr_mask);
    }
    else
    {
      /* Set Mask for determining IQ Ordering */
      iq_mask = SR_DATA_TYPE_C;
#if PACKED
      iq_state = GC_PACKED_IMAG_Q_DATA_C;
#else
      iq_state = GC_UNPACKED_IMAG_Q_DATA_C;
#endif

      /* Set Status Mask for Fifo Empty Flag  */
      status_mask = SR_FIFO_EMPTY_C;

        led_on();
      *Control |= (CR_FIFO_RELEASE_C | CR_GC_UNPACK_DATA_C | intr_mask);

      /* Restore decimated clock and output mode */
      GrayC[CH_FILTER_MODE] = temp;
    }

    /* Wait for Fifo to have at least one sample */
    while ((*Status & status_mask) == 0);

    /* Read the first sample, this is necessary to update the Data */
    /* Type flag in the status register                            */
    temp1 = *Fifo;

    /* Read data until a first Real Sample */
    while (1)
    {
      /* Wait for Fifo to have at least one sample */
      while ((*Status & status_mask) == 0);

      /* While Status indicates next sample is Imaginary */
      /* Read the next sample and discard it             */
      if ((*Status & iq_mask) == iq_state)
         temp1 = *Fifo;
      else
         break;
    }
```

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```
#if PACKED
    /* Now that the proper sample order has been determined,  */
    /* Enter Packed Mode if selected                          */
    if (chan_select == CHANNEL_A)
      *Control &= ~CR_HR_UNPACK_DATA_A;
    else if (chan_select == CHANNEL_B)
      *Control &= ~CR_HR_UNPACK_DATA_B;
    else
      *Control &= ~CR_GC_UNPACK_DATA_C;
#endif
}

c_int01()
{
    unsigned int temp;
    int          num_samples;

    if (CHAN_SELECT == CHANNEL_C)
    {
      /* Since this example only requires 1K samples, turn off clock to */
      /* Graychip.  This will prevent fifo from a narrow write pulse    */
      /* when fifo fills up during data read out.                       */
      temp = GrayC[CH_FILTER_MODE];
      GrayC[CH_FILTER_MODE] = 0x0;
      /* Read out the data samples */
      (void) ReadSamples(Samples, samples_needed);
      /* Indicate to the main program that data is ready */
      data_ready = 1;
      /* Disable Interrupt */
      *Control &= ~intr_mask;
    }
    else     /* Channels A or B */
    {
      /* Determine how many samples left to read */
      if (samples_needed <= half_fifo_size)
          num_samples = samples_needed;
      else
          num_samples = half_fifo_size;
      /* Read the data from the fifo */
      samplesP = ReadSamples(samplesP, num_samples);
      /* Decrement number of samples needed */
      samples_needed -= num_samples;
      /* If all the samples have been gathered */
      if (samples_needed == 0)
      {
          /* Set Data Ready Flag */
          data_ready = 1;
          /* Disable Interrupt */
          *Control &= ~intr_mask;
      }
    }
    temp = *Status;           /* Clear interrupt latch */
    /* Clear Processor Interrupt */
    clearInterrupt();
}
```

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```
unsigned int *timer1_address = (unsigned int *)0x100030;
unsigned int *timer0_address = (unsigned int *)0x100020;
led_on()
{
      *timer1_address = 0x302u;               /* led ON  */
      *timer0_address = 0x302u;               /* led ON  */
}

led_off()
{
      *timer1_address = 0x306u;               /* led OFF  */
      *timer0_address = 0x306u;               /* led OFF  */
}

toggle_led()
{
      *timer1_address = ((*timer1_address & 0x306u) ^ 0x4);
}

/************************* End of File ****************************/
```

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```
/*********************************************************************
 * FILE: process.c
 * Description: Dynamically allocates Hanning and Sine Tables.
 * Requires FFT_SIZE * 3 of heap space.  The linker command file may
 * need to have its heap space increased accordingly.
 *********************************************************************/

#include <math.h>
#include <stdlib.h>
#include "mod.h"

#define FFT_NUM_STAGES  5
#define TWOPI   6.28318

/* Hanning and Sine Tables are dynamically allocated.  This program requires
   FFT_SIZE * 3 of heap space.  The linker command file may need to have its
   heap space increased accordingly.
*/
double  *hannWinP;
double  *sinTabP;
extern double  data_buf[];  /* This is defined in fft_c4.asm.  This buffer is
*/
                            /* allocated in it's own data section(.databuf)
*/
                            /* The FFT routine uses circular addressing which
*/
                            /* requires the N LSBs must be zero. N is an
*/
                            /* integer such that 2**N > R.  R is the size of
*/
                            /* data buffer.
*/

void ProcessData(int *sampleP, double *data_bufP, int num_samples)
{
     /* Perform a Hanning window on the data */
     performHannWindow(sampleP, data_bufP, hannWinP, num_samples);

     /* Perform a complex FFT on data */
     fft_c4(num_samples, FFT_NUM_STAGES, data_bufP, sinTabP);
}

InitFFTTables(int num_samples)
{
    /* Allocate the hanning table and sin tables */
    hannWinP = (double *) malloc(sizeof(double) * num_samples);
    sinTabP = (double *) malloc(sizeof(double) * num_samples * 2);

    /* Initialize the Sine Table */
    init_fft_sintab(sinTabP, num_samples);

    /* Calculate the Hanning Table */
    init_hanning(hannWinP, num_samples);
}
```

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```
void init_fft_sintab(double *sinTabP, int n)
{
    int    idx;
    double factor;
    double arg;
    factor = TWOPI / ((double) n);
    /* Calculate the Sine Table */
    for (idx = 0; idx < (n + (n >> 2)); idx++) /* 1 & 1/4 */
    {
      arg = ((double) idx) * factor;
      *sinTabP++ = sin(arg);
    }
}

void init_hanning(double *hannWinP, int n)
{
    int  idx;
    double factor;

    factor = 8.0 * atan(1.0) / (n - 1);

    /* Calculate the Hanning Window */
    for (idx = 0; idx < n; idx++)
    {
       *hannWinP++ = 0.5 - 0.5 * cos(factor * idx);
    }

}
void performHannWindow(int *sourceP, double *destP, double *hannWinP,
                  int num_samples)
{
    register int i;

    /* Convert the sample to floating point and multiply the */
    /* the sample by the hanning window coefficients         */
    for (i = 0; i < num_samples; ++i)
    {
      #if REAL
         *destP++ = (double)*sourceP++ * *hannWinP++;
         *destP++ = 0.0;
      #else
         *destP++ = (double)*sourceP++ * *hannWinP;
         *destP++ = (double)*sourceP++ * *hannWinP++;
    }
}
```

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```
/*********************************************************************
 * FILE: Display.c
 * Description: This file contains 4272 module Display Scaling
 * coefficients
 *********************************************************************/

#include <math.h>
#include "mod.h"

/* Display Scaling coefficients */
#define SCALE -300000000
#define OFFSET 750000000
#define PRESCALE 0.01

/* Addresses in Shared Memory used to communicate with host */
#if BB_4283
#define DATADR_ADR ((int  *) 0x208000)
#define FLAG       ((volatile int  *) 0x204000)
#else
#define DATADR_ADR ((int  *) 0x80008000)
#define FLAG       ((volatile int  *) 0x80004000)
#endif

void DisplayData(double *data_bufP, int num_samples)
{
     register int    i;
     register double xnew;
     register double ynew;
     register double *fftdataP;
     register int    *destP = DATADR_ADR;

     /* Handshake with the Host to determine if the host is finished */
     /* with buffer                                                  */
     *FLAG = 0;
     while (*FLAG == 0);

     /* Scale the data for the display */
     fftdataP = data_bufP;
     for (i = 0; i < num_samples / 2; i++)
     {
        xnew = *fftdataP++;
        ynew = *fftdataP++;
        xnew = (xnew + *fftdataP++) * 0.5 * PRESCALE;
        ynew = (ynew + *fftdataP++) * 0.5 * PRESCALE;
        (*destP++) = OFFSET + SCALE * log10((xnew*xnew)+(ynew*ynew));
     }
}
```

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```
/*************************************************************************
 * FILE: Intr.c
 * Description: Decides from the Information contained in mod.h which
 * Mix Interrupt should be enabled by the processor void
 * enableInterrupts()
 *************************************************************************/


#include "mod.h"

unsigned int *int01_vector;
extern int   c_int01();

/* This Routine decides from the Information contained in mod.h */
/* which Mix Interrupt should be enabled by the processor       */
void enableInterrupts()
{
#if BB_4283
    /* If the MOD_SELECT value used to select each MIX Module    */
    /* Position matches, then enable the corresponding Interrupt */
    if (MOD_SELECT == MOD0_SELECT)
        Init1();
    else if (MOD_SELECT == MOD1_SELECT)
        Init2();
    else
        Init3();
#endif
#if BB_4284 & !(MM_4270 | MM_425X)
    /* If the Base Address used to address each MIX Module       */
    /* Position matches, then enable the corresponding Interrupt */
    if (MOD == MOD0_ADDR)
        Init1();
    else if (MOD == MOD1_ADDR)
        Init2();
    else
        Init3();
#endif
#if MM_4270 | MM_425X
    /* Based on the position of the 4270 or 425X Mix Modules    */
    /* and position of the mix module generating the interrupts */
    /* enable the corresponding Interrupt                       */
    if (MIX_POS == 0)
    {
        if (MOD == MOD1_ADDR)
            IntInit2();
        else
            IntInit3();
    }
    else if (MIX_POS == 1)
    {
        if (MOD == MOD0_ADDR)
            IntInit3();
        else
            IntInit2();
    }
```

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```
    else
    {
        if (MOD == MOD0_ADDR)
            IntInit2();
        else
            IntInit3();
    }

#if BB_4200 | BB_4201
    /* If the BaseBoard is a 4200 or 4201, Disable the VIC Local Interrupt
       Control Registers from responding to the MIX Interrupt generated
       from the Mix Module
    */
    if (MOD == MOD0_ADDR)
       *(unsigned long *) 0xffff0009 = 0x80;
    else if (MOD == MOD1_ADDR)
       *(unsigned long *) 0xffff000a = 0x80;
    else
       *(unsigned long *) 0xffff000b = 0x80;
#endif

#endif
}
void clearInterrupt()
{

#if MM_4270 | MM_425X | BB_4284
    asm("   iack @0");     /* Clear Any Pending Interrupts */
#endif
#if BB_4283
    if (MOD_SELECT == MOD0_SELECT)
        *(int *)0x800000 = 0x0c;  /* Acknowledge 4283 interrupt processor */
    else if (MOD_SELECT == MOD1_SELECT)
        *(int *)0x800000 = 0x0a;  /* Acknowledge 4283 interrupt processor */
    else
        *(int *)0x800000 = 0x06;  /* Acknowledge 4283 interrupt processor */

    asm("       NOP");
    *(int *)0x800000 = 0x0e;   /* Re-arm 4283 interrupt processor */


    asm("   LDI 0,IF");        /* Clear out any spurious interrupts */
    asm("   LDI 0,IF");        /* Clear out any spurious interrupts */
#endif

}
```

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```
#if BB_4283 | BB_4284
void Init1()
{

#if BB_4283
      /* setup int 1 vector jump */
      *(int *)0x809804 = (int)&c_int01 | 0x60000000;

      *(int *)0x800000 = 0x00;      /* Arm IACK Pal */
      asm("       NOP");
      *(int *)0x800000 = 0x0e;

      /* enable interrupt 0 and 1 */

      asm("   LDI 0,IF");         /* Clear out any spurious interrupts */
      asm("   LDI 3,IE");
      asm("   OR 2000h,ST");
#else
        /* Enable C40 Int 0 as MixInt0 */
        *(unsigned int *) 0x10000003 = *(unsigned int *) 0x10000003 |
                                       0x00000008;

        int01_vector = (unsigned int *) c_int01;
        asm("   LDEP IVTP,AR0");
        asm("   LDI @_int01_vector,R0");
        asm("   STI R0,*+AR0(3)");
        asm("   IACK @0");
        asm("   LDI IIF,R0");
        asm("   ANDN 000fH,R0");
        asm("   OR 0009H,R0");
        asm("   LDI R0,IIF");
        asm("   OR 2000H,ST");
#endif
}


void Init2()
{
#if BB_4283
      /* setup int 2 vector jump */

        *(int *)0x809808 = (int)&c_int01 | 0x60000000;

      *(int *)0x800000 = 0x00;      /* Arm IACK Pal */
      asm("       NOP");
      *(int *)0x800000 = 0x0e;

    /* enable interrupt 0 and 2 */

      asm("   LDI 0,IF");         /* Clear out any spurious interrupts */
        asm("   LDI 5,IE");
      asm("   OR 2000h,ST");
```

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```
#else
        /* Enable C40 Int 2 as MixInt1 */
        *(unsigned int *) 0x10000003 = *(unsigned int *) 0x10000003 |
                                       0x00100000;

        int01_vector = (unsigned int *) c_int01;
        asm("   LDEP IVTP,AR0");
        asm("   LDI @_int01_vector,R0");
        asm("   STI R0,*+AR0(5)");
        asm("   IACK @0");
        asm("   LDI IIF,R0");
        asm("   ANDN 0f00H,R0");
        asm("   OR 0900H,R0");
        asm("   LDI R0,IIF");
        asm("   OR 2000H,ST");
#endif
}

void Init3()
{
#if BB_4283
      /* setup int 3 vector jump */

        *(int *)0x80980c = (int)&c_int01 | 0x60000000;

      *(int *)0x800000 = 0x00;      /* Arm IACK Pal */
      asm("       NOP");
      *(int *)0x800000 = 0x0e;

    /* enable interrupt 0 and 3 */

      asm("   LDI 0,IF");         /* Clear out any spurious interrupts */
        asm("   LDI 9,IE");
      asm("   OR 2000h,ST");
#else
        /* Enable C40 Int 3 as MixInt2 */
        *(unsigned int *) 0x10000003 = *(unsigned int *) 0x10000003 |
                                       0x20000000;

        int01_vector = (unsigned int *) c_int01;
        asm("   LDEP IVTP,AR0");
        asm("   LDI @_int01_vector,R0");
        asm("   STI R0,*+AR0(6)");
        asm("   IACK @0");
        asm("   LDI IIF,R0");
        asm("   ANDN 0f000H,R0");
        asm("   OR 09000H,R0");
        asm("   LDI R0,IIF");
        asm("   OR 2000H,ST");
#endif
}
#endif
```

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```
#if MM_4270 | MM_425X
void IntInit2()
{

    int01_vector = (unsigned int *) c_int01;
    asm("   LDEP IVTP,AR0");
    asm("   LDI @_int01_vector,R0");
    asm("   STI R0,*+AR0(6)");
    asm("   IACK @0");
    asm("   LDI IIF,R0");
    asm("   ANDN 0f000H,R0");
    asm("   OR 09000H,R0");
    asm("   LDI R0,IIF");
    asm("   OR 2000H,ST");
}
void IntInit3()
{

    int01_vector = (unsigned int *) c_int01;
    asm("   LDEP IVTP,AR0");
    asm("   LDI @_int01_vector,R0");
    asm("   STI R0,*+AR0(5)");
    asm("   IACK @0");
    asm("   LDI IIF,R0");
    asm("   ANDN 0f00H,R0");
    asm("   OR 0900H,R0");
    asm("   LDI R0,IIF");
    asm("   OR 2000H,ST");
}
#endif
```

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```
/*********************************************************************
 * File: fft_c4 --- radix-4 complex FFT to be called as a C function.
 *
 * Synopsis:
 *    int  fft_c4(N, M, data,sine)
 *    int  N          FFT size: N=4**M
 *    int  M          Number of stages = log4(N)
 *    float *data    Array with input and output data
 *    float *sine    Array with twiddle factors
 *
 * Description:  Generic function to do a radix-4 FFT computation on
 * the 320C30.  The data array is 2*N-long, with real and imaginary
 * values alternating.  The program is based on the FORTRAN program in
 * the Burrus and Parks book, p. 117. In order to have the final result
 * in bit-reversed order, the two middle branches of the radix-4
 * butterfly are interchanged during storage.  Note this difference
 * when comparing with the program in p. 117.  The computation is done
 * in place, and the original data is destroyed.  Bit reversal is
 * implemented at the end of the function.  If this is not necessary,
 * this part can be commented out. The sine/cosine table for the
 * twiddle factors should have the following format:
 * value1 = sin(0*2*pi/N) ,value2 = sin(1*2*pi/N) ,
 * value3 = sin(2*2*pi/N),
 * ..... value(5N/4) = sin((5*N/4-1)*2*pi/N).
 *
 * The values value1, value2, etc., are the sine wave values.  For an
 * N-point FFT, there are N+N/4 values for a full and a quarter period
 * of the sine wave.  In this way, a full sine and cosine period are
 * available (superimposed).
 *
 * Stack structure upon the call:
 *                +--------------+
 *    -FP(5)      |    sine      |
 *    -FP(4)      |    data      |
 *    -FP(3)      |    M         |
 *    -FP(2)      |    N         |
 *    -FP(1)      | return addr  |
 *    -FP(0)      |   old FP     |
 *                +--------------+
 *
 * Registers used: R0, R1, R2, R3, R4, R5, R6, R7, AR0, AR1, AR2, AR3, AR4,
 *    AR5, AR6, AR7, IR0, IR1, RS, RE, RC
 *
 * AUTHOR: PANOS E. PAPAMICHALIS
 *      TEXAS INSTRUMENTS                    OCTOBER 13, 1987
 *
 * Update: Daniel Mazzocco                          April 2nd, 1992
 *         Fixed a compilation & a functional bug.
 *         Added Sine table address as a function argument.
 *********************************************************************/
 *
FP   .set      AR3

      .GLOBL      _fft_c4           ; ENTRY POINT FOR EXECUTION
        .GLOBL  _data_buf
```

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```
      .BSS   FFTSIZ,1
      .BSS   LOGFFT,1
      .BSS   INPUT,1
        .BSS   SINTAB,1

_data_buf:      .usect  ".databuf",4096 ; Data buffer
        .TEXT

;   INITIALIZE C FUNCTION

_fft_c4:  PUSH        FP              ; SAVE DEDICATED REGISTERS
        LDI           SP,FP
        PUSH          R4
        PUSH          R5
        PUSHF     R6
        PUSHF     R7
        PUSH          AR4
        PUSH          AR5
        PUSH          AR6
        PUSH          AR7

        LDI           *-FP(2),R0      ; MOVE ARGUMENTS TO LOCATIONS MATCHING
        STI           R0,@FFTSIZ      ;  THE NAMES IN THE PROGRAM
        LDI           *-FP(3),R0
        STI           R0,@LOGFFT
        LDI           *-FP(4),R0
        STI           R0,@INPUT
          LDI       *-FP(5),R0
          STI       R0,@SINTAB

; INITIALIZE FFT ROUTINE

        .BSS          STAGE,1         ; FFT STAGE #
        .BSS          RPTCNT,1        ; REPEAT COUNTER
        .BSS          IEINDX,1        ; IE INDEX FOR SINE/COSINE
        .BSS          LPCNT,1         ; SECOND-LOOP COUNT
        .BSS          JT,1       ; JT COUNTER IN PROGRAM, P. 117
        .BSS          IA1,1      ; IA1 INDEX IN PROGRAM, P. 117

      LDI   @FFTSIZ,R0
      LDI   @FFTSIZ,IR0
      LDI   @FFTSIZ,IR1
      LDI   0,AR7
      STI   AR7,@STAGE  ; @STAGE HOLDS THE CURRENT STAGE NUMBER
      LSH   1,IR0              ; IR0=2*N1 (BECAUSE OF REAL/IMAG)
      LSH   -2,IR1            ; IR1=N/4, POINTER FOR SIN/COS TABLE
      LDI   1,AR7
      STI   AR7,@RPTCNT       ; INITIALIZE REPEAT COUNTER OF FIRST LOOP
      LSH   -2,R0
      STI   AR7,@IEINDX       ; INITIALIZE IE INDEX
      ADDI  2,R0
      STI   R0,@JT               ; JT=R0/2+2
      SUBI  2,R0
      LSH   1,R0           ; R0=N2
```

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```
;   OUTER LOOP

LOOP:
      LDI   @INPUT,AR0  ; AR0 POINTS TO X(I)
      ADDI  R0,AR0,AR1  ; AR1 POINTS TO X(I1)
      ADDI  R0,AR1,AR2  ; AR2 POINTS TO X(I2)
      ADDI  R0,AR2,AR3  ; AR3 POINTS TO X(I3)
      LDI   @RPTCNT,RC
      SUBI  1,RC        ; RC SHOULD BE ONE LESS THAN DESIRED #

; FIST LOOP

      RPTB   BLK1
      ADDF   *+AR0,*+AR2,R1         ; R1=Y(I)+Y(I2)
      ADDF   *+AR3,*+AR1,R3         ; R3=Y(I1)+Y(I3)
      ADDF   R3,R1,R6         ; R6=R1+R3
      SUBF   *+AR2,*+AR0,R4         ; R4=Y(I)-Y(I2)
      STF    R6,*+AR0         ; Y(I)=R1+R3
      SUBF   R3,R1                  ; R1=R1-R3
      LDF    *AR2,R5                ; R5=X(I2)
||    LDF    *+AR1,R7         ; R7=Y(I1)
      ADDF   *AR3,*AR1,R3           ; R3=X(I1)+X(I3)
      ADDF   R5,*AR0,R1             ; R1=X(I)+X(I2)
||    STF    R1,*+AR1         ; Y(I1)=R1-R3
      ADDF   R3,R1,R6         ; R6=R1+R3
      SUBF   R5,*AR0,R2             ; R2=X(I)-X(I2)
||    STF    R6,*AR0++(IR0)         ; X(I)=R1+R3
      SUBF   R3,R1                  ; R1=R1-R3
      SUBF   *AR3,*AR1,R6           ; R6=X(I1)-X(I3)
      SUBF   R7,*+AR3,R3            ; -R3=Y(I1)-Y(I3)  !!!
||    STF    R1,*AR1++(IR0)         ; X(I1)=R1-R3
      SUBF   R6,R4,R5         ; R5=R4-R6
      ADDF   R6,R4                  ; R4=R4+R6
      STF    R5,*+AR2         ; Y(I2)=R4-R6
||    STF    R4,*+AR3         ; Y(I3)=R4+R6
      SUBF   R3,R2,R5         ; R5=R2-R3  !!!
      ADDF   R3,R2                  ; R2=R2+R3  !!!
BLK1  STF    R5,*AR2++(IR0)         ; X(I2)=R2-R3  !!!
||    STF    R2,*AR3++(IR0)         ; X(I3)=R2+R3  !!!

; IF THIS IS THE LAST STAGE, YOU ARE DONE

      LDI    @STAGE,AR7
      ADDI   1,AR7
      CMPI   @LOGFFT,AR7
      BZD    END
      STI    AR7,@STAGE             ; CURRENT FFT STAGE

; MAIN INNER LOOP

         LDI       1,AR7
       STI          AR7,@IA1           ; INIT IA1 INDEX
       LDI          2,AR7
       STI          AR7,@LPCNT         ; INIT LOOP COUNTER FOR INNER LOOP
```

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```
INLOP:
        LDI         2,AR6           ; INCREMENT INNER LOOP COUNTER
        ADDI        @LPCNT,AR6
        LDI         @LPCNT,AR0
        LDI         @IA1,AR7
        ADDI        @IEINDX,AR7     ; IA1=IA1+IE
        ADDI        @INPUT,AR0          ; (X(I),Y(I)) POINTER
        STI         AR7,@IA1
        ADDI        R0,AR0,AR1          ; (X(I1),Y(I1)) POINTER
        STI         AR6,@LPCNT
        ADDI        R0,AR1,AR2          ; (X(I2),Y(I2)) POINTER
        ADDI        R0,AR2,AR3          ; (X(I3),Y(I3)) POINTER
        LDI         @RPTCNT,RC
        SUBI        1,RC        ; RC SHOULD BE ONE LESS THAN DESIRED #
        CMPI        @JT,AR6             ; IF LPCNT=JT, GO TO
        BZD         SPCL        ;    SPECIAL BUTTERFLY
        LDI         @IA1,AR7
        LDI         @IA1,AR4
        ADDI        @SINTAB,AR4 ; CREATE COSINE INDEX AR4
          SUBI      1,AR4             ; fix initial bug
        ADDI        AR4,AR7,AR5
        SUBI        1,AR5       ; IA2=IA1+IA1-1
        ADDI        AR7,AR5,AR6
        SUBI        1,AR6       ; IA3=IA2+IA1-1

; SECOND LOOP

        RPTB        BLK2
        ADDF        *+AR2,*+AR0,R3      ; R3=Y(I)+Y(I2)
        ADDF        *+AR3,*+AR1,R5      ; R5=Y(I1)+Y(I3)
        ADDF        R5,R3,R6            ; R6=R3+R5
        SUBF        *+AR2,*+AR0,R4      ; R4=Y(I)-Y(I2)
        SUBF        R5,R3       ; R3=R3-R5
        ADDF        *AR2,*AR0,R1 ; R1=X(I)+X(I2)
        ADDF        *AR3,*AR1,R5 ; R5=X(I1)+X(I3)
        MPYF        R3,*+AR5(IR1),R6    ; R6=R3*CO2
||      STF         R6,*+AR0            ; Y(I)=R3+R5
        ADDF        R5,R1,R7            ; R7=R1+R5
        SUBF        *AR2,*AR0,R2 ; R2=X(I)-X(I2)
        SUBF        R5,R1       ; R1=R1-R5
        MPYF        R1,*AR5,R7          ; R7=R1*SI2
||      STF         R7,*AR0++(IR0)      ; X(I)=R1+R5
        SUBF        R7,R6       ; R6=R3*CO2-R1*SI2
        SUBF        *+AR3,*+AR1,R5      ; R5=Y(I1)-Y(I3)
        MPYF        R1,*+AR5(IR1),R7    ; R7=R1*CO2
||      STF         R6,*+AR1            ; Y(I1)=R3*CO2-R1*SI2
        MPYF        R3,*AR5,R6          ; R6=R3*SI2
        ADDF        R7,R6       ; R6=R1*CO2+R3*SI2
        ADDF        R5,R2,R1            ; R1=R2+R5
        SUBF        R5,R2       ; R2=R2-R5
        SUBF        *AR3,*AR1,R5 ; R5=X(I1)-X(I3)
        SUBF        R5,R4,R3            ; R3=R4-R5
        ADDF        R5,R4       ; R4=R4+R5
        MPYF        R3,*+AR4(IR1),R6    ; R6=R3*CO1
||      STF         R6,*AR1++(IR0)      ; X(I1)=R1*CO2+R3*SI2
```

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```
        MPYF        R1,*AR4,R7          ; R7=R1*SI1
        SUBF        R7,R6         ; R6=R3*CO1-R1*SI1
        MPYF        R1,*+AR4(IR1),R6    ; R6=R1*CO1
||      STF         R6,*+AR2            ; Y(I2)=R3*CO1-R1*SI1
        MPYF        R3,*AR4,R7          ; R7=R3*SI1
        ADDF        R7,R6         ; R6=R1*CO1+R3*SI1
        MPYF        R4,*+AR6(IR1),R6    ; R6=R4*CO3
||      STF         R6,*AR2++(IR0)      ; X(I2)=R1*CO1+R3*SI1
        MPYF        R2,*AR6,R7          ; R7=R2*SI3
        SUBF        R7,R6         ; R6=R4*CO3-R2*SI3
        MPYF        R2,*+AR6(IR1),R6    ; R6=R2*CO3
||      STF         R6,*+AR3            ; Y(I3)=R4*CO3-R2*SI3
        MPYF        R4,*AR6,R7          ; R7=R4*SI3
        ADDF        R7,R6         ; R6=R2*CO3+R4*SI3
BLK2    STF         R6,*AR3++(IR0)      ; X(I3)=R2*CO3+R4*SI3

      CMPI  @LPCNT,R0
      BP    INLOP                 ; LOOP BACK TO THE INNER LOOP
      BR    CONT

;    SPECIAL BUTTERFLY FOR W=J

SPCL    LDI         IR1,AR4
        LSH         -1,AR4        ; POINT TO SIN(45)
        ADDI        @SINTAB,AR4   ; CREATE COSINE INDEX AR4=CO21

        RPTB        BLK3
        ADDF        *AR2,*AR0,R1  ; R1=X(I)+X(I2)
        SUBF        *AR2,*AR0,R2  ; R2=X(I)-X(I2)
        ADDF        *+AR2,*+AR0,R3      ; R3=Y(I)+Y(I2)
        SUBF        *+AR2,*+AR0,R4      ; R4=Y(I)-Y(I2)
        ADDF        *AR3,*AR1,R5  ; R5=X(I1)+X(I3)
        SUBF        R1,R5,R6            ; R6=R5-R1
        ADDF        R5,R1         ; R1=R1+R5
        ADDF        *+AR3,*+AR1,R5      ; R5=Y(I1)+Y(I3)
        SUBF        R5,R3,R7            ; R7=R3-R5
        ADDF        R5,R3         ; R3=R3+R5
        STF         R3,*+AR0            ; Y(I)=R3+R5
||      STF         R1,*AR0++(IR0)      ; X(I)=R1+R5
        SUBF        *AR3,*AR1,R1  ; R1=X(I1)-X(I3)
        SUBF        *+AR3,*+AR1,R3      ; R3=Y(I1)-Y(I3)
        STF         R6,*+AR1            ; Y(I1)=R5-R1
||      STF         R7,*AR1++(IR0)      ; X(I1)=R3-R5
        ADDF        R3,R2,R5            ; R5=R2+R3
        SUBF        R2,R3,R2            ; R2=-R2+R3 !!!
        SUBF        R1,R4,R3            ; R3=R4-R1
        ADDF        R1,R4         ; R4=R4+R1
        SUBF        R5,R3,R1            ; R1=R3-R5
        MPYF        *AR4,R1             ; R1=R1*CO21
        ADDF        R5,R3         ; R3=R3+R5
        MPYF        *AR4,R3             ; R3=R3*CO21
||      STF         R1,*+AR2            ; Y(I2)=(R3-R5)*CO21
        SUBF        R4,R2,R1            ; R1=R2-R4  !!!
        MPYF        *AR4,R1             ; R1=R1*CO21
||      STF         R3,*AR2++(IR0)      ; X(I2)=(R3+R5)*CO21
```

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```
        ADDF        R4,R2          ; R2=R2+R4  !!!
        MPYF        *AR4,R2             ; R2=R2*CO21  !!!
BLK3    STF         R1,*+AR3            ; Y(I3)=-(R4-R2)*CO21  !!!
||      STF         R2,*AR3++(IR0)      ; X(I3)=(R4+R2)*CO21  !!!

      CMPI  @LPCNT,R0
      BPD   INLOP                   ; LOOP BACK TO THE INNER LOOP
CONT    LDI         @RPTCNT,AR7
        LDI         @IEINDX,AR6
        LSH         2,AR7      ; INCREMENT REPEAT COUNTER FOR NEXT TIME
        STI         AR7,@RPTCNT
        LSH         2,AR6          ; IE=4*IE
        STI         AR6,@IEINDX
        LDI         R0,IR0         ; N1=N2
        LSH         -3,R0
        ADDI        2,R0
        STI         R0,@JT         ; JT=N2/2+2
        SUBI        2,R0
        LSH         1,R0           ; N2=N2/4
        BR      LOOP           ; NEXT FFT STAGE

; DO THE BIT-REVERSING OF THE OUTPUT

END:  LDI   @FFTSIZ,RC         ; RC=N
      SUBI  1,RC         ; RC SHOULD BE ONE LESS THAN DESIRED #
      LDI   @FFTSIZ,IR0              ; IR0=SIZE OF FFT=N
      LDI   @INPUT,AR0
      LDI   @INPUT,AR1

        RPTB    BITRV
      CMPI  AR0,AR1
        BGE     CONT1
      LDF   *AR0,R0
||    LDF   *AR1,R1
      STF   R0,*AR1
||    STF   R1,*AR0
      LDF   *+AR0(1),R0
||    LDF   *+AR1(1),R1
      STF   R0,*+AR1(1)
||    STF   R1,*+AR0(1)
CONT1   NOP     *++AR0(2)
BITRV       NOP   *AR1++(IR0)B

; RESTORE THE REGISTER VALUES AND RETURN

        POP         AR7
        POP         AR6
        POP         AR5
        POP         AR4
        POPF        R7
        POPF        R6
        POP         R5
        POP         R4
        POP         FP
        RETS
```

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```
;=========================================================================
 ; FILE: util.asm
 ;=========================================================================

;
FP              .set        ar3         ; FP is AR3

        .global _fdiv
        .global DIV_F

*************************************************************************
*  fdiv - Floating point division
*************************************************************************
        .text
_fdiv:  PUSH    FP              ; Preserve C environment.
            LDI     SP,FP

            LDF     *-FP(2),R0      ; move numerator off stack
            LDF     *-FP(3),R1      ; move denominator off stack

        CALL    DIV_F           ; call floating point division routine

;
; Return to C environment.
;

            POP     FP
            RETS

            .end
```

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Appendix B: Alternate Input Configurations

B.1 Differential ECL Input Configuration (Option 012)

The Differential ECL input option for the Model 4272 differs from the standard (single-ended TTL) configuration in several areas. The Mezzanine board for this configuration is full-sized, meaning that it reaches all the way from the card cage front panel to the VMEbus backplane. In fact, the Mezzanine board for the Model 4272 Option 012 actually connects to, and draws power from, the VME backplane. (No connections are made to any of the VME data, address, or control signals. Only power connections are made, to provide the voltage rails for the ECL/TTL level translators.) This Mezzanine Board is shown in Figure B-2, on Page B-3. **Note that there are NO CONFIGURATION JUMPERS in this version.**

The other major difference is the pinout of the input connectors, which is shown in Figure B-1, on Page B-2. These differences are discussed in the section below.

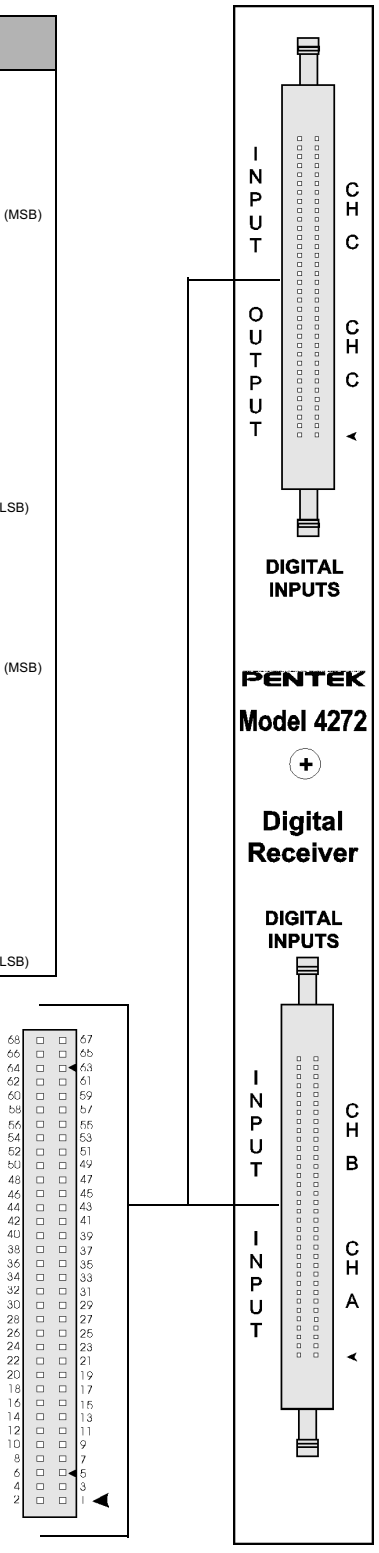
B.1.1 Input Connectors

Figure B-1, Page B-2, shows the Input Connector pinouts for Option 012 for the Model 4272. Note that the grounds that separated the single-ended input lines in the standard configuration (see Figure 2-1 on Page B-18 in the main body of this manual) have been replaced in this arrangement by the complementary signals.

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Top Differential Input/Output Connector Wudeband Channel (C)			
68	GND	67	GND
66	Ch C - GS in	65	Ch C - $\overline{GS}$ in
64	Ch C - $\overline{CK}$ in	63	Ch C - CK in
62	Ch C - AS in	61	Ch C - $\overline{AS}$ in
60	Ch C - SS in	59	Ch C - $\overline{SS}$ in
58	Ch C - $\overline{D11}$ in (MSB)	57	Ch C - D11 in (MSB)
56	Ch C - $\overline{D10}$ in	55	Ch C - D10 in
54	Ch C - $\overline{D9}$ in	53	Ch C - D9 in
52	Ch C - $\overline{D8}$ in	51	Ch C - D8 in
50	Ch C - $\overline{D7}$ in	49	Ch C - D7 in
48	Ch C - $\overline{D6}$ in	47	Ch C - D6 in
46	Ch C - $\overline{D5}$ in	45	Ch C - D5 in
44	Ch C - $\overline{D4}$ in	43	Ch C - D4 in
42	Ch C - $\overline{D3}$ in	41	Ch C - D3 in
40	Ch C - $\overline{D2}$ in	39	Ch C - D2 in
38	Ch C - $\overline{D1}$ in	37	Ch C - D1 in
36	Ch C - $\overline{D0}$ in (LSB)	35	Ch C - D0 in (LSB)
34	GND	33	GND
32	$\overline{FRST}$	31	$\overline{FRD}$
30	GND	29	GND
28	Sync Out	27	$\overline{FF}$
26	$\overline{HF}$	25	$\overline{EF}$
24	GND	23	GND
22	GND	21	GND
20	Ch C - D15 out (MSB)	19	Ch C - D14 out
18	Ch C - D13 out	17	Ch C - D12 out
16	Ch C - D11 out	15	Ch C - D10 out
14	Ch C - D9 out	13	Ch C - D8 out
12	GND	11	GND
10	GND	9	GND
8	Ch C - D7 out	7	Ch C - D6 out
6	Ch C - D5 out	5	Ch C - D4 out
4	Ch C - D3 out	3	Ch C - D2 out
2	Ch C - D1 out	1	Ch C - D0 out (LSB)

Bottom Differential Input Connector Channels A and B			
68	GND	67	GND
66	GND	65	N/C
64	Ch B - $\overline{CK}$ in	63	Ch B - CK in
62	Ch B - AS in	61	Ch B - $\overline{AS}$ in
60	Ch B - SS in	59	Ch B - $\overline{SS}$ in
58	Ch B - $\overline{D11}$ in (MSB)	57	Ch B - D11 in (MSB)
56	Ch B - $\overline{D10}$ in	55	Ch B - D10 in
54	Ch B - $\overline{D9}$ in	53	Ch B - D9 in
52	Ch B - $\overline{D8}$ in	51	Ch B - D8 in
50	Ch B - $\overline{D7}$ in	49	Ch B - D7 in
48	Ch B - $\overline{D6}$ in	47	Ch B - D6 in
46	Ch B - $\overline{D5}$ in	45	Ch B - D5 in
44	Ch B - $\overline{D4}$ in	43	Ch B - D4 in
42	Ch B - $\overline{D3}$ in	41	Ch B - D3 in
40	Ch B - $\overline{D2}$ in	39	Ch B - D2 in
38	Ch B - $\overline{D1}$ in	37	Ch B - D1 in
36	Ch B - D0 in (LSB)	35	Ch B - D0 in (LSB)
34	GND	33	GND
32	GND	31	GND
30	Ch A - $\overline{CK}$ in	29	Ch A - CK in
28	Ch A - AS in	27	Ch A - $\overline{AS}$ in
26	Ch A - SS in	25	Ch A - $\overline{SS}$ in
24	Ch A - $\overline{D11}$ in (MSB)	23	Ch A - D11 in (MSB)
22	Ch A - $\overline{D10}$ in	21	Ch A - D10 in
20	Ch A - $\overline{D9}$ in	19	Ch A - D9 in
18	Ch A - $\overline{D8}$ in	17	Ch A - D8 in
16	Ch A - $\overline{D7}$ in	15	Ch A - D7 in
14	Ch A - $\overline{D6}$ in	13	Ch A - D6 in
12	Ch A - $\overline{D5}$ in	11	Ch A - D5 in
10	Ch A - $\overline{D4}$ in	9	Ch A - D4 in
8	Ch A - $\overline{D3}$ in	7	Ch A - D3 in
6	Ch A - $\overline{D2}$ in	5	Ch A - D2 in
4	Ch A - $\overline{D1}$ in	3	Ch A - D1 in
2	Ch A - D0 in (LSB)	1	Ch A - D0 in (LSB)



The mating flat cable socket connector is 3M #82068-6006 and the strain relief is 3M #3858-068.

Two each of these items are supplied with the Model 4272.

The recommended 0.025 in. pitch flat cable is 3M #3756/68.

Figure B-1: Model 4272 - Front Panel Input Connector Pin Assignment - ECL Differential Inputs (Option 012)

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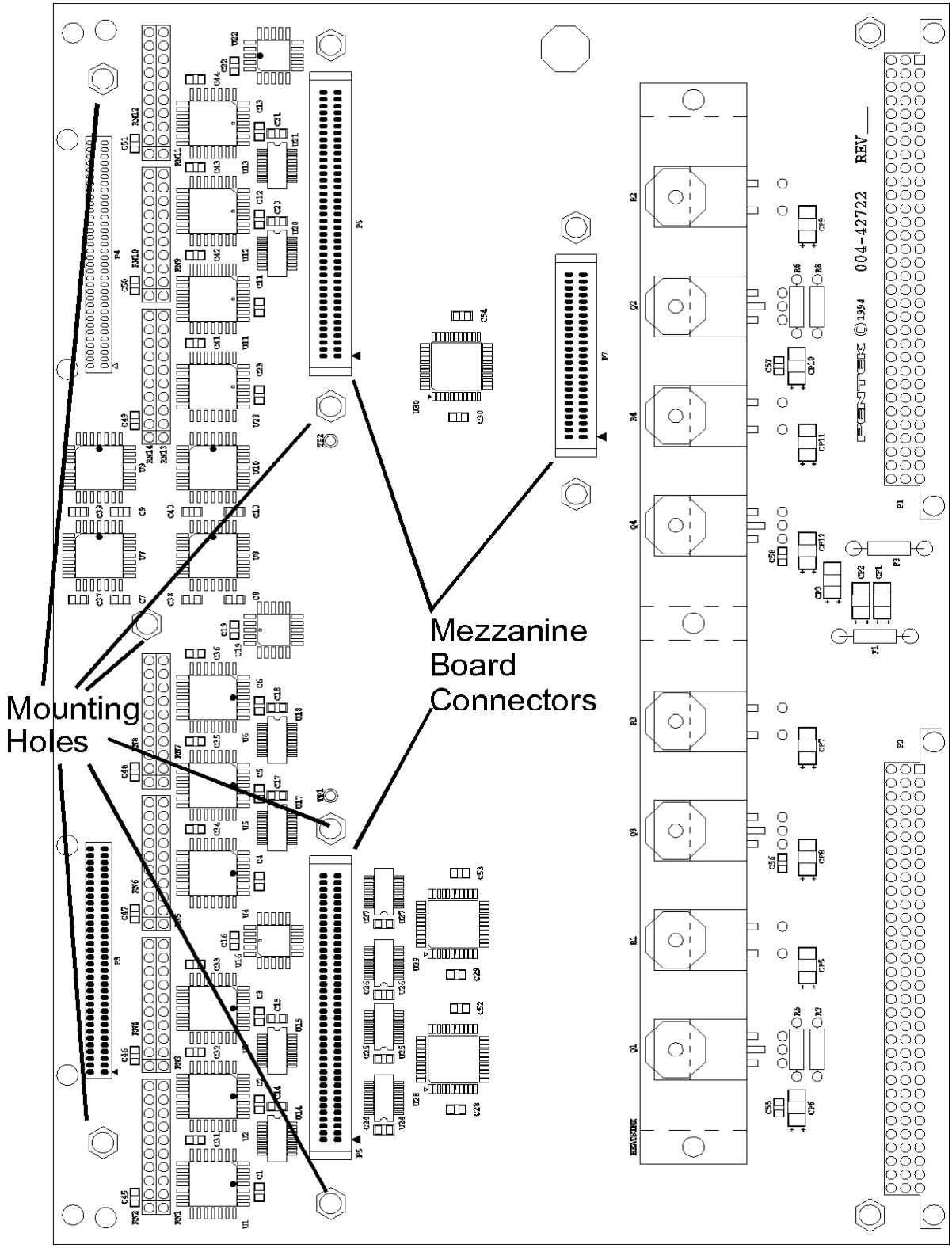


Figure B-2: Model 4272, Option 012 - Mezzanine Board - Connector and Mounting Locations - Differential ECL Input

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B.2 16-Bit TTL Input Configuration (Option 019)

This input configuration was designed for use with either Pentek's 64xx series of A/D converters, or the Pentek Model 4261 Option 019, as the source of digital input data. In either case, some special cabling between the A/D and the receiver may be necessary. Figure B-3 on Page B-5, gives the pinout of the two front panel connectors for this option. Note that 80 pin connectors are used for this option, as opposed to the 68-pin connectors used on the standard units. The 3M part number for the male connector on the 4272 Option 019 is #81080-620203. The 3M part number for the mating ribbon cable connector is #82080-6006, and the strain relief is 3M #3858-080. Figure B-4, on Page B-6, shows a picture of the mezzanine board used with this option.

The other difference between units equipped with Option 019 and the standard Model 4272 Multiband Digital Receiver is the addition of extended input multiplexing capabilities. In the subsections that follow, we will first discuss the multiplexing issue, and then deal with interfacing issues between the 4272 Option 019 and its intended front end devices.

B.2.1 Input Multiplexing with Option 019

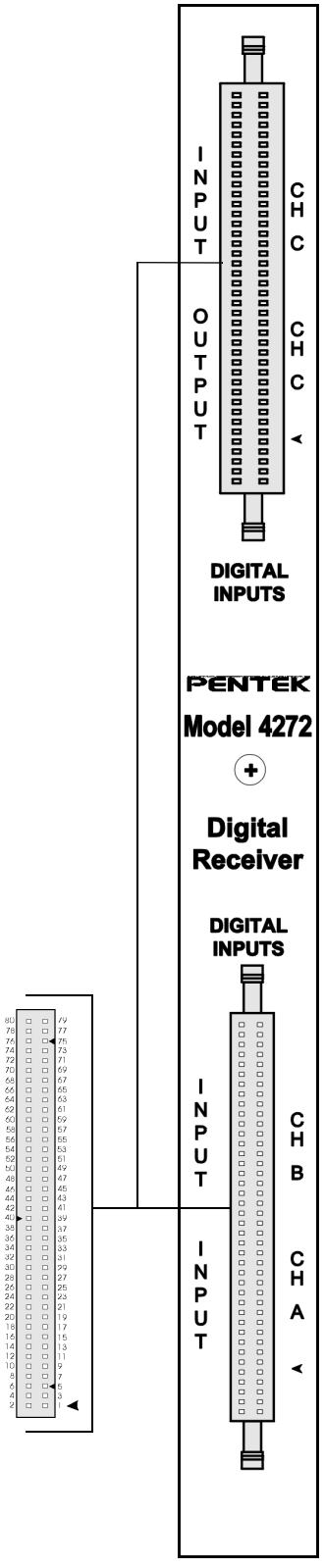
As mentioned above, Option 019 extends the input multiplexing capabilities of the standard Model 4272. In the standard unit, the input for either narrowband channel (A or B) may be taken either from its the data presented at its own dedicated front-panel input pins, or from the input presented to the wideband channel (C). In option 019, the input data presented at either narrowband input may also be used to drive both narrowband channels.

The input multiplexing function is still controlled by bits D30 and D29 in the Control Register, at symbolic address Control_Reg. However, instead of each bit selecting the input source for a single channel (see Section 3.3.12, Page B-41), the two bits are used in combination to control the inputs to both channels. For Option 019, these two bits are renamed Input MUX 1 and Input MUX 0. Table B-1, at the top of Page B-7, is a reprint of Table 3-2 on Page B-30, which defines the bit arrangement of the Control Register, with the changed bits shown in Italic print. Table B-2, below Table B-1, tell how to program these bits to select which channel is driven from which front panel input port.

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Top Differential Input/Output Connector Wudeband Channel (C)			
80	GND	79	Ch C - D3 in
78	GND	77	Ch C - D2 in
76	GND	75	Ch C - D1 in
74	GND	73	Ch C - $\overline{GS}$ in
72	GND	71	Ch C - D0 in (LSB)
70	GND	69	Ch C - CK in
68	GND	67	Ch C - $\overline{AS}$ in
66	GND	65	Ch C - $\overline{SS}$ in
64	GND	63	Ch C - D15 in (MSB)
62	GND	61	Ch C - D14 in
60	GND	59	Ch C - D13 in
58	GND	57	Ch C - D12 in
56	GND	55	Ch C - D11 in
54	GND	53	Ch C - D10 in
52	GND	51	Ch C - D9 in
50	GND	49	Ch C - D8 in
48	GND	47	Ch C - D7 in
46	GND	45	Ch C - D6 in
44	GND	43	Ch C - D5 in
42	GND	41	Ch C - D4 in
40	GND	39	GND
38	GND	37	Ch C - D0 out (LSB)
36	GND	35	$\overline{FF}$
34	GND	33	$\overline{HF}$
32	GND	31	$\overline{EF}$
30	GND	29	Ch C - D15 out (MSB)
28	GND	27	Ch C - D14 out
26	GND	25	Ch C - D13 out
24	GND	23	Ch C - D12 out
22	GND	21	Ch C - D11 out
20	GND	19	Ch C - D10 out
18	GND	17	Ch C - D9 out
16	GND	15	Ch C - D8 out
14	GND	13	Ch C - D7 out
12	GND	11	Ch C - D6 out
10	GND	9	Ch C - D5 out
8	GND	7	Ch C - D4 out
6	$\overline{FRST}$	5	Ch C - D3 out
4	$\overline{FRD}$	3	Ch C - D2 out
2	Sync Out	1	Ch C - D1 out

Bottom Differential Input Connector Channels A and B			
80	GND	79	Ch B - D3 in
78	GND	77	Ch B - D2 in
76	GND	75	Ch B - D1 in
74	GND	73	GND
72	GND	71	Ch B - D0 in (LSB)
70	GND	69	Ch B - CK in
68	GND	67	Ch B - $\overline{AS}$ in
66	GND	65	Ch B - $\overline{SS}$ in
64	GND	63	Ch B - D15 in (MSB)
62	GND	61	Ch B - D14 in
60	GND	59	Ch B - D13 in
58	GND	57	Ch B - D12 in
56	GND	55	Ch B - D11 in
54	GND	53	Ch B - D10 in
52	GND	51	Ch B - D9 in
50	GND	49	Ch B - D8 in
48	GND	47	Ch B - D7 in
46	GND	45	Ch B - D6 in
44	GND	43	Ch B - D5 in
42	GND	41	Ch B - D4 in
40	GND	39	GND
38	GND	37	Ch A - D0 out (LSB)
36	GND	35	Ch A - CK in
34	GND	33	Ch A - $\overline{AS}$ in
32	GND	31	Ch A - $\overline{SS}$ in
30	GND	29	Ch A - D15 in (MSB)
28	GND	27	Ch A - D14 in
26	GND	25	Ch A - D13 in
24	GND	23	Ch A - D12 in
22	GND	21	Ch A - D11 in
20	GND	19	Ch A - D10 in
18	GND	17	Ch A - D9 in
16	GND	15	Ch A - D8 in
14	GND	13	Ch A - D7 in
12	GND	11	Ch A - D6 in
10	GND	9	Ch A - D5 in
8	GND	7	Ch A - D4 in
6	GND	5	Ch A - D3 in
4	GND	3	Ch A - D2 in
2	GND	1	Ch A - D1 in



The mating flat cable socket connector is 3M #82068-6006 and the strain relief is 3M #3858-080.

Two each of these items are supplied with the Model 4272.

The recommended 0.025 in. pitch flat cable is 3M #3756/80.

Figure B-3: Model 4272 - Front Panel 80-pin Input Connector Pin Assignment - 16-bit TTL Inputs - (Option 019)

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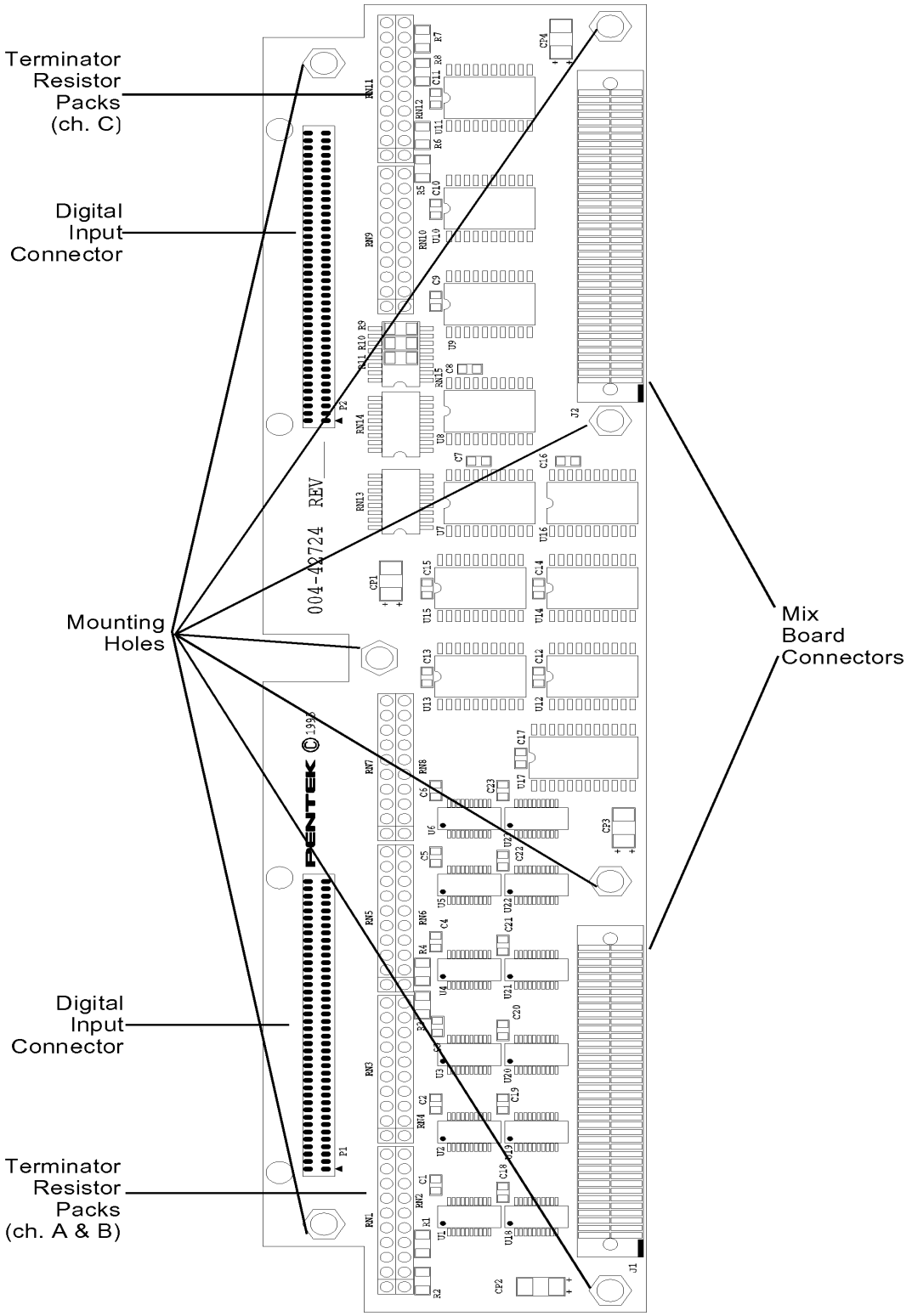


Figure B-4: Model 4272 Option 019 - Mezzanine Board - Connector and Mounting Locations - 16-bit TTL Input

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B.2 16-Bit TTL Input Configuration (Option 019) (continued)

B.2.1 Input Multiplexing with Option 019 (continued)

Table B-1: Model 4272, Option 019 - Control Register - Read/Write @ Control_Reg

Ch. C Bits	D31	D30	D29	D28	D27	D26	D25	D24
Function	N/U	Input Mux 1	Input Mux 0	N/U	Graychip Software GainSync	Graychip SW System Sync	Graychip SW Accumulator Sync	Graychip Sync Source
Logic '1'	-	See	See	-	Run	Run	Run	Front Panel
Logic '0"	-	Table B-2	Table B-2	-	Set Gain	Sync	Set Freq.	Software
Ch. C Bits	D23	D22	D21	D20	D19	D18	D17	D16
Function	Interrupt Mask Bits					Packed Data Mode	Front Panel Output	Graychip FIFO Reset
	FIFO FULL	FIFO Half Full	FIFO Not Empty	Overflow Flag	Graychip Interrupt			
Logic '1'	Enabled	Enabled	Enabled	Enabled	Enabled	Disabled	Enabled	Release
Logic '0'	Disabled	Disabled	Disabled	Disabled	Disabled	Enabled	Disabled	Reset
Ch. B Bits	D15	D14	D13	D12	D11	D10	D9	D8
Ch. A Bits	D7	D6	D5	D4	D3	D2	D1	D0
Function	Interrupt Mask Bits			Packed Data Mode	Command Shift Mode	Harris Reset Source	Harris Internal Reset	Harris FIFO Reset
	FIFO FULL	FIFO Half Full	FIFO Not Empty					
Logic '1'	Enabled	Enabled	Enabled	Enabled	Disabled	External	Reset	Release
Logic '0'	Disabled	Disabled	Disabled	Disabled	Enabled	Internal	Release	Reset

Table B-2: Model 4272, Option 019 - Input Multiplexing - Control Register (Control_Reg), bits D30 and D29

Input MUX 1 (D30)	Input MUX 0 (D29)	Channel A Input from...	Channel B Input from...
0	0	A In	B In
0	1	A In	A In
1	0	B In	B In
1	1	C In	C In

B.2.2 Interfacing with 64xx Series A/D Converters

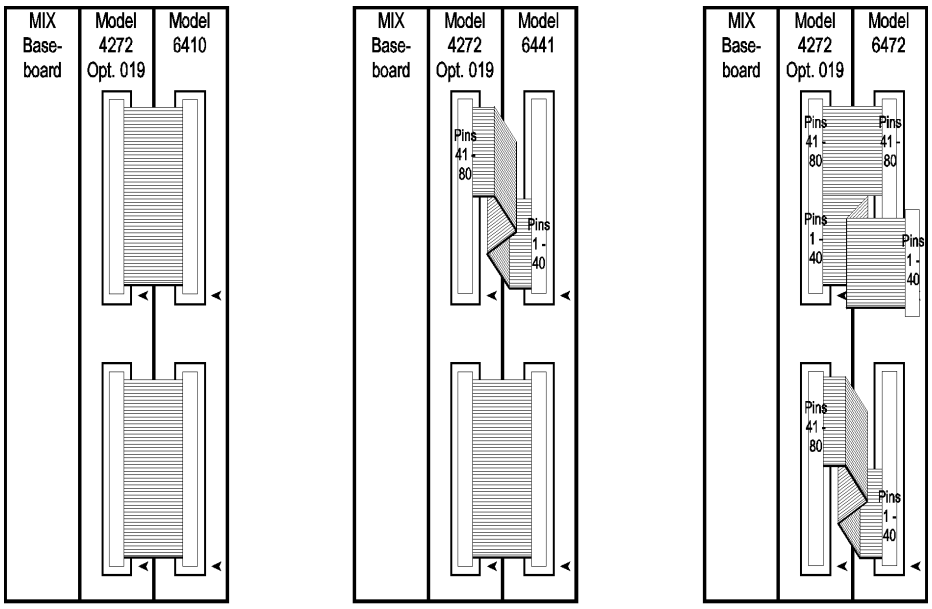
Pentek's 64xx Series are Dual-Channel, A/D Converter VMEbus boards, designed specifically to be used as a front end for Pentek's 4272 and 4271 Digital Receiver MIX Modules. These devices are essentially non-programmable, and use the VMEbus only to provide power. Output data is delivered to a front-panel parallel port at the input sample rate, with no handshaking signals. Using a 64xx as a front end for the 4272 Option 019 is a simple matter of connecting the cables between the units properly.

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B.2 16-Bit TTL Input Configuration (Option 019) (continued)

B.2.2 Interfacing with 64xx Series A/D Converters (continued)

Both of the 80-pin output data connectors on the Model 64xx's front panel carry data from both channels, and the pinout of these connectors matches the arrangement of the 4272's narrowband input connector exactly. Thus, an 80-pin cable may be connected directly between the two lower connectors on the 6410 and the 4272. If desired, either channel of the 64xx's output data may be used as the input to both of the 4272's narrowband channels by programming the input select multiplexer accordingly (see Section B.2.1, above). When connecting the 4272's wideband channel to the 64xx, remember that most of the pins on the lower half of the wideband connector (pins 1-40) carry output signals, driven by the 4272. The user must either leave these pins unconnected to the 64xx, or make sure that the output drivers are not enabled (they are disabled by default at reset, see Section 3.3.6). Some possible cabling schemes for interfacing the 64xx to the 4272 Option 019 are shown in Figure B-5, below.



(a) 64xx channel 1 drives 4272 A inputs, 64xx channel 2 drives 4272 B and C inputs NOTE: 4272 outputs **MUST** be disabled in this configuration

(b) 64xx channel 1 drives 4272 A and C inputs, 64xx channel 2 drives 4272 B inputs

(c) 64xx channel 1 drives 4272 B input, 64xx Channel 2 drives 4272 C input, cabling provided for 4272 outputs

Figure B-5: Model 4272 Option 019 - Cabling Schemes for Interfacing with Model 64xx

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B.2 16-Bit TTL Input Configuration (Option 019) (continued)

B.2.3 Interfacing with the Model 4261 Option 019

The Model 4261 is a 10 MHz, 12- or 14-bit A/D Converter VMEbus board, with a dual, swinging buffer memory arrangement. The swinging buffer allows new data to be written into one buffer by the A/D, while previously-acquired data is read out of the other buffer by the system controller. The data may be read over the VMEbus or from a front-panel parallel output port. Option 019 for the Model 4261 adds extends the features of the parallel port by adding a direct A/D readout (bypassing the memory buffers). When used with the Model 4272 Option 019, the direct A/D output from the 4261 may drive the wideband (channel C) input of the receiver, and used to determine which band(s) of the delayed data (from the memory buffers) will be focused on by the narrowband channel(s) (i. e., channels A and/or B).

Figure B-6, to the right, shows the cabling arrangement for using the Model 4261 Option 019 as a front end for the Model 4272 Option 019. As the figure shows, the 80-line ribbon cable connected to the 4261's front panel port must be split down the middle (i. e., between pins 40 and 41). The upper 40 (pins 41 - 80) wires carry the direct, unbuffered A/D data, and should be connected to the wideband (channel C) input port of the 4272 (pins 41 - 80 of the 4272's upper connector). The lower 40 pins 0f the 4261's output port carry the delayed data from the swinging memory buffers. These pins must be connected to the A input port of the 4272, as the figure shows (the 4261's pinout does not match up with the B input port). The input data may then be directed to the other channel as well, by programming the multiplexer (see Section B.2.1).

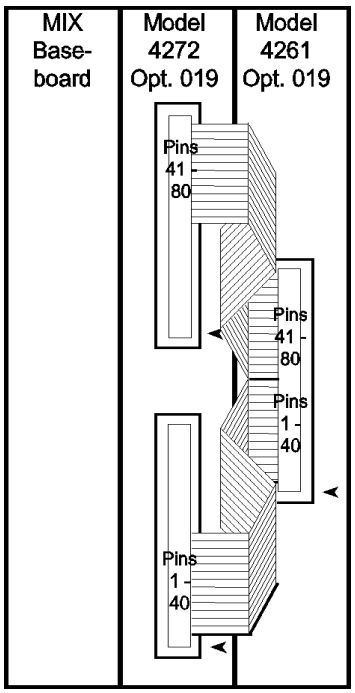


Figure B-6: Model 4272 Option 019 - Cabling for Interface with Model 4261 Option 019

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Appendix C: Harris HSP50016 Digital Down Converter

C.1 Introduction

The following section contains the data sheet for the Harris HSP50016 Digital Down Converter.

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Digital Down Converter

The Digital Down Converter (DDC) is a single chip synthesizer, quadrature mixer and lowpass filter. Its input data is a sampled data stream of up to 16 bits in width and up to a 75 MSPS data rate. The DDC performs down conversion, narrowband low pass filtering and decimation to produce a baseband signal.

The internal synthesizer can produce a variety of signal formats. They are: CW, frequency hopped, linear FM up chirp, and linear FM down chirp. The complex result of the modulation process is lowpass filtered and decimated with identical real filters in the in-phase (I) and quadrature (Q) processing chains.

Lowpass filtering is accomplished via a High Decimation Filter (HDF) followed by a fixed Finite Impulse Response (FIR) filter. The combined response of the two stage filter results in a -3dB to -102dB shape factor of better than 1.5. The stopband attenuation is greater than 106dB. The composite passband ripple is less than 0.04dB. The synthesizer and mixer can be bypassed so that the chip operates as a single narrow band low pass filter.

The chip receives forty bit serial commands as a control input. This interface is compatible with the serial I/O port available on most microprocessors.

The output data can be configured in fixed point or single precision floating point. The fixed point formats are 16, 24, 32, or 38-bit, two's complement, signed magnitude, or offset binary.

The circuit provides an IEEE 1149.1 Test Access Port.

Features

- 75 MSPS Input Data Rate
- 16-Bit Data Input; Offset Binary or 2's Complement Format
- Spurious Free Dynamic Range Through Modulator >102dB
- Frequency Selectivity: <0.006Hz
- Identical Lowpass Filters for I and Q
- Passband Ripple: <0.04dB
- Stopband Attenuation: >104dB
- Filter -3dB to -102dB Shape Factor: <1.5
- Decimation Factors from 32 to 131,072
- IEEE 1149.1 Test Access Port
- HSP50016-EV Evaluation Board Available

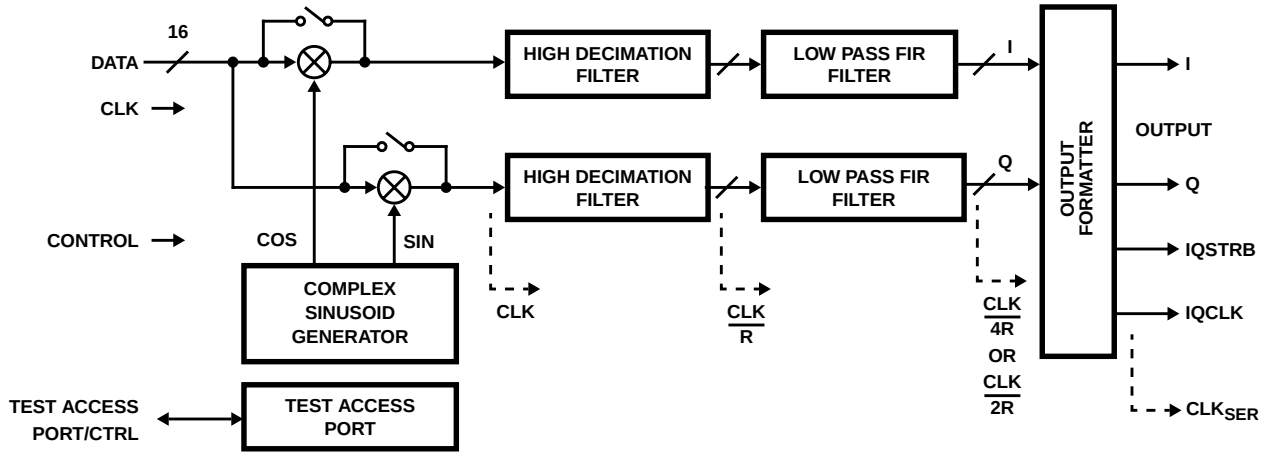
Applications

- Cellular Base Stations
- Smart Antennas
- Channelized Receivers
- Spectrum Analysis
- Related Products: HI5703, HI5746, HI5766 A/Ds

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP50016JC-52	0 to 70	44 Ld PLCC	N44.65
HSP50016JC-75	0 to 70	44 Ld PLCC	N44.65
HSP50016GC-52	0 to 70	48 Ld CPGA	G48.A

Block Diagram

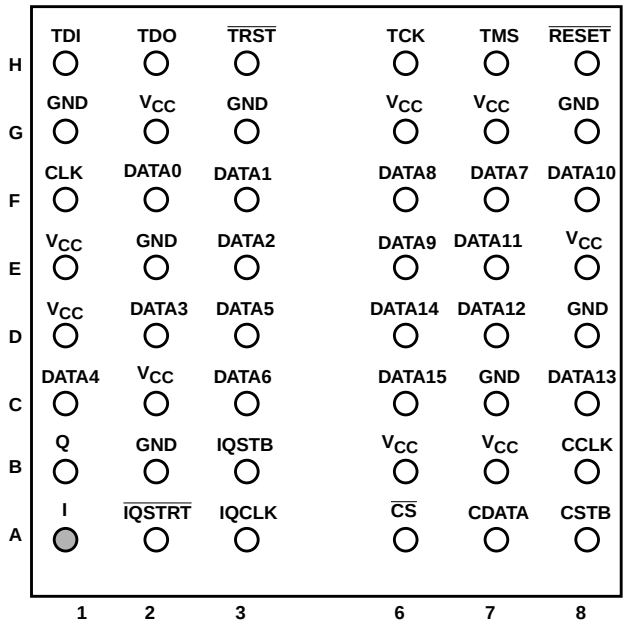


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Pinouts

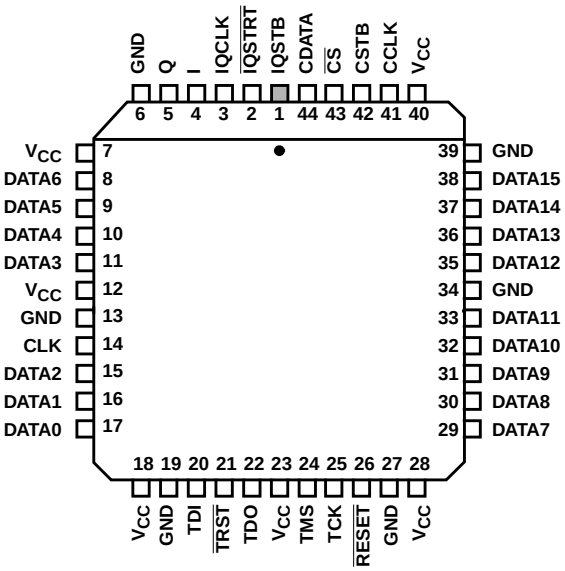
48 PIN CPGA
BOTTOM VIEW



48 PIN CPGA
TOP VIEW

	1	2	3		6	7	8
A	I	IQSTRT	IQCLK		CS	CDATA	CSTB
B	Q	GND	IQSTB		V_{CC}	V_{CC}	CCLK
C	DATA4	V_{CC}	DATA6		DATA15	GND	DATA13
D	V_{CC}	DATA3	DATA5		DATA14	DATA12	GND
E	V_{CC}	GND	DATA2		DATA9	DATA11	V_{CC}
F	CLK	DATA0	DATA1		DATA8	DATA7	DATA10
G	GND	V_{CC}	GND		V_{CC}	V_{CC}	GND
H	TDI	TDO	TRST		TCK	TMS	RESET

44 LEAD PLCC
TOP VIEW



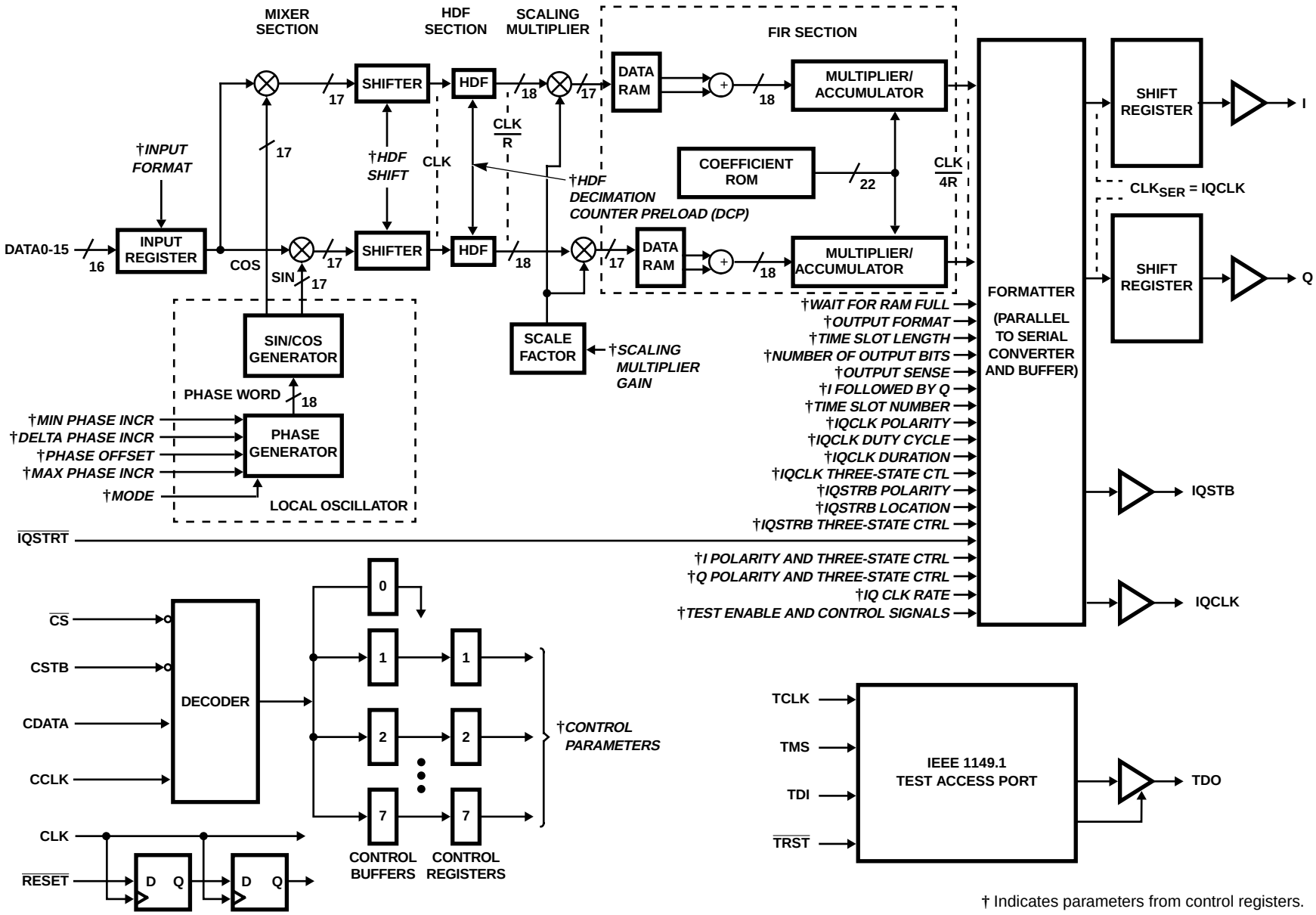
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Pin Description

NAME	TYPE	DESCRIPTION
V_{CC}	-	+5V Power.
GND	-	Ground.
DATA0-15	I	Input Data Bus. Selectable between two's complement and offset binary. DATA0 is the LSB.
CLK	I	Clock for input data bus. f_S is the frequency of CLK, which is also the input sample rate.
$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$ initializes the internal state of the DDC. During $\overline{\text{RESET}}$, all internal processing stops. $\overline{\text{RESET}}$ facilitates the synchronization of multiple chips for Auto Three-State operation. If the Force bits in Control Word 7 are inactive and the IEEE Test Access Port is in an Idle state, $\overline{\text{RESET}}$ causes the IQCLK, IQSTB, I and Q outputs to go to a high impedance state. All Control Registers are updated from their respective Control Buffer Registers on the third rising edge of CLK after the deassertion of $\overline{\text{RESET}}$. If $\overline{\text{RESET}}$ is deasserted t_{RS} nanoseconds prior to the rising edge of CLK, the internal reset will deassert synchronously. If t_{RS} is violated, then the circuit contains a synchronizer which will cause reset to be deasserted internally one or more clocks later. An initial reset is required to guarantee proper operation of the DDC. Active low.
I	O	The I output has three modes: I data; I data followed by Q data; real data.
Q	O	The Q output has two modes: Q data and the carry out of the Phase Adder.
IQCLK	O	IQ Clock: Bit or word clock for the I and Q outputs.
IQSTB	O	IQ Strobe: Beginning or end of word indicator for I and Q.
$\overline{\text{IQSTRT}}$	I	IQ Start: Initiates output data sequence. Active low.
CDATA	I	Control Data: Port for control data input.
CCLK	I	Control Data Clock: Control data input bit clock.
CSTB	I	Control Data Strobe: Beginning of word indicator for control data.
$\overline{\text{CS}}$	I	Chip Select: Enables control data loading of DDC. Active low.
TCK	I	Test Clock: Bit Clock for IEEE 1149.1 Data. This signal should be either tied low or pulled high when the TAP is not used.
TMS	I	Test Port Mode Select: This signal should be either left unconnected or pulled high when the TAP is not used.
TDI	I	Test Data Input for IEEE Test Port: This signal should be either left unconnected or pulled high when the TAP is not used.
TDO	O	Test Data Output for IEEE Test Port: This output will be in the high impedance state when the TAP is not used.
$\overline{\text{TRST}}$	I	Test Port Reset. Active Low. This signal should be tied low when the TAP is not used.

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DDC Functional Block Diagram

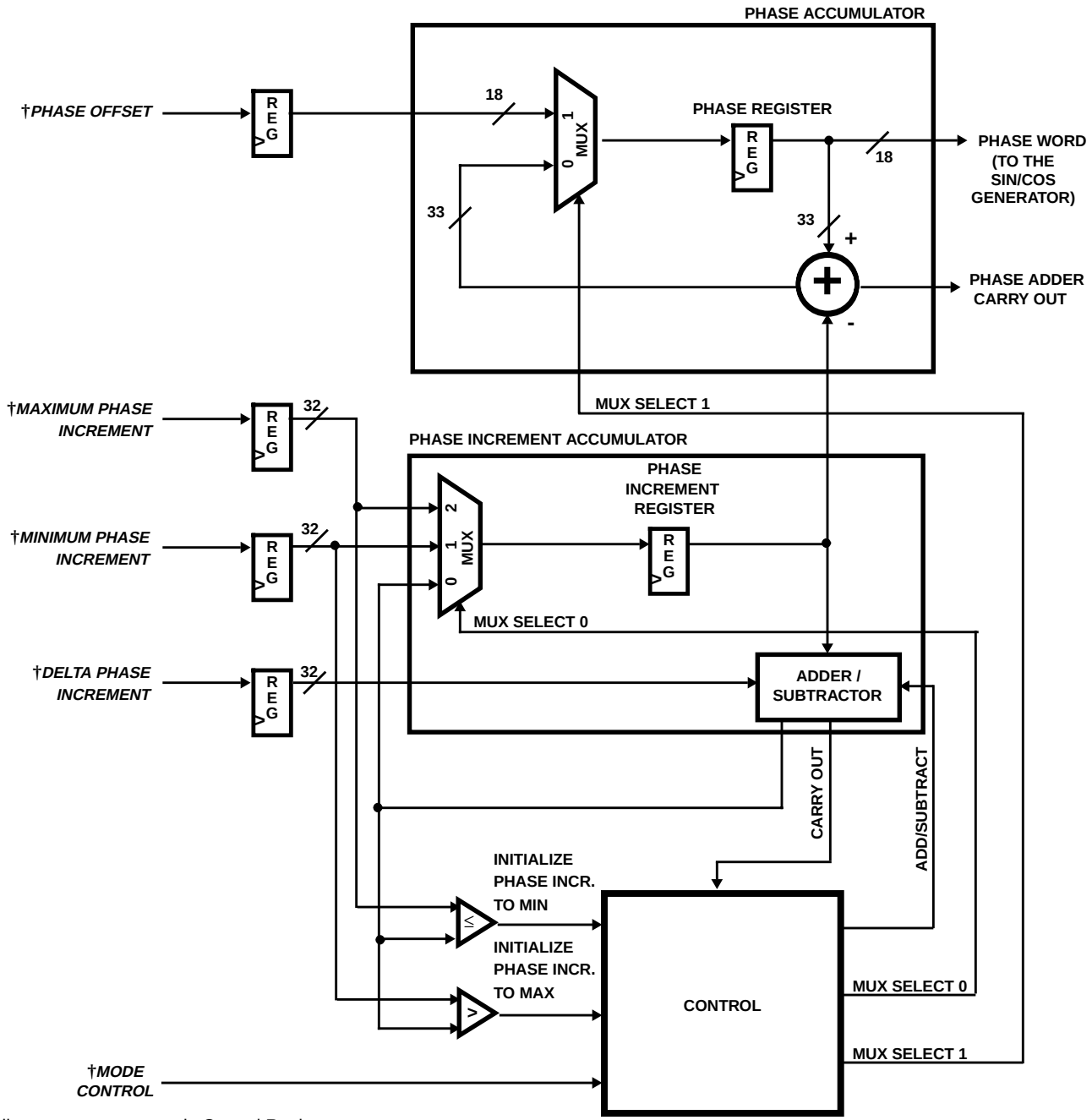


† Indicates parameters from control registers.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

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Phase Generator Block Diagram



† Indicates parameters set in Control Registers.

FIGURE 2. PHASE GENERATOR BLOCK DIAGRAM

Functional Description

The primary function of the DDC is to extract a narrow frequency band of interest from a wideband input, convert that band to baseband and output it in either a quadrature or real form. This narrow band extraction is accomplished by down converting and centering the band of interest at DC. The conversion is done by multiplying the input data with a quadrature sinusoid. A quadrature lowpass filter is applied to the multiplier outputs. Identical real lowpass filters are provided in the in-phase (I) and quadrature phase (Q) processing branches. Each filtering chain consists of a cascaded HDF and FIR filter, which extracts the band of interest. During filtering, the signal is decimated by a rate which is proportional to the output bandwidth. The bandwidth of the resulting signal is the double sided passband width of the lowpass filters. An Output Formatter manipulates the filter output to provide the data in a variety of serial data formats.

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Local Oscillator

Signal data clocked into the DATA0-15 input of the DDC is multiplied by a quadrature sinusoid in the Mixer Section (see Figure 1). The data input to the DDC is a 16-bit real data stream which is sampled on the rising edges of CLK. It can be in two's complement or offset binary format.

The input data is passed to a mixer, which is composed of two real multipliers. One of these multiplies the input data samples by the in-phase (cosine) component of the quadrature sinusoid, and the other multiplies the input data samples by the quadrature (sine) component. The in-phase and quadrature data paths are designated I and Q respectively. The sine and cosine are generated in the local oscillator as shown in Figure 1.

The local oscillator is programmed to produce a quadrature sinusoid with programmable frequency and phase. The frequency can be constant (Continuous Wave - CW), linearly increasing (up chirp), linearly decreasing (down chirp), or linear up/down chirp. The initial phase of the waveform is set by the phase offset.

The phase, frequency and chirp limits of the quadrature sinusoid are controlled by the Phase Generator (Figure 2). The output of the Phase Generator is an 18-bit phase word that represents the current phase angle of the complex sinusoid. The Phase Generator automatically increments the phase angle by a preprogrammed amount on every rising edge of CLK. Stepping the output phase from 0 through full scale (2^{18} - 1) steps the phase angle of the quadrature sinusoid from 0 to $(-2+2^{-17})\pi$ radians. ***NOTE: The phase is stepped in a clockwise (decreasing) direction to support down conversion.*** The frequency of the complex sinusoid is determined by the number of clocks needed for the phase to step though its full range of 2π radians. The required phase increment for a given local oscillator frequency is calculated by:

$$\text{Phase Increment} = \text{INT}\left[(f_C/f_S)\,2^{33}\right]\text{H} \qquad \text{(EQ. 1)}$$

$$f_C = (\text{Phase Incr})\,f_S\,2^{-33};\ 0 < f_C < f_S/2$$

where:

f_C is the desired local oscillator frequency

f_S is the input sampling frequency

Phase Increment is the Control Word Value (in Hex)

There are five parameters which control the Phase Generator: Phase offset, minimum phase increment, maximum phase increment, delta phase increment and Mode Control. These values are programmed via Control Words 2, 3, and 4. Mode Control is used to select the function of the other parameters.

The phase offset is the initial setting of the phase word going to the SIN/COS Generator. Subsequent phases of the sinusoid are calculated relative to this offset. The minimum phase increment has two mode dependent functions: when the SIN/COS Generator is forming a CW waveform, the minimum phase increment is the phase step taken on every clock. When the SIN/COS Generator is producing a chirped sinusoid, the minimum phase increment is the smallest phase step taken. Maximum phase increment is only used during Chirped Modes; it is the largest allowable phase increment. During Chirp Modes, the delta phase increment is the difference between successive phase increments.

The four phase parameters are stored in their respective registers in the Phase Generator. The Phase Register stores the current phase angle. On the first clock following the deassertion of $\overline{\text{RESET}}$, the 18 MSBs of the Phase Register are loaded from the Phase Offset Register. On every rising edge of CLK thereafter, the output of the Phase Increment Register is subtracted from the 32 LSBs of the current phase. The 33-bit difference is stored back in the Phase Register on the next CLK. The 18 most significant bits of the Phase Register form the phase word, which is the input to the SIN/COS Generator.

Figure 3 gives a graphic representation of the phase parameters for the CW case. To understand their interrelationships, the phase should be visualized as the angle of a rotating vector. When the local oscillator in the DDC is programmed to generate a CW waveform, the multiplexers are configured so that the Minimum Phase Increment is stored in the Phase Increment Register; this value is subtracted from the output of the Phase Register on every CLK and the difference becomes the new Phase Register value. The Delta Phase Increment and Maximum Phase Increment are ignored when generating a CW.

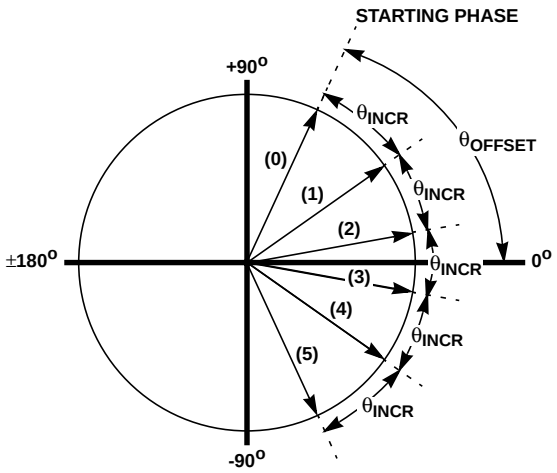


FIGURE 3. PHASE WORD PARAMETERS FOR CW CASE

In Up Chirp Mode the local oscillator generates a signal with a linearly increasing frequency (Figure 4A). The Phase Increment Register is initially loaded with the minimum Phase Increment value; on every clock, the contents of the Phase Increment Register is subtracted from the current output of the Phase Register. Simultaneously, the Delta

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Phase Increment Register is added to the 24 LSBs of the output of the Phase Increment Register. On the next CLK, that sum is stored back in the Phase Increment Register, the new phase is stored in the Phase Register and the process is repeated. The phase increment is allowed to grow until the next phase increment would equal or exceed the maximum phase increment value. When this happens, the Phase Increment Register is reset to the minimum phase increment and the cycle starts over again.

NOTE: The phase increment is never equal to the maximum phase increment, since the Phase Increment Register is reloaded if the next phase increment value would be greater than the maximum phase increment.

From the time the Phase Generator starts at the minimum phase increment until it reaches the maximum phase increment, the phase word on clock n is given by:

$$\text{Phase Word} = \text{Phase Offset} - [\text{Minimum Phase Increment} + n\ (\text{Delta Phase Increment})] \quad \text{(EQ. 2)}$$

An example of the outputs of the Phase Increment Register, Phase Register, and the I output of the SIN/COS Generator are shown in Figure 4B.

In Down Chirp Mode the local oscillator generates a signal with a linearly decreasing frequency (Figure 5A). The maximum phase increment is loaded into the Phase Increment Register and the phase offset value goes into the Phase Register. The delta phase increment is subtracted from the 24 LSBs of the phase increment to form a new phase increment at each clock. The phase increment is allowed to diminish until it reaches the minimum phase increment value, then it is reset to the maximum phase increment value and the cycle is repeated. Note that the value of the phase increment can be equal to, but never less than the minimum phase increment, since the Phase Increment Register is reloaded if the next phase increment value would be less than the minimum phase increment. This feature protects the DDC from exceeding the Nyquist frequency. In this case, from the time the Phase Generator starts at the maximum phase increment until it reaches the minimum phase increment, the phase word on clock n is given by:

$$\text{Phase Word} = \text{Phase Offset} - [\text{Minimum Phase Increment} - n\ (\text{Delta Phase Increment})] \quad \text{(EQ. 3)}$$

See Figure 5B for a graphical representation of this process.

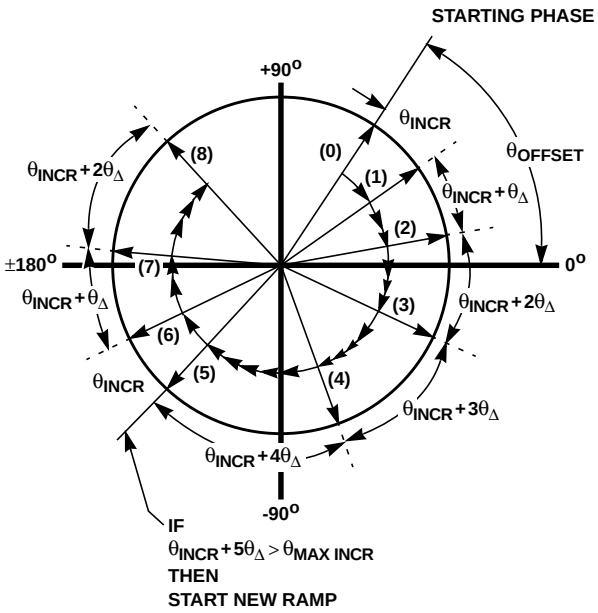


FIGURE 4A. PHASE WORD DURING UP CHIRP

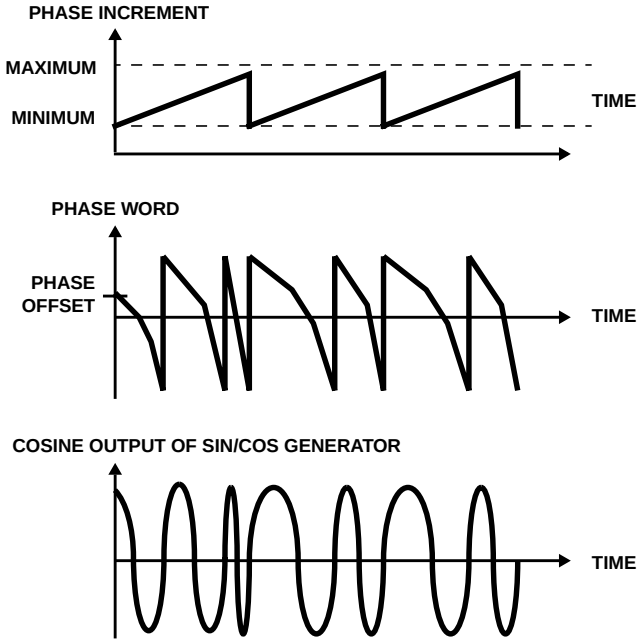


FIGURE 4B. UP CHIRP

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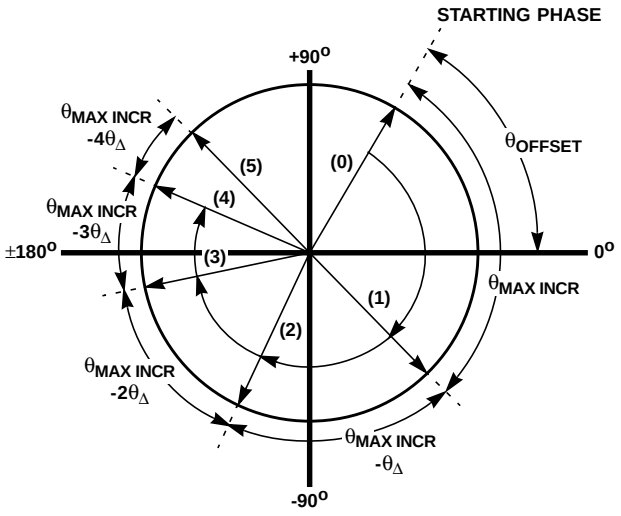


FIGURE 5A. PHASE WORD DURING DOWN CHIRP

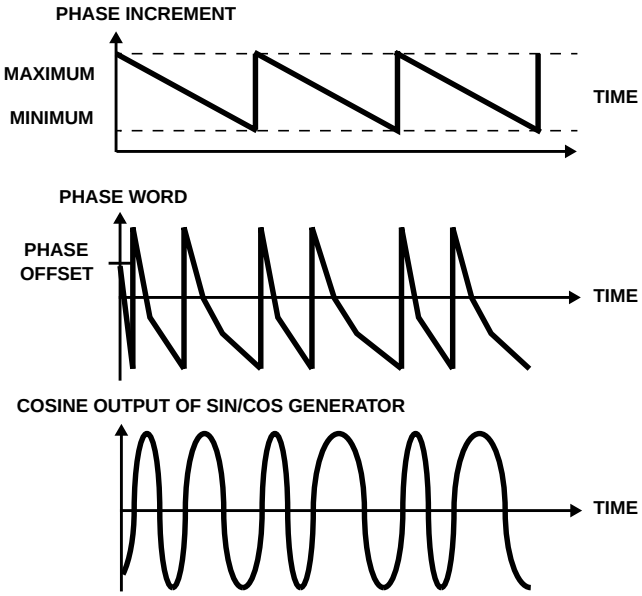


FIGURE 5B. DOWN CHIRP

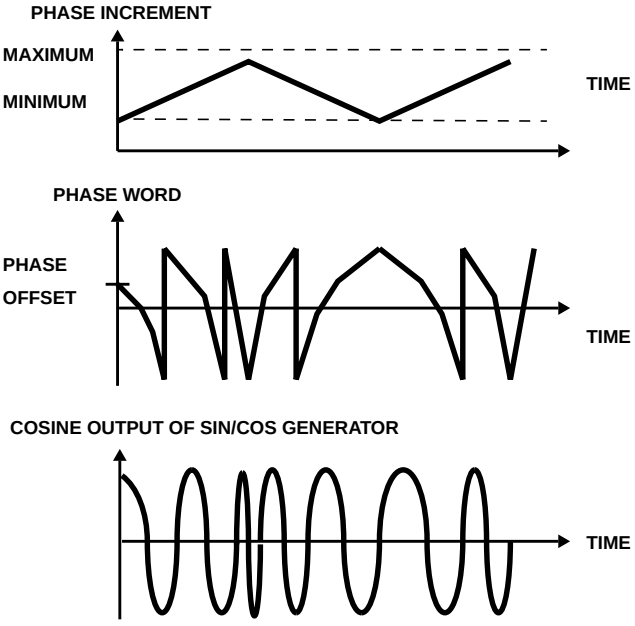


FIGURE 6. UP/DOWN CHIRP

In Up/down Chirp Mode, the phase accumulator is set to the phase offset value and the minimum phase increment is loaded into the Phase Increment Register. The delta phase increment is added to the 24 LSBs of the Phase Increment Register to form a new phase increment at each clock. The phase increment is allowed to grow until it nears the maximum phase increment value (as defined in the up chirp description). The delta phase increment value is then subtracted from the least significant bits of the Phase Increment Register to form a new phase increment at each clock. The phase increment is allowed to diminish until it reaches the minimum phase increment value (as defined in the down chirp description). The Phase Increment Register is then reloaded with the minimum phase increment, and the up/down cycle begins again. See Figure 6 for a graphical representation of this process.

The minimum and maximum phase increments have allowable values from 0 to 2^{32}-1. This corresponds to the phase increment:

$$0 < \text{Phase Increment} < \pi(1 - 2^{-32}) \text{ radians} \quad \text{(EQ. 4)}$$

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The Delta Phase Increment parameter can take on values from 0 to 2^{24} - 1 which corresponds to the Delta Phase Increment:

$$0 < \text{Delta Phase Increment} < \pi(2^{-8} - 2^{-32}) \text{ radians} \quad \text{(EQ. 5)}$$

The output of the phase accumulator forms the input to the SIN/COS Generator which in turn produces a quadrature vector which rotates clockwise: the outputs are cos(ωn) and -sin(ωn). The outputs of the SIN/COS Generator are two's complement values which are scaled to prevent overflow in subsequent operations in the DDC under normal operation. The scale factor has a negligible effect on the end to end DDC gain.

The frequency resolution of the DDC = (frequency of CLK)/(Number of Phase Register bits). At the maximum clock rate, this results in a frequency selectivity of 75MHz/2^{33} = 0.009Hz. The 18-bit phase word yields a phase noise figure of greater than 102dB.

Mixer

The Mixer performs quadrature modulation by multiplying the output of the SIN/COS Generator by the input data. The outputs of the I and Q multipliers are symmetrically rounded to 17 bits to preserve the 102dB spurious free dynamic range (SFDR). The result of the quadrature modulation process is passed to the High Decimating Filter (HDF) Section.

High Decimation Filter

The High Decimation Filter (HDF) Section is comprised of two real HDF filters, one processing the I data branch and one processing the Q data branch. Each branch has the lowpass response shown in Figure 7. The normalized HDF frequency impulse response is given by the equation:

$$H(f) = \left[\frac{\text{Sin}(\pi F_S)}{\text{Sin}(\pi F_S/R)}\right]^5 \left[\frac{1}{R}\right]^5 \quad \text{(EQ. 6)}$$

where F_S is the input sampling rate; R is the decimation (rate change) factor.

Figure 7A shows this equation plotted from DC to the first null, while Figure 7B shows the equation plotted from DC response to f_S.

NOTE: The HDF is a true FIR filter; i.e., the phase is linear.

The data path through the HDF was designed to ensure a true 16-bit noise floor (approximately 98dB) at the output of the DDC. The structure of the HDF filter used in the DDC is a five stage decimation filter. The width of each successive stage decreases such that the LSBs are lost due to truncation [1]. As a result, the data must be processed in the MSBs of the filter so that the noise due to truncation is below the required noise floor. Thus, the input data of the HDF must be shifted so that its output data fills the HDF output word. The shift is a function of the desired HDF decimation rate R and the number of HDF filter stages (which is fixed at 5). The shift is performed by the Data Shifter, which positions the input data to the HDF for the maximum dynamic range while avoiding overflow errors. The shift factor is programmed into the Shift field of Control Word 4. The value in this field is calculated by the equation:

$$\text{Shift} = 75 - \text{Ceiling}(5 \log_2(R)) \quad \text{(EQ. 7)}$$

where R is the HDF decimation factor and Ceiling(X) denotes the ceiling function of X; i.e., the result is X if X is an integer, otherwise the result is the next higher integer.

During $\overline{\text{RESET}}$, the HDF is initialized and will not output any information until it is filled with new data.

NOTE: The output rate of the HDF is CLK divided by the HDF decimation factor (CLK/R). The HDF decimation counter preload (DCP) is programmed in Control Word 5, bits 21-35 and has the value: DCP = R -I, where R is the HDF decimation factor.

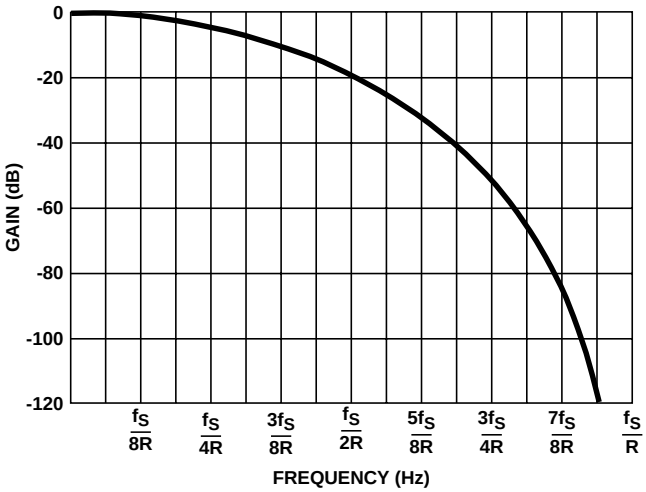


FIGURE 7A. FREQUENCY RESPONSE OF HIGH DECIMATION FILTER FROM DC TO FIRST NULL (FOR R = 16) Gain (dB) = 20log [H(f)]

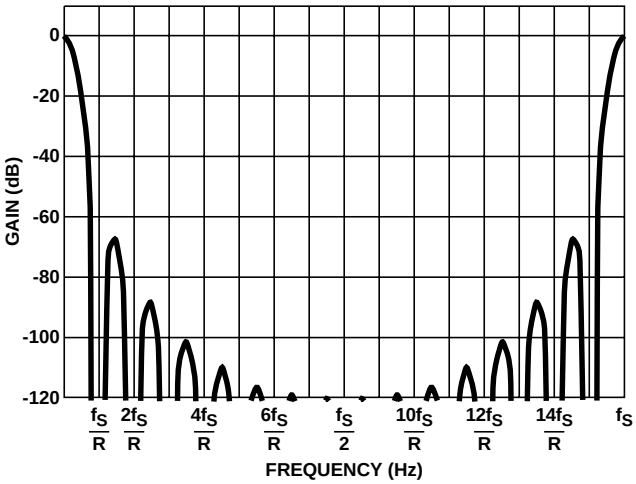


FIGURE 7B. DDC HC FREQUENCY RESPONSE (FOR R = 16) Gain (dB) = 20log[H(f)]

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Scaling Multipliers

The output of each HDF is passed to a Scaling Multiplier. The Scaling Multipliers are used to compensate for the HDF gain, which is between 1 (inclusive) and 0.5 (non-inclusive), or (0.5, 1.0). The gain through the HDF is dependent on the decimation factor: when the decimation is an even power of two, the HDF gain is equal to 1; otherwise, the gain must be compensated for in the Scaling Multiplier. The HDF gain is given by the equation:

$$\text{HDF Gain} = R^5/2^{\text{CEILING}(5\log_2(R))} \quad \text{(EQ. 8)}$$

where R is the HDF decimation factor. The compensating Scale Factor, which is input to both Scaling Multipliers, is given by the equation:

$$\text{Scale Factor} = 2^{\text{CEILING}(5\log_2(R))}/R^5 \quad \text{(EQ. 9)}$$

where R is the HDF decimation factor.

NOTE: The Scale Factor falls in the interval [1, 2). The output of the scaling multiplier is symmetrically rounded to 17 bits.

The binary formats of the inputs and outputs of the scaling multiplier are as follows:

Input from HDF:	$a_0(-2^0).\ a_1(2^{-1})\ a_2(2^{-2})\ldots\ a_{17}(2^{-17})$
Scale factor:	$a_0(2^0).\ a_1(2^{-1})\ a_2(2^{-2})\ldots\ a_{15}(2^{-15})$
Output:	$a_0(-2^0).\ a_1(2^{-1})\ a_2(2^{-2})\ldots\ a_{16}(2^{-16})$

FIR Filter

The Scaling Multiplier output is passed to the FIR Filter, which performs aliasing attenuation, passband roll off compensation and transition band shaping. The FIR Filter Section is functionally two identical 121 tap lowpass FIR filters, one each for the I and Q channel. The two filters are each implemented as sum of products, each with a single multiplier, with the coefficients stored in ROM. The filters' passbands are precompensated to be the inverse of the response of the HDF. The frequency responses of the HDF, FIR, and Composite HDF/FIR filters are shown in Figure 8. The composite passband of the HDF and FIR filter frequency response is shown in Figure 9. The FIR coefficients are scaled so that the maximum gain of the composite filter is less than or equal to 0dB. The composite passband ripple is less than 0.04dB.

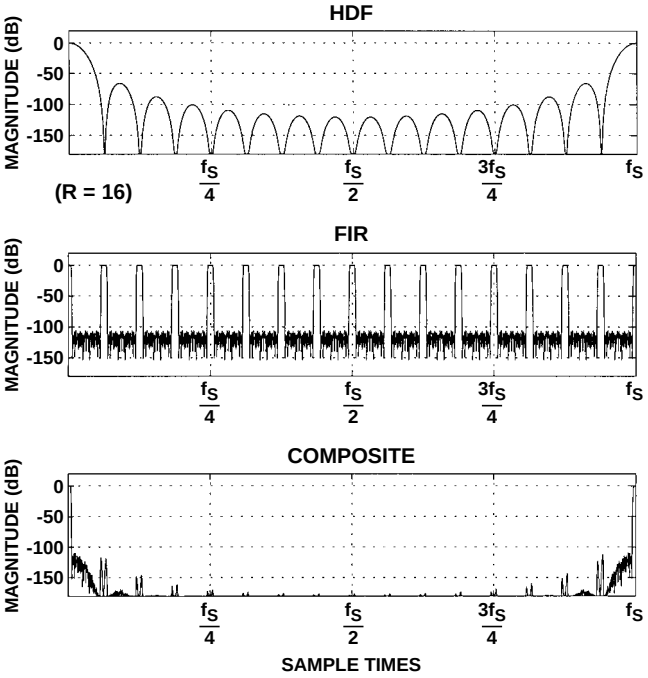


FIGURE 8A. DDC HDF, FIR, AND COMPOSITE FILTER RESPONSE (FOR R = 16)

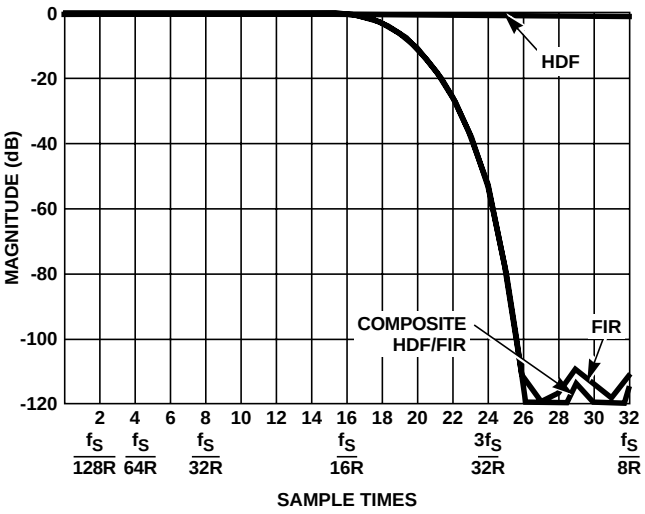


FIGURE 8B. DDC FILTER RESPONSES (FOR R = 16)

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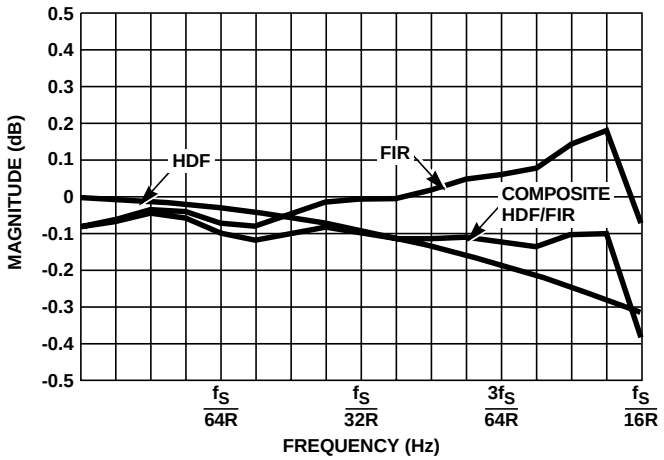


FIGURE 9. FIR COMPENSATION FOR HDF ROLL OFF (FOR R = 16)

The coefficients of the filter are quantized to 22 bits to preserve greater than 106dB of stopband attenuation. The sum of products of each filter output calculation is a 38-bit number with 37 fractional bits.

When a quadrature output is selected, the outputs of the FIR filters are decimated by a factor of four. When real output is selected, only the I output is active. The output is decimated by two in this case. When Filter Only Mode is selected, only the I filter path is active and its output is decimated by four.

The composite filter bandwidths are a function of the HDF decimation rate and the FIR Filter shape. The double sided bandwidths are specified by Equations 10 and 11.

$$-3dB\ BW_{DS} = 0.1375F_S/R \quad 16 < R < 16384 \qquad \text{(EQ. 10)}$$

$$-102dB\ BW_{DS} = 0.2002F_S/R \quad 16 < R < 16384 \qquad \text{(EQ. 11)}$$

where F_S = CLK; R = HDF Decimation Factor.

The single sided bandwidths are specified in Equations 12 and 13.

$$-3dB\ BW_{SS} = 0.06875F_S/R \qquad \text{(EQ. 12)}$$

$$-102dB\ BW_{SS} = 0.100097F_S/R \qquad \text{(EQ. 13)}$$

where F_S = CLK; R = HDF Decimation Factor.

NOTE: The output data rate of the FIR is the HDF output rate divided by either 2 or 4, depending on mode. Recall the HDF output rate is CLK/R. (See Table 1.)

TABLE 1. FIR OUTPUT RATE AND DECIMATION

OUTPUT MODE	FIR OUTPUT RATE	FIR DECIMATION
Real	CLK/2R	2
Complex	CLK/4R	4
Filter Only	CLK/4R	4

R - HDF Decimation Factor

Output Formatter

The circuit has two serial data outputs, I and Q. The timing of the output bits is referenced to IQCLK and IQSTB. There are several modes of operation for the data and control line interface, all of which were designed to be compatible with common microprocessors. These interface modes are selected by loading the appropriate control words (see Tables 3 through 10, with Table 9 containing most interface parameters).

Quadrature data output can occur in one of two ways: simultaneously or sequentially. The simultaneous method clocks out the I and Q data on their respective serial output pins. The I followed by Q method clocks I and Q out sequentially on the I output pin: the entire I word is serially clocked out first, then the entire Q word. In real data Output Mode, the Formatter converts the quadrature data to real and clocks it out serially on the I output pin. In all modes, the I and Q outputs return to the zero state after the last bit is transmitted.

When the “I followed by Q” signal (CW6, bit 35) is low, I data will appear on the I output and Q data will appear on the Q output.

When the “I followed by Q” signal (CW6, bit 35) is asserted, the Q output is inactive and I data, followed by Q data appear on the I output. When in this state, and both the “Test Enable” signal (CW1, Bit 3), and “Q Strobe on Rollover” signal (CW7, Bit 10) signal are asserted, the Phase

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Generator Carry Out will appear on the output. Control Word 5 contains fields to set the number of output bits transmitted to the arithmetic representation and interface control of the serial output data. Control Word 4, Bits 31-32, allow selection of baseband centered quadrature on baseband offset quadrature complex outputs. Control Word 4, Bit 0, allows selection of spectral inversion. In addition, the output drivers for I, Q, IQCLK and IQSTB can be individually enabled or placed in a high impedance state using Control Word 6, Bits 20-28. These options are explained below.

When the “Output Spectrum” signal (CW4, bits 31-32) is set to “01”, then the real output data appears on the I output and the Q output in the I/Q separate mode. When in I Mode followed by Q Mode, the Q slot is also real data since the real mode outputs at twice the rate of the complex mode (CW4, bits 31-32 = 00).

When set for fixed point output, the output data can be in two's complement, offset binary or signed magnitude form. Data is converted to offset binary by complementing the most significant bit of a two's complement number. The length of the output data word can be 16, 24, 32 or 38-bits. The first three options are symmetrically rounded to the LSB of the output data; the fourth option represents the full 38-bit width of the accumulator and so represents exact arithmetic.

The output has a saturation option to prevent possible overflow due to a step input at power up. When Overflow Protection is enabled, the output is forced to be either the most positive or most negative number. Saturation is available in all four fixed point output options, and is set via Control Word 7, Bit 0.

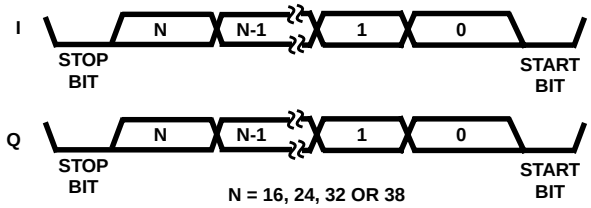
Data can also be output in single precision floating point format (see Table 2). For all output data formats, the internal calculations are performed in exact two’s complement integer arithmetic and the resulting data is converted in the Output Formatter.

TABLE 2. FLOATING POINT FORMAT

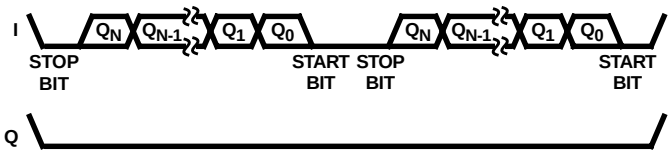
SIGN	EXPONENT	MANTISSA	
-2^0	2^7 to 2^0	Implied 1	0.2^{-1} to 2^{-23}

The I and Q pins can be programmed for either simultaneous or I followed by Q output. In simultaneous mode, the I and Q data appear on the I and Q pins, respectively. Each data sample is preceded by a leading zero bit, followed by the output data, followed by a trailing zero bit. In I followed by Q Mode, the output data appears on the I pin, and consists of a leading zero bit, then the I data, a trailing zero, a leading zero, the Q data, and finally a trailing zero bit. In Figures 10 through 12, the leading and trailing zero bits occur before bit 0 and after bit N, respectively.

$$\text{IQCLK Rate} = \frac{\text{CLK}}{\text{IQCLK Frequency}} - 1 \qquad \text{(EQ. 14)}$$



A. SIMULTANEOUS OUTPUT MODE



B. I FOLLOWED BY Q OUTPUT MODE

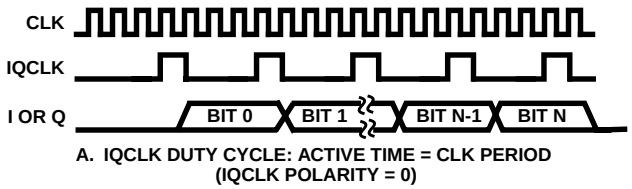
FIGURE 10. DATA OUTPUT MODES

IQCLK is used to delineate the bit or word timing of the I and Q outputs. There are several options on the configuration of IQCLK, which are controlled with Control Word 6 (see Table 8). The frequency of IQCLK is programmed to be a fraction of the CLK frequency, from (CLK rate)/2 to (CLK rate)/8192 (see Equation 14). If IQCLK Rate = 0, then IQCLK remains in its inactive state and the output bits change on the rising edges of CLK.

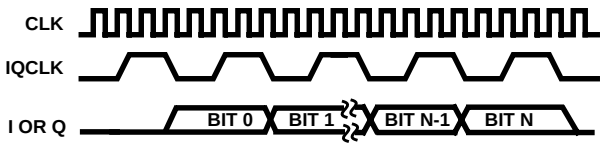
IQCLK can be programmed to be active continuously, or only during I or Q data output via the IQCLK duration bit. Using the IQCLK Duty Cycle bit, IQCLK is selectable as either 50% duty cycle or to be high for one period of CLK. In addition, the Formatter can be set so that the data bits are clocked on either the positive or negative edges of IQCLK with the IQCLK Polarity bit. Figure 11 shows the various modes of operation with IQCLK Polarity programmed for active high operation.

Control Word 6 also configures IQSTB, as shown in Figure 12. When programmed for Active Prior to Data Word, IQSTB is high for one period of IQCLK and terminates simultaneously with the beginning of the first data bit; otherwise it goes active with the beginning of the first bit and inactive with the end of the last bit. IQSTB can be programmed to be either active high or low.

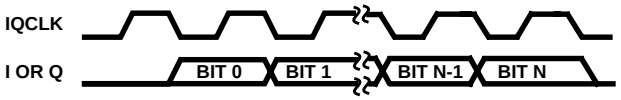
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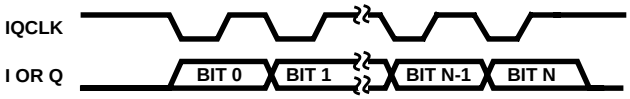
A. IQCLK DUTY CYCLE: ACTIVE TIME = CLK PERIOD (IQCLK POLARITY = 0)



B. IQCLK DUTY CYCLE: 50%

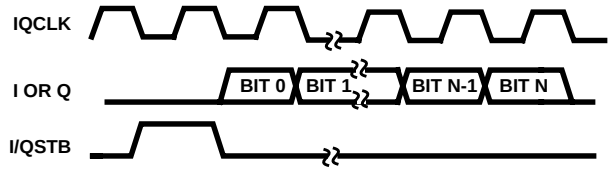


C. IQCLK DURATION: CONTINUOUS

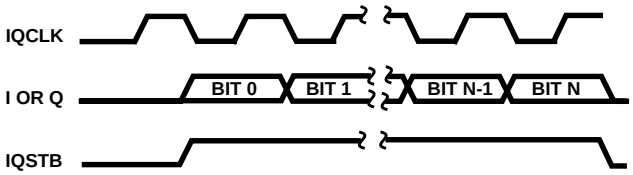


D. IQCLK DURATION: ACTIVE DURING I OR Q ONLY

FIGURE 11. TIMING FOR CLK, IQCLK, IQSTB, I AND Q



A. IQSTB ACTIVE PRIOR TO DATA WORD



B. IQSTB ACTIVE DURING DATA WORD

FIGURE 12. IQSTB TIMING

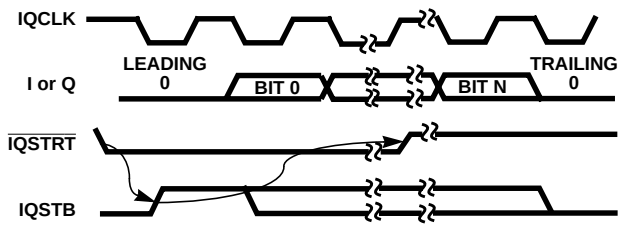


FIGURE 13. REQUESTED DATA OUTPUT TIMING

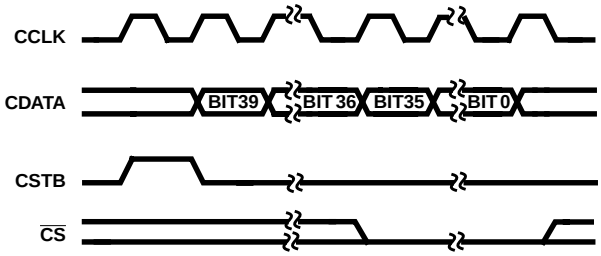


FIGURE 14. CONTROL WORD TIMING DIAGRAM

Data can be read out of the DDC on request through the use of the $\overline{\text{IQSTRT}}$ pin. After passing through the Output Formatter, the I and Q data are stored in output buffers, which are updated at the end of the FIR Filter processing cycle. The $\overline{\text{IQSTRT}}$ and IQSTB lines form a two line handshake as shown in Figure 13. $\overline{\text{IQSTRT}}$ initiates the request. If the buffer has data in it, the DDC will begin an output data sequence on the next edge of IQCLK. The DDC will then put out one bit per IQCLK until the output cycle is complete. In I followed by Q Mode, one $\overline{\text{IQSTRT}}$ will initiate an I output word followed by a Q output word. In real data Output Mode, one IQSTRT will initiate two samples of real data on the I pin.

To avoid the generation of multiple read cycles, IQSTRT must go inactive within 10 cycles of IQCLK after the initiation of IQSTB. The DDC will not update the output buffer again until the current output cycle has completed. When IQSTRT is used in this handshake mode, it must consist of pulses that satisfy the set up and hold requirements listed in the AC Timing Specifications and the pulses must occur at a rate of at least CLK/(HDF Decimation Factor x 4 -1). This mode of operation requires the Time Slot Number in Control Word 6 to be 0.

NOTE: When handshake mode is not used, $\overline{\text{IQSTRT}}$ should be at a logic low.

Auto Three-State Mode for IQCLK, IQSTB, I and Q allows multiple chips to operate using common data and output control lines. Each chip is assigned a Time Slot Number on the bus to use for outputting its data. All outputs programmed for Auto Three-State Mode are active during their time slot and are in a high impedance state at all other times. A time slot starts one CLK period prior to the beginning of the first bit of I or Q and ends (Time Slot Length) CLK periods afterwards. Assignment of a time slot is with reference to the deassertion of $\overline{\text{RESET}}$. The minimum possible Time Slot Length for a given application is:

$$\text{Length}_{MIN} = [(\text{Number of Output Bits} + 2) \times \text{Mode}] + 1; \text{ or} \quad \text{(EQ. 15)}$$

where Mode = 2 if the DDC is in either Real Output or I followed By Q Mode; else Mode = 1.

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Note that Equation 15 is useful in all modes for calculating the number of IQCLKs necessary to complete one output data cycle. For a given decimation rate and output word length, the maximum value in the IQCLK Rate field is:

$$IQCLKRate_{MAX} = Floor\left[\frac{(R)\times 4}{Length_{MIN}}\right] - 1; \quad \text{(EQ. 16)}$$

where Floor(X) represents the integer part of X, R is the HDF decimation factor, 4 is the FIR decimation factor.

Example Clock Calculations

Clarification of the use of Equations 14-16, the calculation of the HDF and FIR clocks and the calculation of the IQCLK is best done by example:

The sample clock, CLK, is 10MHz . . . . . CLK = 10MHz
The HDF Decimation Factor, R, is 100 (which makes the decimation counter preload = 99). . . . . R = 100
The Output Mode is I followed by Q . . . . . Mode = 2
Complex output . . . . . FIR Decimation = 4
The desired number of output bits is 32.

1. We begin by identifying the HDF Input Rate:
   HDF Input Rate = CLK = 10MHz . . . . . CLK = 10MHz
2. Next we calculate the HDF Output Rate:
   HDF Output Rate = CLK/R = 10MHz/(100) = 100kHz
   . . . . . .HDF Output Rate = 100kHz
3. Next we calculate the FIR output Rate:
   FIR Output Rate = CLK/4R = 25kHz.
   . . . . . FIR Output Rate = 25kHz
4. Next we calculate the minimum time slot length:
   Equation 15:
   $Length_{MIN}$ = [(Number of Output Bits + 2) x Mode] +1
   where the number of output bits = 32 and the Mode is 2 because of the I followed by Q output selection.
   $Length_{MIN}$ = [(32 + 2) x 2] +1 = 69 IQCLKs
   . . . . . $Length_{MIN}$ = 69 IQCLKs
5. Next we calculate the IQCLK frequency:
   IQCLK frequency = [(F_S)($Length_{MIN}$)/(R)(4)] - 1
   IQCLK frequency = [(10MHz)(69)/(100)(4)] - 1 = 1.725MHz
   The IQCLK frequency can be no slower than 1.725MHz if all of the bits are to be output of the DDC in a time slot.
   . . . . . .Slowest Serial Output Rate = 1.725MHz
6. The Programmed value for the maximum IQCLK Rate, from Equation 16, is:
   $IQCLKRATE_{MAX}$ = Floor[(R) x 4/ $Length_{MIN}$] -1
   $IQCLKRATE_{MAX}$ = Floor[(100 x 4)/69] - 1 = 4
   The IQCLKRATE can be not greater than 4 if all of the bits are to be output of the DDC in a time slot.
   . . . . . Control Word Value for IQCLK Ratemax =
   [00004]H; 0 0000 0000 0100_{LSB}
7. Let's sanity check with Equation 14.
   IQCLK Rate = [(CLK/IQCLKfreq)-1] = [10E6/1.725E6] -1 = 4.
   This checks!

Control Word Input

The DDC has eight 40-bit control words which are loaded through the four pin control interface. The format and timing of this interface is compatible with the serial interface timing of most common DSP microprocessors (see Figure 14). The words are shifted MSB first, where bit 39 of the control word is the MSB. Bits 39 through 37 are the control word address, i.e., the target control buffer. $\overline{CS}$ must go low before bit 35 is clocked in. All 40 bits of the control word must be loaded. The formats of the control words are shown in Tables 3 through 10.

The control words are double buffered: each control word is initially loaded into one of eight control buffers for subsequent down loading into the corresponding Control Register. The internal circuitry of the DDC uses the Control Registers to regulate its operation. Control buffers can be downloaded in one of two ways. Loading a Buffer Register with bit 36 = 1 causes all Control Registers to be updated from their respective control buffers when the current word is finished loading. If bit 36 = 0, then only that control buffer is updated and the operation of the DDC is not affected. All Control Registers are updated from their respective buffers on the third rising edge of CLK following the deassertion of RESET. ***NOTE: Control Word 0 is unique in that it is only used to update the seven Control Registers, and it is recognized by the DDC regardless of the state of CS.*** In systems with multiple DDCs, this allows the user to update the configuration of all chips simultaneously without using RESET.

To ensure that the control information is properly loaded, the frequency of CLK must be greater than the frequency of CCLK. In addition, $\overline{RESET}$ must remain inactive during the loading of a control word.

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TABLE 3. DESTINATION ADDRESS = 0

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	000 = Control Word 0
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-32	Reserved	All Zeroes

TABLE 4. PHASE GENERATOR/TEST ENABLE/OUTPUT REGISTER

DESTINATION ADDRESS = 1		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	001 = Control Word 1
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-4	Minimum Phase Increment	Bits 35-4 = $2^{31}...2^{0}$. Range: 0 < Minimum Phase Increment < π $(1-2^{-32})$ radians. In the CW mode this is the phase increment of the NCO which is added to the NCO intitial phase offset state. The desired Sin/Cos generator (local oscillator) frequency is set by the equation: **f_C = (phase increment)$f_S 2^{-33}$**; where f_C is the desired local oscillator frequency, f_S is the input sampling frequency, and phase increment is the control word value in hexidecimal. To calculate the value to be programmed into this field, use this equation: **phase increment = INT[f_C / f_S)2^{33}]hex** Some examples of phase increments and local oscillator frequencies: 00000000h: f_C = zero frequency 00000001h: $f_C = f_S / 2^{33}$ - lowest frequency (75MHz x 2^{-33} = 8.73mHz) 10000000h: $f_C = f_S /32$ 20000000h: $f_C = f_S /16$ 40000000h: $f_C = f_S /8$ 80000000h: $f_C = f_S /4$ ffffffffh: $f_C = (0.49999) f_S$ - highest frequency (75MHz x 2^{-33} = 37.49MHz) In the CHIRP modes, this is the smallest allowable phase increment. In the Filter Only mode, this parameter should be set to 0.
3	Test Enable	0 = Test Features Disabled 1 = Test Features Enabled
2-0	Phase Generator Mode	000 = Filter Only 001 = Normal Mode (CW) 010 = Reserved 011 = Up Chirp 100 = Reserved 101 = Down Chirp 110 = Reserved 111 = Up/Down Chirp ***Note that the lsb sets the gain through the DDC as follows:*** ***0 = Gain is1*** ***1 = Gain is 2***

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TABLE 5. PHASE GENERATOR REGISTER

DESTINATION ADDRESS = 2		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	010 = Control Word 2
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-32	Reserved	All Zeroes
31-0	Maximum Phase Increment	Bits 31-0 = 2^{31}... 2^{0}. Range: is 0 < Maximum Phase Increment < $\pi(1-2^{-32})$ radians. This parameter is only used in the CHIRP modes, and this is the largest allowable phase increment. Set to 0 in the Filter Only and CW modes.

TABLE 6. PHASE GENERATOR/OUTPUT TIME SLOT REGISTER

DESTINATION ADDRESS = 3		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	011 = Control Word 3
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-32	Reserved	All Zeroes
31-18	Time Slot Length	Time Slot Length in IQCLK Periods; Bits 31-18 = 2^{13}... 2^{0}. Range is (19,25, 33, 37, 39, 49, 65 and 77) The equation for calculating the value for this field is: **TSL = [[(Number of Output Bits + 2)Mode] + 1]Hex**; where mode is 2 if the DDC is in either the real or I followed by Q mode. Mode is 1 for all other DDC operational modes. Allowable Minimum Time Slot Lengths: (18)1 + 1 = 19 (13 hexidecimal) (18)2 + 1 = 37 (25 hexidecimal); Real Output or I followed by Q (24)1 + 1 = 25 (19 hexidecimal) (24)2 + 1 = 49 (31 hexidecimal); Real Output or I followed by Q (32)1 + 1 = 33 (21 hexidecimal) (32)2 + 1 = 65 (41 hexidecimal); Real Output or I followed by Q (38)1 + 1 = 39 (27 hexidecimal) (38)2 + 1 = 77 (4d hexidecimal); Real Output or I followed by Q
17-0	Phase Offset	Starting Phase Angle of Phase Accumulator; Range = 0 to 2π. Bits 17-0 = 2^{32}... 2^{15}. Some example phase offset hexidecimal values : `0000` - 0 `1000` - π/2 `2000` - π `3000` - 3π/2 `3fff` - 2π

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TABLE 7. PHASE GENERATION/HDF.OUTPUT REGISTER

DESTINATION ADDRESS = 4		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	100 = Control Word 4
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-33	Reserved	All Zeroes
32-31	Output Spectrum	00 = No Up Conversion,Complex Output 01 = Up Convert by f”/4, Real Output 10 = Up Convert by f”/2,Complex Output 11 = Reserved Mode
30-7	Delta Phase Increment	24-Bit Delta Phase Increment. Bits 30-7 = 2^{23}... 2^{0}. Range: 0 < Delta Phase Increment < π (2^{-8}-2^{-32})
6-1	HDF Data Shift (Shift Factor)	16-Bit HDF Gain Compensation Number - the shift portion. HDF Input Data Shift (Towards LSB). Bits 6-1 = 2^{5}...2^{0}. Range: 0 ≤ Shift Factor ≤ 55 decimal; Range: [0 ≤ Shift Factor ≤ 37]hex Calculate the value for this field using this equation: **HDF Data Shift = [75 - Ceiing(5 $\log_2$(R))]hex** Note: $\log_2(x) = (3.32)\log(x)$
0	Spectral Reverse	0 = Normal Output 1 = Spectrally Reversed Output

TABLE 8. HDF/OUTPUT REGISTER

DESTINATION ADDRESS = 5		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	101 = Control Word 5
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-21	HDF Decimation Counter Preload (HDF DCP)	HDF Decimation Counter Preload. Range: 15 < HDF Decimation Counter Preload < 32,767 Calculate the value for this feild using this equation: **HDF DCP = R - 1;** where R is the HDF decimation (rate change) factor. Common HDF decimation (rate change) factors and associated hexidecimal HDF DCP values: `000f`: R = 16 `00ff`: R = 128 `01ff`: R = 512 `03ff`: R = 1,024 `07ff`: R = 2,048 `0fff`: R = 4,096 `1fff`: R = 8,192 `3fff`: R = 16,384 `7fff`: R = 32,768

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TABLE 8. HDF/OUTPUT REGISTER (Continued)

DESTINATION ADDRESS = 5		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
20-5	Scaling Multiplier Gain (Scale Factor)	16-Bit HDF Gain Compensation Number - the multiplier portion. Range: $1 \leq$ Scale Factor < 2, Field Format = $2^0.2^{-1}...2^{-15}$. Calculate the value for this field using this equation: **Scale Factor = $2^{CEILING(5log_2(R))}/(R)^5$**; where R is the HDF decimation (rate change) factor and CEILING(x) is equal to x for integer values, otherwise is equal to the next higher integer. Common HDF decimation factors (R), decimation counter preload (DCP) and Scale Factors (SF) values:

R	DCP(dec)	DCP(hex)	SF(dec)	SF(hex)
16	15	000f	1.000	8000
128	127	007f	1.000	8000
512	511	01ff	1.00	8000
1,024	1,023	03ff	1.000	8000
2,048	2,047	07ff	1.000	8000
4,096	4,095	0fff	1.000	8000
8,192	8,191	1fff	1.00	8000
16,384	16,382	3fff	1.00	8000
32,768	32,768	7fff	1.000	8000

Note that the Scale Factor is 1 (8000hex) for power of 2 decimation factors.
The compensation for the HDF gain is performed with a shifter and a multiplier. Thus to program the HDF Gain compensation, there is an associated Shift Factor and the Scale Factor. As the Decimation Factor increases, the multiplier moves away from the value 1 and approaches the value 2. When the calculated value for the multiplier equals or exceeds 2, the shifter is incremented and the multiplier returns to 1 and increases towards 2 again as the Decimation Factor increases.

As an example, the table below details the values of Scale Factor for values of R from 16 to 32:

R	DCP(dec)	DCP(hex)	SF(dec)	SF(hex)
16	15	000f	1.000000000	8000
17	16	0010	1.477013647	BD0E
18	17	0011	1.109857915	8E0F
19	18	0012	1.693916116	D8D2
20	19	0013	1.310720000	A7C5
21	20	0014	1.026983417	8374
22	21	0015	1.627707993	D058
23	22	0016	1.303318981	A6D3
24	23	0017	1.053497942	86D9
25	24	0018	1.717986918	DBE6
26	25	0019	1.412060017	B4BE
27	26	001a	1.169233029	95A9
28	27	001b	1.949663831	F98E
29	28	001c	1.635911864	D165
30	29	001d	1.380840823	B0BF
31	30	001e	1.172037271	9605
32	31	001f	1.000000000	8000

4-3	Output Format	00 = Two's Complement 01 = Offset Binary 10 = Sign Magnitude 11 = Single Precision Floating Point Format

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TABLE 8. HDF/OUTPUT REGISTER (Continued)

DESTINATION ADDRESS = 5		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
2-1	Number Of Output Bits	00 = 16 Bits 01 = 24 Bits 10 = 32 Bits 11 = 38 Bits
0	Output Sense	0 = LSB First 1 = MSB First

TABLE 9. INPUT AND OUTPUT FORMAT REGISTER

DESTINATION ADDRESS = 6		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	110 = Control Word 6
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35	I followed by Q	0 = I and Q Output Separately 1 = I and Q Data Output on I Pin
34-29	Time Slot Number	Bits 34-29 = $2^5...2^0$. Range: 0 < Time Slot Number < 63. This implies that 64 different channels may be mutliplexed, assigning one time slot per channel.
28	IQCLK Polarity	0 = Output Data Stable On Rising Edge Of IQCLK; IQCLK High between I or Q Bit Periods when IQCLK Duration = 0. 1 = Output Data Stable on Falling Edge of IQCLK; IQCLK Low between I or Q Bit Periods when IQCLK Duration = 0.
27	IQCLK Duty Cycle	0 = IQCLK Active Time = CLK Period. 1 = 50% Duty Cycle
26	IQCLK Duration	0 = Active During I or Q Output Periods Only 1 = Active Continuously
25-24	IQCLK Three-State Control	00 = Three-State IQCLK 01 = Enable IQCLK 1x = Auto-Three-State Enable IQCLK (during time slot)
23	IQSTB Polarity	0 = Active High 1 = Active Low
22	IQSTB Location	0 = IQSTB Prior to the Beginning of the Data Word. 1 = IQSTB During the Data Word.
21-20	IQSTB Three-State Control	00 = Three-State IQSTB 01 = Enable IQSTB 1x = Auto Three-State Enable IQSTB (during time slot)
19	I Polarity	0 = True Data 1 = Inverted Data
18-17	I Three-State Control	00 = Three-State I 01 = Enable I 1x = Auto Three-State Enable I (during time slot)
16	Q Polarity	0 = True Data 1 = Inverted Data

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TABLE 9. INPUT AND OUTPUT FORMAT REGISTER (Continued)

DESTINATION ADDRESS = 6		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
15-14	Q Three-State Control	00 = Three-State Q 01 = Enable Q 1x = Auto Three-State Enable Q (during time slot)
13	Input Format	0 = Offset Binary 1 = Two's Complement
12-0	IQCLK Rate Counter Preload	I/QCLK Rate Counter Preload, Bits 12-0 = $2^{12} \cdots 2^{0}$. Range: 2 ≤ IQCLK Rate Counter Preload ≤ 1701. To calculate the value in this field use this equation: **IQCLK Rate Counter Preload = [FLOOR[(HDF Decimation Factor x 4)/TSL] - 1]hex**; where FLOOR(x) represents the integer part of x, and TSL is the decimal value of Control Word 3, bit 31-18.

TABLE 10. PHASE OFFSET REGISTER

DESTINATION ADDRESS = 7		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	111 = Control Word 7
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-14	Reserved	All Zeroes
13	Data	0 = Normal Data Input 1 = Force Input Data to 8000 Hex.
12-11	FIR Accumulator Control	00 = Normal Accumulation - The accumulator is reset on every FIR cycle. 01 = No Accumulation -The accumulator is disabled. 10 = Continuous Accumulation -The accumulator is not reset on every FIR cycle. This test mode was created to allow the user to perform the equivilent of a check sum test. A very long term test could be run and an accumulated output would yeild a specific numeric value. If the answer differed, the part is not functioning properly. 11 = Reserved
10	Q Strobe on Roll Over	0 = Q carries Normal Data 1 = Q Strobes When Phase Generator Rolls Over
9	Force Outputs	0 = Normal Output Response 1 = Force Outputs
8	IQCLK Forced Data	If Bit 9 = 1, Force IQCLK = Bit 8; Else Normal
7	IQSTB Forced Data	If Bit 9 = 1, Force IQSTB = Bit 7; Else Normal.
6	I Forced Data	If Bit 9 = 1, Force I = Bit 6; Else Normal.
5	Q Forced Data	If Bit 9 = 1, Force Q = Bit 5; Else Normal.
4	Sin/Cos Generator Bypass	0 = Sin Cos Generator Normal, 1 = Bypass Sin Cos Generator; Sin = Cos = 0.fffff (approximately 1)
3	Scaling Multiplier Bypass	0 = Scaling Multiplier Normal, 1 = Scale Factor = 1.
2	Reserved	Must be Zero for Proper Operation while Test Features are Enabled.
1	Wait For RAM Full	If Bit = 0, DDC will Output Data Normally after a Reset, which will Include Unpredictable Data in Data RAMs. If Bit = 1, No Chip Output will Occur until Sufficient Data RAM Locations are Written.
0	Disable Overflow Protection	0 = Normal Operation 1 = Disable Overflow Protection

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HSP50016 supports two types of testing. Control Word 7 can be used to verify the operation of the circuit through the divide and conquer method. Setting the Enable Test Bit (Control Word 1, Bit 3) equal to a 1 enables the test features controlled by Control Word 7. (This bit is in Control Word 1 so that Word 7 does not have to be loaded if the test features are not being used.) The functions allowed by Control Word 7 are shown in Table 10.

NOTE: Asserting bits 9 and 13 of Control Word 7 will put all outputs to a static mode. This may remove strobe enables or clocks used to read the data signals. This Test Mode was intended for interface evaluation at the board level.

The DDC also has a Test Access Port (TAP). This port is fully conformant to IEEE Std. 1149.1 - 1990 - IEEE Standard Test Access Port and Boundary-Scan [2]. The TAP supports the following instructions: BYPASS, SAMPLE/PRELOAD, INTEST, EXTEST, RUNBIST and IDCODE. In addition, there are seven instructions called RDCNTLWD1-7, which read the contents of the control words over the TAP. The address bits and bit 36 are only used to determine the destination of data during loading; they are not stored, so they are not read out with the RDCNTLWD1-7 instruction.

Summary

To use the DDC in a down conversion application three items must be considered and designed to compliance. Solutions must satisfy all three items.

1. The Nyquist Sampling Rate for the bandwidth of interest $F_S \geq 2BW$, where BW is the bandwidth of interest.
2. The composite FIR/HDF double sided bandwidth, $BW_{-3dB} = 0.1375F_S/R$.
3. The desired serial output clock rate (total decimation, plus parallel to serial conversion rate increase).

$$\text{IQCLK Frequency} = \left\lceil \frac{f_S \ \text{Length}_{MIN}}{(R_{FIR})\ (R)} \right\rceil - 1$$

NOTE: R_{FIR} = 2 for real mode, 4 for all other modes.

Applications

Down Conversion

The primary spectral operation in the DDC is down conversion of an input signal to base band, see Figure 15. This process is done in two steps: multiplication of the input waveform by an internally generated quadrature sinusoid, i.e., modulation and lowpass filtering to attenuate the unwanted spectral components. The unwanted spectral components have two sources, the input signal and an artifact of the modulation process.

The modulation process can be written as:

$$u(n) = x(n)e^{-j\omega c} = x(n)[\cos(\omega_C) - j\sin(\omega_C)] \quad \text{(EQ. 17)}$$

Where x(n) is the real input data sequence, $\omega = 2\pi f$, and ω_C is the frequency of the signal generated by the SIN/COS Generator.

For demonstration purposes let $x(n) = \cos(\omega_k n)$. The multiplication then becomes:

$$\begin{aligned} u(n) &= \cos(\omega_k n)[\cos(\omega_C n) - j\sin(\omega_C n)] \\ &= 1/2[\cos((\omega_k - \omega_C)n) + \cos((\omega_k + \omega_C)n) \\ &\quad - j(\sin((\omega_k + \omega_C)n) - \sin((\omega_k - \omega_C)n))] \end{aligned} \quad \text{(EQ. 18)}$$

The signal u(n) is passed through a low pass filter; assuming that the filter passes the low frequency terms with no degradation and attenuates the high frequency terms completely, the filtering operation produces the output:

$$\begin{aligned} v(n) &= 1/2(\cos((\omega_k - \omega_C)n) + j\sin((\omega_k - \omega_C)n)) \\ &= 1/2e^{j(\omega_k - \omega_C)n} \end{aligned} \quad \text{(EQ. 19)}$$

When the magnitude of the input signal x(n) is one, the magnitude of v(n) is 1/2. Both the I and Q channels are multiplied by a factor of two to yield:

$$\begin{aligned} w(n) &= \cos((\omega_k - \omega_C)n) + j\sin((\omega_k - \omega_C)n) \\ &= e^{j(\omega_k - \omega_C)n}. \end{aligned} \quad \text{(EQ. 20)}$$

Figure 16 shows an HSP50016 in a single channel down conversion circuit. Notice that the input data is only 12 bits, so it is justified to the MSB of the DDC's input data. If a smaller sample width is used, it is recommended that the MSB of the data is input into DATA15. The unused bits are connected to ground. This alignment makes it easier to locate the position of the MSB in the output data. Note that the input is configured for offset binary arithmetic and the output is set up for I followed by Q, which enables the use of only one serial connection to the output processor. The serial data clock of the processor and the Control Clock of the DDC are driven by a TTL compatible oscillator. (IQCLK cannot be used for this purpose since its frequency is indeterminate until the DDC has been configured). Note that many processors provide a bit clock which eliminates the need for the external oscillator.

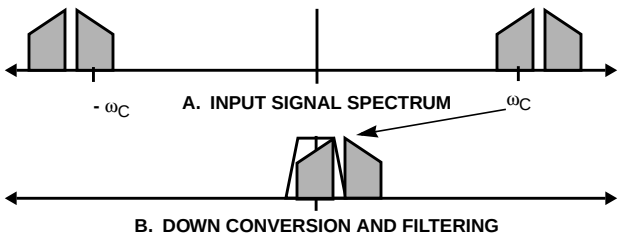


FIGURE 15. DOWN CONVERSION

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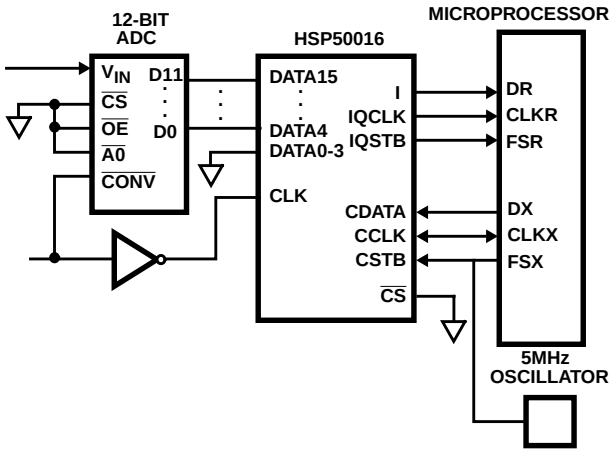


FIGURE 16. CIRCUIT FOR SINGLE CHANNEL OPERATION

An example of the control word contents for this mode of operation is given in Tables 11 through 17. In this setup, the DDC has been configured for a constant down conversion frequency, decimation by 64 and Test Features disabled. Bit fields of three bits or less are in binary notation; longer fields are in hexadecimal. Control Words Zero and Seven are not used.

TABLE 11. SAMPLE FORMAT FOR CONTROL WORD 1 - PHASE GENERATOR/TEST ENABLE

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	001 = Control Word 1.
36	Update	1 = Control Register Update.
35-4	Minimum Phase Increment	Minimum Phase Increment Computed according to $[f_C/f_S]\ 2^{33}$.
3	Test Enable	0 = Test Features Disabled.
2-0	Phase Generator Mode	001 = Normal Mode.

0011 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX 0001

TABLE 12. SAMPLE FORMAT FOR CONTROL WORD 2 - PHASE GENERATOR

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	010 = Control Word 2.
36	Update	1 = Control Register Update.
35-32	Reserved	All Zeroes.
31-0	Maximum Phase Increment	All Zeroes.

0101 0000 0000 0000 0000 0000 0000 0000 0000 0000

TABLE 13. SAMPLE FORMAT FOR CONTROL WORD 3 - PHASE GENERATOR/OUTPUT TIME SLOT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	011 = Control Word 3.
36	Update	1 = Control Register Update.
35-32	Reserved	All Zeroes.
31-18	Time Slot Length	All Zeroes.
17-0	Phase Offset	All Zeroes.

0111 0000 0000 0000 0000 0000 0000 0000 0000 0000

TABLE 14. SAMPLE FORMAT FOR CONTROL WORD 4 - PHASE GENERATOR/HDF/OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	100 = Control Word 4.
36	Update	1 = Control Register Update.
35-33	Reserved	All Zeroes.
32	Up Convert	0 = Do Not Up convert.
31	Real Mode	0 = Complex Mode.
30-7	Delta Phase Increment	All Zeroes.
6-1	Shift	37 = Decimal 55, the Shift Corresponding to HDF Decimation by 16.
0	Spectral Reverse	0 = No Spectral Reversal

1001 0000 0000 0000 0000 0000 0000 0000 0110 1110

TABLE 15. SAMPLE FORMAT FOR CONTROL WORD 5 HDF/OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	101 = Control Word 5.
36	Update	1 = Control Register Update.
35-21	HDF Decimation Counter Preload	F = Decimation by 16 in HDF.
20-5	Scaling Multiplier Gain	8000 = Scaling Multiplier Gain of 1.
4-3	Output Format	00 = Two's Complement.
2-1	Number of Output Bits	00 = 16-Bits.
0	Output Sense	1 = MSB First.

1011 0000 0000 0001 1111 0000 0000 0000 0000 0000

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TABLE 16. SAMPLE FORMAT FOR CONTROL WORD 6 - OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	110 = Control Word 6.
36	Update	1 = Control Register Update.
35	I followed by Q	1 = I and Q Data Output on I Pin.
34-29	Time Slot	Time Slot Number = 0.
28	IQCLK Polarity	0 = Data Stable on Rising Edge of IQCLK.
27	IQCLK Duty Cycle	1 = IQCLK Duty Cycle is 50%.
26	IQCLK Duration	1 = Active Continuously.
25-24	IQCLK Three-State Control	01 = Enable IQCLK.
23	IQSTB Polarity	0 = IQSTB Active High.
22	IQSTB Location	0 = IQSTB Active Prior to the Beginning of the Data Word.
21-20	IQSTB Three-State	01 = Enable IQSTB.
19	I Polarity	0 = I Output Active High.
18-17	I Three-State Control	01 = Enable I.
16	Q Polarity	0 = Q Output Active High.
15-14	Q Three-State Control	00 = Disable Q.
13	Input Format	1 = Two's complement.
12-0	IQCLK Rate	All Zeroes = CLK Used to Clock Output Bits.

1101 1000 0000 1101 0001 0010 001X XXXX XXXX XXXX

TABLE 17. SUMMARY OF CONTROL WORDS FOR THE EXAMPLE

CONTROL WORD	HEX VALUE
0	0 0 0 0 0 0 0 0 0 0
1	3 X X X X X X X X 1
2	5 0 0 0 0 0 0 0 0 0
3	7 0 0 0 0 0 0 0 0 0
4	9 0 0 0 0 0 0 0 6 E
5	B 0 0 1 F 0 0 0 0 0
6	D 8 0 D 1 2 X X X X
7	0 0 0 0 0 0 0 0 0 0

Quadrature To Real Conversion

After the input data has been processed by the DDC, the output can be converted into a real signal if desired. In that case, the baseband centered quadrature signal is upcobaseband. The real part of the upconverted signal is taken as the output. To satisfy the Nyquist criteria, the sample rate of the resulting signal must be at least twice the minimum sample rate of the I and Q components of the quadrature signal. This prevents one sideband from aliasing onto the other sideband when the real part of the output signal is taken.

The spectrum of a quadrature signal which has been over sampled by 2 is shown in Figure 17A. This represents the output of the filters. As described in the previous paragraph, the oversampling is a necessary feature of this process, since the final signal will occupy twice the bandwidth of the filter output. To prevent aliasing upon taking the real part of the signal, it is necessary to perform an up conversion by f"/4, where f" is the decimated sample frequency. (Note that f_S is defined as the input sampling frequency, f' is the input sampling frequency divided by the HDF decimation rate R, and f" is f' divided by the FIR decimation rate. f" is the FIR output sampling rate). The up conversion function is:

$$e^{j2\pi nf"/4f"} = e^{j\pi n/2} \quad \text{(EQ. 21)}$$

For n = 0, 1, 2, 3, 4,... the output values of the local oscillator in rectangular representation are: 1 + 0j, 0 + j, -1 + 0j, 0 - j, 1 + 0j,.... Since the real half of the complex multiplication of the local oscillator values by the filtered signal values (the desired output is the real part of the product) require only trivial operations, this up conversion is done in the Formatter. Figure 17B shows the signal spectrum after up conversion. Figure 17C shows the spectrum of the real output signal.

Continuing with the single tone example from the previous section, the quadrature signal output from the FIR filters is:

$$w(n) = \cos((\omega_k - \omega_c)n) + j\sin((\omega_k - \omega_c)n) = e^{j(\omega_k - \omega_c)n} \quad \text{(EQ. 22)}$$

Multiplying w(n) by the up convert function and summing the result is equivalent to the output sequence:

$$\begin{aligned} &y(n) = 1 \times \cos((\omega_k - \omega_c)n), \\ &y(n+1) = j \times j\sin((\omega_k - \omega_c)(n+1)), \\ &y(n+2) = -1 \times \cos((\omega_k - \omega_c)(n+2)), \\ &y(n+3) = -j \times j\sin((\omega_k - \omega_c)(n+3)), \\ &y(n+4) = 1 \times \cos((\omega_k - \omega_c)(n+4)),... \end{aligned} \quad \text{(EQ. 23)}$$

$$y = \cos((\omega_k - \omega_c)n), -\sin((\omega_k - \omega_c)(n+1)), -\cos((\omega_k - \omega_c)(n+2)), \sin((\omega_k - \omega_c)(n+3)), \cos((\omega_k - \omega_c)(n+4)),...$$

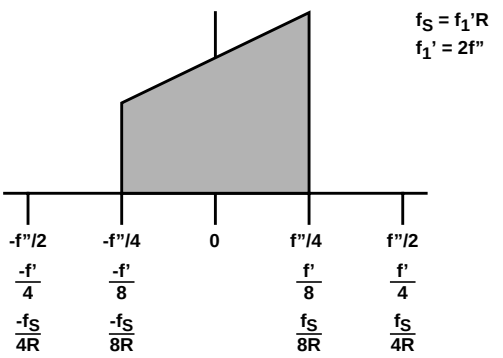
Or:

$$y = RE(w(n)), - IM(w(n+1)), - RE(w(n+2)), IM(w(n+3)), RE(w(n+4)),...$$

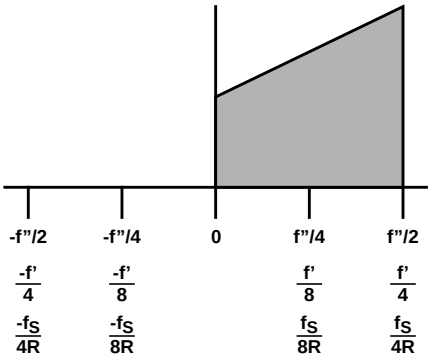
Since $|e^{j\pi n/2}| = 1$ and |w(n)| = 1, no further magnitude corrections are required.

The setup for this application is similar to that of the down conversion circuit given above, except the Output Formatter is set for Real Mode (Bit 31 in Control Word 4). This bit configures the part for up conversion by f"/4 and summing of the real and imaginary parts of the filter output.

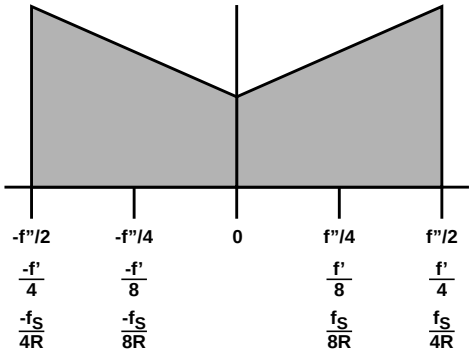
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A. OUTPUT OF FIR FILTERS: SIGNAL OVERSAMPLED BY 2



B. FIRST OPERATION IN FORMATTER: UP CONVERT BY SAMPLE FREQUENCY / 4



C. SECOND OPERATION IN FORMATTER: I OUTPUT = I + Q

FIGURE 17. QUADRATURE TO REAL CONVERSION OF AN OUTPUT SIGNAL

Up Conversion by f"/2

This operation allows the user to exchange the positions of the upper and lower halves of a down converted signal while leaving each half unchanged. Quadrature up conversion by f"/2 is performed by multiplying the output signal by $e^{j2\pi nf"/2} = \cos(2pnf"/2) + j \sin(2pnf"/2)$. When sampled at a rate of f", cos(2pnf"/2) takes on the values 1, -1, 1, -1,... and sin(2pnf"/2) always = 0. Thus, the up convert LO sequence is:

$$e^{j\pi n} = 1 + j0, -1 + j0, 1 + j0, \ldots \quad \text{(EQ. 24)}$$

This sequence is multiplied by the output of the I and Q branches of the filter:

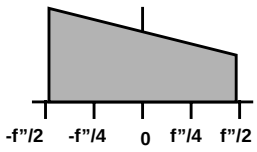
$$w(n) = \cos((\omega_k - \omega_c)n) + j\sin((\omega_k - \omega_c)n) = e^{j(\omega_k - \omega_c)n}, \quad \text{(EQ. 25)}$$

yielding an output sequence:

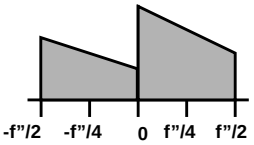
$$y = (RE(w(n)), IM(w(n))), \quad \text{(EQ. 26)}$$
$$-RE(w(n+1)), - IM(w(n+1))),$$
$$RE(w(n+2)), IM(w(n+2))), \ldots$$

The Formatter contains the circuitry to shift the quadrature output spectrum up by one half of the output sample frequency f". This operation is independent of the function of the Phase Generator and Mixer. The spectra of the outputs of the Filter and Formatter are shown in Figure 18.

The setup is identical to the down conversion configuration, except that the Up Convert Bit is set in Control Word 4.



A. OUTPUT OF FIR FILTERS



B. FILTER OUTPUT UP CONVERTED BY OUTPUT SAMPLE FREQUENCY / 2

FIGURE 18. UP CONVERSION BY F" / 2

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Quadrature Spectral Reversal

Spectral reversal is often used to negate a spectral reversal which has occurred due to a previous operation in the processing chain. Examples of this are spectral reversal in an analog down conversion or in a constructive aliasing operation. The DDC gives the user the ability to convert the signal to baseband in either forward or reverse fashion. Quadrature spectral reversal is achieved by translating the lower sideband of the input to baseband rather than the upper sideband. This is implemented in the DDC by mixing the input signal with $e^{j2\pi f_c n}$ - that is, up converting the input rather than down converting it. The resulting signal is:

$$u(n)= x(n)e^{j2\pi f_c n} = x(n)[\cos(\omega_c n) + j\sin(\omega_c n)] \quad \text{(EQ. 27)}$$

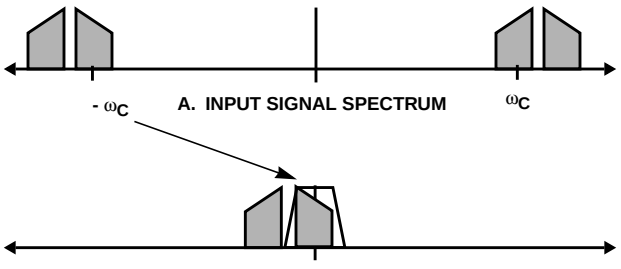
Assuming $x(n) = \cos(\omega_k n)$,

$$\begin{aligned} u(n) &= \cos(\omega_k n)[\cos(\omega_c n) + j\sin(\omega_c n)] \quad \text{(EQ. 28)} \\ &= [\cos((\omega_k - \omega_c)n) + \cos((\omega_k + \omega_c)n) \\ &+ j(\sin((\omega_k + \omega_c)n) - \sin((\omega_k - \omega_c)n))] \end{aligned}$$

After quadrature filtering and correcting for the gain of 1/2, we have:

$$\begin{aligned} w(n) &= \cos((\omega_k - \omega_c)n) - j\sin((\omega_k - \omega_c)n) \quad \text{(EQ. 29)} \\ &= \cos(-(\omega_k - \omega_c)n) + j\sin(-(\omega_k - \omega_c)n) \\ &= \cos((\omega_c - \omega_k)n) + j\sin((\omega_c - \omega_k)n) \\ &= e^{j(\omega_c - \omega_k)n} \end{aligned}$$

The appropriate spectral plots are shown in Figure 19. In up conversion, the sine output of the SIN/COS Generator is negated so that the vector output of the Local Oscillator rotates counter clockwise. This is implemented by setting the Spectral Reverse bit in Control Word 4 to a one. Otherwise, the setup for this mode is the same as the one for down conversion.

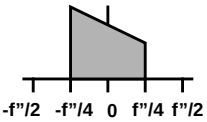


B. UP CONVERSION AND FILTERING

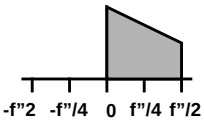
FIGURE 19. UP CONVERSION OF FILTER OUTPUT SIGNAL

Real Spectral Reversal

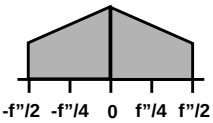
Real spectral reversal is simply quadrature spectral reversal with quadrature to real conversion in the Formatter. The up converted and filtered signal w(n) is upconverted again by f”/4 in the Formatter. Each sideband of the result is spectrally reversed from the sidebands that would have been produced by down conversion with quadrature to real conversion. The output spectrum is shown in Figure 20.



A. OUTPUT OF FILTERS: SIGNAL OVERSAMPLED BY 2



B. FIRST OPERATION IN FORMATTER: UP CONVERT BY SAMPLE FREQUENCY / 4



C. SECOND OPERATION IN FORMATTER: I OUTPUT = I + Q

FIGURE 20. QUADRATURE TO REAL CONVERSION OF AN OUTPUT SIGNAL

The setup for this application is similar to that of down conversion, except in Control Word 4, where the Spectral Reverse and Real Output bits are set to one.

High Decimation Filter Only

The DDC can be operated as a single high decimation filter. This is done by setting the Phase Generator to Filter Only and the Minimum Phase Increment and Phase Offset to 0. This multiplies the incoming data stream by a constant hexadecimal 3FFFF in the I channel and 0 in the Q channel. The HDF Section of the circuit requires a minimum decimation rate of 16 to allow sufficient time for the FIR to compute its response. This mode of operation implements a filter which has a decimation rate from 64 to 131,072. The frequency response is shown in Figures 7, 8 and 9. Only the I output has valid data in this mode; the Q output should be set to high impedance state to reduce circuit noise.

Multichannel Operation

Several DDCs can be placed in parallel with each one operating on a different frequency band. To minimize wiring, their outputs can be configured so that they are connected over a common serial bus. Each DDC is assigned a time slot number (Control Word 6) and a time slot length (Control Word 3). Each DDC in turn controls the bus for long enough to output its data, then relinquishes the bus. The time slot assignment and length are programmed at configuration time. Up to 64 chips can be multiplexed in this manner.

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Figure 21 shows a Block Diagram of this configuration. The DDCs are configured by the microprocessor by first writing a logical 0 to its Chip Select line. The control words are written to that part in any order. When the part has been configured, $\overline{CS}$ is written high again, and the next part is configured in the same manner. Collisions are prevented by programming each DDC with a unique Time Slot number, which holds its output from 0 to 63 output word times before transmission. Each part also has a Time Slot Length, whose minimum value is given in Equation 8. Note that a value greater than the minimum can be used to give the processor time to operate on the data

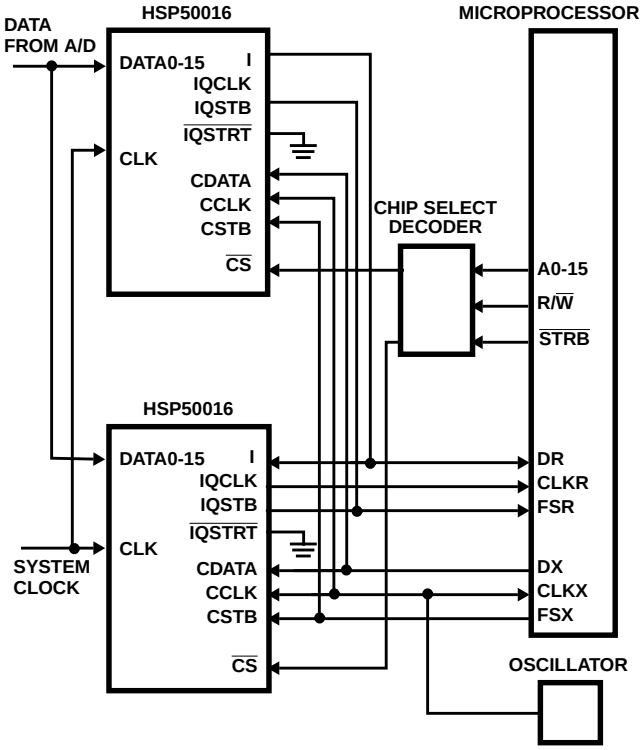


FIGURE 21. CIRCUIT FOR MULTIPLE CHANNEL OPERATION (AUTO THREE-STATE)

The corresponding Configuration Register setup is similar to that of single channel down conversion, except for the Auto Three-State fields. In this example, the first DDC in the chain is set to drive IQCLK; the others have this output set for high impedance. (It makes no difference which DDC is chosen to be the one to drive IQCLK, but it must be active continuously). The unused outputs are put in their high impedance condition on the other DDCs to minimize power consumption. Note also that this example shows all DDCs in I followed by Q Mode so that only one data line to the microprocessor is necessary. Figure 22 gives the timing of the output data.

When operating a set of HSP50016s in the Multiple Channel Operation Mode, the two control signals that ensure proper time slot operation are: $\overline{CS}$ and $\overline{RESET}$. The $\overline{CS}$ allows unique Control Word loading of each DDC. The $\overline{RESET}$ synchronizes all of the DDC's to the start of the first time slot.

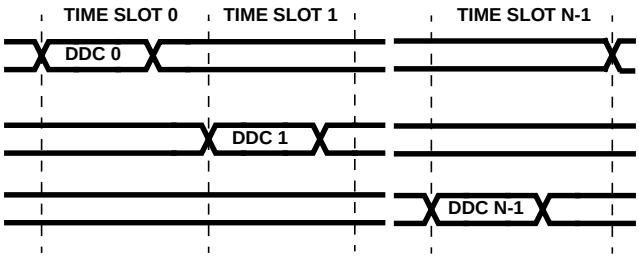


FIGURE 22. TIMING FOR MULTIPLE CHANNEL OPERATION (AUTO THREE-STATE)

NOTE: In this mode, it was anticipated that parallel DDC's would be programmed identically, except for the NCO (L.O.) frequency and Time Slot Number. This implies identical HDF Decimation factors, Time Slot Length's, Number of Output Bits, Output Mode are identical in all DDCs. This means that the output rate of all DDC HDFs, FIRs and Parallel to Serial Converters are identical.

The DDC keeps an internal count of the number of IQCLK periods that have transpired since the rising edge of $\overline{RESET}$. The internal counter of each DDC is set to enable the serial output at the time slot number assigned to that DDC. The count is based on the time slot length, number of output bits, HDF decimation, and Output Mode programmed to that part.

NOTE: In the Multiple Channel Operation Mode, all the time slot lengths should be set to the same value to avoid output signal contention. The time slot length should be equal to the largest "minimum time slot length" as calculated by Equation 15, for every DDC in the multichannel arrangement. Note that Equation 8 is in IQCLK periods, not CLK periods. Equations 7 and 9 will be helpful in making the translation to CLK periods.

This mode does not require that all of the time slots be used (assigned to a DDC). If only two parts were used and the maximum time signal isolation was desired, one could assign the first signal time slot 31 and the second signal time slot 63. This would ensure that the maximum separation in time occurred. It is the designers responsibility to ensure that the output rate, including the decimation is consistent with the time allotted to output each signal.

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Let's return to the clock calculation example found in the Output Formatter, and add the requirement of 4 time slots. The calculations in the Example Clock Calculation Section remain true, but step 8 must be added:

8. Now lets consider the multichannel timing. Each channel must output the data at no less than 1.725MHz to get all the I/Q data out in the allocated time for the assigned time slot. Time margin is created when the output is clocked out at a higher rate. Because each channel is outputting data in only one of four channels, the effective output rate for each channel is 1.725MHz /4 = 431.25kHz, even though the part is outputting data 1.7MHz in every time slot. . . . . Effective Channel Output Rate = 431.25kHz

Alternatively, the processor can request data from each of the DDCs asynchronously. In this setup, Requested Output Mode is used. The Data Concentrator polls each channel individually and is responsible for ensuring that each channel is polled before the output data is lost. The Data Concentrator is a custom circuit designed by the user. A Block Diagram of such a system is shown in Figure 23. The interface between the controller and the DDCs has been omitted for the sake of clarity.

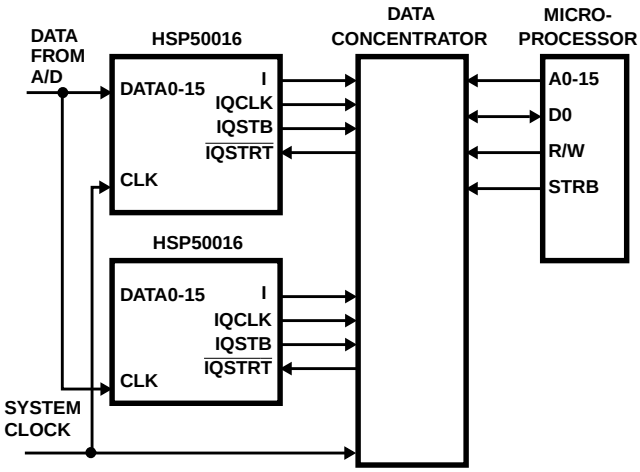


FIGURE 23. CIRCUIT FOR MULTIPLE CHANNEL OPERATION (REQUESTED OUTPUT)

References

[1] Hogenauer, Eugene V., An Economical Class of Digital Filters for Decimation and Interpolation, IEEE Transactions on Acoustics, Speech and Signal Processing, April 1981.

[2] IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1 - 1990.

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Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.75V to +5.25V
Operating Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CPGA Package	45	7
PLCC Package	35	N/A

Maximum Junction Temperature
CPGA Package . . . . . 150^oC
PLCC Package . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

Gate Count . . . . . 65,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5.0V ±5%, T_A = 0^o to 70^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = Max, CLK Frequency 52.6MHz Notes 2, 3	-	394	mA
		V_{CC} = Max, CLK Frequency 76.9MHz Notes 2, 3	-	577	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	500	µA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC} TMS, TDI, $\overline{TRST}$	-500	10	µA
		V_{CC} = Max, Input = 0V or V_{CC} All other inputs	-10	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min	-	0.8	V
Logical One Input Voltage: CLK, $\overline{TRST}$	V_{IHC}	V_{CC} = Max	3.0	-	V
Logical One Output Voltage	V_{OH}	I_{OH} = -5mA, V_{CC} = Min	2.6	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 5mA, V_{CC} = Min	-	0.4	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz All measurements referenced to GND. T_A = 25^oC, Note 4	-	10	pF
Output Capacitance	C_{OUT}		-	10	pF

NOTES:

2. Power supply current is proportional to frequency. Typical rating is 7.5mA/MHz. Note that operation at maximum clock frequency will exceed maximum junction temperature of device. Use of a heat sink and/or air flow is required under these conditions: Recommended heat sink is EG&G Wakefield D10650-40.
3. Output load per test circuit and C_L = 40pF.
4. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications

V_{CC} = 5.0V ±5%, T_A = 0^o to 70^oC, (Note 5)

PARAMETER	SYMBOL	NOTES	-52(52.6)MHz		-75(76.9)MHz		UNITS
			MIN	MAX	MIN	MAX	
CLK Period	t_{CP}		19	-	13	-	ns
CLK High	t_{CH}		7	-	5	-	ns
CLK Low	t_{CL}		7	-	5	-	ns
Setup Time DATA0-15 to CLK	t_{DS}		10	-	7	-	ns
Hold Time DATA0-15 from CLK	t_{DH}		1	-	1	-	ns
$\overline{RESET}$ Pulse Width	t_{RL}		t_{CP}+11	-	t_{CP}+8	-	ns

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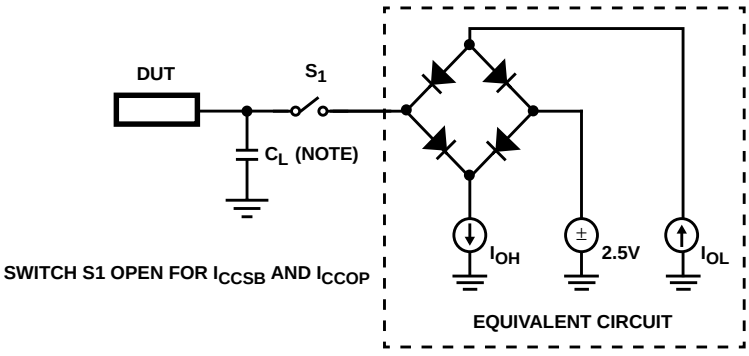
AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0^o to 70^oC, (Note 5) **(Continued)**

PARAMETER	SYMBOL	NOTES	-52(52.6)MHz		-75(76.9)MHz		UNITS
			MIN	MAX	MIN	MAX	
$\overline{RESET}$, $\overline{IQSTRT}$ Setup Time from CLK	t_{RS}	Note 6	10	-	7	-	ns
RESET, $\overline{IQSTRT}$ Hold Time to CLK	t_{RH}	Note 6	1	-	1	-	ns
CLK to I, Q, IQSTB, IQCLK Delay	t_{DO}		-	15	-	12	ns
CCLK Period	t_{CCP}		100	-	100	-	ns
CCLK High	t_{CCH}		40	-	40	-	ns
CCLK Low	t_{CCL}		40	-	40	-	ns
CDATA, CSTB, $\overline{CS}$ Setup to CCLK	t_{CDS}		30	-	30	-	ns
CDATA, CSTB, $\overline{CS}$ Hold from CCLK	t_{CDH}		30	-	30	-	ns
CCLK Low Setup to CLK	t_{CLS}	Notes 6, 7	30	-	30	-	ns
CCLK High Hold from CLK	t_{CHH}	Notes 6, 7, 10	30	-	30	-	ns
TCK Period	t_{TCP}	Note 8	100	-	100	-	ns
TCK High	t_{TH}		40	-	40	-	ns
TCK Low	t_{TL}		40	-	40	-	ns
$\overline{TRST}$ Pulse Width	t_{TRL}		100	-	100	-	ns
TCK to TDO, Data Delay	t_{TDO}		-	30	-	30	ns
Setup Time On All Inputs to TCK	t_{ATS}	Note 9	30	-	30	-	ns
Hold Time On All Inputs from TCK	t_{ATH}	Note 9	30	-	30	-	ns
TCK Setup Time to CLK	t_{TCS}	Note 8	30	-	30	-	ns
TCK Hold Time from CLK	t_{TCH}	Note 8	30	-	30	-	ns
Output Enable Time from CLK	t_{OE}	Note 10	-	18	-	12	ns
Output Disable Time from CLK	t_{OD}	Note 10	-	18	-	12	ns
Output Enable Time from TCK	t_{TOE}	Note 10	-	32	-	32	ns
Output Disable Time from TCK	t_{TOD}	Note 10	-	32	-	32	ns
Output Rise, Fall Time	t_{RF}	Note 10	-	5	-	5	ns

NOTES:

5. AC tests performed with C_L= 40pF, I_{OL} = 5mA, and I_{OH} = -5mA. Input reference level for CLK, $\overline{TRST}$ is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V; V_{OH} = V_{OL} = 2.5V.
6. These are asynchronous inputs; setup and hold times must only be maintained in order to predict which clock cycle they take effect internally.
7. Timing must only be maintained when Update bit is active in control word data being loaded.
8. Special Timing relationship between TCK and CLK is required for Test Instructions RUNBIST, EXTEST and INTEST.
9. All inputs except $\overline{TRST}$, and only when TCK is driving internal clock.
10. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

AC Test Load Circuit



NOTE: Test head capacitance.

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Waveforms

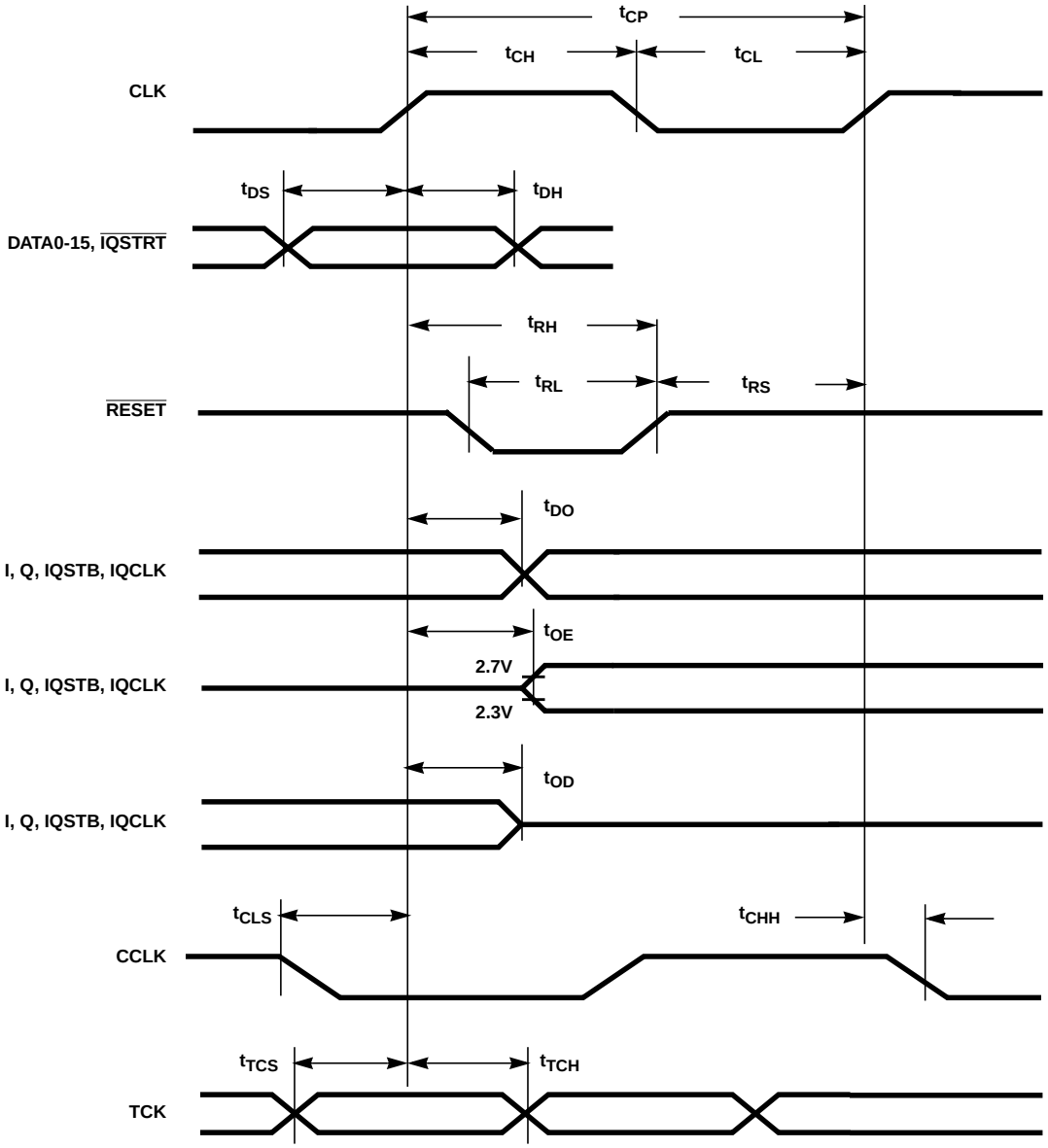


FIGURE 24. TIMING RELATIVE TO CLK

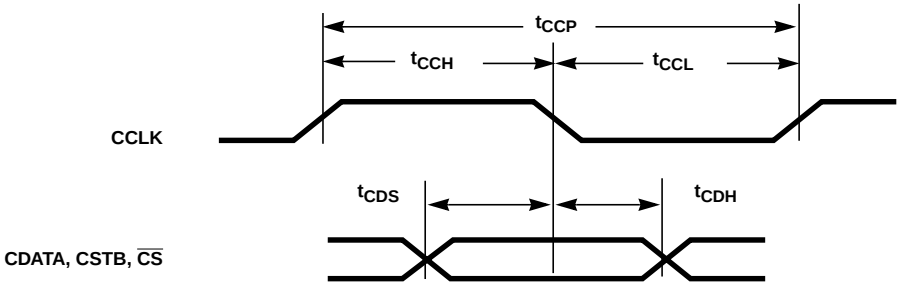


FIGURE 25. TIMING RELATIVE TO CCLK

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Waveforms (Continued)

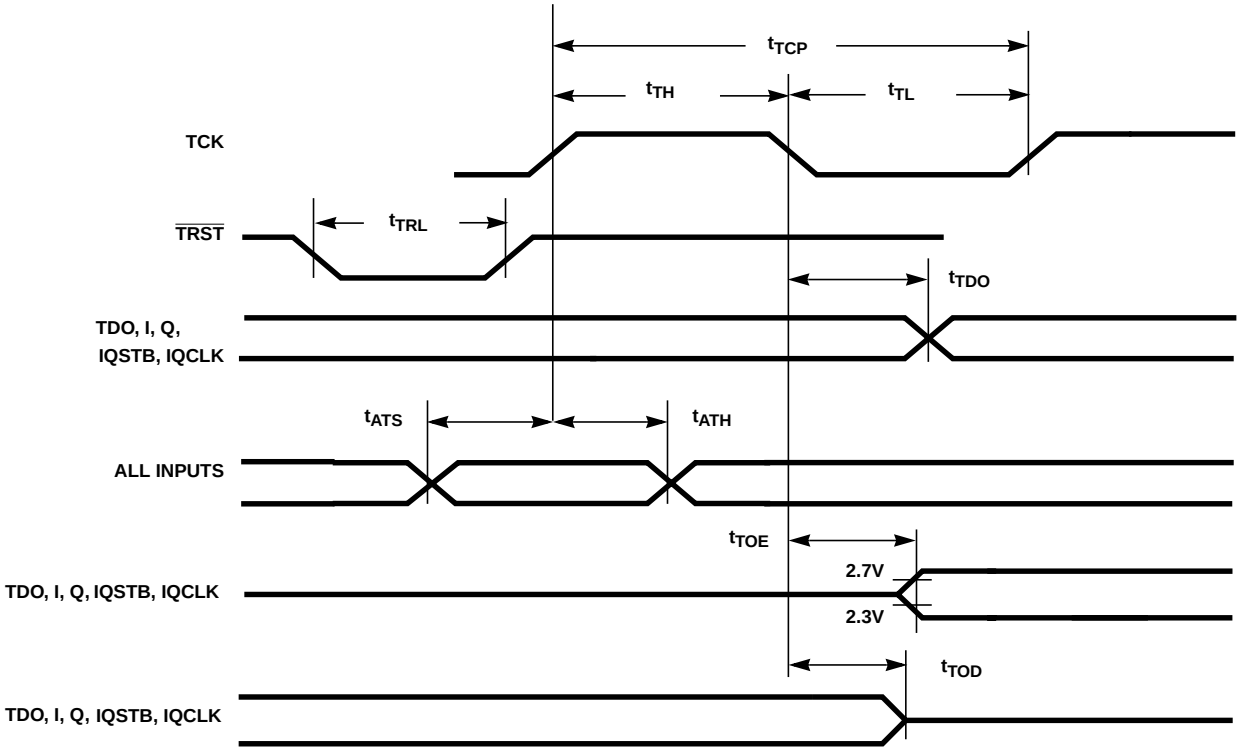


FIGURE 26. TIMING RELATIVE TO TCK

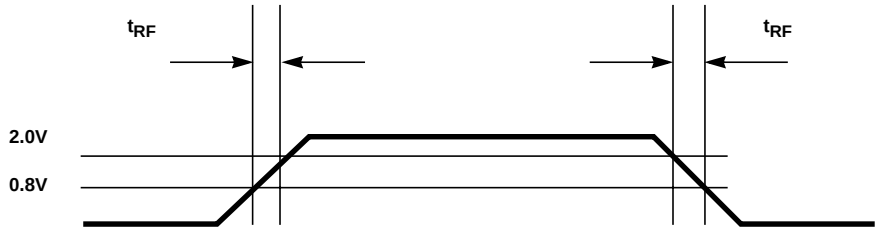


FIGURE 27. OUTPUT RISE AND FALL TIMES

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Appendix D: Graychip GC1012A Digital Tuner Chip

D.1 Introduction

The following section contains the data sheet for the Graychip GC1012A Digital Tuner Chip.

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GC1012A

DIGITAL TUNER CHIP

DATASHEET

Revision 0.0

February 18, 1998

This datasheet contains information which may be changed at any time without notice.

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REVISION HISTORY

This datasheet is revised from the GC1012 datasheet to reflect the changes in the GC1012A replacement.

Revision	Date	Description
0.0	18 Feb 1998	First GC1012A datasheet. Major changes in specifications. Bits 5,6,7 of register 7 and bit 7 of register 9 changed to reflect new power down/keepalive modes.
0.1	?	Page 8: Pin pitch P on drawing corrected to 0.8mm. Table was correct.

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GC1012A DATASHEET

1.0 FUNCTIONAL DESCRIPTION

Fabricated in high speed CMOS technology, the GC1012A chip is an all digital tuner which can downconvert and band limit signals from wide band digitized sources. At full rate operation (80 MHz input rate), the input bandwidth can be up to 40 MHz wide. Any signal within the input bandwidth can be down-converted to zero frequency, low pass filtered, and output at a reduced sample rate. The chip's output can be formatted as either a complex data stream, or as a real data stream. The complex samples are output at rates equal to $F_O=F_{CK}/D$, where F_O is the output rate, D is 1, 2, 4, 8, 16, 32 or 64 and F_{CK} is the input sample (clock) rate. The real output rates are $F_O=2F_{CK}/D$ for D equal to 2, 4, 8, 16, 32, or 64.

The signal is low pass filtered to remove out of band energy before the sample rate is decreased. The filter's out of band rejection is over 75 dB and its passband ripple is less than 0.2 dB peak to peak. The passband of the output filter covers 80% of the output bandwidth.

The 28 bit accumulator in the chip's digital oscillator circuit provides a tuning accuracy equal to the input clock rate divided by 2^{28}. The tuning resolution at a clock rate of 50 MHz is less than 0.2 Hz giving a tuning accuracy of +/- 0.1 Hz. The phase noise in the oscillator is low enough to provide a spur free dynamic range of over 75 dB.

The chip's output circuit allows the user to select a real or complex data output format, to select spectral inversion, or to offset the output spectrum by half of the output sample rate. The output's signal gain can be adjusted in 0.03 dB steps. The word size of the output samples are either 10, 12, 14, or 16 bits.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of an 8 bit data I/O port, a 4 bit address port, a read/$\overline{\text{write}}$ bit, and a control select strobe.

I and Q output registers can be read from the control port to allow an external processor to monitor or process the chip's output samples. These registers are valuable for monitoring the chip's output power in order to set and adjust gain levels.

1.1 KEY FEATURES

- 80 million samples per second input rate
- 0.1 Hz tuning resolution
- >75 dB dynamic range
- Programmable output bandwidth
- 12 bit inputs, 10, 12, 14, or 16 bit outputs
- Real or complex output formats
- Built in strobe/sync generator
- Symmetric rounding used throughout
- Gain adjust in 0.03 dB steps
- Microprocessor interface for control, output, and diagnostics
- Power down mode
- Auto power down with clock loss detection
- Built in diagnostics
- 3.25W power at 50 MHz, 5 volts
- 850 mW at 30 MHz, 3.3 volts
- 120 pin quad flat pack package

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1.2 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1

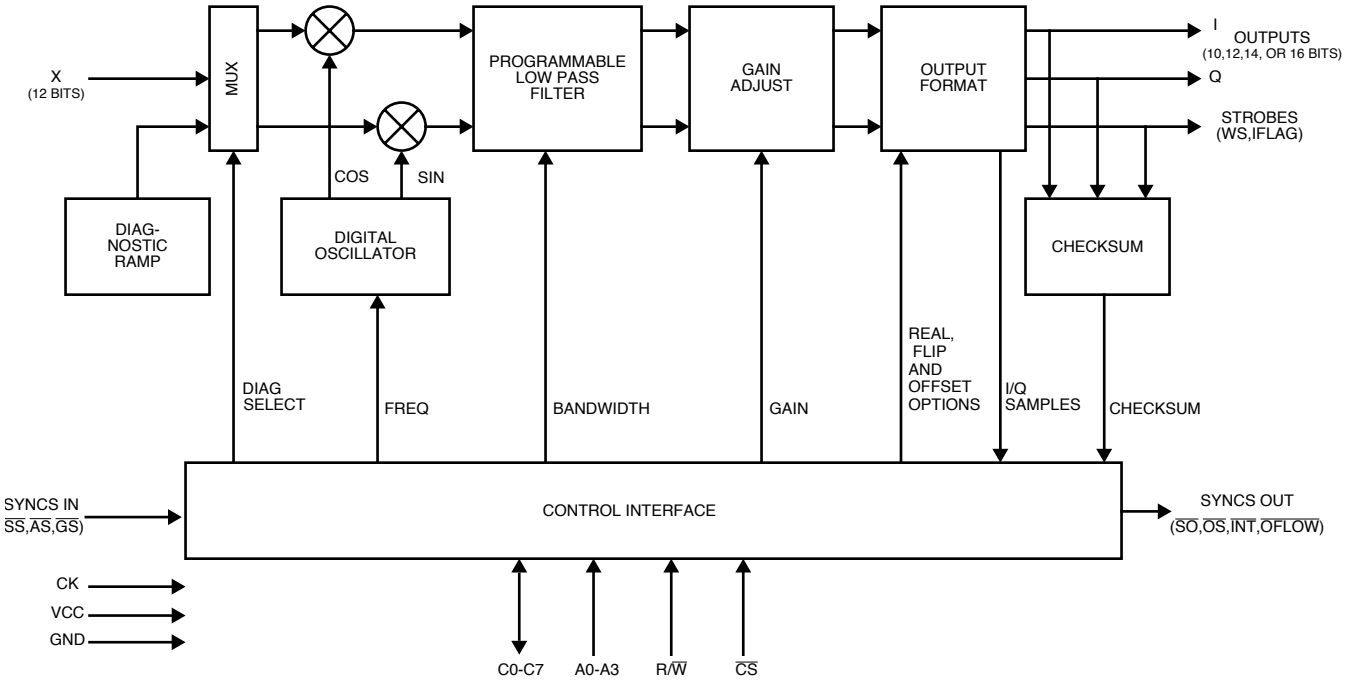


Figure 1. GC1012A Block Diagram

Each of these functions are described below.

1.3 CONTROL INTERFACE

The control interface performs four major functions: It allows an external processor to configure the chip, it allows an external processor to capture and read output samples from the chip, it allows an external processor to perform diagnostics, and it generates internal synchronization strobes.

The chip is configured by writing control information into 8 bit control registers within the chip. The contents of these control registers and how to use them are described in Section 3. The registers are written to or read from using the **C[0:7]**, **A[0:3]**, **R/$\overline{W}$**, and **$\overline{CS}$** pins. Each control register has been assigned a unique address within the chip. An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:3]** to the desired register address, setting the **R/$\overline{W}$** pin low, setting **D[0:7]** to the desired value and then pulsing **$\overline{CS}$** low.

To read from a control register the processor must set **A[0:3]** to the desired address, set **R/$\overline{W}$** high, and then set **$\overline{CS}$** low. The chip will then drive **C[0:7]** with the contents of the selected register. After the processor has read the value from **C[0:7]** it should set **$\overline{CS}$** high. The **C[0:7]** pins are turned off (high impedance) whenever **$\overline{CS}$** is high or **R/$\overline{W}$** is low. The chip will only drive these pins when **$\overline{CS}$** is low and **R/$\overline{W}$** is high.

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Control register addresses 12, 13, 14, and 15 are reserved to allow an external processor to read output samples from the chip. Addresses 12 and 13 are the I-registers which store the16 bit in-phase part of the output sample. Addresses 14 and 15 are the Q-registers which store the quadrature part. In the real mode the I registers store the even-time output samples and the Q registers store the odd-time output samples. Output ready and missed flags are provided in control register 9 in order to synchronize the storing and reading of the output samples. An interrupt output pin is also provided on the chip which can be used to interrupt the external processor when a new sample is ready. See the description of control register 9 in Section 3.6 for more details. The setup, hold and pulse width requirements for control read or write operations are given in Section 4.4.

Checksums are read from the chip during diagnostics using address 11. More details on the diagnostic modes is given in Section 1.11.

Address 10 is used to generate a one-shot pulse on the $\overline{\textbf{OS}}$ output pin. This pulse can be used to synchronize the output timing and/or frequency oscillators of multiple GC1012A chips.

The control interface also generates the chip's internal sync strobes. The user may select to synchronize the chip using an external sync strobe ($\overline{\textbf{SS}}$), or use the chip's internal sync counter. The internal sync counter can be synchronized to $\overline{\textbf{SS}}$, or left to free run (See **SS_OFF** in Section 3.2). The period of the internal sync counter can be either 256 clocks or 2^{20} clocks. The 256 clock period is intended to be used for chip test purposes only. The internal sync counter is used during diagnostics to clear the data paths and strobe the checksum generator. The internal sync counter can also be used to periodically re-synchronize all of the counters in the chip during normal operating modes.

1.4 DIGITAL OSCILLATOR

The digital oscillator generates sine and cosine sequences which are used to mix the desired signal down to zero frequency. The digital oscillator contains a 28 bit frequency register, a 28 bit frequency accumulator, and a sine-cosine generator. The tuning frequency of the oscillator is set by loading a 28 bit frequency word from the control registers into the frequency register. If the frequency register is set to the word **FREQ**, then the tuning frequency will be: $\text{Frequency} = \frac{\text{Sample Rate}}{2^{28}}\textbf{FREQ}$. The tuning frequency should be set to the middle of the desired output bandwidth.

The frequency word **FREQ** is stored into the control registers at control addresses 0,1,2 and 3. The 28 bit word is then transferred into the frequency register using one of the following methods:

(1) The frequency register is always loading (the frequency changes immediately as the frequency word is loaded into the control registers).

(2) The frequency register is loaded when the user sets a control register bit.

(3) The frequency register is synchronously loaded when the accumulator sync strobe ($\overline{\textbf{AS}}$) goes low.

(4) The frequency register is synchronously loaded when the system sync strobe ($\overline{\textbf{SS}}$) goes low.

See Section 3.2 for more details on the frequency load modes.

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The 28 bit frequency word is accumulated in the 28 bit frequency accumulator. The frequency accumulator will normally free run, but can be synchronously cleared by either the system sync (**$\overline{\text{SS}}$**) or the accumulator sync (**$\overline{\text{AS}}$**). The accumulator clear modes are controlled by bits in control register 4. See Section 3.2 for details.

The upper 13 frequency accumulator bits are used to generate the oscillator's sine and cosine outputs. These sines and cosines are generated to 12 bit accuracy. The oscillator's peak spur levels are below -75 dB.

1.5 MIXER

The mixer multiplies the 12 bit input samples by the 12 bit sine and cosine values coming from the digital oscillator. An input signal at the oscillator's tuning frequency will be centered at zero frequency after passing through the mixer. The mixer outputs are rounded to 13 bits using the "round-to-even" rounding algorithm. The "round-to-even" algorithm prevents a DC rounding bias by detecting fractions which are exactly equal to 0.5 and rounding them up half of the time and rounding them down half of the time. The choice to round up or down is made so as to always give an even result.

1.6 PROGRAMMABLE LOW PASS FILTER

The mixer's output is filtered using a programmable bandwidth low pass filter. The filter allows the output sample rate to be reduced by a factor of **D** = 2, 4, 8, 16, 32, or 64. The value of **D** is set using control register 5. The filter can be bypassed by setting **D** equal to 1. This allows the chip to be used as a mixer without any output filtering.

The low pass filter is a finite impulse response (FIR) filter with linear phase, 0.13 dB peak to peak ripple and over 75 dB of out of band rejection. The 2 dB output bandwidth is +/- $0.4F_S$ (80% usable bandwidth) where F_S is the complex output rate. The 0.1 dB bandwidth is +/- 0.36 F_S (72% usable bandwidth).

The coefficients for the 40 tap decimate by 2 filter are:

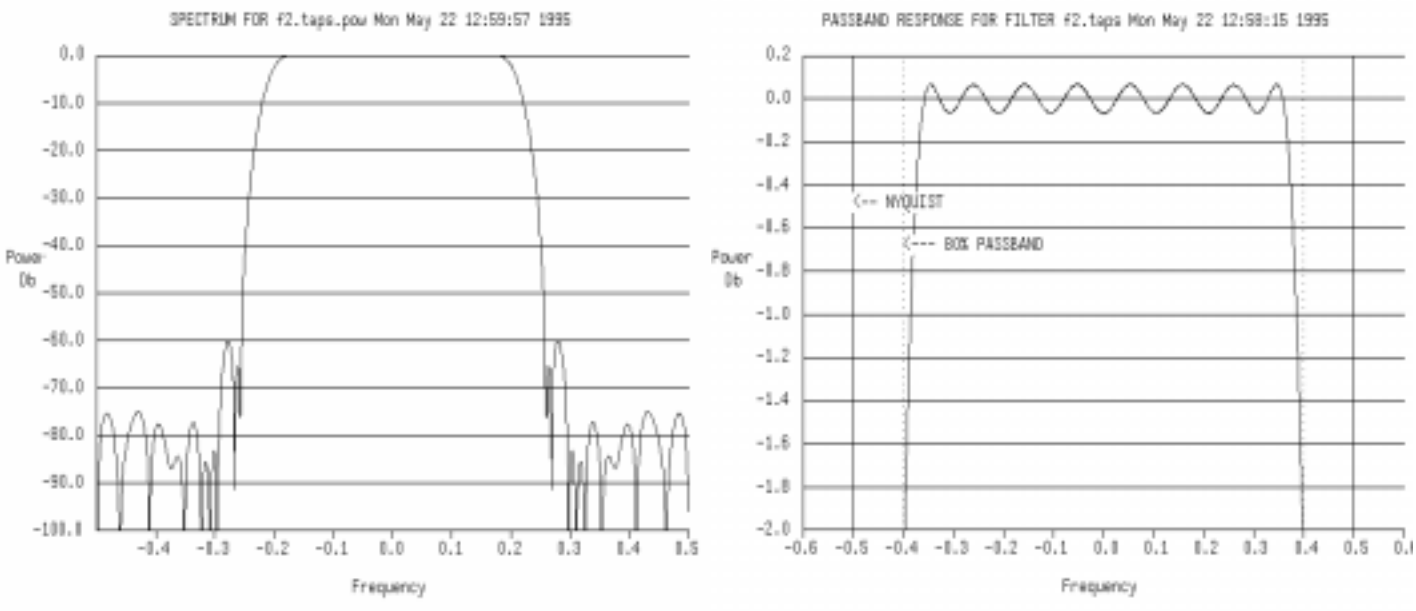
-12	-42	-52	7	85	46	-110	-145	82	276
39	-396	-293	434	714	-273	-1400	-409	3115	6462
6462	3115	-409	-1400	-273	714	434	-293	-396	39
276	82	-145	-110	46	85	7	-52	-42	-12

The coefficients for the other filters are available from GRAYCHIP.

Figure 2 shows the spectral response of the decimate by 2 low pass filter. The decimate by 4, 8, 16, 32 and 64 filters are similar. Figure 2(a) shows the overall frequency response prior to decimation.Note that the filter rolls off quickly to 60 dB and is down below 75 dB in the region which aliases back into the passband. Figure 2(b) shows the 0.13 dB ripple in the passband.

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(a) Overall (b) Passband

Figure 2. Filter Response

1.7 GAIN

The programmable bandwidth filter is followed by a gain circuit which adjusts the output level in 0.03 dB steps. The gain is controlled by the power of two gain value **S** and the fractional gain value **F**. The input to output gain of the chip is equal to $\mathbf{G} = 2^{(\mathbf{S}-B)}(1+\mathbf{F}/256)$, where **S** ranges from 0 to 15, **F** ranges from 0 to 255, and **B** is the base gain setting for each value of **D**. The base gain setting **B** gives a unity input to output gain for the chip, i.e., a 12 bit constant going into the chip will come out in the 12 MSBs of the 16 bit output word. The values of **B** are:

D	**B**
1	6
2	5
4	4
8	3
16	2
32	1
64	0

The **S** and **F** gain settings are double buffered so that they can be applied synchronously. A new gain setting takes effect either when **S** is loaded, or, if the GS_MODE control bit is used, when the $\overline{\mathbf{GS}}$ strobe is received.

The gain settings and GS_MODE bit are stored in control registers 6 and 7.

Overflow detection circuitry detects overflow conditions in the gain output words and saturates the samples to plus or minus full scale. Overflows are reported in the STATUS register and on the $\overline{\mathbf{OFLOW}}$ output pin. The overflow status can be used to detect if the gain settings are too high.

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1.8 OUTPUT FORMATTING

The output format circuit allows the user to flip the output spectrum, to offset the spectrum by one-fourth the Nyquist rate, to convert the complex output stream to a real one at twice the rate, to round the samples to 10, 12, 14 or16 bits, and to multiplexes the I and Q samples together. These options are set using control register 8.

A word strobe (**WS**) is generated as an output clock signal. The **WS** strobe is either one clock cycle wide or is a 50% duty cycle clock. The polarity of **WS** is programmable.

The I and Q samples can be multiplexed together onto the I output pins by using the IQMUX mode. The **IFLAG** output pin is used in this mode to identify when the I words are being output. The **WS** strobe rate is doubled in this mode. The Q output pins are cleared in this mode.

Only the I output pins are used in the real mode. The Q pins are cleared. The output spectrum is centered from 0 to $F_O/2$ in the real mode. The spectrum is centered from $-F_O/2$ to $+F_O/2$ in the complex mode. The OFFSET control allows the spectrum to be centered from 0 to F_O.

The output format circuitry is synchronized by the $\overline{\textbf{SS}}$ input sync. This allows one to synchronize the output timing of multiple GC1012A chips.

1.9 POWER DOWN AND KEEPALIVE MODES

Unused chips in a system can be powered down by setting the POWER_DOWN control bit in register 9 (See Section 3.6). This reduces the internal clock rate down to 1 KHz to minimize the power consumed by the chip while still refreshing the internal dynamic nodes at a suitable rate.

The chip includes a “keepalive” circuit which detects when the clock has stopped for more than 2 milliseconds. The chip will automatically go into the power down mode if clock loss is detected. The keepalive detection circuit can be disabled by setting bit 5 in register 7 (See Section 3.4). NOTE: The chip will draw up to an Amp of current if the clock is stopped and the keepalive circuit is disabled.

1.10 THE ONE SHOT PULSE GENERATOR

The chip can generate a one-shot pulse which is output on the $\overline{\textbf{OS}}$ pin by writing to address 10. The pulse can be connected to the $\overline{\textbf{SS}}$, $\overline{\textbf{AS}}$, or $\overline{\textbf{GS}}$ sync input pins of GC1012A chips (including itself) to synchronize the output timing, frequency oscillators, or gain settings of multiple chips.

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1.11 DIAGNOSTICS

An input ramp generator, a sync period generator, and a checksum generator are provided on the chip in order to run diagnostic tests. Diagnostics are performed by turning on the ramp generator, enabling the diagnostic syncs, letting the chip operate for at least 4 sync periods, reading the checksum and comparing it to its predicted value. A new checksum is generated every sync period. The input ramp sequence is the same for every sync period and the chip is re-initialized at the beginning of each sync period so that each checksum should be the same once the chip's data path has been flushed. The chip requires at least 3 sync periods to flush, so the fourth and following checksums should be valid. The test is then repeated for several different tuning frequencies, decimation settings, and output modes.

The sync period is 2^{20} clocks, or approximately 1 million clock cycles, so four sync periods will be about 4 million clocks. This represents a delay of less than 15 milliseconds for a clock rate of 60 MHz.

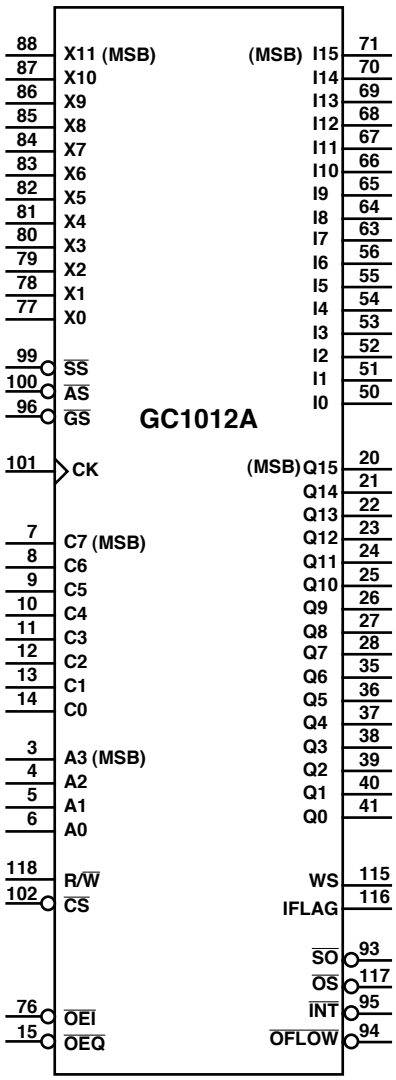
The following table lists the expected checksums for four test configurations. All values are in HEX.

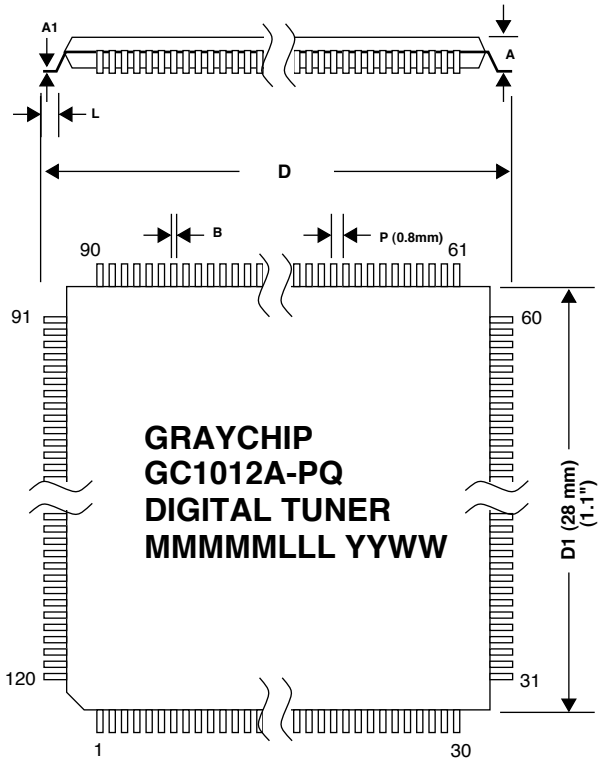
CONTROL REGISTER	TEST 1	TEST 2	TEST 3	TEST 4
FREQ (REG 0,1,2,3)	0000101	0F0F0F0	55AA55A	AA55AA5
SYNC MODE (REG 4)	A9	A9	A9	A9
FILTER MODE (REG 5)	82	93	E4	D7
GAIN FRACTION (REG 6)	AA	55	00	FF
GAIN EXPONENT (REG 7)	5	4	3	0
OUTPUT (REG 8)	16	46	21	80
EXPECTED CHECKSUMS (REG 11)	64	50	A7	03

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2.0 PIN DESCRIPTIONS





120 PIN QUAD FLAT PACK PACKAGE

GC1012A-PQ = Enhanced Thermal Plastic Package
GC1012A-CQ = Ceramic Package

Package Markings: MMMMM = Mask Code
LLL = Lot Number
YYWW = Date Code

DIMENSION		PLASTIC	CERAMIC
D	(width pin to pin)	31.2 mm (1.228")	32.0 mm (1.260")
D1	(width body)	28.0 mm (1.102")	28.0 mm (1.102")
P	(pin pitch)	0.8 mm (0.031")	0.8 mm (0.031")
B	(pin width)	0.35 mm (0.014")	0.35 mm (0.014")
L	(leg length)	0.88 mm (0.035")	0.70 mm (0.028")
A	(height)	4.07 mm (0.160")	3.25 mm (0.128")
A1	(pin thickness)	0.17 mm (0.007")	0.2 mm (0.008")

VCC PINS: 2,16,17,29,32,33,43,44,47,48,58,59,62,74,75,89,91,97, 104,105,106,109,110,114,119

GND PINS: 1,18,19,30,31,34,42,45,46,49,57,60,61,72,73,90,92,98, 103,107,108,111,112,113,120

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

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SIGNAL	DESCRIPTION
X[0:11]	**INPUT DATA.** Active high The 12 bit two's complement input samples. New samples are clocked into the chip on the rising edge of the clock. The input data rate is assumed to be equal to the clock rate.
CK	**CLOCK INPUT.** Active high The clock input to the chip. The **X**, **$\overline{SS}$**, **$\overline{GS}$** and **$\overline{AS}$** signals are clocked into the chip on the rising edge of this clock. The **I**, **Q**, **WS**, **IFLAG**, **$\overline{OS}$**, **$\overline{OFLOW}$** and **$\overline{SO}$** signals are clocked out on the rising edge of this clock.
$\overline{SS}$	**SYSTEM SYNC**. Active low The sync input to the chip. All timers, accumulators, and control counters are, or can be, synchronized to **$\overline{SS}$**. Bits in control register 4 (see Section 3.2) determine the operation of **$\overline{SS}$**. This sync is clocked into the chip on the rising edge of the clock.
$\overline{AS}$	**ACCUMULATOR SYNC**. Active low The accumulator sync is provided to synchronously change tuning frequencies. This sync can be used to load a new tuning frequency into the frequency register and/or to clear the frequency accumulator. This signal is clocked into the chip on the rising edge of the clock.
$\overline{GS}$	**GAIN SYNC**. Active low The gain sync is provided to synchronously change gain settings. This signal is clocked into the chip on the rising edge of the clock.
I[0:15]	**IN-PHASE OUTPUT DATA**. Active high The I part of each complex output sample is output as a 16 bit word on this pin. The bits are clocked out on the rising edge of the clock.
$\overline{OEI}$	**IN-PHASE OUTPUT ENABLE**. Active low The **I[0:15]** output pins are put into a high impedance state when this pin is high.
Q[0:15]	**QUADRATURE OUTPUT DATA**. Active high The Q part of each complex output sample is output as a 16 bit word on this pin. The bits are clocked out on the rising edge of the clock.
$\overline{OEQ}$	**QUADRATURE OUTPUT ENABLE**. Active low The **Q[0:15]** output pins are put into a high impedance state when this pin is high.
WS	**WORD STROBE**. Programmable active high or low level This strobe is output synchronous with the **I** and **Q** data words. The strobe occurs once per bit and is either one clock wide or has a 50% duty cycle. The high/low polarity of the strobe is programmable. See Section 3.5 for details.
IFLAG	**IN-PHASE STROBE**. Active high This strobe identifies the in-phase half of a complex pair when the outputs are in the IQ_MUX mode. See Section 3.5 for details. This signal is high when the I-half is output and is low when the Q-half is output.
$\overline{SO}$	**SYNC OUT**. Active low This signal is either a delayed version of the input system sync **$\overline{SS}$**, or, if SS_MUX in control register 4 is set, is the internally generated sync which has a period of 2^{20} clocks.
$\overline{INT}$	**INTERRUPT OUT**. Active low This signal is the READY flag from control register 9. This interrupt goes active when a new output sample is ready in control registers 12, 13, 14, and 15.
$\overline{OS}$	**ONE SHOT STROBE**. Active low This output is a one-shot sync strobe generated by writing to control address 10. The strobe is one clock cycle wide.
$\overline{OFLOW}$	**OVERFLOW FLAG**. Active low This signal goes low when an overflow is detected in the gain circuit. The signal will either pulse low for one clock cycle or will stay low depending upon the state of the OFLOW_MODE bit in control register 9.
C[0:7]	**CONTROL DATA I/O BUS**. Active high This is the 8 bit control data I/O bus. Control register data is loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{CS}$** is low and **R/$\overline{W}$** is high.
A[0:3]	**CONTROL ADDRESS BUS**. Active high These pins are used to address the 16 control registers within the chip. Each of the 16 control registers within the chip are assigned a unique address. A control register can be written to or read from by setting **A[0:3]** to the register's address.
R/$\overline{W}$	**READ/$\overline{WRITE}$ CONTROL**. High for read, low for write This pin determines if the control bus cycle is a read or write operation. The pin is high for a read and is low for a write.
$\overline{CS}$	**CONTROL STROBE**. Active low This control strobe enables the read or write operation. The contents of the register selected by **A[0:3]** will be output on **C[0:7]** when **R/$\overline{W}$** is high and **$\overline{CS}$** is low. If **R/$\overline{W}$** is low when **$\overline{CS}$** goes low, then the selected register will be loaded with the contents of **C[0:7].**

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3.0 CONTROL REGISTERS

The chip is configured and controlled through the use of 16 eight bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{CS}$**, **R/$\overline{W}$**, **A[0:3]**, and **C[0:7]**) described in the previous section. The register names and their addresses are:

ADDRESS	NAME	ADDRESS	NAME
0	FREQ byte 0	8	Output Mode
1	FREQ byte 1	9	Status
2	FREQ byte 2	10	One Shot
3	FREQ byte 3	11	Checksum
4	Sync mode	12	I-output byte 0
5	Filter mode	13	I-output byte 1
6	Gain Fraction	14	Q-output byte 0
7	Gain Exponent	15	Q-output byte 1

The following sections describe each of these registers. The type of each register bit is either R or R/W indicating whether the bit is read only or read/write. All bits are active high.

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3.1 FREQUENCY WORD REGISTERS

Registers 0, 1, 2, and 3 contain the 28 bit frequency tuning word. Bit 0 is the LSB, bit 27 is the MSB.

ADDRESS 0: FREQUENCY BYTE 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[0:7]	Byte 0 (least significant) of frequency word

ADDRESS 1: FREQUENCY BYTE 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[8:15]	Byte 1 of frequency word

ADDRESS 2: FREQUENCY BYTE 2

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[16:23]	Byte 2 of frequency word

ADDRESS 3: FREQUENCY BYTE 3

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**FREQ**[24:27]	4 most significant bits of the frequency word
4-7	R/W	-	unused

If the desired tuning frequency is **F**, then the frequency word should be set to:

$$\mathbf{FREQ} = 2^{28}\mathbf{F}/(\text{clock rate})$$

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3.2 SYNC MODE REGISTER

The sync mode register controls the action of the $\overline{\text{SS}}$ and $\overline{\text{AS}}$ sync strobes and how they affect the chip's internal timers, counters, and accumulators.

ADDRESS 4: Sync Mode Register

BIT	TYPE	NAME	DESCRIPTION
0 (LSB)	R/W	SS_OFF	This bit disables the $\overline{\text{SS}}$ input.
1	R/W	AS_ON	Enables the accumulator sync $\overline{\text{AS}}$. Normally the frequency accumulator will free run. This bit causes the frequency accumulator to be initialized to the contents of the frequency register when $\overline{\text{AS}}$ goes low. $\overline{\text{SS}}$, instead of $\overline{\text{AS}}$, will reset the accumulator if AS_MUX is set and $\overline{\text{SS}}$ is not disabled by SS_OFF.
2	R/W	AS_MUX	Use $\overline{\text{SS}}$ for the accumulator sync. The $\overline{\text{AS}}$ input is ignored and the $\overline{\text{SS}}$ strobe is used in its place when this bit is set and $\overline{\text{SS}}$ is not disabled by SS_OFF. (See AS_ON and AS_FREQ).
3	R/W	LD_FREQ	Load the frequency register in the digital oscillator with the contents of the frequency word registers. If left on, this bit will cause the frequency register to load whenever a frequency word register is changed.
4	R/W	AS_FREQ	Enables the synchronous frequency load mode. When this bit is set and $\overline{\text{AS}}$ goes low, the frequency register will be synchronously loaded with the contents of the frequency control registers. $\overline{\text{SS}}$, instead of $\overline{\text{AS}}$, will load the frequency register if AS_MUX is set and $\overline{\text{SS}}$ is not disabled by SS_OFF.
5	R/W	SS_DIAG	Enables diagnostic syncs. This bit routes the internal sync to the checksum generator and to all accumulators and control counters within the chip. This forces the chip to re-initialize at the start of every sync period. The internal sync period will be 2^{20} clocks if SS_MUX is set, otherwise it will be determined by the period of an externally provided $\overline{\text{SS}}$ strobe.
6	R/W	TEST	Shortens the internal sync counter period from 2^{20} clocks to 2^{8} clocks. This mode is used to test chips at the factory.
7 (MSB)	R/W	SS_MUX	Use the sync counter's terminal count strobe for the internal sync instead of the sync input $\overline{\text{SS}}$. The internal sync is output on the $\overline{\text{SO}}$ pin.

The operation of these control bits are illustrated in Figure 3.

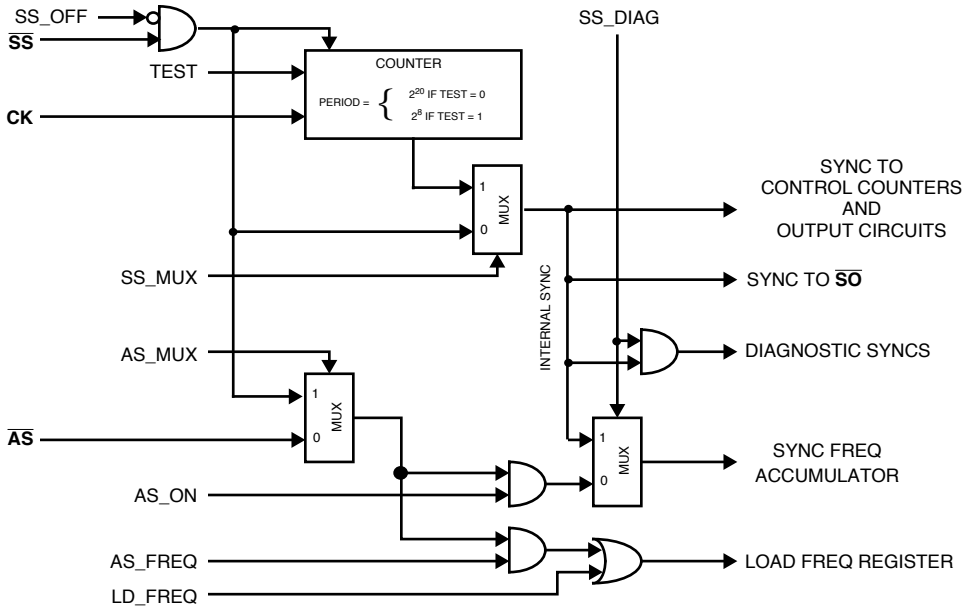


Figure 3. Sync Controls

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3.3 FILTER MODE REGISTER

This register controls filtering, output formatting and the diagnostic input mode.

ADDRESS 5: Filter Mode Register

BIT	TYPE	NAME	DESCRIPTION
0-2	R/W	**DEC[0:2]**	The decimation mode. The output sample rate is set using **DEC** according to the following table: **DEC** — **F_O COMPLEX** (REAL = 0) — **F_O REAL** (REAL = 1) 0 or 1 — F_{CK} — ? 2 — $F_{CK}/2$ — F_{CK} 3 — $F_{CK}/4$ — $F_{CK}/2$ 4 — $F_{CK}/8$ — $F_{CK}/4$ 5 — $F_{CK}/16$ — $F_{CK}/8$ 6 — $F_{CK}/32$ — $F_{CK}/16$ 7 — $F_{CK}/64$ — $F_{CK}/32$ Where F_{CK} is the input rate and F_O is the output rate.
3	R/W	-	Unused.
4	R/W	REAL	Output real samples instead of complex samples. The output spectrum is centered from 0 to $F_O/2$ where F_O is the output rate (see **DEC** above for the REAL mode). NOTE: The FLIP bit described below is active low in the real mode.
5	R/W	OFFSET	Offset the complex output spectrum. Used in the complex output mode (REAL=0) to force the output spectrum to be centered at $F_O/2$, where F_O is the output sample rate (see **DEC** above for the COMPLEX mode). This mode is useful for single-sideband AM signals because it moves the lower band edge up to zero frequency where it belongs. The upper half of the spectrum will appear as negative frequencies.
6	R/W	FLIP	Flip the output spectrum. This bit inverts the output spectrum. In the complex mode the spectrum is flipped about zero. In the real mode the spectrum is flipped about $F_O/4$, where F_O is the real mode's output sample rate. In the complex mode FLIP=1 flips the spectrum. In the real mode FLIP=0 flips the spectrum.
7	R/W	DIAG	Use the diagnostic ramp for the input to the chip instead of the **X** input. The ramp counts from -2048 to +2047 and then starts over again.

The effect on the output spectrum of the REAL, OFFSET and FLIP bits is illustrated in the following diagram. (F_O is the output sample rate)

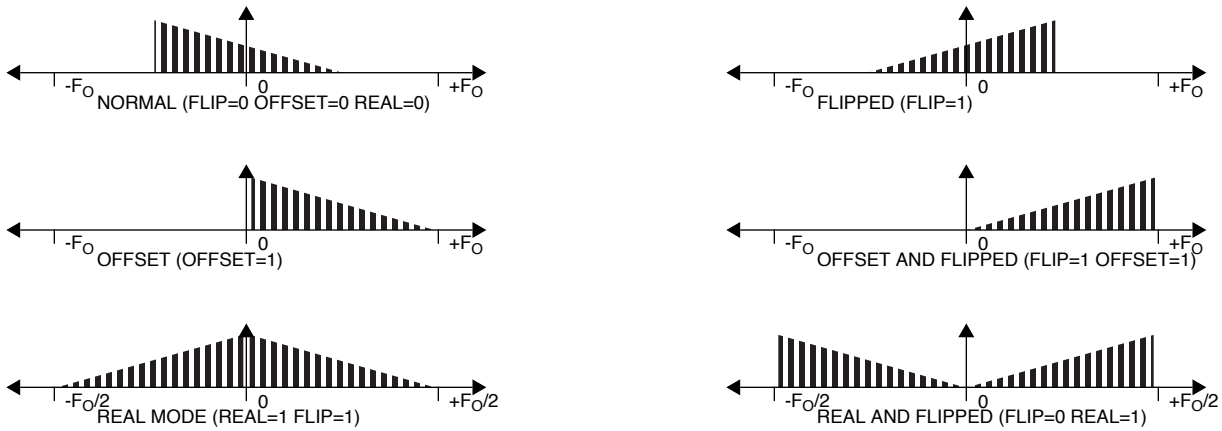


Figure 4. Output Spectral Formats

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3.4 GAIN CONTROL REGISTERS

These registers set the output gain.

ADDRESS 6: Gain Control Register

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**F[0:7]**	The 8 bit gain fraction.

ADDRESS 7: Gain Exponent Register

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**S[0:3]**	The 4 bit gain exponent.
4	R/W	GS_MODE	Turns on the synchronous gain mode. See below.
5	R/W	KA_DISABLE	Provided for testability. Turns off the clock loss detect function in the keepalive circuit. This bit powers up low and should be kept low.
6	R	KA_CK	A read only bit which monitors the 1 KHz (approximate) clock used in the power down mode (See bit 7, address 9, Section 3.6).
7	R	KA_MODE	This bit will read back high if the chip is in the power down mode, either due to the loss of clock, or by setting bit 7 in register 9.

The chip's input to output gain is set using **F** and **S** according to the formula:

$$GAIN = 2^{(\mathbf{S}-\mathbf{B})}(1+\mathbf{F}/256)$$

where **B** is the base gain setting which is a function of the decimation mode of the chip. The unity gain setting (**S**=**B** and **F**=0) means that a 12 bit DC input will show up in the upper 12 bits of the 16 bit output.

The values of **B** are:

DEC	B
0 or 1	6
2	5
3	4
4	3
5	2
6	1
7	0

The GS_MODE control bit determines when new gain settings are applied to the output. New gain settings are double buffered so that they can be synchronized with the output words. If GS_MODE is low, then the gain settings are applied to the output samples immediately after **S** has been loaded. If GS_MODE is high, then the new gain settings are not used until $\overline{\mathbf{GS}}$ goes low.

NOTE: The gain settings must be loaded in the correct order- **F** first and then **S**. The circuit detects new gain settings by sensing when **S** is loaded. this means that **S** must be loaded even if one only wishes to change **F**.

Bits 5, 6, and 7 of this register were unused R/W bits in the original GC1012 chip. Applications using the GC1012A as a GC1012 replacement should ignore these bits when reading address 7.

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3.5 OUTPUT MODE REGISTER

The output mode register controls the output formatting.

ADDRESS 8: Output mode register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	IQ_MUX	The IQ_MUX control is used in the complex mode to multiplex the I and Q output words onto the **I[0:15]** output pins. Normally the I and Q halves are output on separate ports. When this bit is high, the halves are multiplexed together so that the I half is output first, followed by the Q half. The word strobe (**WS**) rate is doubled in this mode. The **IFLAG** output signal is used in this mode to identify the I half of each complex pair. The **Q[0:15]** output pins are forced low in this mode.
1	R/W	WS_POL	Changes the polarity of **WS**.
2	R/W	WS_MODE	Changes the mode of **WS**. Normally **WS** pulses high during the clock cycle before an **I** or **Q** output transition. This bit changes **WS** so that it is a 50% duty cycle clock with its rising edge in the middle of each output period
3	R/W	-	Unused
4	R/W	R10	Round the output samples to the 10 bits MSBs of the output word.
5	R/W	R12	Round the output samples to the 12 bits MSBs of the output word.
6	R/W	R14	Round the output samples to the 14 bits MSBs of the output word.
7	R/W	R16	Round the output samples to the 16 bits MSBs of the output word.

One and only one of the rounding options should be selected. Unused LSBs are cleared.

The IQ_MUX and WS_MODE controls are illustrated in the timing diagrams shown in Figure 5. Note that the polarity shown for **WS** can be changed using the WS_POL control.

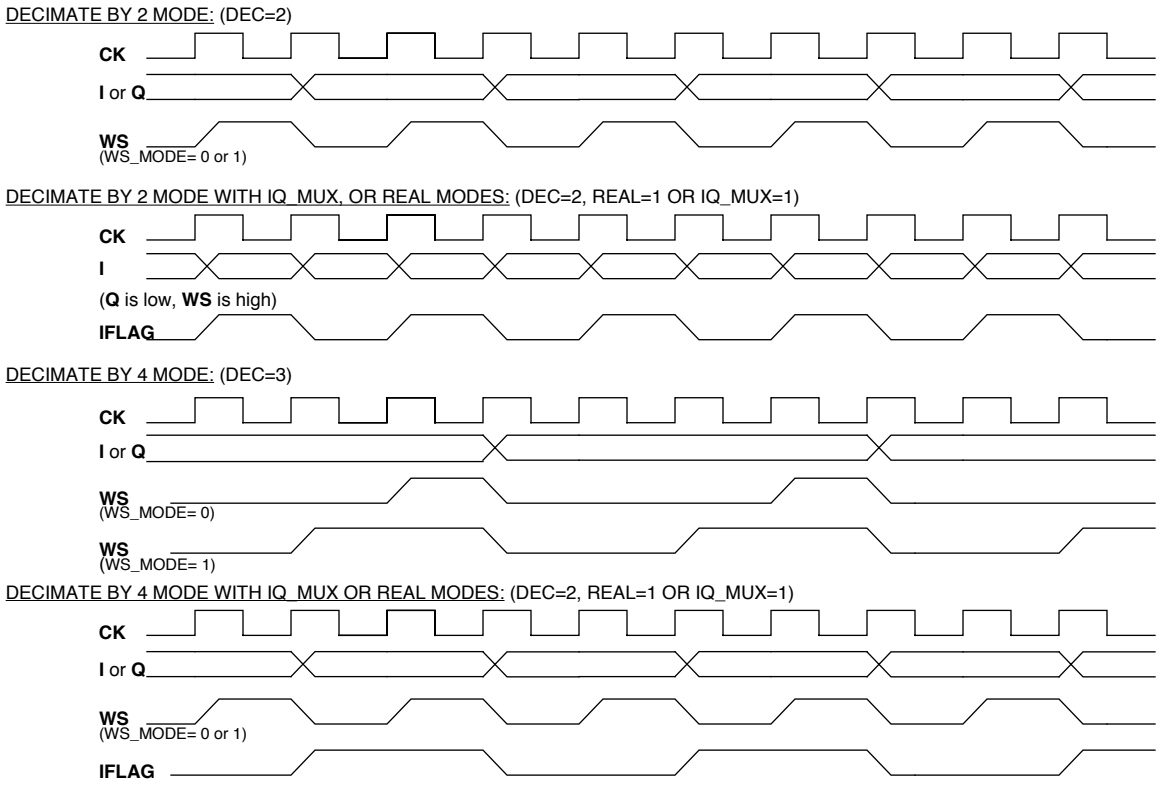


Figure 5. Timing For Output Modes

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3.6 OUTPUT STATUS REGISTER

This register contains flags and status information for the output samples.

ADDRESS 9: Output Status Register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	READY	Tells the chip that the user is ready to capture an output sample. The chip clears this bit when it has captured the sample. See Notes below.
1	R/Clear	MISSED	The chip sets this bit high if a new output sample was ready but the user had not set READY high. This lets the user know if a sample has been missed. This bit is cleared by writing a 0 to the bit. Attempting to write a 1 to this bit does nothing.
2	R/W	INT_ENABLE	This bit is used to turn on the interrupt output. If this bit is off the **$\overline{\text{INT}}$** output pin is forced high. When this bit is high the **$\overline{\text{INT}}$** output pin is equal to READY. When READY goes low, meaning that a new sample has been captured, the **$\overline{\text{INT}}$** pin will go low. If **$\overline{\text{INT}}$** is tied to a processor's interrupt input, then the processor will be interrupted whenever a new sample is ready.
3	R/W	-	Unused
4	R/W	OFLOW_MODE	This bit sets the mode of the **$\overline{\text{OFLOW}}$** output. When OFLOW_MODE is low the **$\overline{\text{OFLOW}}$** output is an inverted version of OVERFLOW (see bit 6 below). If OFLOW_MODE and OFLOW_ENABLE are high, then the **$\overline{\text{OFLOW}}$** output pulses low for one clock cycle each time there is an overflow.
5	R/W	OFLOW_ENABLE	This bit enables the overflow modes. If this bit is low, then OVERFLOW (see bit 6 below) will not be set and the **$\overline{\text{OFLOW}}$** output will not go low. This bit does not affect the overflow detection and saturation logic in the gain circuit.
6	R/Clear	OVERFLOW	The chip sets this bit when an overflow occurs and OFLOW_ENABLE is turned on. This bit can be used to indicate if the gain is set too high. This bit stays high until the user clears it. The bit is cleared by writing a 0 to it. Attempting to write a 1 to this bit does nothing.
7	R/W	POWER_DOWN	This bit is used to put the chip into a power down (standby) mode. In this mode the internal clock rate is reduced to approximately 1 KHz. All control register settings are preserved, but the output data will be invalid.

The READY signal is used to capture output samples and to read them into an external processor. The user captures outputs by setting the READY bit and then waiting for the bit to be cleared by the chip. When the bit goes low the processor can read the samples out of the I and Q output registers described in section 3.9. The processor can wait for READY to go low by either continuously reading this register, or it can use the interrupt output **$\overline{\text{INT}}$** to tell it when the sample is ready. To use the interrupt output mode the user must tie the **$\overline{\text{INT}}$** output pin from the chip to an interrupt input of the processor. The processor can then capture samples by setting READY and then setting INT_ENABLE (INT_ENABLE should be set after READY in order to avoid a spurious interrupt due to the interrupt being enabled before READY has settled to its high state). The processor will be interrupted when READY goes low again. When it is interrupted the processor can turn off INT_ENABLE, read the I/Q outputs, and then start over again.

The MISSED flag is provided to let the processor know if it has taken too long to read the I/Q samples before rearming the READY bit. If the processor wants to use the MISSED flag it should clear the flag the first time it sets the READY bit and then check it after setting the READY bit thereafter. The READY bit is set and the MISSED bit cleared by writing a 01(hex) to this register. The READY bit is set and the MISSED bit is left alone by writing a 03(hex) to this register.

NOTE: The READY bit will not be cleared if the sample is captured while the user is setting the READY bit. This will cause the READY bit to stay high after the output is captured and will not allow the chip to capture any more samples until the bit is cleared and set again. The user can detect this incorrect "ready" state by always clearing the MISSED bit when setting the READY bit. The incorrect state is detected if MISSED goes high when READY is high. The work-around to guarantee capturing an output sample is to always clear READY before setting it.

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3.7 ONE SHOT ADDRESS

The one shot pulse is generated on the **$\overline{OS}$** pin by writing to address 10. This is a write-only address and the data written to it is irrelevant.

ADDRESS 10: ONE SHOT

3.8 CHECKSUM REGISTER

This read-only register stores the checksums generated in the diagnostic mode.

ADDRESS 11: CHECKSUM

BIT	TYPE	NAME	DESCRIPTION
0-7	R	CHECK[0:7]	The 8 bit checksum. The checksum is generated as a non-linear feedback accumulation of the **BS**, **FS**, **I**, and **Q** output bits. The current checksum is stored in this register and the checksum generator is cleared whenever the internal sync goes low (see SS_MUX in Section 3.2 for the modes of the internal sync).

3.9 I AND Q OUTPUT REGISTERS

These registers are used to capture output samples.

ADDRESS 12: I-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[0:7]**	Least significant 8 bits of the **I** output.

ADDRESS 13: I-Output Byte 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[8:15]**	Most significant 8 bits of the **I** output.

ADDRESS 14: Q-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**Q[0:7]**	Least significant 8 bits of the **Q** output.

ADDRESS 15: Q-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**QI[8:15]**	Most significant 8 bits of the **Q** output.

The user reads the **I** and **Q** outputs through these read-only registers. The captured samples can be used for gain control, analysis, display, or diagnostics.

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4.0 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Table 1: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	7	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.7	V_{CC}+0.7	V	
Storage Temperature	T_{STG}	-65	150	°C	
Lead Soldering Temperature (10 seconds)			300	°C	
Clock Rate	F_{CK}	1		KHz	1

Notes:

1. Below 1 KHz the keepalive circuit will power down the chip. If the keepalive circuit is disabled (bit 5, address 7) and the clock is stopped, he chip will draw up to one Amp of power supply current for approximately 10 seconds. After 10 seconds the current will go down to below 50 mAmps.

4.2 RECOMMENDED OPERATING CONDITIONS

Table 2: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	3.0	5.5	V	
Temperature Ambient, no air flow	T_A	-40	+85	°C	1
Junction Temperature	T_J		140	°C	1

Notes:

1. Thermal management is required to keep T_J below MAX for full rate operation. See Table 3 below.

4.3 THERMAL CHARACTERISTICS

Table 3: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	GC1012A-CQ			GC1012A-PQ			UNITS
		2 Watts	4 Watts	6 Watts	2 Watts	4 Watts	6 Watts	
Theta Junction to Ambient	θja	29	16	15	18	11	10	°C/W
Theta Junction to Case	θjc	8	7	6	4	4	4	°C/W

Note: Air flow will reduce θ**ja** and is highly recommended.

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4.4 DC CHARACTERISTICS

All parameters are industrial temperature range of -40 to 85 ^{o}C ambient unless noted.:

Table 4: DC Operating Conditions

PARAMETER	SYMBOL	Vcc = 3.3V		Vcc = 5 V		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Voltage input low	V_{IL}		0.8		0.8	V	1
Voltage input high	V_{IH}	2.0		2.5		V	2
Input current (V_{IN} = 0V)	I_{IN}	Typical +/- 50				uA	2
Voltage output low (I_{OL} = 4mA)	V_{OL}		0.5		0.5	V	2
Voltage output high (I_{OH} = -4mA)	V_{OH}	2.4	3.3	3.0	5	V	2
Data input capacitance (All inputs except **CK** and **C[0:15]**)	C_{IN}	Typical 4				pF	1
Clock input capacitance (**CK** input)	C_{CK}	Typical 10				pF	1
Control data capacitance (**C[0:15]** I/O pins)	C_{CON}	Typical 6				pF	1

Notes:

1. Controlled by design and process and not directly tested. Verified on initial parts evaluation.
2. Each part is tested at 85^{o}C for the given specification.

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4.5 AC CHARACTERISTICS

Table 5: AC Characteristics (-40 TO +85°C Ambient, unless noted)

PARAMETER	SYMBOL	3.3V +/- 5%		5 V +/- 5%		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Clock Frequency	F_{CK}	0.01	45	0.01	80	MHz	2, 3, 4
Clock low period (Below V_{IL})	t_{CKL}	8		5		ns	1
Clock high period (Above V_{IH})	t_{CKH}	8		5		ns	1
Data setup before **CK** goes high (**X, SS, AS** or **GS**)	t_{SU}	4		2		ns	1
Data hold time after **CK** goes high	t_{HD}	0		0		ns	1
Data output delay from rising edge of **CK**. (**I, Q, WS, IFLAG, OS, OFLOW, SO**	t_{DLY}	2	13	2	9	ns	1, 5
Data to tristate delay (**I** or **Q** to hiZ from **OEI** or **OEQ**)	t_{DZ}	2	5	2	5		1
Tristate to data output delay (**I** or **Q** valid from **OEI** or **OEQ**)	t_{ZD}	3	13	3	9	ns	1, 5
Control Setup before **CS** goes low (**A**, **R/W** during read, and **A**, **R/W**, **C** during write)	t_{CSU}	10		10		ns	1
Control hold after **CS** goes high (**A**, **R/W** during read, and **A**, **R/W**, **C** during write)	t_{CHD}	10		10		ns	1
Control strobe (**CS**) pulse width (Write operation)	t_{CSPW}	60		30		ns	1,6
Control output delay **CS** low to **C** (Read Operation)	t_{CDLY}		120		90	ns	1,6
Control tristate delay after **CS** goes high	t_{CZ}		20		10	ns	1
Quiescent supply current (V_{IN}=0 or V_{CC}, F_{CK} = 1KHz)	I_{CCQ}		200		200	uA	1
Supply current (F_{CK} =45MHz)	I_{CC}		386		585	mA	1, 7

Notes:

1. Controlled by design and process and not directly tested. Verified on initial part evaluation.
2. Each part is tested at 25 deg C for the given specification.
3. Temperature range is verified by lot sampling.
4. The chip may not operate properly at clock frequencies below MIN and MAX.
5. Capacitive output load is 20pf. Delays are measured from the rising edge of the clock to the output level rising above V_{IH} or Falling below V_{IL}.
6. Capacitive output load is 80pf.
7. Current changes linearly with voltage and clock speed. Icc (MAX) $= \left(\frac{VCC}{5}\right)\left(\frac{F_{CK}}{45M}\right) 585\text{mA}$

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5.0 APPLICATION NOTES

5.1 POWER AND GROUND CONNECTIONS

The GC1012A chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC} and GND pins. If possible the GC1012A chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 and 0.1 μf) adjacent to each GC1012A chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors adjacent to each V_{CC} and GND pair.

IMPORTANT

The GC1012A chip may not operate properly if these power and ground guidelines are violated.

5.2 STATIC SENSITIVE DEVICE

The GC1012A chip is fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments.

5.3 80 MHZ OPERATION

Care must be taken in generating the clock when operating the GC1012A chip at its full 80 MHz clock rate. The user must insure that the clock is above 2 volts for at least 5 nanoseconds and is below 1 volt for at least 5 nanoseconds. At 80 MHz the clock period is only 12.5 nanoseconds so that the clock must have a duty cycle of exactly 50%, and the rise and fall times can only be 1.25 nanoseconds each. One must also be careful to prevent clock undershoot below ground. An ideal clock at 80 MHz would be a square wave with a low voltage of 0.5 volts and a high voltage of 2.5 volts.

5.4 REDUCED VOLTAGE OPERATION

The power consumed by the GC1012A chip can be greatly reduced by operating the chip at the lowest V_{CC} voltage which will meet the application's timing requirements. When operating at a reduced voltage, GRAYCHIP recommends driving the GC1012A chip inputs with 5 volt to 3 volt interface chips.

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5.5 SYNCHRONIZING MULTIPLE GC1012A CHIPS

A system containing a bank of GC1012A chips will need to be synchronized so that the output frames from each chip are aligned, and, if desired, so that their frequency accumulators are running synchronously. The GC1000 Input Switch chip has built in sync counters which are designed specifically for this purpose. If the GC1000 chip is not used, then the one-shot strobe (see Section 3.7) can be used. The bank of chips should be interconnected so that the **$\overline{\text{OS}}$** pin of one GC1012A chip is tied to the **$\overline{\text{SS}}$** input of all of the chips. The one-shot strobe mode can then be used to simultaneously synchronize all of the chips. The **$\overline{\text{OS}}$** pin of a second GC1012A chip should be tied to the **$\overline{\text{AS}}$** input of all of the chips. The one-shot mode of the second chip can be used to synchronize the frequency accumulators whenever the tuning frequency has been changed.

5.6 PROCESSING COMPLEX DATA

Two GC1012A chips can be used to process complex input data by using one chip to process the I-input data and the other to process the Q-input data. If the two chips are synchronized as discussed above, then the complex output stream can be reconstructed by adding and subtracting the I and Q outputs of the two chips. A programmable gate array chip such as from XILINX would be ideal for this post-processing. The configuration for processing complex data is illustrated in Figure 6.

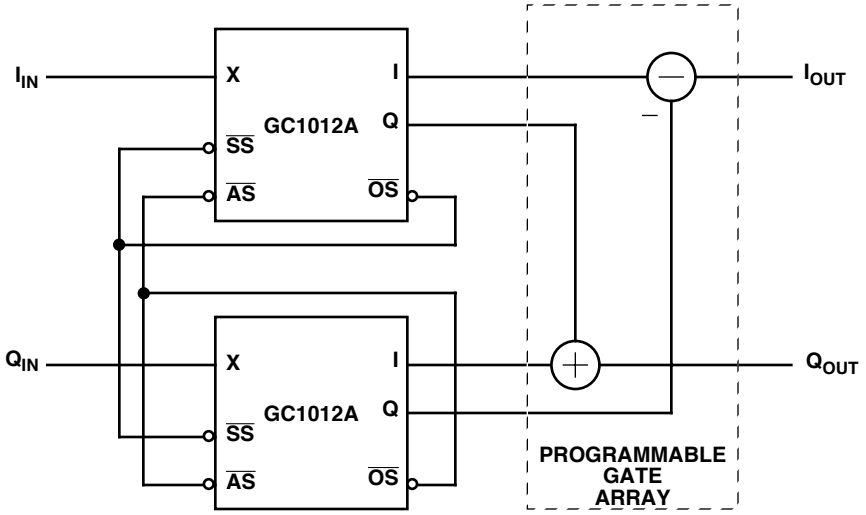


Figure 6. Processing Complex Input Data

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5.7 EXAMPLE RECEIVER ARCHITECTURE

An example digital receiver architecture using the GC1012A chip is shown in Figure 7.

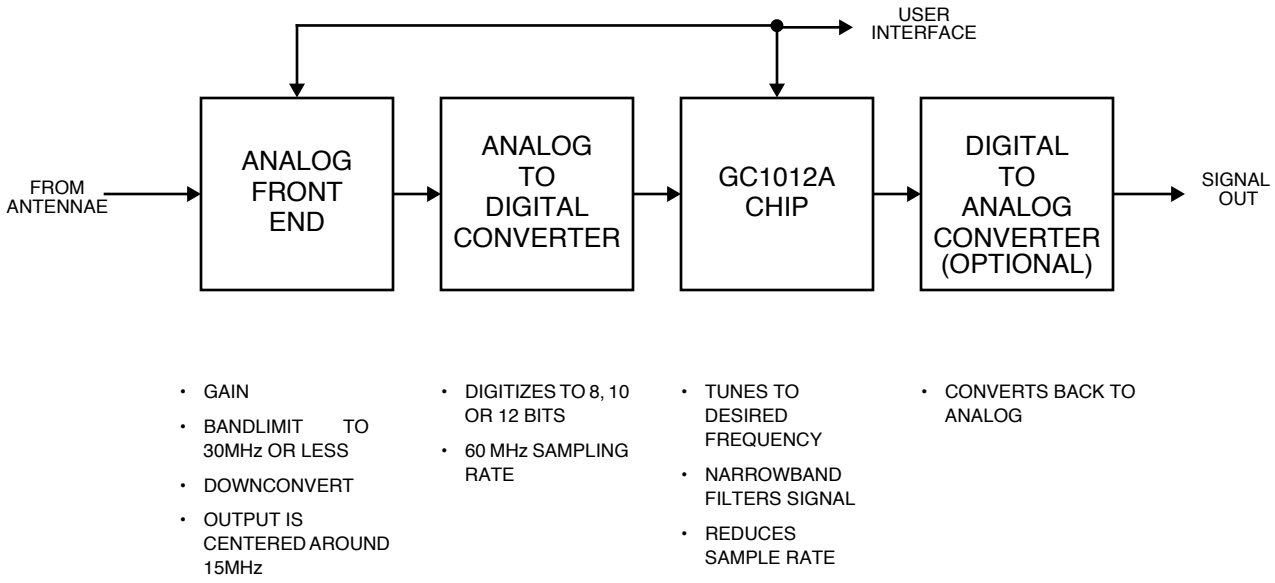


Figure 7. Example Digital Receiver Architecture

The receiver contains an analog front end which downconverts up to 30MHz of radio spectrum to an IF frequency around 15MHz[1]. It also adjusts the gain of the signal so that it fills the dynamic range of the analog to digital converter (ADC). The ADC digitizes the signal using up to 12 bits of resolution at a sampling rate up to 60 MHZ. The GC1012A chip tunes, downconverts, and narrowband filters desired frequencies from within the 30 MHz band. The GC1012A output can either be converted back to analog or kept in its digital state for subsequent signal processing.

1. Note that the HF spectrum (1 to 30MHz) can be digitized directly.

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5.8 LATENCY THROUGH THE GC1012A

Two latencies are of interest, the latency from a step function in to a step function out (midpoint), and the latency from a step function until the end of the “ringing” in the step function output (endpoint). These latencies are:

Table 6: Latency

Output Mode	Midpoint	Endpoint	Values of D (decimation)
Real	41 + 20D	41 + 40D	1, 2, 4, 8, 16 and 32
Complex	35 + 10D	35 + 20D	2, 4, 8, 16, 32 and 64

Another latency of interest is the delay from SS input to stable WS. The WS strobe becomes stable and is low after 9 clocks, before 9 clocks the WS is unknown and may go high at any time. The delay until the first valid high WS is a function of decimation. For decimate by 2 the delay from SS is 10 clocks, for 4 the delay is 12 clocks, for 8 the delay is 16 clocks and for decimation ratios of 16, 32 and 64 the delay is 24 clocks. WS is high at clock 24 for all decimations.

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