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OPERATING MANUAL

MODEL 4275B

32 Channel, 100 kHz, 16-bit
Sigma-Delta A/D Converter
MIX Module for VMEbus Systems

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Pentek Model 4275B Operating Manual Revision History

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Chapter 1: General Description

1.1 Introduction

The Model 4275B is a 32-channel A/D converter MIX module compatible with Pentek's extensive line of data acquisition and DSP products for VMEbus. It features 32 individual sigma-delta A/D converters, each providing 16 bits of resolution and sampling rates up to 100 kHz. This device can be attached to any of Pentek's MIX baseboards, which provide a range of DSP functions and VMEbus interfaces including VME slave, VME master, and VSB master interfaces. DSP functions can be provided by baseboards containing TMS320C30 or TMS320C40 processors. Up to three Model 4275B's can be attached to any baseboard, and any of Pentek's numerous other MIX modules may be included to provide additional interfaces and DSP resources.

This chapter of the Operating Manual briefly describes the features of the Model 4275B, and then presents a list of specifications and a functional block diagram. Chapter 2 provides information on the setup and installation procedures for the unit. Chapter 3 gives detailed operating information, including the unit's memory map and bitwise definitions of the control and status registers and Chapter 4 describes procedures to be followed when writing programs to control the operation of this device.

Appendix A contains 'C' language source code examples demonstrating the use of this device on any of Pentek's MIX baseboards. Pentek's Mix Tutorial for VMEbus Systems, Manual Part number 800.00001 provides information on the MIX technology employed in our extensive family of DSP and data acquisition products. New users of Pentek products may wish to read this information before proceeding to the installation and operation sections of this manual, as terminology used throughout the manual is explained in these tutorials.

1.2 MIX Module Operation

The Model 4275B attaches to any of Pentek's MIX Baseboards, using standard MIX connectors, and occupies its own single slot in the VME card cage. In these MIX subsystems, the unit's resources are directly mapped to MIX bus address space.

1.3 Input Amplifiers

Each of the 32 inputs is buffered by an amplifier stage providing a ±5.0 V full scale input voltage range (other ranges are optionally available; contact Pentek for further information). Front panel multi-pin connectors provide a convenient method for attaching signal inputs via flat ribbon cable or discrete wiring harnesses. Differential inputs can be accommodated by the Model 4275B when equipped with Option 007.

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1.4 Digital Filters and Analog to Digital Converters

Following the amplifier section are 32 A/D converters, one for each input signal. These converters utilize sigma-delta technology, and incorporate a powerful digital filtering scheme. This architecture eliminates the need for front-end sample and hold circuitry. Signal-to-noise performance of these converters is 103 dB with peak spurious components less than 100 dB below full scale for signal bandwidths up to 45 kHz.

The digital filtering section performs the anti-aliasing functions, thereby eliminating the need for separate, external low pass pre-filters in most applications. Another major benefit is the linear phase response of these filters, very useful for processing multi-sensor array signals such as those found in sonar applications. The cutoff frequency of the filters tracks the sampling rate at a constant ratio of 0.45.

1.5 Specifications

Input Channels

Quantity:	32
Input Type:	
Standard Unit:	Single-ended
Option 007:	Differential
Input Impedance:	
Standard Unit:	10kΩ
Option 007:	
Each Input to Ground:	100 kΩ
Each Input to its Complement:	200 kΩ
Full Scale Voltage	± 5.0 volts (differential for option 007)
Frequency Response:	± 0.1 dB, DC to 50 kHz
Common Mode Rejection:	> 40 dB, DC to 10 kHz (applies to Option 007 only)

Input Filters

Type:	Digital, Low-pass
Cutoff Frequency:	0.4535 x Sampling Frequency
Stopband:	–110 dB @ 0.54 x Sampling Frequency
Passband Ripple:	±0.003 dB
Group Delay:	38.8 sample periods
Group Delay Variance:	0 µs

A/D Converters

Quantity:	32
Type:	AKM AK5393
Conversion Method:	Sigma-delta
Resolution:	16 bits
Sample Rate:	100 kHz max.
High Pass Filter:	2.08 Hz @ 100 kHz

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1.5 **Specifications** (continued)

Overall Distortion

Signal-to-Noise Ratio:	88 dB (minimum) > 90 dB (typical)
Harmonic & IM Components:	–85 dB (minimum) > 90 dB (typical)

Multiplexer & Multiplexer Control

Active Channels:	1 through N, with N programmable from 1 to 32

Sampling Rate Control

Internal Sample Clock:	16 frequencies, from 100 kHz to 6.25 kHz, programmable with a 4-bit binary word. Sample Rate = 25.6 MHz ÷ (128 x D), where D is programmed divider, and D ≥ 2
External Sample Clock:	TTL input levels, via front panel BNC connector. Sample Rate = Clock Frequency ÷ (128 x D), where D is programmed divider, and D ≥ 2
FIFO Memory:	16k samples x 32 bits (Two 16-bit samples available at each read)

A/D Output Coding

Format:	16-bit, 2's complement
Coding (16-bit):	
+Full Scale:	0x7FFF
Zero:	0x0000
- Full Scale:	0x8000

MIX Interface

FIFO Output Modes

Non-Packed Mode:	One 16-bit sample in each 32-bit MIX bus transfer in sequential order by channel.
Time Packed Mode:	One pair of sequential 16-bit samples from the same channel, packed in each 32-bit MIX bus transfer.
Channel Packed Mode:	One 16-bit sample from one channel and one 16-bit sample from the next channel packed in each 32-bit MIX bus transfer.
MIX Transfer Speed:	250 nsec / 32 bit longword transfer
Control Register:	Control bits for start/stop, interrupt mask for FIFO full, half-full, & empty, internal/external clock select, sample generator frequency
Status Register:	Status bits for FIFO full, half-full, & empty, framing bit, interrupt status, active channel numbers and FIFO ordering sequence

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1.5 Specifications (continued)

Input Connectors

External Clock Input:	One BNC female on front panel, Input Frequency may be delivered directly or divided by at least 256
Analog Inputs:	Two female DB-37 connectors, 16 channels per connector, on front panel

Power (from MIX baseboard)

+5 V DC	3.0 A max.
+12 V DC	0.5 A max.
- 12 V DC	0.5 A max.

Dimensions	Each module occupies one VMEbus slot position and has its own front panel.
Height:	10.3"
Depth:	4.0"
Width (including panel):	0.8"

1.6 Block Diagram

The block diagram of the Pentek Model 4275B, 32 Channel, 100 kHz, 16-bit, Sigma-Delta A/D Converter MIX Module for VMEbus Systems is presented below.

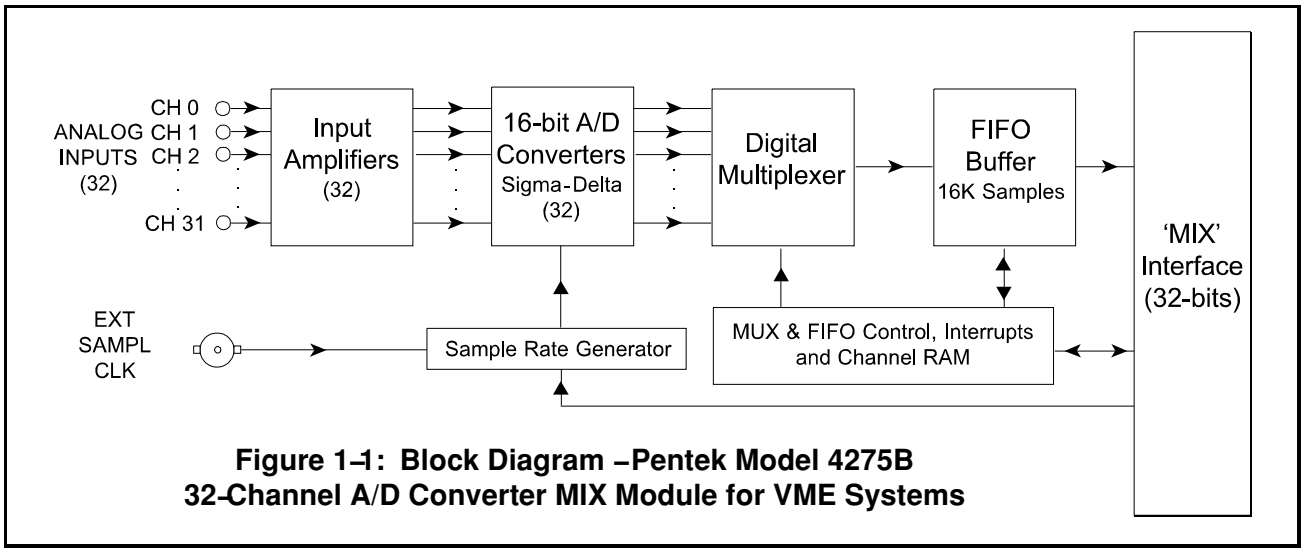


Figure 1-1: Block Diagram –Pentek Model 4275B 32-Channel A/D Converter MIX Module for VME Systems

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If you discover any damage, please contact Pentek immediately, at (201) 818-5900. Please save the original shipping container and packing material, in case reshipment is required.

2.2 Jumper Settings

The subsections below describe the parameters that are programmed by the placement or removal of shorting jumpers on the Model 4275B.

2.2.1 Jumper Block Locations

On the following page is a drawing of the Model 4275B MIX board, showing the locations of the jumper blocks referred to in the sections below. The MIX board contains 16 of the 4275B's 32 A/D channels. The other 16 channels are contained on the Mezzanine board, shown for reference purposes on Page 13. There are no jumper blocks on the Mezzanine board, and the boards do not need to be separated in order to configure the jumpers on the MIX board.

There are only two jumper blocks on the Model 4275B's MIX board, and they are both of the 3-pin, single-in-line variety. For both blocks, if the board is positioned component side up, with the front panel facing you, pin 1 will be on your left.

2.2.2 **Frequency Divider Input Select Jumper** - Jumper Block JP1

The sigma-delta A/D converter used in the Model 4275B synthesizes its sample rate from a clock signal 128 times higher than the desired rate. This clock signal may be derived from one of two sources: division of the internal 25.6 MHz crystal oscillator, or the front panel SAMP CLK connector. To achieve sample rates of 100 kHz or less, the crystal oscillator frequency must be divided by at least 2 before it is delivered to the ADC. The SAMP CLK signal may also need to be divided before delivery to the ADC. The selection of the input signal to the Model 4275B's frequency divider circuit is accomplished by setting a jumper on jumper block JP1.

If the jumper on JP1 is placed between pins 1 and 2, then the internal crystal oscillator clocks the frequency divider circuit (this is the factory default setting). If the jumper on JP1 is placed between pins 2 and 3, then the signal applied to the front panel SAMP CLK connector clocks the divider. Note that the SAMP CLK connector must be configured as an input if this operating mode is desired. See Section 2.2.3 for more details.

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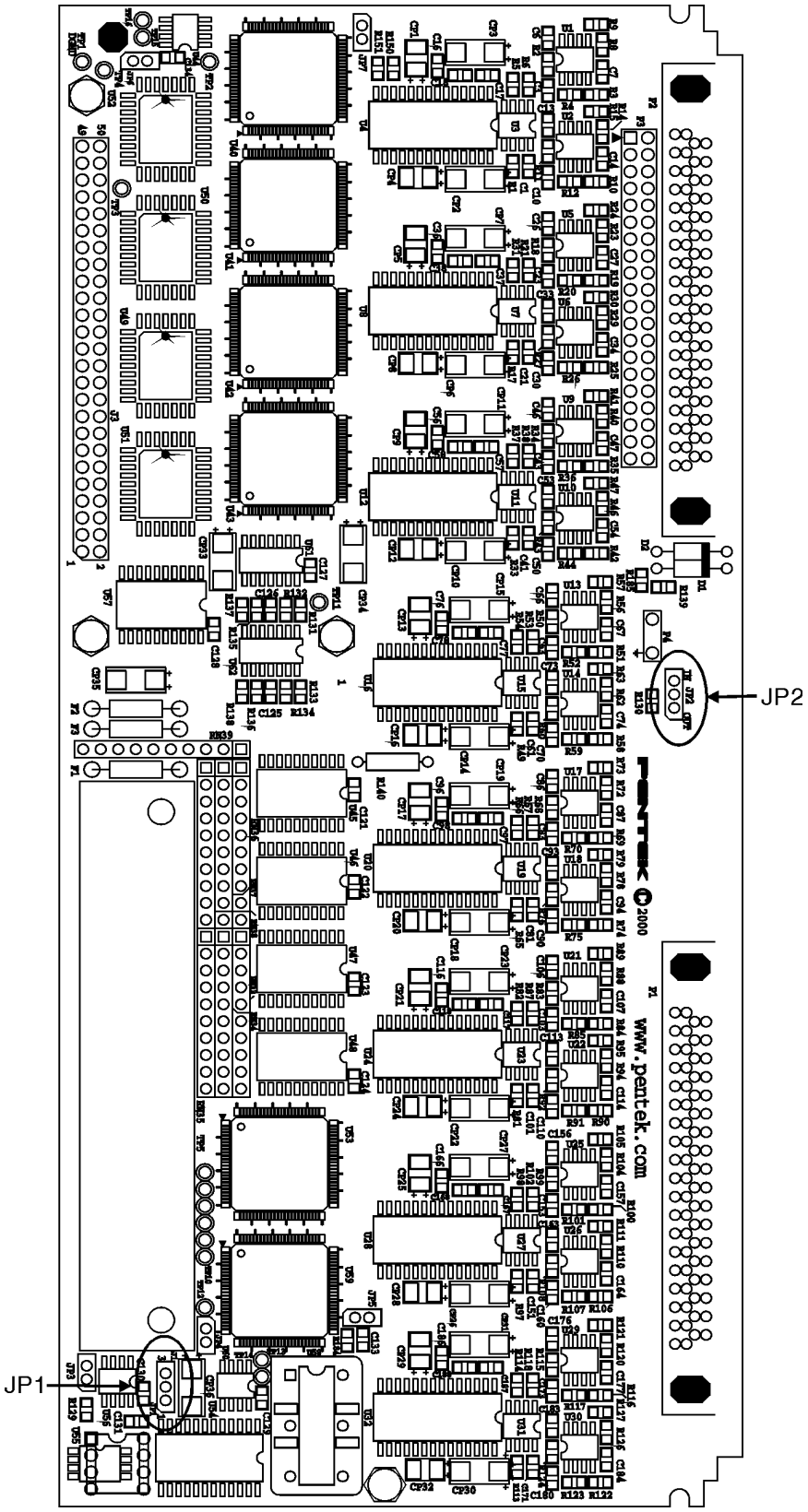


Figure 2-1: Model 4275B MIX Board Drawing Showing Jumper Block Locations

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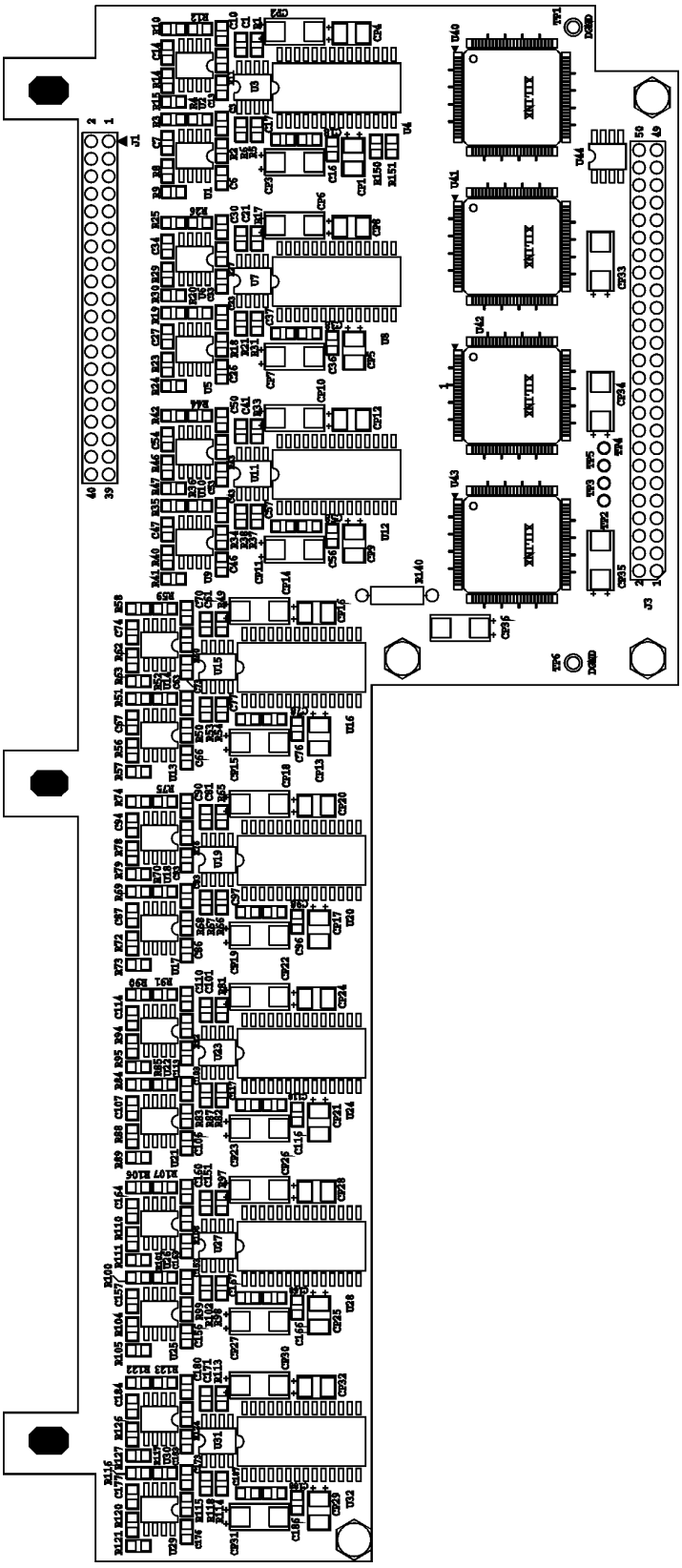


Figure 2-2: Model 4275B Mezzanine Board Drawing

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2.2 Jumper Settings (continued)

2.2.2 Frequency Divider Input Select Jumper - Jumper Block JP1 (continued)

Table 2-1, below, summarizes the settings for jumper block JP1.

Table 2-1: Model 4275B –Jumper Block JP1 –Frequency Divider Clock Selection

Jumper Position	Divider Clock Source
Pins 1 –2*	Internal Oscillator
Pins 2 –3	SAMP CLK Connector
* –Factory Default Setting	

2.2.3 SAMP CLK In/Out Jumper - Jumper Block JP2

The BNC connector on the Model 4275B's front panel, labeled SAMP CLK, can be configured as either a sample clock input or a sample clock output. This is dependent upon the position of the jumper on jumper block JP2.

A jumper installed between pins 1 and 2 of JP2 configures the SAMP CLK connector as an output. This is the factory setting of this jumper block. If you wish to use the SAMP CLK connector as a sample clock input, place the jumper between pins 2 and 3 of JP2.

Table 2-2, below, summarizes the settings for jumper block JP2.

Table 2-2: Model 4275B –SAMP CLK Connector Configuration –Jumper Block JP2

Jumper Position	SAMP CLK Connector
Pins 1 –2*	Sample Clock Out
Pins 2 –3	Sample Clock In
* –Factory Default Setting	

2.2.4 Other Jumper Blocks

Jumper blocks that are not discussed in the sections above are present on the boards for testing and configuration purposes, and should not be tampered with by anyone other than factory-trained, Pentek personnel. If you suspect that some of these jumper blocks have been re-configured, please contact Pentek at (201) 818-5900.

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2.3 Model 4275B Front Panel

The Model 4275B's front panel features two DB-37 connectors, each of which delivers 16 analog inputs to the device. Also on the front panel is the SAMP CLK BNC connector, which may be configured as either an input or an output (see Section 2.2.3, and Table 2-2). A sketch of the panel is shown in Figure 2-3, at the right.

2.3.1 Analog Input Connectors

The connectors that mate with the DB-37 analog input connectors on the Model 4275B are from ITT-Cannon, Model DCM-37PK87 or an equivalent. The ITT-Cannon part number for this connector's hood is DC121073-152, and their part number for the thumbscrews is 250-8501-013. Two of these connectors are included with your Model 4275B, along with two hoods and four thumbscrews.

The pin numbering scheme is shown to the left of the upper connector in Figure 2-3. Table 2-3 (next page, top left) tells which pin on which of the analog input connectors drives which channel's input amplifier in the standard (i.e., single-ended) Model 4275B. All pins not mentioned in the table are grounded in the single-ended configuration.

For units equipped with differential inputs (Option 007), the same connector and pin numbering scheme is used. In these units, the pins that carried the input signals for the single-ended unit carry the – (inverting) input, and the adjacent pins carry the + (non-inverting) input. The pinout for differential input units is shown in Table 2-4, on the next page, top right. Figure 2-4, below, shows how the standard and differential input units respond to input signals.

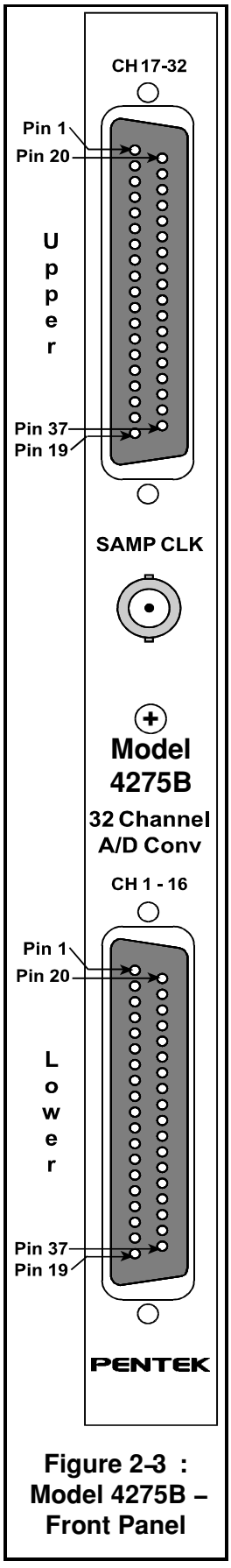
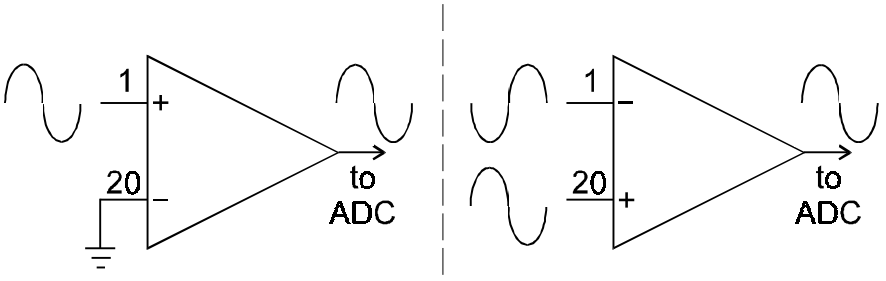


Figure 2-3 : Model 4275B – Front Panel



(a) Single-Ended Input (b) Differential Input

Figure 2-4: Model 4275B –Input Signal Polarity
(Pin numbers for Channel 1 shown)

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2.3 Model 4275B Front Panel (continued)

2.3.1 Analog Input Connectors (continued)

Table 2-3: Analog Input Connector Pinouts – Single Ended Inputs

Channel		Pin #
Lower Connector	Upper Connector	
1	17	1
2	18	2
3	19	3
4	20	4
5	21	5
6	22	6
7	23	7
8	24	8
9	25	12
10	26	13
11	27	14
12	28	15
13	29	16
14	30	17
15	31	18
16	32	19
Pins 9 - 11 and 20 - 37 are grounded on both connectors.		

Table 2-4: Model 4275B, Option 007 – Differential Analog Input Connector Pinouts

Lower Connector			Upper Connector		
Channel	- Input	+ Input	Channel	- Input	+ Input
1	1	20	17	1	20
2	2	21	18	2	21
3	3	22	19	3	22
4	4	23	20	4	23
5	5	24	21	5	24
6	6	25	22	6	25
7	7	26	23	7	26
8	8	27	24	8	27
9	12	30	25	12	30
10	13	31	26	13	31
11	14	32	27	14	32
12	15	33	28	15	33
13	16	34	29	16	34
14	17	35	30	17	35
15	18	36	31	18	36
16	19	37	32	19	37
Pins 9, 10, 11, 28, and 29 are connected to ground on both connectors.					

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2.3 Model 4275B Front Panel (continued)

2.3.2 SAMP CLK Connector

The BNC connector on the Model 4275B's front panel, labeled SAMP CLK, can be configured as either an input or an output for the ADC clock signal. The configuration jumper is described in Section 2.2.3 and in Table 2-2. Depending upon jumper placement and register settings, the frequency of the clock signal delivered to the A/D converter may either be equal to the frequency of the signal at this connector, or some sub-multiple of this frequency. See Sections 3.3.1.3, 3.3.1.4, 4.2 and 4.4 for more detailed information on sample rate programming.



NOTE

The Sample Rate is always equal to the Clock Frequency divided by 128.

If you are using this connector as an input, the signal applied should ideally be a TTL-level square wave. If you program the Control Register such that the signal applied here bypasses the clock divider (see Section 3.3.1.4), then the duty cycle of the signal applied to this connector MUST be between 47.5% and 52.5% for proper operation of the A/D converter. To avoid damage to the Model 4275B's internal circuitry, the signal applied to this connector must never be more positive than +9 V_{DC}, or more negative than -4 V_{DC}.

2.4 Installing the MIX Module on a MIX Baseboard

For MIX module installation instructions, see Pentek's Mix Tutorial for VMEbus Systems, Manual Part number 800.00001.

2.5 Installing the Assembly in the VMEbus Card Cage

Pentek's Mix Tutorial for VMEbus Systems, Manual Part number 800.00001 covers the installation of the assembled MIX stack in the VME card cage.

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Chapter 3: Memory Maps and Register Descriptions

3.1 Programming Overview

The following sections cover access to the Model 4275B from the MIX Baseboard and the issuing of commands for module control and data transfers. There are two cases to be considered, dependent upon the type of Baseboard used. This chapter gives details for Baseboards that use direct MIX addressing, such as Pentek's Models 4200, 4200A, 4201, 4201A, 4202, 4284 and 4285. General information on the use of these Baseboards is given in Pentek's Mix Tutorial for VME-bus Systems, Manual Part number 800.00001. The Mix Tutorial gives general information on access to MIX modules from Baseboards that use an Address Page Register, such as Pentek's Model 4283. A Memory Map for use with the Model 4283 is also included in this chapter.

3.2 Address Maps

The Model 4275B operates only as a MIX bus slave. The sections below will present address maps for the resources available on the Model 4275B, for each type of MIX Baseboard available from Pentek. Each of the slave resources will be assigned a symbolic name, by which that resource will be referred to in subsequent sections of the manual. There are five cases to consider, each of which is covered in a separate section.

If the Baseboard you will be using is a Model 4200, 4200A, 4201 or 4201A, use the address map presented in Section 3.2.1. If you will be using your Model 4275B with a Model 4202 Baseboard, use the address map in Section 3.2.2. If the Model 4283 will be the MIX Baseboard for your Model 4275B, skip to Section 3.2.3, and use the address map found there. If your Model 4275B will be mounted on a Model 4284 Baseboard, use the address map in Section 3.2.4. Finally, if the Model 4285 is the baseboard that will control your MIX modules, refer to the address map in Section 3.2.5.

By convention, the MIX addresses given in this manual are generally given as 8-digit hexadecimal codes, with a space between the first and second four digits, simply for notational convenience. The form is MIX_base+0xYYYY ZZZZ. The leading '0x' is common notation for a hex value in the 'C' programming language.

Since each hex digit represents 4 bits, the 8-digit MIX address represents 32 bits of address. The MIX_base part of the address is dependent upon the Baseboard in use, and is used to select each module by its stack position. This geographical addressing scheme avoids the need for address jumpers and possible conflicts, but requires that software must accommodate the physical placement of modules in the MIX stack.

The exception to this convention will be for the Model 4283 Baseboard, whose TMS320C30 processor only has a 24-bit address bus on the port it uses for the MIX bus. In this case, a page register is used for module selection (as opposed to different base addresses for each module), and the addresses are given as 6-digit hexadecimal codes, of the form 0xYY ZZZZ.

A final point must now be made about MIX nomenclature. Module 0 (or MIX position 0) refers to the closest module to the Baseboard, whether or not it is nested. Module 1 (or MIX position 1) is the module that may be mounted above Module 0, and Module 2 is the device that may be stacked above Module 1.

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3.2 Address Maps (continued)

3.2.1 Model 4275B Address Map for the 4200/01 Series Baseboards

Pentek's Models 4200 and 4201 Baseboards use a 16 MHz 68030 processor as the MIX bus controller. The 4200A and 4201A use a 40 MHz 68030. From the 68030's viewpoint, the MIX bus is mapped identically for all four of these Baseboards. The MIX_base address for Module 0 (which may either be nested, sharing the Baseboard's VMEbus slot, or be stacked in the adjacent slot), is 0xC000 0000. For the next device in the stack, Module 1, the base address is 0xD000 0000. Finally for the last MIX Module in the stack, Module 2, the MIX_base address is 0xE000 0000. Table 3-1, below, gives the physical addresses, in the memory space of the 68030 processor on any of these four Baseboards, that correspond to the symbolic names used to represent the Model 4275B's slave resources in subsequent sections of this manual.

Table 3-1: Memory Map for Use with Models 4200, 4200A, 4201 and 4201A MIX Baseboards 68030 View

4200/01 68030 Address	Symbolic Name	Resource
MIX_base+0x0000 0010	Control_3_Reg	Serial Programming of ADC Register
MIX_base+0x0000 000C	Control_2_Reg	Interrupt Mask and Status (R/W)
MIX_base+0x0000 0008	Control_1_Reg	Control Register (R/W)
MIX_base+0x0000 0004	InData_Reg	A/D FIFO (32 bits –Read Only)
MIX_base+0x0000 0000	InData_Reg	A/D FIFO (32 bits –Read Only)
Note: Any data in the A/D FIFO can be read at either of the addresses listed above.		
MIX_base Address: If Model 4275B is in MIX position 0, MIX_base = 0xC000 0000 If Model 4275B is in MIX position 1, MIX_base = 0xD000 0000 If Model 4275B is in MIX position 2, MIX_base = 0xE000 0000		

Note that the 4200 series of VME/MIX Baseboards also support mastering of the MIX bus by Upper MIX Bus Masters (UMBMs), and by other VMEbus Masters. For further information about MIX Bus access on these Baseboards in this manner, please refer to Pentek's Mix Tutorial for VMEbus Systems, Manual Part number 800.00001.

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3.2 Address Maps (continued)

3.2.2 Model 4275B Address Map for the Model 4202 Baseboard

The Model 4202 is a VMEbus slave-only Baseboard, and contains no processor. This device maps the resources connected to its MIX Bus into VMEbus A32, A24 or A16 slave address space. The VMEbus A32 or A24 base address is programmed into a register in the 4202's A16 interface by a VMEbus Master (the A16 base address is set by switches on the board). This register is cleared at power-up, resulting in a default base address of 0x0000 0000 in A32 space, or 0x00 0000 in A24 space.

In direct addressing mode, the two most significant bits of the VMEbus address (i.e., A31 and A30 in A32 space, A23 and A22 in A24 space or A15 and A14 in A16 space) select a particular 4202 Baseboard, by comparison with the two Least Significant Bits (D1 and D0) of the VMEbus Address Register. The next two VMEbus address bits (i.e., A29 and A28 in A32 space, A21 and A20 in A24 space, or A13 and A12 in A16 space) select among the MIX modules stacked on the 4202. Thus, assuming A32 operation and that the VMEbus Address Register is NOT written to, the MIX_base address for Module 0 is 0x0000 0000. Making the same assumptions, Module 1's MIX_base address is 0x1000 0000 and the MIX_base address for Module 2 is 0x2000 0000. These are the base addresses used by VMEbus masters when accessing modules in the 4202's MIX stack.

Table 3-2, below, presents the slave memory map for a Model 4275B installed on a Model 4202 Baseboard, assuming direct addressing, A32 or A24 operation, and that nothing has been written to the 4202's VME Address Register.

Table 3-2: Memory Map for Use with the Model 4202 MIX Baseboard

VMEbus Address	Symbolic Name	Resource
MIX_base+0x0000 0010	Control_3_Reg	Serial Programming of ADC Register
MIX_base+0x0000 000C	Control_2_Reg	Interrupt Mask and Status (R/W)
MIX_base+0x0000 0008	Control_1_Reg	Control Register (R/W)
MIX_base+0x0000 0004	InData_Reg	A/D FIFO (32 bits –Read Only)
MIX_base+0x0000 0000	InData_Reg	A/D FIFO (32 bits –Read Only)

Note: Any data in the A/D FIFO can be read at either of the addresses listed above.

Default MIX_base Address:

If Model 4275B is in MIX position 0, MIX_base = 0x0000 0000 for A32, or 0x00 0000 for A24
If Model 4275B is in MIX position 1, MIX_base = 0x1000 0000 for A32, or 0x10 0000 for A24
If Model 4275B is in MIX position 2, MIX_base = 0x2000 0000 for A32, or 0x20 0000 for A24

For information about using Paged Addressing Mode, A16 MIX access, multiple 4202's in the same card cage or Upper MIX Bus Masters, please refer to the Operating Manual for the Model 4202 Baseboard or the UMBM.

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3.2 Address Maps (continued)

3.2.3 Model 4275B Address Map for the Model 4283 Baseboard

On the Model 4283 Baseboard, there are two levels of addressing: 1) selection of the particular expansion module by its stack position and 2) selection of one of the resources within the module.

3.2.3.1 Module Selection

The TMS320C30 selects among MIX Modules by using a two-bit field in the Model 4283 Page Register, located at 'C30 address 0x80 0002. These two bits select one of the three possible MIX stack positions according to Table 3-3, below.

Table 3-3: Module Selection –Model 4283 Page Register 'C30 Address 0x80 0002

Page Register Bits>	D31-D18	D17	D16	D15	D14	D13-D0	Example
Stack Position 0	x	MXA27	1	1	MXA21	x	0x01 8000
Stack Position 1	x		1	0		x	0x01 0000
Stack Position 2	x		0	1		x	0x00 8000
x = other functions							

Access to some resources on certain MIX modules may require that either or both of the MIX bus A27 (MX_A27) and A21 (MX_A21) bits be set to the logic '1' state. On the 4283 baseboard, these bits are also contained in the Address Page Register. MX_A27 is the D17 bit of this register, and MX_A21 is the D14 bit. Table 3-3 also shows these bits.

3.2.3.2 Register Selection Within the Module

Once the module has been selected, all the slave resources (including the RAM Banks) of the Model 4275B appear in the TMS320C30 address map according to Table 3-4, below. Accessing these registers is accomplished by simply reading and writing these locations. The 24-bit addressing scheme accesses 32-bit data locations for the TMS320C30, even though many of the elements correspond to 8-bit or 16-bit devices.

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3.2 Address Maps (continued)

3.2.3 Model 4275B Address Map for the Model 4283 Baseboard (continued)

3.2.3.2 Register Selection Within the Module (continued)

Table 3-4: Memory Map for Use with the Model 4283 MIX Baseboard		
4283 'C30 Address	**Symbolic Name**	**Resource**
0x80 4004	Control_3_Reg	Serial Programming of ADC Register
0x80 4003	Control_2_Reg	Interrupt Mask and Status (R/W)
0x80 4002	Control_1_Reg	Control Register (R/W)
0x80 4001	InData_Reg	A/D FIFO (32 bits –Read Only)
0x80 4000	InData_Reg	A/D FIFO (32 bits –Read Only)
Note: Any data in the A/D FIFO can be read at either of the addresses listed above.		

3.2.4 Model 4275B Address Map for the Model 4284 Baseboard

The Model 4284 Baseboard uses a TMS320C40 Digital Signal Processor to master transactions with the MIX bus. The three MIX module locations are each mapped into separate, 64 M-Longword regions of the 'C40's memory space. Module 0's MIX_base address in the 'C40 memory map is 0x2000 0000. The MIX_base address for Module 1 is 0x2400 0000, and the 'C40's MIX_base address for Module 2 is 0x2800 0000. Table 3-5, below, presents the memory map for the slave resources on the Model 4275B, as seen by the 'C40 processor on the Model 4284 Baseboard.

Table 3-5: Memory Map for Use with the Model 4284 MIX Baseboard		
4284 'C40 Address	**Symbolic Name**	**Resource**
MIX_base+0000 0004	Control_3_Reg	Serial Programming of ADC Register
MIX_base+0000 0003	Control_2_Reg	Interrupt Mask and Status (R/W)
MIX_base+0000 0002	Control_1_Reg	Control Register (R/W)
MIX_base+0000 0001	InData_Reg	A/D FIFO (32 bits –Read Only)
MIX_base+0000 0000	InData_Reg	A/D FIFO (32 bits –Read Only)
Note: Any data in the A/D FIFO can be read at either of the addresses listed above.		
MIX_base Address: If Model 4275B is in MIX position 0, MIX_base = 0x2000 0000 If Model 4275B is in MIX position 1, MIX_base = 0x2400 0000 If Model 4275B is in MIX position 2, MIX_base = 0x2800 0000		

This Baseboard also supports mastering of the MIX bus by processor modules in the MIX stack, known as UMBM's (Upper MIX Bus Masters). For further details on this type of transaction, please refer to Pentek's Mix Tutorial for VMEbus Systems, Manual Part number 800.00001, the Model 4284 Operating Manual, or the UMBM's Operating Manual.

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3.2 Address Maps (continued)

3.2.5 Model 4275B Address Map for the Model 4285 Baseboard

When the Model 4285 is equipped with one of the MIX Expansion Bus Adapters (Options 031 or 036) all eight of its 'C40 processors can access modules on the MIX bus via the 4285's Main Bus. Additionally, four of the processors (A, B, E and F) have a separate access path to devices on the MIX bus via their Global I/O expansion ports. Separate control registers are provided for each of these five interfaces to the MIX bus. Two addressing modes, Normal and Compressed, are available for any of these access paths.

The control registers mentioned above each provide a 5-bit address page field. For this Baseboard, however, the page setting is NOT used to determine which MIX module is being addressed (i.e., the direct addressing method is used). The mapping of the page field onto the address bus is a function of the selected addressing mode. For complete details, refer to the Operating Manual for the Model 4285. For purposes of this operation summary, we will say that in Normal Addressing Mode, page bit 2 is used to assert the MXA27 address bit, while in Compressed Mode, MXA27 is asserted by 'C40 Global Address bit GA20.

Table 3-6, below, presents the memory map for the slave resources on the Model 4275B, as seen by the 'C40 processors on the Model 4285 Baseboard. The table also provides the MIX_base addresses, in the memory spaces of the 'C40 processors, for the Expansion bus and Global I/O access paths. For further information on the use of the 4285 as a MIX baseboard, including VME access to MIX resources on the 4285, please refer to Section 3.4 of the 4285 Operating Manual.

Table 3-6: Memory Map for Use with the Model 4285 MIX Baseboard

4285 'C40 Address	Symbolic Name	Resource
MIX_base+0000 0004	Control_3_Reg	Serial Programming of ADC Register
MIX_base+0000 0003	Control_2_Reg	Interrupt Mask and Status (R/W)
MIX_base+0000 0002	Control_1_Reg	Control Register (R/W)
MIX_base+0000 0001	InData_Reg	A/D FIFO (32 bits –Read Only)
MIX_base+0000 0000	InData_Reg	A/D FIFO (32 bits –Read Only)

Note: Any data in the A/D FIFO can be read at either of the addresses listed above.

MIX_base Address for Expansion Bus:	MIX_base Address for Global I/O Bus:
If Model 4275B is in MIX position 0, MIX_base = 0x9000 0000	If Model 4275B is in MIX position 0, MIX_base = 0xC800 0000
If Model 4275B is in MIX position 1, MIX_base = 0x9020 0000	If Model 4275B is in MIX position 1, MIX_base = 0xC820 0000
If Model 4275B is in MIX position 2, MIX_base = 0x9040 0000	If Model 4275B is in MIX position 2, MIX_base = 0xC840 0000

NOTE: MXA27 is asserted via page bit 2 in Normal addressing mode, or via 'C40 address bit GA20 in Compressed addressing mode

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3.3 Model 4275B Register Descriptions

The Model 4275B contains two 16-bit registers that are used to control the operating characteristics of the device. The Control Register (symbolic address Control_1_Reg) contains bits that control the number of active channels, the data packing mode of the output FIFO, and the sample clock source and divider. This register is described in detail in Section 3.3.1. The Interrupt Mask and Status Register (symbolic address Control_2_Reg) contains control bits that can start or stop the A/D conversion process and reset the output FIFO. This register also contains FIFO status and interrupt mask/enable bits, and is described further in Section 3.3.2.

3.3.1 Control Register - R/W @ Control_1_Reg

The bit structure of the Control Register on the Model 4275B, at symbolic address Control_1_Reg, is described in Table 3-7, below. The subsections that begin at the top of the next page discuss this register's bit structure in detail.

Table 3-7: Model 4275B –Control Register –Read/Write @ Control_1_Reg

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Not Used	Int_Clock_ Div_Mask_1	Int_Clock_ Div_Mask_0	Ext_Clock _Enable	Freq_Div_ Mask_3	Freq_Div_ Mask_2	Freq_Div_ Mask_1	Freq_Div_ Mask_0
Bit Function	Not Applicable	See Table 3-12, in Section 3.3.1.5		0=Internal 1=External	See Table 3-10, in Section 3.3.1.3			
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Not Used	Pack_Mode_ Mask_1	Pack_Mode_ Mask_0	Channel_ Mask_4	Channel_ Mask_3	Channel_ Mask_2	Channel_ Mask_1	Channel_ Mask_0
Bit Function	Not Applicable	See Table 3-9, in Section 3.3.1.2		See Table 3-8, in Section 3.3.1.1				

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3.3 Model 4275B Register Descriptions (continued)

3.3.1 Control Register - R/W @ Control_1_Reg (continued)

3.3.1.1 Channel Mask Bits: D0 - D4

These 5 bits contain the binary code (N-1) to enable and/or disable (i.e., mask) A/D conversion in N channels of the Model 4275B. The channels that are enabled will be channels 1 through N. Note that no matter how many channels are enabled, each channel scan requires about 7 µs to complete at the fastest sample rate. Table 3-8, below, tells which channels will be active as a function of the states of these bits.

Table 3-8: Model 4275B –Control Register –Channel_Mask_Bits (D0 –D4)

Ch_M_4 (D4)	Ch_M_3 (D3)	Ch_M_2 (D2)	Ch_M_1 (D1)	Ch_M_0 (D0)	Hex Code	Active Chans	Ch_M_4 (D4)	Ch_M_3 (D3)	Ch_M_2 (D2)	Ch_M_1 (D1)	Ch_M_0 (D0)	Hex Code	Active Chans
0	0	0	0	0	0x00	1	1	0	0	0	0	0x10	1 –17
0	0	0	0	1	0x01	1 –2	1	0	0	0	1	0x11	1 –18
0	0	0	1	0	0x02	1 –3	1	0	0	1	0	0x12	1 –19
0	0	0	1	1	0x03	1 –4	1	0	0	1	1	0x13	1 –20
0	0	1	0	0	0x04	1 –5	1	0	1	0	0	0x14	1 –21
0	0	1	0	1	0x05	1 –6	1	0	1	0	1	0x15	1 –22
0	0	1	1	0	0x06	1 –7	1	0	1	1	0	0x16	1 –23
0	0	1	1	1	0x07	1 –8	1	0	1	1	1	0x17	1 –24
0	1	0	0	0	0x08	1 –9	1	1	0	0	0	0x18	1 –25
0	1	0	0	1	0x09	1 –10	1	1	0	0	1	0x19	1 –26
0	1	0	1	0	0x0A	1 –11	1	1	0	1	0	0x1A	1 –27
0	1	0	1	1	0x0B	1 –12	1	1	0	1	1	0x1B	1 –28
0	1	1	0	0	0x0C	1 –13	1	1	1	0	0	0x1C	1 –29
0	1	1	0	1	0x0D	1 –14	1	1	1	0	1	0x1D	1 –30
0	1	1	1	0	0x0E	1 –15	1	1	1	1	0	0x1E	1 –31
0	1	1	1	1	0x0F	1 –16	1	1	1	1	1	0x1F	1 –32
Channel_Mask_(4-0) = Number of channels –1													

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3.3 Model 4275B Register Descriptions (continued)

3.3.1 Control Register - R/W @ Control_1_Reg (continued)

3.3.1.2 FIFO Data Packing Mode Mask Bits: D5 - D6

These two bits are used to determine the content of the 32-bit longword that is output by the Model 4275B's data FIFO. If both of these bits are cleared to the logic '0' state, then both words (D15 - D0 and D31 - D16) contain the same sample from the same channel. We refer to this as non-packed mode. If the Pack Mode Mask 0 bit (D5) is set to the logic '1' state, and the Pack Mode Mask 1 bit (D6) is cleared to the logic '0' state, then the FIFO operates in what we call channel packed mode. In channel packed mode, the upper 16 bits (D31 - D16) of each 32-bit longword delivered by the FIFO contain a sample from an odd-numbered channel, and the lower 16 bits (D15 - D0) contain a sample from the next higher even-numbered channel (e.g., D31 - D16 might contain a sample from channel 1, and D15 - D0 a sample from channel 2).

If the Pack Mode Mask 1 bit (D6) is set to the logic '1' state and the Pack Mode Mask 0 bit (D5) is set to either logic state '0' or '1', then the FIFO outputs data in time packed mode. In time packed mode, each 32-bit FIFO read provides two consecutive 16-bit samples from the same channel. The earlier sample will be in the upper 16 bits, with the later sample in the lower 16 bits.

Table 3-9, below, summarizes the settings of the Packing Mode bits in the Control Register of the Model 4275B.

Table 3-9: Model 4275B –Control Register –FIFO Data Packing Mode Mask Bits (D6 & D5)

Pack Mode Mask Bits		FIFO Longword Output		Packing Mode
PMM1 (D6)	PMM0 (D5)	High Word (D31 –D16)	Low Word (D15 –D0)	
0	0	Channel N, Sample T	Channel N, Sample T	Unpacked
0	1	Channel N, Sample T	Channel N+1, Sample T	Channel Packed*
1	0	Channel N, Sample T–1	Channel N, Sample T	Time Packed
1	1			

* –Notes for Channel Packed mode:
(1) N is an odd number
(2) An even number of channels must be enabled

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3.3 Model 4275B Register Descriptions (continued)

3.3.1 Control Register - R/W @ Control_1_Reg (continued)

3.3.1.3 Sample Clock Frequency Divider Mask Bits: D8 - D11

These bits determine the quantity by which the frequency of applied clock signal (whether it comes from the on-board crystal oscillator or from the SAMP CLK BNC connector) will be divided, before it is delivered to the A/D converter. The sigma-delta ADC utilized in the Model 4275B synthesizes its sample rate from a clock frequency that is 128 times higher than the desired rate. For sample rates of 100 kHz or less, the output of the 25.6 MHz crystal oscillator used on the Model 4275B is always divided by at least 2 before it is delivered to the ADC. An externally applied SAMP CLK signal may also need to be divided in frequency before it can drive the ADC's clock input. Selection of the input signal to the clock divider is made by the setting of JP1 (see Section 2.2.2). These four bits determine how much the frequency of that signal will be divided, as described in Table 3-10, below. The table also gives the ADC clock signal frequency and the sample rate that will be obtained if the internal crystal oscillator is selected to drive the divider.

Table 3-10: Model 4275B –Control Register – Sample Clock Frequency Divider Mask Bits (D8 –D11)

D11 (FDM3)	D10 (FDM2)	D9 (FDM1)	D8 (FDM0)	Hex Code	Clock Divider	with internal clock...	
						Clock Freq.	Sample Rate
0	0	0	0	0x0	2	12.8 MHz	100 kHz
0	0	0	1	0x1	4	6.4 MHz	50 kHz
0	0	1	0	0x2	6	4.27 MHz	33.33 kHz
0	0	1	1	0x3	8	3.2 MHz	25 kHz
0	1	0	0	0x4	10	2.56 MHz	20 kHz
0	1	0	1	0x5	12	2.13 MHz	16.67 kHz
0	1	1	0	0x6	14	1.83 MHz	14.29 kHz
0	1	1	1	0x7	16	1.6 MHz	12.5 kHz
1	0	0	0	0x8	18	1.42 MHz	11.11 kHz
1	0	0	1	0x9	20	1.28 MHz	10 kHz
1	0	1	0	0xA	22	1.16 MHz	9.09 kHz
1	0	1	1	0xB	24	1.07 MHz	8.33 kHz
1	1	0	0	0xC	26	985 kHz	7.69 kHz
1	1	0	1	0x0D	28	914 kHz	7.14 kHz
1	1	1	0	0x0E	30	853 kHz	6.67 kHz
1	1	1	1	0x0F	32	800 kHz	6.25 kHz
Divider = (FDM(3...0) + 1) X 2 or FDM(3...0) = (Divider/2) –1							

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3.3 Model 4275B Register Descriptions (continued)

3.3.1 Control Register - R/W @ Control_1_Reg (continued)

3.3.1.4 External Clock Enable Bit: D12

Bit D12 in the Model 4275B's Control Register selects the source of the clock signal delivered to the ADC. If this bit is cleared to the logic '0' state, the ADC is clocked by the output of the frequency divider circuit. If this bit is set to the logic '1' state, the signal applied to the SAMP CLK BNC connector on the 4275B's front panel drives the ADC. This signal is divided by the clock divider value set in the sample clock frequency divider mask bits. To operate in this mode, the SAMP CLK connector must be jumper-configured as an input (see Section 2.2.3).

Table 3-11, below, summarizes the settings of this bit. See Sections 4.2 and 4.4 for detailed discussions on the topic of clocking the Model 4275B's A/D Converters.

Table 3–11: Model 4275B –External Clock Enable Bit (D12)

Ext_Clk_Enable	ADC Clock Source
0	Frequency Divider O/P
1	Samp Clk BNC

3.3.1.5 Internal Clock Output Divider Mask Bits: D13 - D14

If the SAMP CLK connector on the Model 4275B's front panel is configured as an output (see Section 2.2.3), the signal delivered to that connector may be either the crystal oscillator's 25.6 MHz output frequency, or that frequency divided by 2, 4 or 8, depending upon the programming of these bits. Table 3-12, below, tells what output frequency can be expected at the SAMP CLK connector will be as a function of the settings of these bits.

Table 3–12: Model 4275B –Internal Clock Divider Mask Bits (D13 –D14)

ICDM1 (D14)	ICDM0 (D13)	SAMP CLK O/P Freq
0	0	25.6 MHz
0	1	12.8 MHz
1	0	6.4 MHz
1	1	3.2 MHz

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3.3 Model 4275B Register Descriptions (continued)

3.3.2 Interrupt Mask and Status Register - R/W @ Control_2_Reg

The bit structure of the Model 4275B's Interrupt Mask and Status Register, at symbolic address Control_2_Reg, is described in Table 3-13, below. The sub-sections that follow the table discuss the register's bit groups and individual bits in detail. Note that the upper 8 bits of this register (D15 - D8) are ignored for write operations.

Table 3-13: Model 4275B –Interrupt Mask and Status Register –Read/Write @ Control_2_Reg

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Last_Chan _Stat	HFIFO_ Empty_Stat	HFIFO_ Hfull_Stat	HFIFO_ Full_Stat	Last_Chan_ Int_Stat	LFIFO_ Empty_Stat	LFIFO_ Hfull_Stat	LFIFO_ Full_Stat
Bit Function	1=Last Chan 0=Not Last	1 = True 0 = False						
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Last_Chan _Int_Ena	FIFO_Not_ Empty_Int_Ena	FIFO_HFull _Int_Ena	FIFO_Full _Int_Ena	Not Used		Release _FIFO	Start_ Conversion
Bit Function	1 = Interrupt Enabled 0 = Interrupt Masked				Not Applicable		1=Release 0=Reset	1 = Run 0 = Stop

3.3.2.1 Start Conversion Bit: D0

While this bit is held in the logic '0' state, the A/D converters in the Model 4275B are disabled and no sampling takes place. When this bit is set to the logic '1' state, sampling and A/D conversion are enabled.

3.3.2.2 Release FIFO Bit: D1

While this bit is held in the logic '0' state, the FIFO on the Model 4275B is held in the reset state and will not accept data from the ADCs. When this bit is cleared, any data that may be in the FIFO is lost. When this bit is set to the logic '1' state, the FIFO is released and will accept the ADCs' output data.

The FIFO reset operation should be implemented as a toggle. In other words, first clear this bit to the logic '0' state (to reset the FIFO), then set it back to logic '1' (to release the reset and allow sample collection).

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3.3 Model 4275B Register Descriptions (continued)

3.3.2 Interrupt Mask and Status Register - R/W @ Control_2_Reg (continued)

3.3.2.3 FIFO Interrupt Enable Bits: D4 - D6

Setting any of these bits to the logic '1' state enables the generation of a MIX bus interrupt when the indicated FIFO condition occurs. The interrupt enabled by D4 will occur when the FIFO has been completely filled. The interrupt enabled by D5 will occur when the FIFO becomes half-full, and D6's interrupt will be generated when the first sample reaches the FIFO (i.e., when the FIFO is no longer empty).

Clearing any of these bits to the '0' state prevents an interrupt from being generated when the indicated FIFO condition becomes true. See Section 4.6 for more information about interrupt generation.

3.3.2.4 Last Channel Interrupt Enable Bit: D7

When this bit is set to the logic '1' state, a MIX bus interrupt will be generated when the data from the last channel converted in a scan is written into the FIFO. A "scan" is the group of samples obtained from channels 1 through N, where N is the number of active channels programmed into the Control Register. A scan requires about 7 µs to complete at the fastest sample rate, regardless of how many channels are enabled. See Section 3.3.1.1 and Table 3-8 for information about the enabling of ADC channels.

When this bit is cleared to the '0' state, the last channel interrupt will not be generated. See Section 4.6 for more information about the interrupter operation of the Model 4275B.

3.3.2.5 FIFO Status Bits: D8 - D10 and D12 - D14

These bits reflect the states of the three flags in each FIFO set on the Model 4275B. The FIFO ICs used in this device are four IDT 7206s, which are 16k x 9 bit devices. One pair of these chips holds the samples delivered to the upper 16 bits of the MIX data bus, and the other pair places its samples on the MIX bus' lower 16 bits. The 9th bit in each FIFO is used as the last channel indicator, and its output is delivered to this status register rather than the MIX data bus. Each pair is configured as a single, 16-bit FIFO, and we refer to them as the High and Low FIFOs.

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3.3 Model 4275B Register Descriptions (continued)

3.3.2 Interrupt Mask and Status Register - R/W @ Control_2_Reg (continued)

3.3.2.5 FIFO Status Bits: D8 - D10 and D12 - D14 (continued)

The state of the Low FIFO's Full, Half-full and Empty flags can be read in bits D8, D9 and D10, respectively, of the 4275B's Interrupt Mask and Status Register. The High FIFO's Full, Half-full and Empty flags can be monitored in bits D12, D13 and D14, respectively. The 'true' state for all of these flags is the logic '1' state.

Any data written to these six bits will be ignored.

3.3.2.6 Last Channel Interrupt Status Bit: D11

This bit will be held the logic '1' state to indicate that a last channel interrupt has been generated. This interrupt occurs when the following two conditions are met: (1) the data from the last enabled channel was written to the FIFO; and (2) bit D7 of this register is set to the logic '1' state (see Section 3.3.2.4). The bit will be cleared when the MIX bus interrupt handler clears the interrupt, and will remain in the logic '0' state until another last channel interrupt is generated. See Section 4.6 for further information about the 4275B as a MIX bus interrupter.

Data written to this bit will be ignored.

3.3.2.7 Last Channel Status Bit: D15

This bit will be set to the logic '1' state to indicate that the last data read from the FIFO contained data from the last enabled channel. It will be in the logic '0' state at any other time.

Data written to this bit will be ignored.

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3.3 Model 4275B Register Descriptions (continued)

3.3.3 ADC Function Programming Register- R/W @ Control_3_Reg

The ADC Function Programming Register drives the Zcal, DFS, and the HPFE pins on AKM AK5393 Analog to Digital Converter chip and the Polarity Select Bit (Option 101 only). The bit structure of this register, at symbolic address Control_3_Reg, is described in Table 3-14, below. The subsections that follow the table discuss the register's bit groups and individual bits in detail. Bit D1 and the upper ten bits (D15 - D5) of this register are not used.

Table 3-14: ADC Function Programming Register –R/W @ Control_3_Reg

Bit #	D15 –D5	D4	D3	D2	D1	D0
Bit Name	Reserved	Polarity Option (Option 101 Only)	Zcal (Option 101 Only)	DFS	Reserved	High Pass Filter Enable
Bit Function	Do Not Use	0 = Disable 1 = Enable	0 = Analog Input 1 = VCOM	Always Write 0	Do Not Use	0 = Disable 1 = Enable

3.3.3.1 High Pass Filter Enable Bit: D0

Bit D0 is connected to the High Pass Filter Enable (HPFE) pin on AKM AK5393 Analog to Digital Converter chip. Setting this bit to logic '1' enables the ADC chips High Pass Filter, which has a cutt-off frequency of 2.08 Hz at a sampling frequency of 100 kHz. Clearing this bit to logic '0' disables the High Pass Filter.

3.3.3.2 Double Speed Sampling Mode Bit: D2

Bit D2, DFS, is connected to the Double Speed Sampling Mode Pin. This bit must be cleared to logic '0', Normal Speed, for the Model 4275B to function properly.

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3.3 Model 4275B Register Descriptions (continued)

3.3.3 ADC Function Programming Register- R/W @ Control_3_Reg (continued)

3.3.3.3 Zero Calibration Control Bit (Option 101 only): D3

On units equipped with Option 101, bit D3 (Zcal) is connected to the Zero Calibration Control Pin. This Pin controls the calibration reference signal. Setting this bit to logic '1' selects the Analog Input Pins AINL+, AINL-, AINR+ and AINR- as the calibration reference signal. Clearing this bit to logic '0' selects the Common Voltage Pins VCOML and VCOMR as the calibration reference signal.

During the calibration cycle, the value of the reference signal is stored This value is then subtracted from all future outputs.



NOTE

The calibration cycle is invoked when the clock is restored after being removed for a duration of 50 ms or longer. See Section 4.3 on Page 36.

3.3.3.4 Polarity Select Bit (Option 101 only): D4

Bit D4, Polarity Select, is used to select the output polarity on units equipped with Option 101. Setting this bit to logic '1', inverts the output polarity signal. Clearing this bit to logic '0', disables this function.

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Chapter 4: Operating Procedures

4.1 Introduction

This chapter draws upon the information presented earlier in this manual to provide the user with procedures to follow when using the Model 4275B. The information presented here assumes that the configuration jumpers on your 4275B have been set according to the requirements of your application (see Chapter 2 for details), and that you have already installed your MIX modules on the Baseboard of your choice (MIX stack assembly instructions are presented in Pentek's Mix Tutorial for VMEbus Systems, Manual Part number 800.00001). Detailed descriptions of the registers referred to in the sections below were given in Chapter 3.

4.2 Selecting the A/D Clock Source

The A/D Converters in the Model 4275B may receive their clock signal directly from a signal applied to the Front Panel SAMP CLK BNC connector, from frequency division of such a signal, or from frequency division of the internal 25.6 MHz crystal oscillator. There are three items in this unit that are involved in the selection of the clock source. These are the Frequency Divider Input Select Jumper (JP1, see Section 2.2.2), the SAMP CLK In/Out Jumper (JP2, see Section 2.2.3), and the External Clock Enable Bit (D12 in the Control Register, at symbolic address Control_1_Reg, see Section 3.3.1.4). Figure 4-1, below, shows the clock selection and divider circuit. Table 4-1, on Page 36, tells what the source of the A/D Converter's clock signal will be as a function of the settings of the three variables referred to above.

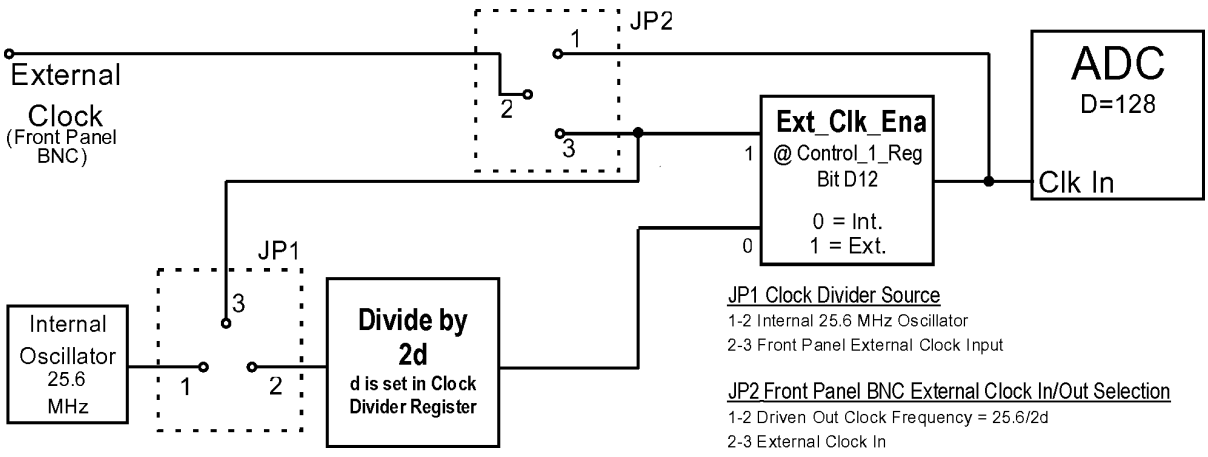


Figure 4–1: Model 4275B –Clock Selection and Divider Circuit

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4.2 Selecting the A/D Clock Source (continued)

Table 4–1: Model 4275B –Clock Source Selection			
JP1	**JP2**	**Ext_Clk_Ena**	**A/D Clock Signal**
1 –2	1 –2	0	Internal XTAL Osc. divided
1 –2	1 –2	1	Do Not Use
1 –2	2 –3	0	Internal XTAL Osc., divided
1 –2	2 –3	1	SAMP CLK BNC, direct
2 –3	1 –2	0	Do Not Use
2 –3	1 –2	1	Do Not Use
2 –3	2 –3	0	SAMP CLK BNC, divided
2 –3	2 –3	1	SAMP CLK BNC, direct

4.3 Calibration Cycle

The Model 4275B has a circuit that detects when the A/D clock is missing. This circuit will detect the absence of a clock signal (such as an external clock) to the A/D converter, after 256 cycles from the internal oscillator have elapsed. The circuit will then assert the reset signal to the A/D converter.

When the clock is reapplied to the A/D converter, the clock detector circuit removes the reset, thus invoking the A/D calibration cycle. By utilizing this function, multiple boards may be synchronized by merely removing and applying the external clock.

During the calibration cycle, the value of the reference signal (the analog input on the standard Model 4272B) is stored This value is then subtracted from all future outputs. For Model 4275B's equipped with Option 101, see Section 3.3.3.3 on Page 34.

Note, that a single board using the internal clock may also initiate calibration by momentarily switching to the external clock mode. Of course, there should not be any clock applied to the front panel BNC connector for the calibration cycle to function.

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4.4 Programming the Sample Rate

If the Model 4275B's frequency divider is selected as the ADCs' clock source, the divider must be programmed to produce a clock frequency that will deliver the desired sample rate. The sample rate is always equal to the clock frequency (whatever its source may be) divided by 128.

The programming of the frequency divider bits, D8 - D11 (Freq_Div_Mask_(3...0)) in the Control Register at symbolic address Control_1_Reg, was discussed in Section 3.3.1.3. The table from that section, which provides most of the details, is reproduced below as Table 4-2.

Table 4-2: Model 4275B –Control Register – Sample Clock Frequency Divider Mask Bits (D8 –D11)

D11 (FDM3)	D10 (FDM2)	D9 (FDM1)	D8 (FDM0)	Hex Code	Clock Divider	with internal clock...	
						Clock Freq.	Sample Rate
0	0	0	0	0x0	2	12.8 MHz	100 kHz
0	0	0	1	0x1	4	6.4 MHz	50 kHz
0	0	1	0	0x2	6	4.27 MHz	33.33 kHz
0	0	1	1	0x3	8	3.2 MHz	25 kHz
0	1	0	0	0x4	10	2.56 MHz	20 kHz
0	1	0	1	0x5	12	2.13 MHz	16.67 kHz
0	1	1	0	0x6	14	1.83 MHz	14.29 kHz
0	1	1	1	0x7	16	1.6 MHz	12.5 kHz
1	0	0	0	0x8	18	1.42 MHz	11.11 kHz
1	0	0	1	0x9	20	1.28 MHz	10 kHz
1	0	1	0	0xA	22	1.16 MHz	9.09 kHz
1	0	1	1	0xB	24	1.07 MHz	8.33 kHz
1	1	0	0	0xC	26	985 kHz	7.69 kHz
1	1	0	1	0x0D	28	914 kHz	7.14 kHz
1	1	1	0	0x0E	30	853 kHz	6.67 kHz
1	1	1	1	0x0F	32	800 kHz	6.25 kHz
Divider = (FDM(3...0) + 1) X 2 or FDM(3...0) = (Divider/2) –1							

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4.5 The Clock Output

When the 4275B is configured such that the front panel SAMP CLK connector is an output, that output is driven by a different frequency divider from the one that provides the A/D clock signal. This divider is programmed by D13 and D14 (Int_Clk_Div_Mask_(0-1)) in the Control Register at symbolic address Control_1_Reg. Details about the programming of these bits can be found in Section 3.3.1.5, and the table from that section is reproduced below as Table 4-3.

Table 4-3: Model 4275B –Internal Clock Divider Mask Bits (D13 –D14)

ICDM1 (D14)	ICDM0 (D13)	SAMP CLK O/P Freq
0	0	25.6 MHz
0	1	12.8 MHz
1	0	6.4 MHz
1	1	3.2 MHz

4.5.1 Synchronizing Multiple 4275Bs

If your application requires more than 32 channels of A/D conversion, up to three Model 4275B MIX modules may be installed on a single MIX Baseboard. In cases such as this, one 4275B can be configured as the 'master' device. This device would use his internal oscillator to clock his ADC, and have the SAMP CLK jumper set to drive the connector with a clock output (jumper on JP2, 1 - 2). The other (slave) device(s) should then be set to accept an input signal on the SAMP CLK connector (jumper on JP2, 2 - 3), and its SAMP CLK input(s) driven from the Master's SAMP CLK output. Depending upon the desired sample rate, you may or may not need to use the internal frequency dividers on the 'Slave' 4275Bs.

To insure that all devices in such a system begin sampling simultaneously, the External Clock Enable bit (D12 @ Control_1_Reg) should initially be set to the logic '1' state on the master as well as the slaves. This prevents the master from driving the clock output until the slave(s) is ready to receive clock signals.

After resetting the FIFOs on all units (by toggling the D1 bit at symbolic address Control_2_Reg, see Section 3.3.2.2), the External Clock Enable bit on the master can be cleared back to logic '0' to start sampling on all devices.

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4.6 Interrupting the MIX Bus

The Model 4275B can be programmed to issue a MIX bus interrupt when it is ready to deliver data to a MIX baseboard or Upper MIX Bus Master (UMBM). Bits D4 - D7 in the Interrupt Mask and Status Register, at symbolic address Control_2_Reg, are the Interrupt Enable Bits, covered in detail in Sections 3.3.2.3 and 3.3.2.4. These bits all mask interrupts for the associated condition when low, and enable interrupts when high. The conditions associated with these bits are listed below, in Table 4-4.

Table 4-4: Model 4275B –Interrupt Mask and Status Register –Interrupt Enable bits and their Associated Conditions

Bit	Condition
D4	FIFO Full
D5	FIFO Half-Full
D6	FIFO Not Empty
D7	Data from Last Chan.
A '1' in any of these bits enables interrupts when the associated condition is met. A '0' in any of these bits masks the interrupt for that condition	

4.7 Using the Status Bits

If you choose not to have the 4275B issue an interrupt when it is ready to deliver data, you may instead have the MIX Baseboard or UMBM check, or 'poll', the Status Bits in the Interrupt Mask and Status Register at symbolic address Control_2_Reg.

The 32-bit output data FIFO is actually composed of two 16-bit devices. We call the FIFO whose data will appear on D15 - D0 of the MIX data bus the Low FIFO, and the one that outputs data to D31 - D16 is known as the High FIFO. The states of the Empty, Half-Full and Full Flags from both the Low and High FIFOs can be read in the Status Bits.

Note that there are times when the flag states for the High and Low FIFOs may not match. Depending upon the output data packing format selected, the duration of the mismatch in flag states may persist for one clock period (in channel packed modes) or for one scan period (about 7 µs, at the fastest sample rate, for time packed modes). See Section 4.9 for more information about the mechanics of the data packing process and the reasons for mismatched flag states. For the discussion at hand, we will simply state that both the High and Low flags should be read and should be valid before reading data from the Model 4275B.

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4.7 Using the Status Bits (continued)

There are also two Status Bits associated with the last enabled channel. One of these indicates that the last read access delivered data from the last enabled channel, and the other indicates that a last channel interrupt is pending.

Table 4-5, below, identifies the Status Bits in the Model 4275B's Interrupt Mask and Status Register.

Table 4-5: Model 4275B –Interrupt Mask and Status Register –Status Bits

Bit	Condition
D8	Low FIFO Full
D9	Low FIFO Half-Full
D10	Low FIFO Empty
D11	Last Chan. Int. Pending
D12	High FIFO Full
D13	High FIFO Half-Full
D14	High FIFO Empty
D15	Data from Last Chan.
A '1' in any of these bits indicates that the associated condition is true	

4.8 Aligning Output Data - The Last Channel

Because the Model 4275B contains no processor or other on-board device to place it in a known initial state, there is no way of knowing which of the enabled ADC channels' data will be first in line in the output FIFO. The purpose of the three last channel indicators discussed in the last two sections is to let you know that the NEXT sample available will be from Channel 1. Thus, an important part of the initialization procedure for this device is to read out the initial samples from the FIFO, while either monitoring the last channel status bit or waiting for the last channel interrupt. The samples read while waiting for the last channel indication may be discarded.

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4.9 Output Data Formats

The data that you read out of the Model 4275B is always presented in 16-bit 2's complement format. The output FIFO, however, is 32-bits wide (to take advantage of the MIX bus' data width), allowing two samples to be read each time the module is accessed. What samples will appear in any given read access to the 4275B is a programmable function, addressed by the Pack Mode Mask(1-0) Bits (D5 and D6) in the Control Register. Details about the programming of these bits may be found in Section 3.3.1.2. The table from that section is reproduced below as Table 4-6.

Table 4-6: Model 4275B –Control Register –FIFO Data Packing Mode Mask Bits (D6 & D5)

Pack Mode Mask Bits		FIFO Longword Output		Packing Mode
PMM1 (D6)	PMM0 (D5)	High Word (D31 –D16)	Low Word (D15 –D0)	
0	0	Channel N, Sample T	Channel N, Sample T	Unpacked
0	1	Channel N, Sample T	Channel N+1, Sample T	Channel Packed*
1	0	Channel N, Sample T–1	Channel N, Sample T	Time Packed
1	1			

* –Notes for Channel Packed mode:
(1) N is an odd number
(2) An even number of channels must be enabled

Familiarity with the mechanics of the data packing process may help with your decision about which format to select. The data packing process on the Model 4275B is controlled by a state machine. The state machine controls the flow of data from the ADC to the High and Low FIFOs. In addition to the state machine, the 4275B contains two independent 16k x 16 FIFO structures, each composed of two 16k x 9 IDT7206 FIFO memory devices.

Each enabled AK5393 A/D converter outputs a 16-bit serial data stream for each sample acquired. The first operation of the FIFO loading state machine is the conversion of the serial stream into a 16-bit parallel word. The next operation, performed on the word, depends on the selected packing format. The simplest case is the unpacked format. In this format, each acquired data word is loaded in parallel to both the Low FIFO and the High FIFO. The data path and FIFO write timing are illustrated in Figure 4-2, at the top of the next page.

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4.9 **Output Data Formats** (continued)

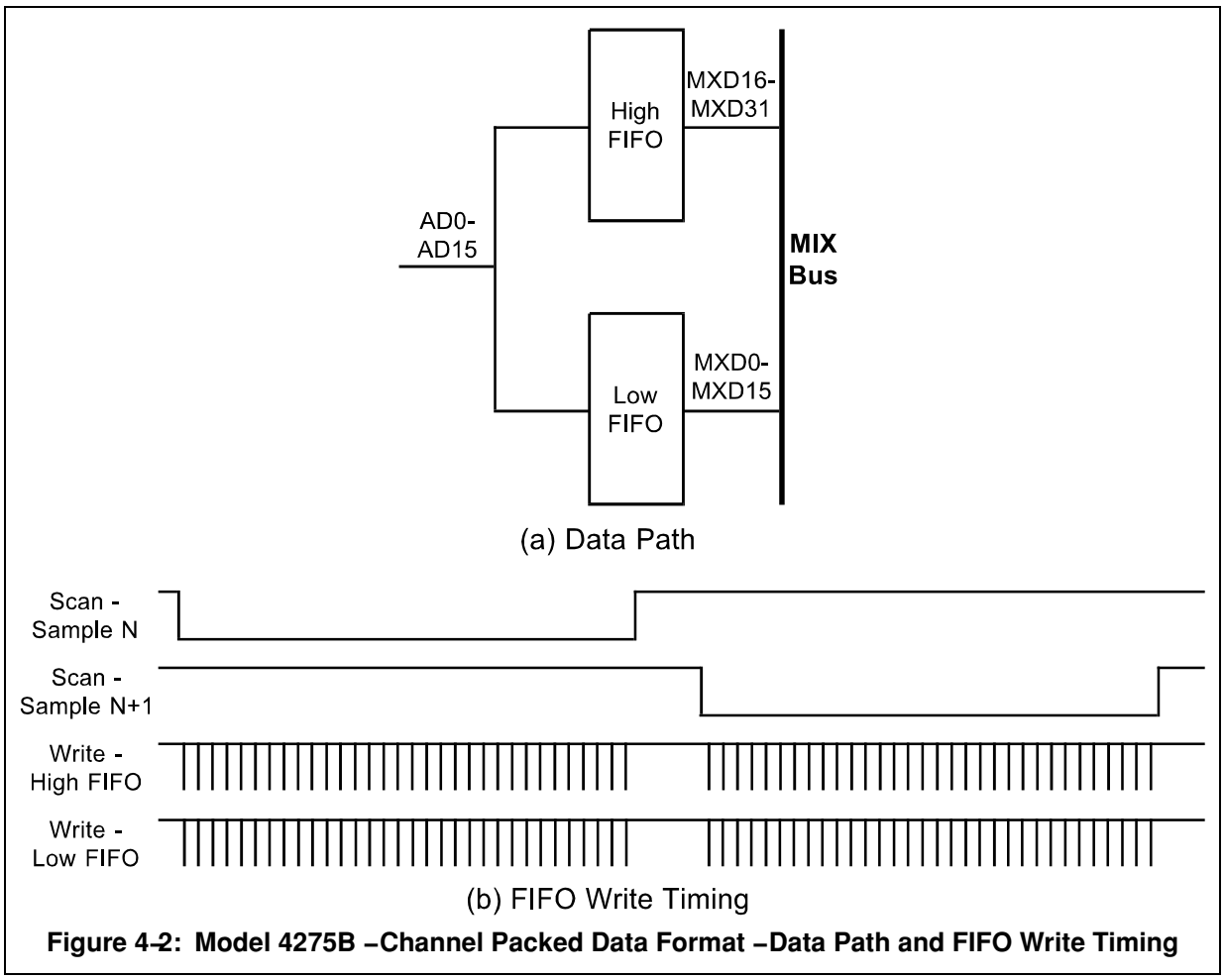


Figure 4-2: Model 4275B –Channel Packed Data Format –Data Path and FIFO Write Timing

If channel packed format is selected, data acquired during a given sample period is output on a channel-paired basis. While reading the description of this format, which begins at the top of the next page, remember that the Model 4275B does not allow the user to select which channels are enabled. If only one channel is enabled, it must be channel 1. If only two are enabled, they must be channels 1 and 2, and so on. Also recall that an even number of channels must be enabled to operate in channel packed mode.

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4.9 Output Data Formats (continued)

When operating in channel packed mode, the first sample acquired (from channel 1) is loaded into the first location in the High FIFO. The second sample acquired (from channel 2, during the same sample period) is loaded into the first location in the Low FIFO. The next sample, whose source will depend on the number of channels enabled (it will come from channel 3 during the same sample period if more than two channels are enabled, or from channel 1 during the next sample period if only two channels are enabled) will be written into the second location in the High FIFO. The fourth sample will go into the second location in the Low FIFO, and so on.

Let's suppose that we are polling the FIFO Status flags while operating in channel packed mode. Since the High and Low FIFOs are written during alternating sample periods, the High FIFO contains one sample more than the Low FIFO during every second sample period. This means that there is a finite chance that when reading the Status register, the High FIFO's flag will be true, and the Low FIFO's flag will be false. This condition, however, will only last for one sample period. Figure 4-3, below, illustrates the data path and FIFO write timing for the channel packed data format.

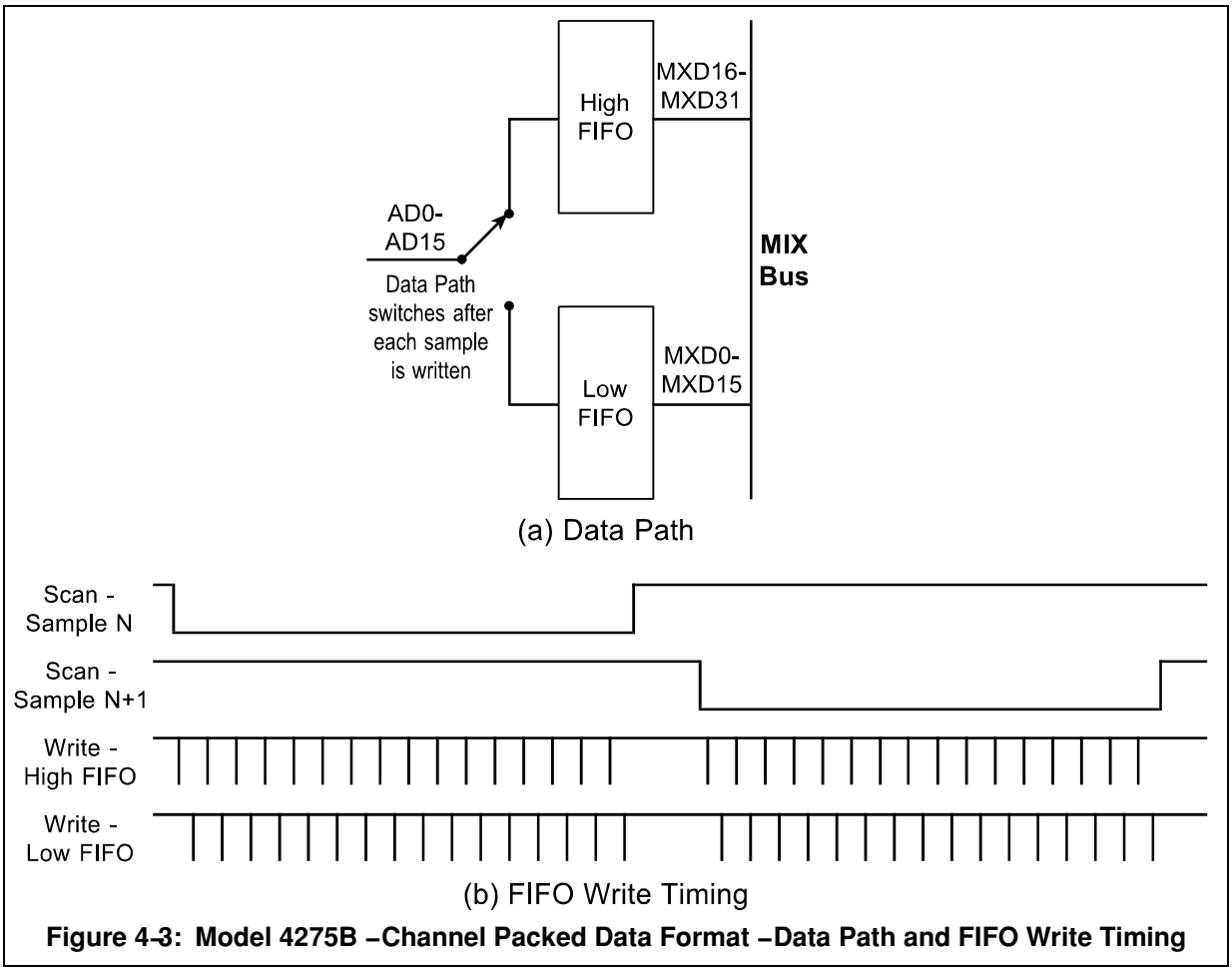


Figure 4-3: Model 4275B –Channel Packed Data Format –Data Path and FIFO Write Timing

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4.9 Output Data Formats (continued)

If one of the two time packed data formats is selected, all samples acquired from all enabled channels in any given scan will be written to one FIFO. The samples acquired during the next scan will be written to the other FIFO. The data acquired during the third scan are written to the next N locations in the first FIFO, the results of the fourth scan are written to the next locations in the second, and so on. The difference between the two time packed formats is simply in which FIFO gets written first.

When monitoring the FIFO flags in the Status register while operating in time packed format, the time period during which the flag states will not match is much longer than in channel packed mode. This is because the second FIFO trails the first by up to 32 samples, rather than by only one sample. The duration of the mismatch in flag states will therefore be a full scan period (about 7 µs, at the fastest sample rate), rather than a single sample period. Figure 4-4, below, illustrates the data path and FIFO write timing relationships in time packed mode.

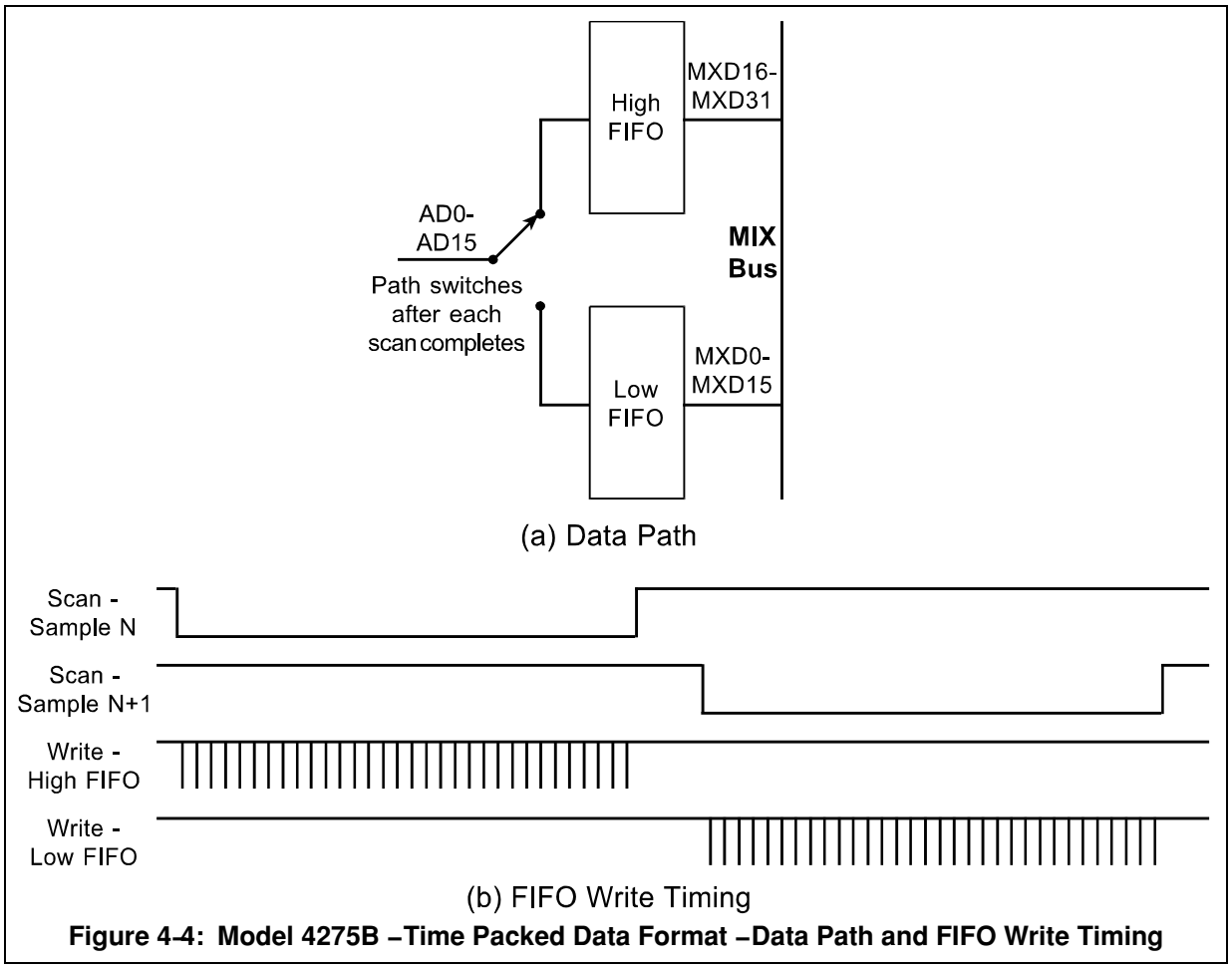


Figure 4-4: Model 4275B –Time Packed Data Format –Data Path and FIFO Write Timing

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4.10 Initial Output Samples

Because of the digital filtering technology used in the output stages of the AK5393 A/D converters in the Model 4275B, the first 17,920 samples available at the A/D converter outputs after calibration are 0's. To insure that the data you take from this device is reliable, we recommend that the first 17,920 samples from each active channel be discarded. All samples taken thereafter may be regarded as valid.

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Appendix A: Programming Examples

A.1 Introduction

The 'C' programs that follow were written to allow the Model 4275B to be used on any of Pentek's VME/MIX baseboards. Five sample source files are included.

Two header files are presented here, **mod.h** (see Section A.4, starting on Page A-5) and **4275.h** (see Section A.2, below). The user initializes constants in the file **mod.h** prior to compiling, to select the type of MIX baseboard he will use and the MIX stack position of the Model 4275B. This file (**mod.h**) initializes several symbolic constants used by the other files included here, and is intended as a general purpose header file for use with all Pentek MIX modules. The file **4275.h** contains header information specific to the Model 4275B.

The file **p4275.c** (see Section A.3, beginning on Page A-2) contains the code that allows the baseboard selected in **mod.h** to initialize the Model 4275B, release it to accept analog inputs, monitor its status and read out the data it collects. Prior to compiling, the user sets symbolic constants in this file to select input configuration, the input clock rate, and to decide whether interrupts or polling will be used to determine when the 4275B is ready to deliver data. The file **init.c** (see Section A.5, starting on Page A-9) performs any necessary pre-initialization chores on the baseboard. Finally, the file **intr.c** (see Section A.6, starting at the top of Page A-10) determines which (if any) MIX interrupts to enable, using information from **mod.h**.

A.2 4275.h

```
/* 4275.h  - This file contains 4275 module specific information */

#ifndef P4275_H
   #define P4275_H

#define P4275_MAX_CHANS        32
#define P4275_FIFO_SIZE        (16 * 1024)

/* 4275 Mix Module Register Offsets */
#define P4275_CONTROL_1_REG    0x00000002L
#define P4275_CONTROL_2_REG    0x00000003L
#define P4275_INDATA_REG       0x00000000L

/* Constants specific to each Register */

/* Control Register #1 */
#define CR_CHANNEL_MASK        0x0000001fL
#define CR_PACK_MODE_MASK      0x00000060L
#define CR_FREQ_DIV_MASK       0x00000f00L
#define CR_EXTERNAL_CLOCK      0x00001000L
#define CR_INT_CLOCK_DIV_MASK  0x00006000L
```


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A.2 **4275.h** (continued)

```
/* Control Register #2 */
#define CR_START_CONVERSION    0x00000001L
#define CR_RELEASE_FIFO        0x00000002L
#define CR_FIFO_FULL_INT_ENA   0x00000010L
#define CR_FIFO_HFULL_INT_ENA  0x00000020L
#define CR_FIFO_EMPTY_INT_ENA  0x00000040L
#define CR_LAST_CHAN_INT_ENA   0x00000080L
#define CR_LFIFO_FULL_STAT     0x00000100L
#define CR_LFIFO_HFULL_STAT    0x00000200L
#define CR_LFIFO_EMPTY_STAT    0x00000400L
#define CR_LAST_CHAN_INT_STAT  0x00000800L
#define CR_HFIFO_FULL_STAT     0x00001000L
#define CR_HFIFO_HFULL_STAT    0x00002000L
#define CR_HFIFO_EMPTY_STAT    0x00004000L
#define CR_LAST_CHAN_STAT      0x00008000L

#endif
```

A.3 p4275.c

```
#include "mod.h"
#include "4275.h"

#define POLLING         0
#define INTERRUPTS      1
#define NUM_CHANNELS    4  /* Number of channels to enable */

#if BB_4283
   unsigned int *PageAddressReg, *ExpBusControlReg;
#endif

unsigned int *Control1, *Control2, *InData;
unsigned int sig1[2048], sig2[2048], sig3[2048], sig4[2048];
unsigned int num_samples;

extern void enableInterrupts();
extern void clearInterrupt();
extern void board_init();

int counter;
```


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A.3 **p4275.c** (continued)

```
main()
{
   int i,j,num;
   unsigned long data;

   #if BB_4283
      ExpBusControlReg   = (unsigned int *) 0x808060u;
      PageAddressReg     = (unsigned int *) 0x800002u;
   #endif

   Control1 = (unsigned int *) (MOD | P4275_CONTROL_1_REG);
   Control2 = (unsigned int *) (MOD | P4275_CONTROL_2_REG);
   InData   = (unsigned int *) (MOD | P4275_INDATA_REG);

   #if BB_4283
      *ExpBusControlReg = 0x68;         /* Remove MIX bus wait states */
      *PageAddressReg = MOD_SELECT;     /* Select module */
   #endif

   /* Reset Fifo's and Stop Conversion Process */
   *Control1 = 0;
   *Control2 = 0;

   board_init();

   #if INTERRUPTS
      counter = 0;
      i = *Control2;        /* Clear any Pending Interrupts */
      enableInterrupts();
   #endif

   /* Enable the Number of Channels, No Packing, Divide by 2 Freq, */
   /* Internal Sample Clock, and 25.6 MHz Clock                    */
   *Control1 = NUM_CHANNELS - 1;

   /* Release Fifo(s) */
   *Control2 = CR_RELEASE_FIFO;
   delay(100);        /* Wait a small amount to allow fifos to release */

   /* Release Fifo and Enable Conversion */
   *Control2 = CR_RELEASE_FIFO | CR_START_CONVERSION;

   /* Determine Number of samples to readout per channel */
   num_samples = (P4275_FIFO_SIZE / 2) / NUM_CHANNELS;

   /* Sync up input by determining last channel*/
   while(!(*Control2 & CR_LAST_CHAN_STAT))
   data = *InData;

   #if INTERRUPTS
   /* Release Fifo, Enable Conversion, and Enable Fifo Half Full Intr */
      *Control2 = CR_FIFO_HFULL_INT_ENA | CR_RELEASE_FIFO |
                  CR_START_CONVERSION;
   #endif
```


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A.3 **p4275.c** (continued)

```
   while(1)
   {
      #if POLLING
         /* wait for input fifo half full */
         while((*Control2 & (CR_LFIFO_HFULL_STAT | CR_HFIFO_HFULL_STAT))!=
               (CR_LFIFO_HFULL_STAT | CR_HFIFO_HFULL_STAT));

         /* Read out the Half the Fifo */
         for(i=0;i<num_samples;i++)
         {
            sig1[i] = *InData;
            sig2[i] = *InData;
            sig3[i] = *InData;
            sig4[i] = *InData;
         }
      #else
      ;
      #endif
   }
}

delay(unsigned long count)
{
   unsigned long i;

   for(i=0;i<count;i++);
}

void c_int01()
{
   unsigned int temp;
   unsigned int i;

   /* Read out the Half the Fifo */
   for(i=0;i<num_samples;i++)
   {
      sig1[i] = *InData;
      sig2[i] = *InData;
      sig3[i] = *InData;
      sig4[i] = *InData;
   }

   /* Read Status Register to clear Interrupt */
   temp = *Control2;

   /* Clear Processor Interrupt */
   clearInterrupt();

   ++counter;
}
```


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A.4 mod.h

```
/* mod.h -  This file determines the MIX Module's base address based on
            the processor which is running the program, the MIX
            Baseboard, and the MIX stack position being addressed.

   Note: This file only supports the following DSP processor boards:
         4283          4254             4257
         4284          4270             4285

   Defining the Baseboard:
      Set the appropriate BB_42XX constant to a 1 and the others to 0

   Running programs on a 4270, 4254, or 4257 Mix Module
      Set the MM_4270 constant if processor is on the 4270
      Set the MM_425X constant if processor is on the 4257

   Running program on the 4285, 4284 or 4283
      Clear the MM_4270 and MM_425X constants

   Specifying the MIX Module stack position of Mix Module being addressed
      For Mix stack position 0, set MOD to MOD0_ADDR
      For Mix stack position 1, set MOD to MOD1_ADDR
      For Mix stack position 2, set MOD to MOD2_ADDR

   Running programs on the 4283 Mix Baseboard(Setting the Page Register)
      To select Mix stack position 0, set MOD_SELECT to MOD0_SELECT
      To select Mix stack position 1, set MOD_SELECT to MOD1_SELECT
      To select Mix stack position 2, set MOD_SELECT to MOD2_SELECT */

/* Define BaseBoard Type */
#define BB_4283             0
#define BB_4284             0
#define BB_4285             1
#define BB_4200             0
#define BB_4201             0
#define BB_4202             0

/* Define Mix Module Type - Only if program is to be executed
                            on a Mix Module Processor */
#define MM_4270             0
#define MM_425X             1

/* Specify Mix Module Position of module being addressed */
#define MOD                 MOD1_ADDR

#if MM_4270 | MM_425X
   /* Specify MIX STACK Position for the 4270 or 425X processor boards */
   #define MIX_POS          0
#endif

#if BB_4283
   /* The 4283 Selects the Mix Module being addressed with a Page Register */
   #define MOD_SELECT       MOD1_SELECT
#else
   #define MOD_SELECT       MOD    /* Only being set to keep code similar */
#endif
```


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A.4 **mod.h** (continued)

```
#if BB_4285
   /* The 4285 has 2 independent paths for accessing the MIX bus resources:
      The Expansion Bus and the Global I/O bus.

      Note: The Expansion Bus may be mastered by any of the on-card 'C40
            processors or by off-card VMEbus masters.  The Global I/O Bus
            can be mastered only by 'C40 processors A, B, E or F.

      Note: MIX interrupts are not supported over the Global I/O Bus */

   #define EXP_BUS          1
   #define GLOB_BUS         0
#endif

/* BaseBoard = 4283 - This BaseBoard does not support Upper Mix Bus Masters */
#if BB_4283
   /* The 4283 Baseboard uses a page register to select which Mix Module
      is being accessed */
   #define  MOD0_SELECT     0x18000
   #define  MOD1_SELECT     0x10000
   #define  MOD2_SELECT     0x8000

   #define  MOD0_ADDR       0x00804000
   #define  MOD1_ADDR       0x00804000
   #define  MOD2_ADDR       0x00804000

   /* Some Mix Modules require the setting of Address Bit 27   */
   /* This is selected in the Page Register for this baseboard */
   #define D17_DATA_BIT        0x00020000

   /* Address Bit in address which corresponds to A27 -
      This is unused by 4283 */
   #define A27_ADDR_BIT     0x00000000

#endif
```


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A.4 **mod.h** (continued)

```
/* BaseBoard = 4284 */
#if BB_4284

   #if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257 */

      #define MOD0_ADDR    0xC0000000
      #define MOD1_ADDR    0xC4000000
      #define MOD2_ADDR    0xC8000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT 0x02000000

   #else                   /* No Mix Module */

      #define MOD0_ADDR    0x20000000
      #define MOD1_ADDR    0x24000000
      #define MOD2_ADDR    0x28000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT 0x02000000
   #endif

#endif

/* BaseBoard = 4200 or 4201 */
#if BB_4200 | BB_4201

   #if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257 */

      #define MOD0_ADDR    0xF0000000
      #define MOD1_ADDR    0xF4000000
      #define MOD2_ADDR    0xF8000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT 0x02000000

   #else                   /* No Mix Module */

      #define MOD0_ADDR    0xC0000000
      #define MOD1_ADDR    0xD0000000
      #define MOD2_ADDR    0xE0000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT 0x02000000
   #endif

#endif
```


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A.4 **mod.h** (continued)

```
/* BaseBoard = 4202  */
#if BB_4202

   #if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257 */

      #define MOD0_ADDR     0xC0000000
      #define MOD1_ADDR     0xC4000000
      #define MOD2_ADDR     0xC8000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT  0x02000000
   #endif

#endif


/* BaseBoard = 4285 */
#if BB_4285

   #if MM_4270 | MM_425X    /* Mix Module = 4270, 4254, or 4257 */
      #define MOD0_ADDR     0xC0000000
      #define MOD1_ADDR     0xC4000000
      #define MOD2_ADDR     0xC8000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT      0x02000000

   #else                    /* No Mix Module */

      #if EXP_BUS
         #define MOD0_ADDR     0x90000000
         #define MOD1_ADDR     0x90200000
         #define MOD2_ADDR     0x90400000

         /* Address Bit in address which corresponds to A27 */
         #define A27_ADDR_BIT  0x00100000
      #endif

      #if GLOB_BUS
         #define MOD0_ADDR     0xC8000000
         #define MOD1_ADDR     0xC8200000
         #define MOD2_ADDR     0xC8400000

         /* Address Bit in address which corresponds to A27 */
         #define A27_ADDR_BIT  0x00100000
      #endif

   #endif

#endif
/************************** End of File ****************************/
```


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A.5 init.c

```
#include "mod.h"

board_init(){
   #if BB_4284 | BB_4285
      /* The bootcode initializes the timer to interrupt the CPU
         periodically to flash the LED on the front panel.  Turn off
         the timer to prevent unwanted interrupts. */
      *(unsigned long *) 0x100020 = 0;     /* Turn off timer 0 */
   #endif

   #if BB_4285 & !(MM_4270 | MM_425X)
      /* Clear 4285 interrupt routing register */
      *(unsigned long *) 0x90600001 = 0;

      /* Setup 4285 Mix Control Register for compressed mode and release
         when done. Compressed mode allows you to avoid having to set a
         page register when accessing MIX modules.  Release when done
         prevents the C40 from hogging the MIX Bus. */
      #if EXP_BUS
         *(unsigned long *) 0x90600000 = 0x2;
      #endif

      #if GLOB_BUS
         *(unsigned long *) 0xC8600000 = 0x2;
         *(unsigned long *) 0xC8600001 = 0;
      #endif
   #endif

   #if MM_425X
      /* Set the release when done bit. This will prevent the C40 from
         hogging the MIX Bus. */
      *(unsigned int *) 0x82000001 = 0x40;    /* Release when done */
   #endif

   #if MM_4270
      /* The 4270 can provide an interrupt to the CPU when it can not
         obtain a shared resource.  Disabling this feature will force the
         C40 to wait for the shared resource to be freed up. */
      *(unsigned int *) 0x34000d = 0xff;      /* Disable NMI generation */
   #endif
}
```


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A.6 intr.c

```
#include "mod.h"

unsigned int    *int01_vector;
extern int      c_int01();

/* This Routines decides from the Information contained in mod.h */
/* which Mix Interrupt should be enabled by the processor        */
void enableInterrupts()
{
   #if BB_4283
      /* If the MOD_SELECT value used to select each MIX Module    */
      /* Position matches, then enable the corresponding Interrupt */
      if (MOD_SELECT == MOD0_SELECT)
         Init1();
      else if (MOD_SELECT == MOD1_SELECT)
         Init2();
      else
         Init3();
   #endif

   #if BB_4285 & !(MM_4270 | MM_425X)
      /* The 4285 Uses IIOF3 for all MIX modules       */
      Init3();
   #endif

   #if BB_4284 & !(MM_4270 | MM_425X)
      /* If the Base Address used to address each MIX Module       */
      /* Position matches, then enable the corresponding Interrupt */
      if (MOD == MOD0_ADDR)
         Init1();
      else if (MOD == MOD1_ADDR)
         Init2();
      else
         Init3();
   #endif
```


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A.6 **intr.c** (continued)

```
   #if MM_4270 | MM_425X
      /* Based on the position of the 4270 or 425X Mix Modules    */
      /* and position of the mix module generating the interrupts */
      /* enable the corresponding Interrupt                       */
      if (MIX_POS == 0)
      {
         if (MOD == MOD1_ADDR)
            IntInit2();
         else
            IntInit3();
      }
      else if (MIX_POS == 1)
      {
         if (MOD == MOD0_ADDR)
            IntInit3();
         else
         IntInit2();
      }
      else
      {
         if (MOD == MOD0_ADDR)
            IntInit2();
         else
            IntInit3();
      }

      #if BB_4200 | BB_4201
         /* If the BaseBoard is a 4200 or 4201, Disable the VIC Local
            Interrupt Control Registers from responding to the MIX
            Interrupt generated from the Mix Module */
         if (MOD == MOD0_ADDR)
            *(unsigned long *) 0xffff0009 = 0x80;
         else if (MOD == MOD1_ADDR)
            *(unsigned long *) 0xffff000a = 0x80;
         else
            *(unsigned long *) 0xffff000b = 0x80;
      #endif

   #endif
}
```


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A.6 **intr.c** (continued)

```
void clearInterrupt()
{
   #if MM_4270 | MM_425X | BB_4284 | BB_4285
      asm("   iack @0");     /* Clear Any Pending Interrupts */
   #endif

   #if BB_4283
      if (MOD_SELECT == MOD0_SELECT)
         *(int *)0x800000 = 0x0c;  /* Acknowledge 4283 interrupt processor */
      else if (MOD_SELECT == MOD1_SELECT)
         *(int *)0x800000 = 0x0a;  /* Acknowledge 4283 interrupt processor */
      else
         *(int *)0x800000 = 0x06;  /* Acknowledge 4283 interrupt processor */

      asm("       NOP");
      *(int *)0x800000 = 0x0e;    /* Re-arm 4283 interrupt processor   */

      asm("    LDI 0,IF");        /* Clear out any spurious interrupts */
      asm("    LDI 0,IF");        /* Clear out any spurious interrupts */
   #endif
}


#if BB_4283 | BB_4284 | BB_4285
void Init1()
{
   #if BB_4283
      /* setup int 1 vector jump */
      *(int *)0x809804 = (int)&c_int01 | 0x60000000;

      *(int *)0x800000 = 0x00;    /* Arm IACK Pal */
      asm("NOP");
      *(int *)0x800000 = 0x0e;

      /* enable interrupt 0 and 1 */
      asm("    LDI 0,IF");        /* Clear out any spurious interrupts */
      asm("    LDI 3,IE");
      asm("    OR 2000h,ST");
   #else
      /* Enable C40 Int 0 as MixInt0 */
      *(unsigned int *) 0x10000003 = *(unsigned int *) 0x10000003 |
                                        0x00000008;

      int01_vector = (unsigned int *) c_int01;
      asm("   LDEP IVTP,AR0");
      asm("   LDI @_int01_vector,R0");
      asm("   STI R0,*+AR0(3)");
      asm("   IACK @0");
      asm("   LDI IIF,R0");
      asm("   ANDN 000fH,R0");
      asm("   OR 0009H,R0");
      asm("   LDI R0,IIF");
      asm("   OR 2000H,ST");
   #endif
}
```


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A.6 **intr.c** (continued)

```
void Init2()
{
   #if BB_4283
      /* setup int 2 vector jump */

      *(int *)0x809808 = (int)&c_int01 | 0x60000000;

      *(int *)0x800000 = 0x00;        /* Arm IACK Pal */
      asm("NOP");
      *(int *)0x800000 = 0x0e;

      /* enable interrupt 0 and 2 */

      asm("   LDI 0,IF");        /* Clear out any spurious interrupts */
      asm("   LDI 5,IE");
      asm("   OR 2000h,ST");
   #else
      /* Enable C40 Int 2 as MixInt1 */
      *(unsigned int *) 0x10000003 = *(unsigned int *) 0x10000003 |
                                        0x00100000;

      int01_vector = (unsigned int *) c_int01;
      asm("   LDEP IVTP,AR0");
      asm("   LDI @_int01_vector,R0");
      asm("   STI R0,*+AR0(5)");
      asm("   IACK @0");
      asm("   LDI IIF,R0");
      asm("   ANDN 0f00H,R0");
      asm("   OR 0900H,R0");
      asm("   LDI R0,IIF");
      asm("   OR 2000H,ST");
   #endif
}
```


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A.6 **intr.c** (continued)

```
void Init3()
{
   unsigned int *IRR_85, *CR_85, proc_id, mod_pos;

   #if BB_4283
      /* setup int 3 vector jump */

      *(int *)0x80980c = (int)&c_int01 | 0x60000000;

      *(int *)0x800000 = 0x00;        /* Arm IACK Pal */
      asm("NOP");
      *(int *)0x800000 = 0x0e;

      /* enable interrupt 0 and 3 */

      asm("   LDI 0,IF");         /* Clear out any spurious interrupts */
      asm("   LDI 9,IE");
      asm("   OR 2000h,ST");
   #else
      #if BB_4284
         /* Enable C40 Int 3 as MixInt2 */
         *(unsigned int *) 0x10000003 = *(unsigned int *) 0x10000003 |
                                          0x20000000;
      #endif

      /* Setup 4285 Interrupt Routing Register based on the Processor ID
         and Mix module position */

      #if BB_4285
         IRR_85   = (unsigned int *)0x90600001;
         CR_85    = (unsigned int *)0x380000;

         proc_id  = (1 << (*CR_85 & 0x7)); /* Get Proc ID from 85 Control Reg */
         mod_pos  = (((MOD >> 20) & 0xF)*4);  /* Get Mod position from mod.h */

         /* Write to 4285 IRR using processor id shifted by the mod position */
         *(unsigned long *) IRR_85 = (proc_id << mod_pos);
      #endif

      int01_vector = (unsigned int *) c_int01;
      asm("   LDEP IVTP,AR0");
      asm("   LDI @_int01_vector,R0");
      asm("   STI R0,*+AR0(6)");
      asm("   IACK @0");
      asm("   LDI IIF,R0");
      asm("   ANDN 0f000H,R0");
      asm("   OR 09000H,R0");
      asm("   LDI R0,IIF");
      asm("   OR 2000H,ST");
   #endif
}
#endif
```


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A.6 **intr.c** (continued)

```
#if MM_4270 | MM_425X
void IntInit2()
{
   int01_vector = (unsigned int *) c_int01;
   asm("   LDEP IVTP,AR0");
   asm("   LDI @_int01_vector,R0");
   asm("   STI R0,*+AR0(6)");
   asm("   IACK @0");
   asm("   LDI IIF,R0");
   asm("   ANDN 0f000H,R0");
   asm("   OR 09000H,R0");
   asm("   LDI R0,IIF");
   asm("   OR 2000H,ST");
}


void IntInit3()
{
   int01_vector = (unsigned int *) c_int01;
   asm("   LDEP IVTP,AR0");
   asm("   LDI @_int01_vector,R0");
   asm("   STI R0,*+AR0(5)");
   asm("   IACK @0");
   asm("   LDI IIF,R0");
   asm("   ANDN 0f00H,R0");
   asm("   OR 0900H,R0");
   asm("   LDI R0,IIF");
   asm("   OR 2000H,ST");
}
#endif
```


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Appendix B: AKM Ak5393 A/D Converter

B.1 AKM Ak5393 Enhanced Dual Bit ΔΣ 96kHz 24-Bitt ADC

The following pages contains the AKM's Data Sheets for the Ak5393 Enhanced Dual Bit ΔΣ 96kHz 24-Bitt Analog to Digital Converter. The company's website is http://www.akm.com/.

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AK5393

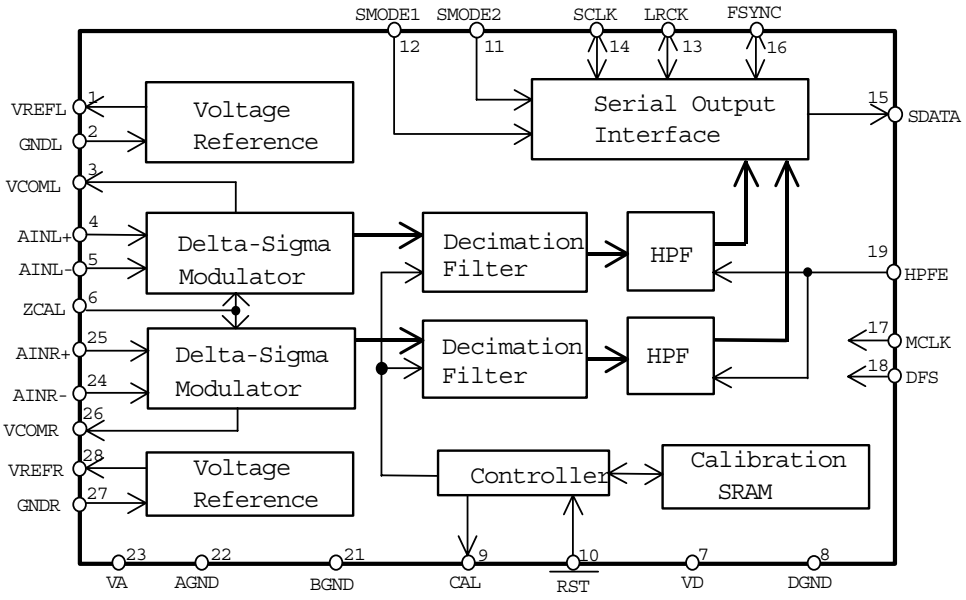
Enhanced Dual Bit ΔΣ 96kHz 24–Bit ADC

GENERAL DESCRIPTION

The AK5393 is a 24bit, 128x oversampling 2ch A/D Converter for professional digital audio systems. The modulator in the AK5393 uses the new developed Enhanced Dual Bit architecture. This new architecture achieves the wide dynamic range, while keeping much the same superior distortion characteristics as conventional Single Bit way. The AK5393 performs 117dB dynamic range, so the device is suitable for professional studio equipment such as digital mixer, digital VTR etc.

FEATURES

- Enhanced Dual Bit ADC
- Sampling Rate: 1kHz~108kHz
- Full Differential Inputs
- S/(N+D): 105dB
- DR: 117dB
- S/N: 117dB
- High Performance Linear Phase Digital Anti-Alias filter
  - Passband: 0~21.768kHz(@fs=48kHz)
  - Ripple: 0.001dB
  - Stopband: 110dB
- Digital HPF & Offset Calibration for Offset Cancel
- Power Supply: ±5V(Analog), 3~5.25V(Digital)
- Power Dissipation: 470mW
- Package: 28pin SOP
- AK5392 Pin compatible

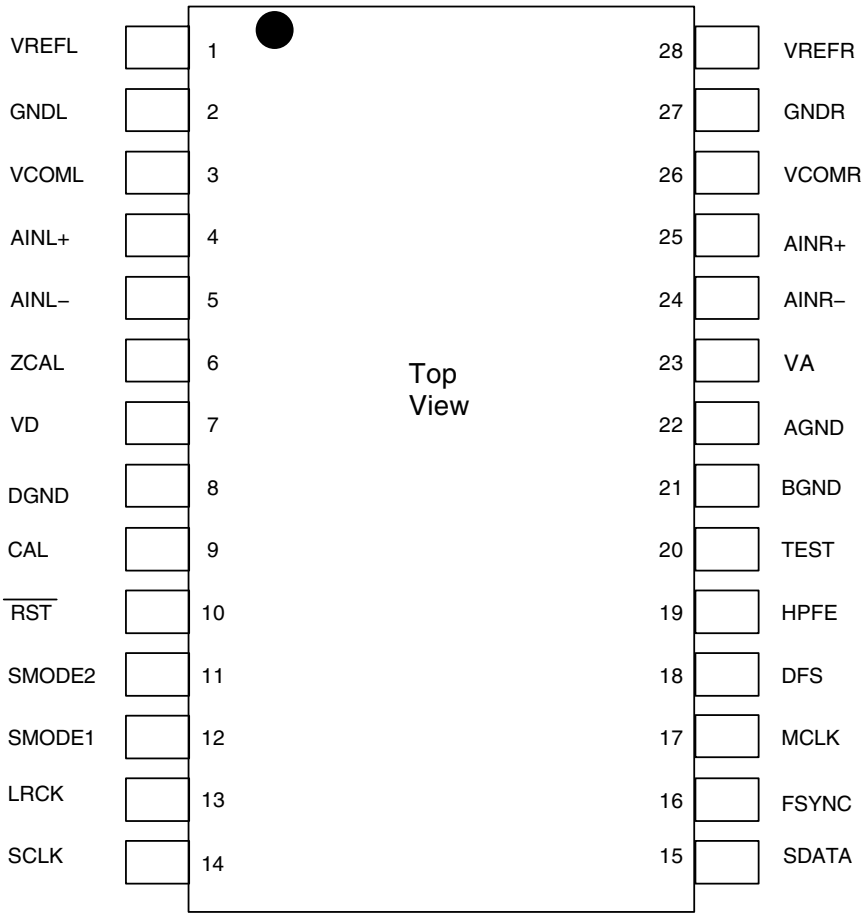


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■ Ordering Guide

AK5393-VS	–10 ~ +70°C	28pin SOP
AKD5393	AK5393 Evaluation Board	

■ Pin Layout



■ Compatibility with AK5392

	AK5392	AK5393
Pin 18	CMODE	DFS
fs (max)	54kHz	108kHz
MCLK (DFS ="L"@fs=48kHz)	256fs/384fs	256fs
MCLK (DFS ="H"@fs=96kHz)	N/A	128fs

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PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VREFL	O	Lch Reference Voltage Pin, 3.75V Normally connected to GNDL with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.
2	GNDL	-	Lch Reference Ground Pin, 0V
3	VCOML	O	Lch Common Voltage Pin, 2.75V
4	AINL+	I	Lch Analog positive input Pin
5	AINL-	I	Lch Analog negative input Pin
6	ZCAL	I	Zero Calibration Control Pin This pin controls the calibration reference signal. "L" :VCOML and VCOMR "H" : Analog Input Pins (AINL±, AINR±)
7	VD	-	Digital Power Supply Pin, 3.3V
8	DGND	-	Digital Ground Pin, 0V
9	CAL	O	Calibration Active Signal Pin "H" means the offset calibration cycle is in progress. Offset calibration starts when $\overline{\text{RST}}$ goes "H". CAL goes "L" after 8704 LRCK cycles for DFS="L", 17408 LRCK cycles for DFS ="H".
10	$\overline{\text{RST}}$	I	Reset Pin When "L", Digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up.
11 12	SMODE2 SMODE1	I I	Serial Interface Mode Select Pin MSB first, 2's compliment. SMODE2 SMODE1 MODE LRCK L L Slave mode : MSB justified : H/L L H Master mode : Similar to I^2S : H/L H L Slave mode : I^2S : L/H H H Master mode : I^2S : L/H
13	LRCK	I/O	Left/Right Channel Select Clock Pin LRCK goes "H" at SMODE2="L" and "L" at SMODE2="H" during reset when SMODE1 "H".

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14	SCLK	I/O	Serial Data Clock Pin Data is clocked out on the falling edge of SCLK. Slave mode: SCLK requires more than 48fs clock. Master mode: SCLK outputs a 128fs(DFS="L") or 64fs(DFS="H") clock. SCLK stays "L" during reset.
15	SDATA	O	Serial Data Output Pin MSB first, 2's complement. SDATA stays "L" during reset.
16	FSYNC	I/O	Frame Synchronization Signal Pin Slave mode: When "H", the data bits are clocked out on SDATA. In I^2S mode, FSYNC is don't care. Master mode: FSYNC outputs 2fs clock. FSYNC stays "L" during reset.
17	MCLK	I	Master Clock Input Pin 256fs at DFS="L", 128fs at DFS="H".
18	DFS	I	Double Speed Sampling Mode Pin "L": Normal Speed "H": Double Speed
19	HPFE	I	High Pass Filter Enable Pin "L": Disable "H": Enable
20	TEST	I	Test Pin (pull-down pin) Should be connected to GND.
21	BGND	-	Substrate Ground Pin, 0V
22	AGND	-	Analog Ground Pin, 0V
23	VA	-	Analog Supply Pin, 5V
24	AINR-	I	Rch Analog negative input Pin
25	AINR+	I	Rch Analog positive input Pin
26	VCOMR	O	Rch Common Voltage Pin, 2.75V
27	GNDR	-	Rch Reference Ground Pin, 0V
28	VREFR	O	Rch Reference Voltage Pin, 3.75V Normally connected to GNDR with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor

Note: All digital inputs should not be left floating.

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ABSOLUTE MAXIMUM RATINGS

(AGND,BGND,DGND=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	VA	-0.3	6.0	V
Digital	VD	-0.3	6.0	V
|BGND-DGND| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Analog Input Voltage	VINA	-0.3	VA+0.3	V
Digital Input Voltage	VIND	-0.3	VD+0.3	V
Ambient Temperature (power applied)	Ta	-10	70	°C
Storage Temperature	Tstg	-65	150	°C

Notes: 1. All voltages with respect to ground.
2. AGND, BGND and DGND must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND,BGND,DGND=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog	VA	4.75	5.0	5.25	V
(Note 3) Digital	VD	3.0	3.3	5.25	V

Notes: 1. All voltages with respect to ground.
3. The power up sequence between VA and VD is not critical.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

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ANALOG CHARACTERISTICS

(Ta=25°C; VA=5.0V; VD=3.3V; AGND,BGND,DGND=0V; fs=48kHz; Signal Frequency=1kHz;
24bit Output; Measurement frequency=10Hz~20kHz; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					24	Bits
Analog Input Characteristics:						
S/(N+D)	fs=48kHz	-1dBFS	98	105		dB
		-20dBFS	-	94		dB
		-60dBFS	-	54		dB
	fs=96kHz BW=40kHz	-1dBFS	96	103		dB
		-20dBFS	-	85		dB
		-60dBFS	-	45		dB
Dynamic Range (-60dBFS with A-Weighted)			112	117		dB
S/N (A-Weighted)			112	117		dB
Interchannel Isolation			110	120		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift					150	ppm/°C
Offset Error	after calibration, HPF=OFF			±200	±1000	LSB_{24}
	after calibration, HPF=ON			±1		LSB_{24}
Offset Drift (HPF=OFF)			-	±10	-	LSB_{24}/°C
Offset Calibration Range (HPF=OFF)				±50		mV
Input Voltage (AIN+)-(AIN-)			±2.3	±2.45	±2.6	V
Input Impedance			2.4	4		kΩ
Power Supplies						
Power Supply Current						
VA				90	130	mA
VD (fs=48kHz; DFS="L")				6	9	mA
(fs=96kHz; DFS="H")				9	14	mA
Power Dissipation				470	680	mW
Power Supply Rejection (Note 4)				70		dB

Note: 4. DC to 26kHz. 110dB(typ) beyond 26kHz.

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FILTER CHARACTERISTICS (fs=48kHz)

(Ta=25°C; VA=5.0V±5%; VD=3.0~5.25V; fs=48kHz, DFS="L")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband	(Note 5)	PB	0		21.768	kHz
Stopband	(Note 5)	SB	26.232			kHz
Passband Ripple		PR			±0.001	dB
Stopband Attenuation	(Note 6)	SA	110			dB
Group Delay Distortion		ΔGD		0		us
Group Delay	(Note 7)	GD		38.7		1/fs
ADC Digital Filter (HPF):						
Frequency response	(Note 5) -3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; VA=5.0V±5%; VD=3.0~5.25V; fs=96kHz, DFS="H")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband	(Note 5)	PB	0		43.536	kHz
Stopband	(Note 5)	SB	52.464			kHz
Passband Ripple		PR			±0.003	dB
Stopband Attenuation	(Note 8)	SA	110			dB
Group Delay Distortion		ΔGD		0		us
Group Delay	(Note 7)	GD		38.8		1/fs
ADC Digital Filter (HPF):						
Frequency response	(Note 5) -3dB	FR		2.0		Hz
	-0.1dB			13.0		Hz

Notes: 5. The passband and stopband frequencies scale with fs.

6. The analog modulator samples the input at 6.144MHz for an output word rate of 48kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 6.144MHz ± 21.768kHz, where n=1,2,3···).

7. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register. 40.7/fs(DFS="L"),40.8/fs(DFS="H")typ. at HPF:ON.

8. The analog modulator samples the input at 6.144MHz for an output word rate of 96kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 6.144MHz ± 43.536kHz, where n=1,2,3···).

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DIGITAL CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage Iout=-20µA	VOH	VD-0.1	-	-	V
Low-Level Output Voltage Iout=20µA	VOL	-		0.1	V
Input Leakage Current	Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Control Clock Frequency					
Master Clock 256fs:	fCLK	0.256	12.288	13.824	MHz
Pulse width Low	tCLKL	29			ns
Pulse width High	tCLKH	29			ns
Serial Data Output Clock (SCLK)	fSLK		6.144	6.912	MHz
Channel Select Clock (LRCK)	fs	1	48	108	kHz
duty cycle		25		75	%
Serial Interface Timing (Note 9)					
Slave Mode(SMODE1="L")					
SCLK Period	tSLK	144.7			ns
SCLK Pulse width Low	tSLKL	65			ns
Pulse width High	tSLKH	65			ns
SCLK falling to LRCK Edge (Note 10)	tSLR	-45		45	ns
LRCK Edge to SDATA MSB Valid	tDLR			45	ns
SCLK falling to SDATA Valid	tDSS			45	ns
SCLK falling to FSYNC Edge	tSF	-45		45	ns
Master Mode(SMODE1="H")					
SCLK Frequency (DFS="L")	fSLK		128fs		Hz
SCLK Frequency (DFS="H")	fSLK		64fs		Hz
duty cycle			50		%
FSYNC Frequency	fFSYNC		2fs		Hz
duty cycle			50		%
SCLK falling to LRCK Edge	tSLR	-20		20	ns
LRCK Edge to FSYNC rising	tLRF		1		tslk
SCLK falling to SDATA Valid	tDSS			45	ns
SCLK falling to FSYNC Edge	tSF	-20		20	ns
Reset/Calibration timing					
$\overline{\text{RST}}$ Pulse width	tRTW	150			ns
$\overline{\text{RST}}$ falling to CAL rising	tRCR			50	ns
$\overline{\text{RST}}$ rising to CAL falling (Note 11)	tRCF		8704		1/fs
$\overline{\text{RST}}$ rising to SDATA Valid (Note 11)	tRTV		8960		1/fs

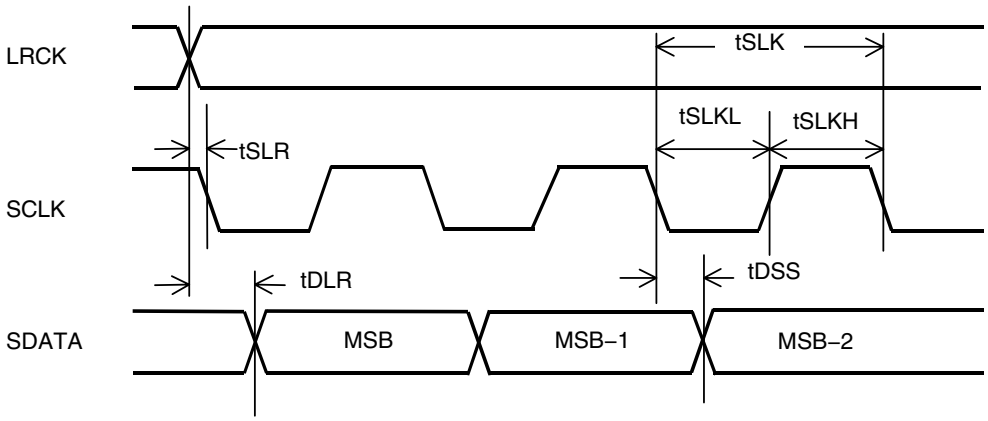
Notes: 9. Refer to Serial Data interface.

10. Specified LRCK edges not to coincide with the rising edges of SCLK.

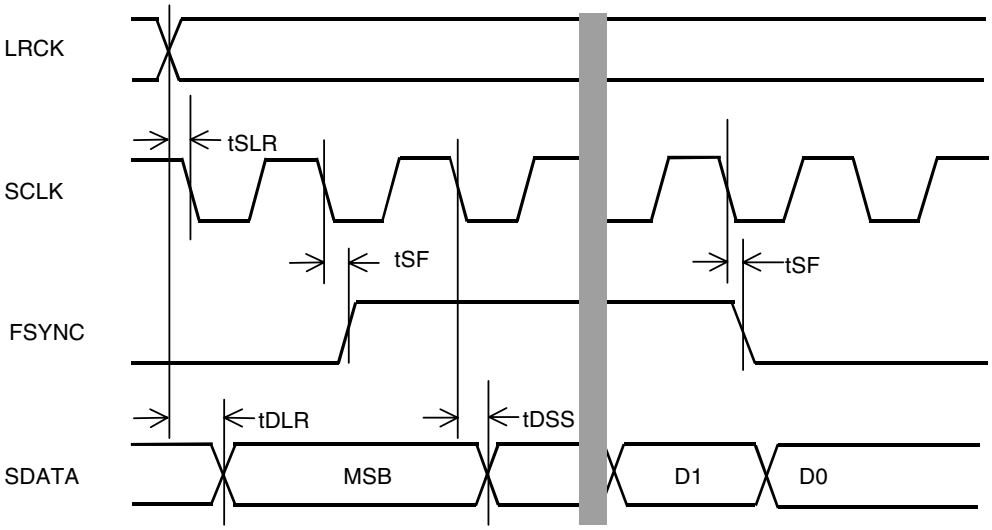
11. The number of the LRCK rising edges after $\overline{\text{RST}}$ brought high at DFS="L". The value is in master mode. In slave mode it becomes one LRCK clock(1/fs) longer. When DFS="H", tRCF=17408 and tRTV=17920.

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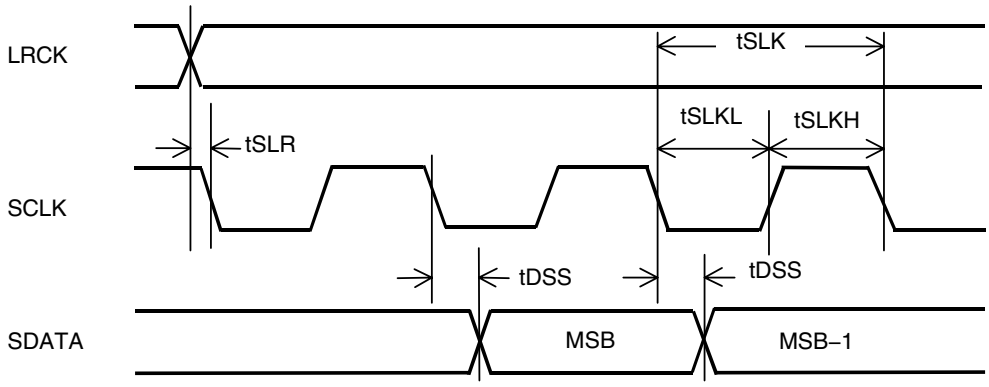
■ Timing Diagram



Serial Data Timing (Slave Mode, FSYNC="H")

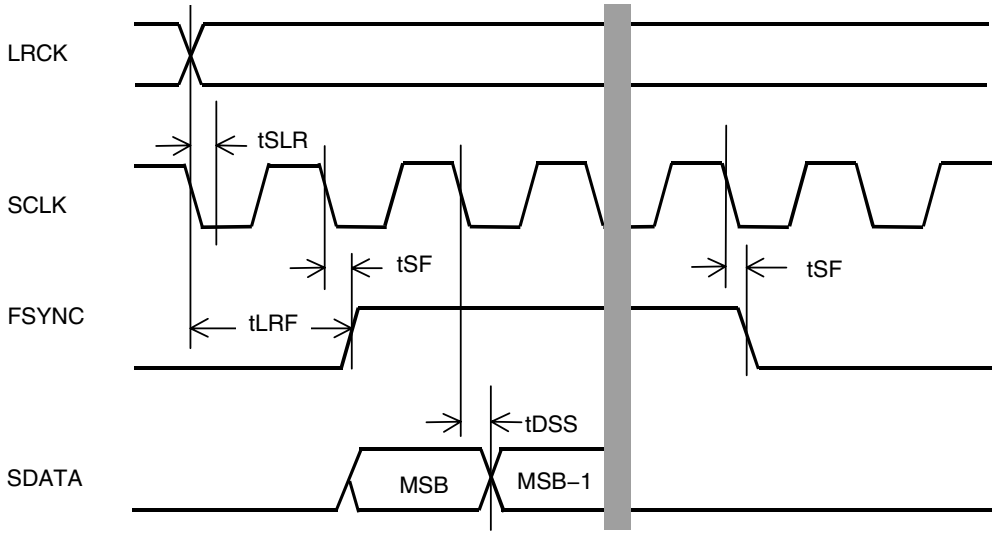


Serial Data Timing (Slave Mode)

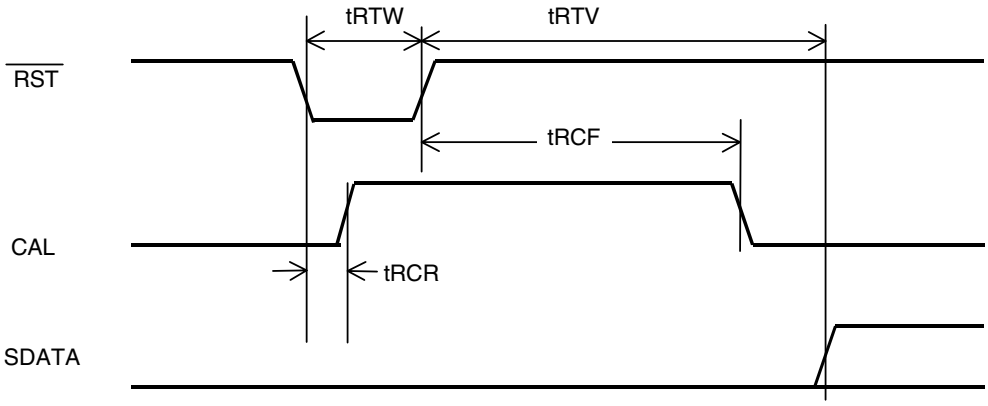


Serial Data Timing (I^2S Slave Mode, FSYNC = Don't Care)

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Serial Data Timing (Master Mode & I^2S Master Mode, DFS ="L")



Reset & Calibration Timing

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OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK5393 are MCLK, LRCK(fs), SCLK. MCLK should be synchronized with LRCK but the phase is free of care. MCLK should be 256fs in normal sampling mode(DFS="L") and double sampling mode needs 128fs as MCLK. Table 2 illustrates standard audio word rates and corresponding frequencies used in the AK5393.

As the AK5393 includes the phase detect circuit for LRCK, the AK5393 is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is only needed for power-up.

All external clocks must be present unless $\overline{\text{RST}}$ ="L", otherwise excessive current may result from abnormal operation of internal dynamic logic.

Speed	Normal(DFS ="L")	Double(DFS ="H")
LRCK (max)	54kHz	108kHz
SCLK	~128fs	~64fs
MCLK	256fs	128fs

Table 1. System Clocks

fs	MCLK	SCLK
32.0kHz	8.1920MHz	4.0960MHz
44.1kHz	11.2896MHz	5.6448MHz
48.0kHz	12.2880MHz	6.1440MHz
96.0kHz	12.2880MHz	6.1440MHz

Table 2. Examples of System Clock Frequency

■ Serial Data Interface

The AK5393 supports four serial data formats which can be selected via SMODE1 and SMODE2 pins(Table 3). The data format is MSB-first, 2's complement.

Figure	SMODE2	SMODE1	Mode	LRCK
Figure 1	L	L	Slave Mode	Lch = H, Rch =L
Figure 2	L	H	Master Mode	Lch =H, Rch =L
Figure 3	H	L	I^2S Slave Mode	Lch =L, Rch =H
Figure 4	H	H	I^2S Master Mode	Lch =L, Rch =H

Table 3. Serial I/F Format

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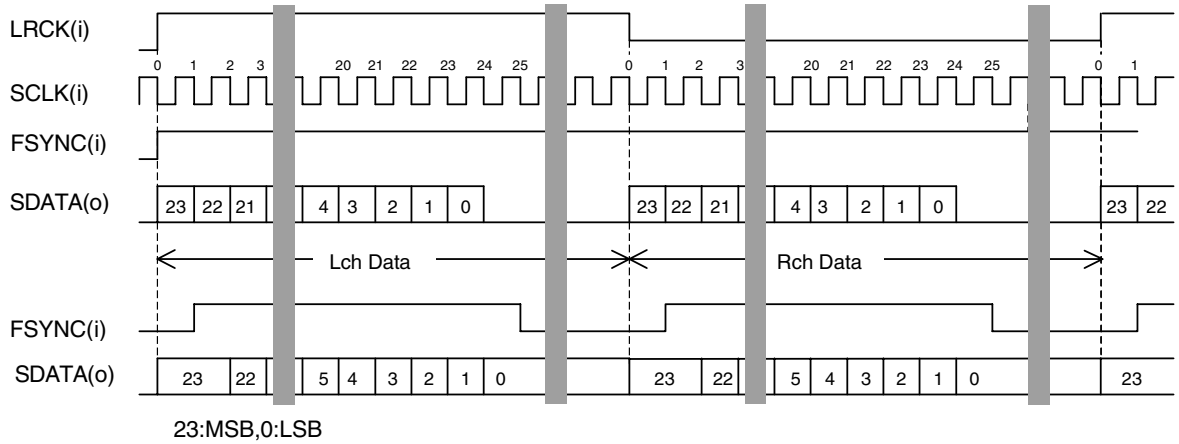


Figure 1. Serial Data Timing (Slave Mode)

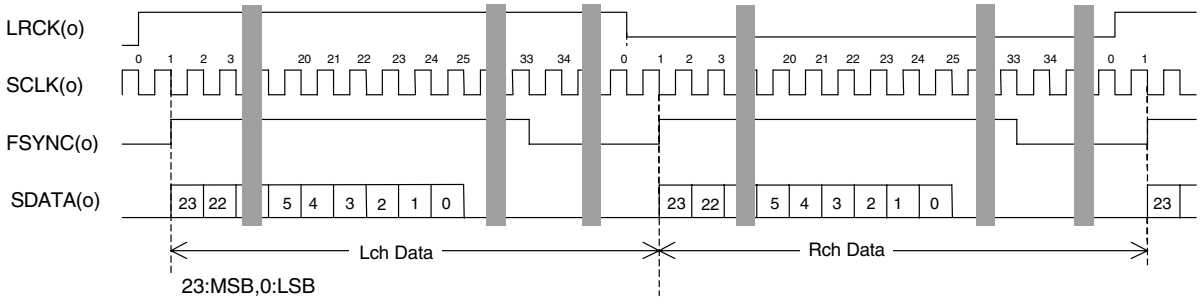


Figure 2. Serial Data Timing (Master mode, DFS="L")

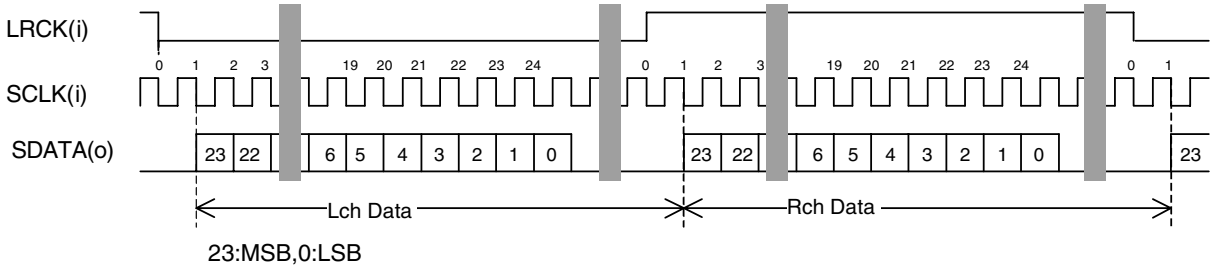


Figure 3. Serial Data Timing (I^2S Slave mode, FSYNC: Don't care.)

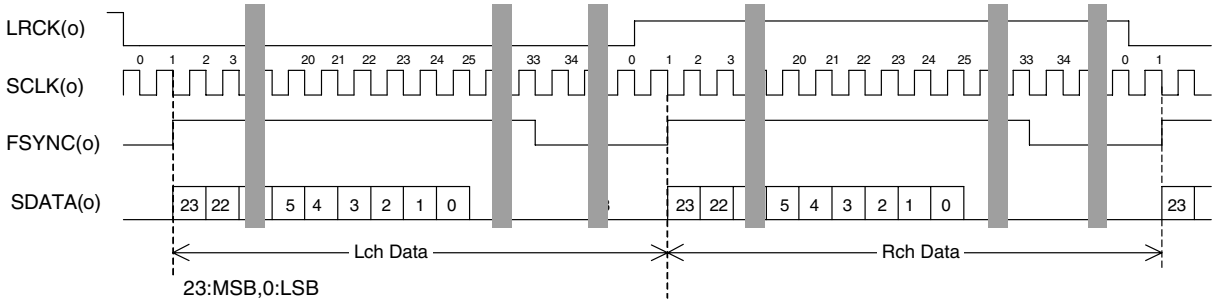


Figure 4. Serial Data Timing (I^2S Master mode, DFS="L")

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■ Offset Calibration

When $\overline{\text{RST}}$ pin goes to "L", the digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up.

During the offset calibration cycle, the digital section of the part measures and stores the values of calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AIN+/-) or the VCOM pins depending on the state of the ZCAL pin. With ZCAL "H", the analog input pin voltages are measured, and with ZCAL "L", the VCOM pin voltages are measured. The CAL output is "H" during calibration.

■ Digital High Pass Filter

The AK5393 also has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 1Hz at fs=48kHz and also scales with sampling rate(fs).

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SYSTEM DESIGN

Figure 5 and 6 show the system connection diagram. An evaluation board[AKD5393] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

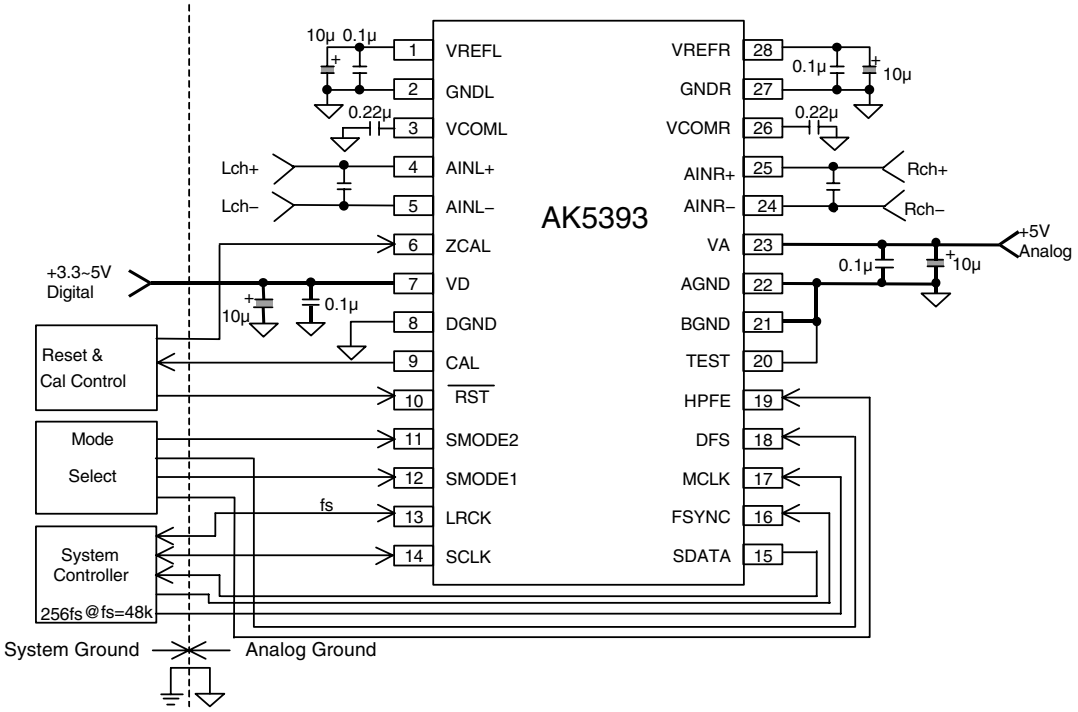


Figure 5. Typical Connection Diagram

Notes:

- LRCK = fs, SCLK=64fs.
- Power lines of VA and VD should be distributed separately from the point with low impedance of regulator etc.
- GND, BGND and DGND must be connected to the same analog ground plane.
- All input pins except pull-down/pull-up pins should not be left floating.

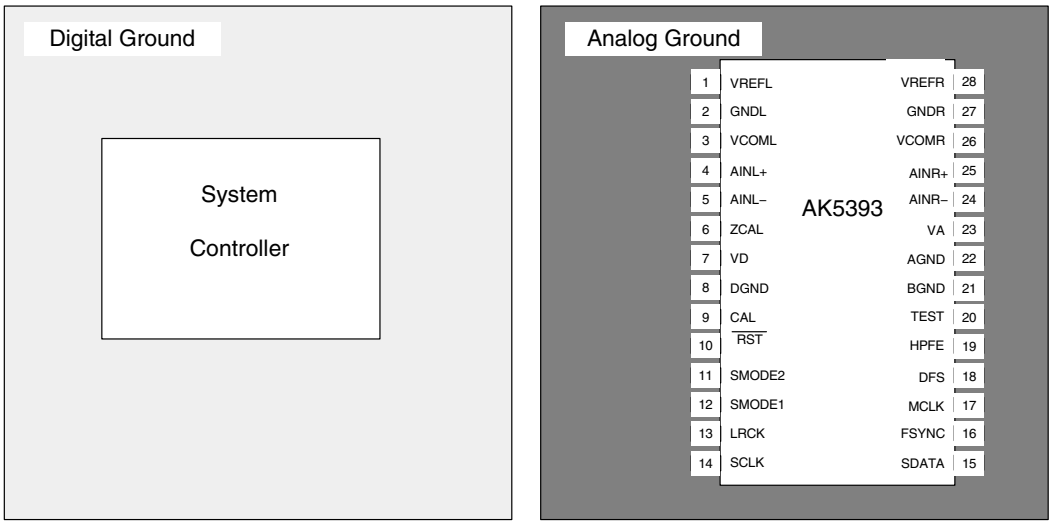


Figure 6 Ground layout

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1. Grounding and Power Supply Decoupling

The AK5393 requires careful attention to power supply and grounding arrangements. Analog ground and digital ground should be separate and connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5393 as possible, with the small value ceramic capacitor being the nearest.

2. On-chip voltage reference and VCOM

The reference voltage for A/D converter is a differential voltage between the VREFL/R output voltage and the GNDL/R input voltage. The GNDL/R are connected to AGND and a 10µF electrolytic capacitor parallel with a 0.1µF ceramic capacitor between the VREFL/R and the GNDL/R eliminate the effects of high frequency noise. Especially a ceramic capacitor should be as near to the pins as possible. And all digital signals, especially clocks, should be kept away from the VREFL/R pins in order to avoid unwanted coupling into the AK5393. No load current may be taken from the VREFL/R pins.

VCOM is a common voltage of the analog signal. In order to eliminate the effects of high frequency noise, a 0.22µF ceramic capacitor should be connected as near to the VCOM pin as possible. And all signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5393. No load current may be drawn from the VCOM pin.

3. Analog Inputs

Analog signal is differentially input into the modulator via the AIN+ and the AIN- pins. The input voltage is the difference between AIN+ and AIN- pins. The full-scale of each pin is nominally ± 2.45Vpp(typ). The AK5393 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFFH(@24bit) for input above a positive full scale and 800000H(@24bit) for input below a negative full scale. The ideal code is 000000H (@24bit) with no input signal. The DC offset is removed by the offset calibration.

The AK5393 samples the analog inputs at 128fs(6.144MHz @fs=48kHz,DFS="L"). The digital filter rejects noise above the stop band except for multiples of 128fs. A simple RC filter may be used to attenuate any noise around 128fs and most audio signals do not have significant energy at 128fs.

The AK5393 accepts +5V supply voltage. Any voltage which exceeds the upper limit of VA+0.3V and lower limit of AGND-0.3V and any current beyond 10mA for the analog input pins(AIN+ /-) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution specially in case of using ±15V in other analog circuits.

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Figure 7shows an input buffer circuit example 1. This is a full-differential input buffer circuit with an inverted-amp (gain :-10dB). The capacitor of 10nF between AIN+ /- decreases the clock feed through noise of modulator, and composes a 1st order LPF(fc=360kHz) with 22ohm resistor before the capacitor. This circuit also has a 1st order LPF(fc=370kHz) composed of op-amp. In this example, the internal offset is removed by self calibration. The evaluation board should be referred about the detail.

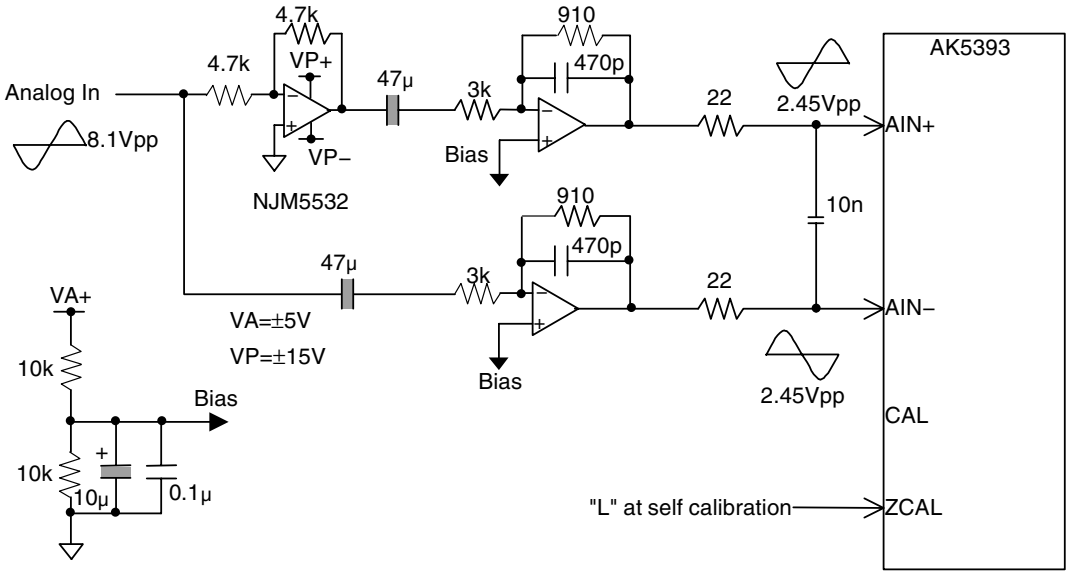


Figure 7 Differential Input Buffer Example 1

Figure 8 shows an input buffer circuit example 2. (1st order HPF; fc=0.66Hz, Table 4, 1st order LPF; fc=590kHz, gain=-14dB, Table 5). The analog signal is able to input through XLR or BNC connectors. (short JP1 and JP2 for BNC input, open JP1 and JP2 for XLR input). The input level of this circuit is +/-12.4Vpp (AK5393: +/-2.45Vpp Typ.).

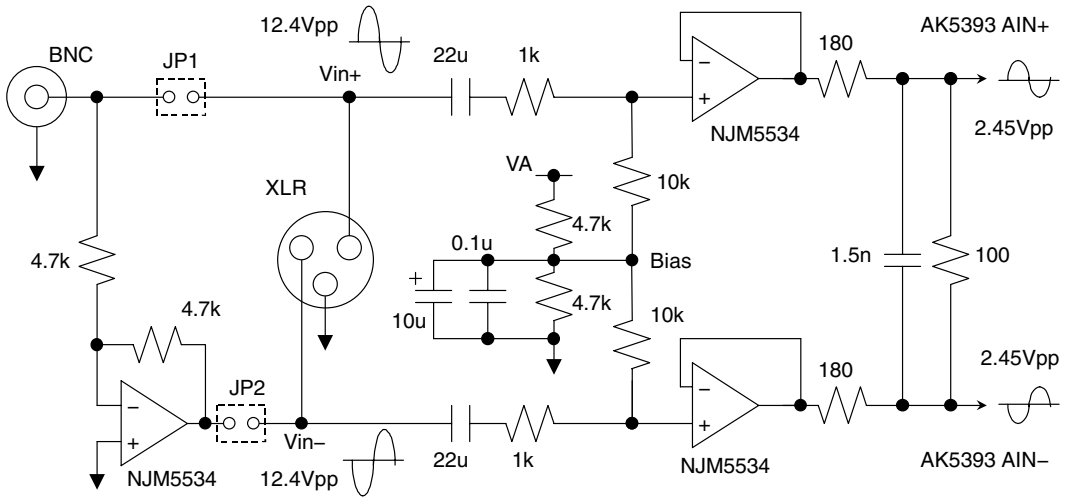


Figure 8 Differential Input Buffer Example 2

fin	1Hz	10Hz
Frequency Response	-1.56dB	-0.02dB

Table 4. Frequency Response of HPF

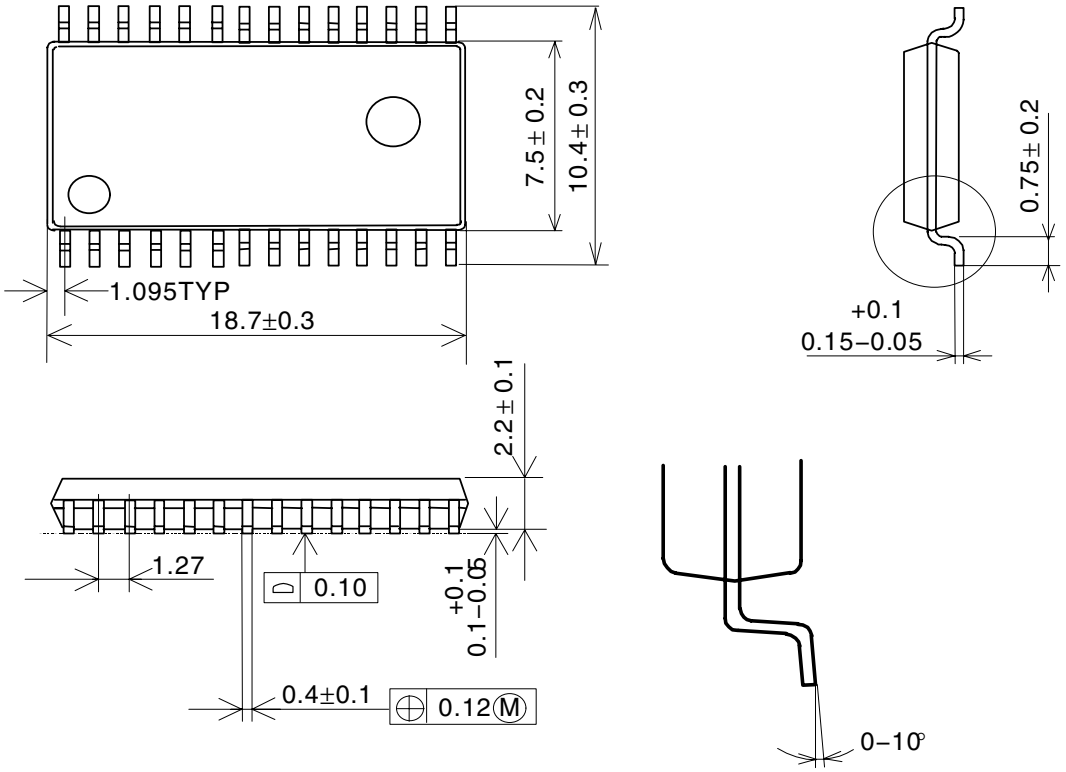
fin	20kHz	40kHz	6.144MHz
Frequency Response	-0.005dB	-0.02dB	-15.6dB

Table 5. Frequency Response of LPF

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PACKAGE

28pin SOP (Unit: mm)

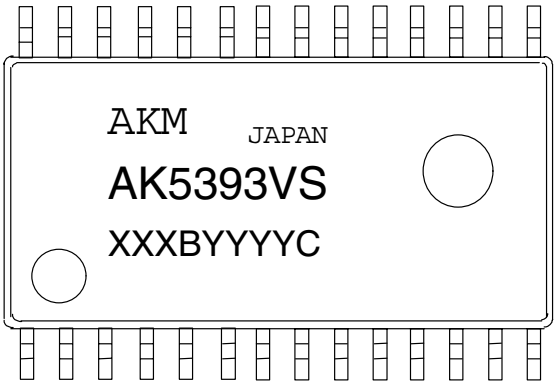


■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

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MARKING



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YYYYC:	Data Code (Y : numbers, C : alphabet)

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