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OPERATING MANUAL

MODEL 4283

TMS320C30 DSP-Based
MIX Baseboard for VMEbus Systems

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Pentek Model 4283 Operating Manual - Revision History

Date	Rev	Applicable Serial #'s	Comments
01/14/98	G	9405001 - Forward	Section 2.10 - Wire jumper is soldered to pins 2 and 3 of jumper block position J6; this prevents the unintentional selection of the internal ROM
01/26/98	G.1	9405001 - Forward	Section 3.6 - Previously stated that 'C30 Control Register is write only; corrected to state that it is Read/Write. Added - Section 7.10 Writing Programming Code to the EPROM Added - Appendix B -Model 4283 bootcode

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Chapter 1: Overview

1.1 Introduction

The Model 4283 Processor Board for VMEbus is based on the Texas Instruments TMS320C30 Floating Point Digital Signal Processor. It features the 32 MFlop TMS320C30 DSP chip, up to 8MBytes of dual-ported DRAM, 256 kBytes of high-speed SRAM, and 128 kByte of EPROM. An expansion connector utilizing the MIX bus supports a growing family of digital and analog I/O modules and co-processor expansion modules.

Since the Model 4283 may function as a VMEbus master and/or system controller, the TMS320C30 may access VMEbus resources simply by reading or writing to certain portions of its memory map. When installed in Slot 1, the Model 4283 can drive the system clock and reset signals and function as the bus arbiter. The DRAM on the Model 4283 is available as a VMEbus memory slave relocatable on 1, 4, or 8 Mbyte address boundaries.

This manual will describe the installation and operation of the Model 4283 in several typical VMEbus environments.

1.2 System Configuration

The Model 4283 can be tailored to many different types of systems. Here are a few of the typical application environments:

Stand-alone Processor	The Model 4283 can act as the main executive processor in the system. In this case the unit may contain executable code stored in EPROM and boot directly. Acting as a VMEbus master, it can access other devices on the VMEbus.
DSP & Data Acquisition Sub-System	When combined with the data acquisition, digital and analog I/O and co-processor MIX expansion modules, the Model 4283 can perform complete DSP, control, and communications functions. It can participate in a larger multi-master VMEbus system as a high-powered node.
Application Accelerator	With a VMEbus host operating system in place, such as MS-DOS, SUN UNIX, and other UNIX systems with C language support, the Model 4283 can act as an host application accelerator and as a pre-processor for the data acquisition expansion modules.

1.3 Software Development Support

No DSP hardware product offering is complete without a full complement of development software. Software products that support the Model 4283 are described on the next page.

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1.3 Software Development Support (continued)

SwiftTools	Pentek's SwiftTools is a complete software development environment for PC-AT and SUN workstations. It is tailored to work directly with Pentek's family of digital signal processing products which incorporate TMS320C40 and TMS320C30 digital signal processors. SwiftTools integrates all of the operations involved in a typical software development project and supports full C language source code generation and debugging with a comprehensive suite of powerful tools for a wide range of applications. SwiftTools includes an in-line assembler and dis-assembler for on-screen changes to object code in RAM. Registers can be examined and loaded, memory regions can be examined, filled, and moved. Full file uploading and downloading routines are provided and provisions for EPROM byte manipulation are included.
SwiftNet	Pentek's SwiftNet is a software product that supports a network of distributed VMEbus systems connected via Ethernet to a host computer, such as a SUN workstation or PC-AT. All software development tools are run on the host with remote target access provided transparently to the user. SwiftNet utilizes the industry standard TCP/IP interface for Ethernet, making it quite portable across many OS environments.
Macro	The assembler translates assembly language source code into machine language object files in common object file format (COFF). The linker section combines the COFF object files into an executable object module. The archiver supports a macro library accessible by the assembler.
C Compiler	The compiler is a full implementation of Kernighan and Ritchie C language, generating assembly language compatible with the Macro Assembler/Linker. Time critical assembly language routines are callable within the C program.
SPOX	SPOX is a real-time kernel operating system featuring a set of high-level C-callable routines for host system interfaces (standard I/O routines) and a complete DSP math library. SPOX speeds up program development and supports the development of real time applications written in C.
XDS-500	The Texas Instruments XDS500 Emulator allows the user to access the 'C30 through a 'back door' port provided by a special 12-pin connector on the board. The emulator board is installed in a PC/AT computer where all software development can take place.
Bus Adaptors	Pentek offers bus adaptors to provide a connecting link between the computer your 'C30 programs will be developed on and the VMEbus card cage where those programs will be run. Supported platforms include PC/AT compatibles, SUN SPARCStations and HP Workstations.

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1.4 Specifications

Processor: Texas Instruments TMS320C30

Processor Clock:
- Standard: 32 MHz
- Option 400: 40 MHz

Dual-Port DRAM:
- **Size:**
  - Standard: 256k x 32 (1 MByte)
  - Option 002: 1M x 32 (4 MBytes)
  - Option 007: 2M x 32 (8 MBytes)
- Arbitration: Hardware, fully transparent
- 'C30 Access: Memory mapped on primary bus - 3 wait states
- VMEbus Access: 1, 4 or 8 MBytes slave memory - Relocatable on 1 MByte boundaries - 250 ns cycle time

Static RAM:
- Size: 64k x 32 (256 kB)
- 'C30 Access: Memory mapped on primary bus - 0 wait states

EPROM:
- Size: 32K x 32 (128kB)
- 'C30 Access: Memory mapped on primary bus - 1 wait state

Expansion Bus:
- Type: Conforms to Intel MIX Bus Specification
- Width: 32-bits for data and address
- Speed: 11 MBytes/sec typical

XDS Connector: 12-pin Connector for Texas Instruments XDS-500 Emulator

Serial I/O Connector: Front Panel 17-pin connector for serial ports, timers, & flags

VMEbus Compliance:
- Bus Master: D32 A32 I(1-7) IH(1-7)
- Slave: D32 A32

Physical:
- Dimensions: 6U Eurocard - (160 mm x 233.35 mm)
  Multilayer construction.
- Power: + 5V DC @ 3 A max.
  +12V DC @ 0 A (passed through to MIX modules only)
  -12V DC @ 0 A (passed through to MIX modules only)

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1.5 Block Diagram

The block diagram of the Model 4283 is shown below. Each of the major elements will be described below. Each element which appears in the TMS320C30 address map has the 'C30 hex address shown next to it. The arrows show flow of data and/or control, depending on the function

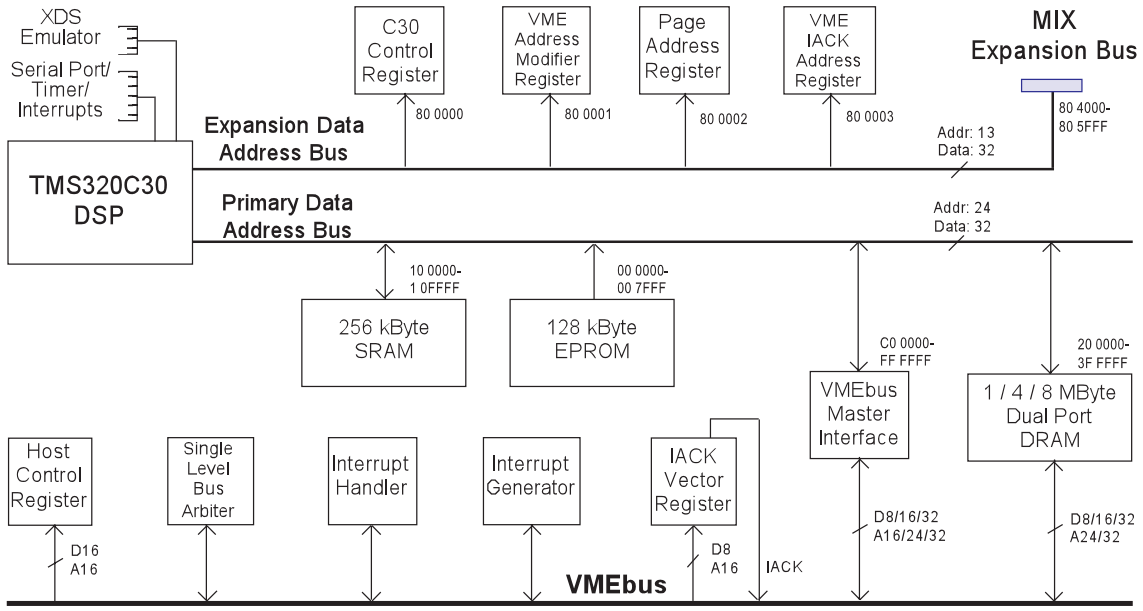


Figure 1-1: Model 4283 - Block Diagram

1.5.1 TMS320C30

The TMS320C30 processor is the central feature of the unit. It acts as the executive for all data transfers within the board, over the MIX expansion bus, and to the VMEbus. It also serves as a powerful 32 Mflop floating-point digital signal processor and a complete DMA controller which runs concurrently with the CPU. Other internal features of the 'C30 are: a 64 x 32 instruction cache, two 1k x 32 RAM's, eight extended precision registers, two address generators, two serial ports, two counter timers, and two general purpose I/O flags. The 'C30 has become an industry standard for floating point DSP applications and is widely supported with software products from various vendors.

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1.5 Block Diagram (continued)

1.5.2 Primary Data and Address Bus

This bus serves as the local data and address bus for the board. The 32-bit data bus connects the major board resources to the 'C30 including the SRAM, EPROM, DRAM, and the VMEbus Master Interface. The 24-bit address bus is sufficient for memory mapping all of these resources directly.

1.5.3 Expansion Bus

This 32-bit data bus serves as the path for the MIX expansion bus as well as four auxiliary registers: the C30 Control Register, the VME Address Modifier Register, VMEbus and MIXbus Page Register, and VMEbus IACK register. Its 13-bit address bus drives the lower 13-bits of the MIX bus for direct accessing of the MIX expansion modules.

1.5.4 Host Control Register

This register is addressable in A16 space on the VMEbus and controls reset and interrupt functions to the TMS320C30.

1.5.5 Single Level Bus Arbiter

When enabled, the Model 4283 can be placed in slot 1 and function as a VMEbus arbiter for bus requests on level 3.

1.5.6 Interrupt Handler

The Model 4283 will respond to VMEbus interrupts on any of 7 levels and interrogate the interrupt generator with interrupt acknowledge bus cycles.

1.5.7 Interrupt Generator and IACK Vector Register

The 'C30 can generate an interrupt on any of 7 levels on the VMEbus by setting a control register bit. The IACK Vector Register stores the ID byte which is sent over the bus in response to an IACK cycle.

1.5.8 Static RAM

The 256 kByte Static RAM is organized as 64k x 32 and features 0 wait state operation. It is ideal for program and data storage where fast access is required.

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1.5 Block Diagram (continued)

1.5.9 EPROM

The EPROM is organized as 32k x 32 and is implemented with four socketed 32k x 8 devices. These EPROM's may be removed from the unit and re-programmed for non-volatile program and data storage. By setting a jumper, the Model 4283 can begin executing a program from the EPROM.

1.5.10 VMEbus Master Interface

The Model 4283 can access data on the VMEbus by performing reads and writes in A16, A24, and A32 address space with data widths of 8, 16, and 32 bits. The bottom 24 bits are directly addressed by the TMS320C30 while the upper 8 bits are determined by the Page Register.

1.5.11 Dual Port DRAM

The dual port DRAM is available in sizes of 1, 4, and 8 MBytes. It is a organized with a 32-bit wide data field and can be accessed directly by both the TMS320C30 and the VMEbus. Full arbitration logic is employed on a cycle-to-cycle basis.

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Chapter 2: Installation

2.1 Introduction

This chapter contains information and instructions for the configuration and various modes of operation of the Model 4283. These are achieved by setting jumpers and switches on the board before it is installed in the VMEbus card cage.

The Model 4283 supports a number of expansion modules which are attached to the MIX stacking connector. These modules and the MIX interface system are described in Appendix A of this manual. It is recommended to wait until the Model 4283 has been successfully installed by itself before attaching any expansion modules since this would make access to the switches and jumpers more difficult.

Figure 2-2, on Page 16, is a component placement drawing of the Model 4283 PC Board, showing the switches and jumper blocks referred to in the sections below.

2.2 Selecting DRAM Memory Size

The dual-port DRAM appears as a VMEbus slave device at a base memory address selected by switches SW1 and SW2. The base address is the VMEbus address corresponding to the bottom (or lowest address) of the DRAM. Detailed instructions for setting these DRAM base address switches is contained in Section 4.4, Page 36.

The size of the DRAM is set at the factory and normally should not be changed. The three memory size options are 1M, 4M and 8 MB. The memory size configuration jumper s are shown for a 4 MB case in Figure 2-1, below.

Table 2-1: Model 4283 - Memory Size Jumpers

Memory Size	Jumpers Installed			SW1 Selections set to 'open'
1 MB	J1-3, 20	J1-2, 19	J1-1, 18	-
4 MB	J1-3, 20	-	-	SW1-1&2
8 MB	-	-	-	SW1-1, 2, &3

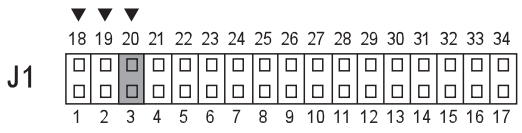


Figure 2-1: Model 4283 - Jumper Block J1 shown with jumpers installed for 4 MB Dram

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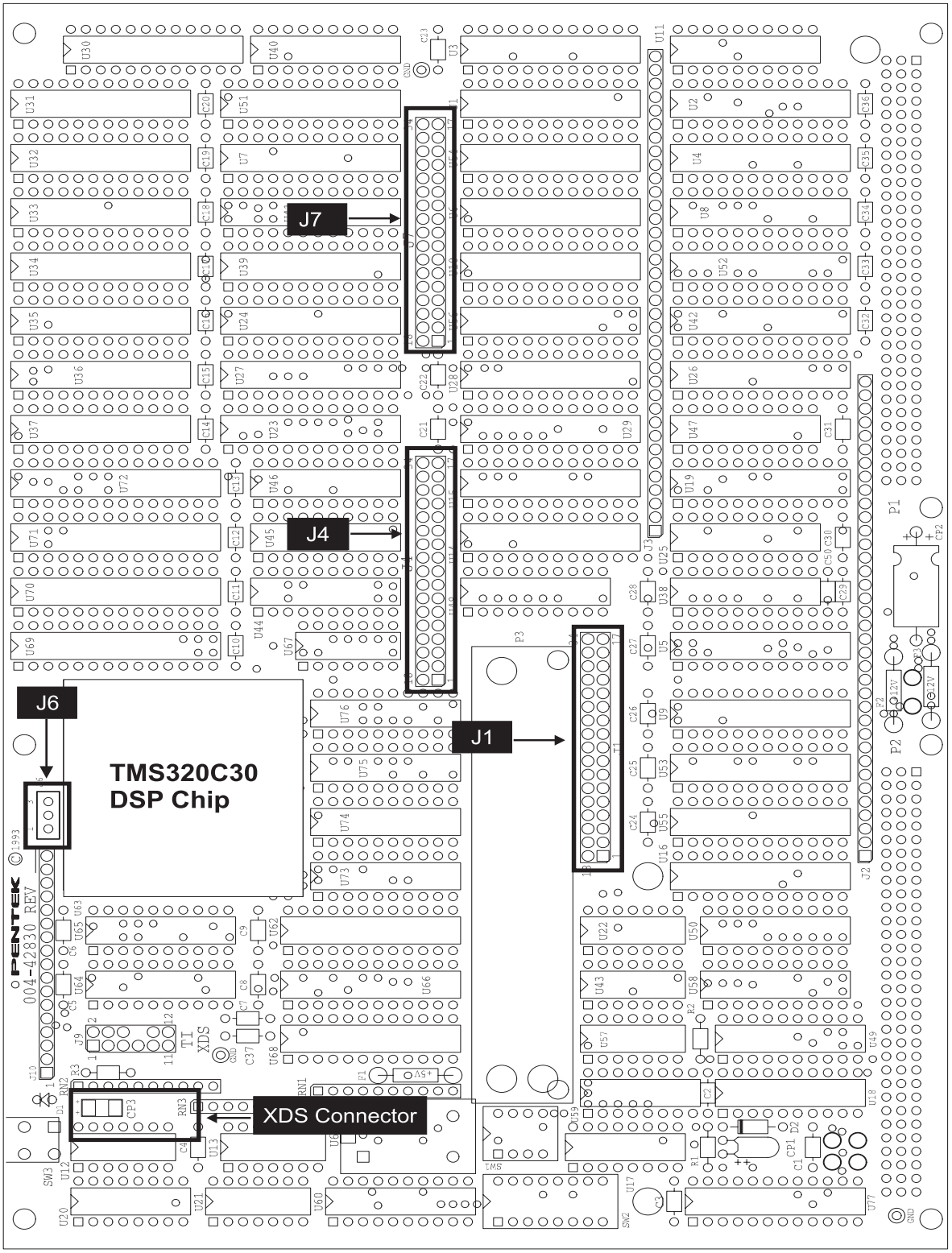


Figure 2-2: Model 4283 - Component, Switch and Jumper Block Placement

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2.3 Selecting the Host Control & IACK Vector Register Base Address

The Host Control Register allows a VMEbus Bus Master to control the reset and interrupt lines into the 'C30. The IACK Vector Register is an 8-bit register loaded from the VMEbus which stores a vector which the Model 4283 sends in response to an interrupt acknowledge cycle.

Both of these registers are mapped into the bottom 1k locations of 16-bit Address Space for AM Codes 29 and 2D. This corresponds to VMEbus Address 0x0000 through 0x03FF. This 1k region is divided into sixteen 64-byte locations, one of which is selected by setting four jumpers on jumper block J4. If there is more than one Model 4283 in a card cage, these jumpers must be set to uniquely configure a different base addresses for the 64-byte region on each board. This address will be called the A16_base address.

For any given board, the IACK Vector Register is mapped at the A16_base address and the Host Control Register is mapped at A16_base+0x0002. Table 2-2, below, defines the addresses of these registers for all 16 jumper configurations. Please refer to Section 4.5, Page 42, for more details.

Table 2-2: Model 4283 - Host Control Register and IACK Vector Register Address Jumpers

IACK Vector Register	Host Control Register	J4-12,29	J4-11,28	J4-10,27	J4-9,26
0000	0002	X	X	X	X
0040	0042		X	X	X
0080	0082	X		X	X
00C0	00C2			X	X
0100	0102	X	X		X
0140	0142		X		X
0180	0182	X			X
01C0	01C2				X
0200	0202	X	X	X	
0240	0242		X	X	
0280	0282	X		X	
02C0	02C2			X	
0300	0302	X	X		
0340	0342		X		
0380	0382	X			
03C0	03C2				

X = jumper installed

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2.3 Selecting the Host Control & IACK Vector Register Base Address (cont.)

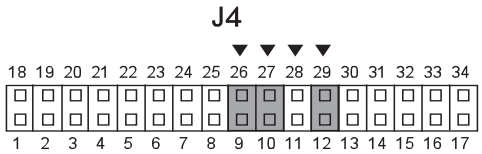


Figure 2-3: Model 4283 - A16_base Address jumpers Set for 0x0080

2.4 Selecting VMEbus Interrupter Level

As a VMEbus Interrupter, the Model 4283 can generate interrupts to the VMEbus. Besides driving one of the bus interrupt lines low, an interrupter must also respond to an interrupt acknowledge bus cycle (IACK cycle). This requires that the interrupter recognizes a 3-bit IACK address and sends an 8-bit IACK Vector over the data bus so that the interrupt handler can determine the identity of the requester. This 8-bit IACK Vector is programmable over the bus and is described in Figure 2-3 and Section 4.5.2, Page 43.

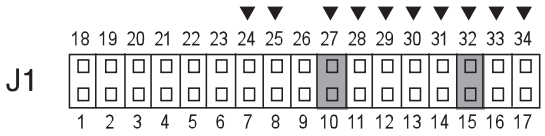


Figure 2-4: Model 4283 - Jumper block J1 shown with jumpers installed for interrupt requester level 3

These two requirements of an interrupter (driving an interrupt line and responding to an IACK cycle) are configured by setting two groups of jumpers. The IRQ jumpers determine which interrupt line is driven and the IACK Address jumpers determine the 3-bit IACK address. The two groups of jumpers must always agree in interrupt level. Note that only one interrupt level is permitted.

Table 2-3: Model4283 - IRQ and IACK Vector Address Jumpers

Int Level	IRQ Jumper	IACK Vector Address Jumpers
1	J1-17,34	J1-10,27 and J1-8,25
2	J1-16,33	J1-10,27 and J1-7,24
3	J1-15,32	J1-10,27
4	J1-14,31	J1-8,25 and J1-7,24
5	J1-13,30	J1-8,25
6	J1-12,29	J1-7,24
7	J1-11,28	none

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2.5 Selecting VMEbus Interrupt Handler Level

As a VMEbus Interrupt Handler, the Model 4283 can respond to any of nine interrupt sources: the 7 IRQ lines on the VMEbus, bit 1 of the Host Control Register and the VMEbus Timeout Interrupt.

Jumper block J4 is used to select which interrupt sources drive the INT0 pin of the TMS320C30. Up to four interrupts can be connected at a time: one from each of the four groups shown in Table 2-4. Group 1 includes the Host Control Register Interrupt and VMEbus lines IRQ1 through IRQ7. Only one jumper can be connected at a time within Group 1. Groups 2 and 3 support IRQ6 and IRQ7. The VME Bus Timeout interrupt in Group 4 is always enabled and no jumpering is required.

Table 2-4: Model 4283 - VMEbus Interrupt Source Selection Jumpers

Interrupt Source	Jumper	Group	Notes
Host Central Reg	J4-1,18	1	Only One at a time
IRQ1	J4-2,19		
IRQ2	J4-3,20		
IRQ3	J4-4,21		
IRQ4	J4-5,22		
IRQ5	J4-6,23		
IRQ6	J4-7,24		
IRQ7	J4-8,25		
IRQ6	J4-13,30	2	
IRQ7	J4-14,31	3	
Bus Timeout	Always Enabled	4	

Jumper J4 is shown to the right configured for handling interrupts from four sources: the VMEbus timeout bit, the Host Control Register and VMEbus lines IRQ6 and IRQ7.

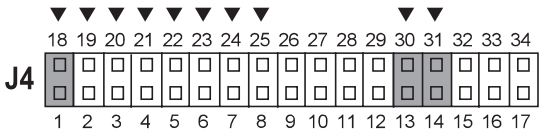


Figure 2-5: Model 4283 - Jumper Block J4 configured for Host Control Register,

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2.6 Selecting VMEbus Bus Request Level - Bus Master Interface

As a VMEbus Bus Master, the Model 4283 must request and acquire the use of the VMEbus on one of four possible request levels. Each time the TMS320C30 accesses the memory space corresponding to the VMEbus, a bus request cycle is conducted. This is accomplished by driving one of the four VMEbus lines, BRQ0 through BRQ3. A bus arbiter, located in slot 0 of the VMEbus cage, resolves requests for use of the bus, and asserts bus grant lines to enable access. (The Model 4283 may also serve as a bus arbiter when installed in slot 1. See Section 7.7, Page 62, through Section 7.9, Page 65, for further discussion.)

Table 2-5: Model 4283 - Bus Request Level Selection Jumpers

BRQ Level	Request Jumpers			Bypass Jumpers		
BRQ0	J7-3,20	J7-7,24	J7-8,25	J7-9,10	J7-11,12	J7-13,14
BRQ1	J7-4,21	J7-9,26	J7-10,27	J7-7,8	J7-11,12	J7-13,14
BRQ2	J7-5,22	J7-11,28	J7-12,29	J7-7,8	J7-9,10	J7-13,14
BRQ3	J7-6,23	J7-13,30	J7-14,31	J7-7,8	J7-9,10	J7-11,12

Jumper block J7 is used to select which one of the four bus request levels is used. Level 3 is the highest priority level. The Request Jumpers configure the board to act at the specified bus request level. The Bypass Jumpers bypass the bus grant signals for the other three bus requester levels. These jumpers are optional, depending upon backplane jumpers installed. See Section 7.9, Page 65.

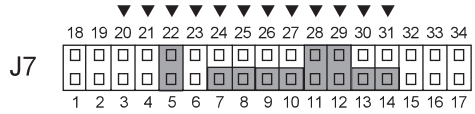


Figure 2-6: Model 4283 - Jumpers Installed for Bus Request level BRQ2

2.7 Selecting Bus Arbiter Operation - Level 3

The Model 4283 can act as a VMEbus bus arbiter on level 3 when installed in slot 1 of the VMEbus cage. The arbiter monitors the BBSY line, the BG3IN and BR0 - BR3 lines, and asserts the BG3OUT line when configured with the jumpers shown in Figure 2-7. (See Section 7.7, Page 62.

Table 2-6: Model 4283 - Bus Arbiter Jumpers Installed - Level 3

J7-6,23	J7-13,30	J7-14,31	J7-15,32
J7-7,8	J7-9,10*	J7-11,12*	

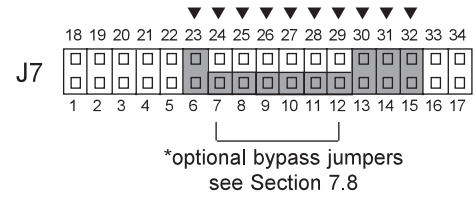


Figure 2-7: Model 4283 - J7 Configured for Bus Arbiter Operation

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2.8 SYSRST INPUT & OUTPUT Jumpers

If the Model 4283 is to drive the VMEbus SYSRST signal then jumper J7-2,19 must be installed as shown to the right (the SYSRST OUTPUT jumper). The reset signal will be asserted for approximately 1 msec when the appropriate bit in the 'C30 Control Register is set.

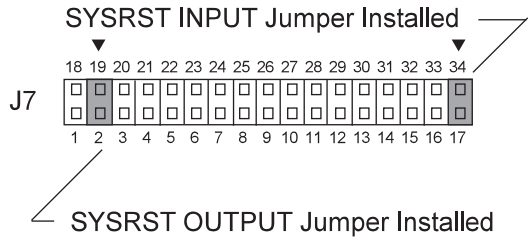


Figure 2-7: Model 4283 - SYSRST Jumpers

If the VMEbus SYSRST signal is to be used to reset the Model 4283, then jumper J7-17,34 must be installed (the SYSRST INPUT jumper). See Section 3.6.1, Page 27, for more discussion and a schematic of the SYSRST jumpers.

2.9 Driving VMEbus SYSCLK.

If the Model 4283 is to drive the VMEbus SYSCLK signal then jumper J7-1,18 must be installed. This will provide a 16 MHz clock to the VMEbus

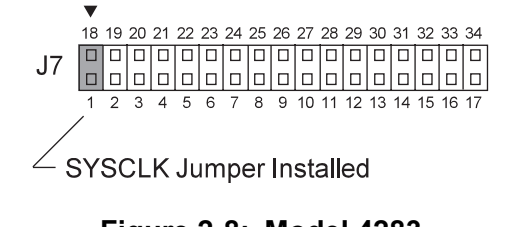


Figure 2-8: Model 4283 - SYSCLK Jumper

2.10 Selecting Internal ROM

To select the internal ROM of the TMS320C30 jumper J6-1,2. To select the external EPROM, jumper J6-2,3. Normally the Model 4283 will be operated in external EPROM mode with the jumper installed as shown to the right.

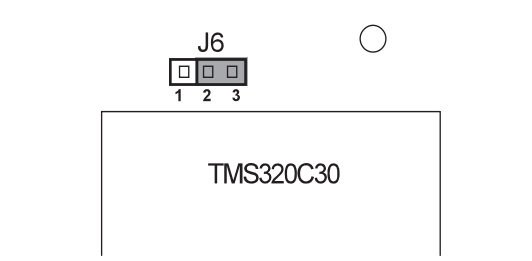


Figure 2-9: Model 4283 - ROM Jumper - External Mode Selected

In newer models (s\n 9405001 and higher) a wire jumper is soldered between pins 2 and 3. This feature prevents the unintentional selection of the internal ROM.

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2.11 Factory Default Jumper Settings

As shipped by the factory, the Model 4283 has the following default jumper settings:

DRAM Base Address: 0x0000 0000	EPROM Mode selected
Interrupt Requester Level: None	SYSCLK not driven
Interrupt Handler: Host Control Reg	SYSRST INPUT enabled
Bus Requester Level: 3	SYSRST INPUT enabled

Factory default jumper configurations for both the 1MB, 4MB and 8M DRAM options are shown in Figure 2-10, Figure 2-11 and Figure 2-11, below and on the next page.

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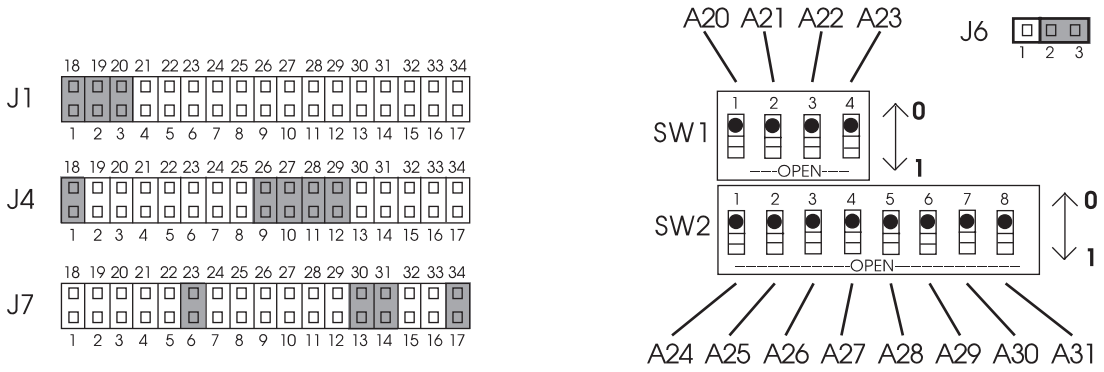


Figure 2-10: Model 4283 - Factory Default Jumpers (1 MB Dram Option)

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2.11 Factory Default Jumper Settings (continued)

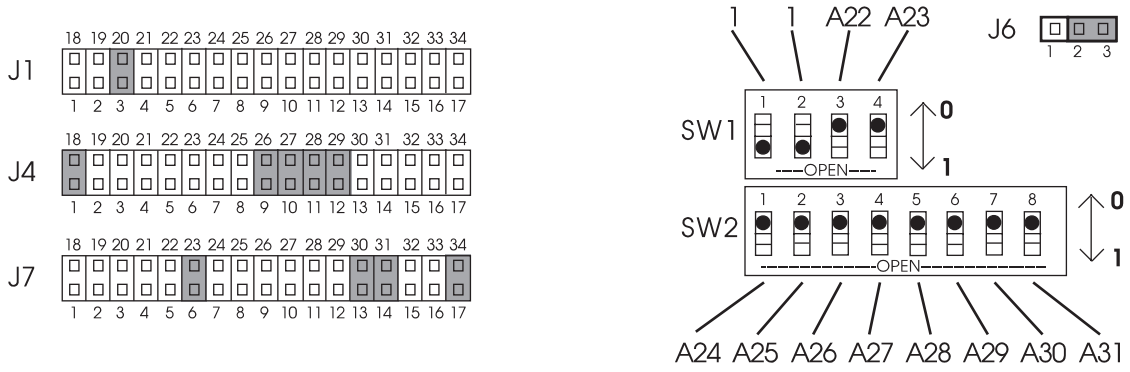


Figure 2-11: Model 4283 - Factory Default Jumpers (4 MB Dram Option)

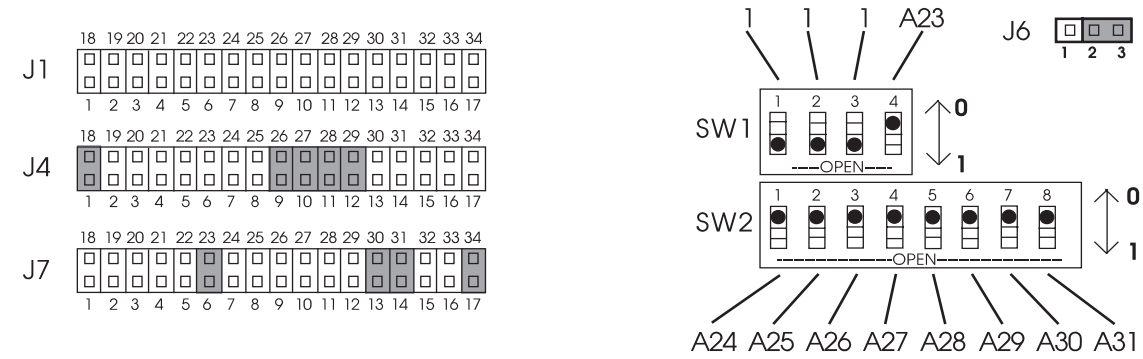


Figure 2-12: Model 4283 - Factory Default Jumpers (8 MB Dram Option)

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Chapter 3: TMS320C30 Memory Map

3.1 Introduction

There are two points of reference for memory resources of the Model 4283: the view from the TMS320C30 (referred to as the 'C30 Memory Map) and the view from the VMEbus (the VMEbus Memory Map). This chapter covers the 'C30 Memory Map and describes the various registers and memory resources and how they are accessed and utilized by TMS320C30. Chapter 4 of this manual will cover the VMEbus Memory Map.

3.2 TMS320C30 Memory Map

The 'C30 employs a 32-bit data bus and a 24-bit address bus, providing 16M locations. The address will be expressed throughout this manual as a 6-digit hexadecimal number, with a space between the first two and the second four digits for notational convenience, in the form 0x0012 3456. (The leading '0x' is common notation for a hex value in the 'C' programming language.) The 'C30 Memory Map is shown in Figure 3-2, on the next page. The shaded regions are redundant memory 'images' or reserved areas and, in general, should be avoided in programming. The memory 'images' are simply repetitions of the same 'base' memory address space. (Reads and writes to these regions will access the same memory resource as the base address.)

3.3 EPROM - 'C30 Address 0x0000 0000 through 0x0000 7FFF

The EPROM memory consists of four 32k x 8 UV erasable programmable read-only memories with 90 nsec access time. These EPROM's are mounted in sockets and can be removed for reprogramming. The four devices are identified by reference designations U69 through U72. The least significant byte of the 32-bit word is stored in U69 and the most significant byte in U72. Accesses to the EPROM by the 'C30 operates at cycle time of 122 nsec.

3.4 Static RAM - 'C30 Address 0x0010 0000 through 0x0010 FFFF

The Static RAM is a zero-wait-state memory organized as 64k x 32. Accesses by the 'C30 occur with cycles times of 61 nsec for reads, and 122 nsec for writes.

3.5 DRAM - 'C30 Address 0x0020 0000 through 0x003F FFFF

The DRAM is organized in three sizes depending upon the option ordered, as shown in Table 3-1. The DRAM is located on a daughtercard assembly and attached to the main board by two pin & socket connectors. Access time for both reads and writes is 250 nsec.

Table 3-1: Model 4283 Dram Organization

1 MB	256k x 32	0x0020 0000 to 0x0023 FFFF
4 MB	1MB x 32	0x0020 0000 to 0x002F FFFF
8 MB	2MB x 32	0x0020 0000 to 0x003F FFFF

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Table 3-2: TMS320C30 Memory Map

Address Range	Description			Section	Page
0x0000 0000 - 0x0000 7FFF	EPROM - 32k x 32			Section 3.3	Page 25
0x0000 8000 - 0x000F FFFF	31 Images of EPROM - Each 32k x 32				
0x0010 0000 - 0x0010 FFFF	STATIC RAM - 64k x 32			Section 3.4	Page 25
0x0011 0000 - 0x001F FFFF	15 Images of STATIC RAM - Each 64k x 32				
0x0020 0000 - 0x0023 FFFF	DRAM - 256k x 32 (1 MB DRAM)	DRAM - 1M x 32 (4 MB DRAM)	DRAM - 2M (8 MB DRAM)	Section 3.5 Section 4.3	Page 25 Page 36
0x0024 0000 - 0x002F FFFF	3 Images of DRAM Each 256k x 32				
0x0030 0000 - 0x003F FFFF	4 Images of DRAM Each 256k x 32	1 Image of DRAM 1M x 32			
0x0040 0000 - 0x007F FFFF	RESERVED				
0x0080 0000	'C30 CONTROL REGISTER			Section 3.5	Page 25
0x0080 0001	VMEbus ADDRESS MODIFIER REGISTER			Section 3.8	Page 31
0x0080 0002	PAGE ADDRESS REGISTER			Section 3.9	Page 32
0x0080 0003	VME JACK ADDRESS REGISTER			Section 3.10	Page 33
0x0080 0004 - 0x0080 07FF	RESERVED				
0x0080 0800	INTERRUPT STATUS REGISTER			Section 3.7	Page 31
0x0080 0801 - 0x0080 3FFF	RESERVED				
0x0080 4000 - 0x0080 5FFF	MIX BUS EXPANSION MODULES - 8k x32 Page			Section 5.3	Page 45
0x0080 6000 - 0x0080 7FFF	RESERVED				
0x0080 8000 - 0x0080 9FFF	C30 INTERNAL MEMORY MAPPED REGISTERS			Section 3.15	Page 34
0x0080 9800 - 0x0080 FFFF	C30 INTERNAL RAM			Section 3.12	Page 34
0x0080 A000 - 0x008F FFFF	VMEbus IACK CYCLE			Section 3.13	Page 34
0x0090 0000 - 0x00BF FFFF	RESERVED				
0x00C0 0000 - 0x00FF FFFF	VMEbus MASTER ACCESS -4M x 32Page - 16 MBytes			Section 3.14 Section 7.7	Page 34 Page 62

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3.6 TMS320C30 Control Register - Read/Write @ 'C30 Address 0x0080 0000

The 'C30 Control Register is a 9-bit read/write register, using the 9 least significant bits of the 32-bit data word. It provides several different control functions including reset, interrupt acknowledge, interrupts, bus lock, and bus cycle type. The bit definition is shown in Table 3-3, below.

Table 3-3: 'C30 Control Register - 'C30 Address 0x0080 0000

Bit	9	8	7	6	5	4	3	2	1	0
Name	TRSEL3	TRSEL2	LOCK	TRSEL1	TRSEL0	VMEINT	IACK3*	IACK2*	IACK1*	SRST

All bits in the 'C30 Control Register except VMEINT are cleared to logic 0 when reset.

3.6.1 SRST - Bit 0 - Active on Low-to-High Edge

On the high-going transition of this bit, a 1 msec pulse is generated by a one-shot pulse generator circuit. This pulse can be connected to the VMEbus signal SYSRST by installing jumper J7-2,19 as described in Section 2.8, Page 21. The SYSRST signal can also be logically OR-ed with other reset signals by installing jumper J7-17,34. This OR-ed signal, called C30RST, resets the 'C30 and a number of other circuits on the board, including the 'C30 Control Register itself. See Section 7.4, Page 58, for more details. A schematic of the reset circuitry is shown in Figure 3-1, below.

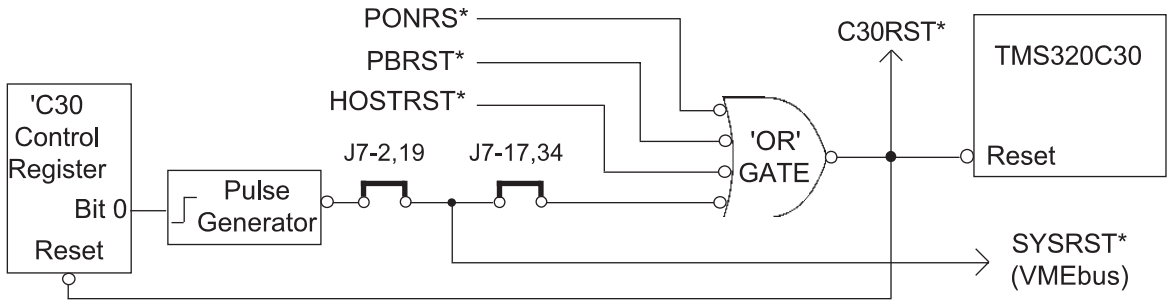


Figure 3-1: Model 4283 - Reset Circuitry Schematic

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3.6.2 IACK1, IACK2 and IACK3

These three bits are used to clear interrupt flip-flops which are set by the interrupt lines from the MIX interface. IACK1, IACK2 and IACK3 serve interrupt flip-flops for MIX modules 0, 1 and 2, respectively. When these lines are set low, the flip-flops are cleared. It is necessary to set the IACK lines low and then high to initialize and enable the interrupt circuitry.

These bits are set low when the 'C30 Control Register is reset by C30RST. A more complete discussion of servicing MIX bus interrupts is presented in Section 5.7, Page 51 and a sample program is shown in Appendix A.

3.6.3 VMEINT - Bit 4 - Active HIGH

This bit sets a flip flop whose output drives an open-collector gate. The output of the gate can be connected to any one of seven VMEbus interrupt lines (IRQ1 through IRQ7) by means of jumpers, described in Section 2.5, Page 19.

The interrupt flip-flop is cleared by the VMEbus interrupt handler when it writes to the IACK Vector register. A schematic of the interrupt circuitry is shown in Figure 3-2, below.

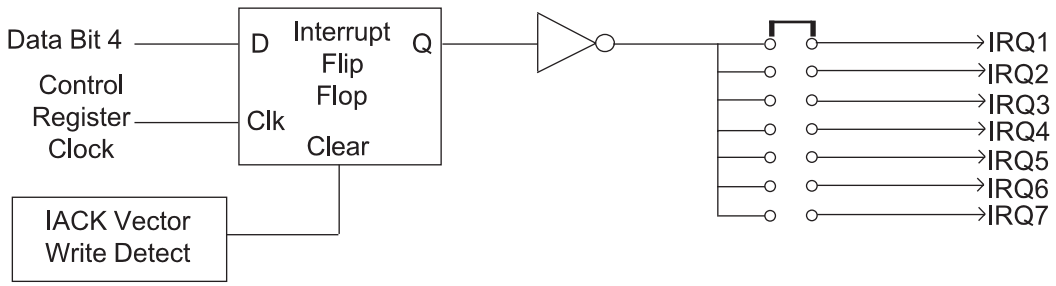


Figure 3-2: Model 4283 - Interrupt Generator Circuitry

3.6.4 TRSEL0 through TRSEL3 (Transfer Select Bits) - Bits 5, 6, 8, and 9

The TRSEL bits determine the memory cycle operation of the Bus Master Interface of the Model 4283. This interface allows the unit to access the VMEbus for read, write, and interrupt acknowledge cycles. Data transfers for reads and writes may be 8, 16, or 32-bits wide, thus supporting many different types of VMEbus devices.

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3.6 TMS320C30 Control Register (continued)

3.6.4 TRSEL0 through TRSEL3 (continued)

The TRSEL bits should be set up prior to conducting bus cycles and may be changed at any time by writing a new pattern. The bit definitions for these bits is shown in Table 3-4, below.

Table 3-4: Model 4283 - Transfer Select (TRSEL) Bit Functions

TRSEL 0 (D5)	TRSEL 1 (D6)	TRSEL 2 (D8)	TRSEL 3 (D9)	Description Type	VMEbus Strobes	VMEbus Addr	VMEbus Data	C30 Data	COMMENTS
0	0	X	X	32-bit Word	DS0, DS1	A01 = L LW* = L	D0 - 31	D0 - 31	Single 32-bit Transfer Cycle
1	0	0	X	16-bit Word Double Cycle	DS0, DS1	A01 = L LW* = H	D0 - 15	D0 - 15	First of Two 16-bit Cycles
				Transfer of 16 bits per cycle	DS0, DS1	A01 = H LW* = H	D0 - 15	D16 - 31	Second of Two 16-bit Cycles
1	0	1	0	16-bit Word Single Word Transfer	DS0, DS1	A01 = L LW* = H	DO - 15	DO - 15	Low Order 16-bit Word Cycle
1	0	1	1	16-bit Word Single Word Transfer	DS0, DS1	A01 = H LW* = H	DO - 15	D16 - 32	High Order 16-bit Word Cycle
0	1	0	0	8-bit Byte Single Byte Transfer	DS0	A01 = L LW* = H	DO - 7	DO - 7	Lowest Order Byte Cycle
0	1	1	0	8-bit Byte Single Byte Transfer	DS1	A01 = L LW* = H	D8-15	D8-15	Next to Lowest Order Byte Cycle
0	1	0	1	8-bit Byte Single Byte Transfer	DS0	A01 = H LW* = H	D0 - 7	D16-23	Next to Highest Order Byte Cycle
0	1	1	1	8-bit Byte Single Byte Transfer	DS1	A01 = H LW* = H	D8-15	D24-31	Highest Order Byte Cycle
1	1	X	X	IACK Cycle	DS0	A1 - A3	D0 - D7	D0 - D7	IACK Vector Read

LW* = VMEbus line LWORD*, X = don't care

3.6.4.1 Longword (32-bit) Memory Cycle

Data is transferred in a single 32-bit cycle with DS0, DS1, and LWORD (longword) lines asserted on the VMEbus. The 32-bit word of the TMS320C30 is aligned on a 32-bit word boundary in VMEbus address space: this implies that VME address A01 = L. All 32-bits of the TMS320C30 and VMEbus data busses are used.

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3.6 TMS320C30 Control Register (continued)

3.6.4.2 Word (16-bit) Memory Cycle (Double Cycle)

Data is transferred in two consecutive 16-bit word cycles with both DS0 and DS1 asserted. The first word is sent with VME address A01 = L, and the second with A01 = H. Both transfers use data lines D0 through D15 of the VMEbus.

The TMS320C30 uses its own data lines D0 through D15 for the first transfer and lines D16 through D31 for the second.

3.6.4.3 Word (16-bit) Memory Cycle (Single Cycle)

In this case, only a single 16-bit word is transferred. Selection of the word is accomplished by setting TRSEL3 = VME address A01. Both DS0 and DS1 are asserted and VMEbus data lines D0 through D15 are used. If TRSEL3 = L, TMS320C30 data lines D0 through D15 are used, and if TRSEL3 = H, D16 through D31 are used.

3.6.4.4 Byte (8-bit) Memory Cycle (Single Cycle)

In this case, a single byte is transferred. Selection of the byte is accomplished by setting TRSEL3 = VME address A01 and TRSEL2 = VME address A00. Each of the four possible cycles is depicted in the chart of Table 3-4. Note that only one data strobe line is asserted, depending on TRSEL2 (A00). Note also the data line correspondence between the data busses for the TMS320C30 and the VMEbus.

3.6.4.5 IACK Cycle

The IACK cycle is used by the TMS320C30 to acknowledge an interrupt on the VMEbus. See Section 7.6, Page 61, for a complete description of the IACK cycle.

3.6.5 LOCK - Bit D7 - Active HIGH

This bit controls the LOCK function for VMEbus memory cycles performed by the Bus Master Interface. Once the Model 4283 is granted access to the bus by the bus arbiter, it asserts the BBSY (bus busy) line on the backplane. If the LOCK bit is set high, the BBSY line is not released until the LOCK bit is set low. This causes the bus arbiter to maintain bus ownership to the Model 4283 without incurring arbitration delays between bus cycles.
CAUTION: This mode can lock up the bus if Model 4283 software fails to restore BBSY low.

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3.7 Interrupt Status Register - 'C30 Address 0x0080 0800

The 'C30 can be interrupted from a variety of sources. Interrupts INT1, INT2, and INT3 are dedicated to the MIX Expansion Modules and are described in Section 5.7, Page 51. Interrupt INT0, however, is driven by any of the seven VMEbus interrupt lines IRQ1 through IRQ7, the VMEbus Timeout Interrupt line, and/or the Host Control Register Interrupt bit. In order to more easily determine the source of interrupts on INT0, the Interrupt Status Register can be polled by the 'C30, typically during an interrupt service routine. Only two bits are used, one for the Host Control Register Interrupt and Bus Timeout. When the bit in the register is logic 1, the interrupt is active. **A write to location 800800H will clear all bits to logic '0'.**

Table 3-5: Model 4283 - Interrupt Status Register -'C30 Address 0x0080 0800

Bit	31-2	1	0
Name	NOT USED	1 = HOST INTERRUPT	1 = BUS TIME OUT

3.8 VMEbus Address Modifier Register -'C30 Address 0x0080 0001 (Write Only)

When the Model 4283 accesses the VMEbus as a Bus Master, the six Address Modifier lines on the VMEbus are driven by the contents of the 6-bit Address Modifier Register. The bit definition for this register is shown in Table 3-6, below.

Table 3-6: Model 4283 - VMEbus Address Modifier Register - 'C30 Address 0x0080 0001 -Write Only

Bit	31-6	5	4	3	2	1	0
Name	NOT USED	AM5	AM4	AM3	AM2	AM1	AM0

Each time a VMEbus memory cycle is performed by the Model 4283, these six AM bits drive the six AM lines on the VMEbus. The AM codes are used to define categories of addressing modes as defined in Table 3-7, on the next page. The AM codes are listed as a two-digit hexadecimal value between 00H and 3FH, where AM5 is the most significant bit and AM0 is the least significant bit.

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3.8 VMEbus Address Modifier Register (continued)

Table 3-7: Model 4283 - Address Modifier Codes

HEX Co	Addr Space	Function	HEX Co	Addr Space	Function
3F	A24	Standard Supervisory Block Transfer	0F	A32	Extended Supervisory Block Transfer
3E	A24	Standard Supervisory Program Access	0E	A32	Extended Supervisory Program Access
3D	A24	Standard Supervisory Data Access	0D	A32	Extended Supervisory Data Access
3B	A24	Standard Nonpriviledged Block Transfer	0B	A32	Extended Nonpriviledged Block Transfer
3A	A24	Standard Nonpriviledged Program Access	0A	A32	Extended Nonpriviledged Program Access
39	A24	Standard Nonpriviledged Data Access	09	A32	Extended Nonpriviledged Data Access
2D	A16	Short Supervisory Access	10 thru 1F		User Defined
29	A16	Short Nonpriviledged Access	all others		Reserved

3.9 Page Address Register - 'C30 Address 0x0080 0002 (Write Only)

The Page Address Register provides the high-order address bits for the VMEbus Bus Master Interface and the MIX Expansion Interface. It is also used to select one of the three MIX Expansion modules. The bit definition is shown in Table 3-8, below.

Table 3-8: Model 4283 - Page Address Register - 'C30 Address 0x0080 0002 - Write Only

BIT	31-18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	not used	A 27	MS 1	MS 0	A 21	A 20	A 19	A 18	A 17	A 16	A 15	A 31	A 30	A 29	A 28	A 27	A 26	A 25	A 24
		Most Significant MIX Expansion Address Bit*	MIX Module Select**		MIX Expansion Page Address (MXA21 thru MXA15)							VMEbus Page Address							

*Most Significant MIX Expansion Address Bit (MXA27)

**MIX Module Select (see below)

Bit 16	Bit 15	MIX Module Select
1	1	Module 0 (First in Stack) - MXSL0
1	0	Module 1 (Second in Stack) - MXSEL1
0	1	Module 2 (Last in Stack) - MXSEL2
0	0	(not valid) MIX Module Select

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3.9 Page Address Register (continued)

The VMEbus Page Address field is used by the VME Bus Master Interface section of the 4283 when operating in the 32-bit addressing mode. See Section 7.7, Page 62, for details about the VMEbus Bus Master Interface.

The MIX Expansion Address bits A27 and A21 through A15 are controlled by bits in the Page Address Register as shown. The two Module Select bits determine which one of the three MIX Expansion modules is selected. See Chapter 5 for details about the MIX Expansion bus.

3.10 VMEbus IACK Address Register - 'C30 Address 0x0080 0003 (Write Only)

The VMEbus IACK Address Register controls the VMEbus interrupt acknowledge (IACK) address. This is a 3-bit address designated as IACK A03, IACK A02, and IACK A01 which is placed on VMEbus address lines A03, A02 and A01 during the IACK cycle. The bit definition is shown below. See Section 7.6, Page 61, for a complete description of interrupt handling.

Table 3-9: Model 4283 - VMEbus IACK Address Register - 'C30 Address 0x0080 0003 - Write Only

Bit		D31 - D3	D2	D1	D0
	IACK LEVEL	not used	IACK A03	IACK A02	IACK A01
	1	-	0	0	1
	2	-	0	1	0
	3	-	0	1	1
	4	-	1	0	0
	5	-	1	0	1
	6	-	1	1	0
	7	-	1	1	1

3.11 MIX Expansion Bus Address Region - 'C30 Address 0x0080 4000 thru 0x0080 5FFF

This range of 8k addresses is the address space of the 'C30 MIX Expansion Bus. Higher order address bits for the MIX Expansion Bus are provided by the Page Address Register. Section 5.6, Page 50, contains a complete description of MIX bus addressing.

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3.12 'C30 Internal RAM - 'C30 Address 0x0080 9800 through 0x0080 9FFF

The 2k x 32 RAM contained within the TMS320C30 is divided into two 1k x 32 blocks, designated as BLOCK 0 and BLOCK 1. The address map for this memory is shown in Table 3-10, below.

Table 3-10: Model 4283 - 'C30 Internal Ram Address Map

Address Range	Description
0x0080 9800 - 0x0080 9BFF	INTERNAL RAM BLOCK 0 - 1K
0x0080 9C00 - 0x0080 9FFF	INTERNAL RAM BLOCK 1 - 1K

3.13 VMEbus IACK Cycle Address - 'C30 Address 0x0080 A000 through 0x008F FFFF

When performing an IACK cycle as a VMEbus Bus Master, the Model 4283 reads from anywhere within this address region to retrieve the IACK vector from the interrupting device. A full description of the IACK cycle is described in Section 7.6, Page 61.

3.14 VMEbus Bus Master Access - 'C30 Address 0x00C0 0000 through 0x00FF FFFF

This range represents a 4 M x 32 bit (16 MBytes) page in the VMEbus address space. See Section 7.7, Page 62, for a complete discussion on VMEbus access.

3.15 'C30 Internal Memory Mapped Registers - 'C30 Address 0x0080 8000 thru 0x0080 9FFF

This memory range is mapped to internal 'C30 peripheral registers. A more detailed view of this address space is presented in Table 3-11, below.

Table 3-11: Model 4283 - 'C30 Internal Memory Mapped Registers

0x0080 8000 - 0x0080 800F	DMA CONTROLLER REGISTER
0x0080 8010 - 0x0080 801F	
0x0080 8020 - 0x0080 802F	TIMER 0 REGISTERS -16
0x0080 8030 - 0x0080 803F	TIMER 1 REGISTERS -16
0x0080 8040 - 0x0080 804F	SERIAL PORT 0 REGISTERS -16
0x0080 8050 - 0x0080 805F	SERIAL PORT 1 REGISTERS -16
0x0080 8060 - 0x0080 806F	PRIMARY & EXPANSION PORT REGISTERS -16
0x0080 8070 - 0x0080 97FF	

For a complete description of each of these registers, refer to Texas Instruments' TMS320C30 User's Guide.

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Chapter 4: VMEbus Memory Map

4.1 Introduction

This chapter describes the view of the Model 4283 from the VMEbus which consists of three elements: the dual-ported DRAM, the Host Control Register, and the IACK (interrupt acknowledge) Vector Register.

4.2 VMEbus Addresses

VMEbus address bits A1 through A31 are implemented as 31 separate bus lines. These lines are used to explicitly address 2^{31} 16-bit words.

VME address bit A0 does not actually correspond to an address line on the bus, but is used in the control of two data strobe lines: DS0 and DS1. DS0 becomes active for the lower byte of the 16-bit word, and DS1 for the upper byte. For single byte transfers, only one of the DS strobes is active. For 16-bit transfers, both data strobes become active at the same time. For 32-bit transfers, in addition to both strobes active, the LWORD (longword) bus line is also asserted.

4.2.1 Address Modifier Codes

There are three addressing modes defined for VMEbus transfers: 32-bit, 24-bit, and 16-bit modes. The modes are provided to support a variety of bus devices ranging from simple I/O functions with only a few memory locations to large RAM arrays with hundreds of mega-bytes of storage. The addressing mode is determined by a special 6-bit code which is placed on 6 dedicated VMEbus lines by the current VMEbus Master and is known as the Address Modifier Code, or AM Code.

The VMEbus specification defines the usage of certain AM codes as shown in Table 4-1. The Model 4283 responds only to the AM codes shown in boldface type. Other codes may be included by modifying the AM Code PAL.

Table 4-1: Model 4283 - Address Modifier Codes

HEX Co	Addr Space	Function	HEX Co	Addr Space	Function
3F	A24	Standard Supervisory Block Transfer	0F	A32	Extended Supervisory Block Transfer
3E	A24	Standard Supervisory Program Access	0E	A32	Extended Supervisory Program Access
3D	A24	Standard Supervisory Data Access	0D	A32	Extended Supervisory Data Access
3B	A24	Standard Nonpriviledged Block Transfer	0B	A32	Extended Nonpriviledged Block Transfer
3A	A24	Standard Nonpriviledged Program Access	0A	A32	Extended Nonpriviledged Program Access
39	A24	Standard Nonpriviledged Data Access	09	A32	Extended Nonpriviledged Data Access
2D	A16	Short Supervisory Access	10 thru 1F		User Defined
29	A16	Short Nonpriviledged Access	all others		Reserved

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4.3 VMEbus Memory Map

The VMEbus sees the Model 4283 as two regions of memory:

1) A16 memory space for the Host Control and IACK Vector Registers.

2) A24 or A32 memory space for the DRAM (depending on AM codes used).

The three memory maps below show how the Model 4283 appears to the VMEbus. Note that A16 space addresses are expressed with 4 hex digits, A24 addresses with 6 digits, and A32 addresses with 8 digits.

Setting the A16 Base Address is described in Figure 2-3, Page 18.

Setting the A24 or A32 DRAM Base Address is described in Section 4.4, Page 36 which follows.

Table 4-2: Model 4283 - VMEbus Memory Map

A16 ADDRESS SPACE	0x0000 to (A16_ base - 0001)	RESERVED
	A16_ base + 0x0000	IACK VECTOR REGISTER
	A16_ base+0x0002	HOST CONTROL REGISTER
	(A16_ base + 0x0003) to 0x03FF	RESERVED
	0x0400 to 0xFFFF	OTHER A16 RESOURCES
A24 ADDRESS SPACE	0x0000 0000 to (DRAM BASE -0x0000 0001)	OTHER MEMORY RESOURCES
	DRAM BASE to 0x00FF FFFF	4283 DRAM - 1, 4 or 8MB
		OTHER MEMORY RESOURCES
A32 ADDRESS SPACE	0x0000 0000 to (DRAM BASE - 0x0000 0001)	OTHER MEMORY RESOURCES
	DRAM BASE to 0xFFFF FFFF	4283 DRAM - 1, 4 or 8MB
		OTHER MEMORY RESOURCES

4.4 Addressing the DRAM - VMEbus Access

The dual-port DRAM appears as a VMEbus slave device at a base memory address selected by switches SW1 and SW2. The base address is the VMEbus address corresponding to the bottom (or lowest address) of the DRAM. Both A32 and A24 addressing modes are supported. The DRAM is available in 1, 4, or 8 MByte capacities.

The DRAM is truly a dual-ported device, one port accessible from the VMEbus and the other from the 'C30. The DRAM presents itself to the 'C30 as an array 32-bit words, and to the VMEbus as an array of 8-bit bytes. For this reason, each single address location of the 'C30 represents four bytes and hence, four addresses in VMEbus address space.

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4.4 Addressing the DRAM (continued)

4.4.1 A32 DRAM Access

The Model 4283 will respond to 32-bit addressing for Address Modifier codes (AM Codes) of 0x000E, 0x000D, 0x000A, and 0x0009.

Switches SW1 and SW2 are shown below with the address bit correspondence. The switches should be set for the 'open' position to match an address bit = 1, and to the 'closed' position for address bit = 0.

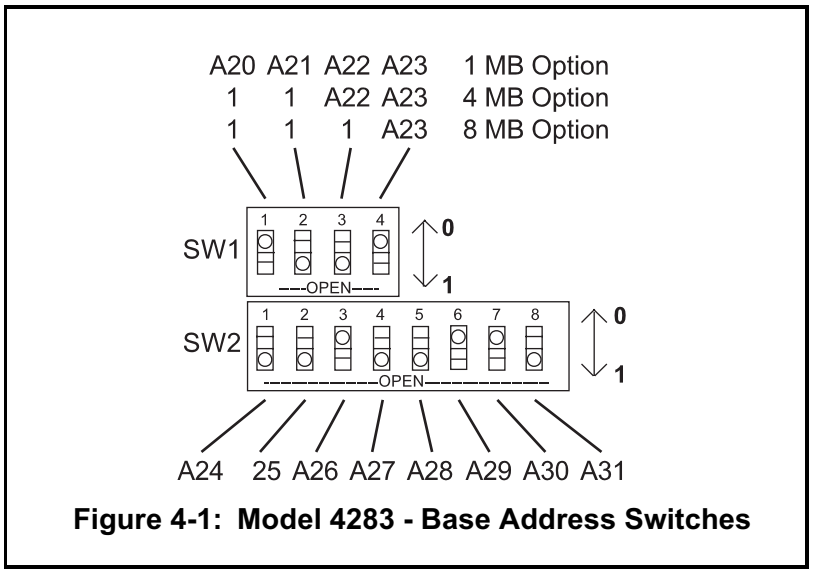


Figure 4-1: Model 4283 - Base Address Switches

The 1 MB DRAM may be located anywhere within the 32-bit address space on any 1 MByte boundary, the 4 MB DRAM on any 4 MB boundary and the 8 MB on any 8 MB boundary. Note that some of the SW1 switches should be set to the '1' or 'open' position as indicated for the 4MB and 8 MB options.

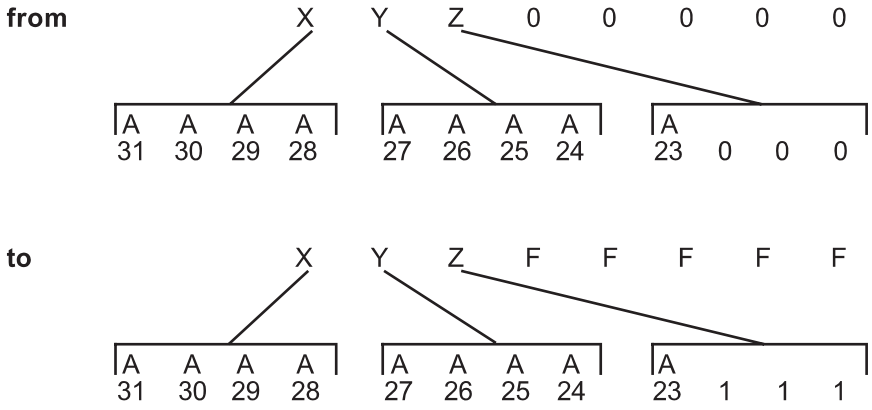
The rocker switch positions are indicated by the arrow pointing to the depressed position. In the Figure 4-1, above, the '0' position is set by depressing the top of the switch and the '1' by depressing the bottom of the switch.

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4.4 Addressing the DRAM (continued)

4.4.1.1 A32 DRAM Access - 8 MByte Option

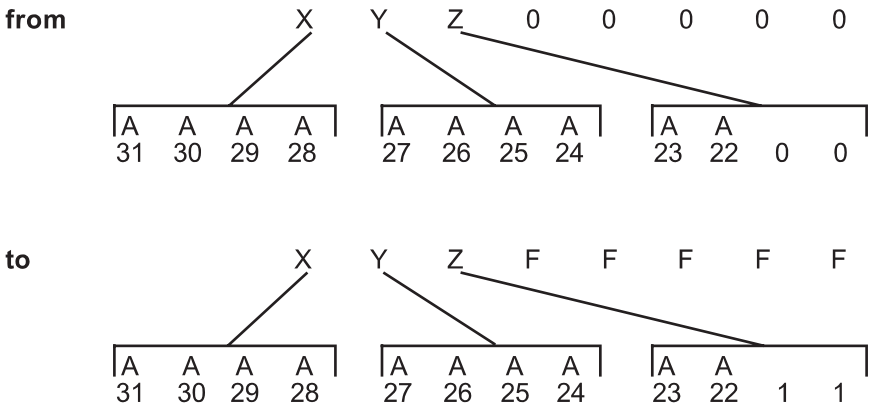
The address range of the 8MB DRAM in 32-bit VMEbus address space is given below in hex:



The first three hex digits are shown decomposed into four binary bits. The first two digits show the address settings from switch SW1 (A31 through A24). The third digit shows the A23 bit setting from SW2 and the remaining three binary bits for the upper and lower address limits. For example, if SW1 has only A28 and A25 set to '1' and SW2 has A23 set to '0', the address range would be from 0x1200 0000 to 0x127F FFFF.

4.4.1.2 A32 DRAM Access - 4MByte Option

The address range of the 4MB DRAM in 32-bit VMEbus address space is given below in hex:



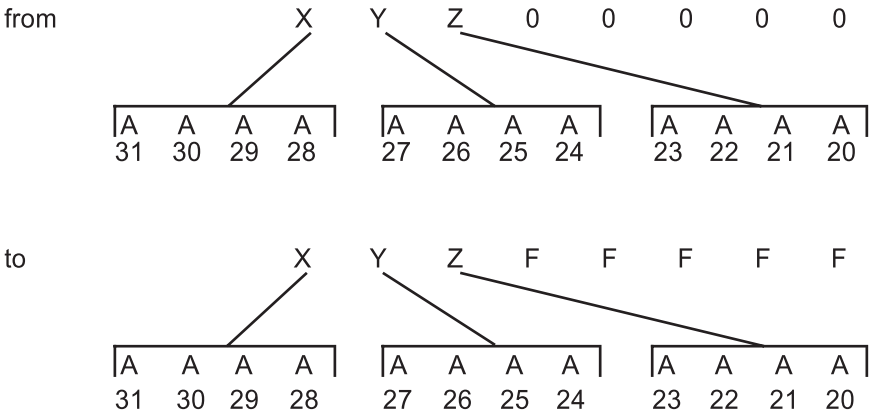
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4.4 Addressing the DRAM (continued)

4.4.1 A32 DRAM Access (continued)

4.4.1.3 A32 DRAM Access - 1 MByte Option

The address range of the 1MB DRAM in 32-bit VMEbus address space is given below in hex:



For example, suppose we wish to locate the 1 MB DRAM at a base address of 0x9B60 0000. The address range will be from 0x9B60 0000 to 0x9B6F FFFF. Switches SW1 and SW2 should be set as shown in Figure 4-2, below. Remember, the **arrows point to the depressed position** (indicated by the black dots in the drawing).

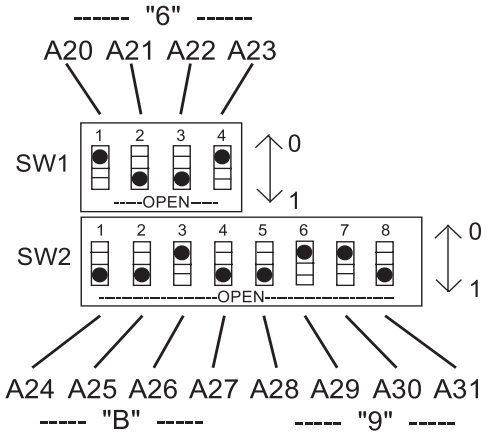


Figure 4-2: Model 4283 - Base Address Switches (A32) - DRAM_base = 9B60 0000

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4.4 Addressing the DRAM (continued)

4.4.2 A24 DRAM Access

The Model 4283 will respond to 24-bit addressing for Address Modifier codes (AM Codes) of 0x0039, 0x003A, 0x003D, and 0x003E.

Switch SW1 is shown below with the corresponding address bit correspondence. The switch should be set for the 'open' position to match an address bit = 1, and to the 'closed' position for address bit = 0.

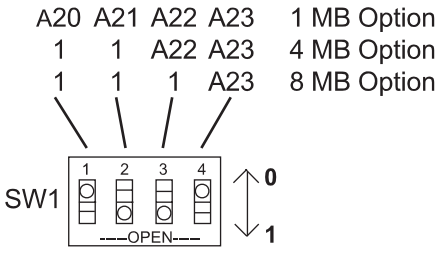


Figure 4-3: Model 4283 - A24 Base Address Switch

The 1 MB DRAM may be located anywhere within the 24-bit address space (16 MBytes total) on any 1 MByte boundary, the 4 MB DRAM on any 4 MB boundary, and the 8 MB DRAM on either 8 MB boundary. There are 16 possible locations for the 1 MB DRAM, 4 locations for the 4MB DRAM and 2 locations for the 8 MB DRAM. Note that in the 4MB and 8MB options, the switch positions marked '1' must be properly set to the '1' or 'open' position.

4.4.2.1 A24 DRAM Access - 8 MByte Option

The address range of the 8MB DRAM in 24-bit VMEbus address space is given below in
hex:



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4.4.2.2 A24 DRAM Access - 4 MByte Option

The address range of the 4MB DRAM in 24-bit VMEbus address space is given below in hex:



4.4.2.3 A24 DRAM Access - 1 MByte Option

The address range of the 1MB DRAM in 24-bit VMEbus address space is given below in hex:



For example, suppose we have a 4 MByte DRAM and wish to map with a base address of 0x0040 0000H. The address range will be from 0x0040 0000 to 0x007F FFFF. The address switch SW1 should be set as shown below.

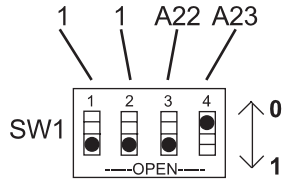


Figure 4-4: Model 4283 -A24 DRAM_base = 0x0040 0000

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4.5 Host Control and IACK Vector Registers

The Host Control Register allows a VMEbus Bus Master to control the reset and interrupt lines into the 'C30. The IACK Vector Register is an 8-bit register loaded from the VMEbus which stores a vector which the Model 4283 sends in response to an interrupt acknowledge cycle.

These two registers are mapped into A16 address space on the VMEbus. This address space is selected by using AM codes of either 29 or 2D. The address bus lines A01 through A15 are used for address decoding and selection. The upper address lines are ignored.

Section 2.3, Page 61, describes the jumper configurations for selecting the A16 base address. Note that there are 16 possible A16 base addresses. For systems with more than one Model 4283 installed, each board can be configured for a different address. This permits individual control of the reset and interrupt functions from the bus. If it is desired that all boards are to be reset and interrupted simultaneously, then multiple boards can be set for the same address.

4.5.1 Host Control Register

The Host Control Register is a 2-bit write-only register, whose bit definitions shown in Table 4-3, below.

Table 4-3: Model 4283 - Host Control Register - VMEbus Address A16_base + 0x0002

Bit	15 - 2	1	0
Name	not used	HOSTINT	HOSTRST

4.5.1.1 HOST INT - Bit 1

This bit can be used as a VMEbus software interrupt to the 'C30 on interrupt level INT0. Jumper block J4 must be properly configured to connect the interrupt line. See Section 2.5, Page 19, for more details.

The bit is active when set to logic '1'. It is reset to '0' by the general purpose reset signal C30RST*. See Section 7.4, Page 58, for more details about reset operation. See Section 7.2, Page 55 and Section 7.3, Page 57 for more details about interrupt handling.

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4.5 Host Control and IACK Vector Registers (continued)

4.5.1 Host Control Register (continued)

4.5.1.2 HOSTRST - Bit 0

This bit can be used for a VMEbus software reset function. It is active when set to logic '1'. It is reset to '0' upon power on reset (PONRS*). It is 'OR-ed' with other sources of reset control as shown in Figure 4-5, below. See Section 7.4, Page 58, for more details

.

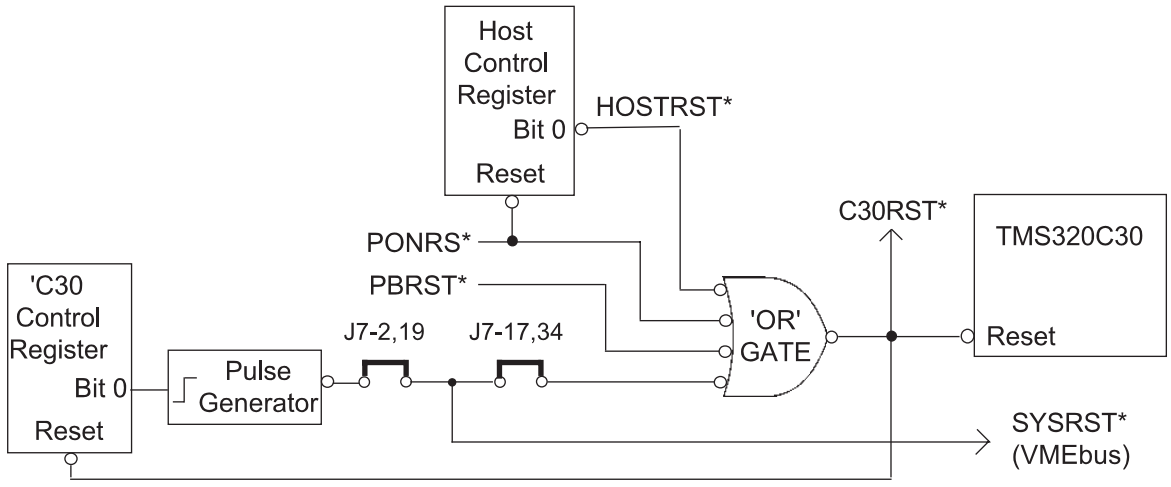


Figure 4-5: Model 4283 - HOSTRST Diagram

4.5.2 IACK Vector Register

The IACK Vector Register stores the interrupt acknowledge ID byte vector which the VMEbus uses to identify the source of an interrupt. This vector is an 8-bit value which is placed on the VMEbus data bus lines D7 through D0 in response to an IACK cycle.

Table 4-4: Model 4283 - IACK Vector Register - VMEbus Address A16 Base

Bit	15 - 2	7	6	5	4	3	2	1	0
Name	not used	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

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Chapter 5: MIX Expansion Bus

5.1 Introduction

The connection between the Model 4283 Processor Board and the family of expansion modules is provided by the 'MIX' interface standard originally developed by Intel Corporation for Multibus II. This system defines an electrical and mechanical standard for a private high-speed 32-bit bus fully supported with interrupt and control functions.

The elements of the MIX system implemented by Pentek for VMEbus are described in the sections below.

5.2 MIX Baseboard - Model 4283

The baseboard is the Model 4283 Board which is a full size VMEbus board in a standard 6U format (160mm x 233 mm). It occupies one standard slot position (0.8 inches of horizontal space) in a VMEbus card cage. The Model 4283 baseboard has two 96-pin male DIN connectors (P1 and P2) which mate with the corresponding female connectors on the VMEbus card cage backplane.

All power for the Model 4283 and any expansion modules comes through these connectors. The baseboard features a surface mount connector pattern near the center of the board which supports the MIX interface. This pattern consists of 130 gold-plated PC pads on the component side of the board and holes in the board for mounting the MIX baseboard connector described below. If no expansion modules are to be used, the MIX baseboard connector need not be installed.

5.3 Expansion Modules (MIX modules)

The expansion modules allow the user to configure a system for many different applications. Up to three of these modules can be stacked on the component side of the baseboard in any order.

Each module is 10.3" long x 4.0" deep x 0.8" wide. No electrical or mechanical connection is made to the VMEbus back plane since all power and signal lines are provided through the MIX interface connector. Each module has its own front panel which is secured to the front mounting edge of the card cage with captive hardware. The rear of the expansion module is secured mechanically by the MIX connector itself.

Each module is accessed by the TMS320C30 on the MIX baseboard as a unique memory region determined by the module stacking position. Separate interrupt and control lines are also provided for each stack position. The expansion modules are designed such that the component side of each module faces the component side of the Model 4283 baseboard.

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5.3 Expansion Modules (continued)

In general, each expansion module occupies one 0.8" card cage slot position. As viewed from the front panel of the Model 4283 baseboard in a vertical card cage, the first expansion module occupies the slot to the immediate right of the baseboard. The second expansion module occupies the second slot to the right of the baseboard, etc.

An exception to the above rule occurs for the Model 4241 and Model 4244. Because of the low profile components used, either of these modules can be installed in the first stacking position so that they occupy the same card cage slot as the Model 4283 baseboard. In this case, the Model 4283 and the expansion module share a common 0.8" front panel.

See Appendix B of this manual for MIX stack assembly instructions.

5.4 MIX Bus Connector Signals

The following chart lists the MIX Bus signal definitions for all 130 pins of the connector as implemented on the Model 4283. Some of the MIX bus signals defined in the Intel specification are not employed by the Model 4283.

Table 5-1: Model 4283 -MIX Bus Signals

Pin	Signal Name	I/O	Description
1	MXRST*	O	Module Power On Reset
2	NC	N/A	Not Connected
3	NC	N/A	Not Connected
4	MXINT1*	I	Interrupt from Module 1
5	NC	N/A	Not Connected
6	NC	N/A	Not Connected
7	NC	N/A	Not Connected
8	NC	N/A	Not Connected
9	MXA27*	O	Module Byte Address Line
10	NC	N/A	Not Connected
11	MXA19*	O	Module Byte Address Line
12	MXA17*	O	Module Byte Address Line
13	MXA13*	O	Module Byte Address Line
14	MXA9*	O	Module Byte Address Line
15	MXA7*	O	Module Byte Address Line
16	MXA3*	O	Module Byte Address Line
17	GND	O	Ground (Low Current)
18	MXSEL0*	O	Module 0 Select Line
19	MXCYC*	O	Module Control Line
20	+5V	O	5 Volts (Low Current)
21	NC	N/A	Not Connected
22	NC	N/A	Not Connected
23	NC	N/A	Not Connected
24	MXD29	I/O	Module Data Line
25	MXD25	I/O	Module Data Line
26	MXD22	I/O	Module Data Line
27	MXD19	I/O	Module Data Line

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Table 5-1: Model 4283 -MIX Bus Signals (Continued)

Pin	Signal Name	I/O	Description
28	MXD15	I/O	Module Data Line
29	MXD12	I/O	Module Data Line
30	MXD9	I/O	Module Data Line
31	MXD5	I/O	Module Data Line
32	MXD2	I/O	Module Data Line
33	MXD0	I/O	Module Data Line
34	+ 12V	O	+ 12 Volt Power
35	GND	I	Ground
36	NC	N/A	Not Connected
37	NC	N/A	Not Connected
38	+5V	O	5 Volt Power
39	NC	N/A	Not Connected
40	NC	N/A	Not Connected
41	GND	I	Ground
42	NC	N/A	Not Connected
43	MXA21*	O	Module Byte Address Line
44	+5V	O	5 Volt Power
45	MXA15*	O	Module Byte Address Line
46	MXA11*	O	Module Byte Address Line
47	GND	I	Ground
48	MXA5*	O	Module Byte Address Line
49	GND	O	Ground (Low Current)
50	+5V	O	5 Volt Power
51	MXSEL2*	O	Module 2 Select Line
52	GND	I	Ground
53	+5V	O	5 Volt (Low Current)
54	NC	N/A	Not Connected
55	+5V	O	5 Volt Power
56	MXD31	I/O	Module Data Line
57	MXD27	I/O	Module Data Line
58	GND	I	Ground
59	MXD21	I/O	Module Data Line
60	MXD17	I/O	Module Data Line
61	+5V	O	5 Volt Power
62	MXD11	I/O	Module Data Line
63	MXD7	I/O	Module Data Line
64	GND	I	Ground
65	+12V	O	+ 12 Volt Power
66	-12V	O	- 12 Volt Power
67	GND	I	Ground
68	NC	N/A	Not Connected
69	MXINT2*	I	Interrupt from Module 2
70	+5V	O	5 Volt Power
71	NC	N/A	Not Connected
72	NC	N/A	Not Connected
73	GND	I	Ground
74	NC	N/A	Not Connected
75	NC	N/A	Not Connected
76	+5V	O	5 Volt Power
77	MXA16*	O	Module Byte Address Line
78	MXA12*	O	Module Byte Address Line
79	GND	I	Ground

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Table 5-1: Model 4283 -MIX Bus Signals (Continued)

Pin	Signal Name	I/O	Description
80	MXA6*	O	Module Byte Address Line
81	MXA2*	O	Module Byte Address Line
82	GND	I	Ground
83	MXSEL1*	O	Module 1 Select Line
84	MXCMD*	O	Module Control Line
85	GND	I	Ground
86	MXWAIT*	I	Module 'C30 Wait State Request
87	NC	N/A	Not Connected
88	+5V	O	5 Volt Power
89	MXD28	I/O	Module Data Line
90	MXD24	I/O	Module Data Line
91	GND	I	Ground
92	MXD18	I/O	Module Data Line
93	MXD14	I/O	Module Data Line
94	+5V	O	5 Volt Power
95	MXD8	I/O	Module Data Line
96	MXD4	I/O	Module Data Line
97	GND	I	Ground
98	- 12V	O	- 12 Volt Power
99	NC	N/A	Not Connected
100	NC	N/A	Not Connected
101	MXINT0*	I	Interrupt from Module 0
102	NC	N/A	Not Connected
103	NC	N/A	Not Connected
104	NC	N/A	Not Connected
105	NC	N/A	Not Connected
106	NC	N/A	Not Connected
107	NC	N/A	Not Connected
108	MXA20*	O	Module Byte Address Line
109	MXA18*	O	Module Byte Address Line
110	MXA14*	O	Module Byte Address Line
111	MXA10*	O	Module Byte Address Line
112	MXA8*	O	Module Byte Address Line
113	MXA4*	O	Module Byte Address Line
114	GND	O	Ground (Low Current)
115	GND	O	Ground (Low Current)
116	NC	N/A	Not Connected
117	MXWR	O	Module Read/Write Control
118	NC	N/A	Not Connected
119	NC	N/A	Not Connected
120	NC	N/A	Not Connected
121	MXD30	I/O	Module Data Line
122	MXD26	I/O	Module Data Line
123	MXD23	I/O	Module Data Line
124	MXD20	I/O	Module Data Line
125	MXD16	I/O	Module Data Line
126	MXD13	I/O	Module Data Line
127	MXD10	I/O	Module Data Line
128	MXD6	I/O	Module Data Line
129	MXD3	I/O	Module Data Line
130	MXD1	I/O	Module Data Line

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5.5 MIX Module Interface Timing

The timing specifications for the interface appear in Table 5-2, below. These may be used for reference or for the design of custom interface modules.

Table 5-2: Module 4283 - MIX Module Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
Tcsu	Command Setup Time		30		ns
Tch	Command Hold Time		30		ns
Twsu	R/W Address Setup Time	60			ns
Ta	Read Access Time	50			ns
Tw	Wait Signal Delay Time			40	ns
Taw	Wait Signal Access Time			20	ns
Tdsu	Write Data Setup Time	60			ns
Tdh	Write Data Hold Time	0			ns

The timing diagram showing the above parameters is given in Figure 5-1, below.

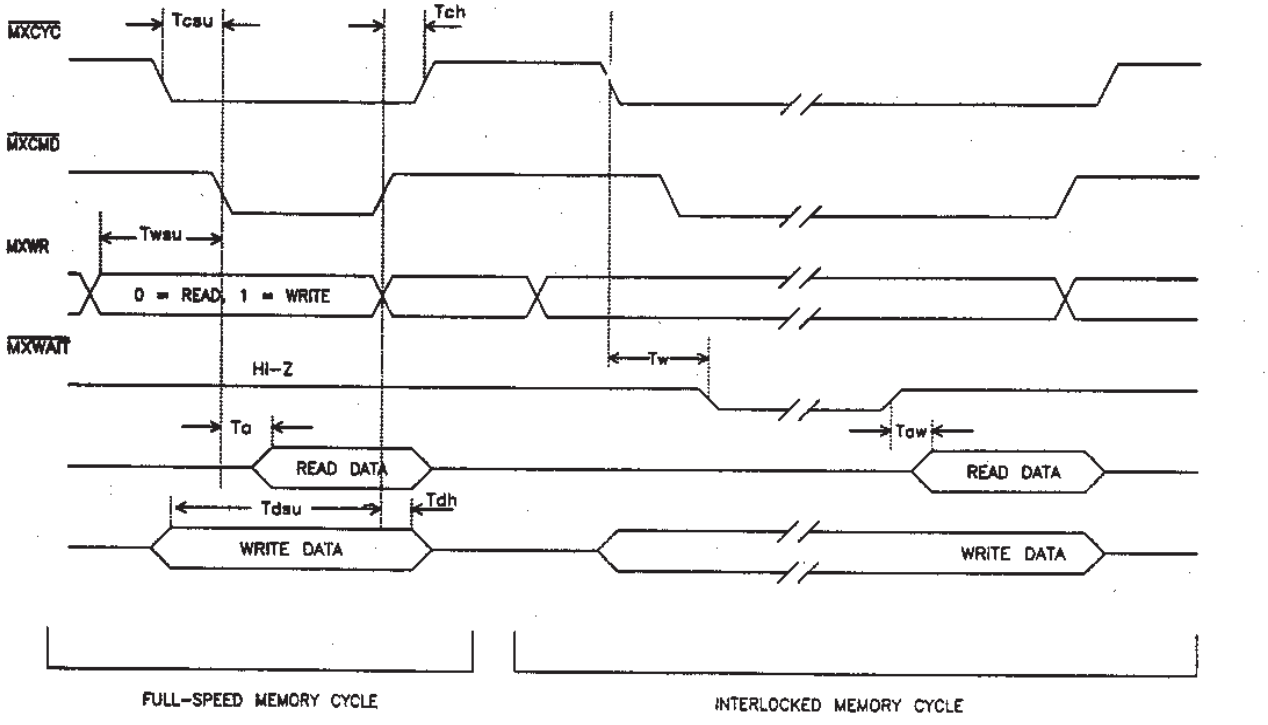


Figure 5-1: Module 4283 - MIX Module Interface Timing Diagram

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5.6 Addressing the MIX Expansion Modules

All resources of the MIX modules appear in the memory map of the Model 4283 in the MIX Bus Expansion address space which extends from 0x0080 4000 to 0x0080 5FFF. This 8k x 32 page serves as the 'C30 window into the module for all control and data transfers. All modules mounted on the 4283 act only as MIX Slave devices: they can not initiate ownership of the MIX bus (i. e., the Model 4283 does not support Upper MIX Bus Mastering). Instead, all transfers must be initiated by the 'C30 on the Model 4283.

There may be a maximum of three MIX modules attached to the Model 4283, and each module is addressed by its physical position in the stack. The Page Address Register contains the MIX Module Select bits MS1 and MS0 which are decoded to drive one of the three MIX Bus lines: MXSEL0, MXSEL1, and MXSEL2. These enable one module at a time for transfers.

The Page Register also contains the MIX Address bits for MXA15 through MXA21 and MXA27. Address lines MXA22 through MXA26 are not driven. The Page Address register is described in Section 3.9, Page 32, and the bit chart is given again in Table 5-3, below.

Table 5-3: Model 4283 - Page Address Register - 'C30 Address 0x0080 0002 - Write Only

BIT	31-18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	not used	A 27	MS 1	MS 0	A 21	A 20	A 19	A 18	A 17	A 16	A 15	A 31	A 30	A 29	A 28	A 27	A 26	A 25	A 24
		Most Significant MIX Expansion Address Bit*	MIX Module Select**		MIX Expansion Page Address (MXA21 thru MXA15)							VMEbus Page Address							

*Most Significant MIX Expansion Address Bit (MXA27)

**MIX Module Select (see below)

Bit 16	Bit 15	MIX Module Select
1	1	Module 0 (First in Stack) - MXSL0
1	0	Module 1 (Second in Stack) - MXSEL1
0	1	Module 2 (Last in Stack) - MXSEL2
0	0	(not valid) MIX Module Select

Addressing a module consists of three steps:

1) Set the Page Register MS (MIX Module Select) bits for the correct module position.
2) Set the Page Register MIX address bits for the correct MIX bus Page as defined in the operating manual for the particular module.
3) Perform reads and writes to the 8k x 32 page of the MIX Expansion Bus (between

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0x0080 4000 and 0x0080 5FFF) for memory mapped module resources as defined in the manual for the module.

5.7 Servicing Interrupts for MIX Modules

Each MIX module has an interrupt output line to the MIX bus which provides a separate path for each line down to the Model 4283. Here, the three module interrupt lines are connected to a PAL which contains three S-R (set-reset) flip flops. A representation of these flip-flops is shown in Figure 5-2, below.

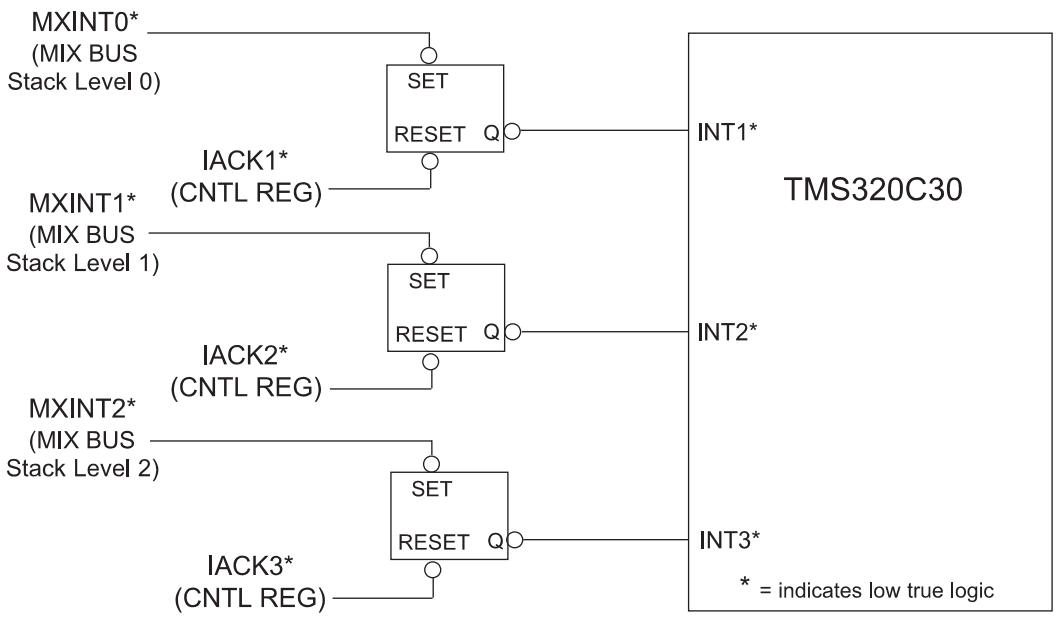


Figure 5-2: Model 4283 - MIX Interrupts to 'C30

The interrupt line from the module in the first MIX stacking position is MXINT0*. It sets the S-R Flip-Flop by making a transition from high to low. The low true output of the flip-flop drives the INT1* pin on the 'C30. This flip-flop is cleared by the signal IACK1* which is one of the 'C30 Control Register bits, as described in Section 3.6.2, Page 28. The interrupt circuitry for the other two module levels is identical, as shown in Figure 5-2.

Initialization software to set up these interrupts should include code which sets the IACKn bit low and then high. This will reset the S-R flip-flop and prepare it to receive a new interrupt. During the interrupt service routine, the sequence of operations shown on the next page should be implemented:

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5.7 Servicing Interrupts for MIX Modules (continued)

- Determine the source and status of the interrupting module
- Service the device (load or unload data)
- Clear the interrupt line from the module (MXINTn line)
- Clear the S-R flip-flop by setting the IACKn bit low
- Reset the ′C30 IF (interrupt flag) register bit
- Enable a new interrupt by setting the IACKn bit high to the S-R flip-flop
- Enable the ′C30 GIE (global interrupt enable) bit

Details of how the ′C30 processes interrupts is covered in the TMS320C30 User's Guide. Refer to the manual for the MIX module for specifics about how interrupts are generated and cleared within the module. See Appendix A for a prototype MIX Module interrupt handler.

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Chapter 6: Interfaces

6.1 Auxiliary Port Connector

The Model 4283 provides a 17-pin front panel connector which provides access to a number of signal lines of the 'C30. These lines serve the 'C30 Peripheral Devices and the IOF (input/output flag) lines.

The signal names are shown on the front panel and are described in Table 6-1, below. The TMS-320C30 User's Guide describes these signals in full detail.

The connector is a single-in-line row of 0.025" square pins on 0.100" spacing. These lines may be connected to another device using a standard 34-pin double-row flat-cable socket connector. In this case, one side of the connector will not be utilized.

However, if a Model 4244 Co-Processor Module is attached in the nested position as the first stacking module, then its Peripheral Connector will align with those from the Model 4283 forming a dual row 34-pin header configuration. In this case, if the 34-pin DIL socket is used, then both sides will be engaged.

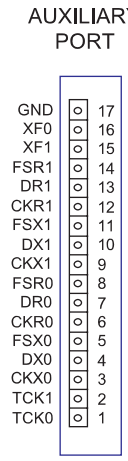


Figure 6-1: Model 4283- Auxiliary Port Connector

The Peripheral Connector may also be used as a general purpose interconnect header with connections made by wire-wrapping or with individual push-on sockets which accommodate 0.025" square posts. A number of different single and dual row socketshare available for discrete wiring arrangements. Manufactures include Berg (DuPont), AMP, Samtec, T&B Ansley, etc.

Table 6-1: Model 4283 - Auxiliary Port Connector

Pin	Signal	In/Out	Description
1	TCLK0	I/0	Timer 0 Clock Input or Clock Output
2	TCLK1	I/0	Timer 1 Clock Input or Clock Output
3	CLKX0	I/0	Serial Port 0 Transmit Clock
4	DX0	O	Serial Port 0 Data Transmit Output
5	FSX0	I/0	Serial Port 0 Frame Synchronization
6	CLKR0	I/0	Serial Port 0 Receiver Clock
7	DR0	I	Serial Port 0 Data Receive Input
8	FSR0	I	Serial Port 0 Frame Synchronization Receive Input
9	CLKX1	I/0	Serial Port 1 Transmit Clock
10	DX1	O	Serial Port 1 Data Transmit Output
11	FSX1	I/0	Serial Port 1 Frame Synchronization
12	CLKR1	I/0	Serial Port 1 Receiver Clock
13	DR1	I	Serial Port 1 Data Receive Input
14	FSR1	I	Serial Port 1 Frame Synchronization Receive Input
15	XF1	I/0	External Flag 1 General Purpose I/o Bit
16	XF0	I/0	External Flag 1 General Purpose I/o Bit
17	GND	-	System Ground - 0 volts reference

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6.2 XDS Emulator Connector

The Model 4283 provides a 12-pin connector compatible with the Texas Instruments' XDS500 Emulator. This is a PC-based development system with a cable for connection to a target 'C30 product such as the Model 4283. The location of the XDS emulator connector is on the component side of the Model 4283 main board, just behind the front panel Peripheral Connector. The pin layout for this connector is shown in Figure 6-2, on the right.

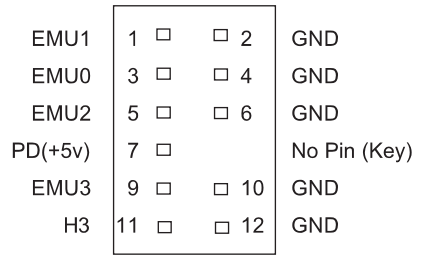


Figure 6-2: Model 4283 - XDS Connector Pin-out

If the emulator cable is used with the Model 4283 alone (without any MIX modules attached) then the cable can be routed out through from panel opening of the adjacent slot in the card cage.

If either the Model 4241 or Model 4244 is attached in the nested stacking position as the first module, access to the XDS connector is impossible. In this case, re-assemble the modules using the MIX Spacer Board and stacking connector as shown in Figure 1-5 of the MIX tutorial. This will leave sufficient space for the emulator cable to be attached.

6.3 Reset Switch

The Front Panel Reset Switch is a momentary push-button switch which allows the user to manually reset the board. See Section 7.4, Page 58, for more details about the reset circuitry.

6.4 XF0 LED

The XF0 bit in the IOF (Input/Output Flag) Register is attached to a LED driver which controls a LED installed just behind the front panel, below the Auxiliary Port Connector. When the XF0 flag is high, the LED in ON and when it is low, the LED is OFF. Since the XF0 bit can be used as an input or an output, the LED will indicate either the input level from an external XF0 source or the output level of the XF0 bit as controlled by the 'C30.

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Chapter 7: Operating Procedures

7.1 Introduction

This chapter contains information about using the various operational modes of the Model 4283.

7.2 Handling Interrupts

There are several separate interrupt inputs to the TMS320C30 on the Model 4283, each of which is shown in Table 7-1, below, with its possible sources.

Table 7-1: Model 4283 - Reset and Interrupt Vectors - TMS320C30

Interrupt Name	Vector Level	EPROM Vector	Interrupt Priority	Internal/ External	Description
RESET	0x0000	none	0	Ext	External Reset Pin
INT0	0x0000	0x0080 9800	1	Ext	VMEbus Timeout Host Control Register
INT1	0x0002	0x0080 9804	2	Ext	Interrupt VMEbus IRQ1 through IRQ7 MIX Expansion Module 0
INT2	0x0003	0x0080 9808	3	Ext	MIX Expansion Module 1
INT3	0x0004	0x0080 980C	4	Ext	MIX Expansion Module 2
XINT0	0x0005	0x0080 9810	5	Int	Serial Port 0 Transmit Buffer Empty
RINT0	0x0006	0x0080 9814	6	Int	Serial Port 0 Receive Buffer Full
XINT1	0x0007	0x0080 9818	7	Int	Serial Port 1 Transmit Buffer Empty
RINT1	0x0008	0x0080 981C	8	Int	Serial Port 1 Receive Buffer Full
TINT0	0x0009	0x0080 9820	9	Int	Timer 0 Interrupt
TINT2	0x000A	0x0080 9824	10	Int	Timer 1 Interrupt
DINT	0x000B	0x0080 9828	11	Int	DMA Controller Interrupt
TRAP0	0x0020	0x0080 982C		Int	Trap 0
....	....	....		....	....
TRAP27	0x003B	0x0080 9898		Int	Trap 27

Interrupts are prioritized as shown in the table, with the highest priority at the top. In order for an interrupt to be processed, it must be enabled by setting a bit in the 'C30 Interrupt Enable Register (IE). The 'C30 Interrupt Flag Register (IF) can be viewed to determine which of the interrupts is active. Refer to the TMS320C30 Users' Guide for more details.

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7.2 Handling Interrupts (continued)

7.2.1 Interrupt Vectors

Once the interrupt is received by the 'C30, it pushes the program counter (PC) and other registers onto the stack and loads the PC with the contents of memory location = Vector Level. For example, an INT3 interrupt would load the PC with the contents of memory location 0x0003.

Note that all of these vector level addresses are located in the EPROM. The values stored in the EPROM will determine the address of the next instruction the 'C30 will execute. Because it is inconvenient to reprogram the EPROM to change these vectors, an intermediate table in internal 'C30 RAM has been setup for re-vectoring these interrupts. The EPROM vectors point to locations in this RAM which can be used to contain branch instructions.

Upon power up, the boot program in EPROM copies branch instructions into this RAM region. These branches point back to interrupt service routines in the EPROM. With this scheme, if a different vector is required, the user can modify the contents of the RAM to re-direct the vector.

7.2.2 Delayed Branch Table

The TMS320C30 normally takes 4 cycles to complete a standard branch instruction. However, a delayed branch instruction executes the next 3 instructions following the delayed branch instruction before branching, also for a total of 4 cycles. This provides a more efficient branch since the first 3 instructions of an interrupt service routine can be placed immediately after the delayed branch instruction, making the interrupt routine run more quickly.

For this reason, 4 memory locations have been allocated for each delayed branch instruction in internal 'C30 RAM vector table. The addresses shown in Table 7-1 in the EPROM Vector column correspond to the location of each delayed branch instruction.

In order to redirect any interrupt vector, the user replaces the delayed branch instruction with a new one. The next three instructions can be used as the first part of the interrupt routine.

If the delayed branch table is not modified, interrupts are vectored back to a generic interrupt handler in EPROM. See the assembly language source code for the EPROM portion of MON30 for more details.

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7.2 Handling Interrupts (continued)

7.2.3 Reset Vector

The reset vector of the 'C30 points to memory location 0. The reset vector is handled differently from the other interrupts in that no registers are pushed onto the stack. This vector branches to the initialization (boot) code which, after initializing the delayed branch table in 'C30 RAM, enables interrupt INT0 and then idles waiting for an interrupt.

7.3 Starting Program Execution

The material in Section 7.2, Page 55, serves as a basis for the following discussion. After initialization, the Model 4283 is waiting for an interrupt on INT0. To execute a program, perform the following steps:

1)Configure the board by setting jumper block J4 so that interrupt INT0 is driven from the desired interrupt source. (See Section 2.5, Page 19).

2)From the VMEbus, write the starting address of the program to be executed into the DRAM at VME address DRAM_base + 0x0140. This will appear at 'C30 address 0x0020 0050. DRAM_base is the base of DRAM as set up in Section 4.4, Page 36.

3)Initiate an INT0 interrupt. The factory default configuration for the interrupt jumpers is for the Host Control Register interrupt to be selected. See Section 4.5.1.1, Page 42, for a discussion of this bit.

The EPROM-based INT0 interrupt service routine acknowledges the interrupt as follows:

1)Executes an IACK instruction

2)Adjusts the Stack Pointer

3)Fetches the address stored at location 0x0020 0050 (starting address) and jumps to it.

Thus, immediately following a power on reset, the initialized delayed branch table in the 'C30 RAM can be used without modification to execute a program from any starting address. If desired, the delayed branch table may then be modified for any special requirements.

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7.4 Reset Operation

A simplified schematic of the reset circuitry is given in Figure 7-1, at the top of the next page. There are five sources of reset signals on the board:

SYSRST* This is the VMEbus signal which can be driven by the Model 4283 or can be used as a source of on-board reset, or both. See **Section 3.6.1**, **Page 27**, for more details.

SRST This is the 'C30 Control Register bit which can be used for driving SYSRST. See Section 3.6.1, Page 27, for details.

PONRS* This is the power on reset signal generated by a time constant circuit. It will momentarily be true after +5V DC power is applied to the board

PBRST* This is the push button reset signal derived from the front panel RESET button. This signal is true as long as the button is pressed.

HOSTRST This signal is generated by the Host Control Register and is programmed over the VMEbus. See Section 4.5.1.2, Page 43, for more details.

The power on reset signal PONRS* is also used to reset the MIX Expansion bus and drives the MXRST* line on that bus.

The signal C30RST*, which is the logical 'or' of the four inputs shown above, is delivered to many different devices on the board:

'C30 Control Register Resets all bits to '0', except the VMEINT bit

TMS320C30 CPU Resets the 'C30 itself

VMEbus Master Interface Resets Bus Master state machine circuitry

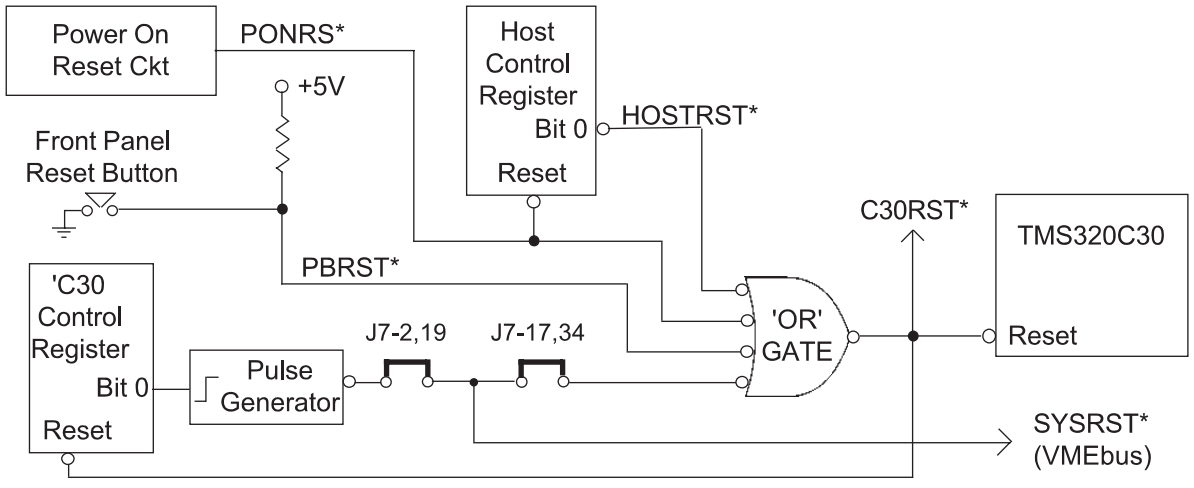


Figure 7-1: Model 4283 - Reset Circuit Schematic

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7.5 VMEbus Interrupter Operation

Interrupts on the VMEbus are generated by interrupters and serviced by **interrupt handlers.** The Model 4283 can act both as an interrupter and an interrupt handler. This section covers the interrupter operation.

The Model 4283 can interrupt the VMEbus on any of seven interrupt levels, 1 through 7. There are several operations involved in the interrupt requester operation:

1) The interrupt driver must be connected to one of 7 bus lines IRQ1 through IRQ7. This is accomplished by setting the IRQ jumpers shown in Figure 7-2.

2) The interrupt acknowledge address must be set to allow the IACK Vector to be interrogated by the VMEbus interrupt handler. This is accomplished by setting IACK Vector Address jumpers as shown in Table 7-2.

3) The IACK Vector register must be loaded by the VMEbus Bus Master (typically the same device as the interrupt handler). This is performed by writing to this register in A16 address space as described in Section 4.5, Page 42.

4) The interrupt is generated by setting the VMEINT flip-flop which is performed when the VMEINT bit in the 'C30 Control Register is set to a logic '1'. This is described in Section 3.6.3, Page 28.

5) The VMEINT flip-flop (and hence the IRQ line on the bus) must be cleared at the end of the interrupt acknowledge cycle. This is performed by re-writing a vector to the IACK Vector Register. This can be the same value each time. The write strobe to this register is connected to the reset pin on the VMEINT flip-flop.

On the next page, the charts and drawings presented in the earlier sections of this manual that are referenced above are reprinted.

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7.5 VMEbus Interrupter Operation (continued)

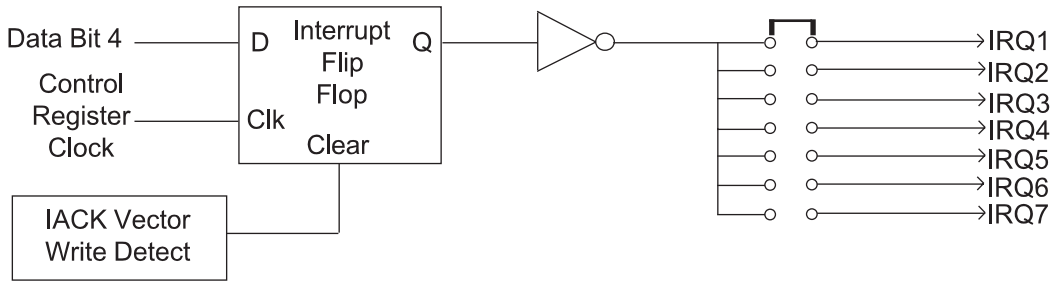


Figure 7-2: Model 4283 - Interrupt Generator Circuitry

Table 7-2: Model4283 - IRQ and IACK Vector Address Jumpers

Int Level	IRQ Jumper	IACK Vector Address Jumpers
1	J1-17,34	J1-10,27 and J1-8,25
2	J1-16,33	J1-10,27 and J1-7,24
3	J1-15,32	J1-10,27
4	J1-14,31	J1-8,25 and J1-7,24
5	J1-13,30	J1-8,25
6	J1-12,29	J1-7,24
7	J1-11,28	none

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7.6 VMEbus Interrupt Handler Operation

The Model 4283 can act as an interrupt handler for the VMEbus on any of seven interrupt levels 1 through 7. In order to prepare the Model 4283 for interrupt handling:

1) Set the VMEbus Interrupt Handler Level jumpers to the correct levels as described in Section 2.5, Page 19. This will cause the INT0 interrupt line on the 'C30 to be driven active when an interrupt occurs.

2) Set the VMEbus board to be serviced so that it generates an interrupt on the desired level and can respond with the IACK Vector. See the operating manual for the board for details. If this board is another Model 4283, see the information in Section 7.5, Page 59, of this manual.

3) Once the system is powered up, write the appropriate IACK Vector to the VMEbus board to be serviced. Information about how to load this register is contained in the operating instructions for that board. If another Model 4283 board is the interrupter, see the information in Section 7.5, Page 59 of this manual.

Section 7.2, Page 55, describes the nature of interrupts and the interrupt vectors which must be in place to start an interrupt service routine for INT0. The following sequence of operations must take place during interrupt handling and should be included in the interrupt service routine:

1) Determine that the source of the INT0 interrupt is due to a VMEbus interrupt by reading the Interrupt Status Register. (See Section 3.7, Page 31)

2) Prepare for an interrupt acknowledge cycle (IACK cycle) by setting the TRSEL bits in the 'C30 Control Register as for TRSEL0 (D5) = 1 and TRSEL1 (D6) = 1. (See Section 3.6.4, Page 31)

3) Set the VMEbus IACK Address Register for the selected interrupt level. (See Section 3.10, Page 33)

4) Perform an IACK cycle by reading from 'C30 address 0x0080 A000. This corresponds to the VMEbus IACK cycle memory mapping. (See Figure 3-2, Page 28) The value returned by the read will contain the IACK Vector from the interrupting device on the bus.

   NOTE: For even INT levels (2, 4, and 6) the 8-bit IACK Vector will appear in bits D0 through D7 of the 32-bit result; for odd INT levels (1, 3, 5, and 7) the IACK Vector will appear in bits D16 through D23 of the 32-bit result.

5) Service the device (load or unload data).

6) Clear the interrupt from the interrupting device.

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7.6 VMEbus Interrupt Handler Operation (continued)

7) Reset the 'C30 IF (interrupt flag) Register bit.

8) Check to see if there are any more interrupts on INT0 and service them.

9) Enable the GIE (Global Interrupt Enable) bit.

7.7 VMEbus Requester (Bus Master) Operation

To access the VMEbus memory space, the 'C30 accesses the region of its memory map between 0x00C0 0000 and 0x00FF FFFF. This 4M x 32 region corresponds to a page of 16 MBytes of VME address space. Prior to accessing VMEbus memory space the following board resources must be set up:

1) Set the VMEbus Address Modifier Register for the desired address mode: A16, A24, or A32. This is described in Section 3.8, Page 31.

2) The 'C30 address is computed by dividing the 24 least significant bits of the VMEbus address by four and adding this to 0x00C0 0000. This is necessary because the 'C30 addresses 32-bit words and the VMEbus addresses 8-bit bytes. The VMEbus 'window' in the 'C30 memory map begins at 0x00C0 0000.

   For A32 address mode operation, the 8 most significant VMEbus address bits (without scaling by four) must be loaded into the Page Address Register as described in Section 3.9, Page 32.

3) The Transfer Select bits (TRSEL0 through TRSEL3) must be set to determine the type of VMEbus transfer. These bits are contained in the 'C30 Control Register (See Section 3.6.4, Page 28).

4) The LOCK bit, also in the 'C30 Control Register, should be set for the desired mode of operation. See Section 3.6.5, Page 30, for more discussion.

Once these facilities have been established, the 'C30 may perform read and write cycles to the VMEbus memory page. When a memory cycle is initiated by the 'C30, the Bus Master Interface on the Model 4283 requests bus ownership by asserting one of the Bus Request lines (BRQ0 through BRQ3). The bus request level is determined by setting jumpers described in Section 2.6, Page 20.

The Bus Arbiter acknowledges the request for bus service and, if it is available, grants the bus to the Model 4283 by sending the appropriate Bus Grant line true (BGIN0 through BGIN3). In response to this grant, the Model 4283 asserts the Bus Busy line (BBSY) during the memory cycle.

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7.7 VMEbus Requester (Bus Master) Operation (continued)

Once granted access to the bus, the Model 4283 retains bus ownership until another master asserts a Bus Request. This scheme is called Release On Request. Alternatively, the TMS320C30 may lock out other access to the bus using the LOCK bit. In general, this bit should be kept low, especially during program development. After programs are successfully debugged, the LOCK bit can be used to boost transfer rates. This bit is also used to create non-separable bus cycles such as Read-Modify-Write cycles. See Section 3.6.5, Page 30.

In troubleshooting bus requester operation, the following items should be checked:

1) Check that the Bus Grant jumpers are correct on the board, on the backplane, and on other boards. Each of the 4 bus request levels uses a daisy chain bus grant line originating from the slot 1 arbiter and passing through each board. The daisy chain input signal to each board is BGINn and the output signal is BGOUTn.

   If the board does use bus request level n, and it is not requesting service, then it must pass the bus grant signal through from BGINn to BGOUTn. This is performed by circuitry on the board which is part of the bus requester function.

   If the board does not use bus request level n, then the bus grant signal must be bypassed around the board at all times. This can be achieved using backplane jumpers or on-board jumpers. See Section 7.9, Page 65, for more details.

   At any rate, in order for any board to conduct a bus cycle it must receive a low (true) bus grant signal at its BGINn input pin.

2) Check that the address modifier codes (AM codes) are being issued correctly as described in Section 3.8, Page 31. Verify which AM code(s) the slave device will respond to. If the VMEbus device being accessed does not respond because the wrong address modifier is used, the bus cycle will fail to complete (DTACK will not be issued).

3) Make sure the transfer select bits are set correctly to match the data width of slave device. For example, if the slave is not capable of conducting a long-word cycle (D32), it will not properly complete the cycle and cause an error.

4) Make sure the correct VMEbus address is used. Remember, an A16 or A24 VMEbus address is accessed by the 'C30 as follows:

   $$\text{'C30 Address} = \frac{\text{VMEbus Address}}{4} + 0x00C0\ 0000$$

   If an A32 address is accessed, the 8 most significant bits must be set in the Page Address Register as described in Section 3.9, Page 32.

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7.7 VMEbus Requester (Bus Master) Operation (continued)

When the Model 4283 attempts to initiate a VMEbus transfer to a memory location at which no VMEbus Slave device exists, it will wait approximately 1 msec before aborting the transfer. This 'bus timeout' condition will cause an interrupt on INT0 of the TMS320C30. In order to distinguish this interrupt from the Host interrupt, the Interrupt Status Register may be read (see Section 3.7, Page 31).

The 'bus timeout' bit in the Interrupt Status Register will remain set until a write to the Interrupt Status Register is performed at 'C30 address 0x0080 0800.

Code for handling the Bus Timeout interrupt is shown below:

```
IntStat  .set  800800h          ; Interrupt Status Register

GenInt   .set  100100h          ; Interrupt Status Register stored here
Timeout  .set  100101h          ; Int Stat Reg stored here only
                                  on Timeout Interrupt
HostISR  .set  2C1h             ; Host Interrupt Service Routine

         ldp   IntStat          ; Point to data page of Int
                                  Status Register
         ldi   @IntStat,r0      ; Get contents of Int Status Reg
         stir  0,@IntStat       ; Clear Int by writing to
                                  Int Stat Reg
         ldp   GenInt           ; Point to Int Stat Reg storage
         ldi   HostISR,r1       ; r1 points to Host ISR
         sti   r0,@GenInt       ; Store General Interrupt Status
         and   1,r0             ; Check for Timeout Interrupt
         bz    r1               ; If not, call Host ISR
         ldi   @GenInt,r0       ; Get stored status
         and   2,r0             ; Check for Host Interrupt
         bnz   r1               ; If not zero must be
                                  Host Interrupt
         ldi   @GenInt,r0       ; If Timeout Int store in
                                  special place
         sti   r0,@Timeout
         reti
```


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7.8 VMEbus Arbiter Operation

The Model 4283 also provides some bus arbitration or 'slot 1' functions. One of these is as a Single-Level Arbiter on level 3. This is enabled by installing jumper J7-15,32 as shown in Section 2.7, Page 20. The Model 4283 looks for a true condition on the BR3 line. If BBSY is not asserted, then the BG3OUT line is asserted granting bus service.

Note that when the Model 4283 is configured as a slot 1 bus arbiter, the Bus Master Interface section must be configured for bus request level 3. The jumper configuration in shown in Section 2.7, Page 20, accomplishes this. Check to make sure that no other Bus Master Interface Bus Request Level jumpers are installed (see Section 2.6, Page 20).

7.9 Bus Grant Bypass

When there are multiple levels of bus grant within the same card cage, then the bus grant signals (BGINn and BGOUTn) which are not used by a given card must be bypassed around its connector. For example, if both level 1 and level 3 bus requests are active within a card cage, then the bus grant lines for level 3 should be bypassed around the board which uses bus request level 1, and vice versa.

There are two methods for bypassing these bus grant signals. The signals can be bypassed on the VMEbus backplane by jumpers which are normally provided for this purpose. Alternately, jumpers on the Model 4283 can be installed which connect BGINn to BGOUTn.

The bypass jumpers for each of the four bus grant levels are shown in Table 7-3, below.

Table 7-3: Model 4283 - Bus Grant Bypass Jumpers

Bus Grant IN/OUT Bypass	Install Jumper
BGIN0 to BGOUT0	J7-7,8
BGIN1 to BGOUT1	J7-9,10
BGIN2 to BGOUT2	J7-11,12
BGIN3 to BGOUT3	J7-13,14

These same jumpers are shown in the Table 2-5, in Section 2.6, Page 20 where the bus request level is set. In that table, all bus request levels other than the level used by the board are bypassed.

7.10 Writing Programming Code to the EPROM

In order to program the EPROMs on the 4283 for a particular application, the application code must be added to the bootcode (see Appendix B) and rebuilt as a unit. The easiest way to do this is to place a branch to _c_int_00 at the first IDLE loop in the assembly code. The Hex30 utility must then be run, which will create the four files necessary for the EPROMs.

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Appendix A: Programming Example

A.1 MIX Module Interrupt Service Routine

The following code for the 'C30 written in C language shows a prototype interrupt handler for a MIX module. The interrupt subroutine is:

```
void Init()

{

*(int *)0x809804 = (int)&c_int01 | 0x60000000;

/* setup int 1 vector jump */

*(int *)0x800000 = 0x00; /* Arm IACK Pal */

*(int *)0x800000 = 0x0e;

asm(" LDI 3,IE"); /* enable interrupt 0 and 1 */

asm(" OR 2000h,ST"); /* enable global interrupts */

}
```

The main program is:

```
c_int01()

{

/* Put code here to clear interrupt from interrupt source */

*(int *)0x800000 = 0x0c; /* Acknowledge 4283 interrupt processor */

*(int *)0x800000 = 0x0e; /* Re-arm 4283 interrupt processor */

asm(" LDI 0,IF"); /* Clear out any spurious interrupts */

}
```


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Appendix B: Model 4283 Bootcode

B.1 General Information

This appendix contains the following source files; written in 'C30 Assembly Language.

- **`asm.bat`** - Batch file code-Page 1
- **`prom30.cmd`** - Linker command file code-Page 2
- **`prom30.asm`** - Monitor program code-Page 3

NOTE: The 4283 uses a wafer scale WS57C256F-70T EEPROM for storing the boot code.

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```
/*****************************************************************************
*
*
*   File :  asm.bat
*
*
*
*****************************************************************************/


asm30 -l %1
lnk30 %1.obj -o %1.out -m %1.map %1.cmd
rom30 -i %1.out
```


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```
/*****************************************************************************
*
*
*   File :  prom30.cmd
*
*
*
*****************************************************************************/


/*****************************************************************************/
/*                      Linker Command File                                  */
/*****************************************************************************/
prom30.obj                      /* Input filename       */
-o prom30.out -m prom30.map     /* Options              */

SECTIONS
{
      init   000h :     { }
      .data  0C0h :     { }
      slook  10Eh :     { }
      sset   116h :     { }
      sgo    11Eh :     { }
      sbreak 146h :     { }
      sieee  173h :     { }
      sc30   18Ah :     { }
      image  200h :     { }
      .text  2B0h :     { }
}
```

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```
/*************************************************************************
*
*
*   File :  prom30.asm
*
*   Description:
*
*
*************************************************************************/



*************************************************************************
*                   TMS320C30 monitor program                           *
*************************************************************************
*
        .sect  "init"
*
BLK0    .set   00809800H   ; Address of internal RAM block 0
                           ; Also destination of image copy operation
*
RESET   .word  INIT        ; Reset Vector
*
INT0    .word  BLK0        ; INT0  Vector
INT1    .word  BLK0+(1*4)  ; INT1  Vector
INT2    .word  BLK0+(2*4)  ; INT2  Vector
INT3    .word  BLK0+(3*4)  ; INT3  Vector
XINT0   .word  BLK0+(4*4)  ; XINT0 Vector
RINT0   .word  BLK0+(5*4)  ; RINT0 Vector
XINT1   .word  BLK0+(6*4)  ; XINT1 Vector
RINT1   .word  BLK0+(7*4)  ; RINT1 Vector
TINT0   .word  BLK0+(8*4)  ; TINT0 Vector
TINT1   .word  BLK0+(9*4)  ; TINT1 Vector
DINT    .word  BLK0+(10*4) ; DINT  Vector
*
RSV     .space 20          ; Reserved space
*
TRAP0   .word  BLK0+(11*4) ; TRAP 0 Vector
TRAP1   .word  BLK0+(12*4) ; TRAP 1 Vector
TRAP2   .word  BLK0+(13*4) ; TRAP 2 Vector
TRAP3   .word  BLK0+(14*4) ; TRAP 3 Vector
TRAP4   .word  BLK0+(15*4) ; TRAP 4 Vector
TRAP5   .word  BLK0+(16*4) ; TRAP 5 Vector
TRAP6   .word  BLK0+(17*4) ; TRAP 6 Vector
TRAP7   .word  BLK0+(18*4) ; TRAP 7 Vector
TRAP8   .word  BLK0+(19*4) ; TRAP 8 Vector
TRAP9   .word  BLK0+(20*4) ; TRAP 9 Vector
TRAP10  .word  BLK0+(21*4) ; TRAP 10 Vector
TRAP11  .word  BLK0+(22*4) ; TRAP 11 Vector
TRAP12  .word  BLK0+(23*4) ; TRAP 12 Vector
TRAP13  .word  BLK0+(24*4) ; TRAP 13 Vector
TRAP14  .word  BLK0+(25*4) ; TRAP 14 Vector
TRAP15  .word  BLK0+(26*4) ; TRAP 15 Vector
TRAP16  .word  BLK0+(27*4) ; TRAP 16 Vector
TRAP17  .word  BLK0+(28*4) ; TRAP 17 Vector
TRAP18  .word  BLK0+(29*4) ; TRAP 18 Vector
TRAP19  .word  BLK0+(30*4) ; TRAP 19 Vector
TRAP20  .word  BLK0+(31*4) ; TRAP 20 Vector
TRAP21  .word  BLK0+(32*4) ; TRAP 21 Vector
TRAP22  .word  BLK0+(33*4) ; TRAP 22 Vector
TRAP23  .word  BLK0+(34*4) ; TRAP 23 Vector
TRAP24  .word  BLK0+(35*4) ; TRAP 24 Vector
TRAP25  .word  BLK0+(36*4) ; TRAP 25 Vector
TRAP26  .word  BLK0+(37*4) ; TRAP 26 Vector
```

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```
TRAP27  .word  BLK0+(38*4) ; TRAP 27 Vector
*
RSV1    .space 4           ; reserve space for TRAPs 28-31
*
        .sect "image"
*
IINT0   BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
IINT1   BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
IINT2   BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
IINT3   BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
IXINT0  BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
IRINT0  BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
IXINT1  BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
IRINT1  BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
ITINT0  BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
ITINT1  BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
IDINT   BR  ISRX           ; INT0 Vector
        NOP
        NOP
        NOP
*
ITRAP0  BR   BRKPNT        ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP1  BR   BRKPNT        ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP2  BR   BRKPNT        ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP3  BR   BRKPNT        ; TRAP 0 Vector
```

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```
         NOP
         NOP
         NOP
ITRAP4   BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP5   BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP6   BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP7   BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP8   BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP9   BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP10  BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP11  BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP12  BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP13  BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP14  BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP15  BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP16  BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP17  BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP18  BR  BRKPNT          ; TRAP 0 Vector
         NOP
         NOP
         NOP
ITRAP19  BR  BRKPNT          ; TRAP 0 Vector
```


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```
        NOP
        NOP
        NOP
ITRAP20 BR  BRKPNT          ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP21 BR  BRKPNT          ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP22 BR  BRKPNT          ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP23 BR  BRKPNT          ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP24 BR  BRKPNT          ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP25 BR  BRKPNT          ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP26 BR  BRKPNT          ; TRAP 0 Vector
        NOP
        NOP
        NOP
ITRAP27 BR  BRKPNT          ; TRAP 0 Vector
        NOP
        NOP
IEND    NOP
*
ISIZE   .set IEND-IINT0     ; size(-1) of image to be copied
                            ; = 9C(-1)(hex) = 156(-1)(decimal)
*
        .data
ZERO    .word 00000000H     ; Holds a zero
MASK    .word 00000001H     ; Holds interrupt mask
STCK    .word 00809D00H     ; Holds address of Stack in internal RAM
EXTRAM .word 00100000H      ; Holds address of external ram
BCREG   .word 00808064H     ; Holds address of bus control register
EPROM   .set 00000000H      ; Address of Bottom of EPROM
SRCE    .word IINT0         ; Source address for copy
DEST    .word BLK0          ; Destination address for copy
PATTRN .word 12345678H      ; Pattern to test byte ordering in New Host
DPRBOT .set 00200000H       ; Address of Bottom of Dual-Ported RAM
DPR     .set 00000050H      ; Address of mailbox in dual-ported ram
ARG1    .set 00000051H      ; Address of mailbox in dual-ported ram
ARG2    .set 00000052H      ; Address of mailbox in dual-ported ram
RDY     .set 00000053H      ; Address of mailbox in dual-ported ram
TEST    .set 00000054H      ; Address of mailbox in dual-ported ram
*
        .text
INIT    LDI  80h,DP         ; Point to control register
        LDI  0,R0
        STI  R0,@0          ; Clear Control Register
        STI  R0,@8060h      ; Clear Expansion Bus Control Register
        LDP  EPROM          ; Point to EPROM
        LDI  @MASK,IE       ; Unmask INT0
        LDI  @STCK,SP       ; Set Stack Pointer
```

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```
        LDI  @BCREG,AR0     ; Address of bus control register
        LDI  10E0H,R0       ; Mask to disable internal wait state counter
        STI  R0,*AR0        ; Store mask in bus control register
COPY:                       ; Copy the interrupt and trap vector image
                            ;      from EPROM to start of internal RAM
        LDI  @SRCE,AR0      ; Source address
        LDI  @DEST,AR1      ; Destination address
        LDI  *AR0++,R0      ; Load the first source contents
        RPTS ISIZE          ; Repeat following instruction SIZE+1 times
        LDI  *AR0++,R0      ; Load the next one and ...
||      STI  R0,*AR1++      ; Store the previous one
        STI  R0,*AR1        ; Store the last one
*
        LDI  @PATTRN,R0     ; Get test pattern
        LDP  DPRBOT         ; Point to DPR
        STI  R0,@TEST       ; Write test pattern to DPR
*
        LDI  0,R0           ; Clear R0
        LDI  0,AR0          ; Clear AR0
        LDI  0,AR1          ; Clear AR1
*
        OR   2000H,ST       ; Global Int Enable
        IDLE                ; Wait for Interrupt
*
ISRX    IACK  @0            ; Command Interrupt Service
        PUSH  R0            ; Adjust Stack Pointer
        PUSH  DP            ; Save Data Page Pointer
        PUSH  ST            ; Save Status Register
        LDP   DPRBOT        ; Load DP needed to point to DPR
        LDI   @DPR,R0       ; Get Command
        LDP   EPROM         ; Point to EPROM data page
        BU    R0            ; Execute Command
*
        .sect "slook"       ; Loaded @ 10EH
        LDI   @LCMD,R0
        BU    R0
*
      .sect "sset"          ; Loaded @ 116H
      LDI   @SCMD,R0
      BU    R0
*
      .sect "sgo"           ; Loaded @ 11EH
      LDI   @GCMD,R0
      BU    R0
*
      .sect "sbreak"        ; Loaded @ 146H
      LDI   @BCMD,R0
      BU    R0
*
      .sect "sieee"         ; Loaded @ 173H
      LDI   @ICMD,R0
      BU    R0
*
      .sect "sc30"          ; Loaded @ 18AH
      LDI   @CCMD,R0
      BU    R0
*
      .data
LCMD  .word LOOK            ; Address of LOOK command
SCMD  .word SET             ; Address of SET command
GCMD  .word GO              ; Address of GO command
BCMD  .word BREAK           ; Address of BREAKOUT command
ICMD  .word IEEE2C30        ; Address of IEEE_to_C30 command
CCMD  .word C302IEEE        ; Address of C30_to_IEEE command
```

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```
       .word 0              ; Leave some spares
       .word 0
       .word 0

*
       .text
LOOK   LDP   DPRBOT         ; Point to DPR
       LDI   @ARG1,AR2      ; Get Address
       LDI   *AR2,R0        ; Get Contents of Address
       STI   R0,@ARG2       ; Return Contents in Arg #2
       LDI   1,R0
       STI   R0,@RDY        ; Set Ready Flag
       POP   DP
       SUBI  3,SP           ; Adjust SP
       OR    2000H,ST       ; Global Int Enable
       IDLE                 ; Wait for Interrupt
*
SET    LDP   DPRBOT         ; Point to DPR
       LDI   @ARG1,AR2      ; Get Address
       LDI   @ARG2,R0       ; Get Data
       STI   R0,*AR2        ; Store Data at Address
       LDI   1,R0
       STI   R0,@RDY        ; Set Ready Flag
       POP   DP
       SUBI  3,SP           ; Adjust SP
       OR    2000H,ST       ; Global Int Enable
       IDLE                 ; Wait for Interrupt
*
GO     LDP   DPRBOT         ; Point to DPR
       LDF   @3,R1          ; Restore Machine State
       LDI   @2,R1
       LDF   @5,R2
       LDI   @4,R2
       LDF   @7,R3
       LDI   @6,R3
       LDF   @9,R4
       LDI   @8,R4
       LDF   @11,R5
       LDI   @10,R5
       LDF   @13,R6
       LDI   @12,R6
       LDF   @15,R7
       LDI   @14,R7
       LDI   @16,AR0
       LDI   @18,AR1
       LDI   @20,AR2
       LDI   @22,AR3
       LDI   @24,AR4
       LDI   @26,AR5
       LDI   @28,AR6
       LDI   @30,AR7
       LDI   @34,IR0
       LDI   @36,IR1
       LDI   @38,BK
       LDI   @40,SP
       LDI   @44,IE
       LDI   @46,IF
       LDI   @48,IOF
       LDI   @50,RS
       LDI   @52,RE
       LDI   @54,RC
       LDI   @56,R0         ; Get PC From DPR
       PUSH  R0             ; Get it ready for RETI
       LDF   @1,R0
```

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```
        LDI   @0,R0
        LDIU  @42,ST          ; Restore ST
        LDIU  @32,DP          ; Restore DP
        RETI
*
BRKPNTPUSH  DP
        PUSH  ST
        LDP   DPRBOT
        STI   R0,@0
        STF   R0,@1
        STI   R1,@2
        STF   R1,@3
        STI   R2,@4
        STF   R2,@5
        STI   R3,@6
        STF   R3,@7
        STI   R4,@8
        STF   R4,@9
        STI   R5,@10
        STF   R5,@11
        STI   R6,@12
        STF   R6,@13
        STI   R7,@14
        STF   R7,@15
        STI   AR0,@16
        STI   AR1,@18
        STI   AR2,@20
        STI   AR3,@22
        STI   AR4,@24
        STI   AR5,@26
        STI   AR6,@28
        STI   AR7,@30
        STI   IR0,@34
        STI   IR1,@36
        STI   BK,@38
        POP   R0              ; Get ST
        STI   R0,@42          ; Save it
        STI   IE,@44
        STI   IF,@46
        STI   IOF,@48
        STI   RS,@50
        STI   RE,@52
        STI   RC,@54
        POP   R0              ; Get DP
        STI   R0,@32          ; Save it
        POP   R0              ; Get PC
        STI   R0,@56          ; Save it
        STI   SP,@40          ; Store correct Stack Pointer
        LDI   1,R0
        STI   R0,@RDY         ; Set Ready Flag
        LDI     @32,R0        ; fix actual DP
        LDI     R0,DP
        LDI     1,IE          ; only allow INT0 until we start again
        OR    2000H,ST        ; Global Int Enable
        IDLE                  ; Wait for Interrupt
*
BREAK LDP   DPRBOT            ; Point to DPR
        SUBI  2,SP            ; SP points to R0
        POP   R0              ; SP points to PC
        STI   R0,@0           ; Save R0 (integer)
        STF   R0,@1           ; Save R0 (float)
        POP   R0              ; Get PC
        STI   R0,@56          ; Save it
        STI   R1,@2
```

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```
      STF   R1,@3
      STI   R2,@4
      STF   R2,@5
      STI   R3,@6
      STF   R3,@7
      STI   R4,@8
      STF   R4,@9
      STI   R5,@10
      STF   R5,@11
      STI   R6,@12
      STF   R6,@13
      STI   R7,@14
      STF   R7,@15
      STI   AR0,@16
      STI   AR1,@18
      STI   AR2,@20
      STI   AR3,@22
      STI   AR4,@24
      STI   AR5,@26
      STI   AR6,@28
      STI   AR7,@30
      STI   IR0,@34
      STI   IR1,@36
      STI   BK,@38
      ADDI  4,SP            ; SP points to ST
      POP   R0              ; R0 = ST, SP points to DP
      STI   R0,@42          ; Save it
      STI   IE,@44
      STI   IF,@46
      STI   IOF,@48
      STI   RS,@50
      STI   RE,@52
      STI   RC,@54
      POP   R0              ; R0=DP, SP points to R0
      STI   R0,@32          ; Save DP
      SUBI  2,SP            ; SP is balanced
      STI   SP,@40          ; Store correct Stack Pointer
      LDI   1,R0            ; Get a "1" and
      STI   R0,@RDY         ; set it into the Ready Flag
      LDI   @32,R0          ; fix actual DP
      LDI   R0,DP
      LDI   1,IE            ; only allow INT0 until we start again
      OR    2000H,ST        ; Global Int Enable
      IDLE                  ; Wait for Interrupt
*
      .data
CTAB  .word 0FF800000H      ; Table for ieee format conversion
      .word 0FF000000H
      .word 07F000000H
      .word 080000000H
      .word 081000000H
*
TABA  .word   CTAB
*
      .text
IEEE2C30:
      LDP   DPRBOT
      LDI   @ARG1,AR0       ; Get Address of Array
      LDI   @ARG2,RC        ; Get Length of Array

      SUBI    1,RC          ; RC <= n - 1
      LDP     @CTAB         ; Load data page pointer
      LDI     @TABA,AR1     ; AR1 -> constant table
```

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```
;     IEEE -> 'C30 conversion loop

      RPTB    LOOP4         ; Repeat loop n times
      AND     *AR0,*AR1,R0  ; Replace fraction with 0
      ADDI    *AR0,R0       ; Shift sign and exponent inserting 0
      LDIZ    *+AR1(1),R0   ; If all zero, load 'C30 0.0
      LDI     *AR0,R1       ; Test original number
      BGED    LOOP4         ; If >= 0, store number (delayed)
      SUBI    *+AR1(2),R0   ; Remove exponent bias (127)
      PUSH    R0            ; Save as an integer
      POPF    R0            ; Unsave as a flt. pt. number

      NEGF    R0            ; Negate 'C30 number

LOOP4:STF     R0,*AR0++     ; Store 'C30 number, incr. AR0
*
      LDP   DPRBOT
      LDI   1,R0
      STI   R0,@RDY         ; Set Ready Flag
      POP   DP
      SUBI  3,SP            ; Adjust SP
      OR    2000H,ST        ; Global Int Enable
      IDLE                  ; Wait for Interrupt

C302IEEE:
      LDP   DPRBOT
      LDI   @ARG1,AR0       ; Get Address of Array
      LDI   @ARG2,RC        ; Get Length of Array

      SUBI  1,RC            ; RC <= n - 1
      LDP     @CTAB         ; Load data page pointer
      LDI     @TABA,AR1     ; AR1 -> constant table

;       'C30 -> IEEE conversion loop

      RPTB    LOOP5         ; Repeat loop n times
      ABSF    *AR0,R0       ; Test |number|
      LDFZ    *+AR1(4),R0   ; If == 0, load fake 0.0
      LSH     1,R0          ; Shift off sign bit
      PUSHF   R0            ; Save as a flt. pt.
      LDF     *AR0,R1       ; Test original number
      BGED    LOOP5         ; If >= 0, store number (delayed)
      POP     R0            ; Unsave as an integer
      ADDI    *+AR1(2),R0   ; Add exponent bias (127)
      LSH     -1,R0         ; Adjust for sign bit
      OR      *+AR1(3),R0   ; Negate IEEE number

LOOP5:STI   R0,*AR0++       ;Store IEEE number, incr. AR0
*
      LDP   DPRBOT
      LDI   1,R0
      STI   R0,@RDY         ; Set Ready Flag
      POP   DP
      SUBI  3,SP            ; Adjust SP
      OR    2000H,ST        ; Global Int Enable
      IDLE                  ; Wait for Interrupt
*
      .end
```

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