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Operating Manual

Models 4290 and 4291

TMS320C6201 and TMS320C6701
Digital Signal Processors for VME bus

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Pentek Models 4290 and 4291 Operating Manual – Revision History

Date	Rev	Applicable Serial #'s	Comments
1996 – 12/98	Prelim – .007	199805000259 – Forward	Contact Factory for manual change history.
1/29/99	A	199805000259 – Forward	Added Chapter 3 on Firmware Self–Tests. Rearranged memory maps so they are now, Local, Global, and VME. This also corresponds to the layout of the manual. Corrected JTAG A16 address from **0x004F** to **0x007F**. Renamed the description of the Dual Port SRAM Mailbox Interrupt Registers in Table 4–2. Corrected the offset of the Global Registers in the Global Bus Memory Map.
8/12/99	B	199805000259 – Forward	Added default register values for most of the registers. Added section on bypassing user boot code. Removed sentence on the incoming & outgoing FIFO flags stating that Almost Full was related to Outgoing FIFO and Almost Empty was related to Incoming FIFO. Added new flowcharts for firmware functions in Section 3.12. Added section on DPSRAM mailbox registers in Chapter 6.
9/19/01	C	199805000259 – Forward	COMPLETE rewrite and reorganization. Most figures, tables & text changed in some way. Added info on Options 316, 320 & 330. Programming Examples removed (replaced by ReadyFlow). JTAG Controller App note added.
10/31/01	C.1	199805000259 – Forward	Update Operating Humidity and Storage Temperature and Humidity specs (Sec. 1.7, pg. 30). Corrected range of Page Register settings for VMEbus Master access – this affects Table 4–3 (pg. 65), the header and text in Sec. 4.2.10 (pg. 80), and Tables 5–15 & 5–16 (pgs 140–141). Correct guaranteed Operating Temperature range, add a max. Supply Voltage spec and Correct Supply Voltage measurment point for Option 316 operating at 40 MHz – this affects Sec. 6.5.2 (pg. 173). Correct address of Boot_Status Flag and starting address of VIM_Code region – this affects Figures 8–1 and 8–2 (pgs. 200 & 201), and Tables 8–2 & 8–3 (pg. 202) and 8–13 (pg. 214).
11/21/01	C.2	199805000259 – Forward	Correction to Fig. 2–4b: GND & T1 IN pins were swapped. Also corrected text in 2nd paragraph of Sec. 2.3.5 to agree with corrected figure.
10/29/02	D	199805000259 – Forward	Corrections to Chapter 8 – additions & changes to the boot flowcharts (Figs 8–1 & 8–2), Sec. 8.3 (corrected info re: BCR, D5), Table 8–7 (address corrections), Secs. 8.5.6 (test results should be read out via VME) & 8.5.7 (clarify what gets tested when), Table 8–13 (changed a comment & noted that Cache_Ckr address applies only to Opt. 330), and Figs. 8–3 & 8–4 (add note re: accessing regions other than Global SRAM , via Page Reg.)

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Chapter 1: Overview

1.1 General Information

Pentek's Model 4290 for VMEbus systems features the Texas Instruments' TMS320C6201 fixed−point Digital Signal Processor, which employs the VelociTI™ architecture and operates at a clock rate of 200 MHz. Incorporating four of these devices, the Model 4290 is a single−slot, 6U VMEbus board delivering up to 6400 MIPS of processing power. The Model 4291 features Texas Instruments' TMS320C6701 floating−point DSP, also employing the VelociTI™ architecture and operating at a clock rate of 167 MHz. With four of these devices on board, the Model 4291 is a single−slot, 6U VMEbus board that delivers up to 4 GFLOPS of processing power. Both boards incorporate a wealth of high−speed interface options to handle the 'C6x* processors' voracious appetites for data.



Throughout this manual, the term 'C6x will be used to refer to either the fixed-point 'C6201 processor or the floating-point 'C6701 processor. Specific references to processor part numbers will be used only when there is a need to differentiate between the fixed- and floating-point devices.

These boards are organized as four identical 'C6x processing nodes, each equipped with several types of I/O and memory resources. This unique architecture has been optimized for handling the most demanding real−time signal processing applications in high−performance VMEbus systems. Since the fixed−point 'C6201 and the floating−point 'C6701 share a common set of development tools , you can easily migrate code developed for either device to the other. Models 4290 and 4291 are architecturally identical and support the same set of peripheral interfaces.

1.2 Features

❑ Model 4290

- Four TMS320C6201 fixed−point DSPs operating at 200 MHz
- 6400 MIPS performance

❑ Model 4291

- Four TMS320C6701 floating−point DSPs operating at 167 MHz
- 4 GFLOPS performance

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1.2 Features (continued)

Common Features

- ❑ Memory resources for each processor:
- 16 MBytes SDRAM
- 512 kBytes zero−wait Synchronous Burst SRAM
- 256 kBytes Dual Port SRAM
- ❑ I/O resources for each processor:
- Two serial full duplex ports for VIM mezzanine I/O
- Memory access to VIM mezzanine
- 2 k x 32 Bi−directional FIFO (1 k x 32 in each direction) for VIM mezzanine board I/O
- Two 2 k x 32 Bi−directional FIFOs (1 k x 32 in each direction) for inter−processor communication
- ❑ Global bus resources accessible by all processors and VMEbus:
- Four 256 kByte Dual Port SRAMs
- 8 kBytes of fast, Non−Volatile SRAM
- 8 MBytes Flash EEPROM memory for 'C6x boot code and user applications
- 2 MBytes Global SRAM for sharing common data
- Memory−mapped slave expansion for other memory and I/O
- Host port for all four processors
- ❑ Velocity Interface Mezzanine (VIM) adapters for application−specific front panel I/O
- ❑ Optional P2 interfaces: RACEway, custom I/O
- ❑ VME64 master/slave interface
- ❑ VME memory−mapped J−TAG controller
- ❑ Software development tools for UNIX and Windows 95/98/NT workstations

1.3 The DSP Nodes

The Digital Signal Processing Nodes on the Models 4290 and 4291 consist of the 'C6x DSPs and their local resources, which include blocks of Synchronous Burst Static RAM (SBSRAM), Synchronous Dynamic RAM (SDRAM) and a Dual Ported Static RAM (DPSRAM) which is also accessible from the Global Bus. The Nodes also include Bi−Directional FIFO structures (referred to herein as Bi−FIFOs, or sometimes simply as BIFOs) for exchanging data with the VIM expansion port and with other on−card DSPs, in addition to buffers for direct access to the VIM expansion card and the Global bus. These resources will be described in more detail in the subsections beginning at the top of the next page.

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1.3 The DSP Nodes (continued)

1.3.1 Digital Signal Processors

The heart of each Processing Node is the fixed−point TMS320C6201 running at 200 MHz on the Model 4290, or the floating−point TMS320C6701 running at 167 MHz on the Model 4291. Each 'C6x communicates with all its local resources via its local data bus, named the V−bus after the VelociTI™ architecture. The V−Bus is capable of running at the full bandwidth provided by the 'C6x's External Memory Interface (EMIF), i. e., 200 MHz on the Model 4290, or 167 MHz on the Model 4291.

1.3.2 Synchronous Burst SRAM

512 kBytes of Synchronous Burst SRAM (SBSRAM) configured as 128 k x 32 is provided as the processors' high−throughput, memory resource. The SBSRAM is the fastest memory on the board, delivering zero−wait state performance for maximum utilization of the 'C6x data bus at 800 MB/sec for the 4290, or 667 MB/sec for the 4291. This memory resource may be used to store critical data or program code which must be accessed frequently, and is accessible to to the Node's 'C6x processor only, as a private resource.

1.3.3 Synchronous DRAM

The SDRAM provides a large, fast 16 MByte work space operating at transfer rates of up to 400 MB/sec for the 4290, or up to 333.2 MB/sec for the 4291. Unlike the SBSRAM, which can provide continuous random access at up to 800 MB/sec, care must be taken when using the SDRAM, as there is a 60 nsec row−access penalty whenever a page boundary is crossed. However, after the row access penalty, all subsequent accesses within the same page will take only two 'C6x clock cycles, thus offering up to 400 MB/s of throughput, using 32−bit transfers. Like the SBSRAM, this memory resource is accessible to the node's 'C6x processor only, as a private resource.

1.3.4 Dual Port SRAM

The Dual Port SRAM (DPSRAM) attached to each Processing Node is a critical element to the power of the Model 4290/4291 architecture. Two size options are available for this resource − Option 244 offers a total of 1 MByte of DPSRAM, and Option 240 provides a total of 512 kBytes. In either case, the DPSRAM is divided into four blocks, with each block ported to one node's Local bus (also known as the V−bus) on one side, and the Global bus on the other. This configuration provides an efficient data transfer resource between each processing node and the VMEbus. Each block is further divided into four banks, and mastership of each bank is obtained separately, by semaphore. This design provides a high− throughput memory device that minimizes Global bus traffic. The structure additionally provides 8 mailbox resources (4 in each direction) between the processor and the Global bus. These offer an efficient means to transfer messages between the VMEbus and each processing node.

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1.3 The DSP Nodes (continued)

1.3.4 Dual Port SRAM (continued)

The performance benefits of this architecture can be realized in two ways. First, because the memory block is dual ported between its Processing Node and the Global bus, a single access is all that is required to transfer a 32−bit word of data between the VMEbus and each Processing Node. This offers a greater than 100% performance improvement over traditional Global shared memory architectures, which require data be transferred into the Global resi−dent SRAM, another arbitration cycle performed, and then transferred out of the Global memory. That would not only take twice as long, but would tie up the Global bus for other processors and for interprocessor communication.

Secondly, due to the large depth of the DPSRAM utilized, the distributed structure significantly increases the size of the available Global memory.

1.3.5 Inter−processor Bi−FIFOs

An essential feature of an effective multiprocessor device is the ability for each Processing Node to be able to effectively and efficiently exchange data with the other processors. The architecture employed on the Models 4290 and 4291 allows each Processing Node to communicate with the two adjacent Nodes. The interprocessor Bi−FIFOs connect the V−buses of adjacent 'C6xs and are ideal for pipelined processing applications, in that they minimize data movement overhead and maximize interprocessor communications speed.

A proprietary, switched−bank, Bi−FIFO scheme allows interprocessor com−munication to occur at up to 100 MB/sec per path on the 4290 (160 MB/sec for Option 316), or up to 83.3 MB/sec per path on the Model 4291 (133.3 MHz for Option 316), along with the ability to utilize multiple paths concurrently. Additionally, the Bi−FIFO scheme passes data directly between the processors eliminating the delays associated with arbitration and traffic associated with a traditional Global bus−based scheme. Either interrupts or polling can be used to determine transfer status through the use of a progammable flag.

1.3.6 The VIM Mezzanine Interface

Velocity Interface Mezzanine (or VIM) boards, providing a rich variety of I/O and peripheral functions, are supported by three high−speed paths to all four 'C6x processors. For extremely high−speed, 32−bit parallel data peripherals such as VIM wideband A/D converters, each of the four mezzanine Bi−FIFOs deliver up to 100 MB/sec for input or output streams to/from the V−bus on the Model 4290 (160 MB/sec for Option 316), or up to 83.3 MB/sec on the Model 4291 (133.3 MHz for Option 316). The Bi−FIFOs effectively decouple the mezzanine device data flow and allows the 'C6x's to move data effi−ciently, for maximum processor utilization.

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1.3 The DSP Nodes (continued)

1.3.6 The VIM Mezzanine Interface (continued)

Two serial ports per processor support high−speed serial peripherals such as high−performance codecs. Each 'C6x is also provided with a 32−bit micro−processor bus interface to the mezzanine, for control and status functions. This interface is a buffered version of the V−bus. A path to the VMEbus P2 backplane connector supports optional RACEway VIM interfaces.

The VIM architecture allows a variety of application−specific front panel con−nectors including both analog and digital signal interfaces. VIM board func−tions include multichannel digital receivers and transmitters, data acquisition subsystems, multichannel codecs, high−speed A/D and D/A converters, 'C40−compatible Comm Port interfaces, high−speed parallel digital I/O, and custom boards for special applications.

1.3.7 'C6x Processor Locations and Labeling

JTAG chain considerations require that the processors that are connected to the chain be labeled with numbers. However, Pentek prefers to designate processors with letters to avoid confusion with our I/O product labeling scheme, which designates I/O channels with numbers. Table 1−1, below, shows how the Processor Letter and JTAG Processor number correlate with each other.

Table 1−1: Model 4290/4291 - 'C6x Processor Designations

Processor Letter	Processor JTAG Number
A	0
B	3
C	1
D	2

1.3.8 'C6x Interrupts

Each 'C6x processor has four input pins for receiving external interrupts, EXT_INT7 through EXT_INT4. All four inputs are edge sensitive, and the edge is programmable (i. e., negative or positive). Each interrupt pin is assigned to a logical function which has multiple interrupt sources behind it. The mapping of logical function to interrupt for the standard Model 4290/4291 is shown at the top of the next page, in Table 1−2. In order to determine the source of the interrupt, the interrupt handler needs to poll the Interrupt Flag Registers (see Section 4.3.2.2).

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1.3 The DSP Nodes (continued)

1.3.8 'C6x Interrupts (continued)

Table 1-2: Standard Model 4290/4291 - 'C6x Interrupt Source Mapping		
External Interrupt	**Description**	**Additional Information**
EXT_INT7	Bi-FIFO Status, VIM / Global bus Expansion	Sections 4.3.2.4 & 6.4.3
EXT_INT6*	Dual Port SRAM Mailboxes	Sections 4.3.2.4 & 7.2.3
EXT_INT5	Bi-FIFO Mailboxes	Sections 6.4.3.1 & 6.4.3.2
EXT_INT4	VIC64 and VMEbus	Section 5.6
*** - When using Pentek's SwiftNet protocols to communicate with your Model 4290/4291, EXT_INT6 is used by SwiftNet. NOTE: Interrupt mapping is programmable on the Model 4290/4291 Option 330. See Section 4.3.2.9.**		

Each motherboard resident interrupt source is associated with three control register bits that affect its operation. These are the interrupt enable, interrupt flag, and interrupt status bits. The enable bit associated with the interrupt allows the indicated source to generate an interrupt when its flag becomes active. When the bit is set, an interrupt is generated by the condition. The interrupt flag is a latched version of the interrupt source, which latches and holds the condition (even after it is rescinded) until the processor clears the flag. The interrupt status bit is a raw (unlatched) version of the interrupt flag. The bit is set when the condition is active (e. g., Bi–FIFO Half–full = 0). The status bit is read only, the flag bit is read/clear, and the enable bit is read/write.

1.3.9 'C6x Endian

The 'C6x processors on most versions of the Models 4290 and 4291 are configured as big endian devices, and this configuration cannot be changed. When compiling code for these Model 4290s or 4291s, your compiler's switches must be set for big endian.

The exception to this rule is units equipped with Option 330. On these devices, the endian mode of the processors can be configured by a jumper as either big endian (the default setting) or little endian. For further information, please refer to Section 2.2.7.

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1.4 Global Bus Resources

In addition to the four Dual Port SRAM blocks (shared with the 'C6x processor Nodes, see Section 1.3.4) the Global bus on the Models 4290 and 4291 provides access to the following resources: 2 MBytes of shared SRAM (which we refer to as the Global SRAM); 8 kBytes of Non−Volatile SRAM (NVSRAM); 8 MBytes of Flash EEPROM; and the VME64 Master/Slave Interface. The Global bus may be mastered by VME, or by any of the on−board 'C6x processors.

The Models 4290 and 4291 also feature a Global bus expansion interface, which allows for the expansion of shared global resources including memory and I/O.

1.4.1 Global SRAM

The board contains 2 MBytes of traditional, shared SRAM, residing on the shared Global bus, configured as 512 k x 32, which is accessible by all four 'C6x processors and the VMEbus. This structure provides a large shared resource that may be used to pass data between all the potential Global bus masters. This memory resource may be accessed for 32−, 16−, or 8−bit transfers by the VMEbus, or by any of the on−board 'C6x processors for 32−bit transfers.

1.4.2 Non−Volatile SRAM

The Models 4290 and 4291 are equipped with 8 kBytes of fast, non−volatile memory. This resource provides a quick and easily accessible storage space for things like board parameters and critical values. It is accessible by all four 'C6x processors and the VMEbus.

1.4.3 Flash EEPROM

The Models 4290 and 4291 contain 8 MBytes of Flash EEPROM configured as 2 M x 32, which acts as the board's non−volatile storage and a boot resource for the processors. This structure is accessible from any of the processors, and from the VMEbus.

1.4.4 VME64 Master Interface

The Models 4290 and 4291 contain a full−featured VME64 interface based on the Cypress VIC64/CY7C964 chipset. This device supports D32 and D64 block transfers as both a master and slave. As a master, the entire VME address space is accessible in A32, A24 an A16 addressing modes. The interface allows each 'C6x processor to directly master the VMEbus, allowing them to move data or perform control and status transfers to virtually any VMEbus device. Single accesses are also supported for A32, A24 an A16 addressing modes as both master and slave. The interface additionally has system controller capability and can act as a VMEbus interrupt generator and handler.

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1.4 Global Bus Resources (continued)

1.4.5 Global Slave Expansion Bus

The Model 4290 provides a global bus expansion interface which allows for the expansion of shared global resources including additional memory and I/O.

1.4.6 J–TAG Controller

An on–board JTAG controller is provided to allow VMEbus access to the processor's emulator port. The controller, a 74ACT8990, is accessible in the board's A16 VME memory space, allowing emulation across the VMEbus. Pentek's SwiftNet Communication Protocols provide a path for seamless integration of third party tools, like Texas Instruments' Code Composer.



Prior to executing code using an XDS emulator, the 'C6x processor's Timer 0 should be disabled. If Timer 0 is not disabled, then when code is loaded by the emulator, the interrupt vector table or interrupt handler may be inadvertently overwritten. To disable Timer 0, immediately after entering the main routine in your code, use:

```
* (unsigned int *) 0x0194 0000 = 0;
```

1.5 Recommended Reference Material on 'C6x Processors

A comprehensive collection of reference materials on the operation and programming of the 'C6x family is available on Texas Instruments' web site, http://www.ti.com. The link below (valid at the time of this document's publication, but obviously subject to change) brings you directly to an area where such material may be downloaded:

http://dspvillage.ti.com/docs/catalog/dspplatform/dspplatform.jhtml?familyID=132

1.6 Block Diagram

A functional block diagram of Pentek's Models 4290 and 4291 is shown in Figure 1–1, on the next page.



The Block Diagram represents the arrangement of the processors from an ELECTRICAL point of view, rather than a PHYSICAL point of view. On the 4290/4291 PC board, the processors are arranged with A at the top, then B, then C, and D at the bottom. The arrangement used in the block diagram was chosen to more clearly represent the flow of JTAG signals.

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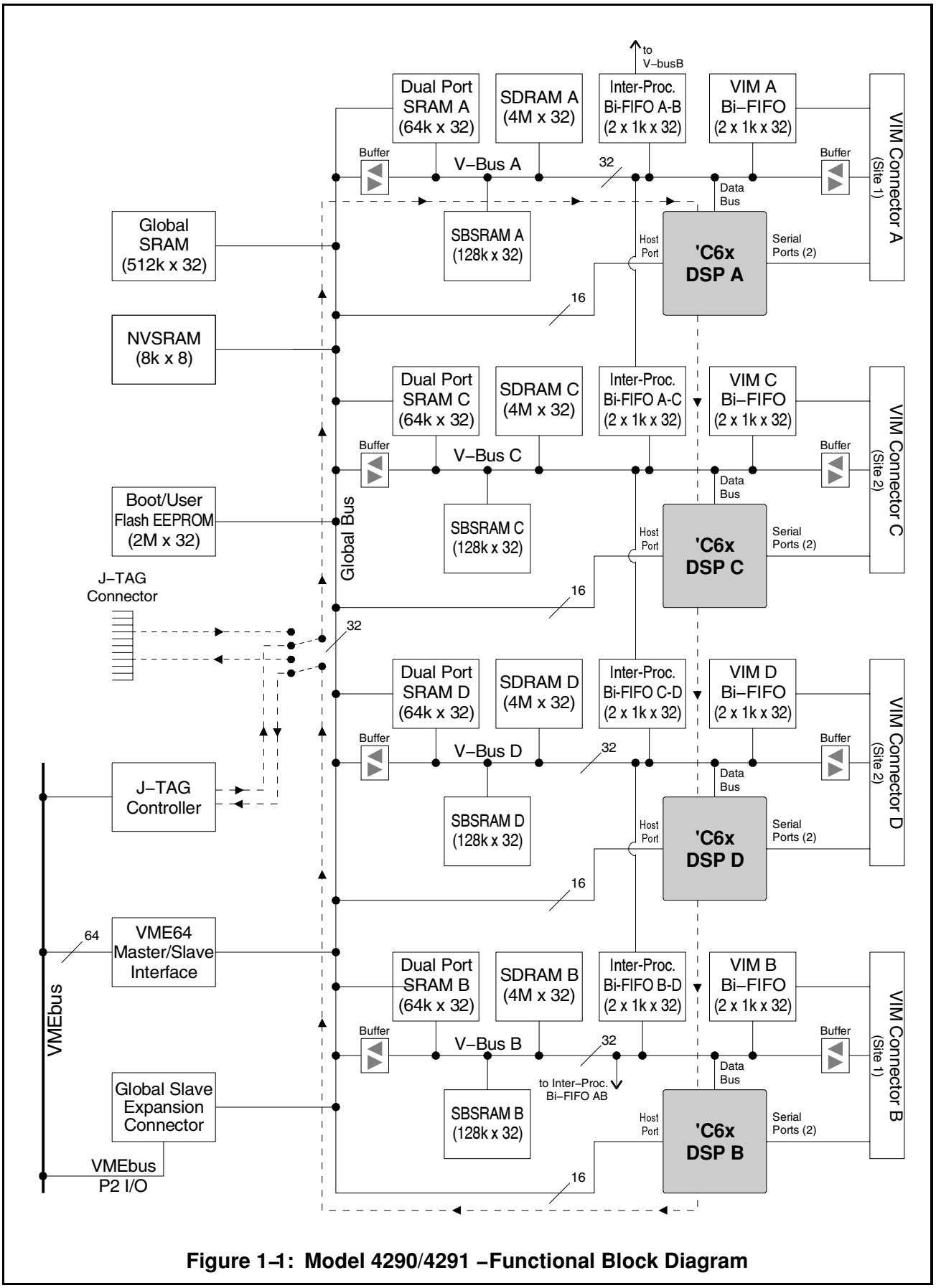


Figure 1–1: Model 4290/4291 –Functional Block Diagram

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1.7 Model 4290/4291 Specifications



All access speed specifications assume a Rev. 3.0 (or higher) TMS320C6201 processor operating at 200 MHz, for the Model 4290, or a Rev. 3.0 (or higher) TMS320C6701 processor operating at 167MHz, for the Model 4291.

Processors:

Type:	Texas Instruments TMS320C6201 (Model 4290) Texas Instruments TMS320C6701 (Model 4291)
Quantity:	4
Clock Speed:	
Model 4290:	200 MHz
Model 4291	167 MHz
Address Bus:	32 Bits
Data Bus:	32 Bits

Memory:

Synchronous Burst SRAM (SBSRAM):

Blocks:	4 (one per processor)
Size:	
Option 244:	512 kBytes (128k x 32) each block, 2 MBytes total
Option 240:	128 kBytes (32k x 32) each block, 512 kBytes total
Arbitration:	None (each block accessible only to one 'C6x processor)
'C6x Access Modes:	8–bit, 16–bit and 32–bit
'C6201 Access (4290):	1 clock access, 800 MB/sec @ 32 bits, after priming pipe
'C6701 Access (4291):	1 clock access, 667 MB/sec @ 32 bits, after priming pipe
VMEbus Access:	None

Synchronous DRAM (SDRAM):

Blocks:	4 (one per processor)
Size:	16 MBytes (4M x 32) each block, 64 MBytes total
Arbitration:	None (each block accessible only to one 'C6x processor)
'C6x Access Modes:	8–bit, 16–bit and 32–bit
'C6201 Access (4290):	0 Wait State, 2 clock access, 400 MB/sec @ 32 bits
'C6701 Access (4291):	0 Wait State, 2 clock access, 333 MB/sec @ 32 bits
VMEbus Access:	None

Global SRAM:

Blocks:	1
Size:	2 MBytes (512k x 32)
Arbitration:	Rotating Priority
'C6201 Access:	35 clock access, 22 MB/sec @ 32 bits, after Global bus arbitration
'C6701 Access:	35 clock access, 19 MB/sec @ 32 bits, after Global bus arbitration
'C6x Access Mode:	32–bit only
VMEbus Access:	
A32:	D32, D32 Word, D32 Byte, D32 Block, D64 Block
A24:	D32, D32 Word, D32 Byte
A16:	Not accessible

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1.7 Model 4290/4291 Specifications (continued)

Memory: (continued)

Dual Port SRAM (DPSRAM):	
Blocks:	4 (one per processor) – each block divided into four banks, mastership of any bank obtained via semaphore
Size:	
Option 244:	256 kBytes (64k x 32) each block, 1 MByte total
Option 240:	128 kBytes (32k x 32) each block, 512 kBytes total
Arbitration:	
via V–bus:	None, but need to obtain semaphore
via Global bus:	Rotating Priority
'C6x Access Mode:	32–bit only
'C6201 Access (4290):	
via V–bus:	16 clock access, 50 MB/sec @ 32 bits
via Global Bus:	40 clock access, 20 MB/sec @ 32 bits, after arbitration
'C6701 Access (4291):	
via V–bus:	16 clock access, 41 MB/sec @ 32 bits
via Global Bus:	40 clock access, 16 MB/sec @ 32 bits, after arbitration
VME Access:	
A32:	D32, D32 Word, D32 Byte, D32 Block, D64 Block
A24:	D32, D32 Word, D32 Byte
A16:	Not accessible
NVSRAM:	
Size:	8 kBytes, 8k x 8
Arbitration:	Rotating Priority
'C6x Access Modes:	32–bit access only, but only the 8 LSBs contain valid data.
'C6201 Access:	45 clock access, 4.4 MB/sec @ 8 bits, after arbitration
'C6701 Access:	45 clock access, 3.7 MB/sec @ 8 bits, after arbitration
VMEbus Access:	**(Only the 8 least significant bits are valid!)**
A32:	D32
A24:	D32
A16:	Not accessible
Global Flash EEPROM:	
Size:	8 MBytes (2M x 32)
Arbitration:	Rotating Priority
'C6x Access Mode:	32–bit only
'C6201 Access:	43 clock access, 18 MB/sec @ 32 bits, after arbitration
'C6701 Access:	43 clock access, 15 MB/sec @ 32 bits, after arbitration
VMEbus Access:	
A32:	D32
A24:	D32
A16:	Not accessible

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1.7 Model 4290/4291 Specifications (continued)

Memory: (continued)

VIM Expansion Bi–directional FIFOs:
- Quantity: 4 (one per processor)
- Size:
  - Standard & Option 330: 8 kBytes (2 x 1k x 32)
  - Options 320 & 321: 128 kBytes (2 x 16k x 32)
- Arbitration: None (each BIFO accessible only to one 'C6x processor)
- 'C6x Access Mode: 32–bit only
- Standard & Options 320 & 321:
  - 'C6201 Write Access: 8 clock access, 100 MB/s @ 32 bits
  - 'C6201 Read Access: 9 clock access, 88.89 MB/s @ 32 bits
  - 'C6701 Write Access: 8 clock access, 83.33 MB/s @ 32 bits
  - 'C6701 Read Access: 9 clock access, 74.11 MB/s @ 32 bits
- Option 330:
  - 'C6201 R/W Access: 2 clock access, 400 MB/s @ 32 bits
  - 'C6701 R/W Access: 2 clock access, 334 MB/s @ 32 bits
- VMEbus Access: None

Inter–Processor Bi–directional FIFOs:
- Quantity:
  - Option 244: 4 (one per processor)
  - Option 240: None
- Size:
  - Standard & Options 321 & 330: 8 kBytes (2 x 1k x 32)
  - Options 320: 128 kBytes (2 x 16k x 32)
- Arbitration: None (each BIFO port is accessible only to one 'C6x)
- 'C6x Access Mode: 32–bit only
- Standard Units & Options 320 & 321:
  - 'C6201 Write Access: 8 clock access, 100 MB/s @ 32 bits
  - 'C6201 Read Access: 9 clock access, 88.89 MB/s @ 32 bits
  - 'C6701 Write Access: 8 clock access, 83.33 MB/s @ 32 bits
  - 'C6701 Read Access: 9 clock access, 74.11 MB/s @ 32 bits
- Option 330:
  - 'C6201 R/W Access: 2 clock access, 400 MB/s @ 32 bits
  - 'C6701 R/W Access: 2 clock access, 334 MB/s @ 32 bits
- VMEbus Access: None

'C6x Internal Program Memory:
- Quantity: 4 (one per processor)
- Size: 256 kBytes (64k x 32)
- Arbitration: None (each block accessible only to one 'C6x processor)
- 'C6x Access Mode: 32–bit only
- 'C6201 Access (4290): 1 clock access, 800 MB/sec @ 32 bits
- 'C6701 Access (4291): 1 clock access, 667 MB/sec @ 32 bits
- VMEbus Access: None

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1.7 Model 4290/4291 Specifications (continued)

Memory: (continued)

'C6x Internal Data Memory:

Quantity:	4 (one per processor)
Size:	256 kBytes (64k x 32)
Arbitration:	None (each block accessible only to one 'C6x processor)
'C6x Access Modes:	8–bit, 16–bit and 32–bit
'C6201 Access (4290):	1 clock access, 800 MB/sec @ 32 bits
'C6701 Access (4291):	1 clock access, 667 MB/sec @ 32 bits
VMEbus Access:	None

VMEbus Interface:

Type:	Master/Slave, Interrupt Handler, Interrupter, System Controller capable
Address:	16, 24 or 32 bit
Data:	8, 16, 32 or 64 bit
Arbitration:	Yes – Handled by system controller
'C6x Access:	Yes – Access time determined by arbitration latencies on the Global bus and the VMEbus and on the response time of the requested slave.

Master Access Modes:

A32:	D32, D16, D8, D32 Block, D64 Block
A24:	D32, D16, D16 Byte
A16:	D16, D16 Byte

Slave Access Modes:

A32:	D32, D32 Word, D32 Byte, D32 Block, D64 Block
A24:	D32, D32 Word, D32 Byte
A16:	D16, D16 Byte

Global Slave Expansion Bus :

Size:	16 MByte address space
Arbitration:	Rotating Priority
'C6x Access:	32, 16 or 8 bit, TBD clock access after Global bus arbitration

VMEbus Access:

A32:	D32, D32 Word, D32 Byte, D32 Block, D64 Block
A24:	D32, D32 Word, D32 Byte
A16:	Not accessible

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1.7 Model 4290/4291 Specifications (continued)

Physical:

Dimensions:	Standard 6U VMEbus board
Depth:	160.0 mm (6.3 in)
Height:	233.5 mm (9.2 in)
Panel Width:	20.3 mm (0.8 in)
Shipping Weight:	890 grams (1.96 lbs)
Temperature:	
Operating:	0 °C to 50 °C @ 20% to 70% Relative Humidity (non−condensing)
Storage:	−20 °C to +90 °C @ 10% to 90% Relative Humidity (non−condensing)

Power: All quantities are typical, executing code after boot.

Supply	4290 @ 200 MHz	4291 @ 167 MHz
+ 5.0 V_{DC}	5.0 A	5.0 A
+12.0 V_{DC}	0 mA	0 mA
−12.0 V_{DC}	0 mA	0 mA

(The 12 V supplies are not used on this board, but are delivered to the VIM modules)

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Chapter 2: Installation and Connections

2.1 Introduction

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If any damage is discovered, please contact Pentek immediately, at (201) 818−5900. Please save the original shipping container and packing material, in case return shipment is required.

2.2 Jumper Block Locations and Jumper Settings

The term **jumper block** refers to a group of two or more pins on a circuit board that may be connected in pairs by means of a shorting jumper. A pair of pins connected in this manner are referred to as **shorted**. A pair of pins that are not connected are called **open**. This is a widely used method for selecting certain operating parameters on many types of electronic equipment. The shorting jumpers used on the Model 4290/4291 are for 0.020" (0.51 mm) square pins spaced on 0.079" (2.00 mm) centers, e. g., DuPont Electronics part # 86730−001, or equivalent. Pentek's part number for these jumpers is 356.00010.

Several of these jumpers are installed in default locations on your device . The operating parameters they select (e. g., the VMEbus address of the device) may or may not meet your requirements. Before installing your Model 4290/4291 into the VMEbus card cage, please review the subsections that follow to determine whether or not you will need to change any of these settings.

Figure 2−1, on the next page shows the jumper block locations. **Jumper blocks that are not circled in the figure or mentioned in the subsections that follow should not be changed. These jumpers are used for factory testing and setup purposes only.**

2.2.1 A16/A32 VMEbus Slave Base Address − Jumper Blocks AJ8 : AJ1

Between the VMEbus P1 connector and IC U30 are a group of jumper blocks labeled AJ8 through AJ1. These jumper blocks are used to set the slave base address (i. e., the lowest address that this device will respond to when addressed as a slave) for the Model 4290/4291 in both A16 and A32 VMEbus address spaces. As shown in Table 2−1, on the page after next, for both address spaces, AJ8 corresponds to the most significant address bit (i. e., A31 in A32 space and A15 in A16 space). Each lower numbered jumper block corresponds to the next less significant address bit, such that AJ1 corresponds to A24 in A32 space and to A8 in A16 space. Shorting a jumper block clears the corresponding address bit to '0' , and an open jumper block sets the corresponding address bit to '1'. In addition to showing which VMEbus address bit corresponds to each jumper block, Table 2−1 also gives the weight of each jumper position, in both address spaces.

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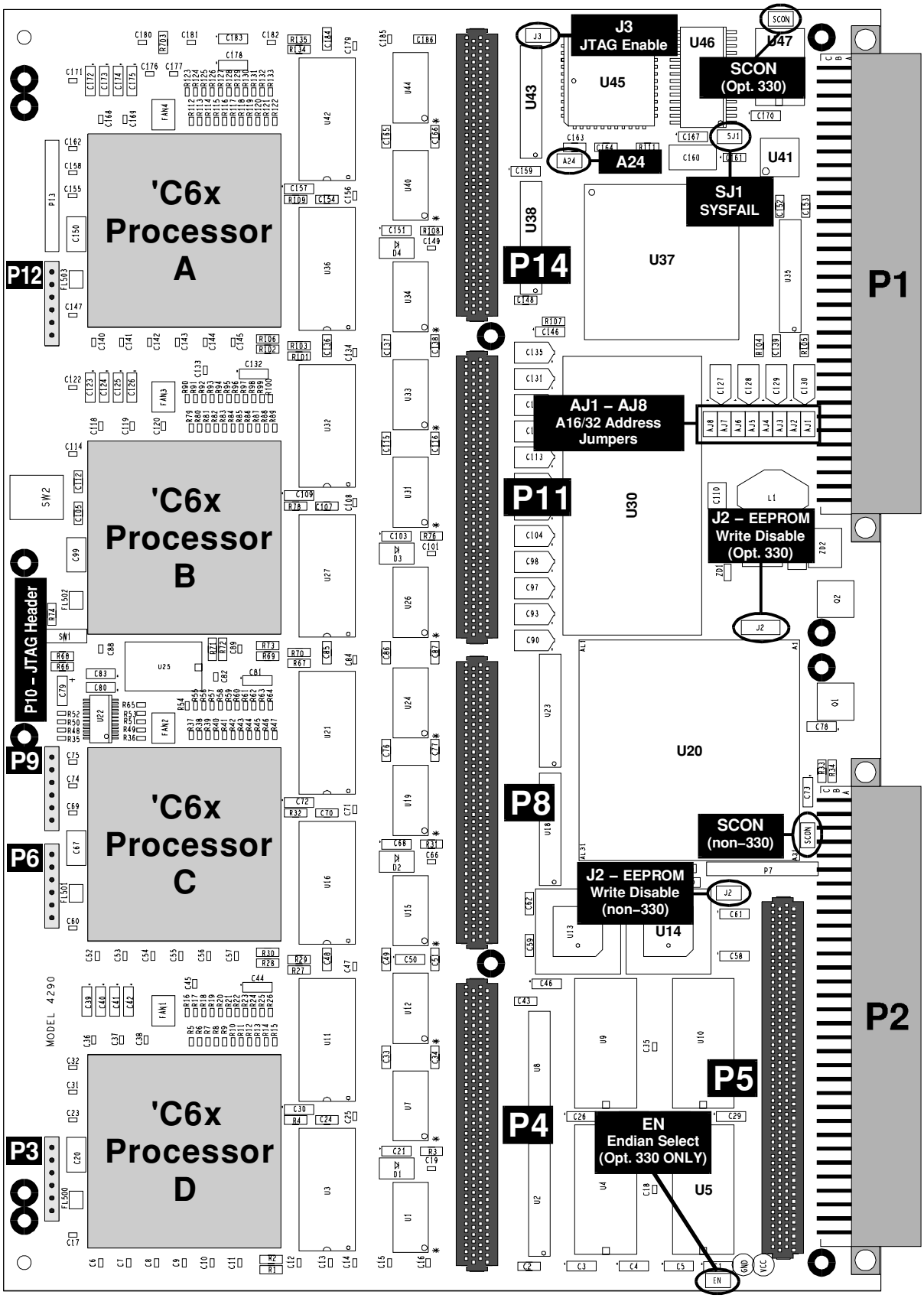


Figure 2–1: Model 4290/4291 –PC Board, Component Side, Connectors and Jumpers

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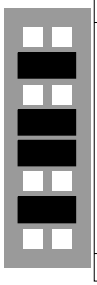
2.2 Jumper Block Locations and Jumper Settings (continued)

2.2.1 A16/A32 VMEbus Slave Base Address (continued)

Table 2–1: Model 4290/4291 –VMEbus A16/A32 Slave Base Address –Jumper Blocks AJ8 : AJ1

Jumper Pins	VME Address Bit		A16 Decimal Weight	A16 Hex Weight	A32 Decimal Weight	A32 Hex Weight
	A16	A32				
AJ8	A15	A31	32,768	0x8000	2,147,483,648	0x8000 0000
AJ7	A14	A30	16,384	0x4000	1,073,741,824	0x4000 0000
AJ6	A13	A29	8,192	0x2000	536,870,912	0x2000 0000
AJ5	A12	A28	4,096	0x1000	268,435,456	0x1000 0000
AJ4	A11	A27	2,048	0x800	134,217,728	0x0800 0000
AJ3	A10	A26	1,024	0x400	67,108,864	0x0400 0000
AJ2	A9	A25	512	0x200	33,554,432	0x0200 0000
AJ1	A8	A24	256	0x100	16,777,216	0x0100 0000
Factory default setting –all jumpers shorted (A16_base = 0x0000, A32_base = 0x0000 0000)						

The selected base address is the sum of the weights of all address bits whose coresponding jumpers are open. For example, suppose you want to set the A16 base address of your Model 4290/4291 to 0xA500. To acheive this setting, you need to set address bits A15, A13, A10 and A8, and clear address bits A14, A12, A11 and A9. Since an open address jumper sets the corresponding address bit to a '1', and a shorted address jumper clears the corresponding address bit to a '0', the proper jumper settings for this base address would be AJ7, AJ5, AJ4 and AJ2 shorted, AJ8, AJ6, AJ3 and AJ1 open. This configuration is illustrated in Figure 2–2, below. Because the A32 base address is also set by these jumpers, the resulting base address in VMEbus A32 space for this setting would be 0xA500 0000.



Jumper	A16 Addr. Bit	A16 Weight	A32 Addr. Bit	A32 Weight
AJ8 = 1	A15	0x8000	A31	0x8000 0000
AJ7 = 0	A14	0x0000	A30	0x0000 0000
AJ6 = 1	A13	0x2000	A29	0x2000 0000
AJ5 = 0	A12	0x0000	A28	0x0000 0000
AJ4 = 0	A11	0x0000	A27	0x0000 0000
AJ3 = 1	A10	0x0400	A26	0x0400 0000
AJ2 = 0	A9	0x0000	A25	0x0000 0000
AJ1 = 1	A8	0x0100	A24	0x0100 0000
Addresses:	A16 =	0xA500	A32 =	0xA500 0000

Figure 2–2: Address Jumper Setting Example

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2.2 Jumper Block Locations and Jumper Settings (continued)

2.2.2 VMEbus A24 Slave Access Enable – Jumper Block A24

A jumper block to enable slave access to the Model 4290/4291 in VMEbus A24 space is located in the area between ICs U37, U38, U43 and U45. The device is shipped with this jumper block shorted, which enables slave access in VME–bus A24 space.

Be aware that the Model 4290/91 occupies the entire 16 MByte A24 memory space when it is made accessible in this region. If your application requires access to any other devices in A24 VMEbus space, you should disable A24 access to the Model 4290/91 by removing the A24 jumper. Table 2–2, below, summarizes the settings of the A24 jumper block.

Table 2-2: Model 4290/4291 –VMEbus A24 Access Enable –Jumper Block A24

A24 Jumper Block	A24 VMEbus Access to . . .	
	Model 4290/4291	Other Devices
***Shorted**	Enabled	Disabled
Open	Disabled	Enabled
*** –Factory default setting**		



Since the Model 4290/91 occupies all of A24 space, when A24 access is enabled its A24_base address will be 0x00 0000, and there is no method (or need) for changing it.

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2.2 Jumper Block Locations and Jumper Settings (continued)

2.2.3 JTAG Emulator Enable – Jumper Block J3

One of the methods that can be used to download programs to the 'C6x processors on the Model 4290/4291, and to control the execution of those programs during software development and debugging, is by using Texas Instruments' XDS–510 in–circuit emulator and the JTAG emulation protocols. Jumper block J3 must be shorted to enable the use of an XDS–510 emulator (this is the factory default setting). Jumper block J3 is located near the top edge of the circuit board, slightly to the rear of center, at the back edge of IC U43.

A more elegant (and generally easier) method of downloading and debugging software programs on the Model 4290/4291 is via the use of TI's Code Composer development software and Pentek's SwiftNet Communication Protocols. In order to use this development system, jumper block J3 must be open. Table 2–3, below, summarizes the settings of jumper block J3.

Table 2-3: Model 4290/4291 –JTAG Enable –Jumper Block J3

J3 Jumper Block	JTAG Emulator	SwiftNet Debug
***Shorted**	Enabled	Disabled
Open	Disabled	Enabled
*** –Factory default setting**		



Additional Information for SwiftNet Users:
When code that uses global memory is running on one of the processors of a 4290/4291, and a Host process is running that also uses global memory, a pnload to a different processor will crash the host process. This occurs because the pnload invokes a board reset, which, in turn, causes a VMEbus error. This behavior can be avoided by removing the jumper from J3.

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2.2 Jumper Block Locations and Jumper Settings (continued)

2.2.4 Global Flash EEPROM Write Protection – Jumper Block J2

On most configurations of the Models 4290 and 4291, jumper block J2 is a 2–pin header, located near the top of the P5 Global Bus connector, below IC U20 and behind IC U14. On units equipped with Option 330, it is a 3–pin header, located above U20, and behind U30. The function of this jumper block is identical without regard to how many pins it contains. It determines whether or not write operations to the protected sector of the Global Flash EEPROM are permitted. The Global Flash EEPROM is divided into 64 sectors. Pentek stores the boot code for the Model 4290/4291 in Sector 0 of the EEPROM, and protects this sector by leaving the 2–pin jumper block J2 open (or by placing a jumper between pins 1 & 2 of the 3–pin jumper block J2 on Option 330 boards). The factory–installed boot code **MUST** reside in this sector of the Flash EEPROM in order for the board to power up properly. Once properly powered up, you may write custom boot code to any of the remaining 63 sec–tors in the Flash EEPROM (sectors 1–63). These remaining 62 sectors are not write protected and the position of J2 has no effect upon them.



Accesses to Flash EEPROM sectors above sector 16 require the user to increment the Page Register, at 'C6x address 0x0028 0024. However, the sample code provided in the Model 4290/4291 Ready-Flow BSP for the purpose of writing to Flash EEPROM does not allow for changing the Page Register value. Thus, if you wish to write to any Flash EEPROM sector above sector 16, you will first need to modify the value in the Page Register on your own.

Jumper block J2 exists solely for the purpose of reprogramming and/or upgrading the FACTORY INSTALLED boot code. The only time a shorting jumper should be installed on the 2–pin J2 (or between pins 2 & 3 of the 3–pin J2 on an Option 330 board) is when updating the FACTORY firmware!

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2.2 Jumper Block Locations and Jumper Settings (continued)

2.2.4 Global Flash EEPROM Write Protection (continued)

Table 2–4, below, summarizes the settings of jumper block J2. Note that the state of this jumper is read at power–up, which means that it must be placed in the desired position **BEFORE** applying power to the Model 4290/4291. Unless you are planning to update the factory firmware, **THIS JUMPER BLOCK MUST BE CONFIGURED IN THE "WRITE PROTECTED" POSI–TION** (see Table 2–4, below) **PRIOR TO POWERING UP THE MODEL 4290/4291. IF THE J2 JUMPER BLOCK IS NOT CONFIGURED IN THE "WRITE PROTECTED" POSITION, THE FIRMWARE CAN BECOME CORRUPT, REQUIRING THAT THE UNIT TO BE RETURNED TO PENTEK.**

Table 2-4: Model 4290/4291 –Flash EEPROM Write Protect –Jumper Block J2

J2 Jumper Block		Flash EEPROM Sector 0	Comment
2-pin (Std.)	3-pin (Opt. 330)		
Shorted	**2 –3**	Write Enabled	**Factory** Boot Code Updates **ONLY**
***Open**	***1 –2**	Write Protected	Normal Position
*** –Factory default setting**			

⚠ WARNING: **DO NOT PLACE A SHORTING JUMPER ON J2 (or between pins 2 & 3 of the 3-pin J2 on Option 330 boards) when writing USER CODE to the EEPROM. This action may result in an accidental overwrite of the factory boot code. The Model 4290/4291 WILL NOT BOOT WITHOUT THE FACTORY BOOT CODE in Sector 0 of the EEPROM, and the unit will then need to be reprogrammed with the correct boot code.**

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2.2 Jumper Block Locations and Jumper Settings (continued)

2.2.5 System Controller Enable – Jumper Block SCON

The Model 4290/4291 can be configured to fulfill the functions of the VME–bus Slot 1 system controller/arbiter by shorting the SCON jumper block. If you would prefer another device to be the Slot 1 controller in your card cage, leave jumper block J2 open (this is the default setting). Remember that one and only one device may be the system controller/arbiter in any given VMEbus card cage. Note that this jumper is located in different places on Option 330 boards and other 4290/4291 boards. On most boards, it is located near the top of the VMEbus P2 connector, just behind the right rear corner of IC U20. On Option 330 boards, it is located at the top rear of the board, above IC U47. Table 2–5, below, summarizes the settings of the SCON jumper block.

Table 2-5: Model 4290/4291 –System Controller Enable –Jumper Block SCON

SCON Jumper Block	System Control Functions	System Controller
Shorted	Enabled	4290/4291
***Open**	Disabled	Other Device
*** –Factory default setting**		

2.2.6 SYSFAIL Inhibit – Jumper Block SJ1

The device used as the VMEbus interface controller on the Model 4290/4291 is Cypress Semiconductor's VIC64. While this chip handles almost all of the bus interface functions quite well, we have noted a bit of a peculiarity with respect to how it handles the System Failure, or SYSFAIL, signal. The VIC appears to assert this signal in response to any reset. This behavior can cause problems for other devices on the VMEbus. To prevent these difficulties from arising, we have placed a jumper block, SJ1, as a series component in the SYSFAIL signal line. SJ1 is located near the top of the VMEbus P1 connector, between ICs U41 and U46. If this jumper block is left open (this is the default setting), the VIC 64's SYSFAIL signal is prevented from being asserted on the VMEbus. If none of the other devices in your VME card cage respond to the SYSFAIL signal, you may short jumper block SJ1.

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2.2 Jumper Block Locations and Jumper Settings (continued)

2.2.7 Endian Select – Jumper Block EN (Option 330 ONLY!)

At the bottom of the 4290/4291 Option 330 board, below the IC designated U5, is an additional jumper block labeled EN. This jumper block selects the endian, or byte ordering, mode for the 'C6x processors, allowing the 4290/91 to easily interface with different host processors. By the factory default setting, this jumper block is shorted, selecting big endian mode. In big endian mode, the most significant byte of a given word is located in the lowest byte address occupied by the word. Big endian mode is generally used by Motorola–type host processors. Conversely, Intel–type host processors usually use little endian mode, in which the most significant byte of a given word is located in the highest byte address occupied by the word. To configure the 'C6x processors on your Model 4290/4291 Option 330 for little endian mode, jumper block EN must be open.

Note that the **ENDIAN MODE IS NOT SELECTABLE ON 4290/4291 UNITS THAT ARE NOT EQUIPPED WITH OPTION 330**. The processors on these units are configured for big endian operation, and this configuration cannot be changed.

2.2.8 Other Jumper Blocks



Any jumper block that was NOT discussed in Sections 2.2.1 through 2.2.7, or is NOT circled in Figure 2–1, is a reserved jumper that is used for factory testing and configuration purposes. These jumpers are configured for the proper operation of your configuration of the Model 4290/4291 at the factory, and THEY SHOULD NOT BE TAMPERED WITH BY ANYONE OTHER THAN FACTORY–TRAINED, PENTEK PERSONNEL!

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2.3 Model 4290/4291 Front Panel

As delivered, the front panel of the Model 4290/4291 consists of 5 segments. The top and bottom sections of the panel are fixed plates that house the captive screws and ejector handles, used to anchor the circuit board into, and remove the board from, the VMEbus card cage. A third fixed plate, at the center of the unit, houses a single XDS connector, a power indicator LED, and a recessed pushbutton to reset the board. The two remaining spaces at the front of the unit are occupied by a pair of "blank" VIM module panels (blank in the sense that that contain no con–nectors – they DO have text silkscreened on them). Each blank panel has a pair of cutouts on its left edge that expose four LEDs mounted on the 4290/4291's circuit board. Alongside each of these cutouts are the identifiers **0**, **1**, **2** & **3**, each associated with the LED to its immediate left. Before installing a Velocity Interface Mezzanine (VIM) module, to provide a front panel I/O source for the 'C6x processors, you must remove one or both blank panels, whose position(s) will be occupied by the module's panel(s). Fig–ure 2–3, at the right, shows the Model 4290/4291 with two blank panels installed. Instructions for installing the VIM module and replacing the 4290/4291's blank panels are included in the Oper–ating Manual(s) supplied with your VIM module(s).

2.3.1 XDS Connector – P10

At the center of the Model 4290/4291's front panel is the XDS–510 Emulator connector, designated P10 on the PC board. The pinout for this standard, 14–Pin JTAG interface is given in Table 2–6, below.

Table 2-6: Model 4290/4291 –XDS Connector (P10)

Pin #	Description	Pin #	Description
1	TMS	2	$\overline{\text{TRST}}$
3	TDI	4	GND
5	+3.3 V_{DC}	6	(KEY –no pin)
7	TDO	8	GND
9	TCKO	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

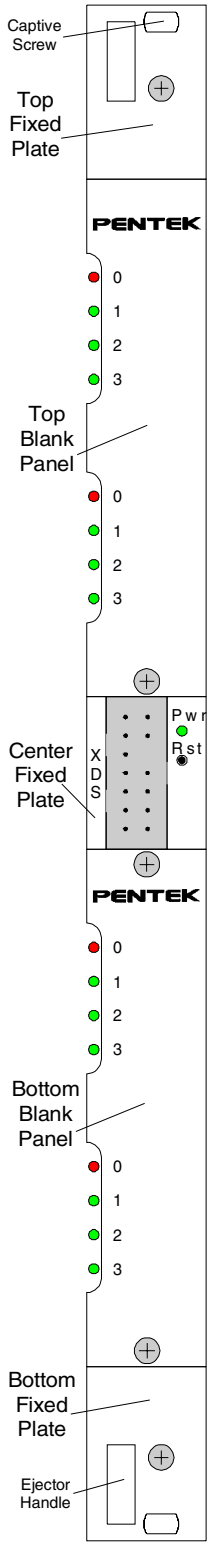


Figure 2-3: Model 4290/4291 Front Panel

Note

Prior to executing code using an XDS emulator, Timer 0 must be disabled. If Timer 0 is not disabled, when code is loaded by the emulator, the interrupt vector table or interrupt handler may get overwritten. To disable Timer 0, immediately after entering the main routine in your code, use:

*** (unsigned int *) 0x01940000 = 0;**

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2.3 Model 4290/4291 Front Panel (continued)

2.3.2 Power LED – Pwr

To the right of the XDS connector, near the top of the center fixed plate is a green LED, labeled **Pwr**, that will be illuminated whenever + 5 V_{DC} power is applied to the Model 4290/4291.

2.3.3 Reset Button – Rst

Below the power LED, to the right of the XDS connector on the fixed center plate of the Model 4290/4291's front panel, is a recessed pushbutton labeled **Rst**, which, when pressed, will return the device to its power–up, reset state. This button's height is approximately even with the panel in its normally open position, so you will need a probe (or fine–point pen, or opened paper clip (this author's personal favorite tool for this application), or something else that will fit through a 0.063" diameter hole) to press this button.

2.3.4 Processor LEDs – 0, 1, 2 & 3

On the Model 4290/4291, a series of four LEDs, one red and three green, are associated with each processor. The individual LEDs in each group are labeled **0**, **1**, **2**, and **3**, and they can be toggled on and off using bits D0 through D3 in each processor's Miscellaneous Control Register 0 (MCR0). The red LED (labeled **0**) is controlled by bit D0, and the three green LEDs (labeled **1**, **2**, & **3**) are controlled using the correspondingly numbered bits (i. e., D1 through D3, respectively).

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2.3 Model 4290/4291 Front Panel (continued)

2.3.5 'C6x Timer Signal I/O – P3, P6, P9 & P12

Located just behind the Model 4290/91's Front Panel, each 'C6x processor has an I/O socket strip, for its four timer signals, T0 In, T0 Out, T1 In and T1 Out (Option 330 units have different connectors here, and only for the T1 signals – see below). The sockets in these single in–line strips can mate with round, machined pins that are 0.018" (0.46 mm) in diameter, and are spaced on 0.100" (2.54 mm) centers. A header that will mate with this strip is the Model # BBS–106–G–E, from Samtec, or an equivalent. This header is a single–inline strip of discrete pins on 0.100" centers, that you can solder wires onto, as opposed to the insulation–displacement, crimp–on style of connector. Figure 2–4(a), at the left, shows the signals present at each header pin. Table 2–7, below, lists the processor associated with each header. Figure 2–1 on page 32 shows the location of each header.

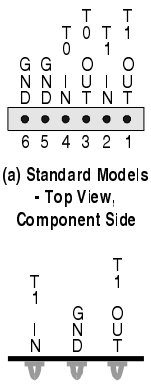


Figure 2-4: Pinout of Timer I/O Headers (P3, P6, P9 &

Table 2–7: Model 4290/4291 –Timer I/O Headers

Processor	Associated Header
A	P12
B	P9
C	P6
D	P3

The Model 4290/4291 Option 330 has a different connector arrangement in these four locations. Instead of the 6–pin socket strips accessible from the component side of the board, the Option 330 boards have three D–shaped posts on the solder side of the board, designed to accept probe hooks of the type that are supplied with most logic analyzers and oscilloscope probes. Available on these posts, as shown in Figure 2–4(b), above left, are (from left to right) T1 In, ground, and T1 Out. The Timer 0 signals are not available to the user on Option 330 boards. Note that if the two Timer1 signals are shorted together while an Option 330 unit is booted, any code resident in that processor's User Flash EEPROM will be erased (see Section 8.7).

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2.4 VIM Connectors

The connectors on the Model 4290/4291 designated P4, P8, P11 and P14 are the Velocity Interface Mezzanine (VIM) Connectors. P14 & P11 comprise the upper module site, and P8 & P4 are the lower module site. The Model 4290/4291 can support up to two VIM−2 modules (one in each site), or one VIM−4 module (which occupies both sites). An additional connector, P5, located at the bottom rear of the assembly (just in front of the VMEbus P2 connector) provides support for VIM−R Modules, which use the P2 bus. The 4290/4291's exclusive Global Slave Expansion Bus, which will be covered in more detail in Section 2.5, is also implemented on connector P5.

The following sections define the pin assignments for the VIM Processor Node Connectors on the Model 4290/4291 VIM motherboard. Each Processor Node Connector contains four rows of pins numbered 1 through 40 (the row nearest the VMEbus connectors), 41 through 80 (the second row from the VME connectors), 81 through 120 (the second row from the front panel) and 121 through 160 (the row nearest the front panel). Figure 2−5, below, shows the pinout looking into the connectors, from the component side of the Model 4290/4291. Table 2−8, next page, shows the pin assignments of the connectors.

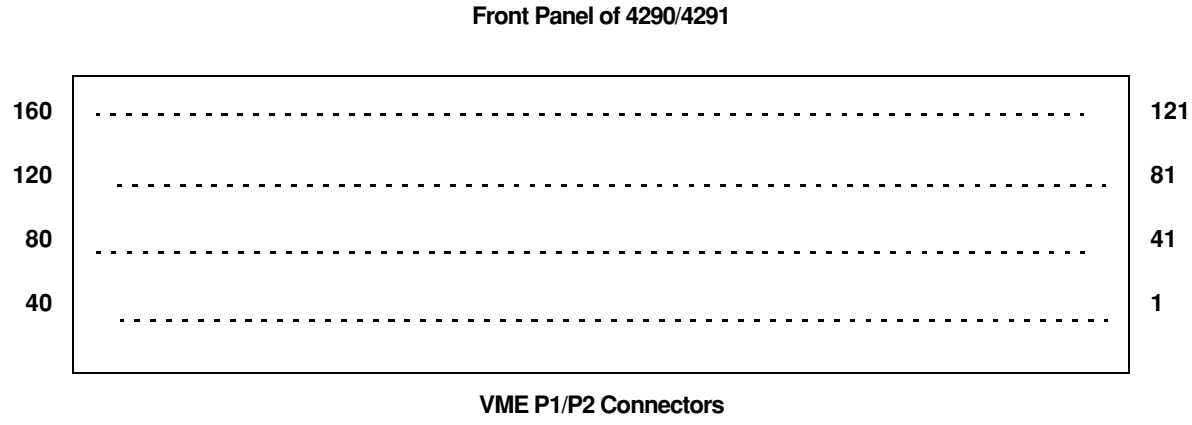


Figure 2-5: Model 4290/4291 −VIM Connector Pin Numbering (Top View)

Connector Definition: Samtec Full Line Catalog, F−197−1, Sept. '97, Pages 38−39

4290/4291 Connector: Samtec SOLC−140−02−S−Q−A: 160 pin, surface mount, gold contact, locking clip

VIM Module Connector: Samtec TOLC−140−32−S−Q−A: 160 pin, surface mount, gold post, locking clip, for 0.472 in mated height

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2.4 VIM Connectors (continued)

Table 2-8: Model 4290/4291 –VIM Connector Pinout

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	NxFClk	41	Vcc	81	NxF$\overline{W}$/R	121	+12 V
2	Vcc	42	$\overline{\text{NxFCSB}}$	82	Vcc	122	$\overline{\text{NxDBINT}}$
3	$\overline{\text{NxMBIN}}$	43	Vcc	83	NxMBSEL	123	–12 V
4	Vcc	44	$\overline{\text{NxMBOUT}}$	84	Vcc	124	$\overline{\text{NxFRST}}$
5	$\overline{\text{NxIFAFL}}$	45	Vcc	85	$\overline{\text{NxOFAFL}}$	125	Vcc
6	$\overline{\text{NxIFAEM}}$	46	$\overline{\text{NxIFEMP}}$	86	$\overline{\text{NxOFAEM}}$	126	$\overline{\text{NxOFEMP}}$
7	Gnd	47	Gnd	87	Gnd	127	Gnd
8	NxFD0	48	NxFD1	88	NxFD2	128	NxFD3
9	NxFD4	49	NxFD5	89	NxFD6	129	NxFD7
10	NxFD8	50	NxFD9	90	NxFD10	130	NxFD11
11	NxFD12	51	NxFD13	91	NxFD14	131	NxFD15
12	Vcc	52	Vcc	92	Vcc	132	Vcc
13	NxFD16	53	NxFD17	93	NxFD18	133	NxFD19
14	NxFD20	54	NxFD21	94	NxFD22	134	NxFD23
15	NxFD24	55	NxFD25	95	NxFD26	135	NxFD27
16	NxFD28	56	NxFD29	96	NxFD30	136	NxFD31
17	Gnd	57	Gnd	97	Gnd	137	Gnd
18	NxAddr2	58	NxAddr3	98	NxAddr4	138	NxAddr5
19	NxAddr6	59	NxAddr7	99	NxAddr8	139	NxAddr9
20	NxAddr10	60	NxAddr11	100	NxAddr12	140	NxAddr13
21	NxAddr14	61	NxAddr15	101	NxAddr16	141	NxAddr17
22	Vcc	62	Vcc	102	Vcc	142	Vcc
23	NxData0	63	NxData1	103	NxData2	143	NxData3
24	NxData4	64	NxData5	104	NxData6	144	NxData7
25	NxData8	65	NxData9	105	NxData10	145	NxData11
26	NxData12	66	NxData13	106	NxData14	146	NxData15
27	Gnd	67	Gnd	107	Gnd	147	Gnd
28	NxData16	68	NxData17	108	NxData18	148	NxData19
29	NxData20	69	NxData21	109	NxData22	149	NxData23
30	NxData24	70	NxData25	110	NxData26	150	NxData27
31	NxData28	71	NxData29	111	NxData30	151	NxData31
32	Vcc	72	Vcc	112	Vcc	152	Vcc
33	NxDR0	73	NxFSR0	113	NxFSR1	153	NxDR1
34	NxDX0	74	NxFSX0	114	NxFSX1	154	NxDX1
35	NxClkS0	75	Gnd	115	NxClkS1	155	Gnd
36	Gnd	76	NxClkX0	116	Gnd	156	NxClkX1
37	NxClkR0	77	Gnd	117	NxClkR1	157	Gnd
38	Gnd	78	$\overline{\text{NxARE}}$	118	Gnd	158	$\overline{\text{NxDBRST}}$
39	$\overline{\text{NxAOE}}$	79	Gnd	119	$\overline{\text{NxAWE}}$	159	Gnd
40	$\overline{\text{NxDBPSNT}}$	80	$\overline{\text{NxARDY}}$	120	Gnd	160	NxDBClk

NOTE: Nx indicates the Processor or Node with which the interface is associated.

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2.4 VIM Connectors (continued)

The surface–mount connectors used for the VIM interface on the Model 4290/ 4291(P4, P8, P11 and P14) contain 160 gold–plated female pins arranged in four staggered rows on a .050" grid, with .025" lead pitch, and is Samtec's SOLC–140–02–S–Q–A or equivalent. The Global Bus/P2 interface connector (P5) contains 200 gold–plated female pins arranged in four staggered rows on a .050" grid, with .025" lead pitch, and is Samtec's SOLC–150–02–S–Q–LC or equivalent.
Figure 2–6, below, shows mechanical drawings of the connectors used for these interfaces.

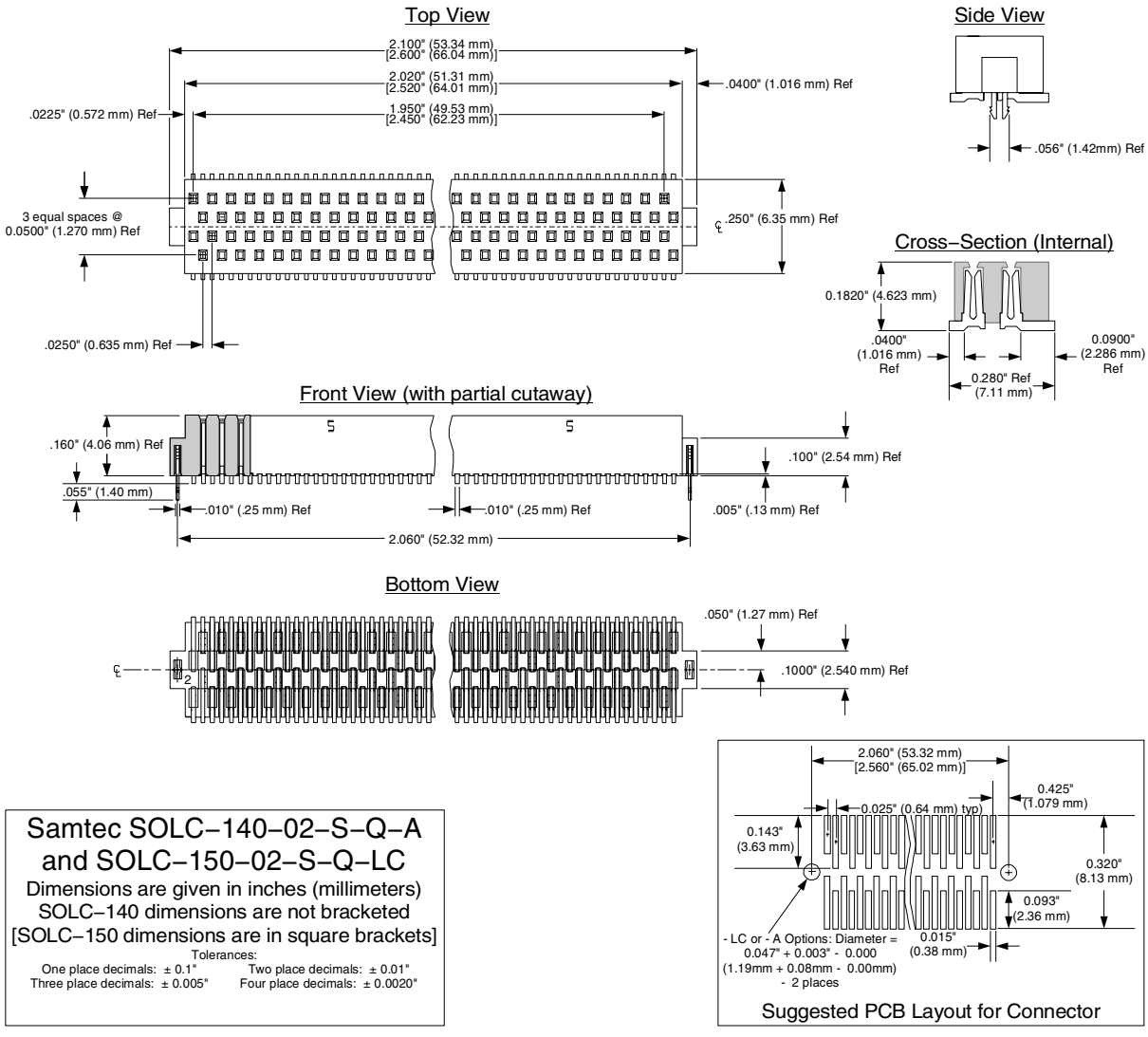


Figure 2-6: VIM Connectors Used On VIM Motherboards –Mechanical Drawings

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2.4 VIM Connectors (continued)

2.4.1 VIM Processor Node Interface Signal Definition

The VIM Processor Node Interface connector contains the signals required to support three types of I/O by the processor(s) on the Model 4290/4291 VIM motherboard. These interfaces are the Synchronous Bi−Directional FIFO based streaming data interface, the random access interface, and the serial port interface. This interface connector is replicated four times across the board. The only change between the connectors is that the second char−acter in each signal's name is logically incremented to indicate the processor (i. e., node) or VIM connector that it is connected to.

All input and output signals are at LVTTL levels, and are 5V tolerant. LVTTL logic levels are defined as follows: $V\ Out_{low(max)} = +0.4\ V_{DC}$; $V\ In_{low(max)} = +0.8\ V_{DC}$; $V\ In_{hi(min)} = +2.0\ V_{DC}$; $V\ Out_{hi(min)} = +2.4\ V_{DC}$. The only ramification of this on designers of VIM interface circuitry is that while essentially any logic device that uses a single, $+5\ V_{DC}$ supply can be used to drive a logic input on the VIM connector, logic outputs from the VIM con−nector cannot be received by standard CMOS logic devices (e. g., the CD4000 series), as the LVTTL high level output is not sufficiently positive to be rec−ognized as high by standard CMOS logic devices.

The signal definition is broken down by the type of interface so you can understand the logical makeup of each of the interfaces. The signal direc−tion is given from the perspective of the Model 4290/4291, i. e., a signal that has its direction listed as O (output) is one that is driven by the Model 4290/4291.

Users who wish to design their own, custom VIM modules should refer to Pentek's VIM Specification (Pentek part number 800.00002), available on our web site (http://www.pentek.com), or directly from the factory (call (201) 818−5900, in the U. S.A.) for detailed signal definitions, timing diagrams, mechanical information, etc.

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2.4 VIM Connectors (continued)

2.4.1 VIM Processor Node Interface Signal Definition (continued)

2.4.1.1 Bi–FIFO Streaming Data Interface

Table 2–9, below, lists the signals that comprise the Synchronous Bi–Directional FIFO–based data streaming interface portion of the Model 4290/4291's VIM Processor Node interface. The table gives signal mnemonics and full names, gives the signal's or group's direction (with respect to the Model 4290/4291 VIM motherboard) and tells which pins on the connector are used for each signal or signal group. For detailed descriptions of each signal or signal group shown in this table, please refer to Pentek's VIM Specification, Pentek part number 800.00002.

Table 2-9: VIM Processor Node Interface –Synchronous Bi-FIFO Data Streaming Interface

Mnemonic	Name / Function	Direction	Pin #(s)
NxFD[31:0]	Node x I/O Bi-FIFO Data Bus	I/O	8-11, 13-16, 48-51, 53-56, 88-91, 93-96, 128-131, 133-136
NxFClk	Node x I/O Bi-FIFO Clock	In	1
$\overline{\text{NxFCSB}}$	Node x Bi-FIFO Port B Chip Select	In	42
NxF$\overline{\text{W}}$/R	Node x I/O Bi-FIFO $\overline{\text{Write}}$ / Read	In	81
$\overline{\text{NxIFAFL}}$	Node x I/O Bi-FIFO Input Almost Full Flag	Out	5
$\overline{\text{NxIFAEM}}$	Node x I/O Bi-FIFO Input Almost Empty Flag	Out	6
$\overline{\text{NxIFEMP}}$	Node x I/O Bi-FIFO Input Empty Flag	Out	46
$\overline{\text{NxOFAFL}}$	Node x I/O Bi-FIFO Output Almost Full Flag	Out	85
$\overline{\text{NxOFAEM}}$	Node x I/O Bi-FIFO Output Almost Empty Flag	Out	86
$\overline{\text{NxOFEMP}}$	Node x I/O Bi-FIFO Output Empty Flag	Out	126
$\overline{\text{NxFRST}}$	Node x I/O Bi-FIFO Reset	Out	124
NxMBSEL	Node x Mailbox Select	In	83
$\overline{\text{NxMBIN}}$	Node x Mailbox Interrupt Input	Out	3
NxMBOUT	Node x Mailbox Interrupt Output	Out	44

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2.4 VIM Connectors (continued)

2.4.1 VIM Processor Node Interface Signal Definition (continued)

2.4.1.2 Random Access Interface

Table 2–10, below, lists the signals that comprise the Random Access Interface portion of the Processor Node interface. The table gives signal mnemonics and full names, gives the signal's or group's direction (with respect to the Model 4290/4291 VIM motherboard) and tells which pins on the connector are used for each signal or signal group. For detailed descriptions of each signal or signal group shown in this table, please refer to Pentek's VIM Specification, Pentek part number 800.00002.

Table 2–10: VIM Processor Node Interface –Random Access Interface

Mnemonic	Name / Function	Direction	Pin #(s)
NxAddr[17:2]	Node x Random Access Address Bus	Out	18-21, 58-61, 98-101, 138-141
NxData[31:0]	Node x Random Access Data Bus	I/O	23-26, 28-31, 63-66, 68-71, 103-106, 108-111, 141-146, 148-151
NxAOE	Node x Random Access Output Enable	Out	39
NxARE	Node x Random Access Read Strobe	Out	78
NxAWE	Node x Random Access Write Enable	Out	119
NxARDY	Node x Random Access Ready Output	In	80
NxDBRST	Daughterboard Expansion Synchronous Reset	Out	158
NxDBClk	Daughterboard Expansion Clock Input	Out	160
NxDBINT	Daughterboard Expansion Interrupt Output	In	122
NxDBPSNT	Expansion Daughterboard Present Output	In	40

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2.4 VIM Connectors (continued)

2.4.1 VIM Processor Node Interface Signal Definition (continued)

2.4.1.3 Serial Port Interface

Table 2–11, below, lists the signals that comprise the Serial Port Interface portion of the Processor Node interface. The table gives signal mnemonics and full names, gives the signal's or group's direction (with respect to the Model 4290/4291 VIM motherboard) and tells which pins on the connector are used for each signal or signal group. 3–Volt LVTTL Buffers are provided for each signal in this group, between the I/O pins on the 'C6x and the VIM connector. For detailed descriptions of each signal or signal group shown in this table, please refer to Pentek's VIM Specification, Pentek part number 800.00002.

Table 2–11: VIM Processor Node Interface –Serial Port Interface

Mnemonic	Name / Function	Direction	Pin #(s)
NxCLKS0	Node x Serial Port 0 External Clock Source	In	35
NxCLKR0	Node x Serial Port 0 Receive Clock	I/O	37
NxCLKX0	Node x Serial Port 0 Transmit Clock	I/O	76
NxDR0	Node x Serial Port 0 Receive Data	In	33
NxDX0	Node x Serial Port 0 Transmit Data	Out	34
NxFSR0	Node x Serial Port 0 Receive Frame Sync	I/O	73
NxFSX0	Node x Serial Port 0 Transmit Frame Sync	I/O	74
NxCLKS1	Node x Serial Port 1 External Clock Source	In	115
NxCLKR1	Node x Serial Port 1 Receive Clock	I/O	117
NxCLKX1	Node x Serial Port 1 Transmit Clock	I/O	156
NxDR1	Node x Serial Port 1 Receive Data	In	153
NxDX1	Node x Serial Port 1 Transmit Data	Out	154
NxFSR1	Node x Serial Port 1 Receive Frame Sync	I/O	113
NxFSX1	Node x Serial Port 1 Transmit Frame Sync	I/O	114

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2.4 VIM Connectors (continued)

2.4.1 VIM Processor Node Interface Signal Definition (continued)

2.4.1.4 Power Supply Connections

Name	Dir	Description
V_{CC}	O	**+ 5 V_{DC} supply –**Provided by Model 4290/4291 VIM mother–board, 1.0 A max. per VIM connector. (Pins 2, 4, 12, 22, 32, 41, 43, 45, 52, 62, 72, 82, 84, 92, 102, 112, 125, 132, 142, 152)
+12 V	I	**+ 12 V_{DC} supply** –Provided by Model 4290/4291 VIM moth–erboard, 400 mA max. per VIM connector (Pin 121)
–12 V	I	**– 12 V_{DC} supply -** Provided by Model 4290/4291 VIM moth–erboard, 400 mA max. per VIM connector (Pin 123)
Gnd	I	**Signal and power ground reference.** Provided by Model 4290/4291 VIM motherboard. (Pins 7, 17, 27, 36, 38, 47, 57, 67, 77, 79, 87, 97, 107, 116, 118, 120, 127, 137, 147, 157, 159)

2.5 The Global Bus Slave Expansion Connector

Table 2–12, below, lists the signals included in the Model 4290/4291's Global Slave Expansion Bus/P2 interface, and gives the number of lines in each signal group and signal direction relative to the VIM module. The surface–mount connectors used for this interface on the VIM motherboard contain 200 gold–plated female pins, and those used on the VIM modules contain 200 gold–plated male pins.

Table 2–12: Global Bus/P2 Interface Signal Summary

Global Bus					
Signal Class	**# of lines**	**Direction**	**Signal Class**	**# of lines**	**Direction**
Data Bits	32	I/O	Address Bits	33	In
Data Strobe	1	In	Address Strobe	1	In
Data Strobe Ack.	1	Out	R/W Enable	2	In
Reset	1	In	Interrupt	1	Out
Module Preset	1	Out	32 MHz Clock	1	In
VMEbus P2 Connector (User–Defined Signals)					
Signal Class	**# of lines**	**Direction**	**Signal Class**	**# of lines**	**Direction**
Row A	32	I/O	Row C	32	I/O
Power					
Supply / # pins	**Supply / # pins**	**Supply / # pins**	**Supply / #pins**	**Supply / # pins**	
+5V_{DC} / 18	+12V_{DC} / 4	+3.3 V_{DC} / 8	Ground / 16	–12V_{DC} / 4	

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2.5 The Global Bus Slave Expansion Connector (continued)

The expansion connector is numbered with four rows of pins numbered 1 through 50 (the row nearest the P2 connector), 51 through 100 (the second row from the P2 connector), 101 through 150 (the second row from the front panel) and 151 through 200 (the row nearest the front panel. Figure 2–7, below, shows the pinout looking into the connectors on the top side of the board. The silkscreen on the motherboard indicates the pinout of the connector. Table 2–13, on the next page, defines the pin assignments of the connector.

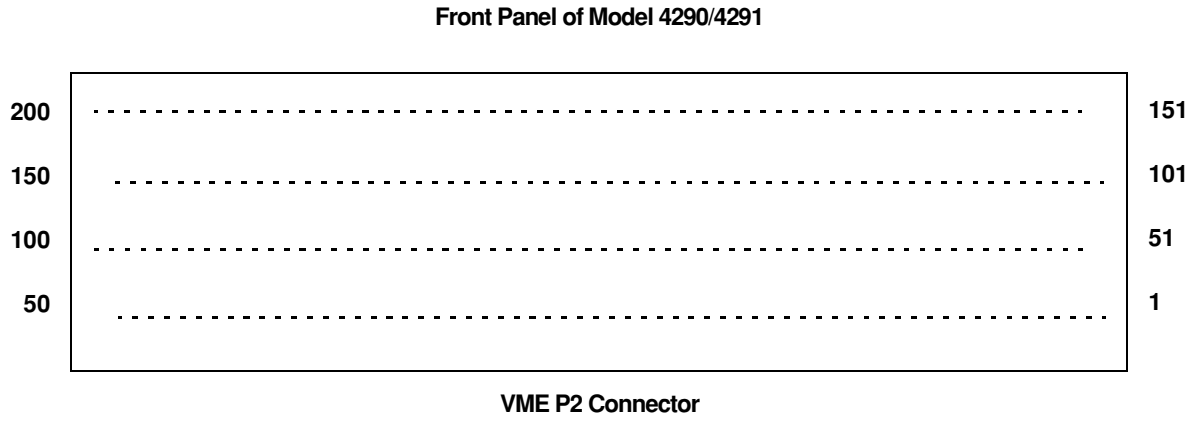


Figure 2–7: Model 4290/4291 –Global Bus / P2 Expansion Connector Pin Numbering (Top View)

Connector Definition: Samtec Full Line Catalog, F–197–1, Sept. '97, Pages 38–39

Model 4290/4291 Connector: Samtec SOLC–150–02–S–Q–LC: 200 pin, surface mount, gold contact, locking clip

Daughterboard Connector: Samtec TOLC–150–32–S–Q–LC: 200 pin, surface mount, gold post, locking clip, for 0.472 in mated height

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2.5 The Global Bus Slave Expansion Connector (continued)

Table 2–13: Model 4290/4291 –Global Bus / P2 Interface Connector Pinout

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	GDAT0	51	GDAT1	101	P2_A1	151	P2_C1
2	GDAT2	52	GDAT3	102	P2_A2	152	P2_C1
3	GDAT4	53	GDAT5	103	P2_A3	153	P2_C3
4	GDAT6	54	GDAT7	104	P2_A4	154	P2_C4
5	$+12V_{DC}$	55	$+12V_{DC}$	105	$+12V_{DC}$	155	$+12V_{DC}$
6	GDAT8	56	GDAT9	106	P2_A5	156	P2_C5
7	GDAT10	57	GDAT11	107	P2_A6	157	P2_C6
8	GDAT12	58	GDAT13	108	P2_A7	158	P2_C7
9	GDAT14	59	GDAT15	109	P2_A8	159	P2_C8
10	$-12V_{DC}$	60	$-12V_{DC}$	110	$-12V_{DC}$	160	$-12V_{DC}$
11	GDAT16	61	GDAT17	111	P2_A9	161	P2_C9
12	GDAT18	62	GDAT19	112	P2_A10	162	P2_C10
13	GDAT20	63	GDAT21	113	P2_A11	163	P2_C11
14	GDAT22	64	GDAT23	114	P2_A12	164	P2_C12
15	$+3.3V_{DC}$	65	$+3.3V_{DC}$	115	$+3.3V_{DC}$	165	$+3.3V_{DC}$
16	GDAT24	66	GDAT25	116	P2_A13	166	P2_C13
17	GDAT26	67	GDAT27	117	P2_A14	167	P2_C14
18	GDAT28	68	GDAT29	118	P2_A15	168	P2_C15
19	GDAT30	69	GDAT31	119	P2_A16	169	P2_C16
20	$+3.3V_{DC}$	70	$+3.3V_{DC}$	120	$+3.3V_{DC}$	170	$+3.3V_{DC}$
21	GADR0	71	GADR1	121	P2_A17	171	P2_C17
22	GADR2	72	GADR3	122	P2_A18	172	P2_C18
23	GADR4	73	GADR5	123	P2_A19	173	P2_C19
24	GADR6	74	GADR7	124	P2_A20	174	P2_C20
25	Gnd	75	Gnd	125	Gnd	175	Gnd
26	GADR8	76	GADR9	126	P2_A21	176	P2_C21
27	GADR10	77	GADR11	127	P2_A22	177	P2_C22
28	GADR12	78	GADR13	128	P2_A23	178	P2_C23
29	GADR14	79	GADR15	129	P2_A24	179	P2_C24
30	$+5\ V_{DC}$	80	$+5\ V_{DC}$	130	$+5\ V_{DC}$	180	$+5\ V_{DC}$
31	GADR16	81	GADR17	131	P2_A25	181	P2_C25
32	GADR18	82	GADR19	132	P2_A26	182	P2_C26
33	GADR20	83	GADR21	133	P2_A27	183	P2_C27
34	GADR22	84	GADR23	134	P2_A28	184	P2_C28
35	Gnd	85	Gnd	135	Gnd	185	Gnd
36	GADR24	86	GADR25	136	P2_A29	186	P2_C29
37	GADR26	87	GADR27	137	P2_A30	187	P2_C30
38	GADR28	88	GADR29	138	P2_A31	188	P2_C31
39	GADR30	89	GADR31	139	P2_A32	189	P2_C32
40	$+5\ V_{DC}$	90	$+5\ V_{DC}$	140	$+5\ V_{DC}$	190	$+5\ V_{DC}$
41	GADR32	91	Gnd	141	$\overline{AS}$	191	Gnd
42	Gnd	92	$\overline{DS}$	142	Gnd	192	$\overline{DSACK}$
43	GRW	93	$+5\ V_{DC}$	143	$\overline{GLO_RDY}$	193	$+5\ V_{DC}$
44	$+5\ V_{DC}$	94	$\overline{GDB_INT}$	144	$+5\ V_{DC}$	194	Reserved
45	Reserved	95	Gnd	145	Reserved	195	Gnd
46	Gnd	96	Reserved	146	Gnd	196	Reserved
47	Reserved	97	$+5\ V_{DC}$	147	$\overline{SPARE1}$	197	$+5\ V_{DC}$
48	$+5\ V_{DC}$	98	$\overline{SPARE2}$	148	$+5\ V_{DC}$	198	$\overline{SPARE3}$
49	$\overline{SPARE4}$	99	$+5\ V_{DC}$	149	$\overline{SPARE5}$	199	$+5\ V_{DC}$
50	$\overline{DBPRSNT}$	100	$\overline{RESET}$	150	$\overline{SPARE6}$	200	CLK32MHz

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2.5 The Global Bus Slave Expansion Connector (continued)

2.5.1 Global Bus/P2 Interface Signal Definitions

The Global Bus/P2 expansion connector contains all of the signals necessary to perform data transfers between daughterboard resident resources, the 4290/4291's global bus, and the user defined pins contained on the VMEbus P2 connector. ***Mastership of the Model 4290/4291's Global bus by the daughterboard is not supported!*** Data transfers occur using a variant of the local bus timing of the VIC64. The VMEbus Interface Handbook (Cypress Semiconductor) is invaluable in the understanding of the signaling of this interface, the daughterboard expansion connector and the VME bus P2 connector. Signal directions are given from the perspective of the daugtherboard.

2.5.1.1 Global Bus Interface Signals

Signal Name	Dir	Description
GADR(32:0)	**I**	**Global Bus Address Lines:** These 5V logic level signals are directly connected to the global address bus of the VIM motherboard. Great care must be exercised in interfacing to these signals as all global accesses will be affected by their extension. These signals should be immediately buffered on the daughterboard with buffers being no more than 0.5 in. (12.7 mm) from the connector. Loading should be limited to a single FCT input load. For boards looking to master the bus, these signals are very heavily loaded on the motherboard so 64 mA drivers should be used wherever possible.
GDAT (31:0)	**I/O**	**Global Bus Data Lines:** These 5V logic level signals are directly connected to the global data bus of the VIM motherboard. Great care must be exercised in interfacing to these signals as all global accesses are impacted by their extension. Therefore, these signals should be immediately buffered on the daughterboard with buffers being no more than 0.5 in. (12.7 mm) from the connector. Loading should be limited to a single FCT load. These signals are moderately loaded on the motherboard, so high current drivers should be employed where possible.
$\overline{\text{GRW}}$	**I**	**Global Bus Write Enable:** This signal is driven low by global bus masters to indicate that a write is occurring across the bus. Great care must be exercised in interfacing to this signal as all global accesses are impacted by its extension. Therefore, GRW should be immediately buffered on the daughterboard with the buffer being no more than 0.5 in. (12.7 mm) from the connector. Loading should be limited to a single FCT load. The signal is valid prior to the assertion of AS and held through the entirety of the AS and DS active cycles.

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2.5 The Global Bus Slave Expansion Connector (continued)

2.5.1 Global Bus/P2 Interface Signal Definitions (continued)

2.5.1.1 Global Bus Interface Signals (continued)

Signal Name	Dir	Description
$\overline{\text{DS}}$	**I**	**Global Bus Data Strobe:** This signal is driven low to qualify data on the bus. During read operations, it is driven low in conjunction with $\overline{\text{AS}}$ to take the valid data from the requested resource. During write operations, the signal is driven low after $\overline{\text{AS}}$, when the data to be written is valid. The signal is rescinded upon receipt of an active DSACK or when a bus timeout occurs.
$\overline{\text{AS}}$	**I**	**Global Bus Address Strobe:** This signal is driven active to indicate that the address on the global bus is valid. It is rescinded upon receipt of an active $\overline{\text{DSACK}}$ or when a bus timeout occurs. When $\overline{\text{AS}}$ is asserted, the daughterboard interface logic should perform a decode on the presented address to determine if it must acknowledge the current global bus access.
$\overline{\text{DSACK}}$	**O**	**Global Bus Data Strobe Acknowledge:** This signal is driven active to acknowledge the completion of a data transfer across the interface. During single accesses, the signal should be rescinded in response to $\overline{\text{AS}}$ and $\overline{\text{DS}}$ being rescinded. Please refer to the Cypress Semiconductor VME–bus Interface handbook for proper acknowledgment of VME–bus slave block transfers to the interface.
$\overline{\text{GDB_INT}}$	**O**	**Global Daughterboard Interrupt Output:** This signal is driven low by the daughterboard when interrupting the motherboard. This signal is treated as an edge sensitive interrupt by the interrupt control logic, channeling an interrupt through to its destination upon detecting a high to low transition of this signal.
$\overline{\text{DBPRSNT}}$	**I**	**Global Daughterboard Present Signal:** This signal is tied to ground on the daughterboard to indicate to the motherboard when a global daughterboard is installed. The signal is connected to a pull up resistor and the Global Control Register on the motherboard. When no daughterboard is installed, the processor reads a 0 in the DB_Present field of the global control register.
$\overline{\text{RESET}}$	**O**	**Asynchronous Motherboard Reset:** This signal is driven active (low) whenever a full board reset occurs. This can occur at power-up, when the front panel reset switch is pressed, or when a reset occurs on the VME bus.
CLK32MHZ	**I**	**32 MHz Global Daughterboard Synchronization Clock:** This 5V logic level signal is in phase with the 64 MHz clock of the VIC64 and can be used to synchronize with timing on the motherboard.

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2.5 The Global Bus Slave Expansion Connector (continued)

2.5.1 Global Bus/P2 Interface Signal Definitions (continued)

2.5.1.2 VMEbus P2 Interface Signals

Signal Name	Dir	Description
P2_A(32:1)	**I/O**	**VME Connector P2 Row A user defined pins:** Each signal is a point to point connection to the corresponding pin on VME connector P2.
P2_C(32:1)	**I/O**	**VME Connector P2 Row C user defined pins:** Each signal is a point to point connection to the corresponding pin on VME connector P2.

2.5.1.3 Power Supply Connections

Signal Name	Dir	Description
+5V_{DC}	**I**	**+ 5 V_{DC} supply** provided by motherboard. 2A Max. (Pins 30, 40, 44, 48, 80, 90, 93,97, 130, 140, 144, 148, 180, 190, 193, 197)
+12V_{DC}	**I**	**+12 V_{DC} supply** provided by motherboard. 0.5 A Max. (Pins 5, 55, 105, 155)
–12V_{DC}	**I**	**–12 V_{DC} supply** provided by motherboard, 0.5 A max. (Pins 10, 60, 110, 160)
+3.3V_{DC}	**I**	**+ 3.3 V_{DC} supply** provided by motherboard, 1 A max. (Pins 15, 20, 65, 70, 115, 120, 165, 170)
Gnd	**I**	**Signal and power ground reference** provided by mother–board. (Pins 25, 35, 42, 46, 75, 85, 91, 95, 125, 135, 142, 146, 175, 185, 191, 195)

2.5.2 Global Slave Expansion Bus Access and Timing

The following information is useful for designing slave devices for use on the Model 4290/4291's Global Slave Expansion bus. For purposes of this discus–sion, we define the term "slave device" as one that takes the address bus as an input and responds to read and write cycles that are initiated by the VMEbus or the DSPs.

The global bus page register must be set to 0x0080 for access to the global con–nector.

Write cycles can function without the external assertion of $\overline{\text{DSACK}}$. Since this signal is required to be asserted by the external circuitry, the cycle takes 17 µsec before being terminated by an internal timeout signal. Read cycles, however, will not function without the external assertion of $\overline{\text{DSACK}}$.

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2.5 The Global Bus Slave Expansion Connector (continued)

2.5.2 Global Slave Expansion Bus Access and Timing (continued)

The setup time for the address, before the assertion of the address strobe (AS), is 40 nsec. The setup time for the data, before the assertion of the data strobe (DS), is 40 nsec. The hold time for the address after the de–assertion o the address strobe (AS), is 8 nsec. The hold time for data, after the de–assertion of the data strobe (DS), is 4 nsec. The setup time for the Global Bus write enable (GRW), before the assertion of the data strobe (DS), is 15 nsec. The hold time for the Global Bus write enable (GRW), after the de–assertion of the data strobe (DS), is 2 nsec.

The data strobe acknowledge signal (DSACK), may be asserted at any time after the data strobe (DS) is asserted, but before the timeout (e. g., within 10 µsec). After assertion of DSACK, DS will de–assert some time later (this can vary). DSACK should be de–asserted within 15 nsec after the de–assertion of DS. The timing information given above is illustrated in Figure 2–8, below, and summarized in Table 2–14, at the bottom of this page.

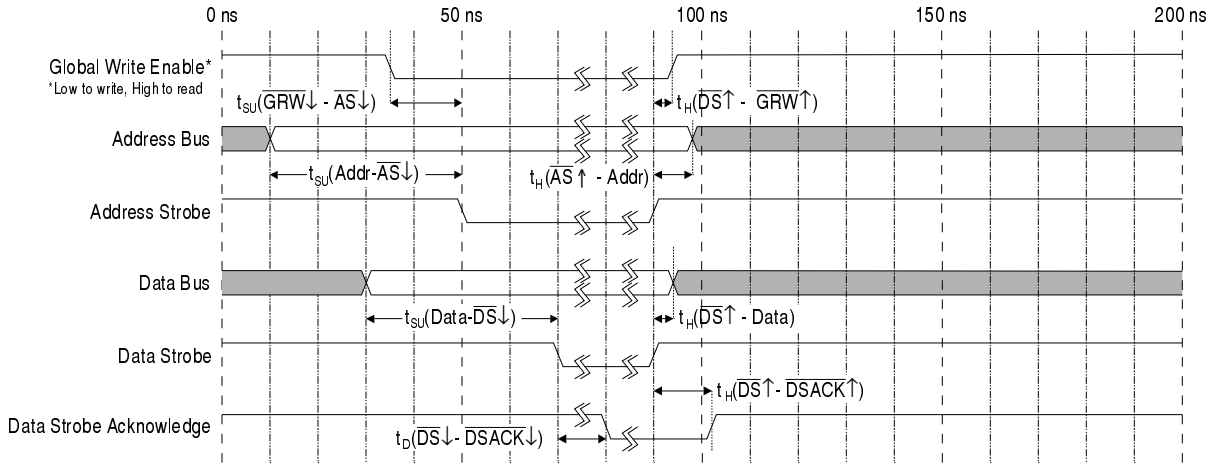


Figure 2-8: Model 4290/4291 –Global Expansion Bus Timing

Table 2–14: Model 4290/4291 Global Expansion Bus Timing

Interval (see Figure 2-8)	Time	Comment
t_{SU} (Addr –$\overline{AS}$)	40 nsec (min)	Setup time, Address bus stable before Address Strobe asserted
t_H ($\overline{AS}$ –Addr)	8 nsec (max)	Hold time, Address bus changes after Address Strobe rescinded
t_{SU} (Data –$\overline{DS}$)	40 nsec (min)	Setup time, Data bus stable before Data Strobe asserted
t_H ($\overline{DS}$ –Data)	4 nsec (min)	Hold time, Data bus changes after Data Strobe rescinded
t_{SU} ($\overline{GRW}$ –$\overline{AS}$)	15 nsec (min)	Setup time, Global Write Enable asserted before Address Strobe asserted
t_H ($\overline{DS}$ –$\overline{GRW}$)	2 nsec (min)	Hold time, Data Strobe rescinded before Global Write Enable rescinded
t_D ($\overline{DS}$ –$\overline{DSACK}$)	0 nsec (min), 17 µsec (max)	Delay time, Data Strobe asserted before Data Strobe Acknowledge asserted
t_H ($\overline{DS}$ –$\overline{DSACK}$)	15 nsec (max)	Hold time, Data Strobe rescinded before Data Strobe Acknowledge rescinded

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2.6 Installing/Removing VIM Modules on/from the Model 4290/4291

Complete instructions for the installation of VIM Modules are included in the operating manuals that are shipped with each module. Since installation may differ slightly from one module to another, please refer to the manual supplied with your VIM module for its particular installation procedure.

2.7 Installing the Model 4290/4291 in the VMEbus Card Cage

After you have verified and/or set the positions of all the jumpers on the Model 4290/4291, and installed any VIM expansion modules your application may require, you are ready to install the assembly in your VMEbus card cage.



TURN OFF ALL POWER IN THE CARD CAGE BEFORE INSERTING OR REMOVING ANY BOARD.

Align the Model 4290/4291 PC card edge with the card cage guides and push evenly and firmly on both ejector handles until the front panel seats against the upper and lower rails. Secure the unit to the card cage by tightening the upper and lower captive retaining screws in the front panel.

2.8 Removing the Model 4290/4291 from the VME Card Cage

Loosen the upper and lower retaining screws; these are captive screws and will remain part of the panel assembly. Gently push both ejector handles apart (away from the center of the panel) until the unit unseats itself from the cage connectors. Then pull outward to remove the unit.

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Chapter 3: Model 4290/4291 Addressing Overview

3.1 Introduction

This chapter provides an overview of the memory architecture used on the Model 4290/4291, and describes how the 'C6x processor's memory regions are apportioned to allow the DSP to access and share the various resources provided on this device. Specific memory maps for the various bus structures on the 4290/4291 will be covered in later chapters.

3.2 'C6x Addressing and CE Space Assignment

The five BOOTMODE pins on each of the 4290/4291's 'C6x processors are tied to supply rails (through resistors) such that BOOTMODE[4:0] = 00010. This selects internal Memory Map 0 (EMIF CE spaces precede Internal Program Memory in the memory map), 32–bit asynchronous memory with default timing at Address 0, and no boot process (i. e., the CPU begins direct execution from the memory located at address 0, which is the Model 4290/4291's Flash EEPROM).

The 'C6x processors on the Model 4290/4291 each have four memory windows, and each of these windows is associated with a Chip Enable, or CE, output pin on the processor. These four memory windows, referred to in Texas Instruments' 'C6x manuals (and herein as well, from now on) as CE spaces, can support four memory types – SBSRAM, SDRAM, ROM and Asynchronous memory. The only two restrictions regarding which kind of memory may be assigned to a given CE space are as follows – conventional ROM is ONLY supported in CE1 space, and SDRAM is NOT supported in CE1 space.

In the architecture used on the Model 4290/4291, the total amount of external memory available through direct addressing in the four CE spaces (CE0 – CE3) is 28 MBytes. In discussing the memory types assigned to each CE space, there are two cases to consider. Different resources are assigned to different CE spaces in 4290/4291s equipped with Option 330 and those without this option. When the term "**standard**" is used in this context, we are referring to a Model 4290/4291 equipped with any option or combination of options that **does NOT include Option 330**. On a standard 4290/4291, CE0 and CE1 spaces are both configured for Asynchronous memory, and CE3 space is configured for SBSRAM. On a 4290/4291 Option 330, CE0 and CE3 spaces are configured as Asynchronous, and CE1 space is configured for SBSRAM. CE2 space is configured for SDRAM in both architectures. Table 3–1, at the top of the next page, illustrates how the four CE spaces are assigned in both architectures of the Model 4290/4291.

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3.2 'C6x Addressing and CE Space Assignment (continued)

Table 3-1: Model 4290/4291 - CE Space Memory Window Setup for the 'C6x Processors

Memory Window	Standard				Option 330			
	Type	Space Available	Space Used	Resource	Type	Space Available	Space Used	Resource
CE3 Space	SBSRAM	4 MB	Opt. 244: 512 kB Opt. 240: 128 kB	SBSRAM	SBSRAM*	4 MB	12 KB	VIM & I-P BIFOs & Mailboxes
CE2 Space	SDRAM	16 MB	16 MB	SDRAM	SDRAM	16 MB	16 MB	SDRAM
CE1 Space	Async*	4 MB	12 KB	VIM & I-P BIFOs & Mailboxes	SBSRAM	4 MB	Opt. 244: 512 kB Opt. 240: 128 kB	SBSRAM
CE0 Space	Async	4 MB	4 MB	Global Bus Resources	Async	4 MB	4 MB	Global Bus Resources

*** NOTE: This memory space is programmable at the factory, and may be configured for either SBSRAM or Async timing, depending on your system requirements and the speeds of the processors and the Bi–FIFOs used in your particular configuration.**

The Model 4290/4291's architecture employs a hybrid addressing scheme, which allows the user a degree of trade–off between high performance and programming ease. The SDRAM and SBSRAM memory windows (CE2 and CE3 spaces, respectively, on a standard unit, or CE2 and CE1 on Option 330) are not affected by this hybrid scheme, as the processors are directly connected to these memory resources. The Bi–FIFO window (CE1 on the standard unit, CE3 on Option 330) is the less complicated of the remaining two windows, as that memory space may be programmed for either SBSRAM or Asynchronous timing, and employs a switched–bank architecture on the standard units. The tradeoff considerations for selecting the Bi–FIFO interface's timing, as well as a detailed description of the operation of these address spaces, is provided in Chapter 6 of this manual, which begins on page 151. The switched–bank architecture is employed to assure optimal performance of the inter–processor and VIM Bi–FIFO paths. Since SBSRAM timing does not allow an adequate amount of time for the logic to perform an address decode on the fly, a pre–decode is performed through the programming of the processor's Miscellaneous Control Register (MCR0). D15 and D14 of the MCR0 control which Bi–FIFO is logically connected to the processor.

In SBSRAM mode, this structure allows each of the FIFO paths to operate at a peak throughput of 100 MB/sec on Standard 4290/4291s. Since a decode in the Asynchronous space would also force a wait state on access, the switched–bank architecture is also useful with this timing.

On Option 330 units, the Bi–FIFOs are mapped and accessed quite differently from the way they are handled on standard units. Option 330's faster Bi–FIFOs are mapped into CE3 space, rather than CE1 space, and each Bi–FIFO is mapped into a unique address range, as opposed to mapping all 3 Bi–FIFOs into the same address space & selecting a specific one via register settings. The Option 330 Bi–FIFOs always use SBSRAM timing, and can operate at a peak throughput of 400 MB/sec.

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3.3 Access to Global Bus Resources by the 'C6x Via the Page Register

Since the 'C6x only offers a maximum address space of 4 MBytes in its Asynchronous window (CE0 space) a paging scheme is employed to allow the addressing of over 2 GBytes, providing the address space necessary for the processor to address all of the board's resources and the VMEbus. Additionally, since some resources, including processor's private registers, the local side of the processor's Dual Port SRAM, and the Random Access VIM interface need to be accessible at all times, this space is divided into two distinct regions, with Global resources occupying the lower 2 MByte region (where A21 = 0) and Private (i. e., Local) resources in the upper 2 MBytes (where A21 = 1). The division of this window was done in this manner to facilitate a quick and simple decode. At reset, the Page Register is set to 0x0000 0000, so the processor is automatically pointed to the Flash EEPROM portion of this window, for boot purposes. The Asynchronous address space is graphically illustrated in Figure 3–1, on the next page.

A local 16–bit Page Register exists for each processor. The upper 12 and lower 2 bits of the register contain the page address field and byte address. Bits 2 and 3 are reserved. The page field is copied into a 32–bit memory location shifted left by 17 bits (such that D14 in the page register will be aligned with the A31 address bit) and the resulting quantity is added to the processor's buffered address to form the 32–bit Global bus address. The most significant bit of the Page Register (bit D15) is set only for A32 VMEbus master accesses. If that bit is set to the logic '1' state, an A32 VMEbus master access will be performed, and the 11 remaining bits of the Page Register are combined with the Global bus address generated by the 'C6x as described above to form the VMEbus address that will be accessed. This allows the processor to have full access to the VMEbus A32 address space. The lower two bits of the Page Register (D1 & D0) specify the VME byte address. The user should be aware that the 'C6x processors on the standard versions of the Models 4290 and 4291 are configured as big endian devices, and this configuration cannot be changed. When compiling code for these Model 4290s or 4291s, your compiler's switches must be set for big endian. The exception to this rule is units equipped with Option 330. On these devices, the endian mode of the processors can be configured by a jumper as either big endian (the default setting) or little endian. For further information, please refer to Section 2.2.7.

After a processor has been granted the bus, the contents of the Page Register and buffered versions of the processor's address and byte enables are combined to drive the bus. The 11 most significant bits of the Global bus address (GA31 : GA21) are taken from bits D14:D4 of the Page Register, and the 21 least significant bits of the Global bus address are formed from bits 20:2 of the processor's address bus (these bits are buffered to form GA20:GA2) and the processor's encoded byte enables (which are used as GA1 and GA0).

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3.3 Access to Global Bus Resources by the 'C6x Via the Page Register (continued)

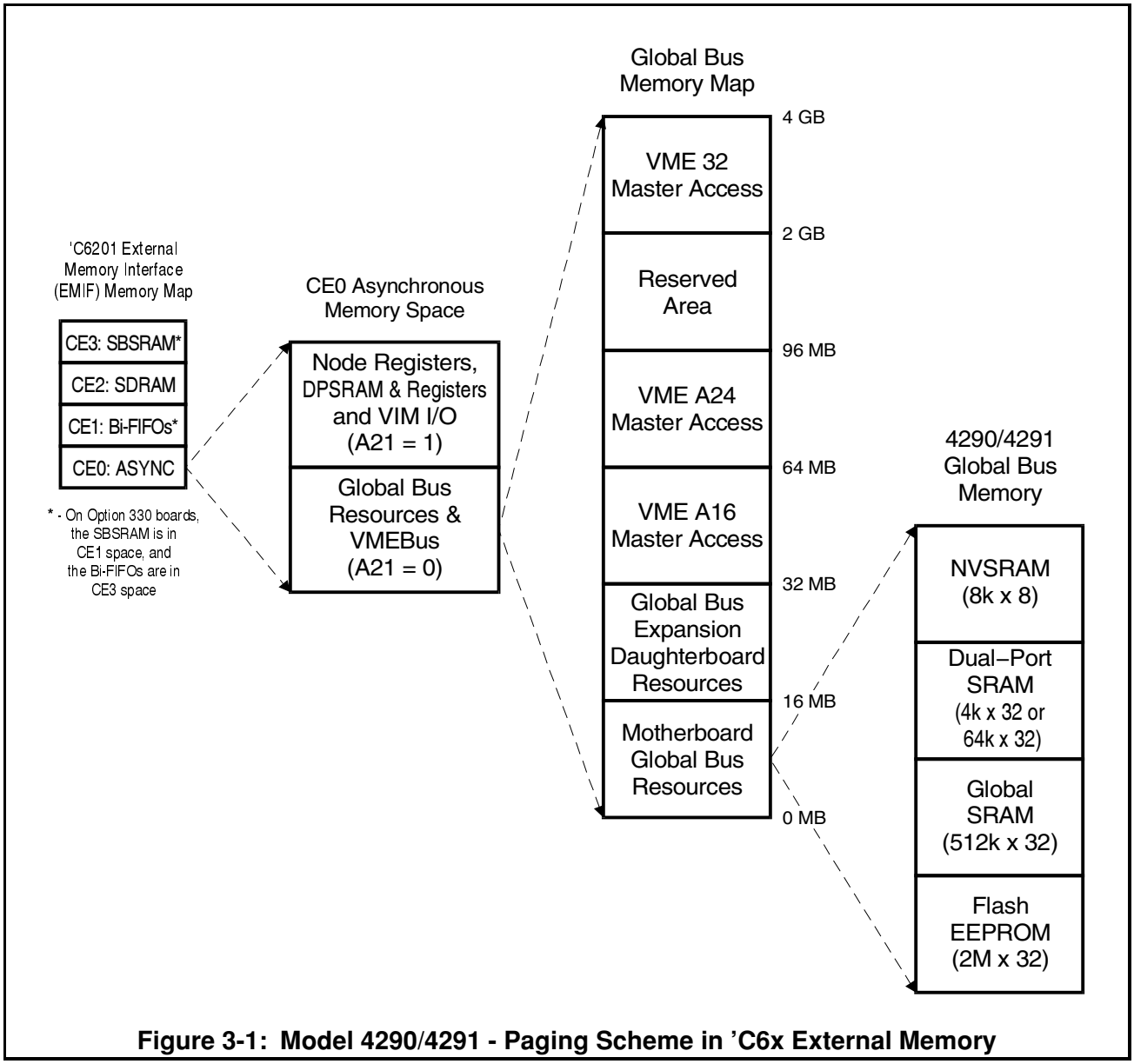


Figure 3-1: Model 4290/4291 - Paging Scheme in 'C6x External Memory

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Chapter 4: 'C6x Local (V–bus) Memory Maps and Resources

4.1 'C6x V–bus Memory Maps

The memory map for resources that are accessed via each 'C6x's V–bus (the DSP's local bus) on a standard (i. e., non–Option 330) Model 4290 or 4291 is shown in Table 4–1, below. The memory map for resources that are accessed via each 'C6x's V–bus on a Model 4290 or 4291 equipped with Option 330 is shown in Table 4–2, on the next page.

Table 4-1: Standard Model 4290/4291 - 'C6x V-bus Memory Map

'C6x Address Range	Size of Region	Resource	Data Width	Access Time	Add'l info
*0x0000 0000 –0x001F FFFF	2 MBytes	*Paged Access to Global Bus: Global SRAM, Flash EEPROM, NVSRAM, etc. (CE0 Space)	32 Bits	TBD	Sections 4.2 and 7.3
0x0020 0000 –0x0023 FFFF	256 kBytes	Dual Port SRAM (Local Side, CE0 Space)	32 Bits	4 clk	Section 7.2
0x0024 0000 –0x0027 FFFF	256 kBytes	Local DPSRAM Mailbox, Interrupts (CE0 Space)	32 Bits	4 clk	Sections 7.2.2 and 7.2.3
0x0028 0000 –0x002B FFFF	256 kBytes	Local Control Registers (CE0 Space)	32 Bits	10 clk	Sections 4.3.2 and 6.4
0x002C 0000 –0x002F FFFF	256 kBytes	Reserved (CE0 Space)	N/A	N/A	—
0x0030 0000 –0x0033 FFFF	256 kBytes	VIM Module Random Access (CE0 Space)	32 Bits	**	Section 4.3.3
0x0034 0000 –0x00FF FFFF	12.75 MBytes	Reserved (CE0 Space)	N/A	N/A	—
0x0100 0000 –0x011F FFFF	2 MBytes	I-P Comm FIFOs & VIM FIFO (CE1 Space)	32 Bits	2 clk or 4 clk	Chapter 6
0x0120 0000 –0x013F FFFF	2 MBytes	I-P Comm FIFO & VIM FIFO Mailboxes (CE1 Space)	32 Bits	2 clk or 4 clk	
0x0140 0000 –0x0140 FFFF	64 kBytes	Internal Program Memory†	32 Bits	1 clk	Section 4.3.6
0x0141 0000 –0x017F FFFF	3936 kBytes	Reserved	N/A	N/A	—
0x0180 0000 –0x01BF FFFF	4 MBytes	Internal Peripheral Space	32 Bits	1 clk	Section 4.3.7
0x01C0 0000 –0x01FF FFFF	4 MBytes	Reserved	N/A	N/A	—
0x0200 0000 –0x02FF FFFF	16 MBytes	SDRAM (CE2 Space)	32 Bits	2 clk	Section 4.3.8
0x0300 0000 –0x0307 FFFF	512 kBytes	SBSRAM (CE3 Space)	32 Bits	1 clk	Section 4.3.9
0x0308 0000 –0x03FF FFFF	15.5 MBytes	Reserved (CE3 Space)	32 Bits	N/A	—
0x0400 0000 –0x7FFF FFFF	1984 MBytes	Reserved	N/A	N/A	—
0x8000 0000 –0x8000 FFFF	64 kBytes	Internal Data Memory‡	32 Bits	1 clk	Section 4.3.10
0x8001 0000 –0xFFFF FFFF	(2048 MB –64 kB)	Reserved	N/A	N/A	—

*** –Page Register must be set to select desired resource prior to access.**

**** –Access times across this interface are largely determined by the slave device being accessed.**

† – When using 'C6x Internal Program Memory (IPM), the chip's cache must be disabled. When cache is enabled, refresh cycles occur periodically in IPM space. If a program is placed into IPM, the refresh cycle may cause the program to be flushed. Cache is disabled by clearing bits D5-D7 of the 'C6x's internal Control/Status Register (CSR) to the logic '0' state.

‡ –The Internal Data Memory can be used in conjunction with the Internal Program Memory to provide extra program space internal to the 'C6x.

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4.1 'C6x V–bus Memory Maps (continued)

Table 4-2: Model 4290/4291 Option 330 - 'C6x V-bus Memory Map

'C6x Address Range	Size of Region	Resource	Data Width	Access Time	Add'l Info
***0x0000 0000 –0x001F FFFF**	2 MBytes	*Paged Access to Global Bus: Global SRAM, Flash EEPROM, NVSRAM, etc. (CE0 Space)	32 Bits	TBD	Sections 4.2 and 7.3
0x0020 0000 –0x0023 FFFF	256 kBytes	Dual Port SRAM (Local Side) (CE0 Space)	32 Bits	4 clk	Section 7.2
0x0024 0000 –0x0027 FFFF	256 kBytes	Local DPSRAM Mailbox, Interrupts (CE0 Space)	32 Bits	4 clk	Sections 7.2.2 and 7.2.3
0x0028 0000 –0x002B FFFF	256 kBytes	Local Control Registers (CE0 Space)	32 Bits	10 clk	Sections 4.3.2 and 6.4
0x002C 0000 –0x002F FFFF	256 kBytes	Reserved (CE0 Space)	N/A	N/A	—
0x0030 0000 –0x0033 FFFF	256 kBytes	VIM Module Random Access (CE0 Space)	32 Bits	**	Section 4.3.3
0x0034 0000 –0x00FF FFFF	12.75 MBytes	Reserved (CE0 Space)	N/A	N/A	—
0x0100 0000 –0x0107 FFFF	*512 kBytes*	*SBSRAM (CE1 Space)*	*32 Bits*	*1 clk*	*Section 4.3.9*
0x0108 0000 –0x013F FFFF	3.5 MBytes	Reserved (CE1 Space)	32 Bits	N/A	—
0x0140 0000 –0x0140 FFFF	64 kBytes	Internal Program Memory†	32 Bits	1 clk	Section 4.3.6
0x0141 0000 –0x017F FFFF	3936 kBytes	Reserved	N/A	N/A	—
0x0180 0000 –0x01BF FFFF	4 MBytes	Internal Peripheral Space	32 Bits	1 clk	Section 4.3.7
0x01C0 0000 –0x01FF FFFF	4 MBytes	Reserved	N/A	N/A	—
0x0200 0000 –0x02FF FFFF	16 MBytes	SDRAM (CE2 Space)	32 Bits	2 clk	Section 4.3.8
0x0300 0000 –0x0303 FFFF	*256 kBytes*	*FIFO XX (Upstream –CE3 Space)*	*32 Bits*	*2 or 4 clk*	*Chapter 6*
0x0304 0000 –0x0307 FFFF	*256 kBytes*	*FIFO XX Mailbox (Upstream –CE3 Space)*	*32 Bits*	*2 or 4 clk*	
0x0308 0000 –0x030B FFFF	*256 kBytes*	*FIFO ZZ (Downstream –CE3 Space)*	*32 Bits*	*2 or 4 clk*	
0x030C 0000 –0x030F FFFF	*256 kBytes*	*FIFO ZZ Mailbox (Downstream –CE3 Space)*	*32 Bits*	*2 or 4 clk*	
0x0310 0000 –0x0313 FFFF	*256 kBytes*	*VIM FIFO (CE3 Space)*	*32 Bits*	*2 or 4 clk*	
0x0314 0000 –0x0317 FFFF	*256 kBytes*	*VIM FIFO Mailbox (CE3 Space)*	*32 Bits*	*2 or 4 clk*	
0x0308 0000 –0x03FF FFFF	15.5 MBytes	Reserved (CE3 Space)	32 Bits	N/A	—
0x0400 0000 –0x7FFF FFFF	1984 MBytes	Reserved	N/A	N/A	—
0x8000 0000 –0x8000 FFFF	64 kBytes	Internal Data Memory‡	32 Bits	1 clk	Section 4.3.10
0x8001 0000 –0xFFFF FFFF	(2048 MB –64 kB)	Reserved	N/A	N/A	—

The italic typeface is used to highlight the differences between the Standard and Option 330 Memory Maps

*** –Page Register must be set to select desired resource prior to access.**

**** –Access times across this interface are largely determined by the slave device being accessed.**

† - When using 'C6x Internal Program Memory (IPM), the chip's cache must be disabled. When cache is enabled, refresh cycles occur periodically in IPM space. If a program is placed into IPM, the refresh cycle may cause the program to be flushed. Cache is disabled by clearing bits D5-D7 of the 'C6x's internal Control/Status Register (CSR) to the logic '0' state.

‡ –The Internal Data Memory can be used in conjunction with the Internal Program Memory to provide extra program space internal to the 'C6x.

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4.2 'C6x Access to Global Bus Resources

The 'C6x processors on the Models 4290 and 4291 can gain access to the resources that are located on the device's Global bus. A 2 MByte region of the 'C6x's V–bus memory map is reserved for access to Global bus resources. You may well ask how it is that the 'C6x can access 8 MBytes of Flash EEPROM, 2 MBytes of Global SRAM, 8 kBytes of NVSRAM, and all 3 regions of VMEbus memory space in a 2MByte memory region. The answer is that a Page Register is provided, at 'C6x address 0x0028 0024, which segments the Global bus region into a group of "pages", each sized at 2 MBytes. Table 4–3, below, gives the Page Register value to use for accessing each Global bus resource via any 'C6x's V–bus.

Table 4-3: Model 4290/4291 –Global Bus Page Register Settings (R/W @ 'C6x V-bus Address 0x0028 0024)

Resource	Setting	Base Offset*	Size	# pages
Flash EEPROM	0x0000 000y – 0x0000 003y	0x0000 0000	8 MBytes	4
Global SRAM	0x0000 004y	0x0000 0000	2 MBytes	1
Dual Port SRAM –Processor A	0x0000 005y	0x0000 0000	256 kBytes	1**
Processor A DPSRAM Mailboxes	0x0000 005y	0x0004 0080	256 kBytes	1**
Dual Port SRAM –Processor C	0x0000 005y	0x0008 0000	256 kBytes	1**
Processor C DPSRAM Mailboxes	0x0000 005y	0x000C 0080	256 kBytes	1**
Dual Port SRAM –Processor D	0x0000 005y	0x0010 0000	256 kBytes	1**
Processor D DPSRAM Mailboxes	0x0000 005y	0x0014 0080	256 kBytes	1**
Dual Port SRAM –Processor B	0x0000 005y	0x0018 0000	256 kBytes	1**
Processor B DPSRAM Mailboxes	0x0000 005y	0x001C 0000	256 kBytes	1**
NVSRAM	0x0000 006y	0x0000 0000	1 MByte	1
Global Bus Control Registers	0x0000 007y	0x0000 0000	2 MBytes	1†
VIC64 Registers	0x0000 007y	0x0010 0000		1†
CY7C964 Compare Register	0x0000 007y	0x0011 0000		1†
CY7C964 Mask Register	0x0000 007y	0x0011 4000		1†
Global Expansion Bus	0x0000 008y – 0x0000 00Fy	0x0000 0000	16 MBytes	8
VMEbus A16 Master Access	0x0000 010y – 0x0000 17y	0x0000 0000	16 MBytes	8
VMEbus A24 Master Access	0x0000 018y – 0x0000 01Fy	0x0000 0000	16 MBytes	8
VMEbus A32 Master Access	0x0000 800y 0x0000 FFFy	0x0000 0000	4 GBytes	2048

NOTES: y = (0:3) = the setting of the Byte Select field (see Section 4.3.2.7 & Table 4-25)
*** –The offset value given is for the base address of the indicated memory region. See the text on the next page for the equation to calculate the page offset as a function of the absolute Global bus address.**
**** - These resources occupy the same page in 'C6x memory**
† - These resources occupy the same page in 'C6x memory

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4.2 'C6x Access to Global Bus Resources (continued)

Given any absolute Global bus address, you can calculate the Page Register value by using the following formula:

Page_Reg_Value = (Address & 0xFFE0 0000) >> 17

For VMEbus master accesses, the offset can be calculated as follows:

Offset = (Address & 0x001F FFFF)

Additionally, when performing VMEbus A32 master accesses from a 'C6x, the most significant bit in the Page Register must be set, using:

VME32_Page_Reg_Value = ((Address & 0xFFE0 0000) >> 17) | 0x8000

The two least significant bits of the Page Register are used only when the 'C6x performs VMEbus master accesses, and should contain physical VMEbus address bits A0 (in D0) and A1 (in D1) for all such transfers.

Additionally, because all resources on the Global bus are shared by all four processors on the 4290/4291 and the VMEbus, mastership of the bus must be arbitrated for. The arbitration scheme used for the 4290/4291's Global bus is hierarchical in nature. In any situation where there is contention for this bus structure, the VMEbus has the highest priority. The second level of the arbitration is a round robin, which assigns priority to each processor on a rotating basis. Of course, if the bus is idle and the lowest priority processor makes an uncontended bus request, it will be immediately granted owner–ship of the bus.

A 'C6x requests the Global bus by making an access to its own CE0 space, with address line A21 in the logic '0' state (i. e., simply by accessing any resource on that bus). Once a master has been granted the Global bus, it can temporarily prevent additional arbi–tration by "locking" the arbiter, using the Bus Lock bit (D1 in the Miscellaneous Inter–rupt & VME Control Register (MIVR) at V–bus address 0x0028 0018 (see page 90, in Section 4.3.2.4). Alternatively, exclusive access to a given Global bus resource can be maintained by implementing a semaphore system, using the General Purpose Global Semaphore bits, in the Local Semaphore Register at V–bus address 0x0028 0028 (see Section 4.3.2.8).

The sections that follow, which describe these shared resources, will give the VME–bus address in addition to the 'C6x address. In this context, we will use the term "VME_base" to mean either the A32 base address (set by jumpers AJ1 : AJ8, see Sec–tion 2.2.1 and Table 2–1) or the A24 base address, which is always 0x00 0000.

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.1 'C6x Access to Flash EEPROM

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0000 : 0x0000 0030
Base Offset – 0x0000 0000

Global Bus Address Region – 0x0000 0000 : 0x007F FFFF
VMEbus Address Region – VME_base+0x0000 0000 : 0x007F FFFF

Except in the special cases of downloading user boot code (see Section 8.12) or upgrading the factory boot code (please refer to the Release Note entitled Updating Model 4290/4291 's Boot Firmware, Pentek part # 800.42908) access to this resource is Read–Only. Because this resource is larger than the 'C6x page size, it appears as four, 512k x 32 blocks of ROM, each of which requires a different Page Register setting for access. VMEbus masters can access this resource in A24 and A32 space (in D32 mode), in the address range from VME_base+0x0000 0000 : VME_base+0x007F FFFF.

4.2.2 'C6x Access to Global SRAM

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0040
Base Offset – 0x0000 0000

Global Bus Address Region – 0x0080 0000 : 0x009F FFFF
VMEbus Address Region – VME_base+0x0080 0000 : 0x009F FFFF

This 512k x 32 block of Static RAM is the primary resource for the sharing of data between the 'C6x processors on the Model 4290/4291 and the VMEbus. It appears as a single block of RAM in the memory maps of the 'C6x proces–sors (where it can be accessed ONLY in D32 mode) and the A24/A32 VME slave memory maps (where it is accessible in D8, D16 and D32 modes, in the address range VME_base+0x0080 0000 : VME_base+09F FFFF).

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.3 'C6x Access to Global Side of Dual Port SRAM & Mailboxes

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0050

Base Offsets –

DPSRAM A	**– 0x0000 0000**	**DP A Mailboxes**	**– 0x0004 0080**
DPSRAM C	**– 0x0008 0000**	**DP C Mailboxes**	**– 0x000C 0080**
DPSRAM D	**– 0x0010 0000**	**DP D Mailboxes**	**– 0x0014 0080**
DPSRAM B	**– 0x0018 0000**	**DP B Mailboxes**	**– 0x001C 0080**

Global Bus Address Region – 0x00A0 0000 : 0x00BF FFFF
DPSRAM A – 0x00A0 0000 : 0x00A3 FFFF
DP A Mailboxes – 0x00A4 0080 : 0x00A7 FFFF
DPSRAM C – 0x00A8 0000 : 0x00AB FFFF
DP C Mailboxes – 0x00AC 0080 : 0x00AF FFFF
DPSRAM D – 0x00B0 0000 : 0x00B3 FFFF
DP D Mailboxes – 0x00B4 0080 : 0x00B7 FFFF
DPSRAM B – 0x00B8 0000 : 0x00BB FFFF
DP B Mailboxes – 0x00BC 0080 : 0x00BF FFFF

VMEbus Address Region – VME_base+0x00A0 0000 : 0x00BF FFFF

Chapter 7 of this manual provides a complete discussion of the Dual Port SRAMs on the Model 4290/4291, and covers all the details about how these SRAM banks and mailboxes are accessed from both the Global bus and Local (V–bus) sides. The topic of Global bus access to the Dual Port SRAMs is covered in Section 7.3. In this chapter, we will simply present the memory map used by the 'C6x processors to access these resources via the Global bus, in Table 4–4, on the next two pages. For more detailed information, please refer to Section 7.3 and its subsections.

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.3 'C6x Access to Global Side of Dual Port SRAM (continued)

Table 4-4: Model 4290/4291 –Memory Map for Global Bus Side of Dual Port SRAM – Addresses for 'C6x V-bus Access - (Page Register Setting = 0x0000 0050)

Resource	Access	Option 244	Option 240
DPSRAM A, bank 0, Global Port	R/W	0x0000 0000 : 0x0000 3FFF	0x0000 0000 : 0x0000 1FFF
DPSRAM A, bank 1, Global Port		0x0000 4000 : 0x0000 7FFF	0x0000 2000 : 0x0000 3FFF
DPSRAM A, bank 2, Global Port		0x0000 8000 : 0x0000 BFFF	0x0000 4000 : 0x0000 5FFF
DPSRAM A, bank 3, Global Port		0x0000 C000 : 0x0000 FFFF	0x0000 6000 : 0x0000 7FFF
Reserved	—	0x0001 0000 : 0x0003 FFFF	0x0000 8000 : 0x0003 FFFF
Reserved		0x0004 0000 : 0x0004 007F	
Global Port A → V-bus A DPSRAM Mailbox	R/W	0x0004 0080	
Global Port C → V-bus A DPSRAM Mailbox		0x0004 0084	
Global Port D → V-bus A DPSRAM Mailbox		0x0004 0088	
Global Port B → V-bus A DPSRAM Mailbox		0x0004 008C	
V-bus A → Global Port A DPSRAM Mailbox	R. O.	0x0004 0090	
V-bus A → Global Port C DPSRAM Mailbox		0x0004 0094	
V-bus A → Global Port D DPSRAM Mailbox		0x0004 0098	
V-bus A → Global Port B DPSRAM Mailbox		0x0004 009C	
DP Interrupt Control/Status Register A	R/W	0x0004 00A0	
Reserved	—	0x0004 00A4 : 0x0007 FFFF	
DPSRAM C, bank 0, Global Port	R/W	0x0008 0000 : 0x0008 3FFF	0x0008 0000 : 0x0008 1FFF
DPSRAM C, bank 1, Global Port		0x0008 4000 : 0x0008 7FFF	0x0008 2000 : 0x0008 3FFF
DPSRAM C, bank 2, Global Port		0x0008 8000 : 0x0008 BFFF	0x0008 4000 : 0x0008 5FFF
DPSRAM C, bank 3, Global Port		0x0008 C000 : 0x0008 FFFF	0x0008 6000 : 0x0008 7FFF
Reserved	—	0x0009 0000 : 0x000B FFFF	0x0008 8000 : 0x000B FFFF
Reserved		0x000C 0000 : 0x000C 007F	
Global Port A → V-bus C DPSRAM Mailbox	R/W	0x000C 0080	
Global Port C → V-bus C DPSRAM Mailbox		0x000C 0084	
Global Port D → V-bus C DPSRAM Mailbox		0x000C 0088	
Global Port B → V-bus C DPSRAM Mailbox		0x000C 008C	
V-bus C → Global Port A DPSRAM Mailbox	R. O.	0x000C 0090	
V-bus C → Global Port C DPSRAM Mailbox		0x000C 0094	
V-bus C → Global Port D DPSRAM Mailbox		0x000C 0098	
V-bus C → Global Port B DPSRAM Mailbox		0x000C 009C	
DP Interrupt Control/Status Register C	R/W	0x000C 00A0	
Reserved	—	0x000C 00A4 : 0x000F FFFF	

NOTES:
The Page Register MUST be set to 0x0000 0050 BEFORE any attempt to access the Dual Port SRAM via the Global bus.
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.
Table 4-4 is Table 4-4: Model 4290/4291 - Memory Map for Global Bus Side of Dual Port SRAM - Addresses for 'C6x V-bus Access - (Page Register setting = 0x0000 0050) (continued) (continued) **on the next page**

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.3 'C6x Access to Global Side of Dual Port SRAM (continued)

Table 4-4: Model 4290/4291 –Memory Map for Global Bus Side of Dual Port SRAM – Addresses for 'C6x V-bus Access - (Page Register setting = 0x0000 0050) (continued)

Resource	Access	Option 244	Option 240
DPSRAM D, bank 0, Global Port	R/W	0x0010 0000 : 0x0010 3FFF	0x0010 0000 : 0x0010 1FFF
DPSRAM D, bank 1, Global Port		0x0010 4000 : 0x0010 7FFF	0x0010 2000 : 0x0010 3FFF
DPSRAM D, bank 2, Global Port		0x0010 8000 : 0x0010 BFFF	0x0010 4000 : 0x0010 5FFF
DPSRAM D, bank 3, Global Port		0x0010 C000 : 0x0010 FFFF	0x0010 6000 : 0x0010 7FFF
Reserved	—	0x0011 0000 : 0x0013 FFFF	0x0010 8000 : 0x0013 FFFF
Reserved		0x0014 0000 : 0x0014 007F	
Global Port A → V-bus D DPSRAM Mailbox	R/W	0x0014 0080	
Global Port C → V-bus D DPSRAM Mailbox		0x0014 0084	
Global Port D → V-bus D DPSRAM Mailbox		0x0014 0088	
Global Port B → V-bus D DPSRAM Mailbox		0x0014 008C	
V-bus D → Global Port A DPSRAM Mailbox	R. O.	0x0014 0090	
V-bus D → Global Port C DPSRAM Mailbox		0x0014 0094	
V-bus D → Global Port D DPSRAM Mailbox		0x0014 0098	
V-bus D → Global Port B DPSRAM Mailbox		0x0014 009C	
DP Interrupt Control/Status Register D	R/W	0x0014 00A0	
Reserved	—	0x0014 00A4 : 0x0017 FFFF	
DPSRAM B, bank 0, Global Port	R/W	0x0018 0000 : 0x0018 3FFF	0x0018 0000 : 0x0018 1FFF
DPSRAM B, bank 1, Global Port		0x0018 4000 : 0x0018 7FFF	0x0018 2000 : 0x0018 3FFF
DPSRAM B, bank 2, Global Port		0x0018 8000 : 0x0018 BFFF	0x0018 4000 : 0x0018 5FFF
DPSRAM B, bank 3, Global Port		0x0018 C000 : 0x0018 FFFF	0x0018 6000 : 0x0018 7FFF
Reserved	—	0x0019 0000 : 0x001B FFFF	0x0018 8000 : 0x001B FFFF
Reserved		0x001C 0000 : 0x001C 007F	
Global Port A → V-bus B DPSRAM Mailbox	R/W	0x001C 0080	
Global Port C → V-bus B DPSRAM Mailbox		0x001C 0084	
Global Port D → V-bus B DPSRAM Mailbox		0x001C 0088	
Global Port B → V-bus B DPSRAM Mailbox		0x001C 008C	
V-bus B → Global Port A DPSRAM Mailbox	R. O.	0x001C 0090	
V-bus B → Global Port C DPSRAM Mailbox		0x001C 0094	
V-bus B → Global Port D DPSRAM Mailbox		0x001C 0098	
V-bus B → Global Port B DPSRAM Mailbox		0x001C 009C	
DP Interrupt Control/Status Register B	R/W	0x001C 00A0	
Reserved	—	0x001C 00A4 : 0x001F FFFF	

NOTES:
The Page Register MUST be set to 0x0000 0050 BEFORE any attempt to access the Dual Port SRAM via the Global bus.
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.4 'C6x Access to Non–Volatile SRAM

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0060
Base Offset – 0x0000 0000

Global Bus Address Region – 0x00C0 0000 : 0x00CF FFFF
VMEbus Address Region – VME_base+0x00C0 0000 : 0x00CF FFFF

This non–volatile memory resource is configured as 8k x 8. When the page register points to this resource, the first 8k addresses in this region are mirrored an additional 31 times in the 256 kByte window. The 'C6x processors access this resource in D32 mode, with valid data appearing only in the eight LSBs of each longword. VMEbus masters can also access this resource, in the address range from VME_base+0x00C0 0000 through VME_base+0x00CF FFFF.

4.2.5 'C6x Access to Global Bus Control Registers

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0070
Base Offset – 0x0000 0000

Global Bus Address Region – 0x00E0 0000 : 0x00EF FFFF
VMEbus Address Region – VME_base+0x00E0 0000 : 0x00EF FFFF

Three registers are accessible in this region, all of which are also accessible from the VMEbus. The register's names, and their addresses at which they are accessed from both the V–bus and the Global bus, are listed in Table 4–5, below. For further information about how to use these registers, please refer to the sub–sections indicated in the right–hand column of the table, which begin on the following page.

Table 4–5: Model 4290/4291 –Global Bus Control Registers

Register Name	V–bus Address (Page Reg. = 70)	Global Address	Additional Information
Global Dual Port SRAM Semaphore Register	0x0000 0000	0x00E0 0000	Section 4.2.5.1
General Purpose Global Semaphore Register	0x0000 0004	0x00E0 0004	Section 4.2.5.2
VME DSP Reset Control Register	0x0000 0008	0x00E0 0008	Section 4.2.5.3
NOTE: For VMEbus access, add the VME_base address to the Global bus address.			

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.5 'C6x Access to Global Registers (continued)

4.2.5.1 Global Dual Port Semaphore Register (DPSR)

'C6x Address – 0x0000 0000
Page Register – 0x0000 0070
Base Offset – 0x0000 0000

Global Bus Address – 0x00E0 0000
VMEbus Address – VME_base+0x00E0 0000

This register holds the semaphores that must be obtained by Global bus masters in order to access any of the Dual Port SRAM banks on the Model 4290/4291. For complete details about the use of this register, please refer to Section 7.3.1, which begins on page 192.

Table 4–6, below, shows the structure of the Global Dual Port SRAM Semaphore Register (DPSR). The upper 16 bits of this register's 32–bit memory location are unused. The remaining 16 bits are divided into four groups of four bits each, one group dedicated to each of the four DPSRAM blocks. one bit in each group controls the semaphore for one of the four banks in the associated block.

Table 4-6: Model 4290/4291 –Global Dual Port SRAM Semaphore Register (DPSR) – V-bus Access: R/W @ 0x0000 0000, Page Reg = 70 –Global Bus Access: R/W @ 0x00E0 0000 –VMEbus Access: R/W @ VME_base+0x00E0 0000

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Semaphore for . . .	DPSRAM_B _Bank_3	DPSRAM_B _Bank_2	DPSRAM_B _Bank_1	DPSRAM_B _Bank_0	DPSRAM_D _Bank 3	DPSRAM_D Bank 2	DPSRAM_D Bank 1	DPSRAM_D Bank 0
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Semaphore for . . .	DPSRAM_C _Bank_3	DPSRAM_C _Bank_2	DPSRAM_C _Bank_1	DPSRAM_C _Bank_0	DPSRAM_A _Bank 3	DPSRAM_A Bank 2	DPSRAM_A Bank 1	DPSRAM_A Bank 0

Semaphore Action Sequence –the following four–step sequence must be followed to obtain access to the Dual Port SRAM banks whose semaphores are controlled by the bits in this register –

Step **1** –**Read** a '**0**' in the associated bit **to check** the semaphore's **availability**
Step **2** - **Write** a '**1**' to the associated bit **to request ownership** of the semaphore
Step **3** - **Read** a '**1**' in the associated bit **to verify ownership** of the semaphore
Step **4** - **Write** a '**0**' to the associated bit **to release** the **semaphore** after completing the access.

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.5 'C6x Access to Global Registers (continued)

4.2.5.2 Global Bus General Purpose Semaphore Register (GBSR)

'C6x Address – 0x0000 0004
Page Register – 0x0000 0070
Base Offset – 0x0000 0000

Global Bus Address – 0x00E0 0004
VMEbus Address – VME_base+0x00E0 0004

Twelve additional, general purpose semaphores are provided on the Model 4290/4291, which may be assigned by the programmer to any shared resource on the board that may become a contended item. These semaphores are shared, on a bit–by–bit basis, between the four procesing nodes and the VMEbus. These semaphores are accessed by the DSPs through the 12 LSBs (D11 : D0) of their Local Semaphore Registers (LSRs). The GBSR is accessible to the VME–bus and to on–board DSPs when they master the Global bus, and is accessed at Global bus address 0x00E0 0004 (VME address VME_base+0x00E0 0004). The 'C6x's access this register by set–ting their page register to 0x0000 0070, and accessing address 0x0000 0004. The semaphores are contained in bits D11 : D0 of this register (bits D31 : D16 at this address are unused, and bits D15 : D12 are reserved).

The general purpose semaphores are obtained in the same man–ner as the Dual Port SRAM semaphores. At the beginning of the sequence, reading a '0' in the associated bit indicates that the semaphore may be available, a '1' indicates that it is already known to be owned by some master. If the semaphore might be available (i. e., if this read operation returns a '0'), a '1' is written to the associated bit to request it. This is followed by reading the bit, to confirm that the semaphore has been granted to the requesting processor (automatically resolved by hardware dur–ing contention). If the associated bit reads back as a '1', the pro–cessor has obtained the semaphore. After performing all necessary accesses, the owning processor writes a '0' to the asso–ciated bit to release the semaphore. At reset, all 12 general pur–pose semaphores are available.

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.5 'C6x Access to Global Registers (continued)

4.2.5.2 Global Bus General Purpose Semaphore Register (continued)

Table 4–7, below, illustrates the structure of the Global Bus General Purpose Semaphore Register.

Table 4–7: Model 4290/4291 –Global Bus General Purpose Semaphore Register (GBSR) – V-bus Access: R/W @ 0x0000 0004, Page Reg = 70 –Global Bus Access: R/W @ 0x00E0 0004 –VMEbus Access: R/W @ VME_base+0x00E0 0004

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Semaphore	Reserved				GP_Global_ Semaphore_11	GP_Global_ Semaphore_10	GP_Global_ Semaphore_9	GP_Global_ Semaphore_8
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D00**
Semaphore	GP_Global_ Semaphore_7	GP_Global_ Semaphore_6	GP_Global_ Semaphore_5	GP_Global_ Semaphore_4	GP_Global_ Semaphore_3	GP_Global_ Semaphore_2	GP_Global_ Semaphore_1	GP_Global_ Semaphore_0

Semaphore Action Sequence –the following four–step sequence must be followed to obtain access to the semaphores are controlled by the bits in this register –
Step **1** –**Read** a '**0**' in the associated bit **to check** the semaphore's **availability**
Step **2** - **Write** a '**1**' to the associated bit **to request ownership** of the semaphore
Step **3** - **Read** a '**1**' in the associated bit **to verify ownership** of the semaphore
Step **4** - **Write** a '**0**' to the associated bit **to release** the **semaphore** after completing the access.

4.2.5.3 VME DSP Reset Control Register (VRCR)

'C6x Address – 0x0000 0008
Page Register – 0x0000 0070
Base Offset – 0x0000 0000

Global Bus Address – 0x00E0 0008
VMEbus Address – VME_base+0x00E0 0008

This register was included to allow any or all of the Model 4290/4291's 'C6x processors to be reset from the VMEbus, although the register is also accessible to any device (including any on–board 'C6x processor) that can master the Global bus. Like the semaphore operations described in the sections above, the 'C6x reset requires a four–step sequence of operations on this register. Unlike the semaphore operations though, all the accesses in the reset sequence are writes.

Bits D31 : D16 at this address are unused. Bits D15 : D12 comprise a processor reset enable field. Each of these four bits is associated with one of the DSPs, and only those processors whose associated bits are set to the logic '1' state in this field will respond to the reset operation. D11 : D9 are also unused, and the 8 LSB's (D7 : D0) are the reset bits.

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.5 'C6x Access to Global Registers (continued)

4.2.5.3 VME DSP Reset Control Register (continued)

The reset sequence consists of four steps, as follows. First, the reg–ister should be cleared (i. e., write 0x0000 to it), to prepare it for the reset operation. The next three write operations will consist of '1's in the bits in the reset enable field (D15 : D12) for those processors you want to reset, '0's in bits D11 : D8, and the following data in the lower 8 bits (D7 : D0) – 0x88 (second write), 0x66 (third write) and 0x11 (fouth and final write).

EXAMPLE: The sequence detailed below would reset 'C6x pro–cessors B and C.

1) Write **0x0000** prepares the register to begin the reset sequence.

2) Write **0xA088** The '**A**' sets bits D15 & D13 to '1' (enabling processors B & C for reset), while '**088**' sets bits D7 and D3 to '1'.

3) Write **0xA066** The '**A**' sets bits D15 & D13 to '1' (enabling processors B & C for reset), while the '**066**' sets bits D6, D5, D2, and D1 to '1'.

4) Write **0xA011** The '**A**' sets bits D15 & D13 to '1' (enabling processors B & C for reset), while the '**011**' sets bits D4 and D0 to '1'.

Table 4–8, below, shows the bit structure of the VME DSP Reset Control Register.

Table 4-8: Model 4290/4291 –VME DSP Reset Control Register (VRCR) – V-bus Access: R/W @ 0x0000 0008, Page Reg = 70 –Global Bus Access: R/W @ 0x00E0 0008 –VMEbus Access: R/W @ VME_base+0x00E0 0008

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Function	Reset_ Enable_B	Reset_ Enable_D	Reset_ Enable_C	Reset_ Enable_A	Reserved			
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Function	Reset_ Bit_#7	Reset_ Bit_#6	Reset_ Bit_#5	Reset_ Bit_#4	Reset_ Bit_#3	Reset_ Bit_#2	Reset_ Bit_#1	Reset_ Bit_#0

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.6 'C6x Access to the VME Interface Configuration Registers

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0070
Base Offsets –
VIC 64 Registers – 0x0010 0000
CY7C964 Compare Register – 0x0011 0000
CY7C964 Mask Register – 0x0011 4000

Global Bus Address Region – 0x00F0 0000 : 0x00F1 FFFF
VIC 64 Registers – 0x00F0 0000 : 0x00F0 FFFF
CY7C964 Compare Register – 0x00F1 0000
CY7C964 Mask Register – 0x00F1 4000

VMEbus Address Region – VME_base+0x00F0 0000 : 0x00F1 FFFF

One VIC64 and and three CY7C964s comprise the VMEbus interface section of the Model 4290/4291. The VME address and data busses are segmented into 8–bit groups, each handled by one of these devices. The VIC64 handles the eight LSBs of each bus, i. e., VMEbus address bits VA0 : VA7, which it translates into the 4290/4291's Global bus address bits GA0 : GA7, and VMEbus data bits VD0 : VD7, which it translates into Global bus data bits GD0 : GD7. One of the three CY7C964s performs the identical translations between VME signals VA8 : VA15 and VD8 : VD15, and 4290/4291's Global bus signals GA8 : GA15 and GD8 : GD16. The other two CY7C964s each translate 8 of the the upper 16 bits of the VME address and data busses to the 4290/4291's Global bus.

The internal register sets of these devices are accessible to the 'C6x processors in this memory window, and to Global bus masters in the Global memory space from 0x00F0 0000 : 0x00F1 FFFF (VMEbus address range VME_base+0x00F0 0000 : VME_base+ 0x00F1 FFFF). A subset of the VIC64 register set is also accessible from the VMEbus in A16 slave space, in the region from A16_base+0x0000 to A16_base+0x003F. These will be discussed further in Section 5.2 and Table 5–4 of this manual. For complete information about these devices, please refer to Cypress Semiconductor's ***VMEbus Interface Handbook***.

The CY7C964s each contain a programmable comparator used to determine when VME is trying to access the 4290/91. These comparators are controlled by two internal, write–only registers: a mask register and a compare register. The mask register enables or disables specific bits for the comparator, and the compare register stores the data pattern (i. e., the local address) that inputs are compared against. The comparator's match output signal is driven by the CY7C964 when the bit pattern on its address pins match the enabled bits in the compare register. Clearing mask register bits to logic '0' enables the corresponding bits of the compare register. Setting bits of the mask register to logic '1' disables those bits in the compare register, effectively placing them in a don't care or "match anything" state.

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.6 'C6x Access to the VME Interface Configuration Registers (continued)

Loading the mask register with all 0's forces the compare register to match all bits of the pattern on it's address pins. Setting all mask register bits to 1's effectively disables the on−board comparator, i. e., the match output will always be asserted. The 3 CY7C964 mask registers are loaded simultaneously by writing the desired bit pattern to the upper 24 bits (D31 : D8) at 4290/91 Global bus address 0x00F1 4000. The 'C6x processors access that address by setting the page register to 0x0070, and accessing the V−bus address 0x0011 4000. Similarly, the 3 compare registers are loaded simultaneously by writing the desired bit pattern to the upper 24 bits (D31 : D8) at 4290/91 Global bus address 0x00F1 000. The 'C6x processors access that address by setting the page register to 0x0070, and accessing the V−bus address 0x0011 000. The function of these registers is essentially transparent to the user. They are initialized with the board's VME_base address at boot time, and constantly compare the VME address bus to the board's base address, to determine whether or not this board should participate in the current VMEbus transaction.

The VIC64 handles the greate majority of the VMEbus interface chores for the 'C6x processors on the Model 4290/4291. The VIC64's configuration registers are accessed by the DSPs in the 2 MByte region of Global bus memory beginning at address 0x00F0 0000. Refer to the excerpts from the VIC64 User's Guide, in Appendix A of this manual, for details about these registers and how they affect the execution of VMEbus transactions. Table 4−9, on the next page, lists the registers in the VIC, their addresses, and the values to which the 4290/4291's boot firmware initializes them. Note that all of the registers in the VIC are mapped on four−byte address boundaries, which simplifies access from 32−bit devices such as the 'C6xs.

A few of these registers are also accessible in VMEbus A16 space. The address range is from A16_base+0x0000 to A16_base+0x003F. See Table 5−4, on page 121, for a complete listing of the VIC64 registers that can be accessed from the VMEbus.

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Table 4-9: Model 4290/4291 –VIC64 Register Map with Values After Firmware Loading			
'C6x Address	**Register**	**Description**	**Firmware Loaded Value**
0x00F0 0000	VIICR	VMEbus Interrupter Interrupt Control Register	1111 1000
0x00F0 0004	VICR1	VMEbus Interrupt Control Register 1	1111 1000
0x00F0 0008	VICR2	VMEbus Interrupt Control Register 2	1111 1000
0x00F0 000C	VICR3	VMEbus Interrupt Control Register 3	1111 1000
0x00F0 0010	VICR4	VMEbus Interrupt Control Register 4	1111 1000
0x00F0 0014	VICR5	VMEbus Interrupt Control Register 5	1111 1000
0x00F0 0018	VICR6	VMEbus Interrupt Control Register 6	1111 1000
0x00F0 001C	VICR7	VMEbus Interrupt Control Register 7	1111 1000
0x00F0 0020	DMASICR	DMA Status Interrupt Control Register	1111 1000
0x00F0 0024	LICR1	Local Interrupt Control Register 1	1000 1000
0x00F0 0028	LICR2	Local Interrupt Control Register 2	1000 1000
0x00F0 002C	LICR3	Local Interrupt Control Register 3	1000 1000
0x00F0 0030	LICR4	Local Interrupt Control Register 4	1000 1000
0x00F0 0034	LICR5	Local Interrupt Control Register 5	1000 1000
0x00F0 0038	LICR6	Local Interrupt Control Register 6	1000 1000
0x00F0 003C	LICR7	Local Interrupt Control Register 7	1000 1000
0x00F0 0040	ICGSICR	ICGS Interrupt Control Register	1111 1000
0x00F0 0044	ICMSICR	ICMS Interrupt Control Register	1110 1001
0x00F0 0048	EGICR	Error Group Interrupt Control Register	1111 1000
0x00F0 004C	ICGSIVBR	ICGS Interrupt Vector Base Register	1111 1000
0x00F0 0050	ICMSIVBR	ICMS Interrupt Vector Base Register	1111 1000
0x00F0 0054	LIVBR	Local interrupt Vector Base Register	1111 1000
0x00F0 0058	EGIVBR	Error Group Interrupt Vector Base Register	1111 1000
0x00F0 005C	ICSR	Interprocessor Communications Switch Register	0000 0000
0x00F0 0060	ICR0	Interprocessor Communications Register 0	0000 0000
0x00F0 0064	ICR1	Interprocessor Communications Register 1	0010 0010
0x00F0 0068	ICR2	Interprocessor Communications Register 2	0000 0000
0x00F0 006C	ICR3	Interprocessor Communications Register 3	0100 0100
0x00F0 0070	ICR4	Interprocessor Communications Register 4	0000 0000
0x00F0 0074	ICR5	Interprocessor Communications Register 5	0000 0010
0x00F0 0078	ICR6	Interprocessor Communications Register 6	0111 1110
0x00F0 007C	ICR7	Interprocessor Communications Register 7	0000 0000
0x00F0 0080	VIRSR	VMEbus Interrupt Request Status Register	0000 0000
0x00F0 0084	VIVBR1	VMEbus Interrupt Vector Base Register 1	0000 0001
0x00F0 0088	VIVBR2	VMEbus Interrupt Vector Base Register 2	0000 0010
0x00F0 008C	VIVBR3	VMEbus Interrupt Vector Base Register 3	0000 0011
0x00F0 0090	VIVBR4	VMEbus Interrupt Vector Base Register 4	0000 0100
0x00F0 0094	VIVBR5	VMEbus Interrupt Vector Base Register 5	0000 0101
0x00F0 0098	VIVBR6	VMEbus Interrupt Vector Base Register 6	0000 0110
0x00F0 009C	VIVBR7	VMEbus Interrupt Vector Base Register 7	0000 0111
0x00F0 00A0	TTR	Transfer Timeout Register	0110 1000
0x00F0 00A4	LBTR	Local Bus Timing Register	0100 0100
0x00F0 00A8	BTDR	Block Transfer Definition Register	0110 1100
0x00F0 00AC	ICR	Interface Configuration Register	0100 0011
0x00F0 00B0	ARCR	Arbiter/Requester Configuration Register	0110 0000
0x00F0 00B4	AMSR	Address Modifier Source Register	0000 0000
0x00F0 00B8	BESR	Bus Error Status Register	0000 0000
0x00F0 00BC	DMASR	DMA Status Register	0000 0000
0x00F0 00C0	SS0CR0	Slave Select 0 Control Register 0	0001 0010
0x00F0 00C4	SS0CR1	Slave Select 0 Control Register 1	0100 0100
0x00F0 00C8	SS1CR0	Slave Select 1 Control Register 0	0101 0100
0x00F0 00CA	SS1CR1	Slave Select 1 Control Register 1	0100 0100
0x00F0 00D0	RCR	Release Control Register	0100 0000
0x00F0 00D4	BTCR	Block Transfer Control Register	0001 0000
0x00F0 00D8	BTLR1	Block Transfer Length Register 1	0000 0000
0x00F0 00DC	BTLR0	Block Transfer Length Register 0	0000 0000
0x00F0 00E0	SRR	System Reset Register	1111 1111
0x00F0 00E4	BTLR2	Block Transfer Length Register 2	0000 0000
NOTE: See the VIC64 information in Appendix A of this manual for an explanation of reset codes.			

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.7 'C6x Master Access to the Global Expansion Bus Daughterboard

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0080
Base Offset – 0x0000 0000

Global Bus Address Region – 0x0100 0000 : 0x0103 FFFF
VMEbus Address Region – VME_base+0x0100 0000 : 0x0103 FFFF

'C6x processors on the Model 4290/4291 can access a daughterboard installed on the Global Expansion Bus as a slave device, by conducting read and write operations to the Global memory window with the Page Register set for 0x0000 0080. This region corresponds to the Global bus memory space from 0x0100 0000 to 0x0103 FFFF.

4.2.8 'C6x Master Access to VMEbus A16 Space

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0100 : 0x0000 0170
Base Offset – 0x0000 0000

Global Bus Address Region – 0x0200 0000 : 0x0200 FFFF

'C6x processors on the Model 4290/4291 can master transactions in VMEbus A16 space by conducting read and write operations in its Global bus memory window, with the page register set within the range 0x0000 0100 : 0x0000 0170. This corresponds to the Global bus memory window extending from 0x0200 0000 to 0x0200 FFFF. Because VMEbus A16 space is only 64 kBytes deep, this entire access region could have been contained within a single page of 'C6x memory, but to simplify the address decoding hardware, eight consecutive pages have been assigned.

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4.2 'C6x Access to Global Bus Resources (continued)

4.2.9 'C6x Master Access to VMEbus A24 Space

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0180 : 0x0000 01F0
Base Offset – 0x0000 0000

Global Bus Address Region – 0x0300 0000 : 0x03FF FFFF

'C6x processors on the Model 4290/4291 can master transactions in VMEbus A24 space by conducting read and write operations in its Global bus memory window, with the page register set to 0x0180. This corresponds to the Global bus memory window extending from 0x0300 0000 to 0x03FF FFFF. The VME–bus A24 access region is 16 MBytes deep, and therefore uses 8 pages of 'C6x memory. To cross page boundaries in this memory region, increment the Page Register setting (i. e., valid Page Register settings for VMEbus A24 space master access are from 0x0000 0180 to 0x0000 001F0, inclusive).

4.2.10 'C6x Master Access to VMEbus A32 Space

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 8000 : 0x0000 FFF0
Base Offset – 0x0000 0000

Global Bus Address Region – 0x1 0000 0000 : 0x1 FFFF FFFF

'C6x processors on the Model 4290/4291 can master transactions in VMEbus A32 space by conducting read and write operations in this memory window. This corresponds to the Global bus memory window extending from 0x1 0000 0000 to 0x1 FFFF FFFF. The VMEbus A32 access region is 4 GBytes deep, and therefore uses 2048 pages of 'C6x memory. To cross page bound–aries in this memory region, increment the Page Register setting (i. e., valid Page Register settings for VMEbus A32 space master access are from 0x0000 8000 to 0x0000 FFF0, inclusive).

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4.3 'C6x Access to Local Bus (V–bus) Resources

The sections that follow cover the resources available to a 'C6x processors on the Model 4290/4291, on its local bus, also known as the V–bus.

4.3.1 'C6x Access to the Local Side of the Dual Port SRAMs & Mailboxes

'C6x Address Region – 0x0020 0000 : 0x0027 FFFF

Chapter 7 of this manual provides a complete discussion of the Dual Port SRAMs on the Model 4290/4291, and covers all the details about how these SRAM banks and mailboxes are accessed from both the Local (V–bus) and Global bus sides. The topic of V–bus access to the Dual Port SRAMs is covered in Section 7.2. In this chapter, we will simply present the memory map used by the 'C6x processors to access these resources from the V–bus, in Table 4–10, below. For more detailed information, please refer to Section 7.2 and its subsections.

Table 4–10: Model 4290/4291 –Memory Map for Local (V-bus) Side of Dual Port SRAM

Resource	Access	Option 244	Option 240
DPSRAM, bank 0, Local Port	R/W	0x0020 0000 : 0x0020 3FFF	0x0020 0000 : 0x0020 1FFF
DPSRAM, bank 1, Local Port		0x0020 4000 : 0x0020 7FFF	0x0020 2000 : 0x0020 3FFF
DPSRAM, bank 2, Local Port		0x0020 8000 : 0x0020 BFFF	0x0020 4000 : 0x0020 5FFF
DPSRAM, bank 3, Local Port		0x0020 C000 : 0x0020 FFFF	0x0020 6000 : 0x0020 7FFF
Reserved	—	0x0021 0000 : 0x0023 FFFF	0x0020 8000 : 0x0023 FFFF
Reserved		0x0024 0000 : 0x0024 007F	
V-bus → Global Port A DPSRAM Mailbox	R/W	0x0024 0080	
V-bus → Global Port C DPSRAM Mailbox		0x0024 0084	
V-bus → Global Port D DPSRAM Mailbox		0x0024 0088	
V-bus → Global Port B DPSRAM Mailbox		0x0024 008C	
Global Port A → V-bus DPSRAM Mailbox	R. O.	0x0024 0090	
Global Port C → V-bus DPSRAM Mailbox		0x0024 0094	
Global Port D → V-bus DPSRAM Mailbox		0x0024 0098	
Global Port B → V-bus DPSRAM Mailbox		0x0024 009C	
Local DP Interrupt Control/Status Register	R/W	0x0024 00A0	
Reserved	—	0x0024 00A4 : 0x0027 FFFF	
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.			

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers

'C6x Address Region – 0x0028 0000 : 0x002B FFFF

There are 21 registers available in this memory region, which are used to control various operating parameters for each DSP. These include Interrupt Enable, Flag and Status registers, the Global Bus Page Register, a Semaphore Register, a Configuration Register and another register with a collection of miscellaneous control bits. Table 4–11, below, lists these registers and their addresses. Information about each register can be found in the subsections that begin on the next page, and more detail may be found in other appro–priate areas of this manual, as indicated in the left–hand column of the table.

Table 4–11: Model 4290/4291 –Processor Node V-bus (Local bus) Control Register Memory Map

'C6x Address	Mnemonic	Resource	Access	Add'l Info
0x0028 0000	IER0	Interrupt Enable Register 0 (XX Port)	R/W	Secs. 4.3.2.1 & 6.4.3
0x0028 0004	IER1	Interrupt Enable Register 1 (ZZ & VIM Ports)	R/W	
0x0028 0008	IFR0	Interrupt Flag Register 0 (XX Port)	R/C	Secs. 4.3.2.2 & 6.4.2
0x0028 000C	IFR1	Interrupt Flag Register 1 (ZZ & VIM Ports)	R/C	
0x0028 0010	ISR0	Interrupt Status Register 0 (XX Port)	R. O.	Secs. 4.3.2.3 & 6.4.1
0x0028 0014	ISR1	Interrupt Status Register 1 (ZZ & VIM Ports)	R. O.	
0x0028 0018	MIVR	Miscellaneous Interrupt & VME Control Register	R/W	Section 4.3.2.4
0x0028 001C	MCR0	Miscellaneous Control Register	R/W	Section 4.3.2.5
0x0028 0020	BCR	Board Configuration Register	R. O.	Section 4.3.2.6
0x0028 0024	GBPR	Global Bus Paging Register	R/W	Section 4.3.2.7
0x0028 0028	LSR	Local Semaphore Register	R/W	Secs. 4.3.2.8 & 7.2.1
0x0028 002C	N/A	Reserved	N/A	—
0x0028 0030*	IMR0*	Interrupt Mapping Register 0*	R/W	Section 4.3.2.9
0x0028 0034 - 0x0028 0038	N/A	Reserved	N/A	—
0x0028 003C*	BVR*	Board Version Register*	R. O.	Section 4.3.2.10
0x0028 0040 - 0x0028 00FC	N/A	Reserved	N/A	—
0x0028 0100	IGCR	VME Interrupt Gating Control Register	R/W	Section 4.3.2.11
0x0028 0104	VIPR	VME Interrupt Pending Register	R. O.	Section 4.3.2.12
0x0028 0108	IVR1	VME IPL1 Interrupt Vector Register	R. O.	Section 4.3.2.13
0x0028 010C	IVR2	VME IPL2 Interrupt Vector Register	R. O.	
0x0028 0110	IVR3	VME IPL3 Interrupt Vector Register	R. O.	
0x0028 0114	IVR4	VME IPL4 Interrupt Vector Register	R. O.	
0x0028 0118	IVR5	VME IPL5 Interrupt Vector Register	R. O.	
0x0028 011C	IVR6	VME IPL6 Interrupt Vector Register	R. O.	
0x0028 0120	IVR7	VME IPL7 Interrupt Vector Register	R. O.	
0x0028 0124	VIER	VME Interrupt Enable Register	R/W	Section 4.3.2.14

*** - These registers are only available on the Model 4290/4291 Option 330 - on all other units, these addresses are Reserved.**

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.1 Interrupt Enable Registers (Read/Write)

'C6x Addresses:
IER0 (XX port) – 0x0028 0000
IER1 (ZZ & VIM ports)– 0x0028 0004

These registers contain enable bits for the interrupt sources associated with the two inter–processor communication Bi–FIFOs. Each processor has a unique version of each of these registers, one for the XX or upstream Bi–FIFO (IER0, at 'C6x address 0x0028 0000), and the other for the ZZ or downstream Bi–FIFO and the VIM Bi–FIFO (IER1, at address 0x0028 0004). Any specific processor can only access its own pair of these registers. Table 4–12, below, shows the contents of IER0. Table 4–13, at the bottom of this page, shows the contents of IER1. The topic of Bi–FIFO related interrupts on the Model 4290/4291 is covered in detail in Section 6.4, which starts on page 160 of this manual. For a complete description of this register and how the bits therein are used, please refer to Section 6.4.3, beginning on page 169.

Table 4–12: Model 4290/4291 –Interrupt Enable Register for Upstream Inter–Processor (XX) Bi–FIFO (IER0) –R/W @ 0x0028 0000

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	XX_Incoming _Mailbox	XX_Outgoing _Mailbox	XX_Outgoing _Almost Full	XX_Outgoing _Almost Empty	XX_Outgoing _Empty	XX_Incoming _Almost Full	XX_Incoming _Almost Empty	XX_Incoming _Empty
Function	1 = Enable Interrupt, 0 = Disable Interrupt							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved							
Function	Write with "0"'s, Mask when Reading							
NOTE: All bits are cleared to the logic '0' state at boot and by resets.								

Table 4–13: Model 4290/4291 –Interrupt Enable Register for Downstream Inter–Processor (ZZ) and VIM Bi–FIFOs (IER1) –R/W @ 0x0028 0004

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	ZZ_Incoming _Mailbox	ZZ_Outgoing _Mailbox	ZZ_Outgoing _Almost Full	ZZ_Outgoing _Almost Empty	ZZ_Outgoing _Empty	ZZ_Incoming _Almost Full	ZZ_Incoming _Almost Empty	ZZ_Incoming _Empty
Function	1 = Enable Interrupt, 0 = Disable Interrupt							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VIM_Incoming _Mailbox	VIM_Outgoing _Mailbox	VIM_Outgoing _Almost Full	VIM_Outgoing _Almost Empty	VIM_Outgoing _Empty	VIM_Incoming _Almost Full	VIM_Incoming _Almost Empty	VIM_Incoming _Empty
Function	1 = Enable Interrupt, 0 = Disable Interrupt							
NOTE: All bits are cleared to the logic '0' state at boot and by resets.								

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.2 Interrupt Flag Registers (Read/Clear)

'C6x Addresses:
IFR0 (XX port) – 0x0028 0008
IFR1 (ZZ & VIM ports)– 0x0028 000C

These registers latch the assertion of the flag outputs for their associ–ated Bi–FIFOs. Each processor has a unique version of each of these registers, one for the XX or upstream Bi–FIFO (IFR0, at 'C6x address 0x0028 0008), and the other for the ZZ or downstream Bi–FIFO and the VIM Bi–FIFO (IFR1, at address 0x0028 000C). Any specific pro–cessor can only access its own pair of these registers. Because the states of the Bi–FIFO flags are intrinsically transient, these registers provide a place that retains the information that a particular state was reached, which may be examined during an interrupt service routine. Table 4–14, below, shows the contents of IFR0. Table 4–15, at the bottom of this page, shows the contents of IFR1. The topic of Bi–FIFO related interrupts on the Model 4290/4291 is covered in detail in Section 6.4, which starts on page 160 of this manual. For a complete description of this register and how the bits therein are used, please refer to Section 6.4.2, beginning on page 165.

Table 4-14: Model 4290/4291 - Interrupt Flag Register for Upstream Inter-Processor (XX) Bi-FIFO (IFR0) - R/C @ 0x0028 0008

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	XX_Incoming _Mailbox	XX_Outgoing _Mailbox	XX_Outgoing _Almost Full	XX_Outgoing _Almost Empty	XX_Outgoing _Empty	XX_Incoming _Almost Full	XX_Incoming _Almost Empty	XX_Incoming _Empty
Function	Read Operation: 1 = Flag has been asserted, 0 = Flag has not been asserted Write Operation: 1 = Clear a set bit that has been set, 0 = No action.							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved							
Function	Write with "0"'s, Mask when Reading							

NOTE: The reset state of this register is indeterminate. Before using this register, it must be cleared, by writing 0xFF00 to it.

Table 4-15: Model 4290/4291 - Interrupt Flag Register for Downstream Inter-Processor (ZZ) and VIM Bi-FIFOs (IFR1) - R/C @ 0x0028 000C

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	ZZ_Incoming _Mailbox	ZZ_Outgoing _Mailbox	ZZ_Outgoing _Almost Full	ZZ_Outgoing _Almost Empty	ZZ_Outgoing _Empty	ZZ_Incoming _Almost Full	ZZ_Incoming _Almost Empty	ZZ_Incoming _Empty
Function	Read Operation: 1 = Flag has been asserted, 0 = Flag has not been asserted Write Operation: 1 = Clear a set bit that has been set, 0 = No action.							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VIM_Incoming _Mailbox	VIM_Outgoing _Mailbox	VIM_Outgoing _Almost Full	VIM_Outgoing _Almost Empty	VIM_Outgoing _Empty	VIM_Incoming _Almost Full	VIM_Incoming _Almost Empty	VIM_Incoming _Empty
Function	Read Operation: 1 = Flag has been asserted, 0 = Flag has not been asserted Write Operation: 1 = Clear a set bit that has been set, 0 = No action.							

NOTE: The reset state of this register is indeterminate. Before using this register, it must be cleared, by writing 0xFFFF to it.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.3 Interrupt Status Registers (Read Only)

'C6x Addresses:
ISR0 (XX port) – 0x0028 0010
ISR1 (ZZ & VIM ports)– 0x0028 0014

These registers mirror the current, real–time states of the flag outputs for their associated Bi–FIFOs. Each processor has a unique version of each of these registers, one for the XX or upstream Bi–FIFO (ISR0, at 'C6x address 0x0028 0010), and the other for the ZZ or downstream Bi–FIFO and the VIM Bi–FIFO (ISR1, at address 0x0028 0014). Any specific processor can only access its own pair of these registers. Table 4–16, below, shows the contents of ISR0. Table 4–17, at the bottom of this page, shows the contents of ISR1. The topic of Bi–FIFO related interrupts on the Model 4290/4291 is covered in detail in Section 6.4, which starts on page 160 of this manual. For a complete description of this register and what the bits therein mean when read, please refer to Section 6.4.1, beginning on page 161.

Table 4–16: Model 4290/4291 –Interrupt Status Register for Upstream Inter–Processor (XX) Bi–FIFO (ISR0) –R. O. @ 0x0028 0010

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	XX_Incoming _Mailbox	XX_Outgoing _Mailbox	XX_Outgoing _Almost Full	XX_Outgoing _Almost Empty	XX_Outgoing _Empty	XX_Incoming _Almost Full	XX_Incoming _Almost Empty	XX_Incoming _Empty
Function	1 = Flag is Asserted, 0 = Flag is NOT Asserted							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved							
Function	Write with "0"'s, Mask when Reading							

NOTE: After a boot or reset, the Almost Empty and Empty bits will be true, and all other bits will be false Thus, the reset state of this register is 0001 1011 XXXX XXXX (in binary) or 0x0000 1Bxx (hex)

Table 4–17: Model 4290/4291 –Interrupt Status Register for Downstream Inter–Processor (ZZ) and VIM Bi–FIFOs (ISR1) –R. O. @ 0x0028 0014

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	ZZ_Incoming _Mailbox	ZZ_Outgoing _Mailbox	ZZ_Outgoing _Almost Full	ZZ_Outgoing _Almost Empty	ZZ_Outgoing _Empty	ZZ_Incoming _Almost Full	ZZ_Incoming _Almost Empty	ZZ_Incoming _Empty
Function	1 = Flag is Asserted, 0 = Flag is NOT Asserted							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VIM_Incoming _Mailbox	VIM_Outgoing _Mailbox	VIM_Outgoing _Almost Full	VIM_Outgoing _Almost Empty	VIM_Outgoing _Empty	VIM_Incoming _Almost Full	VIM_Incoming _Almost Empty	VIM_Incoming _Empty
Function	1 = Flag is Asserted, 0 = Flag is NOT Asserted							

NOTE: After a boot or reset, the Almost Empty and Empty bits will be true, and all other bits will be false Thus, the reset state of this register 0001 1011 0001 1011 (in binary) or 0x0000 1B1B (hex)

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.4 Miscellaneous Interrupt & VMEbus Control Register (MIVR) – R/W

'C6x Address – 0x0028 0018

This register contains the interrupt control bits for those interrupt sources that are associated with sources other than the three Bi–FIFOs for each processor node. These interrupt sources include the Dual Port SRAM Mailboxes, the VIM module interrupt, and the global expansion daughterboard interrupt. The register also includes bits that the 'C6x processor needs when mastering Global bus and VMEbus transactions, including data size bits and a bus lock bit. Each processor is presented with a unique version of this register at V–bus address 0x0028 0018. Any given processor can only access its own copy of this register. Table 4–18, below, shows the arrangement of bits in the Miscellaneous Interrupt & VME Control Bus Register. The paragraphs beginning at the top of the next page describe how these bits are used.

Table 4–18: Model 4290/4291 –Miscellaneous Interrupt & VME Control Register (MIVR) –R/W @ 0x0028 0018

Bit #	D15	D14	D13*	D12	D11†	D10*	D9	D08†
Bit Name	Reserved		Reset_ Status*	DP_MB_Int _Enable	DP_MB_Int _Flag†	DP_MB_Int _Status*	VIM_Int _Enable	VIM_Int _Flag†
Bit Function	Write with Zeros Mask on Reads		0 = Power 1 = VME / FP	1 = Enable 0 = Disable	1 = Latched 0 = Not Latched	1 = Asserted 0 = Not Asserted	1 = Enable 0 = Disable	1 = Latched 0 = Not Latched
Bit #	**D7***	**D6**	**D5†**	**D4***	**D3**	**D2**	**D1**	**D0**
Bit Name	VIM_Int _Status*	Gbus_DB_Int _Enable	Gbus_DB_Int _Flag†	Gbus_DB_Int _Status*	VME_ Size_1	VME_ Size_0	Gbus/VME Lock	VME Word
Bit Functio	1 = Asserted 0 = Not Asserted	1 = Enable 0 = Disable	1 = Latched 0 = Not Latched	1 = Asserted 0 = Not Asserted	1,1 = N/U 1,0 = Word	0,1 = Byte 0,0 = LW	1 = Lock 0 = Unlock	1 = D16 / D8 0 = D32

*** –These bits are Read Only † - These bits are Read/Clear - after reading a '1', write a '1' to clear**
The binary reset value of this register is XXR1 0000 0000 0001, where X is indeterminate, and R is dependent upon how the board was reset.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.4 Miscellaneous Interrupt & VMEbus Control Register (continued)

- Reset Status Bit (R. O.) – D13 @ MIVR (0x0028 0018)

  The state of this read–only bit tells the user how the board was last reset. If the last reset occurred when power was applied, (i. e., due to a "cold" start) this bit will read back in the logic '0' state. If the node in question was last reset from the VME DSP Reset Control Register (see Section 4.2.5.3), or if the board was last reset by a VME System Reset or by the front panel **RST** pushbutton (i. e., due to a "warm" start), this bit will read back in the logic '1' state. Writes to this bit have no effect.

- Dual Port SRAM Mailbox Interrupt Enable Bit (R/W) – D12 @ MIVR (0x0028 0018)

  Set this bit to the logic '1' state, to allow a DSP to be interrupted when data has been placed in its Dual Port SRAM Mailbox. To prevent such interrupts, clear the associated bit to the logic '0' state. The Model 4290/4291's boot firmware sets this bit during initialization, i. e., this interrupt is enabled by default. On a standard Model 4290/4291, this interrupt is asserted on the EXT_INT6 input of the 'C6x processors. For a Model 4290/4291 Option 330, please refer to Section 4.3.2.9, which describes Interrupt Mapping Register 0.

- Dual Port SRAM Mailbox Flag Latch Bit (R/C) – D11 @ MIVR (0x0028 0018)

  This bit will read back in the logic '1' state after data has been placed in the node's Dual Port SRAM mailbox. After reading the mailbox data, this latched flag bit may be cleared by writing a '1' to it.

- Dual Port SRAM Mailbox Status Bit (R. O.) – D10 @ MIVR (0x0028 0018)

  When this bit reads back in the logic '1' state, it indicates that the node's Dual Port SRAM mailbox flag is set, i. e., that new data is currently in the mailbox. A logic '0' in this bit indicates that no new DPSRAM mailbox data is available. Writes to this bit have no effect.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.4 Miscellaneous Interrupt & VMEbus Control Register (continued)

- VIM Module Interrupt Enable Bit (R/W) – D9 @ MIVR (0x0028 0018)

  Set this bit to the logic '1' state, to allow a DSP to be interrupted by the VIM Daughterboard Interrupt signal ($\overline{\text{NxDBINT}}$). Refer to the VIM module's Operating Manual for information on how a specific module generates this signal. To prevent such interrupts, clear this bit to the logic '0' state. On a standard Model 4290/4291, this interrupt is asserted on the EXT_INT7 input of the 'C6x processors. For a Model 4290/4291 Option 330, please refer to Section 4.3.2.9, which describes Interrupt Mapping Register 0.

- VIM Module Interrupt Latch Bit (R/C) – D8 @ MIVR (0x0028 0018)

  This bit will read back in the logic '1' state after a VIM Daughterboard Interrupt signal ($\overline{\text{NxDBINT}}$) has been generated. Refer to the VIM module's Operating Manual for information on how a specific module generates this signal. After servicing the interrupt, this latched flag bit may be cleared by writing a '1' to it.

- VIM Module Interrupt Status Bit (R. O.) – D7 @ MIVR (0x0028 0018)

  When this bit reads back in the logic '1' state, it indicates that the VIM Daughterboard Interrupt signal ($\overline{\text{NxDBINT}}$) is currently asserted. A logic '0' in this bit indicates that the VIM $\overline{\text{NxDBINT}}$ signal is not asserted. Writes to this bit have no effect.

- Global Bus Daughterboard Interrupt Enable Bit (R/W) – D6 @ MIVR (0x0028 0018)

  Set this bit to the logic '1' state, to allow a DSP to be interrupted by the Global Bus Daughterboard Interrupt signal ($\overline{\text{GDB_INT}}$). Refer to the Global Bus Daughterboard's operating instructions for information on how this signal is generated. To prevent such interrupts, clear this bit to the logic '0' state. On a standard Model 4290/4291, this interrupt is asserted on the EXT_INT7 input of the 'C6x processors. For a Model 4290/4291 Option 330, please refer to Section 4.3.2.9, which describes Interrupt Mapping Register 0.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.4 Miscellaneous Interrupt & VMEbus Control Register (continued)

- Global Bus Daughterboard Interrupt Latch Bit (R/C) – D5 @ MIVR (0x0028 0018)

  This bit will read back in the logic '1' state after a Global Bus Daughterboard Interrupt signal ($\overline{\text{GDB_INT}}$) has been generated. Refer to the Global Bus Daughterboard's operating instructions for information on how this signal is generated. After servicing the interrupt, this latched flag bit may be cleared by writing a '1' to it.

- Global Bus Daughterboard Interrupt Status Bit (R. O.) – D4 @ MIVR (0x0028 0018)

  When this bit reads back in the logic '1' state, it indicates that the Global Bus Daughterboard Interrupt signal ($\overline{\text{GDB_INT}}$) is currently asserted. A logic '0' in this bit indicates that the $\overline{\text{GDB_INT}}$ signal is not asserted. Writes to this bit have no effect.

- VME Size Bits (R/W) – D3 : D2 @ MIVR (0x0028 0018)

  When a 'C6x processor on the Model 4290/4291 needs to master the VMEbus, using the services of the VIC64, these two bits are used to tell the VIC about the size of the data element(s) to be transferred. Table 4–19, below, describes the settings of this bit field.

Table 4–19: Model 4290/4291 –VME_Size Bits D3 & D2 @ MIVR (0x0028 0018)

D3	D2	Data Element	# of bits / transfer
0	0	Long Word	32
0	1	Byte	8
1	0	Word	16
1	1	Not Used	

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.4 Miscellaneous Interrupt & VMEbus Control Register (continued)

- Global bus / VMEbus Lock Bit – D1 @ MIVR (0x0028 0018)

  This bit is used when a 'C6x processor on the Model 4290/4291 needs to master the on–board Global bus, or the VMEbus, for an atomic sequence of operations (during which no other master may be granted access to that bus, e. g., read–modify–write). After being granted mastership of the bus in question, and performing an access to that bus, the DSP may set this bit to the logic '1' state to "lock" the bus. The arbiter will not grant the bus to any other potential master for as long as this bit remains set. When the atomic access has been completed, this bit should be cleared to the logic '0' state to release the bus lock and allow access by other masters.

- VME Word Bit – D1 @ MIVR (0x0028 0018)

  This bit is directly connected to the $\overline{\text{WORD}}$ pin on the VIC64. When this bit is cleared to the logic '0' state, the VIC will drive the VMEbus with appropriate signals for D32 transfers. When this bit is set to the logic '1' state, the VIC will drive the VME–bus with appropriate signals for D16 or D8 transactions, depending upon the states of the VME Size bits, D3 and D2 in this register (see Table 4–19, previous page).

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.5 Miscellaneous Control Register (MCR0) – R/W

'C6x Address – 0x0028 001C

Each of the 'C6x processors on the Model 4290/4291 has a unique copy of this register, which contains control bits associated with non–interrupt related functions of the Bi–FIFOs and the front panel LED indicators associated with each processor node. The Bi–FIFO select bits determine which of the three bi–directional FIFO paths are selected when accessing the node's BI–FIFO memory space on a standard (i. e., non–Option 330) Model 4290/4291. These select bits apply when accessing either one of the Bi–FIFOs or the Bi–FIFO mailboxes. The Bi–FIFO reset bits allow for the individual reset of any or all of the three Bi–FIFOs within a given node. Note that only the processor connected to the A side of an inter–processor Bi–FIFO can reset that FIFO. For the VIM Bi–FIFOs, each processor can reset its own FIFO. Bits used to illuminate the front panel LEDs are also included in these registers. The bitwise layout of the Miscellaneous Control Register is shown in Table 4–20, below. The paragraphs that begin at the top of the page after next describe how these bits are used.

Table 4–20: Model 4290/4291 –Miscellaneous Control Register 0 (MCR0) –R/W @ 0x0028 001C

Bit #	D15*	D14*	D13	D12	D11	D10	D9	D8
Bit Name	Bi-FIFO_ Select_1*	Bi-FIFO_ Select_0*	Reserved	Bi-FIFO_ZZ _Reset	Bi-FIFO_XX _Reset	VIM_Bi-FIFO _Reset	Reserved	
Bit Function	1,1 = VIM 1,0 = VIM	0,1 = I-P XX 0,0 = I-P ZZ	Write '0', Mask on Reads	1 = Reset & Hold 0 = Release & Operate			Write with '0's Mask on Reads	
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved				LED 3	LED 2	LED 1	LED 0
Bit Function	Write with Zeroes, Mask when Reading				1 = LED is ON (Lit) 0 = LED is OFF (Not Lit)			

*** –These bits are Reserved on the Model 4290/4291 Option 330**
All bits in this register are cleared to the logic '0' state on reset and boot.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.5 Miscellaneous Control Register (continued)

- Bi–FIFO Select Bits (R/W) – D15 : D14 @ MCR0 (0x0028 001C)

On the standard Model 4290/4291 (i. e., non–Option 330), access to all three of the Bi–directional FIFOs connected to each processor's V–bus is provided in the same address range, from 0x0100 0000 to 0x011F FFFF. Selection of a specific Bi–FIFO is accomplished using these two bits. Setting D15 in MCR0 to the logic '1' state selects the VIM Bi–FIFO, regardless of the state of D14. When D15 is cleared to the logic '0' state, then the state of D14 determines which of the inter–processor Bi–FIFOs is selected. When both bits are cleared, the upstream, or XX Bi–FIFO port is selected. When D14 is set to the logic '1' state (with D15 = 0), the downstream, or ZZ Bi–FIFO port is selected. Table 4–21, below, summarizes these settings.

Table 4–21: Standard Model 4290/4291 –Bi–FIFO Selection Bits –D15 & D14 @ MCR0, (0x0028 001C)

D15*	D14*	Bi-FIFO Selected	Path Enabled*
0	0	XX (Upstream) Port	A -> C or C -> D or D -> B or B -> A
0	1	ZZ (Downstream) Port	A -> B or B -> D or D -> C or C -> A
1	0	VIM	Any Processor to its own VIM Interface
1	1		



On the Model 4290/4291 Option 330, each of the three V–bus Bi–FIFOs is mapped into a unique address region in CE3 space. Thus, on Option 330 boards, these two bits are Reserved.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.5 Miscellaneous Control Register (continued)

❑ Bi–FIFO Reset Bits (R/W) – D12 : D10 @ MCR0 (0x0028 001C)

Each of these three bits is used to reset one of the all three Bi–directional FIFOs connected to each processor's V–bus. When a Bi–FIFO is reset, it is cleared of all data, its Empty and Almost Empty flags are asserted, and all other flags are rescinded (false). Bit D12 is used to reset the ZZ or Downstream inter–processor Bi–FIFO, D11 resets the XX or Upstream Bi–FIFO, and bit D10 operates on the VIM Bi–FIFO (see Figure 4–2, on page 108, for an illustration of the Bi–FIFO connection paths). To reset a Bi–FIFO, set the associated bit to the logic '1' state. The Bi–FIFO will be held in its reset state until the associated reset bit is cleared to the logic '0' state. Table 4–22, below, summarizes the operation of the Bi–FIFO Reset bits.

Table 4-22: Model 4290/4291 –Bi-FIFO Reset Bits –D12 : D10 @ MCR0, (0x0028 001C)

Bit #	Resets Bi-FIFO . . .	Function
D12	ZZ Bi-FIFO (Upstream)	1 = Reset & Hold 0 = Release & Operate
D11	XX Bi-FIFO (Downstream)	
D10	VIM Bi-FIFO	

❑ LED Bits (R/W) – D3 : D0 @ MCR0 (0x0028 001C)

Each of these four bits is used to light (by writing), or to check the status of (by reading) one of the four front panel LEDs asso–ciated with each processor. Each LED is associated with the bit in this register identified by the same number that is next the LED on the panel, i. e, bit D0 is associated with LED 0 (the red one), bit D1 with LED 1, D2 with LED 2 and D3 with LED 3. If one of these bits reads back in the logic '0' state, then the associ–ated LED is off (unlit). Setting that bit to the logic '1' state will light that LED (turn it on). If a bit reads back in the logic '1 ' state, then the associated LED is lit (on). To turn that LED off (unlight it), clear the associated bit to the logic '0' state.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.6 Board Configuration Register (BCR)

'C6x Address – 0x0028 0020

This register contains configuration and status bits that provide the processor with information regarding system configuration issues. These include the board's VME_base address, indicators bits for the presence of VIM and/or global bus daughterboards, the processor's ID number and the number of DSPs installeded on the 4290/4291 board. The entire register is Read Only and all the register's bit set–tings may be regarded as static. Each processor has a unique local copy of this register. Table 4–23, below, summarizes the contents of the register. The paragraphs that begin below the table describe their significance.

Table 4–23: Model 4290/4291 –Board Configuration Register (BCR) –R. O. @ 0x0028 0020

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	VME_Address _Jumper_AJ8 (A15 / A31)	VME_Address _Jumper_AJ7 (A14 / A30)	VME_Address _Jumper_AJ6 (A13 / A29)	VME_Address _Jumper_AJ5 (A12 / A28)	VME_Address _Jumper_AJ4 (A11 / A27)	VME_Address _Jumper_AJ3 A10 / A26)	VME_Address _Jumper_AJ2 (A9 / A25)	VME_Address _Jumper_AJ1 (A8 / A24)
Bit Function	1 = Jumper is NOT Installed (Address bit = 1) 0 = Jumper IS Installed (Address bit = 0)							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3***	**D2***	**D1***	**D0***
Bit Name	Bi-FIFO _Mode	Board_ Speed	VIM_Module _Installed	Global_Bus_ Daughterboard _Installed	Processor _ID_3*	Processor _ID_*	Processor _ID_1*	Processor _ID_0*
Bit Function	1 = Sync 0 = Async	1 = >100 MHz 0 = 100 MHz	1 = Installed 0 = Not Installed		1,1,1,1 = Proc. A 1,1,1,0 = Proc. C		1,1,0,0 = Proc. D 1,0,0,0 = Proc. B	

*** - The values shown for these bits ONLY apply for a Model 4290/4291 with four 'C6x processors installed. For dual or single processor configurations, please refer to Table 4-24, on the page after next.**

- VME Address Jumper Bits (R. O.) – D15 : D8 @ BCR (0x0028 0020)

  This 8–bit, read–only field reflects the states of the eight VMEbus base address jumpers, AJ8 : AJ1. D15 corresponds to AJ8, and D8 corresponds to AJ1. These jumpers establish the base address of the Model 4290/4291 in both A32 and A16 VMEbus address spaces (see Section 2.2.1, on page 31 of this manual). If a bit in this field reads back in the logic '0' state, the corresponding jumper is installed, and the corresponding VMEbus address bit must also be a '0' to match this board's address. If a bit in this field reads back in the logic '1' state, the corresponding jumper is not installed, and the corresponding VMEbus address bit must also be a '1' to match this board's address.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.6 Board Configuration Register (continued)

- Bi–FIFO Mode Bit (R. O.) – D7 @ BCR (0x0028 0020)

  This read–only bit tells the user whether the Bi–FIFOs installed on the Model 4290/4291 are of the Synchronous or Asynchronous variety, which in turn affects the way in which the firmware programs the EMIF for the Bi–FIFO memory space. The setting is made at the factory, and cannot be changed by the user. A logic '0' in this bit indicates that the Bi–FIFOs are Asynchronous, and a logic '1' indicates the presence of Synchronous Bi–FIFOs. At the time of this publi–cation, only 4290/4291's equipped with Option 330 feature Synchronous Bi–FIFOs (i. e., on Option 330 units ONLY, this bit should read back as a '1' – it will be a '0' for all other con–figurations).

- Board Speed Bit (R. O.) – D6 @ BCR (0x0028 0020)

  This read–only bit tells the user the clock rate of the 'C6x processors on the Model 4290/4291. If this bit reads back in the logic '0' state, the DSPs are clocked at 100 MHz. A '1' in this bit indicates that the DSPs are clocked at 167 MHz (for 'C6701's on a Model 4291), or 200 MHz (for 'C6201's on a Model 4290). In general, the lower clock rate units are pretty rare, as they were all manufactured and shipped before TI began shipment of production quantities of the full–speed rated devices (around June of 1998). Thus, this bit should almost always read back in the logic '1' state. Should it read back as a '0', you have a fairly old unit, which may be eligable for an upgrade.

- Daughterboard Installed Bits (R. O.) – D5 : D4 @ BCR (0x0028 0020)

  These read–only bits tells the user whether or not a daugh–terboard is installed on the associated interface. D5 is associ–ated withe the VIM interface, and D4 is associated with the Global bus daughterboard interface. For either bit, a '1' indi–cates that a daughterboard (or VIM module) is installed. If this bit reads back in the logic '0' state, then no daughter–board is installed on the associated interface for the processor in question.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.6 Board Configuration Register (continued)

- Processor ID Bits (R. O.) – D3 : D0 @ BCR (0x0028 0020)

This 4–bit read–only field holds the ID code for the DSP, and also indicates how many DSPs are installed on a given Model 4290/4291. By special order, the Model 4290/4291 has been available in single– (Options 010 and/or 014 – neither of which is available any longer) and dual– (Options 220 and 224) DSP configurations. The code that will be contained in these four bits is dependent upon both how many processors are installed, and which processor's BCR is being read. Table 4–24, below, describes the possible contents of this bit field, dependent upon the processor and board configura–tion. TheReadyFlow example program **`P4290GetProcId`** in the Model 4290/4291 Board Support Library package shows how a processor is identified by reading this bit field (refer to Section 2.3.1 in the Model 4290/4291 ReadyFlow manual, Pentek part # 801.42900).

Table 4–24: Model 4290/4291 –Processor ID Code to Processor Quantity & ID Mapping D3 : D0 @ BCR (0x0028 0020)

# Processors Installed	Processor A				Processor C				Processor D				Processor B			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
1	0	0	0	1	N/A				N/A				N/A			
2	0	0	1	1	0	0	1	0	N/A				N/A			
4	1	1	1	1	1	1	1	0	1	1	0	0	1	0	0	0

NOTE: The values listed above are the only valid combinations for this bit field. Any other value read in these bits should be regarded as an error condition, and usually indicates a serious problem with the Model 4290/4291 board. For example, if processor B reads any value other than 1000 in these bits, something is very wrong.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.7 Global Bus Page Register (GBPR)

'C6x Address – 0x0028 0024

Because the 'C6x's asynchronous memory window is only 4 MBytes deep, a paging scheme is used on the Model 4290/4291. This scheme allows the DSPs to address over 8 GBytes of memory, providing the address space necessary for the processors to address all of the on–board resources as well as the VMEbus. Additionally, since some resources (e. g., the V–bus registers under discussion here, the local side of the processor's Dual Port SRAM, and the Random Access VIM interface) need to be accessible at all times, this space is divided into two distinct regions, with Global resources occupying the lower 2 MByte region (where A21 = 0) and Local (V–bus) resources in the upper 2 MBytes (where A21 = 1). The window was divided in this manner to allow for a quick and simple decode.

A local 16–bit Page Register exists for each processor, at address 0x0028 0024 on its V–bus. The upper 12 and lower 2 bits of the register contain the page and byte address fields, respectively. Bits 2 and 3 are reserved. The page field is converted into a 32–bit value, and shifted left by 17 bits (such that D14 from the page register is aligned with address bit A31), and then is added to the processor's buffered address to form the 32–bit Global bus address. The most significant bit of the Page Register (bit D15) is set only for A32 VMEbus master accesses. If that bit is set to the logic '1' state, an A32 VMEbus master access will be performed, and the 11 remaining bits of the Page Register are combined with the Global bus address generated by the 'C6x as described above to form the VMEbus address that will be accessed. This allows the processor to have full access to the VMEbus A32 address space. The lower two bits of the Page Register (D1 & D0) specify the VME byte address.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.7 Global Bus Page Register (continued)

Given any absolute Global bus address, you can calculate the Page Register value by using the following formula:

Page_Reg_Value = (Address & 0xFFE0 0000) >> 17

For VMEbus master accesses, the offset can be calculated as follows:

Offset = (Address & 0x001F FFFF)

Additionally, when performing VMEbus A32 master accesses from a 'C6x, the most significant bit in the Page Register must be set, using:

Page_Reg_Value = ((Address & 0xFFE0 0000) >> 17) | 0x8000

Table 4–25, below, shows the contents of the Global Bus Page Register. The paragraphs that begin below the table describes the use of this register.

Table 4-25: Model 4290/4291 –Global Bus Page Register (GBPR) –R/W @ 0x0028 0024

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
Bit Name	VME_A32 _Master	Gbl_Page _Bit_31	Gbl_Page _Bit_30	Gbl_Page _Bit_29	Gbl_Page _Bit_28	Gbl_Page _Bit_27	Gbl_Page _Bit_26	Gbl_Page _Bit_25	Gbl_Page _Bit_24	Gbl_Page _Bit_23	Gbl_Page _Bit_22	Gbl_Page _Bit_21
Bit Function	1 = Enable 0 = Disable	Global Bus Page Select Field See Table 4-26 on page 99										

Bit #	D 3	D 2	D 1	D 0
Bit Name	Reserved		Global_Bus_Byte Select_1	Global_Bus_Byte Select_0
Bit Function	Write with Zeros Mask when Reading		1, 1 = Byte 3 1, 0 = Byte 2	0, 1 = Byte 1 0, 0 = Byte 0

All bits in this register are cleared to the logic '0' state by boot and reset operations, which points the Page Register to the Global Flash EEPROM

- ❑ VME A32 Master Enable Bit (R/W) – D15 @ GBPR (0x0028 0024)

  Set this bit to the logic '1' state when you need to perform any kind of master access to A32 VMEbus space. When this bit is set, the remaining bits in this register are used to allow the 'C6x processors access to the entire 4 GByte A32 VMEbus region. For any and all other master accesses (i. e., to any region other than A32 VMEbus space), clear this bit to the logic '0' state.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.7 Global Bus Page Register (continued)

❑ Global Bus Page Select Field (R/W) – D14 : D4 @ GBPR (0x0028 0024)

This 11–bit field must be initialized to the proper value by the processor before accessing any global bus resource. The con–tent of this field is converted to a 32–bit value, shifted left by 17 bits (such that D14 from the page register is aligned with address bit A31), and then added to the quantity on the processor's own address bus to form the address of the global bus resource to be accesesed. Table 4–26, below, gives the Page Register value required to access each resource available to the 4290/4291's 'C6x processors via the Global bus.

Table 4–26: Model 4290/4291 – Global Bus Page Select Field Settings (D14 : D4 @ 0x0028 0024)

Resource	Setting	# pages
Flash EEPROM	0x0000 000y : 0x0000 003y	4†
Global SRAM	0x0000 004y	1
Dual Port SRAM & Mailboxes	0x0000 005y	1
NVSRAM	0x0000 006y	1
Global, VIC & CY7C964 Registers	0x0000 007y	1
VMEbus A16 Master Access	0x0000 010y	1
VMEbus A24 Master Access	0x0000 018y	8†
***VMEbus A32 Master Access**	0x0000 800y	1024†

NOTES: y = (0:3) = setting of Byte Select field (see below)
† – For resources that occupy more than one page, this table lists the setting for the base page, i. e., the lowest–addressed page, for that resource.
*** – D15 is set to logic '1' for A32 VME master accesses, in addition to the Page Select settings that may be necessary**

❑ Global Bus Byte Select Field (R/W) – D1 : D0 @ GBPR (0x0028 0024)

When a DSP becomes master of the 4290/4291's Global bus, these two bits drive the two LSBs of the Global address bus, which are also connected to the LA1 : LA0 inputs of the VIC64. These signals, along with the $\overline{SIZ1}$, $\overline{SIZ0}$ and $\overline{WORD}$ inputs, are used by the VIC in determining which VMEbus address control signals ($\overline{DS0}$, $\overline{DS1}$, $\overline{A01}$, $\overline{LWORD}$) are asserted during VMEbus master transactions. For longword transfers, both of these bits should be cleared to the logic '0' state. For other transfers, please refer to the Cypress ***VIC068A / VAC068A User's Guide***, Tables 5–1 through 5–4.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.8 Local Semaphore Register (LSR)

'C6x Address – 0x0028 0028

The four MSBs of the Local Semaphore Registers (D15 : D12) contain the semaphores for the four banks of Dual Port SRAM that are locally accessible to each processor on its V–bus. These four banks of SRAM are also accessible from the global bus, and access to them is controlled by a set of interlocking semaphores. The remaining twelve bits are general purpose global bus semaphores, which the user may implement at his own discretion for any of the shared resources on the global bus. Each 'C6x processor on the Model 4290/4291 has a unique copy of this register.

The topic of Local bus (V–bus) access to the Dual Port SRAM is covered in detail in Section 7.2 of this manual, beginning on page 191 of this manual. For complete details about the LSR and how the bits it contains are used, please refer to Section 7.2.1, which starts on page 183. Table 4–27, below, shows the contents of the Local Semaphore register.

Table 4–27: Model 4290/4291 –Local Semaphore Register (LSR) –R/W @ 0x0028 0028

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Local_DP_ Semaphore_3	Local_DP_ Semaphore_2	Local_DP_ Semaphore_1	Local_DP_ Semaphore_0	GP_Global_ Semaphore_11	GP_Global_ Semaphore_10	GP_Global_ Semaphore_9	GP_Global_ Semaphore_8
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	GP_Global_ Semaphore_7	GP_Global_ Semaphore_6	GP_Global_ Semaphore_5	GP_Global_ Semaphore_4	GP_Global_ Semaphore_3	GP_Global_ Semaphore_2	GP_Global_ Semaphore_1	GP_Global_ Semaphore_0
Bit Function	1) Read '0' to check availability 2) Write '1' to request ownership				3) Read '1' to verify ownership 4) Write '0' to release			
All bits in this register are cleared to the logic '0' state by boot and reset operations.								

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.9 Interrupt Mapping Register (IMR0) – Option 330 ONLY!

'C6x Address – 0x0028 0030

This register is composed of four 4–bit fields, each of which is used to determine which interrupt–enabled event will be asserted on one of the 'C6x interrupt inputs EXT_INT4 :7. Table 4–28, below, shows which bitfield is used to select the sources of which interrupt. Table 4–29, at the bottom of this page, gives the interrupt sources that are selected for each 4–bit code that can be written to the bitfield associated with a given interrupt .

Table 4–28: Model 4290/4291 Opt. 330 –Interrupt Mapping Register –R/W @ 0x0028 0030

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	EXT_INT7_3	EXT_INT7_2	EXT_INT7_1	EXT_INT7_0	EXT_INT6_3	EXT_INT6_2	EXT_INT6_1	EXT_INT6_0
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	EXT_INT5_3	EXT_INT5_2	EXT_INT5_1	EXT_INT5_0	EXT_INT4_3	EXT_INT4_2	EXT_INT4_1	EXT_INT4_0
Function	See Table 4-29 , below							

All bits in this register are cleared to the logic '0' state by boot and reset operations.

Table 4–29: Model 4290/4291 –Interrupt Mapping Bit Settings

EXT_INTx_3	EXT_INTx_2	EXT_INTx_1	EXT_INTx_0	Events
1	x	x	x	Reserved - Undefined
0	1	1	1	Dual-Port SRAM Mailbox Interrupt
0	1	1	0	Incoming VIM Bi-FIFO Almost Full, Almost Empty, Empty or Mailbox
0	1	0	1	Outgoing VIM Bi-FIFO Almost Full, Almost Empty, Empty or Mailbox
0	1	0	0	Incoming ZZ Bi-FIFO Almost Full, Almost Empty, Empty or Mailbox
0	0	1	1	Outgoing ZZ Bi-FIFO Almost Full, Almost Empty, Empty or Mailbox
0	0	1	0	Incoming XX Bi-FIFO Almost Full, Almost Empty, Empty or Mailbox
0	0	0	1	Outgoing XX Bi-FIFO Almost Full, Almost Empty, Empty or Mailbox
0	0	0	0	Original (Standard) 4290/4291 Configuration*

*** –The Original (i. e., Standard) 4290/4291 interrupt configuration is as follows:**
Bi–FIFO Flags, VIM & Global Daughterboard Interrupts => EXT_INT7
Dual Port SRAM Mailbox Interrupt => EXT_INT6
Bi–FIFO Mailbox Interrupts => EXT_INT5
VIC 64 & VMEbus Interrupts => EXT_INT4
Refer to Figure 4-2, on page 108, for identification of the XX, ZZ & VIM Bi-FIFOs



Interrupts from the VMEbus, VIC & Global bus daughterboard, and Non–FIFO interrupts from VIM modules are effectively disabled for 'C6x interrupt inputs associated with any field in this register that contains a non-Zero value.

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.10 Board Version Register (BVR) – Option 330 ONLY!

'C6x Address – 0x0028 003C (Read Only)

Reading this address from a Revision 1 Model 4290/4291 board with Option 330 will return a '1'. The same read operation on a standard 4290/4291 board will return a '0'. Future board revisions will return larger numbers.

4.3.2.11 VME Interrupt Gating Control Register (IGCR)

'C6x Address – 0x0028 0100

This register is used when a 'C6x processor acts as a VMEbus interrupt handler, to determine which interrupt signals the DSP can respond to. Setting a bit in this register to the logic '1' state allows the corresponding IPL signal from the VIC64 to set the associated bit in the VME Interrupt Pending Register (VIPR, at V–bus address 0x0028 0104 – see Section 4.3.2.12, on the next page). Whether or not an IPL that does get passed to the Interrupt Pend–ing Register actually results in an interrupt to the DSP is deter–mined by the state of the associated bit in the IPL Enable Register (VIER, at V–bus address 0x0028 0124 – see Section 4.3.2.14, on page 106). Each 'C6x has a unique copy of this register. When the Model 4290/4291 is booted or reset, this register has a value of 0x0000, which means that no IPL signals are passed to the Inter–rupt Pending Register. Table 4–30, below, shows the bit structure of the IGCR.

Table 4-30: Model 4290/4291 –VME Interrupt Gating Control Register (IGCR) – R/W @0x0028 0100

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IPL_7_Gate	IPL_6_Gate	IPL_5_Gate	IPL_4_Gate	IPL_3_Gate	IPL_2_Gate	IPL_1_Gate	Reserved
Bit Function	1 = Pass IPL Signal to Interrupt Pending Register 0 = Do Not Pass IPL Signal to Interrupt Pending Register							Write '0' Mask on Reads
All bits in this register are cleared to the logic '0' state by boot and reset operations.								

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.12 VME Interrupt Pending Register (VIPR)

'C6x Address – 0x0028 0104 (Read Only)

This Read–Only register is used when a 'C6x processor acts as a VMEbus interrupt handler, to latch those IPLs that are passed by the Interrupt Gating Control Register (IGCR, at V–bus address 0x0028 0100, see Section 4.3.2.11, on the previous page). A logic '1' in any bit position in this register indicates that the IGCR has passed an IPL at the corresponding level from the VIC64. Whether or not the bits that become set in this register will generate an interrupt to the 'C6x depends upon the state of the corresponding bit in the Interrupt Enable Register (VIER, at V–bus address 0x0028 0124 – see Section 4.3.2.14, on page 106). This register may also be polled, allowing the 'C6x to monitor the states of IPLs that are not enabled for interrupt generation. Table 4–31, below, shows the bit structure of the VIPR. Figure 4–1, at the top of the next page, shows the resources involved in passing a VMEbus IRQ to a 'C6x processor on the Model 4290/4291.

Table 4–31: Model 4290/4291 –VME Interrupt Pending Register (VIPR) –R. O. @0x0028 0104

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IPL_7_ Pending	IPL_6_ Pending	IPL_5_ Pending	IPL_4_ Pending	IPL_3_ Pending	IPL_2_ Pending	IPL_1_ Pending	Reserved
Bit Function	1 = IPL Interrupt Pending 0 = No IPL Interrupt Pending							Write '0' Mask on Reads
All bits in this register are cleared to the logic '0' state by boot and reset operations.								

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

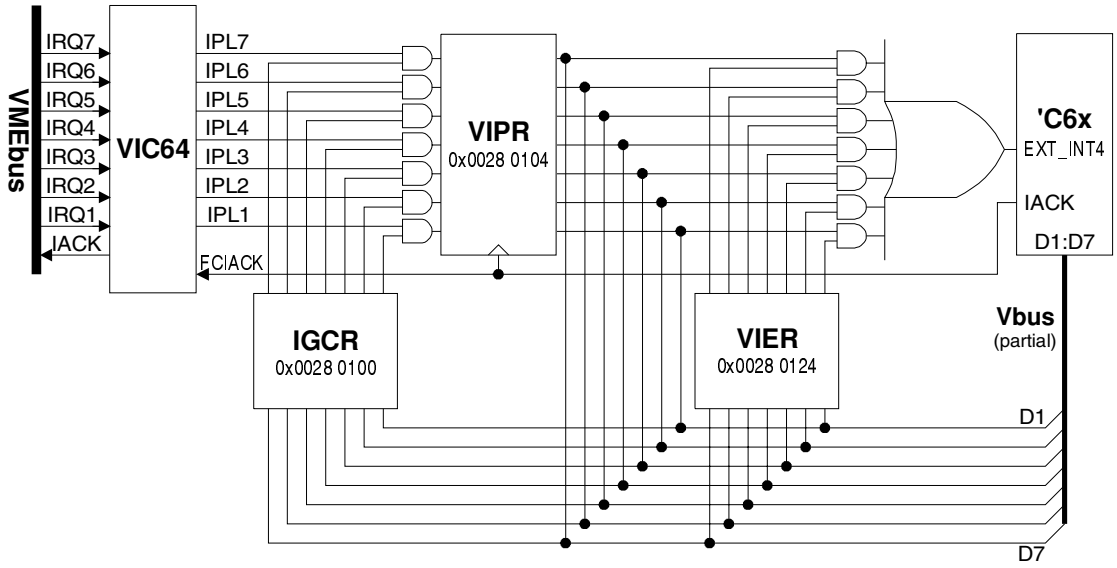


Figure 4-1: Model 4290/4291 - VMEbus Interrupt Path to 'C6x's

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.13 VME Interrupt Vector Registers (IVR(1:7))

'C6x Addresses:
IVR1 (IPL1) – 0x0028 0108
IVR2 (IPL2) – 0x0028 010C
IVR3 (IPL3) – 0x0028 0110
IVR4 (IPL4) – 0x0028 0114
IVR5 (IPL5) – 0x0028 0118
IVR6 (IPL6) – 0x0028 011C
IVR7 (IPL7) – 0x0028 0120

These registers are used when a 'C6x processor acts as a VMEbus interrupter. They store the IACK Vector Address (VA in the table below), for each VMEbus interrupt that may be asserted by a 'C6x Processor on the Model 4290/4291. Seven of these registers are provided for each DSP, one for each VMEbus interrupt level. The contents of this register will be placed on the VME Data bus when a resource on the Model 4290/4291 issues an interrupt to VME, in response to the IACK generated by the interrupt han–dler. Table 4–32, below, shows the correspondence between the bits in this register and the VME Data Bus lines that are their destinations.

Table 4–32: Model 4290/4291 –VMEbus IACK Vector Registers (IVR(1:7))–R/W @ 0x0028 0034

*Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Name	VA_15	VA_14	VA_13	VA_12	VA_11	VA_10	VA_9	VA_8
*Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Name	VA_7	VA_6	VA_5	VA_4	VA_3	VA_2	VA_1	VA_0
Function	VMEbus Interrupt Vector Address							

All bits default to the logic '0' state at power-up and resets.
***NOTE: The bit #'s in this register correspond to BOTH the bit's position in the register AND the VMEbus data signal upon which the bit's state will be asserted during the IACK cycle.**

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4.3 'C6x Access to Local Bus (V–bus) Resources (continued)

4.3.2 V–bus Control Registers (continued)

4.3.2.14 VME Interrupt Enable Register (VIER)

'C6x Address – 0x0028 0124

This register is used when a 'C6x processor acts as a VMEbus interrupt handler, to determine which IPL signals from the VIC64 will be allowed to interrupt the DSP. Those VMEbus interrupts that are allowed to propagate all the way through the register chain to the DSP (see Figure 4–1, on page 104) are delivered to the EXT_INT4 input of the 'C6x. To enable a given IPL to interrupt the DSP, set the associated bit in this register to the logic '1' state. A VMEbus IRQ can cause an interrupt to a 'C6x processor on the Model 4290/4291 **ONLY** when the following conditions are met:

1) The corresponding bit in the VME Interrupt Gating Control Register (IGCR, at V–bus address 0x0028 0100 – see Section 4.3.2.11, on page 102) is set to the logic '1' state.

2) The corresponding bit in this register (the VIER) is set to the logic '1' state.

3) **FOR OPTION 330 ONLY**: All four bits in the EXT_INT4 field of Interrupt Mapping Register 0 (D0 : D3 of IMR0, at V–bus address 0x0028 0030 – see Section 4.3.2.9 on page 101) are cleared to the logic '0' state.

Table 4–33, below, shows the bit structure of the VIER.

Table 4–33: Model 4290/4291 –VME Interrupt Enable Register (VIER) –R/W @0x0028 0124

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IPL_7_ Enable	IPL_6_ Enable	IPL_5_ Enable	IPL_4_ Enable	IPL_3_ Enable	IPL_2_ Enable	IPL_1_ Enable	Reserved
Bit Function	1 = Interrupt Enabled 0 = Interrupt Disabled							Write '0' Mask on Reads
All bits in this register are cleared to the logic '0' state by boot and reset operations.								

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.3 Random Access to VIM Modules

'C6x Address Region – 0x0030 0000 : 0x0033 FFFF

The Local 'C6x address region from 0x0030 0000 to 0x0033 FFFF is reserved for Direct, random access to the VIM module that may be installed on the processor's mezzanine interface. We have reserved the region between 0x0030 0000 and 0x0031 FFFF for I/O space, and the remaining region (from 0x0032 0000 to 0x0033 FFFF) for memory space. At the time of this publication, there are no VIM modules available from Pentek that utilize the I/O space. Module control registers and the like are generally mapped into the memory space. For information about the resources available in this region on any specific VIM module, please refer to the VIM module's operating manual.

4.3.4 Inter–Processor and VIM Bi–FIFO Access

Standard 'C6x Address Region – 0x0100 0000 : 0x011F FFFF

Option 330 'C6x Address Regions:

XX Bi–FIFO (Upstream)	**– 0x0300 0000 : 0x0303 FFFF**
ZZ Bi–FIFO (Downstream)	**– 0x0308 0000 : 0x030B FFFF**
VIM Bi–FIFO	**– 0x0310 0000 : 0x0313 FFFF**

The three Bi–directional FIFOs connected to each 'C6x's Local bus provide a powerful resource for the exchange of data with the other processors on the board, and with the VIM I/O expansion module. Additionally, since each processor's port to any given Bi–FIFO is available only to that particular processor, arbitration is never required for access.

Figure 4–2, on the next page, provides a simplified illustration of the inter–processor Bi–FIFO paths. We have (somewhat arbitrarily) chosen the designations XX and ZZ to distinguish between the two inter–processor Bi–FIFO ports available to each processor. We will also make reference in our discussions in the subsections that follow, to "upstream" and "downstream" access directions, which essentially refer to the J–TAG signal path. Thus, a downstream access means an exchange of data with the processor that preceeds the one in question in the J–TAG path, while an upstream access is an exchange with the next processor on the J–TAG path. The J–TAG path is illustrated in Figure 1–1, the Model 4290/4291 Block Diagram, on page 25 of this manual. An upstream access would be an access in the clockwise direction in Figure 4–2, while a downstream access would go counterclockwise in the figure.

Chapter 6 of this manual covers the topic of Bi–FIFO access in complete detail. For this section, we will simply point out that on standard versions of the Model 4290/4291, all 3 Bi–FIFOs are mapped into the same region of the 'C6x's CE1 space, and the programmer selects among the 3 Bi–FIFOs by means of the Bi–FIFO Select bits (D15 : D14) in the Miscellaneous Control Register (MCR) at address 0x0028 001C. On Option 330 units, each Bi–FIFO is mapped into a unique region of each DSP's CE3 space. Please refer to Sections 6.1.1 and 6.1.3 for further details.

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.4 Inter–Processor and VIM Bi–FIFO Access (continued)

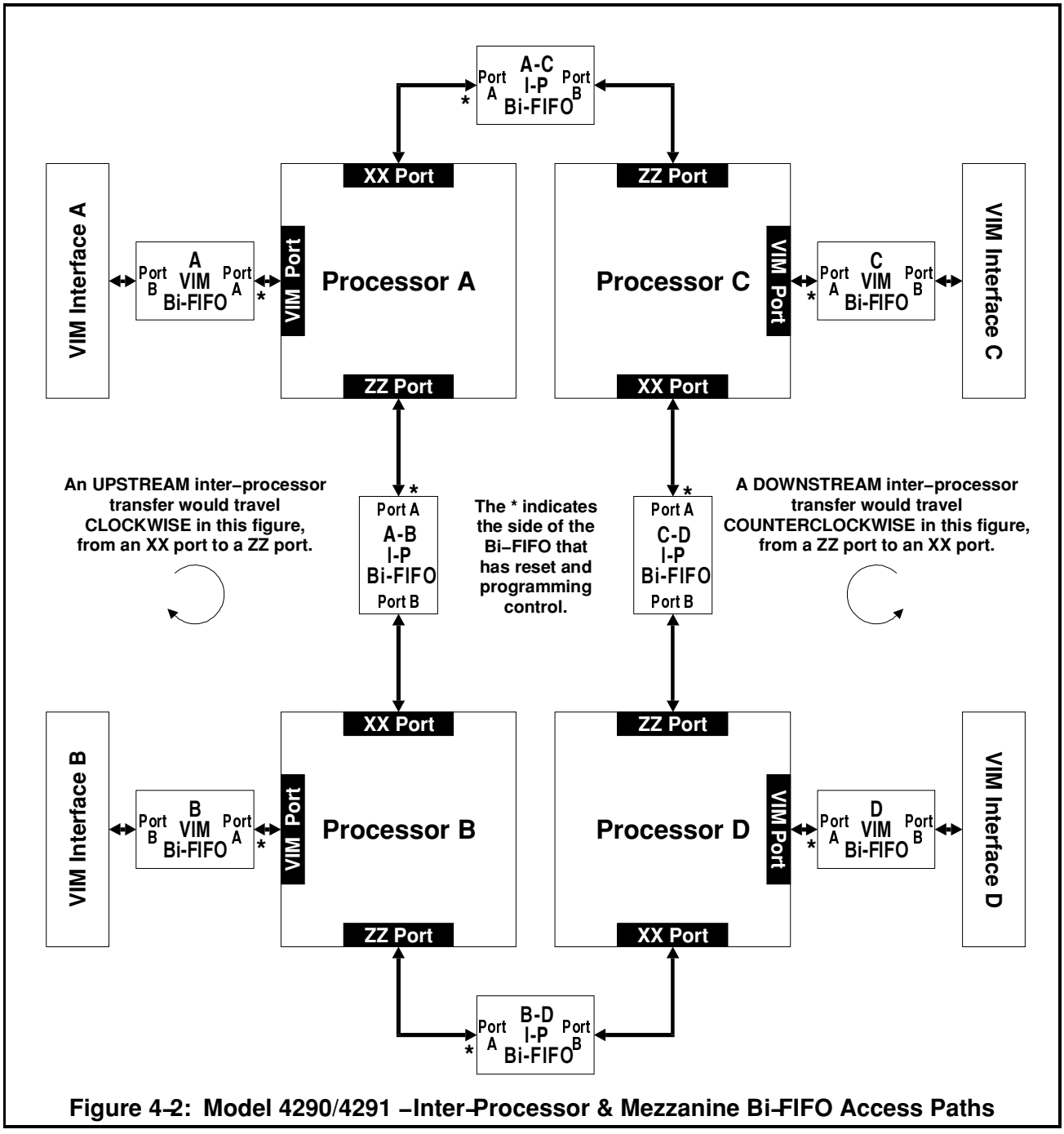


Figure 4-2: Model 4290/4291 –Inter-Processor & Mezzanine Bi-FIFO Access Paths

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.5 Inter–Processor and VIM Bi–FIFO Mailbox Register Access

Standard 'C6x Address Region – 0x0120 0000 : 0x013F FFFF

Option 330 'C6x Address Regions:

XX Bi–FIFO Mailbox – 0x0304 0000 : 0x0307 FFFF
ZZ Bi–FIFO Mailbox – 0x030C 0000 : 0x030F FFFF
VIM Bi–FIFO Mailbox – 0x0314 0000 : 0x0317 FFFF

Each of the three Bi–directional FIFOs connected to each 'C6x's Local bus on the Model 4290/4291 contains a mailbox, used for message passing, and connected to the board's interrupt structure. If a given Bi–FIFO port's mailbox interrupt is enabled, the processor that "owns" that port will be interrupted whenever data is written to that mailbox. As with the Bi–FIFOs themselves, mailbox access is handled differently in standard units and Option 330 units. Each of the 3 Bi–FIFO mailbox is mapped into the same address region on standard versions of the Model 4290/4291, and selection among the mailboxes (just like selection among the Bi–FIFOs themselves) is accomplished by setting the Bi–FIFO Select bits (D15 : D14) in the Miscellaneous Control Register (MCR) at address 0x0028 001C. On Option 330 units, each Bi–FIFO mailbox is mapped into a unique region of each DSP's CE3 space. For further information, please refer to Sections 6.1.2 and 6.1.4.

4.3.6 'C6x Internal Program Memory Access

'C6x Address Region – 0x0140 0000 : 0x0140 FFFF



When cache is enabled on the 'C6x, this is the internal resource that the DSP uses as the cache memory. Therefore, the 'C6x's Internal Program Memory is NOT ACCESSIBLE WHEN CACHE IS ENABLED.

Access to the 'C6x's 64 kByte Internal Program Memory (IPM) is provided in the region of the Local bus memory map from 0x0140 0000 to 0x0140 FFFF. Since this is also the internal resource that serves as the 'C6x's cache memory, it is **ONLY AVAILABLE** for those applications that will work **WITH CACHE DISABLED**. Remember that when using the IPM, the 'C6x always gives its CPU priority over its DMA engine. For DMA to access the IPM, there must be time slots during which it can gain access. These slots occur when a fetch packet (eight instructions) contains multiple execute packets (a group of instructions executed in one cycle). This leaves cycles available in which the CPU is not requesting a fetch packet, during which the DMA engine can access the IPM.

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.7 Access to 'C6x Internal Peripherals

'C6x Address Region – 0x0180 0000 : 0x01BF FFFF

This region of the 'C6x's local memory map provides access to the control registers internal to the 'C6x for the following functional blocks: the External Memory Interface (EMIF), the Direct Memory Access engine (DMA), the Host Port Interface (HPI), the two Multi−channel Bi−directional Serial Ports (McBSP's), and the two 32−bit timers (T0 & T1). Each of these peripherals will be discussed briefly in a serparate subsection, beginning at the top of the next page. For complete description of these peripherals, please refer to Texas Instruments' ***TMS320C6000 Peripherals Reference Guide ('C6x PRG)***, TI document # SPRU 190D, published in February, 2001. The subsections that follow will supply references to specific sections of the ***'C6xPRG***.

4.3.7.1 External Memory Interface (EMIF) Controls

⚠ WARNING: **The factory-supplied boot firmware resident on your Model 4290/4291initializes the EMIF registers for the optimum reliability of your board's configuration. TAMPERING WITH THESE REGISTERS IS NEITHER RECOMMENDED NOR SUPPORTED BY PENTEK.**

The 'C6x's EMIF supports a glueless interface to a variety of external devices, including Synchronous−burst SRAM (SBSRAM), Synchronous DRAM (SDRAM), asynchronous devices (including SRAM, ROM, and FIFOs) and external shared−memory devices. The EMIF services requests to the external bus from four requesters: the on−chip program memory controller (which services CPU program fetches); the on−chip data memory controller (which services CPU data fetches); the on−chip DMA controller; and an external shared−memory device controller. If multiple requests arrive simultaneously, the EMIF prioritizes them and performs the necessary number of operations. Table 4−34, at the top of the next page, lists the EMIF control registers, their addresses, and where you can find more information about them in Texas Instruments' ***TMS320C6000 Peripherals Reference Guide***.

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.7 Access to 'C6x Internal Peripherals (continued)

4.3.7.1 External Memory Interface (EMIF) Controls (continued)

Table 4-34: Model 4290/4291 - 'C6x EMIF Control Registers		
Address	**Register**	**Add'l Info***
0x0180 0000	EMIF Global Control Register	Sec. 10.2.1
0x0180 0004	EMIF CE1 Space Control Register	Sec. 10.2.2
0x0180 0008	EMIF CE0 Space Control Register	
0x0180 000C	Reserved	—
0x0180 0010	EMIF CE2 Space Control Register	Sec. 10.2.2
0x0180 0014	EMIF CE3 Space Control Register	
0x0180 0018	EMIF SDRAM Control Register	Sec. 10.2.3
0x0180 001C	EMIF SDRAM Timing Register	Sec. 10.2.4
* - entries in this column refer to section #'s in Texas Instruments' ***TMS320C6000 Peripherals Reference Guide***, TI document # SPRU 190D, published in February, 2001.		

Table 4–35, below, shows the default values for the 'C6x External Memory Interface (EMIF) Timing. These default settings were used in determining the number of clock cycles in the data transfer timing table in Chapter 9.

Table 4-35: Model 4290/4291 –EMIF Register Initialization Values			
Resource	**Address**	**Std. 4290 / 4291 (200 / 167 MHz)**	**4290 / 4291 Opt. 330 (200 / 167 MHz)**
EMIF Global Control Register	0x0180 0000	0x0000 33EC	0x0000 33EC
EMIF CE0 Space Control Register	0x0180 0008	0x71B7 0723	0x71B7 0B23
EMIF CE1 Space Control Register	0x0180 0004	0x30B5 0321	0x0000 0040
EMIF CE2 Space Control Register	0x0180 0010	0x0XXX X030	0x0XXX X030
EMIF CE3 Space Control Register	0x0180 0014	0x0XXX X040	0x0XXX X040
EMIF SDRAM Control Register	0x0180 0018	0x0744 F000	0x0744 F000
EMIF SDRAM Timing Register	0x0180 001C	0x0006 1200	0x0006 1200
NOTE: X = These bitfields are initialized to 0, but their readback values are indeterminate.			

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.7 Access to 'C6x Internal Peripherals (continued)

4.3.7.2 Direct Memory Access (DMA) Controls

The 'C6x's direct memory access (DMA) controller transfers data between regions in the memory map without intervention by the CPU. The DMA controller allows movement of data to and from internal memory, internal peripherals, or external devices to occur in the background of, thus simultaneously with, CPU operations. The DMA controller has four independent programmable chan–nels, allowing four different DMA operations to occur at the same time. In addition, a fifth channel, referred to as the auxilliary channel, is provided for the DMA controller to use for servicing requests from the host port interface (HPI). Table 4–36, below, lists the DMA control registers. Additional information may be found in the Texas Instruments' ***TMS320C6000 Peripherals Ref–erence Guide***.

Table 4-36: Model 4290/4291 - 'C6x DMA Control Registers

Address	Register
0x0184 0000	DMA Channel 0 Primary Control Register
0x0184 0004	DMA Channel 2 Primary Control Register
0x0184 0008	DMA Channel 0 Secondary Control Register
0x0184 000C	DMA Channel 2 Secondary Control Register
0x0184 0010	DMA Channel 0 Source Address Register
0x0184 0014	DMA Channel 2 Source Address Register
0x0184 0018	DMA Channel 0 Destination Address Register
0x0184 001C	DMA Channel 2 Destination Address Register
0x0184 0020	DMA Channel 0 Transfer Counter
0x0184 0024	DMA Channel 2 Transfer Counter
0x0184 0028	DMA Global Count Reload Register A
0x0184 002C	DMA Global Count Reload Register B
0x0184 0030	DMA Global Index Register A
0x0184 0034	DMA Global Index Register B
0x0184 0038	DMA Global Address Register A
0x0184 003C	DMA Global Address Register B
0x0184 0040	DMA Channel 1 Primary Control Register
0x0184 0044	DMA Channel 3 Primary Control Register
0x0184 0048	DMA Channel 1 Secondary Control Register
0x0184 004C	DMA Channel 3 Secondary Control Register
0x0184 0050	DMA Channel 1 Source Address Register
0x0184 0054	DMA Channel 3 Source Address Register
0x0184 0058	DMA Channel 1 Destination Address Register
0x0184 005C	DMA Channel 3 Destination Address Register
0x0184 0060	DMA Channel 1 Transfer Counter
0x0184 0064	DMA Channel 3 Transfer Counter
0x0184 0068	DMA Global Address Register C
0x0184 006C	DMA Global Address Register D
0x0184 0070	DMA Auxillary Control Register

* - entries in this column refer to section #'s in Texas Instruments' ***TMS320C6000 Peripherals Reference Guide***, TI document # SPRU 190D, published in February, 2001.

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.7 Access to 'C6x Internal Peripherals (continued)

4.3.7.3 Host Port Interface Controls

The host−port interface (HPI) is a 16−bit wide parallel port which a host processor can use to directly access the CPU's memory space. The host device is the master of this interface, which makes access to it easier. As used herein, the term "host" generally refers to any processor on another VMEbus board (or an external computer act−ing as a VMEbus device, via an adapter board, ethernet interface, etc.) that has become master of the VMEbus and addresses the Model 4290/4291 as a VME slave. The host and DSP can also use memory located either internal or external to the DSP to exchange information. The host gains its direct access to memory−mapped peripherals via this interface. Connectivity to the DSP's memory space is provided through the DMA controller. Dedicated address and data registers, which are not accessible to the DSP, connect the HPI to the DMA auxiliary channel, which in turn connects the HPI to the DSP's memory space. Both the host and the DSP can access the HPI control register (HPIC). ONLY the host can access the HPI address register (HPIA), the HPI data register (HPID). The host uses the external data and interface control signals to access those registers and the HPIC. Table 4−37, below, summarizes the resources that comprise the Host Port Interface. Additional infor−mation may be found in the Texas Instruments' ***TMS320C6000 Peripherals Reference Guide***.

Table 4-37: Model 4290/4291 - 'C6x HPI Registers

Address	Register
—†	HPI Data Register
—†	HPI Address Register
0x0188 0000	HPI Control Register

* – entries in this column refer to section #'s in Texas Instruments' ***TMS320C6000 Peripherals Reference Guide***, TI document # SPRU 190D, published in February, 2001.

† - These registers cannot be accessed by the DSP - they are only accessible to the Host.

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.7 Access to 'C6x Internal Peripherals (continued)

4.3.7.4 Serial Port Controls

The two multichannel buffered serial ports (McBSPs) in the 'C6x processors each consist of a data path and a control path, which connect to external devices. Data is communicated to these external devices via separate pins for transmission and reception. Control information (clocking and frame synchronization) is communicated via four other pins. The DSP communicates with the McBSPs via 32−bit−wide control registers accessible via the internal peripheral bus. Table 4−38, below, summarizes the Serial Port Control Registers. Additional information may be found in the Texas Instruments' ***TMS320C6000 Peripherals Reference Guide***.

Table 4-38: Model 4290/4291 - 'C6x McBSP Control Registers

McBSP0 Address	McBSP1 Address	Register
0x018C 0000	0x0190 0000	Data Receive Register
0x018C 0004†	0x0190 0004†	Data Transmit Register†
0x018C 0008	0x0190 0008	Serial Port Control Register
0x018C 000C	0x0190 000C	Receive Control Register
0x018C 0010	0x0190 0010	Transmit Control Register
0x018C 0014	0x0190 0014	Sample Rate Generator Register
0x018C 0018	0x0190 0018	Multichannel Control Register
0x018C 001C	0x0190 001C	Receive Channel Enable Register
0x018C 0020	0x0190 0020	Transmit Channel Enable Register
0x018C 0024	0x0190 0024	Pin Control Register

* – entries in this column refer to section #'s in Texas Instruments' ***TMS320C6000 Peripherals Reference Guide***., TI document # SPRU 190D, published in February, 2001.
† - These registers are Read Only.

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.7 Access to 'C6x Internal Peripherals (continued)

4.3.7.5 Timer Controls

Each 'C6x processor on the Model 43290/4291 contains two 32–bit general–purpose timers, called T0 and T1, that you can use to time or count events, generate pulses, generate interrupts or synchro–nize events with the DMA. The timers have two signaling modes and can be clocked by an internal or external source. Input pin and output pins are provided for each timer. The input and output pins can function as timer clock input and clock output, or they may be configured for general–purpose input and output, respec–tively. With an internal clock, the timer can signal an external A/D converter to start a conversion, or it can trigger the DMA controller to begin a data transfer. With an external clock, the timer can count external events and interrupt the CPU after a specified number of events. Table 4–39, below, summarizes the Timer Con–trol Registers. Additional information may be found in the Texas Instruments' ***TMS320C6000 Peripherals Reference Guide***.

Table 4-39: Model 4290/4291 - 'C6x Timer Control Registers

T0 Address	T1 Address	Register
0x0194 0000	**0x0198 0000**	Timer Control Register
0x0194 0004	**0x0198 0004**	Timer Period Register
0x0194 0008	**0x0198 0008**	Timer Counter Register

* – entries in this column refer to section #'s in Texas Instruments' ***TMS320C6000 Peripherals Reference Guide***, TI document # SPRU 190D, published in February, 2001.

4.3.8 SDRAM Access

'C6x Address Region – 0x0200 0000 : 0x02FF FFFF

16 MBytes of Synchronous DRAM are available to each 'C6x processor on the Model 4290/4291, mapped into CE2 memory space. This resource is arranged as four banks of 4 MBytes each, with each bank consisting of 4 k rows of 1 kByte each in length. This is a completely private resource for each proces–sor . Since the "owner" processor is the only device that can access the SDRAM, there is never a need to arbitrate for the it. This is also one of the faster memory resources available on the 4290/4291 – the 'C6x can complete both read and write accesses between the SDRAM and its Internal Data Mem–ory in two clock cycles. There is, however, a 60 nsec row–access penalty that will be incurred on any access that crosses a row boundary with respect to the previous access.

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4.3 'C6x Local Data Bus Memory Resources (continued)

4.3.9 SBSRAM Access

Standard 'C6x Address Region – 0x0300 0000 : 0x0307 FFFF

Option 330 'C6x Address Region – 0x0100 0000 : 0x0107 FFFF

This is the fastest memory available on the Model 4290/4291, able to complete transfers with the 'C6x Internal Data Memory in a single clock cycle. This 512 kByte (organized as 128k x 32) resource is also available only to the 'C6x processor that "owns" it, so that arbitration for it is never necessary. It resides in CE3 space ('C6x address range 0x0300 0000 through 0x0307 FFFF) on stan–dard 4290/4291's, and in CE1 space (0x0100 0000 through 0x0107 FFFF) on Option 330 units.



Due to a bug in the design of the TMS3206701 DSP chip, DMA READ operations from SBSRAM will take TWO clock cycles to complete on the Model 4291. The 4291 can still do DMA WRITES to SBSRAM in a single clock cycle, and the 4290 can complete both DMA READS and WRITES with SBSRAM in a single cycle.

4.3.10 'C6x Internal Data Memory Access

'C6x Address Region – 0x8000 0000 : 0x8000 FFFF

Each 'C6x processor on the 4290/4291 has 64 kBytes of Internal Data RAM, which are organized as two blocks of 32 kBytes, located from address 0x8000 0000 to 0x8000 7FFF and 0x8000 8000 to 0x8000 FFFF. The DMA con–troller or side A and side B of the CPU can simultaneously access any portion of the internal memory without conflict, provided that they access different blocks. Both blocks are organized as four 4 kByte banks of 16–bit halfwords. Therefore you do not have to consider the address within a block if simulta–neous accesses occur to different blocks. Accesses to different blocks never cause performance penalties. Both CPU and DMA can still simultaneously access data that resides in different banks within the same block without a performance penalty. To avoid performance penalties, you have to pay attention to address LSBs when the two accesses involve data in the same block. This organization also allows the two CPU data ports, A and B, to simultaneously access neighboring 16–bit data elements inside the block without a resource conflict.

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Chapter 5: VMEbus and Global Bus Memory Maps and Resources

5.1 Overview and Memory Maps

The Model 4290/4291 provides a full featured master/slave VME64 interface. As a bus master, the board can access the user address spaces for A32, A24, and A16 modes of operation, and as a result can also access any external slave as a master. As a VMEbus slave, the board presents memory images in A32, A24 and A16 space. Utilizing the VIC64/CY7C964 chipset from Cypress Semiconductor as the core of the interface, the board supports 64–, 32–, and 16–bit master and slave block transfers. The board also supports 32–, 16– and 8–bit single cycle transfers as a VME master and slave. As a VME system controller, the board can act as a bus arbiter for multiple–master systems. The Model 4290/4291 additionally supports VMEbus interrupt generation and handling. For additional detailed information on this interface, please refer to the ***VIC64/CY7C964 Design Notes*** and the ***VIC068A/VAC068A User's Guide***. Excerpts from these documents are included in this manual as Appendix A.

This chapter contains memory maps for, and a review of, those resources that are accessible on the Model 4290/4291's Global bus. As pointed out in the previous chapter, all resources on the Global bus are available to all four 'C6x processors on the 4290/4291 board, and are also accessible to VMEbus masters. The on–board processors access these resources via a 2 MByte window of their V–bus (i. e., local) memory maps, with the assistance of a Page Register. The V–bus addresses and Page Register settings used by the DSPs to access these resources were all covered in Chapter 4. The memory maps in this chapter will be presented from the point of view of an off–card VMEbus master.

Three independent address regions are defined for the VMEbus: A16 space which uses only 16 bits of the VME address bus and allows access to over 65,500 discrete addresses; A24 space, which uses 24 bits of the VME address bus, allowing access to over 16,700,000 discrete addresses; and A32 space, which utilizes all 32 VMEbus address bits and allows access to over 4,250,000,000 discrete memory locations.

Each Model 4290/4291 installed in a given VMEbus system will always occupy 256 bytes of A16 space, and 32 MBytes of A32 space. (Note that these quantities indicate the total amount of space within a given VMEbus memory region that is assigned to any installed Model 4290/4291, as opposed to the amount of memory resources actually available on that device.) If A24 access is enabled for a given 4290/4291 board, (see Section 2.2.2, on page 34 of this manual), then that board will occupy the ENTIRE 16 MByte A24 memory region. Thus, in a system with multiple 4290/4291's, only one can be enabled for A24 access. Stated another way, if a Model 4290/4291 that is installed in your VMEbus system is enabled for A24 access, no other device in that system can also be enabled for A24 access.

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5.1 Overview and Memory Maps (continued)

A group of eight jumper blocks, AJ1 : AJ8 (see Section 2.2.1, on page 31), are used to set the slave base address (i. e., the lowest address that a given device will respond to when addressed as a slave) for the Model 4290/4291 in both A16 and A32 VMEbus address spaces. The address of any given resource in either of these address spaces will be expressed as an offset from that space's base address, e. g., A16_base+0x0040 or A32_base+0x00A4 00A0. Because the board occupies the entire A24 region, the A24_base address is always 0x00 0000, and A24 addresses will be stated simply as the unaltered Global bus address (e. g., 0xA4 00A0).

Tables 5–1, 5–2 and 5–3, below and on the next two pages, present the slave memory maps for a Model 4290/4291 in A16, A24 and A32 VMEbus address spaces. Note that the only resources available in A16 space are internal registers of the VIC64 VME Interface Controller, and the 74ACT8990 JTAG Interface Controller. Access to the other Global bus resources (the Global, Dual Port & Non−Volatile SRAMs, the Flash EEPROM and the Global bus Control Registers) are provided in the A24 and A32 memory maps. VMEbus access to the Global Expansion Daughterboard is only available in A32 space.

Table 5–1: Model 4290/4291 –VMEbus A16 Slave Memory Map
(Board occupies 256 Bytes of 64 kByte A16 VMEbus address space.)

VMEbus A16 Address Range	Resource	Block Size	Access Mode	Add'l Info
A16_base+0x0000 - 0x003F	VIC64 Registers	64 Bytes	A16/D16, A16/D8	Table 5–4
A16_base+0x0040 - 0x007F	JTAG Controller	64 Bytes	A16/D16	Table 5–5

NOTES: A16 access is limited to the VIC64 and JTAG controller registers.
The jumpers AJ8 : AJ1 are used to set both the A16 and A32 base addresses (see Section 2.2.1).
Address bit A7 is not used in the address decode, thus
the identical VIC registers are also accessible @ A16_base+0x0080 - 0x00BF,
and the identical JTAG registers can also be accessed @ A16_base+0x00C0 - 0x00FF

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5.1 Overview and Memory Maps (continued)

Table 5-2: Model 4290/4291 –VMEbus A24 Slave Memory Map
(If A24 access is enabled*, board occupies 16 MBytes of 16 MByte A24 VMEbus address space.)

VMEbus A24 Address Range	Resource	Block Size	Access Mode	Additional Information
0x00 0000 –0x7F FFFF	Flash EEPROM	8 MB	A24/D32	Section 5.3.1
0x80 0000 –0x9F FFFF	Global SRAM	2 MB	A24/D32, A24/D16, A24/D8, BLT†	Section 5.3.2
0xA0 0000 –0xA3 FFFF	'C6x A DPSRAM	256 kB	A24/D32, A24/D16, A24/D8, BLT†	Section 5.3.3 & Chapter 7
0xA4 0000 –0xA7 FFFF	'C6x A DPSRAM Mailbox & Interrupt Control	256 kB	A24/D32, A24/D16, A24/D8	
0xA8 0000 –0xAB FFFF	'C6x C DPSRAM	256 kB	A24/D32, A24/D16, A24/D8, BLT†	
0xAC 0000 –0xAF FFFF	'C6x C DPSRAM Mailbox & Interrupt Control	256 kB	A24/D32, A24/D16, A24/D8	
0xB0 0000 –0xB3 FFFF	'C6x D DPSRAM	256 kB	A24/D32, A24/D16, A24/D8, BLT†	
0xB4 0000 –0xB7 FFFF	'C6x D DPSRAM Mailbox & Interrupt Control	256 kB	A24/D32, A24/D16, A24/D8	
0xB8 0000 –0xBB FFFF	'C6x B DPSRAM	256 kB	A24/D32, A24/D16, A24/D8, BLT†	
0xBC 0000 –0xBF FFFF	'C6x B DPSRAM Mailbox & Interrupt Control	256 kB	A24/D32, A24/D16, A24/D8	
0xC0 0000 –0xCF FFFF	NVSRAM	1 MB	A24/D32 (Only 8 MSBs of data are valid)	Section 5.3.4
0xD0 0000 –0xDF FFFF	'C6x Host Port Interfaces	1 MB	A24/D16	Section 5.3.5
0xE0 0000 –0xEF FFFF	Global Bus Control Registers	1 MB	A24/D16	Section 5.3.6
0xF0 0000 –0x FF FFFF	Reserved	1 MB	N/A	—

*** –A24 access is enabled by shorting jumper block A24 (see Section 2.2.2)**
† –BLT indicates Block Transfer support in D16, D32, and D64 modes

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5.1 Overview and Memory Maps (continued)

Table 5-3: Model 4290/4291 –VMEbus A32 Slave Memory Map
(Board occupies 32 MBytes of 4 GByte A32 VMEbus address space.)

VMEbus A32 Address Range	Resource	Block Size	Access Mode	Add'l Info
A32_base+0x0000 0000 - 0x007F FFFF	Flash EEPROM	8 MB	A32/D32	Section 5.3.1
A32_base+0x0080 0000 - 0x009F FFFF	Global SRAM	2 MB	A32/D32, A32/D16, A32/D8, BLT*	Section 5.3.2
A32_base+0x00A0 0000 - 0x00A3 FFFF	'C6x A DPSRAM	256 KB	A32/D32, A32/D16, A32/D8, BLT*	Section 5.3.3 & Chapter 7
A32_base+0x00A4 0000 –0x00A7 FFFF	'C6x A DPSRAM Mailbox & Interrupt Control	256 KB	A32/D32, A32/D16, A32/D8	
A32_base+0x00A8 0000 –0x00AB FFFF	'C6x C DPSRAM	256 KB	A32/D32, A32/D16, A32/D8, BLT*	
A32_base+0x00AC 0000 –0x00AF FFFF	'C6x C DPSRAM Mailbox & Interrupt Control	256 KB	A32/D32, A32/D16, A32/D8	
A32_base+0x00B0 0000 –0x00B3 FFFF	'C6x D DPSRAM	256 KB	A32/D32, A32/D16, A32/D8, BLT*	
A32_base+0x00B4 0000 –0x00B7 FFFF	'C6x D DPSRAM Mailbox & Interrupt Control	256 KB	A32/D32, A32/D16, A32/D8	
A32_base+0x00B8 0000 –0x00BB FFFF	'C6x B DPSRAM	256 KB	A32/D32, A32/D16, A32/D8, BLT*	
A32_base+0x00BC 0000 –0x00BF FFFF	'C6x B DPSRAM Mailbox & Interrupt Control	256 KB	A32/D32, A32/D16, A32/D8	
A32_base+0x00C0 0000 –0x00CF FFFF	NVSRAM	256 KB	A32/D32 (Only 8 MSBs of data are valid)	Section 5.3.4
A32_base+0x00D0 0000 –0x00DF FFFF	'C6x Host Port Interfaces	128 KB	A32/D16	Section 5.3.5
A32_base+0x00E0 0000 –0x00EF FFFF	Global Bus Control Registers	512 KB	A32/D32, A32/D16	Section 5.3.6
A32_base+0x00F0 0000 –0x00F0 FFFF	Reserved	1 MB	N/A	—
A32_base+0x0100 0000 –0x01FF FFFF	Global Bus Expansion Daughterboard	16 MB	A32/D32, A32/D16, A32/D8, BLT*	Section 5.3.7

NOTES: The jumpers AJ8 : AJ1 are used to set both the A32 and A16 base addresses (see Section 2.2.1).
*** –BLT indicates Block Transfer support in D16, D32, and D64 modes**

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5.2 VMEbus A16 Slave Resources

Each Model 4290/4291 installed in your VMEbus system will occupy 256 bytes of A16 memory space, starting at the base address selected by the settings of jumper blocks AJ1 : AJ8 (see Section 2.2.1). As shown in Table 5–1, there are two groups of resources available in A16 space. One of these groups is the internal register set of the Cypress VIC64 VMEbus Interface Controller. These registers are listed in Table 5–4, below, and are described in detail in Appendix A of this manual, which contains excerpts from the VIC64 manual. The other group is the internal register set of the on–board JTAG Test Bus Controller (TBC), Texas Instruments' 74ACT8990. These registers are listed in Table 5–5, on the next page, and are described in detail in Appendix B of this manual, which contains a TI application note about the use and programming of the TBC.

Table 5-4: Model 4290/4291 –VMEbus A16 Master-Accessible Registers in the VIC64

VMEbus A16 Address	Register	Description	Access
A16_base+0x0001	ICR0	Interprocessor Communications Register 0	Read / Write
A16_base+0x0003	ICR1	Interprocessor Communications Register 1	
A16_base+0x0005	ICR2	Interprocessor Communications Register 2	
A16_base+0x0007	ICR3	Interprocessor Communications Register 3	
A16_base+0x0009	ICR4	Interprocessor Communications Register 4	
A16_base+0x000B	ICR5	Interprocessor Communications Register 5	
A16_base+0x000D	ICR6	Interprocessor Communications Register 6	
A16_base+0x000F	ICR7	Interprocessor Communications Register 7	
A16_base+0x0010	CLR_ICGS0	Clear Interprocessor Comm. Global Switch 0	Write Only
A16_base+0x0011	SET_ICGS0	Set Interprocessor Comm. Global Switch 0	
A16_base+0x0012	CLR_ICGS1	Clear Interprocessor Comm. Global Switch 1	
A16_base+0x0013	SET_ICGS1	Set Interprocessor Comm. Global Switch 1	
A16_base+0x0014	CLR_ICGS2	Clear Interprocessor Comm. Global Switch 2	
A16_base+0x0015	SET_ICGS2	Set Interprocessor Comm. Global Switch 2	
A16_base+0x0016	CLR_ICGS3	Clear Interprocessor Comm. Global Switch 3	
A16_base+0x0017	SET_ICGS3	Set Interprocessor Comm. Global Switch 3	
A16_base+0x0020	CLR_ICMS0	Clear Interprocessor Comm. Module Switch 0	
A16_base+0x0021	SET_ICMS0	Set Interprocessor Comm. Module Switch 0	
A16_base+0x0022	CLR_ICMS1	Clear Interprocessor Comm. Module Switch 1	
A16_base+0x0023	SET_ICMS1	Set Interprocessor Comm. Module Switch 1	
A16_base+0x0024	CLR_ICMS2	Clear Interprocessor Comm. Module Switch 2	
A16_base+0x0025	SET_ICMS2	Set Interprocessor Comm. Module Switch 2	
A16_base+0x0026	CLR_ICMS3	Clear Interprocessor Comm. Module Switch 3	
A16_base+0x0027	SET_ICMS3	Set Interprocessor Comm. Module Switch 3	

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5.2 VMEbus A16 Slave Resources (continued)

Table 5-5: Model 4290/4291 – VMEbus A16 Master-Accessible JTAG Test Bus Controller Registers

VMEbus A16 Address	Register	Description	Access
A16_base+0x0040	Control0	Interrupt Control Bits	Read / Write
A16_base+0x0041	Control1	Special Test Functions	
A16_base+0x0042	Control2	TMS(0:5) Connections	
A16_base+0x0043	Control3	TMS/Event Function, TDO on/off, TMS/TCK data format	
A16_base+0x0044	Control4	Delay, TDI/TDO data format	
A16_base+0x0045	Control5	Event pins data output & direction	
A16_base+0x0046	Control6	Event Choice of EVENT 0/1 inputs	
A16_base+0x0047	Control7	Event Choice of EVENT 2/3 inputs	
A16_base+0x0048	Control8	COUNTER1 control	
A16_base+0x0049	Control9	COUNTER2 control	
A16_base+0x004A	Minor Command	Replace Interrupt Flag bits, Control of Test Run, Read Status, Load counters & Count, SW Reset	
A16_base+0x004B	Major Command	STATE command, EXECUTE command, SCAN command	
A16_base+0x004C	Counter1 Update0	COUNTER1 lower value word or COUNTER10	
A16_base+0x004D	Counter1 Update1	COUNTER1 higher value word or COUNTER11	
A16_base+0x004E	Counter2 Update0	COUNTER2 lower value word or COUNTER20	
A16_base+0x004F	Counter2 Update1	COUNTER2 higher value word or COUNTER21	
A16_base+0x0050	Status0	Internal States	Read Only
A16_base+0x0051	Status1	External Signals & Requests	
A16_base+0x0052	Status2	State of test board & Buffer	
A16_base+0x0053	Status3	Not Used	
A16_base+0x0054	Capture0	COUNTER1 lower value word	
A16_base+0x0055	Capture1	COUNTER1 higher value word	
A16_base+0x0056	Read Buffer	Input Buffer for TDI	
A16_base+0x0057	Write Buffer	Output Buffer for TDO	Write Only



Users of Pentek's SwiftNet DSP Networking Software should be aware of the following:

1) **Administration of this register is handled completely by SwiftNet, such that it becomes transparent to the user.**
2) **In order to use SwiftNet, Jumper Block JB3 must be OPEN (i.e., the jumper must be removed).**

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5.3 VMEbus A24/A32 Slave Resources

All the resources contained in the VMEbus slave memory maps for both A24 space and A32 space are accessed via the Model 4290/4291's Global bus, and are also accessible to the 'C6x processors. The subsections that follow will include descriptions of these resources, and may also include cross−references to descriptions found elsewhere in this manual. From the point of view of the DSP's on the Model 4290/4291, all of the resources described in the following subsections will appear in the same address range, 0x0000 0000 : 0x001F FFFF. The 'C6xs access the resources on the Global bus via a page register. The appropriate page register setting for 'C6x access to each resource will be given at the beginning of each section, along with the VMEbus A24 and A32 slave addresses.

5.3.1 Flash EEPROM

Global Bus Address Region – 0x0000 0000 : 0x007F FFFF
VMEbus A32 Address Region – A32_base+0x0000 0000 : A32_base+0x007F FFFF
VMEbus A24 Address Region – 0x00 0000 : 0x7F FFFF

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0000 : 0x0000 0030
Base Offset – 0x0000 0000

Except in the special cases of downloading user boot code (see Section 8.12) or upgrading the factory boot code (please refer to the Release Note entitled Updating Model 4290/4291 's Boot Firmware, Pentek part # 800.42908) access to this resource is Read−Only. This resource appears as a single, 8 MByte block of ROM in either VMEbus address space, and is always accessed in D32 mode. This resource is also accessible to the on−board DSP's, with the page register set for 0x0000 0000, 0x0000 0010, 0x0000 0020 or 0x0000 0030 (the EEPROM occupies four pages of 'C6x memory).

5.3.2 Global SRAM

Global Bus Address Region – 0x0080 0000 : 0x009F FFFF
VMEbus A32 Address Region – A32_base+0x0080 0000 : A32_base+0x009F FFFF
VMEbus A24 Address Region – 0x80 0000 : 0x9F FFFF

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0040
Base Offset – 0x0000 0000

This 512k x 32 block of Static RAM is the primary resource for the sharing of data between the VMEbus and the 'C6x processors on the Model 4290/4291. It appears as a single block of RAM in the A24/A32 VME slave memory maps (where it is accessible in D8, D16 and D32 modes, in the address range VME_base+0x0080 0000 : VME_base+09F FFFF), and in the memory maps of the 'C6x processors (where it can be accessed ONLY in D32 mode), with the page register set for 0x0000 0040.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.3 Dual Port SRAM and Mailboxes

Global Bus Address Region – 0x00A0 0000 : 0x00BF FFFF
VMEbus A32 Address Region – A32_base+0x00A0 0000 : A32_base+0x00BF FFFF
VMEbus A24 Address Region – 0xA0 0000 : 0xBF FFFF
Base Offsets –

DPSRAM A –	**0x00A0 0000 : 0x00A3 FFFF**
DP A Mailboxes –	**0x00A4 0000 : 0x00A7 FFFF**
DPSRAM C –	**0x00A8 0000 : 0x00AB FFFF**
DP C Mailboxes –	**0x00AC 0000 : 0x00AF FFFF**
DPSRAM D –	**0x00B0 0000 : 0x00B3 FFFF**
DP D Mailboxes –	**0x00B4 0000 : 0x00B7 FFFF**
DPSRAM B –	**0x00B8 0000 : 0x00BB FFFF**
DP B Mailboxes –	**0x00BC 0000 : 0x00BF FFFF**

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0050
Base Offsets –

DPSRAM A – 0x0000 0000	**DP A Mailboxes – 0x0004 0080**
DPSRAM C – 0x0008 0000	**DP C Mailboxes – 0x000C 0080**
DPSRAM D – 0x0010 0000	**DP D Mailboxes – 0x0014 0080**
DPSRAM B – 0x0018 0000	**DP B Mailboxes – 0x001C 0080**

There are four blocks of Dual Port SRAM on the Model 4290/4291. The size of each block depends upon the option ordered: Option 240 provides four blocks of 128 kBytes (32k x 32) each, for a total of 512k Bytes (128k x 32); Option 244 provides four blocks of 256 kBytes (64k x 32) each, for a total 1 MByte (256k x 32).

Each 'C6x processor has V–bus access to one of the four blocks of Dual Port SRAM. All four 'C6x processors and the VMEbus have Global bus access to all four blocks of Dual Port SRAM. In general, a given processor accesses its own block of Dual Port SRAM via its V–bus (in the address range from 0x0020 0000 : 0x0023 0000), and the other three processsors' blocks via the Global bus (with the Page Register set to 0x0000 0050, in the address window from 0x0000 0000 : 0x001F FFFF, using the offsets indicated above).

Detailed information about this powerful shared resource, and how it is configured, used and controlled, can be found in Chapter 7 of this manual.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.3 Dual Port SRAM and Mailboxes (continued)

Table 5-6: Model 4290/4291 –Memory Map for Global Bus Side of Dual Port SRAM – VMEbus Address Offsets

Resource	Access	Option 244	Option 240
DPSRAM A, bank 0, Global Port	R/W	0x00A0 0000 : 0x00A0 3FFF	0x00A0 0000 : 0x00A0 1FFF
DPSRAM A, bank 1, Global Port		0x00A0 4000 : 0x00A0 7FFF	0x00A0 2000 : 0x00A0 3FFF
DPSRAM A, bank 2, Global Port		0x00A0 8000 : 0x00A0 BFFF	0x00A0 4000 : 0x00A0 5FFF
DPSRAM A, bank 3, Global Port		0x00A0 C000 : 0x00A0 FFFF	0x00A0 6000 : 0x00A0 7FFF
Reserved	—	0x00A1 0000: 0x00A3 FFFF	0x00A0 8000 : 0x00A3 FFFF
Reserved		0x00A4 0000 : 0x00A4 007F	
Global Port A → V-bus A DPSRAM Mailbox	R/W	0x00A4 0080	
Global Port C → V-bus A DPSRAM Mailbox		0x00A4 0084	
Global Port D → V-bus A DPSRAM Mailbox		0x00A4 0088	
Global Port B → V-bus A DPSRAM Mailbox		0x00A4 008C	
V-bus A → Global Port A DPSRAM Mailbox	R. O.	0x00A4 0090	
V-bus A → Global Port C DPSRAM Mailbox		0x00A4 0094	
V-bus A → Global Port D DPSRAM Mailbox		0x00A4 0098	
V-bus A → Global Port B DPSRAM Mailbox		0x00A4 009C	
DP Interrupt Control/Status Register A	R/W	0x00A4 00A0	
Reserved	—	0x00A4 00A4 : 0x00A7 FFFF	
DPSRAM C, bank 0, Global Port	R/W	0x00A8 0000 : 0x00A8 3FFF	0x00A8 0000 : 0x00A8 1FFF
DPSRAM C, bank 1, Global Port		0x00A8 4000 : 0x00A8 7FFF	0x00A8 2000 : 0x00A8 3FFF
DPSRAM C, bank 2, Global Port		0x00A8 8000 : 0x00A8 BFFF	0x00A8 4000 : 0x00A8 5FFF
DPSRAM C, bank 3, Global Port		0x00A8 C000 : 0x00A8 FFFF	0x00A8 6000 : 0x00A8 7FFF
Reserved	—	0x00A9 0000 : 0x00AB FFFF	0x00A8 8000 : 0x00AB FFFF
Reserved		0x00AC 0000 : 0x00AC 007F	
Global Port A → V-bus C DPSRAM Mailbox	R/W	0x00AC 0080	
Global Port C → V-bus C DPSRAM Mailbox		0x00AC 0084	
Global Port D → V-bus C DPSRAM Mailbox		0x00AC 0088	
Global Port B → V-bus C DPSRAM Mailbox		0x00AC 008C	
V-bus C → Global Port A DPSRAM Mailbox	R. O.	0x00AC 0090	
V-bus C → Global Port C DPSRAM Mailbox		0x00AC 0094	
V-bus C → Global Port D DPSRAM Mailbox		0x00AC 0098	
V-bus C → Global Port B DPSRAM Mailbox		0x00AC 009C	
DP Interrupt Control/Status Register C	R/W	0x00AC 00A0	
Reserved	—	0x00AC 00A4 : 0x00AF FFFF	

NOTES: The addresses given above are valid as shown for A24 VME slave access.
For A32 access, the A32_base address must be added to all addresses shown.
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.
Table 5-6 is continued on the next page

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.3 Dual Port SRAM and Mailboxes (continued)

Table 5-6: Model 4290/4291 –Global Bus Side of Dual Port SRAM – VMEbus Address Offsets (continued)

Resource	Access	Option 244	Option 240
DPSRAM D, bank 0, Global Port	R/W	0x00B0 0000 : 0x00B0 3FFF	0x00B0 0000 : 0x00B0 1FFF
DPSRAM D, bank 1, Global Port		0x00B0 4000 : 0x00B0 7FFF	0x00B0 2000 : 0x00B0 3FFF
DPSRAM D, bank 2, Global Port		0x00B0 8000 : 0x00B0 BFFF	0x00B0 4000 : 0x00B0 5FFF
DPSRAM D, bank 3, Global Port		0x00B0 C000 : 0x00B0 FFFF	0x00B0 6000 : 0x00B0 7FFF
Reserved	—	0x00B1 0000 : 0x00B3 FFFF	0x00B0 8000 : 0x00B3 FFFF
Reserved		0x00B4 0000 : 0x00B4 007F	
Global Port A → V-bus D DPSRAM Mailbox	R/W	0x00B4 0080	
Global Port C → V-bus D DPSRAM Mailbox		0x00B4 0084	
Global Port D → V-bus D DPSRAM Mailbox		0x00B4 0088	
Global Port B → V-bus D DPSRAM Mailbox		0x00B4 008C	
V-bus D → Global Port A DPSRAM Mailbox	R. O.	0x00B4 0090	
V-bus D → Global Port C DPSRAM Mailbox		0x00B4 0094	
V-bus D → Global Port D DPSRAM Mailbox		0x00B4 0098	
V-bus D → Global Port B DPSRAM Mailbox		0x00B4 009C	
DP Interrupt Control/Status Register D	R/W	0x00B4 00A0	
Reserved	—	0x00B4 00A4 : 0x00B7 FFFF	
DPSRAM B, bank 0, Global Port	R/W	0x00B8 0000 : 0x00B3 FFFF	0x00B8 0000 : 0x00B8 1FFF
DPSRAM B, bank 1, Global Port		0x00B8 4000 : 0x00B8 7FFF	0x00B8 2000 : 0x00B8 3FFF
DPSRAM B, bank 2, Global Port		0x00B8 8000 : 0x00B8 BFFF	0x00B8 4000 : 0x00B8 5FFF
DPSRAM B, bank 3, Global Port		0x00B8 C000 : 0x00B8 FFFF	0x00B8 6000 : 0x00B8 7FFF
Reserved	—	0x00B9 0000 : 0x00BB FFFF	0x00B8 8000 : 0x00BB FFFF
Reserved		0x00BC 0000 : 0x00BC 007F	
Global Port A → V-bus B DPSRAM Mailbox	R/W	0x00BC 0080	
Global Port C → V-bus B DPSRAM Mailbox		0x00BC 0084	
Global Port D → V-bus B DPSRAM Mailbox		0x00BC 0088	
Global Port B → V-bus B DPSRAM Mailbox		0x00BC 008C	
V-bus B → Global Port A DPSRAM Mailbox	R. O.	0x00BC 0090	
V-bus B → Global Port C DPSRAM Mailbox		0x00BC 0940	
V-bus B → Global Port D DPSRAM Mailbox		0x00BC 0098	
V-bus B → Global Port B DPSRAM Mailbox		0x00BC 009C	
DP Interrupt Control/Status Register B	R/W	0x00BC 00A0	
Reserved	—	0x00BC 00A4 : 0x00BF FFFF	

NOTES: The addresses given above are valid as shown for A24 VME slave access.
For A32 access, the A32_base address must be added to all addresses shown.
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.4 Non–Volatile SRAM

Global Bus Address Region – 0x00C0 0000 : 0x00CF FFFF
VMEbus A32 Address Region – A32_base+0x00C0 0000 : A32_base+0x00CF FFFF
VMEbus A24 Address Region – 0xC0 0000 : 0xCF FFFF

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0060
Base Offset – 0x0000 0000

This non–volatile memory resource is configured as 8k x 8, but must be accessed in D32 mode. Only the data in the eight MSBs is considered valid for either read or write accesses. VMEbus masters access this resource, in the Global bus address range 0x00C0 0000 : 0x00CF FFFF. The 'C6x processors access this resource with the page register set for 0x0000 0060, also in D32 mode, with only the 8 MSB's valid.

5.3.5 'C6x Host Port Interfaces & HPI Control Registers

Global Bus Address Region – 0x00D0 0000 : 0x00DF FFFF
VMEbus A32 Address Region – A32_base+0x00D0 0000 : A32_base+0x00DF FFFF
VMEbus A24 Address Region – 0xD0 0000 : 0xDF FFFF

'C6x Address – 0x0188 0000 (HPI Control Register only)

The host–port interface (HPI) is a 16–bit wide parallel port which a host processor can use to directly access the CPU's memory space. The host device is the master of this interface, which makes access to it easier. As used herein, the term "host" generally refers to any processor on another VMEbus board (or an external computer acting as a VMEbus device, via an adapter board, ethernet interface, etc.) that has become master of the VMEbus and addresses the Model 4290/4291 as a VME slave. The host and DSP can also use memory located either internal or external to the DSP to exchange information. The host gains its direct access to memory–mapped peripherals via this interface. Connectivity to the DSP's memory space is provided through the DMA controller. Dedicated address and data registers, which are not accessible to the DSP, connect the HPI to the DMA auxiliary channel, which in turn connects the HPI to the DSP's memory space. Both the host and the DSP can access the HPI control register (HPIC). ONLY the host can access the HPI address register (HPIA), the HPI data register (HPID). The host uses the external data and interface control signals to access those registers and the HPIC.

The Model 4290/4291 provides a total of eight addresses in each of the four processing nodes that provide access to the Host Port interface registers. These are 16–bits registers, each of which is used for half of the 32–bit longword used internally by the 'C6x. Two pairs of registers are provided for access to the HPI data register of each node. One pair, intended for use during block transfers with the HPI, will automatically post–increment the address with each write operation. The other pair, intended for single longword transfers. will not.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.5 'C6x Host Port Interfaces & HPI Control Registers (continued)

Table 5–7, below, summarizes the resources that comprise the Host Port Interface, and gives the VMEbus addresses for each register in each node. Detailed descriptions of these resources can be found in Chapter 7 of Texas Instruments' ***TMS320C6000 Peripherals Reference Guide,*** TI document # SPRU 190D, published in February, 2001

Table 5–7: Model 4290/4291 –VMEbus Addresses for Host Port Interface Registers

VMEbus Address	Register Description
VME_base+00D0 0000	'C6x A Host Port Control Register 1st Halfword
VME_base+00D0 0004	'C6x A Host Port Control Register 2nd Halfword
VME_base+00D0 0008	'C6x A Host Port Data Register 1st Halfword*
VME_base+00D0 000C	'C6x A Host Port Data Register 2nd Halfword*
VME_base+00D0 0010	'C6x A Host Port Address Register 1st Halfword
VME_base+00D0 0014	'C6x A Host Port Address Register 2nd Halfword
VME_base+00D0 0018	'C6x A Host Port Data Register 1st Halfword**
VME_base+00D0 001C	'C6x A Host Port Data Register 2nd Halfword**
VME_base+00D1 0000	'C6x C Host Port Control Register 1st Halfword
VME_base+00D1 0004	'C6x C Host Port Control Register 2nd Halfword
VME_base+00D1 0008	'C6x C Host Port Data Register 1st Halfword*
VME_base+00D1 000C	'C6x C Host Port Data Register 2nd Halfword*
VME_base+00D1 0010	'C6x C Host Port Address Register 1st Halfword
VME_base+00D1 0014	'C6x C Host Port Address Register 2nd Halfword
VME_base+00D1 0018	'C6x C Host Port Data Register 1st Halfword**
VME_base+00D1 001C	'C6x C Host Port Data Register 2nd Halfword**
VME_base+00D2 0000	'C6x D Host Port Control Register 1st Halfword
VME_base+00D2 0004	'C6x D Host Port Control Register 2nd Halfword
VME_base+00D2 0008	'C6x D Host Port Data Register 1st Halfword*
VME_base+00D2 000C	'C6x D Host Port Data Register 2nd Halfword*
VME_base+00D2 0010	'C6x D Host Port Address Register 1st Halfword
VME_base+00D2 0014	'C6x D Host Port Address Register 2nd Halfword
VME_base+00D2 0018	'C6x D Host Port Data Register 1st Halfword**
VME_base+00D2 001C	'C6x D Host Port Data Register 2nd Halfword**
VME_base+00D3 0000	'C6x B Host Port Control Register 1st Halfword
VME_base+00D3 0004	'C6x B Host Port Control Register 2nd Halfword
VME_base+00D3 0008	'C6x B Host Port Data Register 1st Halfword*
VME_base+00D3 000C	'C6x B Host Port Data Register 2nd Halfword*
VME_base+00D3 0010	'C6x B Host Port Address Register 1st Halfword
VME_base+00D3 0014	'C6x B Host Port Address Register 2nd Halfword
VME_base+00D3 0018	'C6x B Host Port Data Register 1st Halfword**
VME_base+00D3 001C	'C6x B Host Port Data Register 2nd Halfword**

NOTES: In A24 VMEbus space, VME_base = 0
The HWOB (D0 in the HPI Control Register) determines the ordering (i. e., significance) of the 1st & 2nd halfwords
* - Address is auto-incremented by 4 byte addresses after every access
**- No auto-increment of address

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.5 'C6x Host Port Interfaces & HPI Control Registers (continued)

The Host Port Interface Control registers are normally the first registers accessed when using the Host Port. These set configuration bits and initialize the interface. The HPIC is organized as a 32–bit register whose high halfword and low halfword contents (with the exception of the FETCH bit, see below) are the same. On a host write, both halfwords must be identical. The low halfword and the high halfword are actually the same storage locations. No storage is allocated for the read–only, reserved values. Only CPU writes to the lower halfword affect HPIC values and HPI operation. Table 5–8, below, shows the contents of the HPIC, and the subsections that follow the table explain how the registers' bits are used.

Table 5–8: Model 4290/4291 - 'C6x Host Port Interface Control Registers

Bit #	D31 – D20	D20	D19	D18	D17	D16
Bit Name	Reserved	Reserved	HRDY	HINT	DSPINT	HWOB
Host Access	Read Only	R/W	R. O.	R/W	R/W	R/W
'C6x Access	Read Only	R. O.	R. O.	R. O.	R. O.	R. O.
Reset Value	0	0	0	0	0	0
Bit Function	Write with Zeros Mask when Reading		1 = Host Ready 0 = Hst Not Rdy	DSP Interrupt to Host	Host Interrupt to DSP	1 = MSB 2nd 0 = MSB 1st
Bit #	**D15 - D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved	FETCH	HRDY	HINT	DSPINT	HWOB
Host Access	Read Only	R/W	R. O.	R/W	R/W	R/W
'C6x Access	Read Only	R. O.	R. O	R/W	R/W	R. O.
Reset Value	0	0	1	0	0	0
Bit Function	Write with Zeros Mask when Reading	1 = Fetch 0 = No Fetch	1 = Host Ready 0 = Hst Not Rdy	DSP Interrupt to Host	Host Interrupt to DSP	1 = MSB 2nd 0 = MSB 1st

5.3.5.1 Half–Word Ordering Bits (HWOB) – D0 & D16

When these bits are set to the logic '1' state, the first halfword is least significant (D0 : D15). When these bits are cleared to the logic '0' state, the first halfword is most significant (D16 : D31). HWOB affects both data and address transfers. Only the host can modify this bit. HWOB must be initialized before the first data or address register access.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.5 'C6x Host Port Interfaces & HPI Control Registers (continued)

5.3.5.2 Interrupt to DSP from Host (DSPINT) – D1 & D17

The host can interrupt the 'C6x by setting the DSPINT bits in the HPIC to the logic '1' state. The DSPINT bit is tied directly to the internal DSPINT signal. By writing DSPINT = 1 when DSPINT = 0, the host causes a low–to–high transition on the DSPINT signal. If you program the selection of the DSPINT interrupt with interrupt selector, the transition of DSPINT is detected as an interrupt condition by the 'C6x. The DSP can clear the DSPINT bits by writing a 1 to DSPINT. Neither a host nor a 'C6x HPIC write with DSPINT = 0 affects the DSPINT bit or signal.

5.3.5.3 Interrupt to Host from DSP (HINT) – D2 & D18

The 'C6x can send an active interrupt condition to the host on its HINT pin by writing to the HINT bits in the HPIC. The HINT bit is inverted and tied directly to the $\overline{\text{HINT}}$ pin. The DSP can set $\overline{\text{HINT}}$ active by setting the HINT bit to the logic '1' state. The host can clear the $\overline{\text{HINT}}$ to inactive by writing a 1 to the HINT bits. Neither a host nor a CPU write to HPIC with HINT = 0 affects either the HINT bit or the $\overline{\text{HINT}}$ signal.

The HINT bit is read twice on the host interface side. The first and second half–word reads by the host can yield different data if the 'C6x changes the state of this bit between the two read operations.

5.3.5.4 Host Ready Bits (HRDY) – D3 & D19

This is the Ready signal to from the 'C6x to the host. It is not masked by $\overline{\text{HCS}}$ (as the $\overline{\text{HRDY}}$ pin is). When HRDY reads back in the logic '0' state, the internal bus is waiting for an HPI data access request to finish, and is therefore not ready.

5.3.5.5 Host Fetch Request (FETCH) – D4

This bit is used by the host to request a fetch operation by the 'C6x. The value read by the host or the 'C6x from this bit is always a logic '0'. The host sets this bit to the logic '1' state to request a fetch into the Host Port Interface Data register of the word at the address pointed to by Host Port Interface Address register.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.6 Global Bus Control Registers

Global Bus Address Region – 0x00E0 0000 : 0x00EF FFFF
VMEbus A32 Address Region – VME_base+0x00E0 0000 : VME_base+0x00EF FFFF
VMEbus A24 Address Region – 0xE0 0000 : 0xEF FFFF

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0070
Base Offset – 0x0000 0000

Three registers are accessible to VMEbus masters in this region, all of which are also accessible from the on–board 'C6x processors. Table 5–9, below, lists the register's names, and the addresses at which they are accessed, from both the V–bus and the Global bus. For further information about how to use these registers, please refer to the sub–sections indicated in the right–hand column of the table, which begin on the following page.

Table 5–9: Model 4290/4291 –Global Bus Control Registers

Register Name	Global Address	V-bus Address (Page Reg. = 70)	Additional Information
Global Dual Port SRAM Semaphore Register	0x00E0 0000	0x0000 0000	Section 5.3.6.1
General Purpose Global Semaphore Register	0x00E0 0004	0x0000 0004	Section 5.3.6.2
VME DSP Reset Control Register	0x00E0 0008	0x0000 0008	Section 5.3.6.3
NOTE: For VMEbus access, add the VME_base address to the Global bus address.			

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.6 Global Bus Control Registers (continued)

5.3.6.1 Global Dual Port SRAM Semaphore Register (DPSR)

Global Bus Address – 0x00E0 0000
VMEbus A32 Address – A32_base+0x00E0 0000
VMEbus A24 Address – 0xE0 0000

'C6x Address – 0x0000 0000
Page Register – 0x0000 0070
Base Offset – 0x0000 0000

Each Dual Port SRAM block is divided into four banks which are 'owned' by (i. e., accessible to) either the local 'C6x processor or whatever is the current master of the Global bus. At reset, the Global bus (which is, by default, granted to VME) owns the semaphores for all four banks in all four blocks. Before accessing any bank, however, any Global bus master should verify that it does indeed still own the semaphore it needs, by executing the Semaphore action sequence with the appropriate bit in the Dual Port Semaphore Register on the Global bus. This sequence is accomplished by performing a series of read and write accesses to the register. Once the semaphore is obtained for a given bank, transfers (read or write) may proceed. Write accesses to banks for which the semaphore is not owned by the master are ignored (although correctly acknowledged) and reads in the absense of semaphore ownership return non–deterministic data.

The Semaphore for each bank of the Dual Port SRAM is acquired and then released in a four step operation. The first step of the sequence is to check the availability of the semaphore. If you read a '0' in the appropriate bit position, the semaphore may be available and you may request it, by writing a '1' to that bit position. Ownership of the semaphore is then verified by reading a '1' in the bit position after the request operation. After use of the bank is completed, the controlling entity releases the semaphore by writing a '0' to it.

The programmer should be aware that separate, independent semaphore registers exist on each processor's V–bus (the Local Semaphore Registers, or LSRs), and on the Global bus. The four MSB's of a given processor's LSR (D15 : D12) represent the semaphores for that node's local DPSRAM block. When a semaphore is claimed via the V–bus register, the Global Semaphore register is NOT updated to reflect this, and neither is the appropriate processor's V–bus register updated when a Global bus master claims a semaphore. **The only way to know for certain if a particular semaphore is available is to try to get it.** Success indicates that it was available; failure to obtain it means that it wasn't.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.6 Global Bus Control Registers (continued)

5.3.6.1 Global Dual Port Semaphore Register (continued)

At any given time, a Dual Port SRAM bank can exist in one of three possible states:

1) The DPSRAM bank is owned by the local 'C6x processor, and is accessible via that DSP's V–bus. The bank is acquired by 'C6x through its Local Semaphore Register (LSR).

2) The DPSRAM bank is owned by a Global bus master (either VME or a 'C6x), and is accessible via the Global bus. The bank is acquired by the Global bus master through this register, the Global Dual Port Semaphore Register (DPSR).

3) The DPSRAM is not owned. By default, the Global bus master is granted access to the DPSRAM. Mastership of the Global bus is granted to VME at reset.

Table 5–10, below, shows the structure of the Global Dual Port SRAM Semaphore Register (DPSR). The upper 16 bits of this register's 32–bit memory location are unused. The remaining 16 bits are divided into four groups of four bits each, one group dedicated to each of the four DPSRAM blocks. One bit in each group controls the semaphore for one of the four banks in the associated block.

Table 5–10: Model 4290/4291 –Global Dual Port SRAM Semaphore Register (DPSR) – VMEbus A32 Access: R/W @ A32_base+0x00E0 0000 –VMEbus A24 Access: R/W @ 0xE0 0000 Global Bus Access: R/W @ 0x00E0 0000 –V-bus Access: R/W @ 0x0000 0000, Page Reg = 70

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Semaphore for . . .	DPSRAM_B _Bank_3	DPSRAM_B _Bank_2	DPSRAM_B _Bank_1	DPSRAM_B _Bank_0	DPSRAM_D _Bank 3	DPSRAM_D Bank 2	DPSRAM_D Bank 1	DPSRAM_D Bank 0
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Semaphore for . . .	DPSRAM_C _Bank_3	DPSRAM_C _Bank_2	DPSRAM_C _Bank_1	DPSRAM_C _Bank_0	DPSRAM_A _Bank 3	DPSRAM_A Bank 2	DPSRAM_A Bank 1	DPSRAM_A Bank 0

Semaphore Action Sequence –the following four–step sequence must be followed to obtain access to the Dual Port SRAM banks whose semaphores are controlled by the bits in this register –
Step **1** –**Read** a '**0**' in the associated bit **to check** the semaphore's **availability**
Step **2** - **Write** a '**1**' to the associated bit **to request ownership** of the semaphore
Step **3** - **Read** a '**1**' in the associated bit **to verify ownership** of the semaphore
Step **4** - **Write** a '**0**' to the associated bit **to release** the **semaphore** after completing the access.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.6 Global Bus Control Registers (continued)

5.3.6.2 Global Bus General Purpose Semaphore Register (GBSR)

Global Bus Address – 0x00E0 0004
VMEbus A32 Address – A32_base+0x00E0 0004
VMEbus A24 Address – 0xE0 0004

'C6x Address – 0x0000 0004
Page Register – 0x0000 0070
Base Offset – 0x0000 0000

Twelve additional, general purpose semaphores are provided on the Model 4290/4291, which may be assigned by the programmer to any shared resource on the board that may become a contended item. These semaphores are shared, on a bit–by–bit basis, between the four processing nodes and the VMEbus.

The GBSR is accessible to the VMEbus and to on–board DSPs when they master the Global bus, and is accessed at Global bus address 0x00E0 0004 (VME address VME_base+0x00E0 0004). The 'C6x's access this register by setting their page register to 0x0000 0070, and accessing address 0x0000 0004. The semaphores are contained in bits D11 : D0 of this register (bits D31 : D16 at this address are unused, and bits D15 :D12 are reserved). These sema–phores are accessed by the DSPs through the 12 LSBs (D11 : D0) of their Local Semaphore Registers (LSRs).

The general purpose semaphores are obtained in the same man–ner as the Dual Port SRAM semaphores. At the beginning of the sequence, reading a '0' in the associated bit indicates that the semaphore may be available, a '1' indicates that it is already known to be owned by some master. If the semaphore is avail–able, a '1' is written to the associated bit to request it. This is fol–lowed by reading the bit, to confirm that the semaphore has been granted to the requesting processor (automatically resolved by hardware during contention). If the associated bit reads back as a '1', the processor has obtained the semaphore. After performing all necessary accesses, the owning processor writes a '0' to the associated bit to release the semaphore, . At reset, all 12 general purpose semaphores are available.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.6 Global Bus Control Registers (continued)

5.3.6.2 Global Bus General Purpose Semaphore Register (continued)

Table 5–11, below, illustrates the structure of the Global Bus General Purpose Semaphore Register.

Table 5-11: Model 4290/4291 - Global Bus General Purpose Semaphore Register (GBSR) - VMEbus A32 Access: R/W @ A32_base+0x00E0 0004 - VMEbus A24 Access: R/W @ 0xE0 0004 - Global Bus Access: R/W @ 0x00E0 0004 - V-bus Access: R/W @ 0x0000 0004, Page Reg = 70

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Semaphore	Reserved				GP_Global_ Semaphore_ 11	GP_Global_ Semaphore_ 10	GP_Global_ Semaphore_ 9	GP_Global_ Semaphore_ 8
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D00**
Semaphore	GP_Global_ Semaphore_ 7	GP_Global_ Semaphore_ 6	GP_Global_ Semaphore_ 5	GP_Global_ Semaphore_ 4	GP_Global_ Semaphore_ 3	GP_Global_ Semaphore_ 2	GP_Global_ Semaphore_ 1	GP_Global_ Semaphore_ 0

Semaphore Action Sequence –the following four-step sequence must be followed to obtain access to the semaphores are controlled by the bits in this register –
Step **1** –**Read** a '**0**' in the associated bit **to check** the semaphore's **availability**
Step **2** - **Write** a '**1**' to the associated bit **to request ownership** of the semaphore
Step **3** - **Read** a '**1**' in the associated bit **to verify ownership** of the semaphore
Step **4** - **Write** a '**0**' to the associated bit **to release** the **semaphore** after completing the access.

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.6 Global Bus Control Registers (continued)

5.3.6.3 VME DSP Reset Control Register (VRCR)

Global Bus Address – 0x00E0 0008
VMEbus A32 Address – A32_base+0x00E0 0008
VMEbus A24 Address – 0xE0 0008

'C6x Address – 0x0000 0008
Page Register – 0x0000 0070
Base Offset – 0x0000 0000

This register was included to allow any or all of the Model 4290/ 4291's 'C6x processors to be reset from the VMEbus, although the register is also accessible to any device (including any on–board 'C6x processor) that can master the Global bus. Like the semaphore operations described in the sections above, the 'C6x reset requires a four–step sequence of operations on this register. Unlike the sema–phore operations though, all the accesses in the reset sequence are writes.

Bits D31 : D16 at this address are unused. Bits D15 : D12 comprise a processor reset enable field. Each of these four bits is associated with one of the DSPs, and only those processors whose associated bits are set to the logic '1' state in this field will respond to the reset operation. D11 : D9 are unused, and the 8 LSB's (D7 : D0) are the reset bits.

The reset sequence consists of four steps, as follows. First, the reg–ister should be cleared (i. e., write 0x0000 to it), to prepare it for the reset operation. The next three write operations will consist of '1's in the bits in the reset enable field (D15 :D12) for those processors you want to reset, '0's in bits D11 : D8, and the following data in the lower 8 bits (D7 : D0) – 0x88 (second write), 0x66 (third write) and 0x11 (fouth and final write).

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.6 Global Bus Control Registers (continued)

5.3.6.3 VME DSP Reset Control Register (continued)

EXAMPLE: The sequence detailed below would reset 'C6x pro–cessors B and C.

1) Write **0x0000** prepares the register to begin the reset sequence.

2) Write **0xA088** The '**A**' sets bits D15 & D13 to '1' (enabling processors B & C for reset), while '**088**' sets bits D7 and D3 to '1'.

3) Write **0xA066** The '**A**' sets bits D15 & D13 to '1' (enabling processors B & C for reset), while the '**066**' sets bits D6, D5, D2, and D1 to '1'.

4) Write **0xA011** The '**A**' sets bits D15 & D13 to '1' (enabling processors B & C for reset), while the '**011**' sets bits D4 and D0 to '1'.

Table 5–12, below, shows the bit structure of the VME DSP Reset Control Register.

Table 5-12: Model 4290/4291 - VME DSP Reset Control Register (VRCR) - VMEbus A32 Access: R/W @ A32_base+0x00E0 0008 - VMEbus A24 Access: R/W @ 0xE0 0008 - Global Bus Access: R/W @ 0x00E0 0008 - V-bus Access: R/W @ 0x0000 0008, Page Reg = 70

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Function	Reset_ Enable_B	Reset_ Enable_D	Reset_ Enable_C	Reset_ Enable_A	Reserved			
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Function	Reset_ Bit_#7	Reset_ Bit_#6	Reset_ Bit_#5	Reset_ Bit_#4	Reset_ Bit_#3	Reset_ Bit_#2	Reset_ Bit_#1	Reset_ Bit_#0

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5.3 VMEbus A24/A32 Slave Resources (continued)

5.3.7 VMEbus Master Access to the Global Expansion Bus Daughterboard

Global Bus Address Region – 0x0100 0000 : 0x0103 FFFF
VMEbus A32 Address Region – A32_base+0x0100 0000 : A32_base+0x0103 FFFF
VMEbus A24 Address Region – Not Accessible

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0080
Base Offset – 0x0000 0000

A32 VMEbus masters can access a daughterboard installed on the Model 4290/4291's Global Expansion Bus as a slave device, by conducting read and write opeartions to the memory region from A32_base+0x0100 0000 to A32_base+0x0103 FFFF. This region corresponds to the Global bus memory space from 0x0100 0000 to 0x0103 FFFF, which is accessed by the 'C6x in its V–bus address region from 0x0000 0000 to 0x001F FFFF, with the page register set to 0x80. This resource is not accessible from VMEbus A24 space.

5.4 Global Bus Arbitration

The arbitration scheme for the Model 4290/4291's Global bus is hierarchical in nature. The VMEbus occupies the top level of the hierarchy, and in a deadlock VME a higher priority than any of the processors. At the second level of the arbitration hierarchy are the four 'C6x processors. A round–robin scheme is employed among them, which assigns priority to each processor on a rotating basis. The processor that had Global mastership most recently gets the lowest priority. However, if a lower priority processor requests the bus while others are idle, it is immediately granted mastership. The 'C6x processors request the Global bus whenever it access its CE0 memory space with A21 asserted. The bus may be re–arbitrated after the current request has been rescinded. Global bus locking by the 'C6x's is supported through the use of the Global/VME bus lock bit (D1) of the Miscellaneous Interrupt Register (MIVR), at V–bus address 0x0028 0018 (see Section 4.3.2.4, on page 90). No Global bus lock bit is provided for VMEbus masters, however. Therefore, the only way that a VMEbus master can retain control of the Global bus is if the bus is idle, or through the use of the General Purpose Semaphore register (see Section 5.3.6.2).

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5.5 Mastering the VMEbus

Any 'C6x processor on the Model 4290/4291 that gains mastership of the board's Global bus can also become a VMEbus master. 'C6x access to VME is available in the Global bus window of the processor's CE0 address space (the memory region from 0x0000 0000 : 0x001F FFFF). The Global Bus Page Register, at V–bus address 0x0028 0024, selects which VME memory space will be accessed, as shown in Table 5–13, below. This table essentially provides a map from a given 'C6x V–bus address, via the page register, to the corresponding Global bus address.

Table 5-13: Model 4290/91 - VMEbus Master Access Regions for 'C6x Processors

VMEbus Address Space	Page Register Base Setting*	# of pages	Block Size	'C6x Address Region	Equivalent Global Bus Address Region
A16	0x0100	8	16 MBytes†	**0x0000 0000 : 0x001F FFFF**	0x0200 0000 : 0x02FF FFFF†
A24	0x0180	8	16 MBytes		0x0300 0000 : 0x03FF FFFF
A32	0x8000	2048	4 GBytes		0x1 0000 0000 : 0x1 FFFF FFFF

*** - Each 'C6x has a unique Global Bus Page Register, located at address 0x0028 0024 on its V-bus.**
† –Although VMEbus A16 space is only 64 kBytes deep, a considerably larger address region was assigned to this resource, in order to simplify the decode logic.

5.5.1 VMEbus Address Modifiers

The Model 4290/4291's VMEbus master interface operates ONLY in Super–visory Data mode. Table 5–14, below, lists the AM (Address Modifier) codes that can be generated by the Model 4290/4291 when operating as a VMEbus master.

Table 5–14: Model 4290/4291 –VMEbus Master Address Modifier Codes

VMEbus Address Space	Access Mode	AM Code
A16	Supervisory Data (8–, 16–, or 32–bit)	0x2D
A24	Supervisory Data (8–, 16–, or 32–bit)	0x3D
A32	Supervisory Data (8–, 16–, or 32–bit)	0x0D

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5.5 Mastering the VMEbus (continued)

5.5.2 Mastering A16 VMEbus Space

A 'C6x processor on the Model 4290/4291 that needs to gain master access to the VMEbus in A16 space must first write the code for A16 master access (0x0100), to its Global Bus Page Register, at V–bus address 0x0028 0024. The processor must then make an access to its Global Bus memory window, in the lower half of CE0 space (address range 0x0000 0000 : 0x001F FFFF), which will generate a request for master access to the 4290/4291's Global bus. If this request is granted, the 'C6x is then given control of the VIC64's VMEbus master interface in A16 mode, and may proceed with its data transfers. The user may take note of the fact that even though A16 VMEbus space is only 64 kBytes deep, a 16 MByte address region has been assigned for these accesses in the 'C6x memory map, to simplify the decode logic.

5.5.3 Mastering A24 VMEbus Space

A 'C6x processor on the Model 4290/4291 that needs to gain master access to the VMEbus in A24 space must first write a valid code for A24 master access (0x0180 : 0x187), to its Global Bus Page Register, at V–bus address 0x0028 0024. The processor must then make an access to its Global Bus memory window, in the lower half of CE0 space (address range 0x0000 0000 : 0x001F FFFF), which will generate a request for master access to the 4290/4291's Global bus. If this request is granted, the 'C6x is then given control of the VIC64's VMEbus master interface in A24 mode. At this point, the processor can directly access the VMEbus for single–cycle transfers (see Section 5.5.5), but block transfers are controlled by the VIC (see Section 5.5.6).

The user should be aware that the 'C6x's page register provides access to the 16 MBytes of VMEbus A24 space in eight pages of 2 MBytes each. Table 5–15, below, gives the A24 VMEbus addresses that are accessible for each 'C6x Page Register setting that points to VMEbus A24 space.

Table 5-15: Model 4290/4291 - 'C6x Address Translations in VMEbus A24 Space

Page Register Setting	'C6x Address Range	VMEbus Address Range
0x018y	0x00 0000 : 0x1F FFFF	0x00 0000 : 0x1F FFFF
0x019y		0x20 0000 : 0x3F FFFF
0x01Ay		0x40 0000 : 0x5F FFFF
0x01By		0x60 0000 : 0x7F FFFF
0x01Cy		0x80 0000 : 0x9F FFFF
0x01Dy		0xA0 0000 : 0xBF FFFF
0x01Ey		0xC0 0000 : 0xDF FFFF
0x01Fy		0xE0 0000 : 0xFF FFFF

NOTE: y = (0:3) = Setting of Byte Select field (see Table 4-25 & Section 4.3.2.7)

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5.5 Mastering the VMEbus (continued)

5.5.4 Mastering A32 VMEbus Space

A 'C6x processor on the Model 4290/4291 that needs to gain master access to the VMEbus in A32 space must first write a valid code for A32 master access (0x8000 : 0x87FF), to its Global Bus Page Register, at V–bus address 0x0028 0024. The processor must then make an access to its Global Bus memory window, in the lower half of CE0 space (address range 0x0000 0000 : 0x001F FFFF), which will generate a request for master access to the 4290/4291's Global bus. If this request is granted, the 'C6x is then given control of the VIC64's VMEbus master interface in A32 mode. At this point, the processor can directly access the VMEbus for single–cycle transfers (see Section 5.5.5), but block transfers are controlled by the VIC (see Section 5.5.6).

The user should be aware that the 'C6x's page register provides access to the 4 GBytes of VMEbus A32 space in 2,048 pages of 2 MBytes each. Table 5–16, below, gives the A32 VMEbus addresses that are accessible for selected 'C6x Page Register settings that point to VMEbus A32 space.

Table 5–16: Model 4290/4291 - 'C6x Address Translations in VMEbus A32 Space

Page Register Setting	'C6x Address Range	VMEbus Address Range
0x800y	0x0000 0000 : 0x001F FFFF	0x0000 0000 : 0x001F FFFF
0x801y		0x0020 0000 : 0x003F FFFF
0x802y		0x0040 0000 : 0x005F FFFF
0x803y		0x0060 0000 : 0x007F FFFF
0x804y		0x0080 0000 : 0x009F FFFF
0x805y		0x00A0 0000 : 0x00BF FFFF
0x806y		0x00C0 0000 : 0x00DF FFFF
0x807y		0x00E0 0000 : 0x00FF FFFF
0x808y		0x0100 0000 : 0x011F FFFF
⋮		⋮
0x80Fy		0x01E0 0000 : 0x01FF FFFF
0x810y		0x0200 0000 : 0x021F FFFF
⋮		⋮
0x81Fy		0x02E0 0000 : 0x02FF FFFF
0x820y		0x0400 0000 : 0x041F FFFF
⋮		⋮
0x87Fy		0x0FE0 0000 : 0x0FFF FFFF
0x880y		0x1000 0000 : 0x101F FFFF
⋮		⋮
0x8FFy		0x1FE0 0000 : 0x1FFF FFFF
0x900y		0x2000 0000 : 0x201F FFFF
⋮		⋮
0x9FFy		0x3EE0 0000 : 0x3FFF FFFF
0xA00y		0x4000 0000 : 0x401F FFFF
⋮		⋮
0xFFFy		0xFFE0 0000 : 0xFFFF FFFF

NOTE: y = (0:3) = Setting of Byte Select field (see Table 4–25 & Section 4.3.2.7)

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5.5 Mastering the VMEbus (continued)

5.5.5 Single Cycle Master Accesses

VME Master single cycle accesses are accomplished in the same manner as accesses to any other global bus resource. However, make sure you have set up the Global Bus Page Register prior to working with the bus. After the cycle is initiated the Global Bus is arbitrated (see Global Bus Arbitration, Section 5.4 for further detail). Once mastership of the bus has been awarded to the pro−cessor, the address and data (if necessary) are enabled onto the bus and decoded. The VME bus is arbitrated, and the transfer is completed. The cycle is completed by sending the READY signal back to the processor. In order to minimize the delays inherent in VMEbus arbitration and access, write accesses are write posted. This means that when the 'C6x writes to VME, the the VIC64 immediately latches the data and acknowledges the transfer from the DSP (thus freeing all involved local resources), even though it may not yet have been granted mastership of the VMEbus.

5.5.6 Block Transfer Master Accesses

The Model 4290/4291 supports D16, D32 and D64 master block transfers through the VIC64 device. The board−resident source or destination for the data transfer is either the Global SRAM block or one of the Dual Port SRAM banks. A semaphore should be used to make sure that only one processor is in control of the block transfer operation at a time. Once the transfer starts, the VIC requests the VMEbus and transfers the data once it has been granted mastership. When the transfer is completed, the processor that initiated the transfer can be interrupted.

5.5.7 Locking the VMEbus

In applications where a 'C6x processor on a given 4290/4291 needs exclu−sive master access to the VMEbus for a period of time (to conduct a block transfer, read−modify−write cycle, or other atomic access, for example), that processor can set the Global Bus / VMEbus Lock bit (D1 in the Miscel−laneous Interrupt & VMEbus Control Register, at V−bus address 0x0028 0018, see Section 4.3.2.4) to the logic '1' state. Setting this bit causes two things to happen. First, the on−board arbiter will be locked, such that no other device can master that board's Global bus. Also, the VIC64 will assert the VMEbus $\overline{\text{BBSY}}$ signal, which prevents any other VME device from obtaining the VMEbus.

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5.6 Interrupting the VMEbus

Any 'C6x processor on the Model 4290/4291 can issue a VMEbus interrupt, on any of the seven IRQ levels, by setting the appropriate bit in the VIC64's internal VMEbus Interrupt Request Status Register (VIRSR –see Section A.2.17), at Global bus address 0x00F0 0080 (see Table 4–9, on page 78). The bit arrangement of this register is shown in Table 5–17, below. To assert an interrupt at a given IRQ level, set the bit whose position matches the desired IRQ level (e. g., set D3 to interrupt on IRQ3), AND the Register Enable bit (D0) to the logic '1 ' state. Individual IRQs can be cleared by clear–ing the associated bit in this register to the logic '0 ' state. When the Register Enable bit (D0) is cleared to the logic '0 ' state, all IRQs are de–asserted and the 4290/4291 cannot interrupt VME. Note that by using this register, the 4290/4291 can issue simultaneous interrupts on multiple levels. For example, if you write the VIRSR with the data 0xF1, the VIC will assert $\overline{IRQ7}$, $\overline{IRQ6}$, $\overline{IRQ5}$ and $\overline{IRQ4}$.

Table 5–17: Model 4290/4291 –VIC64 Internal VME Interrupt Request Status Register (VIRSR) –R/W @ Global Bus Address 0x00F0 0080

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	$\overline{IRQ7}$	$\overline{IRQ6}$	$\overline{IRQ5}$	$\overline{IRQ4}$	$\overline{IRQ3}$	$\overline{IRQ2}$	$\overline{IRQ1}$	Register Enable
Bit Function	1 = Assert Interrupt Request on the indicated level 0 = No Interrupt Request asserted on the indicated level							1 = Enable 0 = Disable

Once a VMEbus interrupter has asserted its interrupt, the other role it must fill in the IACK cycle is to respond to the handler's acknowledgement of the interrupt with an appropriate Interrupt Vector. This facility is also provided via the VIC64, by use of the VMEbus Interrupt Vector Base Registers 1 through 7 (VIVBR(1:7)), located at the longword address boundaries between Global bus addresses 0x00F0 0084 and 0x00F0 009C (inclusive, see Table 4–9, on page 78). The number associated with each of these registers corresponds to the IRQ level that the register must supply the vector for during the IACK cycle. Thus these registers should be loaded with the addresses of the appropriate vector routines at initialization, or at some point prior to the first assertion of the associated IRQ.

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5.7 Handling Interrupts from the VIC64 and VMEbus

The EXT_INT4 interrupt input to each 'C6x processor is associated with interrupts that cause the state of the VIC64 VMEbus Interface Controller's IPL lines to change. These sources include Local Interrupts, VIC64 resident mailboxes, error conditions, and general status (such as DMA completion), in addition to VMEbus interrupts. Unlike the other 'C6x interrupt sources, each of which has a unique source for each processor, the EXT_INT4 interrupt sources are common to all processors, and have the ability to interrupt any or all of the processors. Because of this, significant additional logic is required to control the IPL destinations and the possibility that additional interrupts may occur before the current interrupt has been acknowledged.

The EXT_INT4 control logic consists of four logic blocks that sit between the 19 potential VMEbus interface related interrupt sources and the EXT_INT4 inputs of each processor. The block diagram contained in Figure 5–1, below, shows the data flow between the blocks that make up the interface. The first stage of the EXT_INT4 processing logic, the IRQ to IPL mapper, is contained within the VIC64 and handles the mapping of interrupt sources to IPL levels. The second stage of logic is contained in a programmable logic device on the 4290/4291 board, and handles the conversion of individual IPL codes to an edge–triggering interrupt signal that can be presented to the EXT_INT4 interrupt control logic for any or all of the 'C6x processors. The third stage of logic controls the IACK management between the processors and the VIC64. The fourth block of the interface contains the enable logic common to all of the interrupt inputs, and determines whether or not the conditioned interrupt signal reaches a given processor.

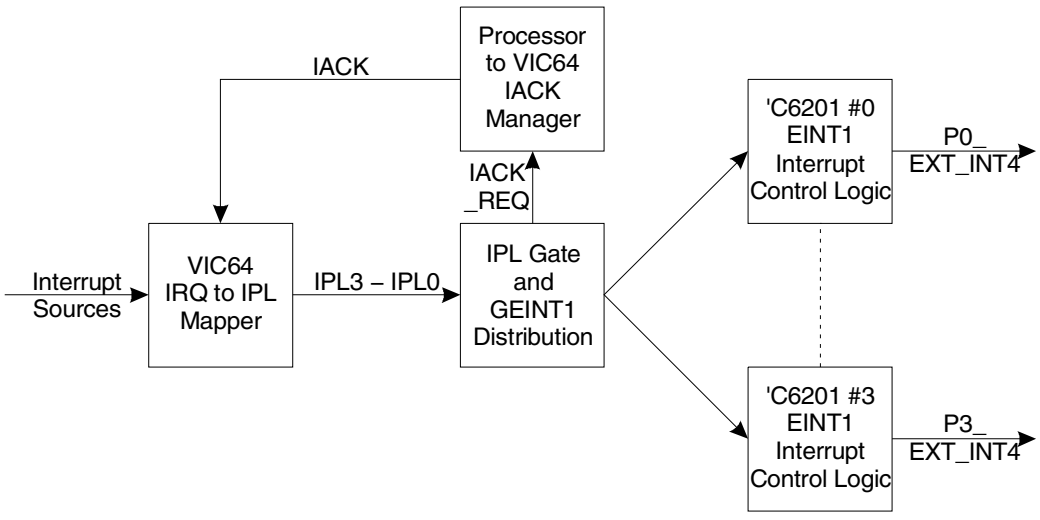


Figure 5–1: Model 4290/4291 –VME Interrupt Logic Control Flow Diagram

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5.7 Handling Interrupts from the VIC64 and VMEbus (continued)

The VIC64's IRQ to IPL mapper logic block is responsible for encoding the 19 possible interrupt sources onto the IPL outputs that are presented to the IPL gate logic. The IRQ to IPL mapper can route each interrupt or interrupt group to any of the seven LICR registers (LICR1–LICR7). The contents of these registers are loaded by processor A after reset. Once programmed, the IPL lines reflect the states of the highest ranked interrupt source. Table 5–18, at the top of the next page, lists the 19 possible interrupt sources and their respective priorities.

The IPL Gate and GEINT1 Distribution logic converts the IPL code received from the VIC64 into a pulsed interrupt that drives the EXT_INT4 Interrupt control logic for each processor. This logic performs gating functions based on the contents of each processor's Gating Register and the state of the IACK (interrupt acknowledge) manager. The format of each IPL Gating Control Register (IGCR) is shown in Table 5–19, at the bottom of the page after next. Each processor has a unique copy of this register located at the same V–bus address (0x0028 0100), and can only see its own copy of the register. Each bit in the register is assigned to a given IPL code. If the bit associated with that IPL code is set, then the GEINT1 output to that processor is pulsed when the associated IPL code is presented and no other interrupts at a higher–priority IPL level are outstanding.

This results in the associated flag being set in that processor's Interrupt Pending Register (the logical equivalent of a flag register). Multiple processors may be enabled to respond to a given IPL code. If no outstanding interrupt for a given IPL level is present, the interrupt acknowledge logic fetches the interrupt vector from the appropriate Interrupt Vector Register (IVR0:7, at V–bus addresses 0x0028 0108 (IVR0) through 0x0028 0120 (IVR7)) and latches it into the VIC64. Once the vector is latched, the interrupt is sent to the processor enable logic.

However, there is a software consideration with this scheme. The VMEbus specification requires support for multiple nested interrupts, and this scheme unfortunately creates a period of time during which an interrupt pulse might be missed by the processor. This is the interval following the assertion of an interrupt and before that interrupt is acknowledged. If a new interrupt is asserted during this period, the 'C6x might not detect it. However, a hardware feature has been provided to allow the interrupt service routine to handle this condition and essentially recover any missing interrupts. During the interrupt acknowledge cycle, the processor should read the contents of its VMEbus Interrupt Pending Register (VIPR, at V–bus address 0x0028 0104). The contents of this register will indicate if one or more additional, unacknowledged interrupts exist, even though the processor can only respond to one interrupt at a time. After servicing the highest priority interrupt, the processor should reread the VIPR, and see if it contains a non–zero value. If so, the processor has another interrupt that it must service, and this sequence is repeated until reading the VIPR returns a zero. Because the pending interrupt information is latched, and subsequent interrupts at that level are gated via the IACK controller, interrupts are not lost.

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5.7 Handling Interrupts from the VIC64 and VMEbus (continued)

Table 5–18: Model 4290/4291 –VME Interrupt Source & Ranking		
Priority Rank	**Interrupt Description**	**Interrupt Source**
1	LIRQ7	DPSRAM B Mailbox
2	Error Group Interrupt	—
3	LIRQ6	DPSRAM D Mailbox
4	LIRQ5	DPSRAM C Mailbox
5	LIRQ4	DPSRAM A Mailbox
6	LIRQ3	Global Daughterboard
7	LIRQ2	Not Used
8	LIRQ1	Local Bus Error
9	ICGS Group Interrupt	VIC64 Interrupts
10	ICGS Group Interrupt	
11	$\overline{\text{IRQ7}}$	
12	$\overline{\text{IRQ6}}$	
13	$\overline{\text{IRQ5}}$	
14	$\overline{\text{IRQ4}}$	
15	$\overline{\text{IRQ3}}$	
16	$\overline{\text{IRQ2}}$	
17	$\overline{\text{IRQ1}}$	
18	DMA Status / Complete Interrupt	—
19	VME Interrupt Acknowledge	—

The Processor to VIC64 IACK Manager is responsible for IACK servicing and vector passing between the multiple 'C6x processors and the VIC64. Additionally, by working with the IPL Pending logic, this block effectively limits the flow of interrupts heading to the processors, such that each has only one interrupt to deal with at any given time. Because the VIC64 only expects one response from one processor for any given interrupt, once an acknowledge is sent back to the VIC64, the vector associated with it is lost forever. Therefore, a latch is employed for each IPL level, to retain the state of the vector until all of the processors have a chance to respond. Also, no additional interrupts for a given IPL level can be passed until the previous interrupt at that level has been fully acknowledged, or an interrupt overrun condition would occur, which could again result in the loss of one or more interrupts.

Because an interrupt vector is lost once a single IACK cycle has been performed by the VIC64, the IACK control logic must latch the value presented by the VIC64 during the first IACK for the eight possible IACK cycles coming from the processors. Once the control logic determines that an IPL code can be acknowledged, it asserts a global bus request. After gaining control of the bus, the control logic performs an interrupt acknowledge cycle, latches the interrupt vector byte for the specific IPL code into its associated Interrupt Vector Register, updates the associated Interrupt Pending Register byte, then releases the Global bus.

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5.7 Handling Interrupts from the VIC64 and VMEbus (continued)

The IACK Manager operates based on the contents of the VIPR. When the register is initially loaded, at the beginning of the IACK cycle, each bit that is set in the IGCR will also be set in the VIPR. As the processor performs the IACK cycle, by reading the appropriate Interrupt Vector Register (IVR*n*, where *n* represents the IPL code), the bit position associated with the IPL code of the interrupt being serviced gets reset. The processor polls this register at the conclusion of the IACK cycle, to determine which interrupts have been serviced and if any other interrupts have occurred between when the original interrupt was asserted and when it was acknowledged.

The value in the VIPR is also used by the IACK manager to determine when a new IPL code can be acknowledged. If the value of the bit (one bit is associated with each IPL) for a specific IPL code is non−zero when that code is presented to the IPL gate logic, it indicates that the previous interrupt at that IPL code has not been acknowledged by all enabled processors. Therefore, an acknowledge can not occur or an interrupt overrun (and loss) will occur. If all of the bits associated with a given IPL are '0' when the VIPR is read, the IACK Manager arbitrates for the Global bus, acknowledges the interrupt, loads the vector, and the VIPR bits associated with the IPL code are loaded based on the contents of the associated IGCR bits. This allows multiple processors to respond to multiple outstanding interrupts without interrupt or vector loss. The registers involved in this process are described in the subsections that begin below.

5.7.1 VME Interrupt Gating Control Register (IGCR)

'C6x Address − 0x0028 0100

The VIC 64 on the Model 4290/4291 responds to VMEbus Interrupt Requests (IRQs) on a given level by generating local Interrupt Pending signals (IPLs) on the corresponding level. This register is used when a 'C6x processor acts as a VMEbus interrupt handler, to determine which IPL signals the DSP can respond to. Setting a bit in this register to the logic '1' state allows the corre−sponding IPL signal to set the associated bit in the VME Interrupt Pending Register (VIPR, at V−bus address 0x0028 0104 − see Section 5.7.2, on the next page). Whether or not an IPL that does get passed to the Interrupt Pending Register actually results in an interrupt to the DSP is determined by the state of the associated bit in the VME Interrupt Enable Register (VIER, at V−bus address 0x0028 0124 − see Section 5.7.3, on the page after next). Each 'C6x has a unique copy of this register. When the Model 4290/4291 is booted or reset, this regis−ter has a value of 0x0000, which means that no IPL signals are passed to the Interrupt Pending Register. Table 5−19, below, shows the bit structure of the IGCR.

Table 5−19: Model 4290/4291 −VME Interrupt Gating Control Register (IGCR) −R/W @0x0028 0100

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IPL_7_Gate	IPL_6_Gate	IPL_5_Gate	IPL_4_Gate	IPL_3_Gate	IPL_2_Gate	IPL_1_Gate	Reserved
Bit Function	1 = Pass IPL Signal to Interrupt Pending Register 0 = Do Not Pass IPL Signal to Interrupt Pending Register							Write '0' Mask on Reads
All bits in this register are cleared to the logic '0' state by boot and reset operations.								

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5.7 Handling Interrupts from the VIC64 and VMEbus (continued)

5.7.2 VME Interrupt Pending Register (VIPR)

'C6x Address – 0x0028 0104 (Read Only)

The VIC64 on the Model 4290/4291 responds to VMEbus Interrupt Requests (IRQs) on a given level by generating local Interrupt Pending signals on the corresponding level (IPLs). This Read–Only register is used when a 'C6x processor acts as a VMEbus interrupt handler, to latch those IPLs that are passed by the Interrupt Gating Control Register (IGCR, at V–bus address 0x0028 0100, see Section 5.7.1, on the previous page). A logic '1' in any bit position in this register indicates that the IGCR has passed the IPL at the corresponding level from the VIC64. Whether or not the bits that become set in this register will generate an interrupt to the 'C6x depends upon the state of the corresponding bits in the Interrupt Enable Register (VIER, at V–bus address 0x0028 0124 – see Section 5.7.3, on the next page). This register may also be polled, allowing the 'C6x to monitor the states of IPLs that are not enabled for interrupt generation. Table 5–20, below, shows the bit structure of the VIPR. Figure 5–2, at the bottom of this page, shows the resources involved in passing a VMEbus IRQ to a 'C6x processor on the Model 4290/4291.

Table 5–20: Model 4290/4291 –VME Interrupt Pending Register (VIPR) –R. O. @0x0028 0104

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IPL_7_ Pending	IPL_6_ Pending	IPL_5_ Pending	IPL_4_ Pending	IPL_3_ Pending	IPL_2_ Pending	IPL_1_ Pending	Reserved
Bit Function	1 = IPL Interrupt Pending 0 = No IPL Interrupt Pending							Write '0' Mask on Reads
All bits in this register are cleared to the logic '0' state by boot and reset operations.								

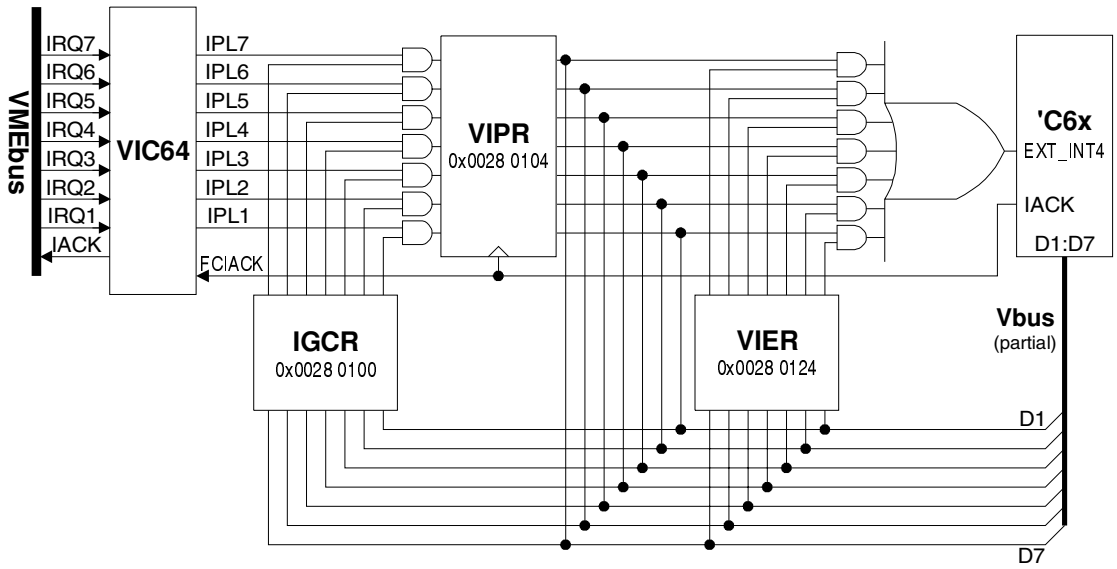


Figure 5-2: Model 4290/4291 - VMEbus Interrupt Path to 'C6x's

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5.7 Handling Interrupts from the VIC64 and VMEbus (continued)

5.7.3 VME Interrupt Enable Register (VIER)

'C6x Address – 0x0028 0124

The VIC 64 on the Model 4290/4291 responds to VMEbus Interrupt Requests (IRQs) on a given level by generating local Interrupt Pending signals (IPLs) on the corresponding level. This register is used when a 'C6x processor acts as a VMEbus interrupt handler, to determine which IPL signals will be allowed to interrupt the DSP. Those VMEbus interrupts that are allowed to propagate all the way through the register chain to the DSP (see Figure 5–2, on the previous page) are delivered to the EXT_INT4 input of the 'C6x. To enable a given IPL to interrupt the DSP, set the associated bit in this register to the logic '1' state. A VMEbus IRQ can cause an interrupt to a 'C6x processor on the Model 4290/4291 **ONLY** when the following conditions are met:

1) The corresponding bit in the VME Interrupt Gating Control Register (IGCR, at V–bus address 0x0028 0100 – see Section 5.7.1, on page 147) is set to the logic '1' state.

2) The corresponding bit in this register (the VIER) is set to the logic '1' state.

3) **FOR OPTION 330 ONLY**: All four bits in the EXT_INT4 field of Interrupt Mapping Register 0 (D0 : D3 of IMR0, at V–bus address 0x0028 0030 – see Section 4.3.2.9 on page 101) are cleared to the logic '0' state.

Table 5–21, below, shows the bit structure of the VIER.

Table 5–21: Model 4290/4291 –VME Interrupt Enable Register (VIER) –R/W @0x0028 0124

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IPL_7_ Enable	IPL_6_ Enable	IPL_5_ Enable	IPL_4_ Enable	IPL_3_ Enable	IPL_2_ Enable	IPL_1_ Enable	Reserved
Bit Function	1 = Interrupt Enabled 0 = Interrupt Disabled							Write '0' Mask on Reads
All bits in this register are cleared to the logic '0' state by boot and reset operations.								

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Chapter 6: Bi–FIFO Operations on the Model 4290/4291

6.1 Overview of Bi–FIFOs on the Model 4290/4291

The three Bi–directional FIFOs connected to each 'C6x's Local bus (V–bus) provide a powerful resource for the exchange of data with the other processors on the board, and with the VIM I/O expansion module. The flag outputs of these Bi–FIFOs are connected to the board's interrupt structure, to allow for tight programming control of data transfers in and out of these devices. Additionally, since each processor's port to any given Bi–FIFO is available only to that particular processor, arbitration is never required for access.

Figure 6–1, on the next page, provides a simplified illustration of the inter–processor Bi–FIFO paths (this is a reprint of Figure 4–2). We have (somewhat arbitrarily) chosen the designations XX and ZZ to distinguish between the two inter–processor Bi–FIFO ports available to each processor. We will also make reference in our discussions in the subsections that follow, to "upstream" and "downstream" access directions, which essentially refer to the J–TAG signal path. Thus, a downstream access means an exchange of data with the processor that preceeds the one in question in the J–TAG path, while an upstream access is an exchange with the next processor on the J–TAG path. (The J–TAG path is illustrated as the dashed lines in Figure 1–1, the Model 4290/4291 block diagram, on page 25 of this manual.) An upstream access would be an access in the clockwise direction in Figure 6–1, while a downstream access would go counterclockwise in the figure. As the figure shows, the XX (or upstream) Bi–FIFO for Processor A is the same physical device as the ZZ (or downstream) Bi–FIFO for Processor C.

Each Bi–FIFO physically contains two internal FIFO structures, one in each direction. The depth of all the internal FIFOs is 4 kBytes (1k x 32) in the standard configurations. In Option 321, the internal FIFOs for the VIM interface are all 64 kBytes deep (16k x 32), while the internal inter–processor FIFOs retain the 4 kbyte (1k x 32) depth. On units equipped with Option 320, all internal FIFOs are 64 kbytes (16k x 32) deep.

Additionally, each of the three Bi–directional FIFOs contains a mailbox, used for message passing, and also connected to the board's interrupt structure. If a given Bi–FIFO port's mailbox interrupt is enabled, the processor that "owns" that port will be interrupted whenever data is written to that mailbox.

Access to the Bi–FIFOs is handled differently on 4290/4291's equipped with Option 330 from the implementation used on units without that option. In the context of Bi–FIFO (and Bi–FIFO mailbox) access, when the term "standard" is used, it means any Model 4290/4291, with any combination of options that does NOT include Option 330. The differences in how the Bi–FIFOs are accessed on standard units and Option 330 units will be discussed in the subsections that begin on the page after next. Option 330 does NOT pertain to the size of the Bi–FIFO, i. e., this option may be combined with the Bi–FIFO depth options listed above. Note that Figure 6–1 applies to ALL Model 4290/4291's, with and without Option 330.

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6.1 Overview of Bi–FIFOs on the Model 4290/4291 (continued)

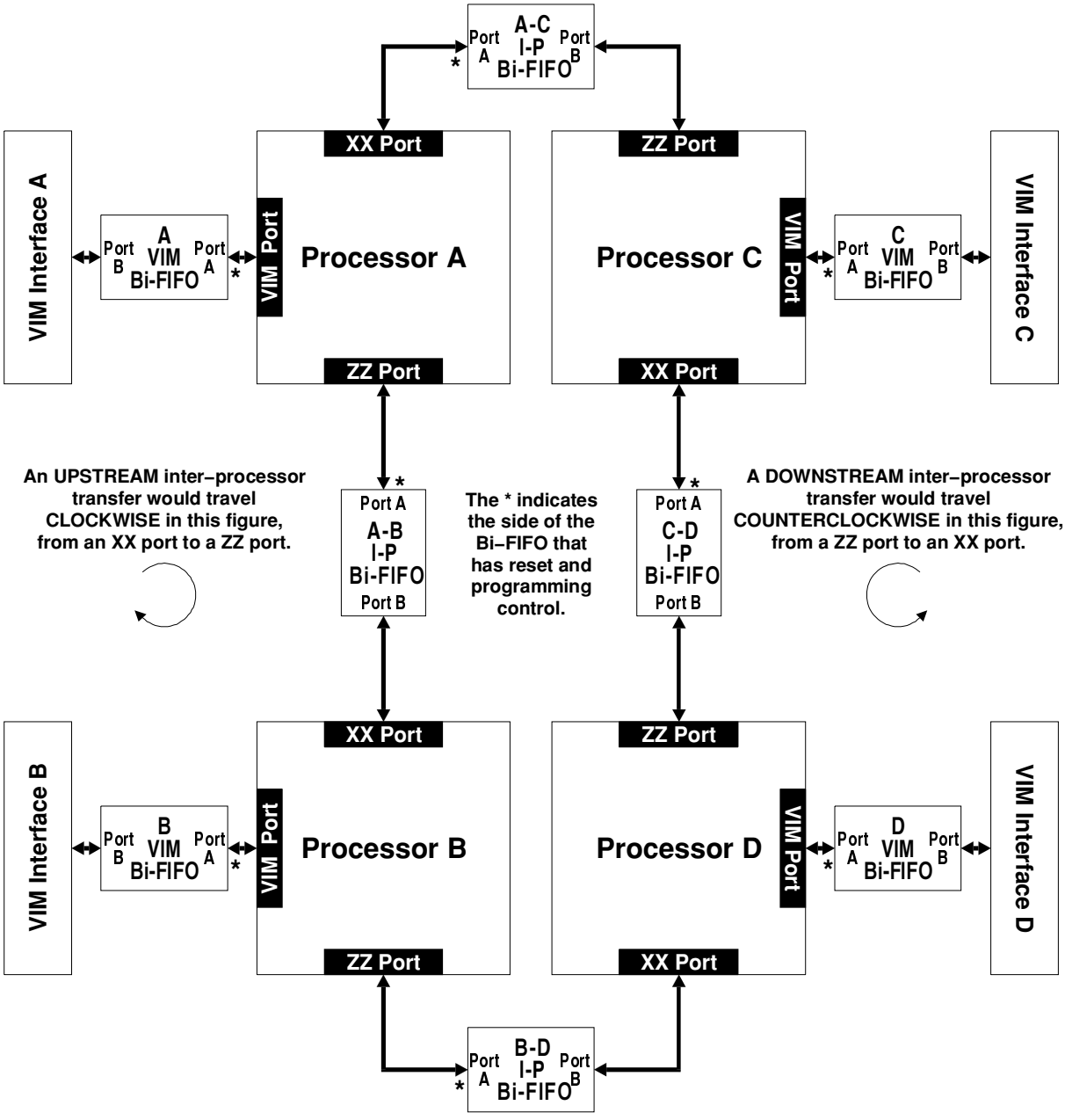


Figure 6–1: Model 4290/4291 –Inter–Processor & VIM Bi–FIFO Access Paths

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6.1 Overview of Bi–FIFOs on the Model 4290/4291 (continued)

6.1.1 Bi–FIFO Access on the Standard Model 4290/4291

Access to all three of the Bi–directional FIFOs connected to each processor's Local Bus is provided in the same address range, from 0x0100 0000 to 0x011F FFFF. Selection of a specific Bi–FIFO is accomplished using two bits (D15 & D14) in the Miscellaneous Control Register (MCR0), at address 0x0028 001C. Setting D15 in MCR0 to the logic '1' state selects the VIM Bi–FIFO, regardless of the state of D14. When D15 is cleared to the logic '0' state, then the state of D14 determines which one of the inter–processor Bi–FIFOs is selected. When both bits are cleared, the upstream, or XX Bi–FIFO port is selected. When D14 is set to the logic '1' state (with D15 = 0), the downstream, or ZZ Bi–FIFO port is selected. Table 6–1, below, summarizes these settings.

Table 6–1: Standard Model 4290/4291 –Bi–FIFO Selection

D15*	D14*	Bi–FIFO Selected	Path Enabled
0	0	XX (Upstream) Port	A -> C or C -> D or D -> B or B -> A
0	1	ZZ (Downstream) Port	A -> B or B -> D or D -> C or C -> A
1	0	VIM	Any Processor to its own Mezzanine Interface
1	1		

*** –These bits are located in the Miscellaneous Control Register (MCR0), at 'C6x Local bus address 0x0028 001C**

6.1.2 Bi–FIFO Mailbox Access on the Standard Model 4290/4291

As with the Bi–FIFOs themselves, accesses to all three mailboxes are performed in a single memory region, from 0x0120 0000 to 0x013F FFFF. The same two bits in the Miscellaneous Control Register (D15 & D14 in MCR0, at address 0x0028 001C) that are used to select one of the three Bi–FIFOs are also used, in the identical manner, to select one of the three mailboxes. These settings are shown in Table 6–1, above. Remember that while the Bi–FIFOs themselves are accessed in the memory range from 0x0100 0000 to 0x011F FFFF, their mailboxes are accessed in the address range from 0x0120 0000 to 0x013F FFFF.

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6.1 Overview of Bi–FIFOs on the Model 4290/4291 (continued)

6.1.3 Bi–FIFO Access on the Model 4290/4291 Option 330

When the Model 4290/4291 is equipped with Option 330, the memory map is changed such that each of the three Bi–FIFOs connected to each processor (and its associated mailbox, see below) occupies a unique, 256 kByte range of adresses in the associated processor's memory map. Thus, what were the Bi–FIFO select bits in the Miscellaneous Control Register (D15 & D14 @ MCR0, 0x0028 001C) in the standard configuration are "Reserved" in Option 330. While the Bi–FIFOs are mapped into CE1 space in the standard configuration, in Option 330 they are mapped into CE3 space. Essentially, in Option 330, the Bi–FIFOs and the SBSRAM exchange the memory spaces that they occupied in the standard configurations. Table 6–2, below, lists the BI–FIFO resources and the address regions that they occupy on a 4290/4291 Option 330.

Table 6–2: Model 4290/4291 Option 330 –Bi–FIFO Memory Map

'C6x Address Range	Resource
0x0300 0000 - 0x0303 FFFF	Bi–FIFO XX (Upstream)
0x0304 0000 - 0x0307 FFFF	Bi–FIFO XX Mailbox (Upstream)
0x0308 0000 - 0x030B FFFF	Bi–FIFO ZZ (Downstream)
0x030C 0000 - 0x030F FFFF	Bi–FIFO ZZ Mailbox (Downstream)
0x0310 0000 - 0x0313 FFFF	VIM Bi–FIFO
0x0314 0000 - 0x0317 FFFF	VIM Bi–FIFO Mailbox
NOTE: Option 330 relocates all these resources to CE3 space	

6.1.4 Bi–FIFO Mailbox Access on the Model 4290/4291 Option 330

On the Model 4290/91 Option 330, each Bi–FIFO mailbox is accessed in a unique, 256 kByte region of the associated 'C6x's memory map. The XX (upstream) Bi–FIFO is accessed in the address range from 0x0304 0000 through 0x0307 FFFF, the ZZ (downstream) Bi–FIFO is accessible from 0x030C 0000 through 0x030F FFFF, and the VIM Bi–FIFO can be found between 0x0314 0000 and 0x0317 FFFF. These addresses ranges are also summarized in Table 6–2, above.

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6.1 Overview of Bi–FIFOs on the Model 4290/4291 (continued)

Once the desired Bi–FIFO is selected or addressed, the device's own architecture guarantees that the access occurs in the proper manner. This means that for any write operation to any Bi–FIFO's memory or mailbox space, the data will always be placed in the outgoing side of that Bi–FIFO. Similarly, for any read operation from any Bi–FIFO's memory or mailbox space, the data is always taken from the incoming side of that Bi–FIFO. Although the Bi–FIFO has only one port at each side to read and write to, it has been mapped over a range of addresses. This facilitates DMA operations, which generally use an incrementing address. Writing to ANY address within the Bi–FIFO's memory space will place the data into the next available memory location within the FIFO. Reading from ANY address within the Bi–FIFO's memory space will access the data currently available at the Bi–FIFO's output. The preceding statements also apply to the Bi–FIFO mailboxes. Reading or writing any address in the mailbox memory region will appropriately access the incoming or outgoing mailbox. Figure 6–2, below, shows the internal architecture if the Bi–FIFOs used on the Model 4290/4291 (inside the dashed box), and also illustrates the connections between two processors and the inter–processor Bi–FIFO that they share.

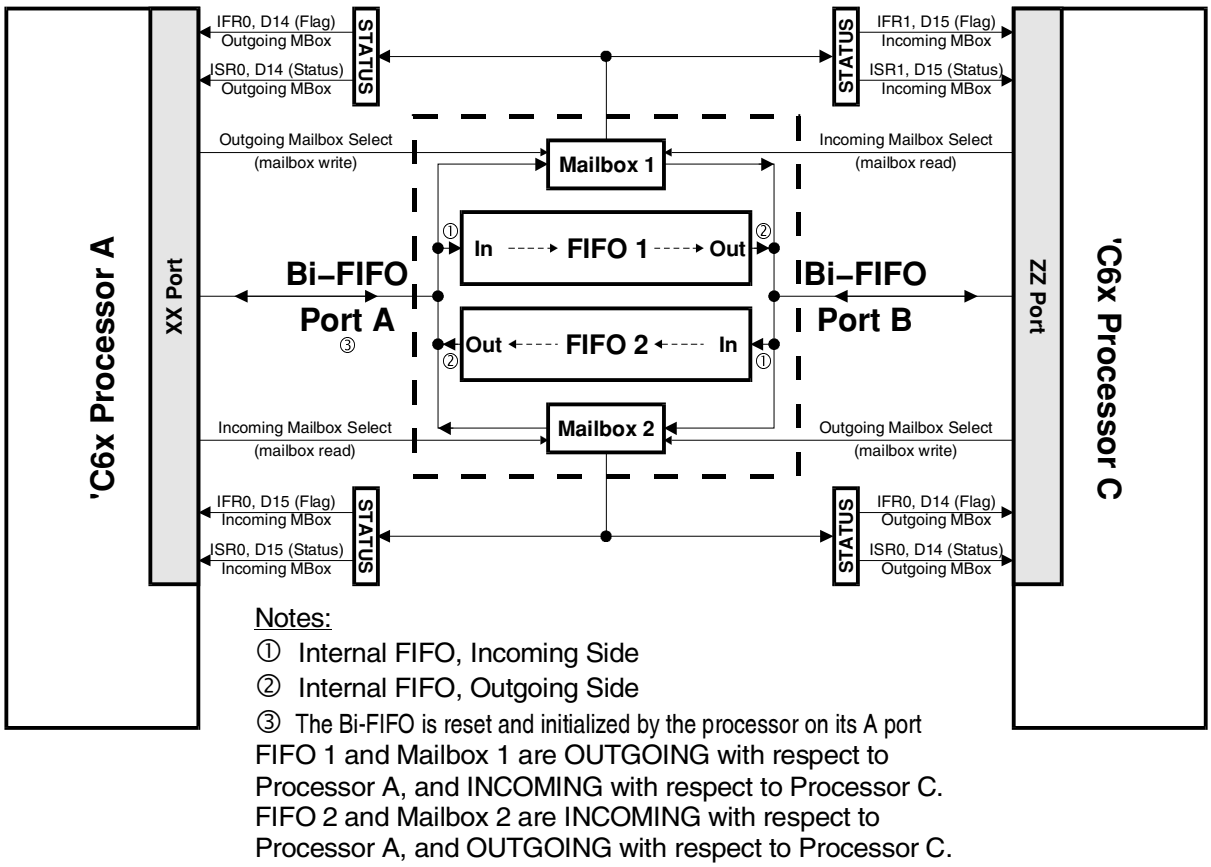


Figure 6–2: Model 4290/4291 –Bi–FIFO Architecture & Inter–Processor Connectivity

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6.2 Resetting the Bi–directional FIFOs

Each Bi–FIFO path may be individually reset under software control. Reset of the paths is accomplished by setting and clearing the Bi–FIFO reset bits (D10 : D12 in the Miscel–laneous Control Register (MCR0), at each processor's Vbus address 0x0028 001C. If the bit associated with a given Bi–FIFO is set but not cleared, that Bi–FIFO will be held in its reset state (no data in either FIFO, mailboxes empty, Empty & Almost Empty flags true, Almost Full& Full flags false).

When the Model 4290/4291 board is booted or reset, the Bi–FIFOs are also reset, and the almost empty and almost full threshold values for both FIFOs within the Bi–FIFO are initialized to the default value of 512, which is half the depth of each FIFO within the standard Bi–FIFO.

Table 6–3, below, specifies which bit is used to reset which Bi–FIFO path.

Table 6–3: Model 4290/4291 –Bi–FIFO Reset Bits – Misc. Control Register (MCR0) @ 0x0028 001C

MCR0 Bit	Bi–FIFO Path Reset
D12	Bi–FIFO Path ZZ
D11	Bi–FIFO Path XX
D10	VIM Bi–FIFO
See Table 4–20 and Section 4.3.2.5 for the complete layout and description of MCR0	

Referring to Figure 6–1, on page 152 of this manual, one can see that each processor is connected to either the A side or B side of each Bi–FIFO. All Bi–FIFO Reset and Ini–tialization operations are performed by the processor connected to the Bi–FIFO's A port. All processors are connected to the A side of their respective VIM Bi–FIFOs and are responsible for the reset and initialization of those components. With respect to the inter–processor Bi–FIFOs, the rule is that the processor with the lower alphabetical designation is connected to the A port of the Bi–FIFO, and is thus responsible for reset and initialization of that device.



Processors do NOT need to use Bi–FIFO Select bits in MCR0 (D15 : D14) to select a particular Bi–FIFO in order to reset it. The Bi–FIFO Select bits have no effect during Bi–FIFO Reset operations.

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6.3 Initializing the Bi–FIFO Structure

After the Bi–FIFO is reset, the programmable flag threshold levels (i. e., the levels at which the Bi–FIFO is considered Almost Empty and/or Almost Full) need to be initialized. This is accomplished by the first four writes to the A side of the Bi–FIFO, which is the same side of the Bi–FIFO responsible for its reset. Even if you have no plans to use the flags, four dummy writes must occur before data transfers, since the first four writes to the A side of the Bi–FIFO are **ALWAYS** loaded into these registers, rather than being placed in the FIFO data pipeline. The valid programming ranges for the flag threshold levels range from decimal 1 to 1023 for 1 kByte internal FIFOs (all the FIFOs on standard units, and the inter–processor FIFOs on Option 321), and from 1 to 16383 for 16 kByte internal FIFOs (All FIFOs in Option 320, and the VIM FIFOs in Option 321). The binary representations of the almost empty flag and almost full flag threshold levels for the internal FIFOs are written by the 'C6x processor on the least significant bits of the data bus, with the most significant digit of the binary number in D9 for the 1k internal FIFOs, or in D13 for the 16k internal FIFOs. After the first four writes that establish the flag threshold values, the structure is now ready to accept data. The procedure for calculating these threshold values, and the order in which they must be written to the Bi–FIFOs are given in Section 6.3.1, on the next page.

Because the data path is exercised during the programming of the flag levels, the Bi–FIFO select bits (D14 & D15 in the Miscellaneous Control Register (MCR0) @ V–bus address 0x0028 001C) must be set to select the desired Bi–FIFO before attempting to set these levels on standard (i. e., non–Option 330) units. Any address within the Bi–FIFO memory space, with the exception of the mailbox space, is valid for this initialization. When the Model 4290/4291 itself is reset (or booted), all flag thresholds are set to the default value of 512, or half the depth of the standard internal FIFOs. This also applies to the 16 kByte internal FIFOs in Options 320 and 321 (i. e., the boot code does not handle the deeper Bi–FIFOs differently).

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6.3 Initializing the Bi–FIFO Structure (continued)

6.3.1 Setting Bi–FIFO Thresholds

As mentioned in the previous section, the first four writes to the A port any Bi–FIFO following a reset will be sent to the internal flag threshold level registers, rather than to the FIFO data pipeline. Even if Bi–FIFO related interrupts will not be used, and it seems unnecessary to set the threshold levels, one must still perform four dummy writes to initialize these registers, or the first four data values written to the A port of the Bi–FIFO will be lost. The order in which the four flag threshold values are written is as follows:

1) The **Almost Full** flag threshold for the **Outgoing Side** of the **A port** (which is also the **Incoming Side** of the **B port**).

2) The **Almost Empty** flag threshold for the **Outgoing Side** of the **A port** (which is also the **Incoming Side** of the **B port**).

3) The **Almost Full** flag threshold for the **Outgoing Side** of the **B port** (which is also the **Incoming Side** of the **A port**).

4) The **Almost Empty** flag threshold for the **Outgoing Side** of the **B port** (which is also the **Incoming Side** of the **A port**).

The terms **Incoming** and **Outgoing**, as used above and in all further discussion of Bi–FIFOs in this manual, are **with respect to the processor** that is performing the initialization. In each case, the value to write to the Bi–FIFO is the number of **EMPTY** data locations that remain in a given FIFO. Thus, when programming the threshold values for the Almost Full flags (first and third writes) the value to write to the Bi–FIFO, AFT (Almost Full Threshold), must be calculated as follows:

$$AFT = D - FL$$

Where:

AFT is the threshold value at which the Almost Full flag should be asserted,

D is the depth of the internal FIFO, which is:
1,024 for standard units or the inter–processor FIFOs in Option 321, or
16,384 for Option 320, or the VIM FIFOs in Option 321, and

FL is the number of locations in the FIFO that are full (i. e., contain data)

The value for the Almost Empty flag threshold (AET) is simply the number of locations that do not contain data. To state this as an equation:

$$AET = EL$$

Where:

AET is the threshold value at which the Almost Empty flag should be asserted, and

EL is the number of locations in the FIFO that are empty (i. e., contain no data).

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6.3 Initializing the Bi–FIFO Structure (continued)

6.3.1 Setting Bi–FIFO Thresholds (continued)

For example, let us suppose one has a standard Model 4290, with a VIM I/O module that uses the Bi–FIFO interface installed in the top position. Processor A sends data to and receives data from this module via the Bi–FIFO interface, and we will further assume that the processor will need to be interrupted when either one of the following conditions is true:

1) The processor is writing data to the module and there are only 16 empty locations remaining in the Outgoing FIFO, or

2) The processor is reading data from the module, and there are only 16 samples remaining in the Incoming FIFO.

The solution is as follows:

a) The first value we must write to the Bi–FIFO is the Almost Full Threshold for the Outgoing Side of Port A, or the side that the processor uses to write data to the module. This value must be calculated using the FIFOs depth, the value given in statement (1) above and the equation:

$$AFT = D - FL = 1024 - 16 = 1008 = 0x03F0$$

b) The next value to write is the Almost Empty Threshold for the Outgoing side of the A port, (again, the side that the processor uses to write data to the module). According to the statement of our problem, this is not a condition we care about. Given that freedom, we will set the value arbitrarily low, at the minimum allowable value of 0x0001.

c) The third value that must be written to the Bi–FIFO is the Almost Full Threshold for the Incoming side of the A port, or the side of the FIFO that the processor reads the module's data from. Again, this is not a condition of concern, but some value must still be written. In this case, we will arbitrarily use the maximum allowable threshold value of 1023, or 0x03FF.

d) The fourth and final write of the initialization process is the Almost Empty Threshold for the Incoming Side of Port A (again, the side that the processor reads the module's data from). Statement (2) above defines this value as 16, which we simply convert to hex and write as 0x0010.

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6.4 Using Bi–FIFO Related Interrupts

In standard configurations of the Model 4290/4291 (meaning, in this sense, any option or combination of options that does not include Option 330), the EXT_INT5 interrupt of each processor is associated with the Bi–FIFO mailboxes, and EXT_INT7 is associated with the Bi–FIFO flags (in addition to Non–FIFO interrupts from VIM and Global bus Daughterboards). On Option 330 boards, the interrupts are mappable, and can drive whichever interrupt input the programmer may select (EXT_INT4 : EXT_INT7, see Section 4.3.2.9). Each Bi–FIFO and its associated mailboxes have enable bits, latched flag bits and flag status bits associated with them. Each of these bits resides in a register with bits of similar function. These are the Interrupt Enable Registers (IER0 & IER1), the Interrupt Flag Registers (IFR0 & IFR1) and the Interrupt Status Registers (ISR0 & ISR1). The Bi–FIFO interrupt control bits are summarized in Table 6–4, below. Detailed descriptions of these registers and bits can be found in the subsections that follow.

Table 6-4: Model 4290/4291 –Bi-FIFO and FIFO Mailbox Interrupt Control Bit Summary

Source	Enable Bit	Flag Bit	Status Bit	Interrupt*
I-P XX Bi-FIFO Outgoing Side Almost Full	IER0 Bit 13	IFR0 Bit 13	ISR0 Bit 13	
I-P XX Bi-FIFO Outgoing Side Almost Empty	IER0 Bit 12	IFR0 Bit 12	ISR0 Bit 12	EXT_INT7
I-P XX Bi-FIFO Outgoing Side Empty	IER0 Bit 11	IFR0 Bit 11	ISR0 Bit 11	
I-P XX Outgoing Mailbox	IER0 Bit 14	IFR0 Bit 14	ISR0 Bit 14	EXT_INT5
I-P XX Bi-FIFO Incoming Side Almost Full	IER0 Bit 10	IFR0 Bit 10	ISR0 Bit 10	
I-P XX Bi-FIFO Incoming Side Almost Empty	IER0 Bit 9	IFR0 Bit 9	ISR0 Bit 9	EXT_INT7
I-P XX Bi-FIFO Incoming Side Empty	IER0 Bit 8	IFR0 Bit 8	ISR0 Bit 8	
I-P XX Incoming Mailbox	IER0 Bit 15	IFR0 Bit 15	ISR0 Bit 15	EXT_INT5
I-P ZZ Bi-FIFO Outgoing Side Almost Full	IER1 Bit 13	IFR1 Bit 13	ISR1 Bit 13	
I-P ZZ Bi-FIFO Outgoing Side Almost Empty	IER1 Bit 12	IFR1 Bit 12	ISR1 Bit 12	EXT_INT7
I-P ZZ Bi-FIFO Outgoing Side Empty	IER1 Bit 11	IFR1 Bit 11	ISR1 Bit 11	
I-P ZZ Outgoing Mailbox	IER1 Bit 14	IFR1 Bit 14	ISR1 Bit 14	EXT_INT5
I-P ZZ Bi-FIFO Incoming Side Almost Full	IER1 Bit 10	IFR1 Bit 10	ISR1 Bit 10	
I-P ZZ Bi-FIFO Incoming Side Almost Empty	IER1 Bit 9	IFR1 Bit 9	ISR1 Bit 9	EXT_INT7
I-P ZZ Bi-FIFO Incoming Side Empty	IER1 Bit 8	IFR1 Bit 8	ISR1 Bit 8	
I-P ZZ Incoming Mailbox	IER1 Bit 15	IFR1 Bit 15	ISR1 Bit 15	EXT_INT5
VIM Bi-FIFO Outgoing Side Almost Full	IER1 Bit 5	IFR1 Bit 5	ISR1 Bit 5	
VIM Bi-FIFO Outgoing Side Almost Empty	IER1 Bit 4	IFR1 Bit 4	ISR1 Bit 4	EXT_INT7
VIM Bi-FIFO Outgoing Side Empty	IER1 Bit 3	IFR1 Bit 3	ISR1 Bit 3	
VIM Outgoing Mailbox	IER1 Bit 6	IFR1 Bit 6	ISR1 Bit 6	EXT_INT5
VIM Bi-FIFO Incoming Side Almost Full	IER1 Bit 2	IFR1 Bit 2	ISR1 Bit 2	
VIM Bi-FIFO Incoming Side Almost Empty	IER1 Bit 1	IFR1 Bit 1	ISR1 Bit 1	EXT_INT7
VIM Bi-FIFO Incoming Side Empty	IER1 Bit 0	IFR1 Bit 0	ISR1 Bit 0	
VIM Incoming Mailbox	IER1 Bit 7	IFR1 Bit 7	ISR1 Bit 7	EXT_INT5

*** –These Interrupt inputs are fixed in standard configurations of the Model 4290/4291. They are mappable on Option 330 boards (see Section 4.3.2.9).**

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.1 Interrupt Status Registers (Read Only)

'C6x Addresses:
ISR0 (XX port) – 0x0028 0010
ISR1 (ZZ & VIM ports)– 0x0028 0014

These registers mirror the current, real–time states of the flag outputs for their associated Bi–FIFOs. Each processor has a unique version of each of these registers, one for the XX or upstream Bi–FIFO (ISR0, at 'C6x address 0x0028 0010), and the other for the ZZ or downstream Bi–FIFO and the VIM Bi–FIFO (ISR1, at address 0x0028 0014). Any specific processor can only access its own pair of these registers. These are Read–Only registers, and write operations to these addresses will have no effect.

The inter–processor Bi–FIFO designations (XX and ZZ) represent different inter–processor connection paths. Figure 6–1, on page 152, illustrates the inter–processor connection paths. Table 6–5, below, shows the contents of ISR0. Table 6–6, at the bottom of this page, shows the contents of ISR1. The subsections that begin at the top of the next page describe the functions of each of the Bi–FIFO flag status bits.

Table 6-5: Model 4290/4291 –Interrupt Status Register for Upstream Inter–Processor (XX) Bi–FIFO (ISR0) –R. O. @ 0x0028 0010

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	XX_Incoming _Mailbox	XX_Outgoing _Mailbox	XX_Outgoing _Almost Full	XX_Outgoing _Almost Empty	XX_Outgoing _Empty	XX_Incoming _Almost Full	XX_Incoming _Almost Empty	XX_Incoming _Empty
Function	1 = Flag is Asserted, 0 = Flag is NOT Asserted							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved							
Function	Write with "0"'s, Mask when Reading							

NOTE: After a boot or reset, the Almost Empty and Empty bits will be true, and all other bits will be false Thus, the reset state of this register is 0001 1011 XXXX XXXX (in binary) or 0x0000 1Bxx (hex)

Table 6-6: Model 4290/4291 –Interrupt Status Register for Downstream Inter–Processor (ZZ) and VIM Bi–FIFOs (ISR1) –R. O. @ 0x0028 0014

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	ZZ_Incoming _Mailbox	ZZ_Outgoing _Mailbox	ZZ_Outgoing _Almost Full	ZZ_Outgoing _Almost Empty	ZZ_Outgoing _Empty	ZZ_Incoming _Almost Full	ZZ_Incoming _Almost Empty	ZZ_Incoming _Empty
Function	1 = Flag is Asserted, 0 = Flag is NOT Asserted							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VIM_Incoming _Mailbox	VIM_Outgoing _Mailbox	VIM_Outgoing _Almost Full	VIM_Outgoing _Almost Empty	VIM_Outgoing _Empty	VIM_Incoming _Almost Full	VIM_Incoming _Almost Empty	VIM_Incoming _Empty
Function	1 = Flag is Asserted, 0 = Flag is NOT Asserted							

NOTE: After a boot or reset, the Almost Empty and Empty bits will be true, and all other bits will be false Thus, the reset state of this register 0001 1011 0001 1011 (in binary) or 0x0000 1B1B (hex)

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.1 Interrupt Status Registers (continued)

6.4.1.1 Incoming Mailbox Flag Status Bits (R. O.)

XX Mailbox – D15 @ ISR0 (0x0028 0010)
ZZ Mailbox – D15 @ ISR1 (0x0028 0014)
VIM Mailbox – D7 @ ISR1 (0x0028 0014)

When one of these bits reads back in the logic '1' state, it indicates that the associated incoming mailbox flag is set, i. e., that new data has been placed in the associated Bi–FIFO's mailbox by another processor. A logic '0' in any of these bits indicates that no new mailbox data is available.

6.4.1.2 Outgoing Mailbox Flag Status Bits (R. O.)

XX Mailbox – D14 @ ISR0 (0x0028 0010)
ZZ Mailbox – D14 @ ISR1 (0x0028 0104)
VIM Mailbox – D6 @ ISR1 (0x0028 0014)

When one of these bits reads back in the logic '1' state, it indicates that the associated outgoing mailbox flag is set, i. e., that the new data placed in the associated Bi–FIFOs mailbox by the associated processor has not yet been read. A logic '0' in any of these bits indicates that no unread data is in the mailbox.

6.4.1.3 Outgoing Bi–FIFO Almost Full Flag Status Bits (R. O.)

XX Bi–FIFO – D13 @ ISR0 (0x0028 0010)
ZZ Bi–FIFO – D13 @ ISR1 (0x0028 0014)
VIM Bi–FIFO – D5 @ ISR1 (0x0028 0014)

When one of these bits reads back in the logic '1' state, it indicates that the associated almost full flag is set, i. e., that the data in the outgoing side of the associated Bi–FIFO is at or above the pro–grammed almost full level. In a continuous, real–time system, this indicates that no more data should be written to this Bi–FIFO until a significant amount has been read from the other side. A logic '0' in any of these bits indicates that the associated Bi–FIFO is not almost full.

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.1 Interrupt Status Registers (continued)

6.4.1.4 Outgoing Bi–FIFO Almost Empty Flag Status Bits (R. O.)

XX Bi–FIFO – D12 @ ISR0 (0x0028 0010)
ZZ Bi–FIFO – D12 @ ISR1 (0x0028 0014)
VIM Bi–FIFO – D4 @ ISR1 (0x0028 0014)

When one of these bits reads back in the logic '1' state, it indicates that the associated almost empty flag is set, i. e., that the data in the outgoing side of the associated Bi–FIFO is at or below the programmed almost empty level. In a continuous, real–time system, this indicates that the processor that is writing data to the Bi–FIFO should resume doing so in short order. A logic '0' in any of these bits indicates that the associated Bi–FIFO is not almost empty.

6.4.1.5 Outgoing Bi–FIFO Empty Flag Status Bits (R. O.)

XX Bi–FIFO – D11 @ ISR0 (0x0028 0010)
ZZ Bi–FIFO – D11 @ ISR1 (0x0028 0014)
VIM Bi–FIFO – D3 @ ISR1 (0x0028 0014)

When one of these bits reads back in the logic '1' state, it indicates that the associated empty flag is set, i. e., that no data remains in the outgoing side of the associated Bi–FIFO. In a continuous, real–time system, this indicates that the processor that is writing data to the Bi–FIFO should resume doing so immediately. A logic '0' in any of these bits indicates that the associated Bi–FIFO has some data in it.

6.4.1.6 Incoming Bi–FIFO Almost Full Flag Status Bits (R. O.)

XX Bi–FIFO – D10 @ ISR0 (0x0028 0010)
ZZ Bi–FIFO – D10 @ ISR1 (0x0028 0014)
VIM Bi–FIFO – D2 @ ISR1 (0x0028 0014)

When one of these bits reads back in the logic '1' state, it indicates that the associated almost full flag is set, i. e., that the data in the outgoing side of the associated Bi–FIFO is at or above the programmed almost full level. In a continuous, real–time system, this indicates that the processor that is reading data from the Bi–FIFO should resume doing so immediately, or data may be lost (if it hasn't been already). A logic '0' in any of these bits indicates that the associated Bi–FIFO is not almost full.

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.1 Interrupt Status Registers (continued)

6.4.1.7 Incoming Bi–FIFO Almost Empty Flag Status Bits (R. O.)

XX Bi–FIFO – D9 @ ISR0 (0x0028 0010)
ZZ Bi–FIFO – D9 @ ISR1 (0x0028 0014)
VIM Bi–FIFO – D1 @ ISR1 (0x0028 0014)

When one of these bits reads back in the logic '1' state, it indicates that the associated almost empty flag is set, i. e., that the data in the outgoing side of the associated Bi–FIFO is at or below the programmed almost empty level. In a continuous, real–time system, this indicates that the processor that is reading data from the Bi–FIFO may have some free time available for other tasks. A logic '0' in any of these bits indicates that the associated Bi–FIFO is not almost empty.

6.4.1.8 Incoming Bi–FIFO Empty Flag Status Bits (R. O.)

XX Bi–FIFO – D8 @ ISR0 (0x0028 0010)
ZZ Bi–FIFO – D8 @ ISR1 (0x0028 0014)
VIM Bi–FIFO – D0 @ ISR1 (0x0028 0014)

When one of these bits reads back in the logic '1' state, it indicates that the associated empty flag is set, i. e., that no data remains in the outgoing side of the associated Bi–FIFO. This indicates that the processor that is reading data from the Bi–FIFO must stop doing so until more data is available. A logic '0' in any of these bits indicates that the associated Bi–FIFO has at least one data sample remaining in its incoming side.

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.2 Interrupt Flag Registers (Read/Clear)

'C6x Addresses:
IFR0 (XX port) – 0x0028 0008
IFR1 (ZZ & VIM ports)– 0x0028 000C

These registers latch the assertion of the flag outputs for their associated Bi–FIFOs. Each processor has a unique version of each of these registers, one for the XX or upstream Bi–FIFO (IFR0, at 'C6x address 0x0028 0008), and the other for the ZZ or downstream Bi–FIFO and the VIM Bi–FIFO (IFR1, at address 0x0028 000C). Any specific processor can only access its own pair of these registers. Because the states of the Bi–FIFO flags are intrinsically transient, these registers provide a place that retains the information that a particular state was reached, which may be examined during an interrupt service routine. These are Read/Clear registers, meaning that data you may write to the bits in these registers will not necessarily be stored in them. When the Bi–FIFO flag associated with one of the bits in this register is asserted, that bit will be set to the logic '1' state, and will retain that state regardless of subsequent logic states that the associated flag may assume. To clear a set bit in one of these registers (after the appropriate action has been taken based on the flag information the bit contains, during an ISR, for example), a '1' is written to the bit to clear it to the logic '0' state, thus arming it for subsequent interrupt generation. Writing a '0' to any of the bits in either of these registers has no effect.

The inter–processor Bi–FIFO designations (XX and ZZ) represent different inter–processor connection paths. Figure 6–1, on page 152, illustrates the inter–processor connection paths. Table 6–7, below, shows the contents of IFR0. Table 6–8, at the top of the next page, shows the contents of IFR1. The paragraphs that begin below Table 6–8 describe the functions of each of the Bi–FIFO flag latch bits.

Table 6–7: Model 4290/4291 –Interrupt Flag Register for Upstream Inter–Processor (XX) Bi–FIFO (IFR0) –R/C @ 0x0028 0008

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	XX_Incoming _Mailbox	XX_Outgoing _Mailbox	XX_Outgoing _Almost Full	XX_Outgoing _Almost Empty	XX_Outgoing _Empty	XX_Incoming _Almost Full	XX_Incoming _Almost Empty	XX_Incoming _Empty
Function	Read Operation: 1 = Flag has been asserted, 0 = Flag has not been asserted Write Operation: 1 = Clear a set bit that has been set, 0 = No action.							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved							
Function	Write with "0"'s, Mask when Reading							

NOTE: The reset state of this register is indeterminate.
Before using this register, it must be cleared, by writing 0xFF00 to it.

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.2 Interrupt Flag Registers (continued)

Table 6–8: Model 4290/4291 –Interrupt Flag Register for Downstream Inter–Processor (ZZ) and VIM Bi–FIFOs (IFR1) –R/C @ 0x0028 000C

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	ZZ_Incoming _Mailbox	ZZ_Outgoing _Mailbox	ZZ_Outgoing _Almost Full	ZZ_Outgoing _Almost Empty	ZZ_Outgoing _Empty	ZZ_Incoming _Almost Full	ZZ_Incoming _Almost Empty	ZZ_Incoming _Empty
Function	Read Operation: 1 = Flag has been asserted, 0 = Flag has not been asserted Write Operation: 1 = Clear a set bit that has been set, 0 = No action.							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VIM_Incoming _Mailbox	VIM_Outgoing _Mailbox	VIM_Outgoing _Almost Full	VIM_Outgoing _Almost Empty	VIM_Outgoing _Empty	VIM_Incoming _Almost Full	VIM_Incoming _Almost Empty	VIM_Incoming _Empty
Function	Read Operation: 1 = Flag has been asserted, 0 = Flag has not been asserted Write Operation: 1 = Clear a set bit that has been set, 0 = No action.							

NOTE: The reset state of this register is indeterminate. Before using this register, it must be cleared, by writing 0xFFFF to it.

6.4.2.1 Incoming Mailbox Flag Latch Bits (R/C)

XX Mailbox – D15 @ IFR0 (0x0028 0008)
ZZ Mailbox – D15 @ IFR1 (0x0028 000C)
VIM Mailbox – D7 @ IFR1 (0x0028 000C)

These bits will read back in the logic '1' state after data has been placed in the associated Bi–FIFO's Incoming Mailbox. After reading the mailbox data, this latched flag bit may be cleared by writing a '1' to it.

6.4.2.2 Outgoing Mailbox Flag Latch Bits (R/C)

XX Mailbox – D14 @ IER0 (0x0028 0008)
ZZ Mailbox – D14 @ IER1 (0x0028 000C)
VIM Mailbox – D6 @ IER1 (0x0028 000C)

These bits will read back in the logic '1' state after data that the DSP has written to the associated Bi–FIFO's Outgoing Mailbox has been removed. This latched flag bit may be cleared by writing a '1' to it.

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.2 Interrupt Flag Registers (continued)

6.4.2.3 Outgoing Bi–FIFO Almost Full Flag Latch Bits (R/C)

XX Bi–FIFO – D13 @ IER0 (0x0028 0008)
ZZ Bi–FIFO – D13 @ IER1 (0x0028 000C)
VIM Bi–FIFO – D5 @ IER1 (0x0028 000C)

These bits will read back in the logic '1' state after the outgoing side of the associated Bi–FIFO has reached the programmed Almost Full level. In a continuous, real–time system, this indicates that no more data should be written to this Bi–FIFO until a significant amount has been read from the other side. This latched flag bit may be cleared by writing a '1' to it.

6.4.2.4 Outgoing Bi–FIFO Almost Empty Flag Latch Bits (R/C)

XX Bi–FIFO – D12 @ IER0 (0x0028 0008)
ZZ Bi–FIFO – D12 @ IER1 (0x0028 000C)
VIM Bi–FIFO – D4 @ IER1 (0x0028 000C)

These bits will read back in the logic '1' state after the outgoing side of the associated Bi–FIFO has reached the programmed Almost Empty level. In a continuous, real–time system, this indicates that the processor that is writing data to the Bi–FIFO should resume doing so in short order. The latched flag bit may be cleared by writing a '1' to it.

6.4.2.5 Outgoing Bi–FIFO Empty Flag Latch Bits (R/C)

XX Bi–FIFO – D11 @ IER0 (0x0028 0008)
ZZ Bi–FIFO – D11 @ IER1 (0x0028 000C)
VIM Bi–FIFO – D3 @ IER1 (0x0028 000C)

These bits will read back in the logic '1' state after all data has been read from the outgoing side of the associated Bi–FIFO. In a continuous, real–time system, this indicates that the processor that is writing data to the Bi–FIFO should resume doing so immediately. This latched flag bit may be cleared by writing a '1' to it.

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.2 Interrupt Flag Registers (continued)

6.4.2.6 Incoming Bi–FIFO Almost Full Flag Latch Bits (R/C)

XX Bi–FIFO – D10 @ IER0 (0x0028 0008)
ZZ Bi–FIFO – D10 @ IER1 (0x0028 000C)
VIM Bi–FIFO – D2 @ IER1 (0x0028 000C)

These bits will read back in the logic '1' state after the incoming side of the associated Bi–FIFO has reached the programmed Almost Full level. In a continuous, real–time system, this indicates that the processor that is reading data from the Bi–FIFO should resume doing so immediately, or data may be lost (if it hasn't been already). This latched flag bit may be cleared by writing a '1' to it.

6.4.2.7 Incoming Bi–FIFO Almost Empty Flag Latch Bits (R/C)

XX Bi–FIFO – D9 @ IER0 (0x0028 0008)
ZZ Bi–FIFO – D9 @ IER1 (0x0028 000C)
VIM Bi–FIFO – D1 @ IER1 (0x0028 000C)

These bits will read back in the logic '1' state after the incoming side of the associated Bi–FIFO reaches the programmed almost empty level. In a continuous, real–time system, this indicates that the processor that is reading data from the Bi–FIFO may have some free time available for other tasks. This latched flag bit may be cleared by writing a '1' to it.

6.4.2.8 Incoming Bi–FIFO Empty Flag Latch Bits (R/C)

XX Bi–FIFO – D8 @ IER0 (0x0028 0008)
ZZ Bi–FIFO – D8 @ IER1 (0x0028 000C)
VIM Bi–FIFO – D0 @ IER1 (0x0028 000C)

These bits will read back in the logic '1' state after all data has been read from the incoming side of the associated Bi–FIFO. This indicates that the processor that is reading data from the Bi–FIFO must stop doing so until more data is available. This latched flag bit may be cleared by writing a '1' to it.

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.3 Interrupt Enable Registers (Read/Write)

'C6x Addresses:
IER0 (XX port) – 0x0028 0000
IER1 (ZZ & VIM ports)– 0x0028 0004

These registers contain enable bits for the interrupt sources associated with the two inter–processor communication Bi–FIFOs. Each processor has a unique version of each of these registers, one for the XX or upstream Bi–FIFO (IER0, at 'C6x address 0x0028 0000), and the other for the ZZ or downstream Bi–FIFO and the VIM Bi–FIFO (IER1, at address 0x0028 0004). Any specific processor can only access its own pair of these registers. The registers contain enable bits that allow the associated Bi–FIFO flags to generate the specified interrupt. If an enable bit is set to the logic '1' state, and the associated flag condition is met, an interrupt results. The inter–processor Bi–FIFO designations (XX and ZZ) represent different inter–processor connection paths. Figure 6–1, on page 152, illustrates the inter–processor connection paths. Note that Processor A's XX Bi–FIFO is also Processor C's ZZ Bi–FIFO, seen from the other side. Table 6–9, below, shows the contents of IER0. Table 6–10, at the bottom of this page, shows the contents of IER1. The subsections that begin on the next page describe the functions of each of the Bi–FIFO flag interrupt enable bits.

Table 6–9: Model 4290/4291 –Interrupt Enable Register for Upstream Inter–Processor (XX) Bi–FIFO (IER0) –R/W @ 0x0028 0000

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	XX_Incoming _Mailbox	XX_Outgoing _Mailbox	XX_Outgoing _Almost Full	XX_Outgoing _Almost Empty	XX_Outgoing _Empty	XX_Incoming _Almost Full	XX_Incoming _Almost Empty	XX_Incoming _Empty
Function	1 = Enable Interrupt, 0 = Disable Interrupt							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved							
Function	Write with "0"'s, Mask when Reading							

NOTE: All bits are cleared to the logic '0' state at boot and by resets.

Table 6–10: Model 4290/4291 –Interrupt Enable Register for Downstream Inter–Processor (ZZ) and VIM Bi–FIFOs (IER1) –R/W @ 0x0028 0004

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	ZZ_Incoming _Mailbox	ZZ_Outgoing _Mailbox	ZZ_Outgoing _Almost Full	ZZ_Outgoing _Almost Empty	ZZ_Outgoing _Empty	ZZ_Incoming _Almost Full	ZZ_Incoming _Almost Empty	ZZ_Incoming _Empty
Function	1 = Enable Interrupt, 0 = Disable Interrupt							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VIM_Incoming _Mailbox	VIM_Outgoing _Mailbox	VIM_Outgoing _Almost Full	VIM_Outgoing _Almost Empty	VIM_Outgoing _Empty	VIM_Incoming _Almost Full	VIM_Incoming _Almost Empty	VIM_Incoming _Empty
Function	1 = Enable Interrupt, 0 = Disable Interrupt							

NOTE: All bits are cleared to the logic '0' state at boot and by resets.

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.3 Interrupt Enable Registers (continued)

On a standard Model 4290/4291, the Bi–FIFO Flag–related interrupts are asserted on the EXT_INT7 input of the 'C6x processors, and the Bi–FIFO mailbox interrupts are asserted on EXT_INT5. For the 4290/4291 Option 330, please refer to Section 4.3.2.9, which describes Interrupt Mapping Register 0.

6.4.3.1 Incoming Mailbox Interrupt Enable Bits (R/W)

XX Mailbox – D15 @ IER0 (0x0028 0000)
ZZ Mailbox – D15 @ IER1 (0x0028 0004)
VIM Mailbox – D7 @ IER1 (0x0028 0004)

Set one of these bits to the logic '1' state, to allow the DSP to be interrupted when data has been placed in the associated Bi–FIFO's Incoming Mailbox. To prevent such interrupts, clear the associated bit to the logic '0' state.

6.4.3.2 Outgoing Mailbox Interrupt Enable Bits (R/W)

XX Mailbox – D14 @ IER0 (0x0028 0000)
ZZ Mailbox – D14 @ IER1 (0x0028 0004)
VIM Mailbox – D6 @ IER1 (0x0028 0004)

Set one of these bits to the logic '1' state, to allow the DSP to be interrupted when data that the DSP has written to the associated Bi–FIFO's Outgoing Mailbox has been removed. To prevent such interrupts, clear the associated bit to the logic '0' state.

6.4.3.3 Outgoing Bi–FIFO Almost Full Interrupt Enable Bits (R/W)

XX Bi–FIFO – D13 @ IER0 (0x0028 0000)
ZZ Bi–FIFO – D13 @ IER1 (0x0028 0004)
VIM Bi–FIFO – D5 @ IER1 (0x0028 0004)

Set one of these bits to the logic '1' state, to allow the DSP to be interrupted when the outgoing side of the associated Bi–FIFO reaches the programmed Almost Full level. To prevent such interrupts, clear the associated bit to the logic '0' state.

6.4.3.4 Outgoing Bi–FIFO Almost Empty Interrupt Enable Bits (R/W)

XX Bi–FIFO – D12 @ IER0 (0x0028 0000)
ZZ Bi–FIFO – D12 @ IER1 (0x0028 0004)
VIM Bi–FIFO – D4 @ IER1 (0x0028 0004)

Set one of these bits to the logic '1' state, to allow the DSP to be interrupted when the outgoing side of the associated Bi–FIFO reaches the programmed almost empty level. To prevent such interrupts, clear the associated bit to the logic '0' state.

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6.4 Using Bi–FIFO Related Interrupts (continued)

6.4.3 Interrupt Enable Registers (continued)

6.4.3.5 Outgoing Bi–FIFO Empty Interrupt Enable Bits (R/W)

XX Bi–FIFO – D11 @ IER0 (0x0028 0000)
ZZ Bi–FIFO – D11 @ IER1 (0x0028 0004)
VIM Bi–FIFO – D3 @ IER1 (0x0028 0004)

Set one of these bits to the logic '1' state, to allow the DSP to be interrupted when no data remains in the outgoing side of the associated Bi–FIFO. To prevent such interrupts, clear the associated bit to the logic '0' state.

6.4.3.6 Incoming Bi–FIFO Almost Full Interrupt Enable Bits (R/W)

XX Bi–FIFO – D10 @ IER0 (0x0028 0000)
ZZ Bi–FIFO – D10 @ IER1 (0x0028 0004)
VIM Bi–FIFO – D2 @ IER1 (0x0028 0004)

Set one of these bits to the logic '1' state, to allow the DSP to be interrupted when the incoming side of the associated Bi–FIFO reaches the programmed almost full level. To prevent such interrupts, clear the associated bit to the logic '0' state.

6.4.3.7 Incoming Bi–FIFO Almost Empty Interrupt Enable Bits (R/W)

XX Bi–FIFO – D9 @ IER0 (0x0028 0000)
ZZ Bi–FIFO – D9 @ IER1 (0x0028 0004)
VIM Bi–FIFO – D1 @ IER1 (0x0028 0004)

Set one of these bits to the logic '1' state, to allow the DSP to be interrupted when the incoming side of the associated Bi–FIFO reaches the programmed almost empty level. To prevent such interrupts, clear the associated bit to the logic '0' state.

6.4.3.8 Incoming Bi–FIFO Empty Interrupt Enable Bits (R/W)

XX Bi–FIFO – D8 @ IER0 (0x0028 0000)
ZZ Bi–FIFO – D8 @ IER1 (0x0028 0004)
VIM Bi–FIFO – D0 @ IER1 (0x0028 0004)

Set one of these bits to the logic '1' state, to allow the DSP to be interrupted when all data has been read from the incoming side of the associated Bi–FIFO. To prevent such interrupts, clear the associated bit to the logic '0' state.

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6.5 Bi–FIFO Performance Issues on the Model 4290/4291

This section identifies the Bi–FIFOs used for the various size & speed options on Pentek's Model 4290/4291 DSP boards, discusses some issues that our users have brought to our attention concerning certain configurations, and provides some strategies you may want to consider when working with these devices.

The information given in the subsections below with respect to the maximum Bi–FIFO access rate is provided for the customer's information **ONLY**, and is **NOT** guaranteed to be achievable by every Model 4290/4291 equipped with the configuration option that the section discusses. Nor do we guarantee that a unit that can achieve such performance will be able to maintain it over variations in temperature or supply voltage.

Additionally, many of the subsections below suggest some alternative settings for the EMIF (External Memory Interface) CE1 Space Control Register, at 'C6x address 0x0180 0004, to improve the performance of certain configurations. The user should be aware, however, that as a general rule Pentek **DOES NOT SUPPORT** user reprogramming of the EMIF. The Model 4290/4291, in **ANY** configuration, is guaranteed to be stable and operational **ONLY** at the factory EMIF settings, and any changes to these settings are made at the user's own risk.

6.5.1 Bi–FIFOs on the Standard Model 4290/4291

Bi–FIFO Type: IDT 7236420–15
FIFO Depth: 1,024 x 36 x 2
Operating Mode: Asynchronous

On the Standard Model 4290:

Read Rate: Set in Firmware to 22.2 MHz (88.8 MBytes/sec)
Tested at up to 33.3 MHz (133.3 MBytes/sec)

Write Rate: Set in Firmware to 25 MHz (100 MBytes/sec)
Tested at up to 33.3 MHz (133.3 MBytes/sec)

To obtain the maximum rate shown above, the user must reprogram the EMIF CE1 Register (at address 0x0180 0004) to 0x20A2 0222 (for 200 MHz 'C6201's).

On the Standard Model 4291:

Read Rate: Set in Firmware to 18.5 MHz (74 MBytes/sec)
Tested at up to 27.8 MHz (111.1 MBytes/sec)

Write Rate: Set in Firmware to 20.8 MHz (83.3 MBytes/sec)
Tested at up to 27.8 MHz (111.1 MBytes/sec)

To obtain the maximum rate shown above, the user must reprogram the EMIF CE1 Register (at address 0x0180 0004) to 0x20A2 0222 (for 167 MHz 'C6701's).

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6.5 Bi–FIFO Performance Issues on the Model 4290/4291 (continued)

6.5.2 Bi–FIFOs on the Model 4290/4291 Option 316

Bi–FIFO Type: IDT 7236420–12
FIFO Depth: 1,024 x 36 x 2
Operating Mode: Asynchronous

Although the Model 4290/4291 Option 316 comes equipped with faster Bi–FIFOs than the standard and Option 320 units (see Section 6.5.3), we program the EMIF for Option 316 identically to the slower units for the sake of stability over varying operating conditions. For Option 316 **ONLY**, Pentek **does** support changing the EMIF CE1 Space Control Register **to the values shown below**, but we can guarantee stable operation at this setting **ONLY** if the following conditions are met:

1) The +5 V_{DC} power supply rail must be maintained at $\geq$ +4.95 V_{DC}, $\leq$ +5.10 V_{DC}, measured on the VME backplane (J1, pin A32, B32 or C32).

2) The temperature in the VMEbus card cage must be maintained at $\leq$ +45°C, measured at the cage's exhaust fan.

On the Model 4290 Option 316:

Read Rate: Set in Firmware to 22.2 MHz (88.8 MBytes/sec)
Tested at up to 40 MHz (160 MBytes/sec)

Write Rate: Set in Firmware to 25 MHz (100 MBytes/sec)
Tested at up to 40 MHz (160 MBytes/sec)

To obtain the maximum rate shown above, the user must reprogram the EMIF CE1 Register (at address 0x0180 0004) to 0x10A3 0121 (for 200 MHz 'C6201's).

On the Model 4291 Option 316:

Read Rate: Set in Firmware to 18.5 MHz (74 MBytes/sec)
Tested at up to 33.3 MHz (133.3 MBytes/sec)

Write Rate: Set in Firmware to 20.8 MHz (83.3 MBytes/sec)
Tested at up to 33.3 MHz (133.3 MBytes/sec)

To obtain the maximum rate shown above, the user must reprogram the EMIF CE1 Register (at address 0x0180 0004) to 0x10A3 0121 (for 167 MHz 'C6701's).

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6.5 Bi–FIFO Performance Issues on the Model 4290/4291 (continued)

6.5.3 Bi–FIFOs on the Model 4290/4291 Option 320

Bi–FIFO Type: Cypress CY7C43682–10
FIFO Depth: 16,384 x 36 x 2
Operating Mode: Asynchronous

On the Model 4290 Option 320:

Read Rate: Set in Firmware to 22.2 MHz (88.8 MBytes/sec)
Tested at up to 40 MHz (160 MBytes/sec)

Write Rate: Set in Firmware to 25 MHz (100 MBytes/sec)
Tested at up to 40 MHz (160 MBytes/sec)

To obtain the maximum rate shown above, the user must reprogram the EMIF CE1 Register (at address 0x0180 0004) to 0x10A2 0221 (for 200 MHz 'C6201's).

On the Model 4291 Option 320:

Read Rate: Set in Firmware to 18.5 MHz (74 MBytes/sec)
Tested at up to 33.3 MHz (133.3 MBytes/sec)

Write Rate: Set in Firmware to 20.8 MHz (83.3 MBytes/sec)
Tested at up to 33.3 MHz (133.3 MBytes/sec)

To obtain the maximum rate shown above, the user must reprogram the EMIF CE1 Register (at address 0x0180 0004) to 0x10A2 0221 (for 167 MHz 'C6701's).



There is a bug in the Empty Flag operation of these Bi-FIFOs that will require a software work-around for any application that reads the FIFO. Please refer to Section 6.5.5, on the page after next, for a description of the problem and suggested work-arounds.

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6.5 Bi–FIFO Performance Issues on the Model 4290/4291 (continued)

6.5.4 Bi–FIFOs on the Model 4290/4291 Option 330



Pentek CANNOT retrofit other 4290 or 4291 units for Option 330. This option MUST be specified at the time of purchase.

Bi–FIFO Type: Cypress CY7C43682–7
FIFO Depth: 16,384 x 36 x 2
Operating Mode: Synchronous

On the Model 4290 Option 330:

Read Rate: Set in Firmware and tested to 100 MHz (400 MBytes/sec)

Write Rate: Set in Firmware and tested to 100 MHz (400 MBytes/sec)

On the Model 4291 Option 330:

Read Rate: Set in Firmware and tested to 83 MHz (333.3 MBytes/sec)

Write Rate: Set in Firmware and tested to 83 MHz (333.3 MBytes/sec)



There is a bug in the Empty Flag operation of these Bi-FIFOs that will require a software work-around for any application that reads the FIFO. Please refer to Section 6.5.5, on the next page, for a description of the problem and suggested work-arounds.

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6.5 Bi–FIFO Performance Issues on the Model 4290/4291 (continued)

6.5.5 The Cypress Bi–FIFO Empty Flag Problem and Work–Arounds

A problem exists, and has been acknowledged by Cypress, with the operation of the Empty flag on the CY7C43682 Bi–FIFOs. The problem affects the Models 4290 and 4291, equipped with Options 320 and/or 330, and manifests itself in the following manner:

1) The FIFO has become empty, and the Empty Flag has gone true.

2) A new sample is written to the FIFO, the Empty Flag goes false, and any number of additional samples is written to the FIFO.

3) When the FIRST sample is read from the FIFO, the Empty Flag again goes true, even though additional samples remain in the FIFO. The flag remains true for 3 cycles of the FIFO clock, during which time the FIFO behaves as if it truly were empty (i. e., the sample that you just read will be repeated for as long as this condition exists). This is true even if the FIFO contains sufficient data to set the Almost–Full or Full Flags.

Because the FIFO clock rate is fast with respect to the 'C6x's read rate, this problem will not present itself if two consecutive read cycles are conducted by the processor, because the processor connot execute the second read operation before three cycles of the FIFO clock have elapsed. The problem DOES present itself, however, when the 'C6x's DMA engine reads out the FIFO. In this mode, a new read operation is conducted for each FIFO clock cycle.

To work around this problem, we offer the following suggestions:

1) Do not let the FIFO go empty. If a few samples always remain in the FIFO, the problem never occurs.

2) Do not use 'C6x DMA to read out the FIFO. In this case, the erroneous assertion of the Empty Flag goes away before the second read operation.

3) If the FIFO has become empty and you MUST use DMA to read it out, first read a single sample without DMA (which will cause the erroneous assertion of the Empty Flag), then enable the DMA engine (during which time the incorrect assertion of the flag will clear itself), then read the remaining data in DMA mode. This method has been tested extensively, and we have found that it does not significantly degrade system throughput for block sizes $\geq$ 256.

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Chapter 7: Dual Port SRAM Operations on the Model 4290/4291

7.1 Overview of Dual–Port SRAMs on the Model 4290/4291

There are four blocks of Dual Port SRAM on the Model 4290/4291. The size of each block depends upon the option ordered: Option 240 provides four blocks of 128 kBytes (32k x 32) each, for a total of 512k Bytes (128k x 32); Option 244 provides four blocks of 256 kBytes (64k x 32) each, for a total 1 MByte (256k x 32). Access to addresses above the offset of the highest valid Dual Port SRAM address for a given option will result in redundant access to locations at equivalent offsets from the Dual Port SRAM base address (i. e., the resource is mirrored throughout its address region).

Each 'C6x processor has V–bus access to one of the four blocks of Dual Port SRAM. All four 'C6x processors and the VMEbus have Global bus access to all four blocks of Dual Port SRAM. In general, a given processor accesses its own block of Dual Port SRAM via its V–bus (in the address range from 0x0020 0000 : 0x0023 FFFF), and the other three processsors' blocks via the Global bus, with the Page Register (at V–bus address 0x0028 0024) set to 0x0050, in the address window from 0x0000 0000 : 0x001F FFFF, using the offset appropriate to the desired SRAM bank or SRAM Mail–box (see Table 7–1). 'C6x access to the Dual Port SRAM resources is conducted in D32 mode ONLY. The Dual Port SRAM and its mailboxes can also be accessed by VMEbus masters, in the address range from VME_base+0x00A0 0000 through VME_base+0x00BF FFFF. The VMEbus can access the Dual Port SRAM resources in D8, D16 or D32 mode.

Each Dual Port SRAM block is subdivided into four equal–sized banks (i. e., each bank is 8k x 32 for Option 240, 16k x 32 for Option 244). This organization is illustrated in Figure 7–1, on the next page.

Because these Dual Port SRAM banks are shared resources, it is necessary to control access to to them, to assure that data placed there by (or for) one master device are not overwritten by a task for another master. On the Model 4290/4291, access to the Dual Port SRAM banks is controlled by a semaphore system.

In order to obtain access to any of the 16 banks of Dual Port SRAM, a master must first obtain the semaphore for that bank. In Figure 7–1, on the next page, the sema–phores are represented by the buffer symbols within the dashed boundary of each DPSRAM block. These are "conceptual" buffers, as opposed to the buffer symbols shown between each processor's V–bus and the Global bus (note that these symbols are drawn differently), which represent physical buffer devices. One might also say that these "conceptual" buffers are "conceptually" enabled by obtaining the sema–phore.

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7.1 Overview of Dual–Port SRAMs on the Model 4290/4291 (continued)

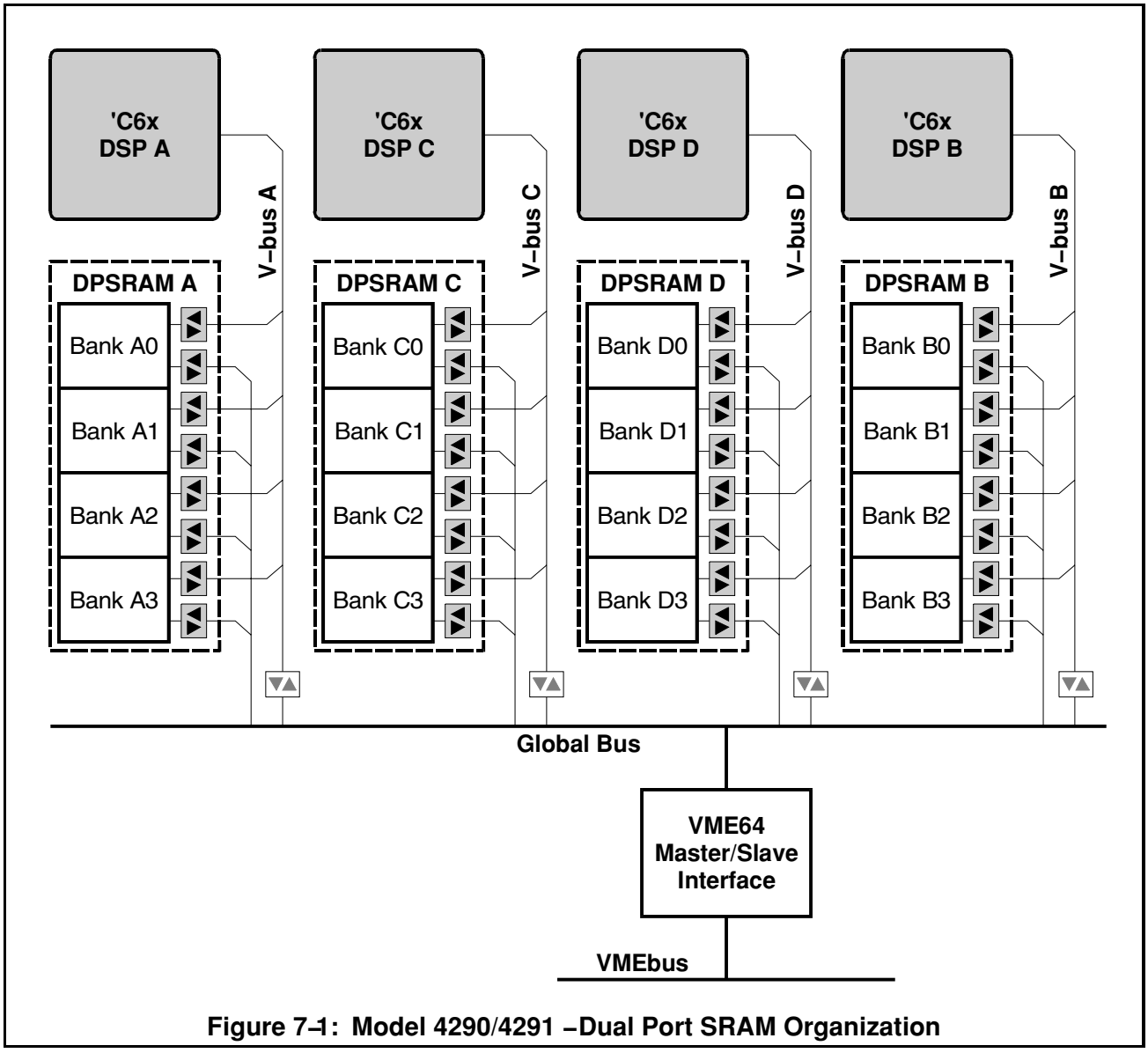


Figure 7–1: Model 4290/4291 –Dual Port SRAM Organization

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7.1 Overview of Dual–Port SRAMs on the Model 4290/4291 (continued)

At any given time, a Dual Port SRAM bank can exist in one of three possible states:

1) The DPSRAM bank is owned by the local 'C6x processor, and is accessible via that DSP's V–bus. The bank is acquired by 'C6x through its Local Semaphore Register (LSR).

2) The DPSRAM bank is owned by a Global bus master (either a 'C6x or VME), and is accessible via the Global bus. The bank is acquired by the Global bus master through the Global Dual Port Semaphore Register (DPSR).

3) The DPSRAM is not owned. By default, the Global bus master is granted access to the DPSRAM.

As shown in Figure 7–1, on the previous page, there are two semaphores associated with each Dual Port SRAM bank, one between the SRAM and the V–bus and one between the SRAM and the Global bus. Be aware, however, that when a semaphore is claimed via the V–bus, the Global semaphore register is NOT updated to reflect this, and neither is the appropriate processor's V–bus register updated when a Global bus master claims a semaphore. **The only way to know for certain if a particular semaphore is available is to try to obtain it.** If you are granted the semaphore, then it was available; if you don't get it, then it wasn't. The procedure for obtaining a semaphore is a four–step sequence of reads and writes, which will be described later in this chapter (refer to Table 7–5, on page 193, for the address and bit locations of the Global Bus semaphores, and Table 7–3, on page 184, for the address and bit locations of the V–bus semaphores).

In addition to the semaphores and the 4 available SRAM banks, each of the four Dual Port SRAM blocks contains eight mailbox registers, which are connected to the 'C6x and VMEbus interrupt structures, and a ninth register which provides interrupt control and status information associated with the mailboxes. This structure is provided as a means to allow the various devices that can master the Dual Port SRAM to notify each other that new data has been placed by one for another, or that data left for one master by another has been read. Four of the mailbox registers are Read–Only, for incoming messages, and the other four are Read/Write accessible, for outgoing messages.

Table 7–1, on the next two pages, shows the complete memory map for the Global bus side of the Dual Port SRAM resources on the Model 4290/4291, from the point of view of a 'C6x Processor's V–bus. Please note that all addresses given in Table 7–1 are V–bus addresses that are mapped into the Global bus space via the Page Register (at V–bus address 0x0028 0024), and that in order to access any of these resources, a 'C6x processor must first set the Page Register to 0x0050.

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7.1 Overview of Dual–Port SRAMs on the Model 4290/4291 (continued)

Table 7–1: Model 4290/4291 –Memory Map for Global Bus Side of Dual Port SRAM – Addresses for 'C6x V-bus Access - (Page Register Setting = 0x0000 0050)

Resource	Access	Option 244	Option 240
DPSRAM A, bank 0, Global Port	R/W	0x0000 0000 : 0x0000 3FFF	0x0000 0000 : 0x0000 1FFF
DPSRAM A, bank 1, Global Port		0x0000 4000 : 0x0000 7FFF	0x0000 2000 : 0x0000 3FFF
DPSRAM A, bank 2, Global Port		0x0000 8000 : 0x0000 BFFF	0x0000 4000 : 0x0000 5FFF
DPSRAM A, bank 3, Global Port		0x0000 C000 : 0x0000 FFFF	0x0000 6000 : 0x0000 7FFF
Reserved	—	0x0001 0000 : 0x0003 FFFF	0x0000 8000 : 0x0003 FFFF
Reserved		0x0004 0000 : 0x0004 007F	
Global Port A -> V-bus A DPSRAM Mailbox	R/W	0x0004 0080	
Global Port C -> V-bus A DPSRAM Mailbox		0x0004 0084	
Global Port D -> V-bus A DPSRAM Mailbox		0x0004 0088	
Global Port B -> V-bus A DPSRAM Mailbox		0x0004 008C	
V-bus A -> Global Port A DPSRAM Mailbox	R. O.	0x0004 0090	
V-bus A -> Global Port C DPSRAM Mailbox		0x0004 0094	
V-bus A -> Global Port D DPSRAM Mailbox		0x0004 0098	
V-bus A -> Global Port B DPSRAM Mailbox		0x0004 009C	
DP Interrupt Control/Status Register A	R/W	0x0004 00A0	
Reserved	—	0x0004 00A4 : 0x0007 FFFF	
DPSRAM C, bank 0, Global Port	R/W	0x0008 0000 : 0x0008 3FFF	0x0008 0000 : 0x0008 1FFF
DPSRAM C, bank 1, Global Port		0x0008 4000 : 0x0008 7FFF	0x0008 2000 : 0x0008 3FFF
DPSRAM C, bank 2, Global Port		0x0008 8000 : 0x0008 BFFF	0x0008 4000 : 0x0008 5FFF
DPSRAM C, bank 3, Global Port		0x0008 C000 : 0x0008 FFFF	0x0008 6000 : 0x0008 7FFF
Reserved	—	0x0009 0000 : 0x000B FFFF	0x0008 8000 : 0x000B FFFF
Reserved		0x000C 0000 : 0x000C 007F	
Global Port A -> V-bus C DPSRAM Mailbox	R/W	0x000C 0080	
Global Port C -> V-bus C DPSRAM Mailbox		0x000C 0084	
Global Port D -> V-bus C DPSRAM Mailbox		0x000C 0088	
Global Port B -> V-bus C DPSRAM Mailbox		0x000C 008C	
V-bus C -> Global Port A DPSRAM Mailbox	R. O.	0x000C 0090	
V-bus C -> Global Port C DPSRAM Mailbox		0x000C 0094	
V-bus C -> Global Port D DPSRAM Mailbox		0x000C 0098	
V-bus C -> Global Port B DPSRAM Mailbox		0x000C 009C	
DP Interrupt Control/Status Register C	R/W	0x000C 00A0	
Reserved	—	0x000C 00A4 : 0x000F FFFF	

NOTES:
The Page Register MUST be set to 0x0000 0050 BEFORE any attempt to access the Dual Port SRAM via the Global bus.
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.
Table 7-1 is continued on the next page

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7.1 Overview of Dual–Port SRAMs on the Model 4290/4291 (continued)

Table 7-1: Model 4290/4291 –Memory Map for Global Bus Side of Dual Port SRAM – Addresses for 'C6x V-bus Access - (Page Register Setting = 0x0000 0050) (continued)

Resource	Access	Option 244	Option 240
DPSRAM D, bank 0, Global Port	R/W	0x0010 0000 : 0x0010 3FFF	0x0010 0000 : 0x0010 1FFF
DPSRAM D, bank 1, Global Port		0x0010 4000 : 0x0010 7FFF	0x0010 2000 : 0x0010 3FFF
DPSRAM D, bank 2, Global Port		0x0010 8000 : 0x0010 BFFF	0x0010 4000 : 0x0010 5FFF
DPSRAM D, bank 3, Global Port		0x0010 C000 : 0x0010 FFFF	0x0010 6000 : 0x0010 7FFF
Reserved	—	0x0011 0000 : 0x0013 FFFF	0x0010 8000 : 0x0013 FFFF
Reserved		0x0014 0000 : 0x0014 007F	
Global Port A -> V-bus D DPSRAM Mailbox	R/W	0x0014 0080	
Global Port C -> V-bus D DPSRAM Mailbox		0x0014 0084	
Global Port D -> V-bus D DPSRAM Mailbox		0x0014 0088	
Global Port B -> V-bus D DPSRAM Mailbox		0x0014 008C	
V-bus D -> Global Port A DPSRAM Mailbox	R. O.	0x0014 0090	
V-bus D -> Global Port C DPSRAM Mailbox		0x0014 0094	
V-bus D -> Global Port D DPSRAM Mailbox		0x0014 0098	
V-bus D -> Global Port B DPSRAM Mailbox		0x0014 009C	
DP Interrupt Control/Status Register D	R/W	0x0014 00A0	
Reserved	—	0x0014 00A4 : 0x0017 FFFF	
DPSRAM B, bank 0, Global Port	R/W	0x0018 0000 : 0x0018 3FFF	0x0018 0000 : 0x0018 1FFF
DPSRAM B, bank 1, Global Port		0x0018 4000 : 0x0018 7FFF	0x0018 2000 : 0x0018 3FFF
DPSRAM B, bank 2, Global Port		0x0018 8000 : 0x0018 BFFF	0x0018 4000 : 0x0018 5FFF
DPSRAM B, bank 3, Global Port		0x0018 C000 : 0x0018 FFFF	0x0018 6000 : 0x0018 7FFF
Reserved	—	0x0019 0000 : 0x001B FFFF	0x0018 8000 : 0x001B FFFF
Reserved		0x001C 0000 : 0x001C 007F	
Global Port A -> V-bus B DPSRAM Mailbox	R/W	0x001C 0080	
Global Port C -> V-bus B DPSRAM Mailbox		0x001C 0084	
Global Port D -> V-bus B DPSRAM Mailbox		0x001C 0088	
Global Port B -> V-bus B DPSRAM Mailbox		0x001C 008C	
V-bus B -> Global Port A DPSRAM Mailbox	R. O.	0x001C 0090	
V-bus B -> Global Port C DPSRAM Mailbox		0x001C 0094	
V-bus B -> Global Port D DPSRAM Mailbox		0x001C 0098	
V-bus B -> Global Port B DPSRAM Mailbox		0x001C 009C	
DP Interrupt Control/Status Register B	R/W	0x001C 00A0	
Reserved	—	0x001C 00A4 : 0x001F FFFF	

NOTES:
The Page Register MUST be set to 0x0000 0050 BEFORE any attempt to access the Dual Port SRAM via the Global bus.
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.

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7.2 Local Access to the Dual Port SRAM

'C6x Address Region – 0x0020 0000 : 0x0023 FFFF

Each 'C6x processor on the Model 4290/4291 has access to the Dual Port SRAM block located on its own V–bus, in the address range from 0x0020 0000 to 0x0023 FFFF. This resource differs from the others that are accessible from the processor's V–bus, however, in that the processor **DOES NOT HAVE EXCLUSIVE ACCESS** to the Dual Port SRAM, as it does to all the other V–bus resources. (One might want to raise the argument that the inter–processor Bi–FIFOs are all available for access to two processors each. However, each processor has exclusive access to it's own Bi–FIFO port, thus there will never be contention for the Bi–FIFOs). All 16 Dual Port SRAM banks on the Model 4290/4291 are accessible to all four 'C6x processors and to the VMEbus. Therefore, even before attempting to write to any of its "own" Dual Port SRAM blocks, the processor must first obtain a semaphore for that block from its Local Semaphore Register, located at V–bus address 0x0028 0028, and described in Section 7.2.1.

Table 7–2, below, shows the complete memory map for the local (V–bus) side of the Dual Port SRAM resources (including the mailboxes) on the Model 4290/4291 from the point of view of a 'C6x Processor's Local bus.

Table 7-2: Model 4290/4291 –Memory Map for Local (V-bus) Side of Dual Port SRAM

Resource	Access	Option 244	Option 240
DPSRAM, bank 0, Local Port	R/W	0x0020 0000 : 0x0020 3FFF	0x0020 0000 : 0x0020 1FFF
DPSRAM, bank 1, Local Port		0x0020 4000 : 0x0020 7FFF	0x0020 2000 : 0x0020 3FFF
DPSRAM, bank 2, Local Port		0x0020 8000 : 0x0020 BFFF	0x0020 4000 : 0x0020 5FFF
DPSRAM, bank 3, Local Port		0x0020 C000 : 0x0020 FFFF	0x0020 6000 : 0x0020 7FFF
Reserved	—	0x0021 0000 : 0x0023 FFFF	0x0020 8000 : 0x0023 FFFF
Reserved		0x0024 0000 : 0x0024 007F	
V-bus -> Global Port A DPSRAM Mailbox	R/W	0x0024 0080	
V-bus -> Global Port C DPSRAM Mailbox		0x0024 0084	
V-bus -> Global Port D DPSRAM Mailbox		0x0024 0088	
V-bus -> Global Port B DPSRAM Mailbox		0x0024 008C	
Global Port A -> V-bus DPSRAM Mailbox	R. O.	0x0024 0090	
Global Port C -> V-bus DPSRAM Mailbox		0x0024 0094	
Global Port D -> V-bus DPSRAM Mailbox		0x0024 0098	
Global Port B -> V-bus DPSRAM Mailbox		0x0024 009C	
Local DP Interrupt Control/Status Register	R/W	0x0024 00A0	
Reserved	—	0x0024 00A4 : 0x0027 FFFF	
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.			

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7.2 Local Access to the Dual Port SRAM (continued)

7.2.1 Local Semaphore Register (LSR)

'C6x Address – 0x0028 0028

The four MSBs of the Local Semaphore Registers (D15 : D12) contain the semaphores for the four banks of Dual Port SRAM that are locally accessible to each processor on its V–bus. These four banks of SRAM are also accessible from the global bus, and access to them is controlled by a set of interlocking semaphores. The remaining twelve bits are general purpose global bus sema–phores, which the user may implement at his own discretion for any of the shared resources on the global bus. Each 'C6x processor on the Model 4290/ 4291 has a unique copy of this register.

A separate register, located on the Global bus (at address 0x00E0 0000 (i. e., VME address VME_base+0x00E0 0000)) holds the semaphores for Global bus access to the Dual Port SRAM banks. Be aware, however, that when a semaphore is claimed via the Global bus, this local semaphore register is NOT updated to reflect that fact, and neither is the Global register updated when a local processor claims a semaphore. **The only way to know for certain if a particular semaphore is available is to try to obtain it.** If you are granted the semaphore, then it was available; if you don't get it, then it wasn't. The procdure for obtaining any of the local or global semaphores is a four–step sequence of reads and writes, which is shown below.

1) **READ** the bit associated with the DPSRAM semaphore in question. A logic '0' in a given bit indicates that the semaphore for that bank has not been claimed from the register you are reading (it may, however, have been claimed via the other register). A logic '1' in a given bit indicates that the semaphore for that bank is not available. The processor should continue to read this bit until a '0' is returned before proceeding.

2) **WRITE** a '1' to the bit associated with the DPSRAM semaphore in question to request the semaphore. Remember, however, that the nature of multi–processing systems is such that any shared resource is likely to be requested by more than one master at any given time. Just because the semaphore has been requested does NOT mean that it has been granted.

3) **READ** the bit associated with the DPSRAM semaphore in question once again. A logic '1' in that bit indicates that the request for the semaphore has been granted. If the bit reads back in the logic '0' state, then the semaphore has NOT been granted. At this point, the processor that needs the semaphore should return to the step (1) of this procedure, and loop through steps (1) – (3) until a '1' is returned in this step before proceeding.

4) Once the semaphore has been granted, the processor is free to access the bank for reads and writes for as long as it holds the semaphore. When exclusive access to the bank is no longer required, the processor should **WRITE** a '0' to the semaphore bit, to release the semaphore and make it available to other master devices.

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7.2 Local Access to the Dual Port SRAM (continued)

7.2.1 Local Semaphore Register (continued)

Table 7–3, below, shows the contents of the Local Semaphore register.

Table 7–3: Model 4290/4291 –Local Semaphore Register (LSR) –R/W @ 0x0028 0028

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Local_DP_ Semaphore_3	Local_DP_ Semaphore_2	Local_DP_ Semaphore_1	Local_DP_ Semaphore_0	GP_Global_ Semaphore_11	GP_Global_ Semaphore_10	GP_Global_ Semaphore_9	GP_Global_ Semaphore_8
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	GP_Global_ Semaphore_7	GP_Global_ Semaphore_6	GP_Global_ Semaphore_5	GP_Global_ Semaphore_4	GP_Global_ Semaphore_3	GP_Global_ Semaphore_2	GP_Global_ Semaphore_1	GP_Global_ Semaphore_0
Bit Function	1) Read '0' to check availability 2) Write '1' to request ownership				3) Read '1' to verify ownership 4) Write '0' to release			
All bits in this register are cleared to the logic '0' state by boot and reset operations.								



1) **When a given processor tries to obtain a semaphore from its LOCAL Semaphore Register (which no other device can access), the initial read operation (Step 1, above) may be omitted.**
2) **Any access to a Dual Port SRAM bank by a master that DOES NOT own the semaphore for that bank will be correctly acknowledged. However, read accesses without semaphore ownership will return non–deterministic data, and write accesses without the semaphore will not change the content of the allegedly accessed address. Consistent use of the semaphore structure is, therefore, HIGHLY RECOMMENDED.**

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7.2 Local Access to the Dual Port SRAM (continued)

7.2.2 Local Access to Dual Port SRAM Mailbox Registers

'C6x Address Region – 0x0024 0000 : 0x0027 FFFF

Each of the four Dual Port SRAM blocks contains eight mailbox registers, which are connected to the 'C6x and VMEbus interrupt structures, and a ninth register which provides control and status information for interrupts to the 'C6x processors associated with the mailboxes. This structure is provided as a means to allow any device that can master the Dual Port SRAM to notify any other potential Dual Port master that new data has been placed for the other master, or that the data left by one master for another has been taken. Four of the mailbox registers are Read–Only, for incoming messages, and the other four are Read/Write accessible, for outgoing messages. Each of the four out–going mailboxes is associated one of the four DSPs on the Model 4290/4291, as are each of the four incoming mailboxes. This arrangement, of course, pro–vides each processor with the dubiously useful ability to write a mailbox message that will interrupt itself, but it also keeps the memory maps for the four processors identical, which was our intent. Figure 7–2, on the next page, depicts the organization of the Dual Port SRAM mailboxes on one processor's V–bus, as seen from the local processor's point of view. As the figure shows, the same mailbox that is used for incoming messages from the Local (V–bus) point of view is used for outgoing messages from the Global bus's viewpoint. That mailbox is Read–Only accessible from the V–bus, but is Read/Write from the Global bus. (Compare this figure with Figure 7–3, on page 195, which shows the same resources from the Global bus's perspective.)

The DPSRAM mailbox registers are commonly used to pass data between two 'C6x processors. The example presented on the page after next illustrates the use of the DPSRAM mailbox registers. In this example, Processor A sends a message to Processor C to cause an interrupt, but any two 'C6x processors could have been used. The Dual Port SRAM Mailbox Interrupt Control Regis–ter (DICR) that is referred to in the example is discussed in Section 7.2.3, which begins at the top of page 188.



The Dual Port SRAM mailbox registers, like the SRAM itself, are 32-bit wide devices. They are composed of two 16-bit wide ICs, one for D0 : D15, the other for D16 : D31. The interrupt is generated by the chip used for the UPPER 16 bits. Therefore, any write to a mailbox write that is intended to cause an interrupt MUST INCLUDE THE UPPER 16 BITS.

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7.2 Local Access to the Dual Port SRAM (continued)

7.2.2 Local Access to Dual Port SRAM Mailbox Registers (continued)

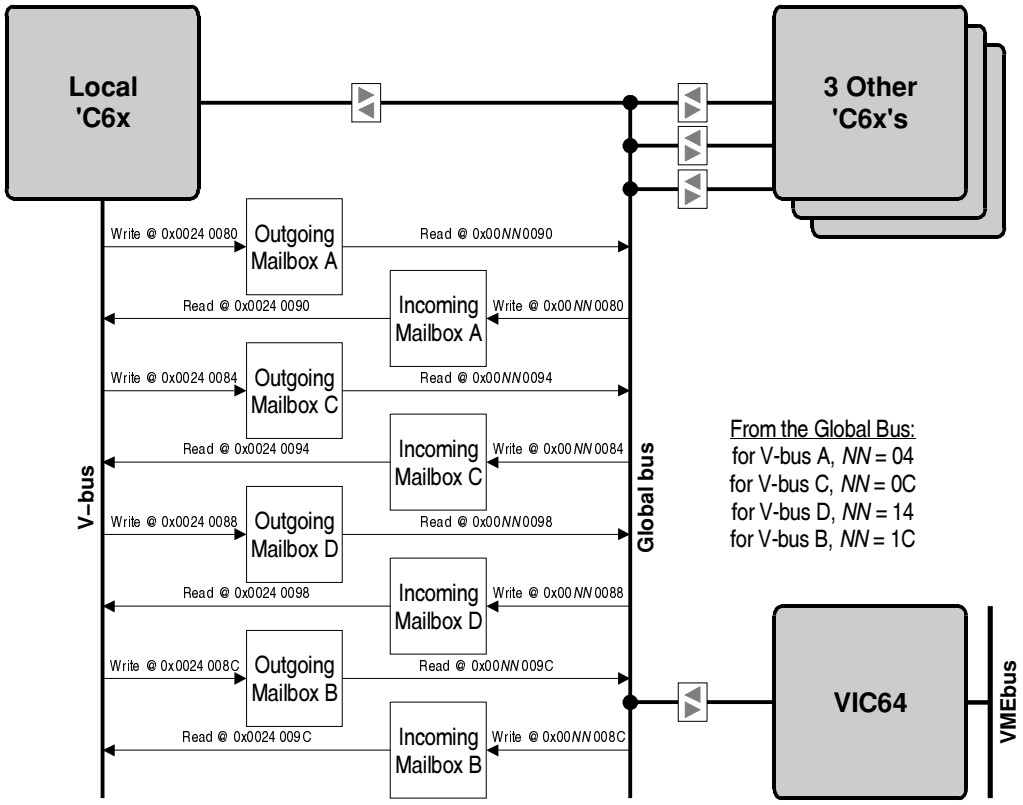


Figure 7-2: Model 4290/91 –Dual Port Mailbox Organization – Local Bus (V-bus) Viewpoint

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7.2 Local Access to the Dual Port SRAM (continued)

7.2.2 Local Access to Dual Port SRAM Mailbox Registers (continued)

Dual-Port Mailbox Interrupt Example

Processor C
Setting up the Interrupt

1) **Cleanup from prior interrupts:** Clear the 4290/4291's MIVR, @ 0x0028 0018, and the 'C6x's internal ICR.
2) **Enable 'C6x EXT_INT6:** OR 0x0040 into the 'C6x's internal IER.
3) **Setup local handlers:** Use `isr_jump_table[INT6]` to setup the handler for the 'C6x interrupt.
4) **Select the desired mailbox interrupt:** Clear D0 @ 0x0024 00A0 to the logic '0' state. This is the Interrupt Mask bit for the Mailbox from Processor A in the DICR.
5) **Enable the mailbox interrupt:** Set D12 @ 0x0028 0018 to the logic '1' state. This is the dual port mailbox interrupt enable bit in the MIVR register.
6) **Enable 'C6x Global Interrupts:** OR 0x0001 into the 'C6x's internal CSR.

Processor A
Generating the Interrupt

1) **Set the Page Register for DPSRAM access :** Write 0x0050 to address 0x0028 0024
2) **Write the mailbox to assert the interrupt:** Write data to 0x000C 0080. This address is the Global Port A to V–bus C DPSRAM mailbox.

NOTE: This step must be performed after the mailbox interrupt is enabled by the receiving processor.

Processor C
Handling the Interrupt

1) **Determine the interrupt source:** Read the Source field (D7:D4) in the DICR @ 0x0024 00A0 – a logic '0' in D4 identifies the source of the interrupt as the incoming mailbox from Processor A
2) **Read the local mailbox:** Read @ 0x0024 0090. This is the Incoming Mailbox from Processor A. Reading the mailbox clears the interrupt.
3) **Clear Dual Port Interrupt Flag:** Set D11 of the MIVR, @ 0x0028 0018 to the logic '1' state.
4) **Clear the 'C6x's internal ICR:** Write 0x40 to the ICR to clear the register.

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7.2 Local Access to the Dual Port SRAM (continued)

7.2.3 Dual Port SRAM Mailbox Interrupt Control Register (DICR)

'C6x Address : 0x0024 00A0 (R/W)

The Dual Port SRAM Mailbox Interrupt Control Register (DICR) contains three four–bit fields. Interrupts from the Dual Port SRAM mailboxes are asserted on the EXT_INT6 inputs of the 'C6x processors on the standard Model 4290/4291 (on the 4290/4291 Option 330, this interrupt is mappable, see Section 4.3.2.9). One bit in each field is associated with the Dual Port SRAM Mailbox registers for one 'C6x processor. The three fields are the read–only Status field (D27 : D24), the Cause field (D23 : D20) and the Mask field (D19 : D16). For each field, the MSB is associated with the Processor B Dual Port Mailbox, the NMSB bit is associated with Processor D's, the NLSB with Processor C's and the LSB is associated with the mailbox for Processor A. The structure of this register is illustrated in Table 7–4, below. The use of the three bitfields is described in the subsections that begin on the next page.

Table 7–4: Model 4290/91 –Dual Port SRAM Mailbox Interrupt Control Register (DICR) –R/W 0x0024 00A0

Bit #	D31	D30	D29	D28	D27*	D26*	D25*	D24*
Bit Name	Reserved				DP_Mailbox _Status_B*	DP_Mailbox _Status_D*	DP_Mailbox _Status_C*	DP_Mailbox _Status_A*
Bit Function	Write with Zeros Mask when Reading				1 = No New Data 0 = New Data in Mailbox			
Bit #	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
Bit Name	Int_From_ Mailbox_B	Int_From_ Mailbox_D	Int_From_ Mailbox_C	Int_From_ Mailbox_A	Mailbox_B Int_Mask	Mailbox_D Int_Mask	Mailbox_C Int_Mask	Mailbox_A Int_Mask
Bit Function	1 = No Interrupt from this mailbox 0 = Interrupt from this mailbox				1 = Interrupt Disabled (Masked) 0 = Interrupt Enabled			
Bit #	**D 1 5 - D 0**							
Name	Reserved							
Function	Write with Zeros, Mask when Reading							

*** –These bits are Read–Only**
Reset and boot operations initialize this register to the value 0x0FFE.
(Only mailbox A interrupt is enabled, no mailbox interrupts asserted, no data in mailboxes)

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7.2 Local Access to the Dual Port SRAM (continued)

7.2.3 Dual Port SRAM Mailbox Interrupt Control Register (continued)

7.2.3.1 Dual Port SRAM Mailbox Status Field – D11 : D8 – Read–Only

The bits in this field give the current, real–time status of the Dual Port SRAM mailbox for the associated processor. D11 is associated with Mailbox B, D10 with Mailbox D, D9 with C and D8 is associated with Mailbox A. All four bits default to the logic '1' state on reset or boot. When new data is placed in a given mailbox, the associated bit is cleared to the logic '0' state. When the local processor reads the mailbox, the bit gets set to the logic '1' state.

7.2.3.2 Dual Port SRAM Mailbox Interrupt Source Field – D7 : D4

When a 'C6x Processor on a standard Model 4290/4291 receives an interrupt on its EXT_INT6 input (or for Option 330, on the interrupt input that Dual Port Mailbox Interrupts are mapped to, see Section 4.3.2.9) this is the bit field that the processor can read to determine the source of the interrupt. Each of the four bits in this field is associated with one of the DPSRAM mailboxes – D7 is associated with Mailbox B, D6 with Mailbox D, D5 with C and D4 is associated with Mailbox A. All four bits default to the logic '1' state on reset or boot. A logic '0' on readback indicates the mailbox that caused the interrupt.



The Dual Port SRAM mailbox registers, like the SRAM itself, are 32-bit wide devices. They are composed of two 16-bit wide ICs, one for D0 : D15, the other for D16 : D31. The interrupt is generated by the chip used for the UPPER 16 bits. Therefore, any write to a mailbox write that is intended to cause an interrupt MUST INCLUDE THE UPPER 16 BITS.

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7.2 Local Access to the Dual Port SRAM (continued)

7.2.3 Dual Port SRAM Mailbox Interrupt Control Register (continued)

7.2.3.3 Dual Port SRAM Mailbox Interrupt Mask Field – D3 : D0

This settings of bits in this field can allow the Status bits discussed above (see Section 7.2.3.1) to assert interrupts on the associated DSPs, or prevent such interrupts from occuring. D3 is associated with Mailbox B, D2 with Mailbox D, D1 with C and D0 is associated with Mailbox A's status. Clearing one of these bits to the logic '0' state allows (or enables) the assertion of an interrupt on the local DSP when new data appears in the associated mailbox. Setting a bit to the logic '1' state disables (or masks) these interrupts. Reset and boot operations clear D0 and set D1 : D3, which means that Mailbox A interrupts are enabled and the other three mailbox interrupts are masked.



In addition to clearing the selected Interrupt Mask bit in this register, the Dual Port Mailbox Interrupt Enable bit (D12) in the MIVR (0x0028 0018) must also be set, to allow the interrupt to reach the processor.

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7.3 Global Access to the Dual Port SRAM

'C6x Address Region – 0x0000 0000 : 0x001F FFFF
Page Register – 0x0000 0050
Base Offsets –
DPSRAM A – 0x0000 0000 DP A Mailboxes – 0x0004 0080
DPSRAM C – 0x0008 0000 DP C Mailboxes – 0x000C 0080
DPSRAM D – 0x0010 0000 DP D Mailboxes – 0x0014 0080
DPSRAM B – 0x0018 0000 DP B Mailboxes – 0x001C 0080

VMEbus Address Region – VME_base+0x00A0 0000 : VME_base+0x00BF FFFF
Base Offsets –
DPSRAM A – 0x00A0 0000 DP A Mailboxes – 0x00A4 0200
DPSRAM C – 0x00A8 0000 DP C Mailboxes – 0x00AC 0200
DPSRAM D – 0x00B0 0000 DP D Mailboxes – 0x00B4 0200
DPSRAM B – 0x00B8 0000 DP B Mailboxes – 0x00BC 0200
Global Bus Address Region – 0x00A0 0000 : 0x00BF FFFF

Any device that can master the Global bus on the Model 4290/4291 can also gain master access to any bank of Dual Port SRAM via the board's Global bus. This includes all four 'C6x processors on the board, and any external device that becomes a VMEbus master of the 4290/4291. Table 7–1, on pages 180 and 181, shows the Memory Map used by 'C6x processors to access the Dual Port SRAM banks and mailboxes. Table 7–7, on pages 196 and 197, gives the addresses used by VMEbus masters for access to the same resources.

Mastering the Dual Port SRAM on this device, though, is not simply a matter of reading or writing to a given address range. Because this powerful resource is shared among several different devices, and because four of the potential masters have access to portions of the resource via two different paths (each 'C6x can also access 4 banks of the Dual Port SRAM via its Local bus (also known as the V–bus)), access is controlled by a system of semaphores. Any device that wants to master a given Dual Port SRAM bank must first obtain the semaphore for that bank. Separate registers are provided for the V–bus and Global bus semaphores to each bank. Each 'C6x processor has a unique copy of the Local Semaphore Register (LSR), at V–bus address 0x0028 0028 (see Section 7.2.1) which holds the semaphores for the four locally accessible SRAM banks. A single Global Semaphore Register holds semaphores for all 16 banks of the Dual Port SRAM. This register will be discussed in Section 7.3.1, at the top of the next page. It is important to remember that when a semaphore for a given bank of Dual Port SRAM is obtained from one of these registers, the bit that represents that semaphore in the other register is NOT updated to reflect that fact. **The only way to know for certain if a particular semaphore is available is to try to obtain it.** If you are granted the semaphore, then it was available; if you don't get it, then it wasn't. The procdure for obtaining any of the local or global semaphores is a four–step sequence of reads and writes, which will also be discussed in Section 7.3.1.

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7.3 Global Access to the Dual Port SRAM (continued)

7.3.1 Global Dual Port SRAM Semaphore Register (DPSR)

'C6x Address – 0x0000 0000
Page Register – 0x0000 0070
Base Offset – 0x0000 0000

VMEbus Address – VME_base+0x00E0 0000
Global Bus Address – 0x00E0 0000

Each Dual Port SRAM block is divided into four banks which are 'owned' by (i. e., accessible to) either the local 'C6x processor or whatever is the current master of the Global bus. At reset, the Global bus owns the semaphores for all four banks in all four blocks. Before accessing any bank, however, any Global bus master should verify that it does indeed still owns the semaphore it needs, by setting the page register appropriately (assuming it is one of the 'C6x's – the page register need not be set if an external VME processor is mastering the Global bus), then executing the Semaphore action sequence with the appro–priate bit in the Dual Port Semaphore Register on the Global bus. This sequence is accomplished by performing a series of read and write acceses to the register. Once the semaphore is obtained for a given bank, transfers (read or write) may proceed. Write accesses to banks for which the semaphore is not owned by the master are ignored (although correctly acknowledged) and reads in the absense of semaphore ownership return non–deterministic data.

The Semaphore for each bank of the Dual Port SRAM is acquired and then released in a four step operation. The first step of the sequence is to check the availability of the semaphore. If you read a '0' in the appropriate bit position, the semaphore may be available and you may request it, by writing a '1' to that bit position. Ownership of the semaphore is then verified by reading a '1' in the bit position after the request operation. After use of the bank is com–pleted, the controlling entity releases the semaphore by writing a '0' to it.

The programmer should be aware that separate, independent semaphore registers exist on each processor's V–bus (the Local Semaphore Registers, or LSRs), and on the Global bus. The four MSB's of a given processor's LSR (D15 : D12) represent the semaphores for that node's local DPSRAM block..



When a semaphore is claimed via the V-bus register, the Global Semaphore register is NOT updated to reflect this, and neither is the appropriate processor's V-bus register updated when a Global bus master claims a semaphore. As stated in previous sections, the only way to know for certain if a particular semaphoreis available is to try to get it.Success indicates that it was available; failure to obtain it means that it wasn't.

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7.3 Global Access to the Dual Port SRAM (continued)

7.3.1 Global Dual Port Semaphore Register (continued)

At any given time, a Dual Port SRAM bank can exist in one of three possible states:

1) The DPSRAM bank is owned by the local 'C6x processor, and is accessible via that DSP's V–bus. The bank is acquired by 'C6x through its Local Semaphore Register (LSR).

2) The DPSRAM bank is owned by a Global bus master (either a 'C6x or VME), and is accessible via the Global bus. The bank is acquired by the Global bus master through this register, the Global Dual Port Semaphore Register (DPSR).

3) The DPSRAM is not owned. By default, the Global bus master is granted access to the DPSRAM.

Table 7–5, below, shows the structure of the Global Dual Port SRAM Semaphore Register (DPSR). The upper 16 bits of this register's 32–bit memory location are unused. The remaining 16 bits are divided into four groups of four bits each, one group dedicated to each of the four DPSRAM blocks. One bit in each group controls the semaphore for one of the four banks in the associated block.

Table 7–5: Model 4290/4291 –Global Dual Port SRAM Semaphore Register (DPSR) – V–bus Access: R/W @ 0x0000 0000, Page Reg = 70 –Global Bus Access: R/W @ 0x00E0 0000 –VMEbus Access: R/W @ VME_base+0x00E0 0000

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Semaphore for . . .	DPSRAM_B _Bank_3	DPSRAM_B _Bank_2	DPSRAM_B _Bank_1	DPSRAM_B _Bank_0	DPSRAM_D _Bank 3	DPSRAM_D Bank 2	DPSRAM_D Bank 1	DPSRAM_D Bank 0
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Semaphore for . . .	DPSRAM_C _Bank_3	DPSRAM_C _Bank_2	DPSRAM_C _Bank_1	DPSRAM_C _Bank_0	DPSRAM_A _Bank 3	DPSRAM_A Bank 2	DPSRAM_A Bank 1	DPSRAM_A Bank 0

Semaphore Action Sequence –the following four–step sequence must be followed to obtain access to the Dual Port SRAM banks whose semaphores are controlled by the bits in this register –

Step **1** –**Read** a '**0**' in the associated bit **to check** the semaphore's **availability**
Step **2** - **Write** a '**1**' to the associated bit **to request ownership** of the semaphore
Step **3** - **Read** a '**1**' in the associated bit **to verify ownership** of the semaphore
Step **4** - **Write** a '**0**' to the associated bit **to release** the **semaphore** after completing the access.

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7.3 Global Access to the Dual Port SRAM (continued)

7.3.2 Global Access to Dual Port SRAM Mailboxes

Each of the four Dual Port SRAM blocks contains eight mailbox registers, which are connected to the VMEbus and 'C6x interrupt structures, and a ninth register which provides control and status information for interrupts to the 'C6x processors associated with the mailboxes. The mailboxes can also generate local interrupt request signals (LIRQs) to the VIC64, which can be used to generate interrupts to the VMEbus. This structure is provided as a means to allow any device that can master the Dual Port SRAM to notify any other potential Dual Port master that new data has been placed for the other master, or that the data left by one master for another has been taken. Four of the mailbox registers are Read–Only, for incoming messages, and the other four are Read/Write accessible, for outgoing messages. Each of the four outgoing mailboxes is associated one of the four DSPs on the Model 4290/4291, as are each of the four incoming mailboxes. Figure 7–3, on the next page, depicts the organization of the Dual Port SRAM mailboxes connected between the Global Bus and one processor's V–bus, with labels and addresses given from the Global bus's point of view. As the figure shows, the same mailbox that is used for incoming messages from the Global bus point of view is used for outgoing messages from the Local bus (V–bus) viewpoint. That mailbox is Read–Only accessible by a Global bus master, but is Read/Write from the V–bus. (Compare this figure with Figure 7–2, on page 186, which shows the same resources from the V–bus's perspective.)

As mentioned above, these mailboxes are generally used to generate interrupts to notify another bus master about the status of data in the Dual Port SRAM. Section 7.2.2 gave an example of how these interrupts would be used in a data exchnge between a pair of processors on a given Model 4290/4291. If the transaction in question was between a 'C6x processor and a VMEbus master, a VMEbus interrupt might need to be generated instead of a 'C6x interrupt. It was also stated previously that these mailboxes can also trigger local interrupt requests (LIRQs), which the VIC64 can map to VMEbus IRQs. Table 7–6, below, tells which LIRQ will be generated for a given mailbox message, as a function of which processor's V–bus that mailbox is connected to.

Table 7-6: Model 4290/4291 –VIC64 LIRQs Generated by DPSRAM Mailboxes

Mailbox on V-bus	Local IRQ Generated
Processor B	LIRQ7
Processor D	LIRQ6
Processor C	LIRQ5
Processor A	LIRQ4
NOTE: These LIRQs are listed in order of their priority.	

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7.3 Global Access to the Dual Port SRAM (continued)

7.3.2 Global Access to Dual Port SRAM Mailbox Registers (continued)

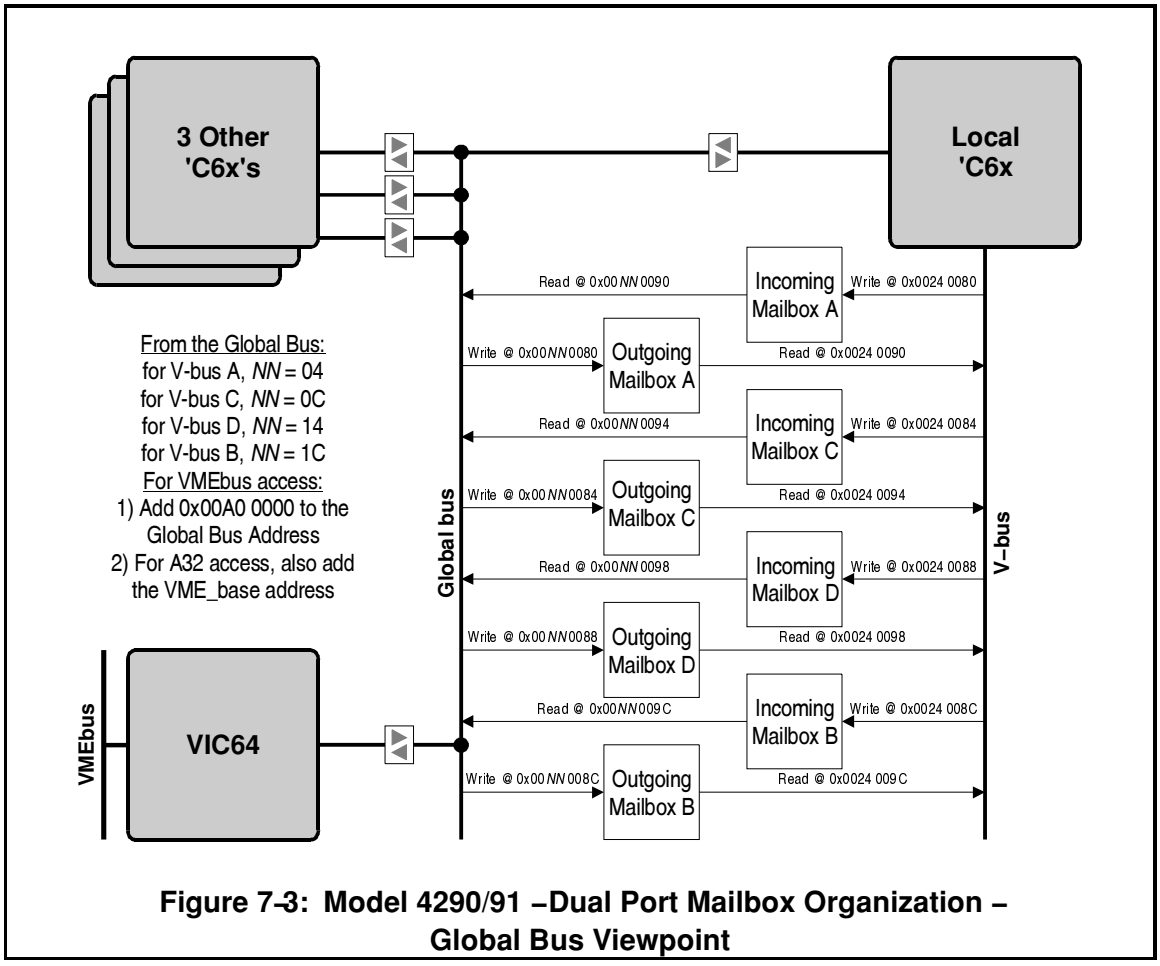


Figure 7-3: Model 4290/91 –Dual Port Mailbox Organization – Global Bus Viewpoint

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7.3 Global Access to the Dual Port SRAM (continued)

7.3.3 VMEbus Memory Map for Dual Port SRAM & Mailboxes

The addresses used by 'C6x processors to access the various Dual Port SRAM resources via the Global bus were given in Table 7–1, on pages 180 and 181. The addresses used by VMEbus masters to access these same resources are given in Table 7–7, which starts below and continues on the next page.

Table 7–7: Model 4290/4291 –Memory Map for Global Bus Side of Dual Port SRAM – VMEbus Address Offsets

Resource	Access	Option 244	Option 240
DPSRAM A, bank 0, Global Port	R/W	0x00A0 0000 : 0x00A0 3FFF	0x00A0 0000 : 0x00A0 1FFF
DPSRAM A, bank 1, Global Port		0x00A0 4000 : 0x00A0 7FFF	0x00A0 2000 : 0x00A0 3FFF
DPSRAM A, bank 2, Global Port		0x00A0 8000 : 0x00A0 BFFF	0x00A0 4000 : 0x00A0 5FFF
DPSRAM A, bank 3, Global Port		0x00A0 C000 : 0x00A0 FFFF	0x00A0 6000 : 0x00A0 7FFF
Reserved	—	0x00A1 0000: 0x00A3 FFFF	0x00A0 8000 : 0x00A3 FFFF
Reserved		0x00A4 0000 : 0x00A4 007F	
Global Port A -> V-bus A DPSRAM Mailbox	R/W	0x00A4 0080	
Global Port C-> V-bus A DPSRAM Mailbox		0x00A4 0084	
Global Port D -> V-bus A DPSRAM Mailbox		0x00A4 0088	
Global Port B -> V-bus A DPSRAM Mailbox		0x00A4 008C	
V-bus A -> Global Port A DPSRAM Mailbox	R. O.	0x00A4 0090	
V-bus A -> Global Port C DPSRAM Mailbox		0x00A4 0094	
V-bus A -> Global Port D DPSRAM Mailbox		0x00A4 0098	
V-bus A -> Global Port B DPSRAM Mailbox		0x00A4 009C	
DP Interrupt Control/Status Register A	R/W	0x00A4 00A0	
Reserved	—	0x00A4 00A4 : 0x00A7 FFFF	
DPSRAM C, bank 0, Global Port	R/W	0x00A8 0000 : 0x00A8 3FFF	0x00A8 0000 : 0x00A8 1FFF
DPSRAM C, bank 1, Global Port		0x00A8 4000 : 0x00A8 7FFF	0x00A8 2000 : 0x00A8 3FFF
DPSRAM C, bank 2, Global Port		0x00A8 8000 : 0x00A8 BFFF	0x00A8 4000 : 0x00A8 5FFF
DPSRAM C, bank 3, Global Port		0x00A8 C000 : 0x00A8 FFFF	0x00A8 6000 : 0x00A8 7FFF
Reserved	—	0x00A9 0000 : 0x00AB FFFF	0x00A8 8000 : 0x00AB FFFF
Reserved		0x00AC 0000 : 0x00AC 007F	
Global Port A -> V-bus C DPSRAM Mailbox	R/W	0x00AC 0080	
Global Port C -> V-bus C DPSRAM Mailbox		0x00AC 0084	
Global Port D -> V-bus C DPSRAM Mailbox		0x00AC 0088	
Global Port B -> V-bus C DPSRAM Mailbox		0x00AC 008C	
V-bus C -> Global Port A DPSRAM Mailbox	R. O.	0x00AC 0090	
V-bus C -> Global Port C DPSRAM Mailbox		0x00AC 0094	
V-bus C -> Global Port D DPSRAM Mailbox		0x00AC 0098	
V-bus C -> Global Port B DPSRAM Mailbox		0x00AC 009C	
DP Interrupt Control/Status Register C	R/W	0x00AC 00A0	
Reserved	—	0x00AC 00A4 : 0x00AF FFFF	

NOTES: The addresses given above are valid as shown for A24 VME slave access.
For A32 access, the A32_base address must be added to all addresses shown.
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.
Table 7-7 is continued on the next page

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7.3 Global Access to the Dual Port SRAM (continued)

7.3.3 VMEbus Memory Map for Dual Port SRAM & Mailboxes (continued)

Table 7-7: Model 4290/4291 –Global Bus Side of Dual Port SRAM – VMEbus Address Offsets (continued)

Resource	Access	Option 244	Option 240
DPSRAM D, bank 0, Global Port	R/W	0x00B0 0000 : 0x00B0 3FFF	0x00B0 0000 : 0x00B0 1FFF
DPSRAM D, bank 1, Global Port		0x00B0 4000 : 0x00B0 7FFF	0x00B0 2000 : 0x00B0 3FFF
DPSRAM D, bank 2, Global Port		0x00B0 8000 : 0x00B0 BFFF	0x00B0 4000 : 0x00B0 5FFF
DPSRAM D, bank 3, Global Port		0x00B0 C000 : 0x00B0 FFFF	0x00B0 6000 : 0x00B0 7FFF
Reserved	—	0x00B1 0000 : 0x00B3 FFFF	0x00B0 8000 : 0x00B3 FFFF
Reserved		0x00B4 0000 : 0x00B4 007F	
Global Port A -> V-bus D DPSRAM Mailbox	R/W	0x00B4 0080	
Global Port C -> V-bus D DPSRAM Mailbox		0x00B4 0084	
Global Port D -> V-bus D DPSRAM Mailbox		0x00B4 0088	
Global Port B -> V-bus D DPSRAM Mailbox		0x00B4 008C	
V-bus D -> Global Port A DPSRAM Mailbox	R. O.	0x00B4 0090	
V-bus D -> Global Port C DPSRAM Mailbox		0x00B4 0094	
V-bus D -> Global Port D DPSRAM Mailbox		0x00B4 0098	
V-bus D -> Global Port B DPSRAM Mailbox		0x00B4 009C	
DP Interrupt Control/Status Register D	R/W	0x00B4 00A0	
Reserved	—	0x00B4 00A4 : 0x00B7 FFFF	
DPSRAM B, bank 0, Global Port	R/W	0x00B8 0000 : 0x00B3 FFFF	0x00B8 0000 : 0x00B8 1FFF
DPSRAM B, bank 1, Global Port		0x00B8 4000 : 0x00B8 7FFF	0x00B8 2000 : 0x00B8 3FFF
DPSRAM B, bank 2, Global Port		0x00B8 8000 : 0x00B8 BFFF	0x00B8 4000 : 0x00B8 5FFF
DPSRAM B, bank 3, Global Port		0x00B8 C000 : 0x00B8 FFFF	0x00B8 6000 : 0x00B8 7FFF
Reserved	—	0x00B9 0000 : 0x00BB FFFF	0x00B8 8000 : 0x00BB FFFF
Reserved		0x00BC 0000 : 0x00BC 007F	
Global Port A -> V-bus B DPSRAM Mailbox	R/W	0x00BC 0080	
Global Port C -> V-bus B DPSRAM Mailbox		0x00BC 0084	
Global Port D -> V-bus B DPSRAM Mailbox		0x00BC 0088	
Global Port B -> V-bus B DPSRAM Mailbox		0x00BC 008C	
V-bus B -> Global Port A DPSRAM Mailbox	R. O.	0x00BC 0090	
V-bus B -> Global Port C DPSRAM Mailbox		0x00BC 0940	
V-bus B -> Global Port D DPSRAM Mailbox		0x00BC 0098	
V-bus B -> Global Port B DPSRAM Mailbox		0x00BC 009C	
DP Interrupt Control/Status Register B	R/W	0x00BC 00A0	
Reserved	—	0x00BC 00A4 : 0x00BF FFFF	

NOTES: The addresses given above are valid as shown for A24 VME slave access.
For A32 access, the A32_base address must be added to all addresses shown.
Read accesses to the Reserved regions will return non-deterministic data, write accesses will have no effect.

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Chapter 8: Model 4290/4291 Boot Sequence & Firmware

8.1 Introduction

When power is applied to the Model 4290/4291, or when the board is reset, a boot sequence is initiated. This chapter will discuss the steps in the factory default boot sequence and describe the actions a user can take to modify the boot sequence to meet his individual needs. Initial conditions of key registers at the conclusion of the factory default boot sequence will be discussed. This chapter will also include procedures for writing, downloading and executing code to make the Model 4290/4291 boot into an application of your own design.

The sections below will make reference to a processor−dependent location in the Glo−bal SRAM called the Boot_Flag. The key difference between the power−up boot and the reset boot is that on power−up, the flags are initialized to a value that forces a self test. On reset, the flags are not overwritten. Thus, a user may write the value that will cause the desired action to the Boot_Flag, then reset the unit and have that action occur.

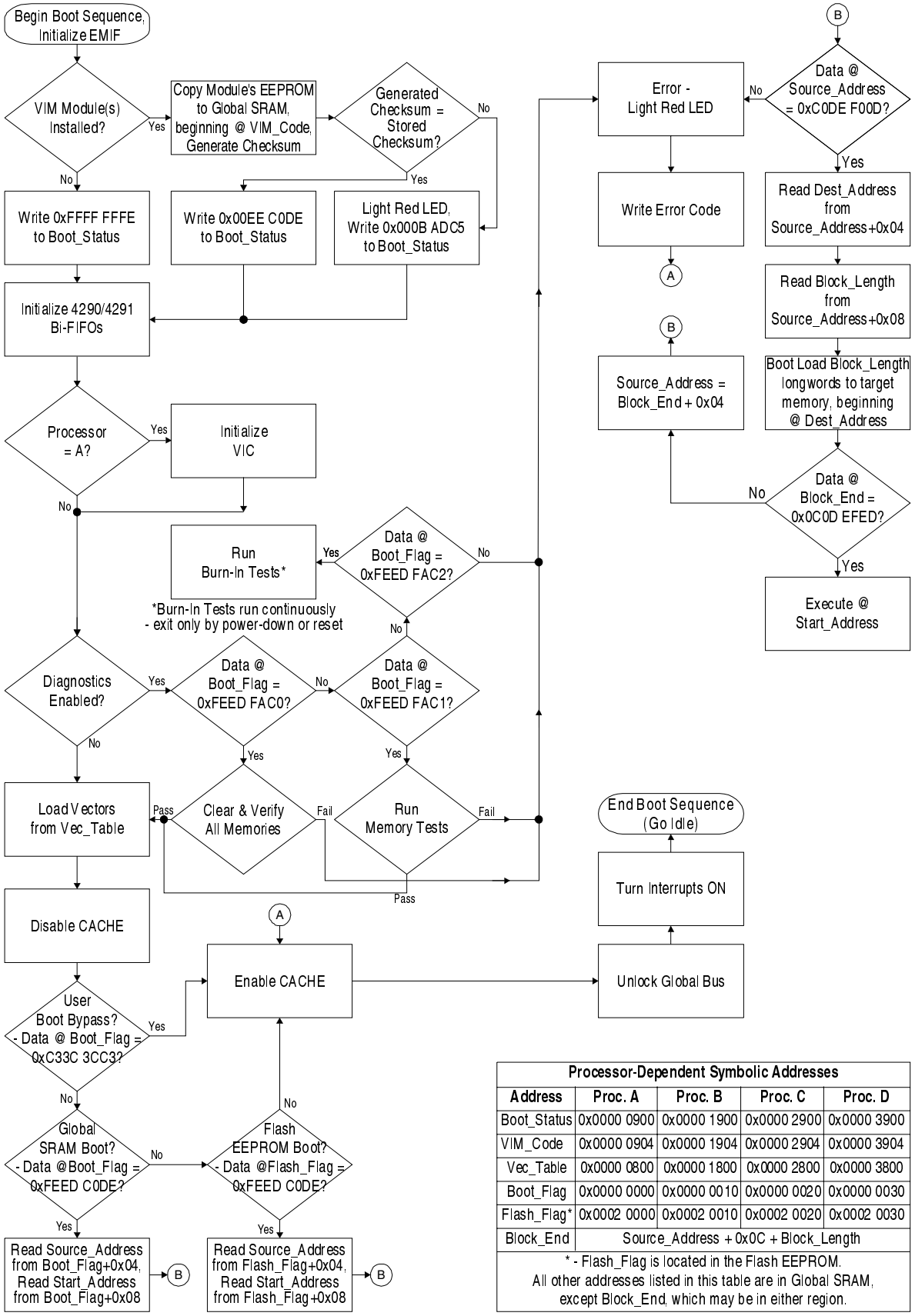
8.2 Model 4290/4291 Firmware Boot Sequence

Figure 8−1 on page 200 contains a flowchart showing the boot sequence for a Model 4290/4291, using the standard factory−installed firmware. For units equipped with Option 330, the sequence is slightly different, and is shown in Figure 8−2, on page 201. At power−up, each processor's EMIF control register is initialized to values that are dependent upon the specific unit's configuration. These are shown in Table 8−1, below. Each processor then copies the boot firmware from the Boot/User Flash EEPROM, on the Global Bus, to its own Local SDRAM, the resource that the boot code is executed from. The boot sequence starts with global bus interrupts disabled, and the C6x's internal cache memory enabled.

Table 8−1: Model 4290/4291 −EMIF Register Initialization Values

Resource	Address	Std. 4290 / 4291 (200 / 167 MHz)	4290 / 4291 Opt. 330 (200 / 167 MHz)
EMIF Global Control Register	0x0180 0000	0x0000 33EC	0x0000 33EC
EMIF CE0 Space Control Register	0x0180 0008	0x71B7 0723	0x71B7 0B23
EMIF CE1 Space Control Register	0x0180 0004	0x30B5 0321	0x0000 0040
EMIF CE2 Space Control Register	0x0180 0010	0x0XXX X030	0x0XXX X030
EMIF CE3 Space Control Register	0x0180 0014	0x0XXX X040	0x0XXX X040
EMIF SDRAM Control Register	0x0180 0018	0x0744 F000	0x0744 F000
EMIF SDRAM Timing Register	0x0180 001C	0x0006 1200	0x0006 1200
NOTE: X = These bitfields are initialized to 0, but their readback values are indeterminate.			

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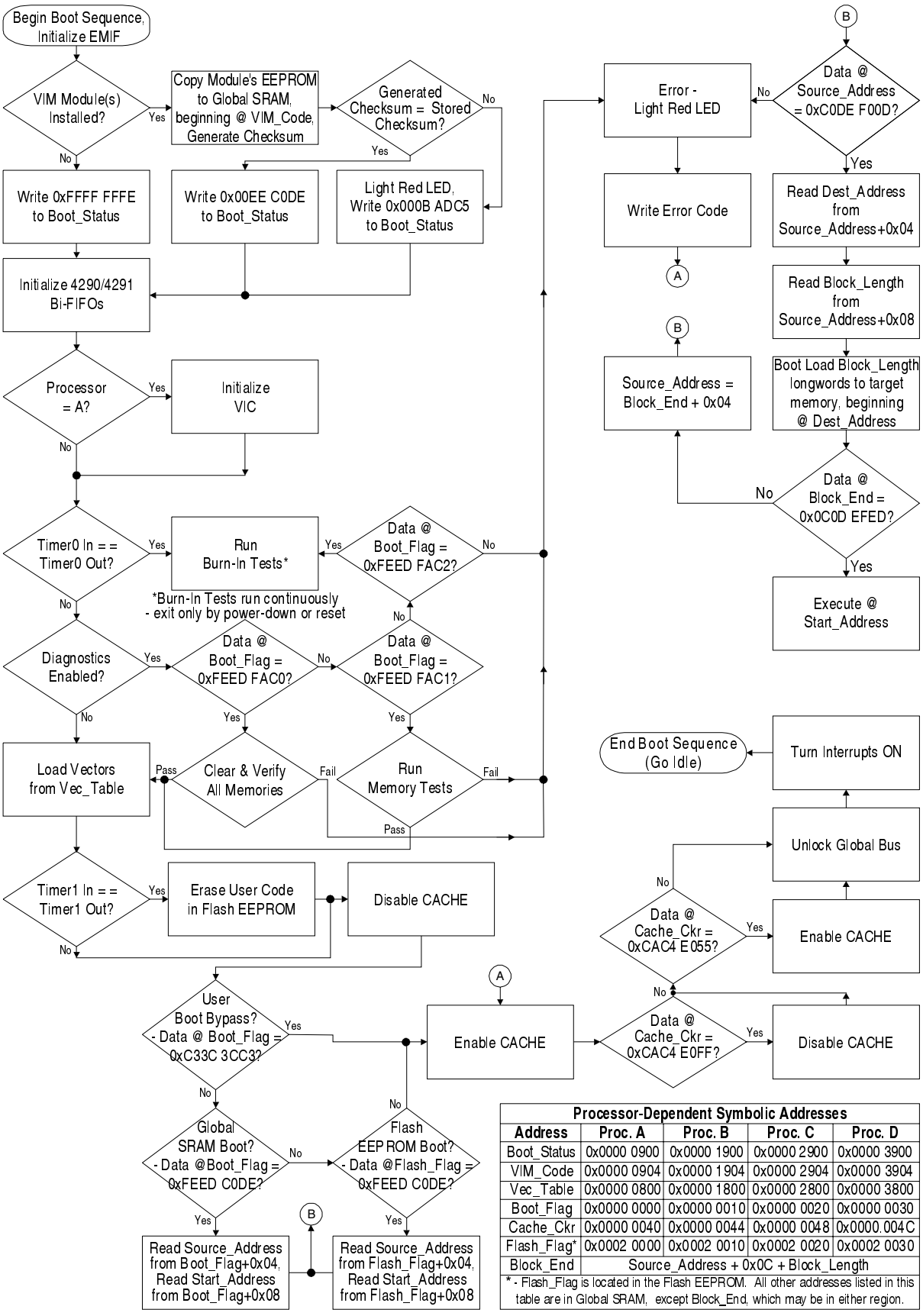


Processor-Dependent Symbolic Addresses				
Address	Proc. A	Proc. B	Proc. C	Proc. D
Boot_Status	0x0000 0900	0x0000 1900	0x0000 2900	0x0000 3900
VIM_Code	0x0000 0904	0x0000 1904	0x0000 2904	0x0000 3904
Vec_Table	0x0000 0800	0x0000 1800	0x0000 2800	0x0000 3800
Boot_Flag	0x0000 0000	0x0000 0010	0x0000 0020	0x0000 0030
Flash_Flag*	0x0002 0000	0x0002 0010	0x0002 0020	0x0002 0030
Block_End	Source_Address + 0x0C + Block_Length			

* - Flash_Flag is located in the Flash EEPROM.
All other addresses listed in this table are in Global SRAM, except Block_End, which may be in either region.

Figure 8-1: Standard Model 4290/4291 –Firmware Boot Sequence

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Processor-Dependent Symbolic Addresses

Address	Proc. A	Proc. B	Proc. C	Proc. D
Boot_Status	0x0000 0900	0x0000 1900	0x0000 2900	0x0000 3900
VIM_Code	0x0000 0904	0x0000 1904	0x0000 2904	0x0000 3904
Vec_Table	0x0000 0800	0x0000 1800	0x0000 2800	0x0000 3800
Boot_Flag	0x0000 0000	0x0000 0010	0x0000 0020	0x0000 0030
Cache_Ckr	0x0000 0040	0x0000 0044	0x0000 0048	0x0000.004C
Flash_Flag*	0x0002 0000	0x0002 0010	0x0002 0020	0x0002 0030
Block_End	Source_Address + 0x0C + Block_Length			

* - Flash_Flag is located in the Flash EEPROM. All other addresses listed in this table are in Global SRAM, except Block_End, which may be in either region.

Figure 8-2: Standard Model 4290/4291 Option 330 –Firmware Boot Sequence

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8.3 Checking for VIM Modules

When a VIM module is installed, the Expansion Daughterboard Present Output line (**NxDBPSNT**) on the node's VIM connector is grounded, which sets the D5 bit in the node's Board Configuration Register (BCR, at V–bus CE0 address 0x0028 0020) to the logic '1' state. The first thing a processor does in the boot routine is to look at that bit, to see if there is a VIM module installed. If the bit reads back as a logic '0', then no module is installed. In this case, the processor writes the code 0xFFFF FFFE to the processor–dependent Boot_Status location in Global SRAM (see Table 8–2, below).

Table 8–2: Model 4290/4291 –Boot_Status Locations in Global SRAM

Processor	Address
A	0x0000 0900
B	0x0000 1900
C	0x0000 2900
D	0x0000 3900

NOTE: For Global SRAM access from the 'C6x, the Page Register, at 'C6x Address 0x00280024, must be set to 0x40
If the bit reads back as a logic '0', then no module is installed.
If the bit reads back as a logic '1', then a VIM module is installed.

If the D5 bit in the BCR reads back as a logic '1', then a module is installed on the node's VIM interface. In this case, the processor begins copying the contents of the module's ID EEPROM into Global SRAM. The processor reads the EEPROM contents serially, via the EEPROM Readout Register at address 0x0032 0000, and writes this data into a processor–dependent region in the Global SRAM, whose starting address is given in Table 8–3, below.

Table 8–3: Model 4290/4291 –VIM ID EEPROM Transfer Locations in Global SRAM

Processor	Address
A	0x0000 0904
B	0x0000 1904
C	0x0000 2904
D	0x0000 3904

NOTE: For Global SRAM access from the 'C6x, the Page Register, at 'C6x Address 0x00280024, must be set to 0x40

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8.3 Checking for VIM Modules (continued)

The VIM module ID EEPROM is a 1 kbit device, containing 64 16−bit words. After all 64 words have been moved from the module's EEPROM into the appropriate Global SRAM locations, the processor generates a checksum from the first 62 words (i. e., words 0 – 61), and compares this generated checksum to the correct checksum, which is stored in the EEPROM's 64th word location (word 63 – word 62 always contains all zeros). If these checksums match, the processor writes the code word 0x00EE C0DE to its own Boot_Status location (see Table 8−2, on the previous page), and proceeds with the rest of the boot sequence. If the generated and stored checksums do not match, then an error has occurred. In this case, the processor writes the code word 0x000B ADC5 (the closest we could come to "Bad CS" using hex numbers) to its Boot_Status location (again, see Table 8−2, on the previous page for the processor−dependent loca−tion), and lights its red LED on the front panel, by setting the D0 bit in its Miscellaneous Control Register (at V−bus CE0 address 0x0028 001C) to the logic '1' state. Note that even though the red LED is lit, which usually indicates a failure, the processor may still be perfectly functional in this case, although it might not be able to access the VIM module.

8.4 Resource Initialization

After dealing with the VIM modules, the processors on the Model 4290/91 start initial−izing the resources they can access. Memory regions are set aside for interrupt service routines. Incoming VMEbus interrupts are temporarily disabled, and any pending VMEbus interrupts are cleared. All the BI−FIFOs are cleared, and the states of the board's various configuration jumpers are read from each node's Board Configuration Register (BCR, at V−bus CE0 address 0x0028 0020). Then each processor reads its Boot_Flag location, to determine what sort of diagnostic routines it should run.

Note that when power is applied to the Model 4290/4291 (or when a processor is reset), a very quick test is run on the Global SRAM. The contents of the Boot_Flag location, how−ever, are not changed when the device is reset. This allows a user to write the desired diagnostic code to that address and push the front panel reset button to initiate the desired self−testing mode, or to leave the flag cleared and boot without diagnostics.

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8.5 Memory Diagnostics

There are three levels of diagnostic routines that may be run at this stage of the boot routine, determined for each processor by the contents of its Boot_Flag locations. The addresses of the Boot_Flags, as a function of the processor's ID, are given in Table 8–4, below left.

Table 8-4: Model 4290/4291 - Boot_Flag Locations in Global SRAM

Processor	Address
A	0x0000 0000
B	0x0000 0010
C	0x0000 0020
D	0x0000 0030

Table 8-5: Model 4290/4291 - Diagnostic Codes at the Boot_Flag Address

Boot_Flag Contents	Diagnostic
0xFEED FAC0	Clear All Memories
0xFEED FAC1	Run Memory Tests
0xFEED FAC2	Run Burn-In Tests

Based on the content of the Boot_Flag address, one of three actions may be taken at this point. These are summarized in Table 8–5, above right. These tests are described in detail in the subsections that begin on the next page.

Note that these tests can be initiated at any time using the factory–supplied firmware's diagnostic functions and each processor's Memory Test Select Flag, located in the Global SRAM. There are actually five different memory tests which can be run separately, or in conjunction with each other, and the selected tests can be run once each or in an endless loop, depending on the contents of the Boot_Flag . Any or all of these five tests may be enabled by setting the appropriate bits at the Test Select Flag location to the logic '1' state. Any combination of the tests may be run in series. For example, writing 0x1F to address 0x0000 0804 runs all five tests on Processor A.

Table 8–6, below, illustrates the bits in the Memory Test Select Flag and tells which test is enabled by each bit. Each processor has its own flag, located at a different address. For Processor A, the address is 0x0000 0804, Processor B's flag is at 0x0000 1804, Processor C's is 0x0000 2804, and Processor D's is 0x0000 3804. The subsections that begin at the top of the next page describe the tests.

Table 8-6: Model 4290/4291 –Memory Test Select Flag –R/W @ 0x0000 z804

Bit #	D31 –D5	D4	D3	D2	D1	D0
Test	Reserved	Pattern Test	Reverse Test	Forward Test	Address in Address	Clear & Verify
Function	Write with 0's, Mask when reading	1 = Enable Test 0 = Disable Test				

NOTE: z = 0 for Processor A, 1 for Processor B, 2 for Processor C, and 3 for Processor D.

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8.5 Memory Diagnostics (continued)

8.5.1 Clear & Verify Memory – Bit D0

When the Clear & Verify Test is enabled (i. e., when bit D0 at the Memory Test Select Flag is set to the logic '1' state), the data value 0x0000 0000 is written to all memory locations to be tested. Each address is then read back. If any memory address contains any data other than 0, Error Code 0xE1 is written to the Self–Test Results location (see Table 8–7, on the page after next, for this processor–dependent address).

8.5.2 Address in Address Test – Bit D1

When the Address in Address Test is enabled (i. e., when bit D1 at the Memory Test Select Flag is set to the logic '1' state), each memory location to be tested is written with a data value equal to its own address. Each address is then read back. If any readback results in data different from the address that it is returned from, Error Code 0xE2 is is written to the Self–Test Results location (see Table 8–7, on the page after next, for this processor–dependent address).

8.5.3 Forward Memory Test – Bit D2

When the Forward Memory Test is enabled (i. e., when bit D2 at the Memory Test Select Flag is set to the logic '1' state), one known bit pattern is written into each address in the region under test. The first memory location is then read back and compared to the first known pattern. If the data matches, a new pattern (the bitwise complement of the first) is written to the first address, and that address is read back again. If the new data again matches, the address counter is incremented, and the next higher address is read and compared to the first pattern. If this data matches, the second pattern is written and compared, and so on. If the data returned by the first readback of a given address does not match the first pattern, Error code 0xE3 is written to the Self–Test Results location. If the second readback of a given address does not match the second pattern, Error Code 0xE4 is written to the Self–Test Results location (see Table 8–7, on the page after next, for this processor–dependent address).

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8.5 Memory Diagnostics (continued)

8.5.4 Reverse Test – Bit D3

When the Reverse Test is enabled (i. e., when bit D3 at the Memory Test Select Flag is set to the logic '1' state), one known bit pattern is written into each address in the region under test. The last memory location is then read back and compared to the first known pattern. If the data matches, a new pattern (the bitwise complement of the first) is written to the last address, and that address is read back again. If the new data again matches, the address counter is decremented, and the next lower address is read and compared to the first pattern. If this data matches, the second pattern is written and compared, and so on. If the data returned by the first readback of a given address does not match the first pattern, Error code 0xE5 is written to the Self–Test Results location. If the second readback of a given address does not match the second pattern, Error Code 0xE6 is written to the Self–Test Results location (see Table 8–7, on the next page, for this processor–dependent address).

8.5.5 Pattern Test – Bit D4

When the Pattern Test is enabled (i. e., when bit D4 at the Memory Test Select Flag is set to the logic '1' state), a known bit pattern is written into each memory address. Each address is then read back, and the returned data is compared to the known pattern. If the patterns do not match, the Error Code 0xE7 is written to the Self–Test Results location (see Table 8–7, on the next page, for this processor–dependent address).

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8.5 Memory Diagnostics (continued)

8.5.6 Memory Test Address Ranges

Table 8–7, below, lists the memory addresses that are tested during the firm–ware's memory tests.

Table 8–7: Model 4290/4291 –Memory Test Address Ranges

Memory Region	Start Address	End Address
Dual Port SRAM (Local Side)	0x0020 0000	0x0023 FFFC
Global Dual Port SRAM (Processor A)	0x00A0 0000	0x00A3 FFFC
Global Dual Port SRAM (Processor B)	0x00A8 0000	0x00AB FFFC
Global Dual Port SRAM (Processor C)	0x00B0 0000	0x00B3 FFFC
Global Dual Port SRAM (Processor D)	0x00B8 0000	0x00BB FFFC
Global SRAM (Processor A)	0x0080 0400	0x0088 2FFC
Global SRAM (Processor B)	0x0088 3000	0x0090 1FFC
Global SRAM (Processor C)	0x0090 2000	0x0098 0FFC
Global SRAM (Processor D)	0x0098 1000	0x009F FFFC
NVSRAM (Processor A)	0x00C0 0000	0x00C0 1FFC
NVSRAM (Processor B)	0x00C0 2000	0x00C0 3FFC
NVSRAM (Processor C)	0x00C0 4000	0x00C0 5FFC
NVSRAM (Processor D)	0x00C0 6000	0x00C0 7FFC
SDRAM*	0x0200 8000	0x02FF FFFC
SBSRAM†	0x0300 0000	0x0307 FFFC
Internal Data Memory	0x8000 0000	0x8000 FFFC

*** –First 32k of SDRAM is not tested because Boot Code is executed from that region, after the code is dumped there from the Flash EEPROM.**

† –For Option 330, SBSRAM range is from 0x0100 0000 to 0x0107 FFFC

The selected memory tests, described in the previous sections, are executed in the regions and by the processors indicated above, one time each if the Boot_Flag contains the code 0xFEED FAC1. If the Boot_Flag contains the code 0xFEED FAC2, then the selected tests are executed in an endless loop. This feature was included for factory burn–in and diagnostic operations, but may also be useful as a diagnostic for the end user. Note that the only ways to ter–minate the continuous testing loop are to reset the Model 4290/91, or to cycle power. To gain any information from the continuous tests, the test loop must be exited by pushing the front panel reset button, which initiates a reboot without a self–test, and preserves the contents of the results locations (see Tables 8–7 & 8–8).

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8.5 Memory Diagnostics (continued)

8.5.7 Memory Test Failures

If one of the memory tests fail, further testing is halted. The red LED illuminates, and a combination of the green LEDs blink to indicate which test failed. In this context, the 3 green LEDs for a given processor represent a 3–bit grouping, with the lowest (#3, the one farthest from the red one) as the least significant bit. They display the binary code for the test in progress. If the test process halts, the displayed green LED indicates at which test the failure has occurred. For example, the red LED and green LED #2 remains lit, to indicate that test #2 failed. If a test does fail, a total of five addresses are written to, which indicate test completion (or the number of test cycles completed in continuous mode) the failed test number, the address at which the failure occurred, the written data and the data read back. Table 8–8, below, lists these processor–dependent addresses in the Global SRAM, and their content. Table 8–9, at the bottom of this page, lists the Error Codes.

Table 8-8: Model 4290/4291 –Memory Test Result Addresses

Address for Processor . . .				Description of Contents
A	B	C	D	
0x0000 0C44	0x0000 1C44	0x0000 2C44	0x0000 3C44	'0' if test completed, or # of test cycles completed in continuous mode
0x0000 0C48	0x0000 1C48	0x0000 2C48	0x0000 3C48	'0' if all tests passed, or Error Code for last test failure
0x0000 0C4C	0x0000 1C4C	0x0000 2C4C	0x0000 3C4C	'0' if all tests passed, or address of last test failure
0x0000 0C50	0x0000 1C50	0x0000 2C50	0x0000 3C50	'0' if all tests passed, or data read during last test failure
0x0000 0C54	0x0000 1C54	0x0000 2C54	0x0000 3C54	'0' if all tests passed, or data written during last test failure
NOTE: For Global SRAM access from the 'C6x, the Page Register, at 'C6x Address 0x0028 0024, must be set to 0x40				

Table 8-9: Model 4290/4291 –Memory Test Error Codes

Code	Description
0xE1	Clear & Verify Test Failure - Non-zero data returned
0xE2	Address in Address Test Failure - Data different from address returned
0xE3	Forward Memory Test Failure - First pattern incorrect
0xE4	Forward Memory Test Failure - Second pattern incorrect
0xE5	Reverse Memory Test Failure - First pattern incorrect
0xE6	Reverse Memory Test Failure - Second pattern incorrect
0xE7	Pattern Test Failure - Pattern does not match

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8.5 Memory Diagnostics (continued)

8.5.7 Memory Test Failures (continued)

The subsections that follow tell which green LEDs are lit to indicate what is being tested when they are lit.

8.5.7.1 Green LED #3 On

A processor turns on its green LED #3 during the testing of the Dual Port SRAM on the local 'C6x side and when testing the Dual Port Global SRAM of the other processors. If the test fails, the red LED and green LED #3 remain lit.

8.5.7.2 Green LED #2 On

A processor turns on its green LED #2 during the testing of the Global SRAM and Global Non−Volatile SRAM (NVSRAM). If the test fails, the red LED and green LED #2 remain lit.

8.5.7.3 Green LED #1 On

A processor turns on its green LED #1 while running the SDRAM Test. If this part of the test fails, the red LED and green LED #1 remain lit.

8.5.7.4 Green LEDs #1 and #3 On

A processor turns on its green LEDs #3 and #1 while running the SBS RAM Test. If this part of the test fails, the red LED and green LEDs #3 & #1 remain lit.

8.5.7.5 Green LEDs #1 and #2 On

A processor turns on its green LEDs #1 and #2 while running the 'C6x Internal Data Memory Test. If this part of the test fails, the red LED and green LEDs #1 & #2 remain lit.

8.5.7.6 Red LED On

A processor turns on its red LED to indicate a test failure.

8.5.7.7 Blinking Green LED #1

At the conclusion of the diagnostics, if all tests pass, the green LED #1 will blink.

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8.6 Self–Test Completion

At the completion of the Self–Test, locations `0x0C40`, `0x1C40`, `0x2C40`, and `0x3C40` are cleared to logic '0'.



In Firmware Versions 2.0 and earlier, locations `0x0C40`, `0x1C40`, `0x2C40`, and `0x3C40` are not cleared to logic '0' at the completion of each test. However, after running each subtest, these locations are breifly cleared to logic '0' (approximately 1 ms). To determine if the test has completed, wathch for logic '0' to appear for at least 1 ms.

8.7 Continuing with the Boot Routine

After the diagnostics routines have completed (assuming that they have been run), each processor loads a vector table from its own table in the Global SRAM (see Table 8–10, below, for the locations of these tables). These vectors consist of a set of pointers to the look, set and block move functions provided as part of the factory supplied firmware (see Section 8.13 for detailed descriptions of these functions and their use, and Table 8–16 for a list of the addresses used by these tables, and their contents), an address used as an interrupt counter, the initial values of of the test patterns used in the memory diagnostics, an address that holds the revision of the boot code, and a copy of the Global Bus Page Register.

Table 8-10: Model 4290/4291 - Vector Table Locations in Global SRAM

Processor	Address
A	0x0000 0800
B	0x0000 1800
C	0x0000 2800
D	0x0000 3800

NOTE: For Global SRAM access from the 'C6x, the Page Register, at 'C6x Address 0x0028 0024, must be set to 0x40

What happens after that operation has completed depends upon how your Model 4290/4291 is equipped. If your Model 4290/4291 is an Option 330 unit, then at this point the processor will toggle its Timer1 output line 100 times, while monitoring its Timer1 input. If the processor sees the same signal at that input (i. e., if the Timer1 out–put has been externally shorted to the Timer1 output, see Section 2.3.5), the User Flash EEPROM will be cleared. Units that do not contain Option 330 skip this step, and move from the diagnostic routines to the steps described in Section 8.8, which begins on the next page.

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8.8 User Boot Code – Boot Loading or Bypassing

Next, the processor once again checks the contents of the Boot_Flag location in Global SRAM (see Table 8–4, on page 204 of this manual) to determine whether to run or bypass any Custom Boot Code that may reside in the Boot Flash EEPROM or in the Global SRAM. The ability to bypass any existing User Boot code is essential, as this gives the user the ability to replace such code, if and when necessary.

If the data in the Boot_Flag is 0xC33C 3CC3, any existing user code is bypassed. In this case, the processor prepares itself to go into the idle state, as described in Section 8.9. If not, another comparison is performed on the Boot_Flag's value, to determine where to find the user code that will be booted.

If the Boot_Flag contains the data 0xFEED C0DE, then the user boot code resides in Global SRAM. The processor reads the next two addresses to get two important pieces of information. The first of these (Boot_Flag+0x04) holds the address at which the desired boot code begins (the Source_Address), and next (Boot_Flag+0x08) holds the address at which to begin executing the code (the Start_Address). After storing these addresses, the processor reads the Source_Address, whose value should be initialized by the programmer to 0xC0DE F00D. If any other value is found at this address, the processor lights it red LED, writes the fail code 0x0BAD 00BC to its Boot_Status location (see Table 8–2, on page 202), and prepares itself to go into the idle state, as described in Section 8.9.

If the data in the Source_Address is 0xC0DE F00D, then the processor again reads the next two addresses. The first of these (Source_Address+0x04) should contain the address to which the code should be loaded (called the destination, or Dest_Address) and the next address (Source_Address+0x08) should hold the number of consecutive addresses in this block of the boot code. The actual code to be boot loaded begins at Source_Address+0x0C. Note that user boot code can be stored across multiple blocks of the memory region in which it resides. We allow for this by performing one more check on the last longword in each block.

If the data stored in the last longword in a given block (this address can be calculated as Block_End = Source_Address + 0x0C + Block_Length), is 0x0C0D EFED, then all the code has been loaded to the appropriate memory region, and the processor can begin executing the user boot code at the Start_Address. If any other data value is detected at the end of the block, then there is more code to be loaded. The processor must then read a new Source_Address from the address following the Block_End, and repeat the procedure described in the paragraph above until it finds a block that does end with the data value 0x0C0D EFED.

If the Boot_Flag address does not contain the value 0xFEED C0DE, then the processor will not look for boot code in the Global SRAM. Instead, it will read another processor dependent flag at an address in the Flash EEPROM, the Flash_Flag, to determine if there is user code to be boot loaded in the Flash EEPROM. These addresses are given in Table 8–11, at the top of the next page

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8.8 Running or Bypassing User Boot Code (continued)

Table 8–11: Model 4290/4291 –Flash_Flag Locations in Flash EEPROM	
Processor	**Address**
A	0x0002 0000
B	0x0002 0010
C	0x0002 0020
D	0x0002 0030

The procedure followed by the processor now is identical to that described on the previ–ous page. If the Flash_Flag contains the data 0xFEED C0DE, then it will boot load the code to the Source_Address (stored at Flash_Flag+0x04), and the Start_Address is read from Flash_Flag+0x08. If the Source_Address contains the word 0xC0DE F00D, then the next two addresses are read to determine the Dest_Address (at Source_Address+0x04) and the Block_Length (at Source_Address+0x08). The code beginning at Source_Address+0x0C is boot loaded as described above, and you know you've moved all of of the boot code, and can begin execution at the Start_Address, when you read the value 0x0C0D EFED at the end of a block. If the Flash_Flag does not contain the data 0xFEED C0DE, the processor prepares to go idle and await additional instructions.

In either of the cases described above (i. e., if the processor entered the Global or Flash Boot routines), if the Source_Address contains any data other than 0xC0DE F00D, then an error condition has been encountered. The red LED will be lit, an error code gets written to the Boot_Status Location (see Table 8–2, on page 202), and the processor prepares to go idle.

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8.9 Completing the Factory Boot in the Idle State

If there is no user boot code to be loaded, or if the processor was directed not to boot such code (by the presence of the bypass code, 0xC33C 3CC3, in the Boot_Flag address), then the standard factory boot will be completed with steps listed below.

First, the processor's internal cache memory is enabled. In the standard units (i. e., those that are NOT equipped with Option 330), interrupts are enabled, the global bus is unlocked, and the processor enters the idle state, awaiting an interrupt to instruct it where to go to find code to execute.

If the 4290/4291 does contain option 330, then additional steps are performed. After enabling the cache, the processor reads yet another flag at a processor dependent address (see Table 8–12, below) in the Global SRAM, which we'll call Cache_Ckr, to determine whether or not you REALLY wanted the cache enabled. If this address contains the value 0xCAC4 E0FF, then the DSP's cache will be disabled. If it contains 0xCAC4 E055, then the cache remains enabled. Option 330 units will then complete the factory boot as above, by enabling interrupts, unlocking the global bus, and going idle until interrupted.

Table 8–12: Model 4290/4291 –Cache_Ckr Locations in Global SRAM

Processor	Address
A	0x0000 0040
B	0x0000 0044
C	0x0000 0048
D	0x0000 004C

NOTE: For Global SRAM access from the 'C6x, the Page Register, at 'C6x Address 0x0028 0024, must be set to 0x40

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8.10 Factory Boot Code Flag Use Summary

Table 8–13, below, summarizes the various flag addresses read and written during the standard factory boot of a Model 4290/4291, the data codes that might be found in those locations, and the actions taken based on the flag values.

Table 8–13: Model 4290/4291 –Flag Addresses Accessed During Boot Routine

Flag Name	Address	Contents	Comment
Boot_Status	0x0000 z900	0x00EE C0DE	VIM Module installed
		0xFFFF FFFE	No VIM Module installed
		0x000B ADC5	VIM EEPROM Checksum Error
VIM_Code	0x0000 z904 - 0x0000 z97C	Module Code	Copied from VIM Module's EEPROM
Vec_Table	0x0000 z800 - 0x0000 z87C	Vector Table	Pointers to Look, Set & Block Move functions
Boot_Flag	0x0000 00z0	0xFEED FAC0	Clear & Verify Memories
		0xFEED FAC1	Run Selected Memory Tests - 1 Pass
		0xFEED FAC2	Run Selected Memory Tests - Continuous
		0xC33C C33C	Bypass User Boot Code
		0xFEED C0DE	Boot Load from Global SRAM
Boot_Flag+0x04	0x0000 00z4	Source_Address	Address of Start of Boot Code in Global SRAM
Boot_Flag+0x08	0x0000 00z8	Start_Address	Address at which User Boot Code Execution Begins
Flash_Flag	0x0002 00z0	0xFEED C0DE	Boot Load from Flash EEPROM
Flash_Flag+0x04	0x0002 00z4	Source_Address	Address of Start of Boot Code in Flash EEPROM
Flash_Flag+0x08	0x0002 00z8	Start_Address	Address at which User Boot Code Execution Begins
Source_Address	Read from 0x0000 00z4 or 0x0002 00z4	0xC0DE F00D	Valid Boot Code (from Global SRAM or Flash EEPROM) follows
Source_Address+0x04	See Above, + 4	Dest_Address	Address to begin Boot Loading the code at
Source_Address+0x08	See Above, + 8	Block_Length	# of longwords of code that follow in this block
Source_Address+0x0C	See Above, +12	Start of Code	Actual Boot Code begins here
Block_End	Source_Address+0x0C +Block_Length	0x0C0D EFED	End of Boot Code
		Other than above	More Boot Code exists - Read new Source_Address from next address
Cache_Ckr (Option 330 Only)	0x0000 004z	0xCAC4 E055	Enable Cache (Option 330 Only)
		0xCAC4 E0FF	Disable Cache (Option 330 Only)

NOTES:

1) **For all addresses above: z = 0 for Processor A, z = 1 for Processor B, z = 2 for Processor C, and z = 3 for Processor D**
2) **For Global SRAM access from the 'C6x, the Page Register, at 'C6x Address 0x0028 0024, must be set to 0x40, and for Flash EEPROM access, the Page Register must be set to 0x0**

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8.11 Checking the Firmware Revision

Addresses are provided in each processor's vector table in the Global SRAM that hold the revision level of the firmware installed on your Model 4290/4291. The specific address in each processor's vector table is shown in Table 8–14, below. For example, in a Model 4290/4291 with revision 2.00 firmware, reading address 0x0000 083C from Processor A would return the data value 0x0000 0200.

Table 8–14: Model 4290/4291 –FW Revision Locations in Global SRAM

Processor	Address
A	0x0000 083C
B	0x0000 183C
C	0x0000 283C
D	0x0000 383C

NOTE: For Global SRAM access from the 'C6x, the Page Register, at 'C6x Address 0x0028 0024, must be set to 0x40

8.12 Loading User Boot Code

The Model 4290/4291 has 2 M x 32–bits of Flash EEPROM memory on its Global bus. This non–volatile resource serves three separate storage functions – it stores the code used to boot the processors, the code for the built–in firmware functions (see Section 8.13), and can hold code for user applications, which may be run automatically after the processors have been booted. The Flash EEPROM on the 4290/4291 is organized as 64 sectors of 128 k–longwords each. The factory boot code and firmware function code (both supplied by Pentek) and the Boot Flag locations are all located in the first two sectors (Sector 0 and Sector 1), one of which (Sector 0) is write protected by a factory default jumper setting (see Section 2.2.4). Sectors 2 thru 15 are available for storing user applications (the maximum length is 2 MBytes), which must be downloaded to the 4290/4291 by the user.

Note that the process of loading a program from Flash EEPROM on the 4290/4291 will disable the 'C6x's cache. If the loaded program does not use the 'C6x's Internal Pro–gram Memory (which also serves as the cache), the program should include commands to re–enable the cache for optimum performance. The user should also be aware that the boot code uses the lowest portion of SDRAM. If the program you load is to be run from SDRAM, it is important that it does not overwrite the addresses used by the boot routine. To allow for this, modify the **`4290.cmd`** file so that the SDRAM address range starts at 0x0201 0000, with a length of 0x00FF 0000 (instead of addr = 0x0200 0000, len = 0x0100 0000).

Sectors 16 thru 63 can be used to store static data that may be needed by the down–loaded applications, but it is again the user's responsibility to load, verify, and unload such data when necessary. Note also that before you can write to any Flash EEPROM sector, you must first erase the current contents of that sector. Table 8–15, on the next page, illustrates the organization of the Flash EEPROM on the Model 4290/4291.

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8.12 Loading User Boot Code (continued)

The ReadyFlow Board Support Library package for the Model 4290/4291 provides several utility programs for loading user programs into the Flash EEPROM. The programs included there give the user three different methods for downloading such programs. One option is via the use of a JTAG Emulator, another uses Pentek's SwiftNet Communication Protocols, and the third uses a VMEbus Host running VxWorks. For complete details about how to use these utilities, please refer to the ReadyFlow Software Support Documentation (Revision 2.2 or later). For ReadyFlow revisions earlier than 2.2, the instructions are available in Readme files on the distribution disc. Note that you can always download the most recent revision of any Pentek manual from our web site, www.pentek.com.

Table 8-15: Model 4290/4291 –Flash EEPROM Organization

Sector #	Address Range	Used For	Comments
Sector 0	0x0000 0000 – 0x0001 FFFF	Factory Boot Code & FW Functions	
Sector 1	0x0002 0000	Processor A Boot Flag	
	0x0002 0004	Pointer to starting address of code for Processor A	Must point to the first address in a sector
	0x0002 0008	Pointer to entry point for Processort A pode	
	0x0002 000C	Reserved	
	0x0002 0010	Processor B Boot Flag	
	0x0002 0014	Pointer to starting address of code for Processor B	Must point to the first address in a sector
	0x0002 0018	Pointer to entry point for Processort B pode	
	0x0002 001C	Reserved	
	0x0002 0020	Processor C Boot Flag	
	0x0002 0024	Pointer to starting address of code for Processor C	Must point to the first address in a sector
	0x0002 0028	Pointer to entry point for Processort C pode	
	0x0002 002C	Reserved	
	0x0002 0030	Processor D Boot Flag	
	0x0002 0034	Pointer to starting address of code for Processor D	Must point to the first address in a sector
	0x0002 0038	Pointer to entry point for Processort D pode	
	0x0002 003C – 0x0003 FFFF	Reserved	
Sector 2	0x0004 0000 – 0x0005 FFFF	User Defined	User Program Space
Sector 3	0x0006 0000 – 0x0007 FFFF		
:	:		
Sector 15	0x001E 0000 – 0x001F FFFF		
Sector 16	0x0020 0000 – 0x0021 FFFF	User Defined	User Data Space
:	:		
Sector 63	0x007E 0000– 0x007F FFFF		

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8.12 Loading User Boot Code (continued)

As described in Section 8.8 of this manual, User Boot code may be downloaded to either the Flash EEPROM or to the Global SRAM. The ReadyFlow Board Support Libraries support downloads to either memory region. As Table 8–15 indicates, when downloading User code into the Flash EEPROM, it must be loaded to an address between 0x0004 0000 and 0x001F FFFF, i. e., into the User Program area. You should also be aware that when downloading User Code into the Global SRAM, it must be loaded at address 0x0080 4000 or higher, to prevent any of the user code from being overwritten by the results of the Model 4290/4291's self–tests.

8.13 Model 4290/4291 Firmware Functions

In addition to the diagnostic and Flash EEPROM write functions discussed in prior sections of his chapter, three more functions are included in the firmware provided by Pentek in the Boot/User Flash EEPROM (LOOK, SET, BLOCK MOVE), to display, load, move or examine code on the Model 4290/4291. Figures 8–3 and 8–4, on the next two pages, contain flow charts showing the steps for implementing each of the firmware functions. In the flowcharts, and the discussions of them that follow, the letter "z" is used to represent a 4–bit, processor –specific address component, defined as follows: For Processor A, z=0; for Processor B, z=1; for Processor C, z=2; for Processor D, z=3.

Table 8–16: Model 4290/4291 –Vector Table for Firmware Functions

Address	Function
0x0000 z800	Function Address from Host
0x0000 z804	LOOK / SET functions: Address BLOCK MOVE function: Source Address Flash EEPROM function: Boot Address
0x0000 z808	SET function: Data from Host BLOCK MOVE function: Destination Address Flash EEPROM function: Data Width
0x0000 z80C	LOOK function: Data to Host BLOCK MOVE function: Block Length (Word Count –1)
0x0000 z810	Ready Flag to Host (0 = Not Ready, 1 = Ready)
0x0000 z814	Pointer to LOOK function
0x0000 z818	Pointer to SET function
0x0000 z81C	Pointer to BLOCK MOVE function
0x0000 z820	Interrupt Counter
0x0000 z824	Diagnostic Test Pattern –0xA5A5 A5A5
0x0000 z828	Diagnostic Test Pattern –0x5A5A 5A5A
0x0000 z82C	Diagnostic Test Pattern –0x1234 5678
0x0000 z830	Diagnostic Test Pattern –0x8765 4321
0x0000 z834	Diagnostic Test Pattern –0xFFFF FFFF
0x0000 z838	Diagnostic Test Pattern –0x0000 0000
0x0000 z83C	Boot Code Revision Level
0x0000 z840	Diagnostic Test Pattern –0x0000 z800
0x0000 z87C	Page Register Value for FW Function access
z = 0 for Processor A, z = 2 for Processor B, z = 2 for Processor C, z = 3 for Processor D	

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8.12 Model 4290/4291 Firmware Functions (continued)

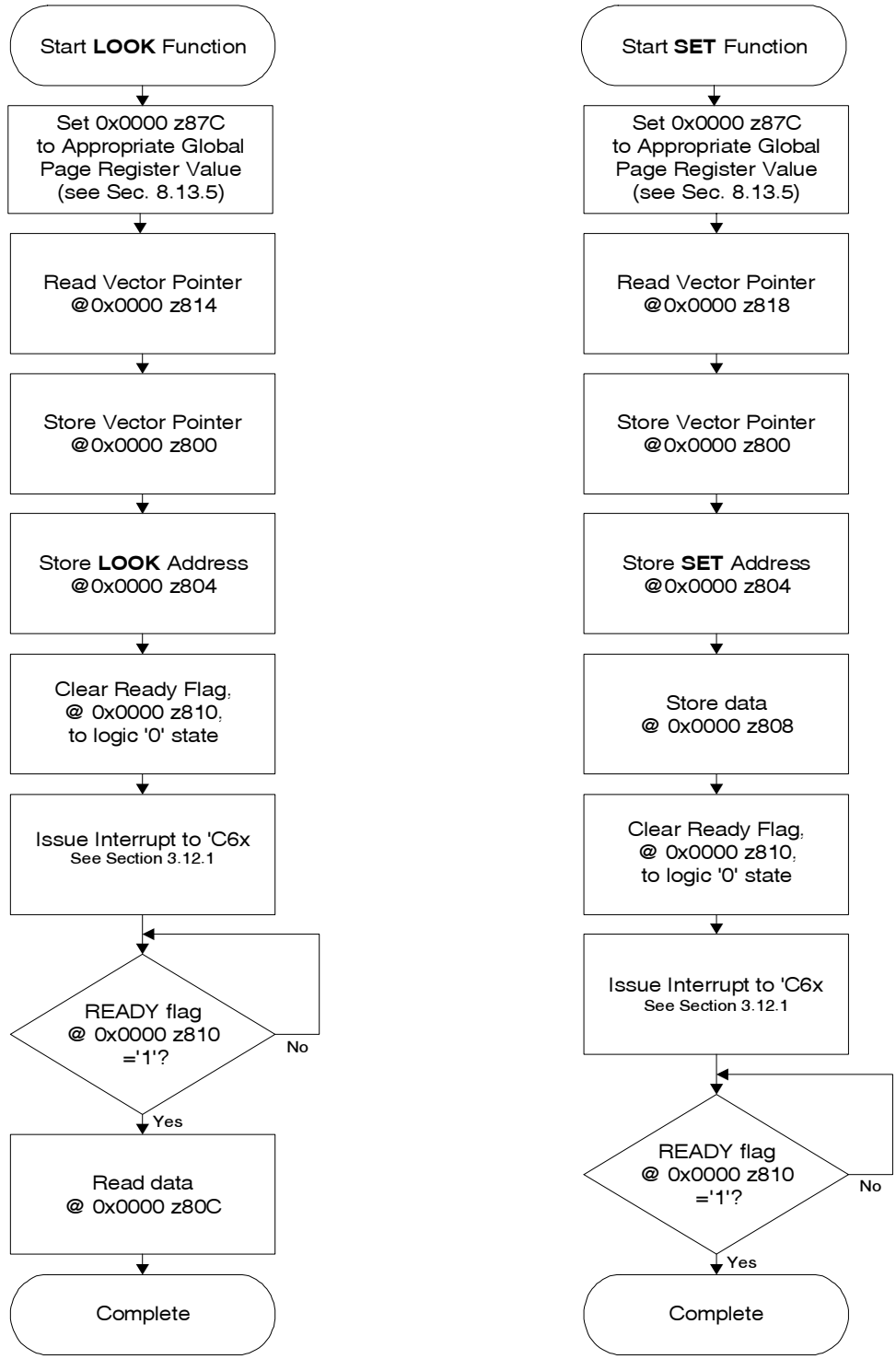


Figure 8–3: Model 4290/4291 – User Flowchart for Firmware LOOK and SET Functions

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8.12 Model 4290/4291 Firmware Functions (continued)

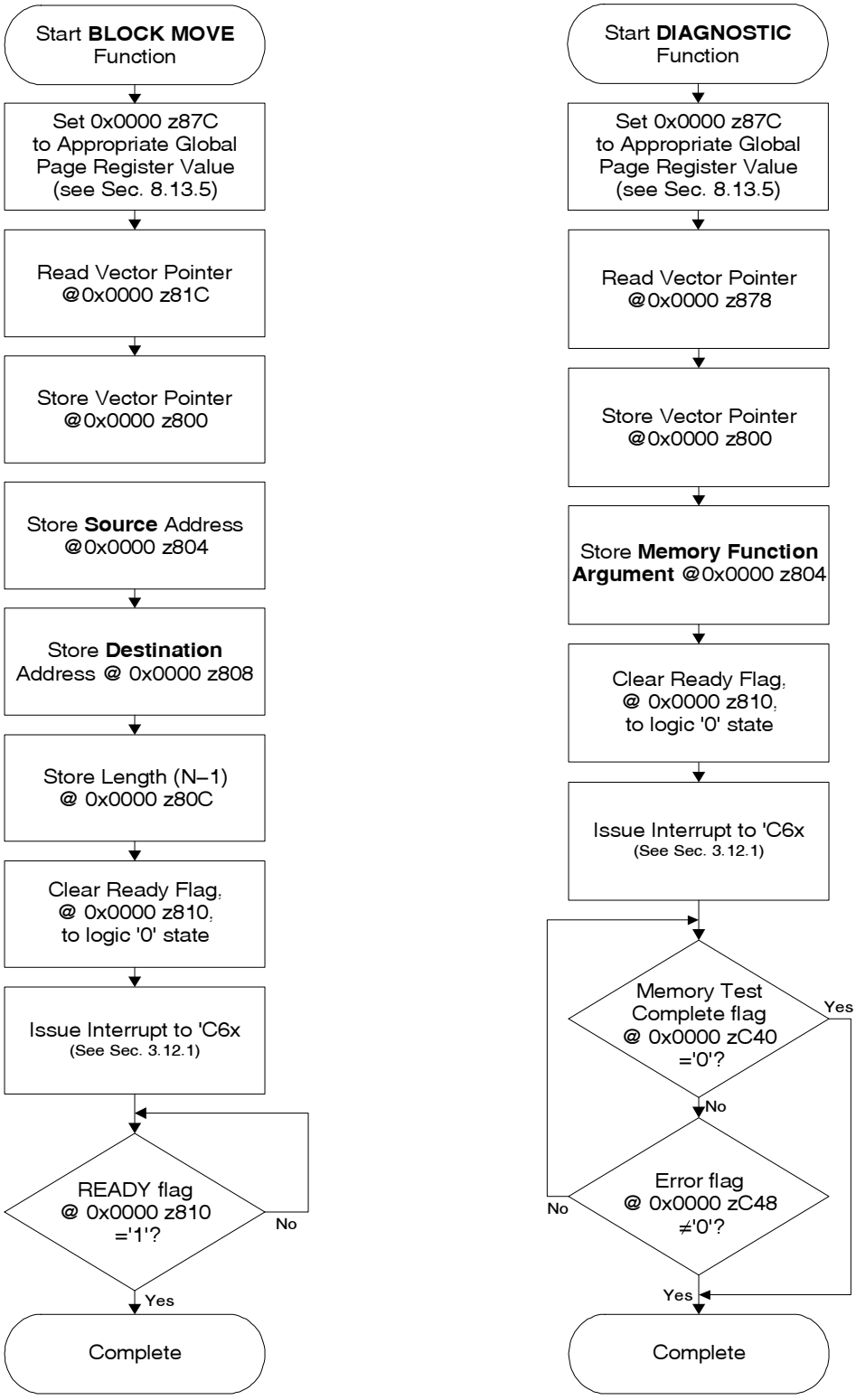


Figure 8-4: Model 4290/4291 - User Flowchart for Firmware BLOCK MOVE & DIAGNOSTICS Functions

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8.13 Model 4290/4291 Firmware Functions (continued)

8.13.1 Issuing 'C6x Interrupts

Each of these firmware functions is launched by issuing an interrupt thru the DPSRAM Mailbox to the 'C6x processor that is to execute the function from its own vector table. The routine that services these interrupts instructs the interrupted processor to read the lowest address in its vector table (0x0000 z800) and use that value it finds there as the starting address of the function to be executed. A separate address is provided for issuing this interrupt to each 'C6x processor on the Model 4290/4291, as shown in Table 8–17, below. Note that these are Write–Only addresses, and the arbitrary data used for the write operation is neither used nor stored.

Table 8–17: Model 4290/4291 –Interrupt Addresses in Global SRAM

Processor	Address
A	0x00A4 0000
B	0x00BC 0000
C	0x00AC 0000
D	0x00B4 0000

NOTE: For Global SRAM access from the 'C6x, the Page Register, at 'C6x Address 0x0028 0024, must be set to 0x40

8.13.2 The LOOK Function

The LOOK function takes a valid memory address in the Model 4290/4291 as an argument, and returns the contents of that address to the host system. A pointer to the start of the LOOK function is stored in the vector table at address 0x0000 z814. Before launching the LOOK function, the contents of address 0x0000 z814 must be copied into the first address in the vector table (0x0000 z800), the address whose contents are to be examined must be written to the next vector table address (0x0000 z804), and the value 0x0000 0000 must be written to the table's Ready flag, at address 0x0000 z810.

The LOOK function may then be launched, by writing to the processor's interrupt address (see Table 8–17), which causes the processor to use the contents of address 0x0000 z800 as a pointer, and execute the code it finds at that address (which was previously initialized as the LOOK function's address). The function will read the address pointed to by table address 0x0000 z804, copy the data it finds at that address to address 0x0000 z80C, and then write the value 0x0000 0001 to the Ready flag (at 0x0000 z810), which the host system should poll to determine when the function has been completed.

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8.13 Model 4290/4291 Firmware Functions (continued)

8.13.3 The SET Function

The SET function allows a host to write a data value (provided as one argument) to a valid memory address in the Model 4290/4291 (the second argument the function requires). A pointer to the start of the SET function is stored in the vector table at address 0x0000 z818. Before launching the SET function, the contents of address 0x0000 z818 must be copied into the first address in the vector table (0x0000 z800). The next two addresses in the vector table must be initialized with the address you want the data to be written to (in address 0x0000 z804) and the data value to be written (in address 0x0000 z808). Also, the value 0x0000 0000 must be written to the table's Ready flag, at address 0x0000 z810.

The SET function may then be launched, by writing to the processor's interrupt address (see Table 8–17), which causes the processor to use the contents of address 0x0000 z800 as a pointer, and execute the code it finds at that address (which was previously initialized as the SET function's address). The function will copy the data value in table address 0x0000 z808 to the address pointed to by table address 0x0000 z804, and then write the value 0x0000 0001 to the Ready flag (at 0x0000 z810), which the host system should poll to determine when the function has been completed.

8.13.4 The BLOCK MOVE Function

The BLOCK MOVE function copies the contents of one group of consecutive addresses in the memory of the 4290/4291 to another group of consecutive addresses. This function requires three arguements: the lowest address of the region where the data is currently stored (the source address); the lowest address of the region you want the data copied to (the destination address), and the number of consecutive addresses to be copied (the block length, which is actually equal to one less than the number of longwords to be copied).

Block_Length = # longwords in block –1

A pointer to the start of the BLOCK MOVE function is stored in the vector table at address 0x0000 z81C. Before launching the BLOCK MOVE function, the contents of address 0x0000 z81C must be copied into the first address in the vector table (0x0000 z800). The next three addresses in the vector table must be initialized with the source address (in address 0x0000 z804), the destination address (in address 0x0000 z808) and the Block_Length, from the equation above (in address 0x0000 x80C). Also, the value 0x0000 0000 must be written to the table's Ready flag, at address 0x0000 z810.

The BLOCK MOVE function may then be launched, by writing to processor's interrupt address (see Table 8–17), which causes the processor to use the contents of address 0x0000 z800 as a pointer, and execute the code it finds at that address (which was previously initialized as the BLOCK MOVE function's address). The function will copy the specified number of data values (i. e., Block_Length+1) from the source region to the destination region, and then write the value 0x0000 0001 to the Ready flag (at 0x0000 z810), which the host system should poll to determine when the function has been completed.

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8.13 Model 4290/4291 Firmware Functions (continued)

8.13.5 The Vector Table's Page Register Setting

The highest address in the Global SRAM's Vector Table (0x0000 z87C)is used to store the 4290/4291's Page Register setting, which allows access to Global bus memory regions that may contain the addresses used in the LOOK, SET or BLOCK MOVE operations. This entry in the Vector Table is initialized with the value 0x0000 0040, which points to the Global SRAM. To illustrate the use of this entry, let us consider an example where we wish to LOOK at an address in the NVSRAM.

The Page Register is located at 'C6x address 0x0028 0024, and the register setting for access to the Global bus' NVSRAM is 0x0000 0060. At some point prior to issuing the interrupt that hands the process off to the firmware, the user must write this value to address 0x0000 z87C. The firmware will store the current value of the Page Register at another location, and copy the data from address 0x0000 z87C into the Page Register before attempting to access the LOOK address. This assures that the proper memory region is accessed. After returning the data from the LOOK address to address 0x0000 z80C, the firmware restores the original Page Register value. Table 8–18, below, gives the Page Register value required to access each resource available to the 4290/4291's 'C6x processors via the Global bus.

Table 8–18: Model 4290/4291 – Global Bus Page Register Settings

Resource	Settings
Flash EEPROM	0x0000 0000
Global SRAM	0x0000 0040
Dual Port SRAM & Mailboxes	0x0000 0050
NVSRAM	0x0000 0060
Global, VIC & CY7C964 Registers	0x0000 0070
Global Expansion Bus	0x0000 0080 –0x0000 00F0
VMEbus A16 Master Access	0x0000 0100 –0x0000 0170
VMEbus A24 Master Access	0x0000 0180 –0x0000 01F0
VMEbus A32 Master Access	0x0000 8000 –0x0000 FFF0

The SET and BLOCK MOVE functions are handled similarly – the necessary Page Register value must be written to 0x0000 z87C prior to issuing the interrupt that starts the firmware routine. The firmware directs the processor to store the original Page Register value and substitute the one from the Vector Table before executing the function, and to restore the orignal Page Register value before the function terminates. For more information about the Page Register and Global bus access, please refer to Section 4.3.2.7.

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Chapter 9: Data Transfer Benchmarks

9.1 Transfer Timing for Model 4290/4291

Table 9–1, below shows the number of clock cycles it takes to move a single, 32–bit data element from one memory resource on the Modle 4290/4291 to another, with DMA enabled. All results listed are derived from the measured time for a transfer of 1000 longwords.

Table 9–1: Model 4290/4291 –Data Transfer Timing

From	To	Clock Cycles to Transfer 1 32-bit longword	
		Standard	Option 330
'C6x Internal Data Memory	Global Flash EEPROM	43	43
	Dual Port SRAM (Global Side)	40	40
	Global NVSRAM	45	45
	Global Registers	45	45
	Global SRAM	35	35
	Dual Port SRAM (Local Side)	16	16
	Local Registers	34	34
	Random Access VIM I/O	22	22
	IP & Mezzanine Bi-FIFOs	8	2
	Local SDRAM	2	2
	Local SBSRAM	1	1
Local Registers	'C6x Internal Data Memory	5	5
Global SRAM		34	34
Dual Port SRAM (Local Side)		43	43
Random Access VIM I/O		17	17
IP & Mezzanine Bi-FIFOs		22	22
Local SDRAM		9	2
Local SBSRAM		2	2
Global SRAM	Global SRAM	1	1
Dual Port SRAM (Local Side)	Dual Port SRAM (Local Side)	89	89
IP & Mezzanine Bi-FIFOs	IP & Mezzanine Bi-FIFOs	39	39
Local SDRAM	Local SDRAM	N/A	11
Local SBSRAM	Local SBSRAM	18	18
		5	5

9.2 time_DMA.c

The data that appear in the table above were acquired using the program **`time_DMA.c`**, listed on the four pages that follow. This short program may be used to test the transfer rate between any two blocks of memory on the Model 4290/4291 simply by initializing the DMA0 control registers with the source address (write this to 0x0184 0010), the destination address (write this to 0x0184 0018), and the number of longwords to transfer between these addresses (write this to 0x0184 0020), before running the program.

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9.2 time_DMA.c (continued)

```
extern cregister volatile unsigned int CSR, ICR;

#define DMA_MOVE_CONTROL 0x3000001
#define DMA_STOP_CONTROL 0x3000000

#define EDMA_INT0        0x2000000

#define CPU_PRIORITY     0x0u
#define DMA_PRIORITY     0x1000000

volatile unsigned int *timer0_address, *timer1_address;
volatile unsigned int *timer1_control, *timer1_period, *timer1_counter;
unsigned int *mcr0, *bcr, *results;
unsigned int *dma0_cont, *dma0_sec, *dma0_src, *dma0_dest, *dma0_cnt;
unsigned int cpu_num, cpu_mask, lc;

int time_dma_move(int src, int inc_src, int dest, int inc_dst, int
length);
void log_error(unsigned int testn,
               unsigned int error_code,
               unsigned int page,
               unsigned int failed_address,
               unsigned int is_data,
               unsigned int sb_data,
               unsigned int pass_cnt);
void toggle_bb_led(int val);
void bb_led_on(int val);
void bb_led_off(int val);

main()
{
   int i;
   int dma_cycles;
   CSR &= ~1;                          /* Disable global interrupts */
                                       /* Cache already enabled     */

   mcr0       = (unsigned int *)0x28001c;
   bcr        = (unsigned int *)0x280020;

   dma0_cont  = (unsigned int *)0x1840000;
   dma0_sec   = (unsigned int *)0x1840008;
/* write the source address to the pointer below */
   dma0_src   = (unsigned int *)0x1840010;
/* write the destination address to the pointer below */
   dma0_dest  = (unsigned int *)0x1840018;
/* write the number of longwords be transferred to the pointer below */
   dma0_cnt   = (unsigned int *)0x1840020;
```


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9.2 **time_DMA.c** (continued)

```
timer0_address =(unsigned int *)0x1940000;
timer1_address =(unsigned int *)0x1980000;
timer1_control =(unsigned int *)0x1980000;
timer1_period  =(unsigned int *)0x1980004;
timer1_counter =(unsigned int *)0x1980008;

/* See what proc this is */

cpu_mask = (*bcr) & 0xf;

for (i=0; i<4; i++)
{
   if (cpu_mask & (1 << i))
      break;
}

if (i==0)
   cpu_num = 0;
else if (i==1)
   cpu_num = 2;
else if (i==2)
   cpu_num = 3;
else if (i==3)
   cpu_num = 1;

results = (unsigned int *)(0x100 + (cpu_num * 0x10));

lc = 1;
results[0] = 0;
results[1] = 0;
results[2] = 0;
results[3] = 0;

bb_led_off(0xf);

bb_led_on(0x1);                    /* Red LED on */

/* Time IDMEM to SBSRAM on 4290/91 */

/* Results for Proc A stored in Global Sram 0x100 - 0x10c */
/* 0x100 = Source address                                 */
/* 0x104 = Destination address                            */
/* 0x108 = Length of move in 32 bit words                 */
/* 0x10c = Number of clock cycles per word                */
```


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9.2 time_DMA.c (continued)

```
   /* Results for Proc B stored in Global Sram 0x110 - 0x11c */
   /* 0x110 = Source address                                 */
   /* 0x114 = Destination address                            */
   /* 0x118 = Length of move in 32 bit words                 */
   /* 0x11c = Number of clock cycles per word                */

   /* Results for Proc C stored in Global Sram 0x120 - 0x12c */
   /* 0x120 = Source address                                 */
   /* 0x124 = Destination address                            */
   /* 0x128 = Length of move in 32 bit words                 */
   /* 0x12c = Number of clock cycles per word                */

   /* Results for Proc D stored in Global Sram 0x130 - 0x13c */
   /* 0x130 = Source address                                 */
   /* 0x134 = Destination address                            */
   /* 0x138 = Length of move in 32 bit words                 */
   /* 0x13c = Number of clock cycles per word                */

   /*********************************************************/
   /*            SBSRAM Timing Check on 4290/91             */
   /*********************************************************/

   dma_cycles = time_dma_move(0x80000000,0,0x3000000,0,65000);

   /*********************************************************/

   bb_led_off(0xf);
   bb_led_on(0xe);                    /* Turn on all Green LED's */

   while(1);
}

int time_dma_move(int src, int inc_src, int dest, int inc_dst, int length)
{
   int elapsed_time;

   *timer1_period = 0xffffffff;       /* Start value */
   /* dma_copy(src,inc_src,dest,inc_dst,length); */

   *dma0_cont = DMA_STOP_CONTROL | (inc_src<<4) | (inc_dst<<6);

   /* *dma0_sec &= ~(0x40); */
   *dma0_src  = src;
   *dma0_dest = dest;
   *dma0_cnt  = length;
```


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9.2 **time_DMA.c** (continued)

```
   *timer1_control = 0x3c0;            /* Start timer */
   *dma0_cont = DMA_MOVE_CONTROL | (inc_src<<4) | (inc_dst<<6);

   /* while (*dma0_cnt != 0); */
   while (((*dma0_cont) & 0xc) != 0);

   *timer1_control = 0x300;            /* Stop timer */
elapsed_time = *timer1_counter;

   *dma0_cont = DMA_STOP_CONTROL | (inc_src<<4) | (inc_dst<<6);

   results[0] = src;
   results[1] = dest;
   results[2] = length;
   results[3] = (elapsed_time*4)/length;

   return(elapsed_time);
}

cache_control(int cache_enable)
{
   if (cache_enable)
      CSR |= 0x140;                    /* Cache on */
   else
      CSR &= ~0x140;                   /* Cache off */
}

void toggle_bb_led(int val)
{
   *mcr0 ^= (val & 0xf);
}

void bb_led_on(int val)
{
   *mcr0 |= (val & 0xf);
}

void bb_led_off(int val)
{
   *mcr0 &= (~(val & 0xf));
}
```


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Appendix A: Cypress Semiconductor VIC64 Data

A.1 VIC64 Interprocessor Communication Facilities

TheVIC64 contains three categories of interprocessor communication facilities (ICFs):

- ❑ Interprocessor Communication Registers (ICRs)
- ❑ Interprocessor Communication Global Switches (ICGSs)
- ❑ Interprocessor Communication Module Switches (ICMSs)

The ICRs are 8–bit registers that may be accessed from either the Local bus or the VMEbus.

The ICGSs and ICMSs are switches that may be set to interrupt the local processor.

These facilities are located in seven registers that are visible from both the Local bus and the VMEbus. When accessed via the Local bus, the registers are read/written by normal VIC64 register access methods. When accessed by the VMEbus, the $\overline{\text{ICFSEL}}$ signal is used as a register select signal. The register addresses, when accessed from the Local bus are not the same as when accessed from the VMEbus. The VIC64 contains an internal arbiter to arbitrate between Local and VMEbus accesses to these facilities.

Additional registers used for the ICFs listed below. The contents of these registers are described in detail in the sections numbers following the abbreviated names in the list.

- ❑ ICGS Interrupt Control Register (ICGSICR – Section A.2.5)
- ❑ ICMS Interrupt Control Register (ICMSICR – Section A.2.6)
- ❑ ICGS Interrupt Vector Base Register (ICGSIVBR – Section A.2.8)
- ❑ ICMS Interrupt Vector Base Register (ICMSIVBR – Section A.2.9)
- ❑ Interprocessor Communication Switch Register (ICSR – Section A.2.12)

A.1.1 Valid ICF Selection

The ICFSEL signal is used to signal that the VMEbus master desires access to the VIC64 interprocessor communication facilities. This signal is usually driven from VMEbus address decoders. When ICFSEL is asserted, the VIC64 checks A[5:1] to determine what ICF is desired. Self–access to the ICF facili–ties is not detected by the VIC64. The VIC64 then verifies the AM codes against an internal table, shown in Table A–1, at the top of the next page.

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A.1 VIC64 Interprocessor Communication Facilities (continued)

1.1.1 Valid ICF Selection (continued)

Table A–1: VIC64 –Valid ICF Address Modifiers		
ICF	**AM Codes**	**Comments**
ICRs	0x29, 0x2D	A16, User or Supervisory Data
ICGSs	0x2D	A16, Supervisory Data
ICMs	0x29, 0x2D	A16, User or Supervisory Data

Once a valid ICF select has occurred, the VIC64 then processes the request. The ICF VMEbus addresses are shown in Table A–2, below.

Table A–2: VIC64 – ICF VMEbus Address Map	
Function	**Address**
ICR0 Access	A16_base+0x81
ICR1 Access	A16_base+0x83
ICR2 Access	A16_base+0x85
ICR3 Access	A16_base+0x87
ICR4 Access	A16_base+0x89
ICR5 Access	A16_base+0x8B
ICR6 Access	A16_base+0x8D
ICR7 Access	A16_base+0x8F
Clear ICGS0	A16_base+0x91
Set ICGS0	A16_base+0x93
Clear ICGS1	A16_base+0x95
Set ICGS1	A16_base+0x97
Clear ICGS2	A16_base+0x99
Set ICGS2	A16_base+0x9B
Clear ICGS3	A16_base+0x9D
Set ICGS3	A16_base+0x9F
Clear ICMS0	A16_base+0xA1
Set ICMS0	A16_base+0xA3
Clear ICMS1	A16_base+0xA5
Set ICMS1	A16_base+0xA7
Clear ICMS2	A16_base+0xA9
Set ICMS2	A16_base+0xAB
Clear ICMS3	A16_base+0xAD
Set ICMS3	A16_base+0xAF

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A.1 VIC64 Interprocessor Communication Facilities (continued)

A.1.2 Interprocessor Communication Registers (ICRs)

The VIC64 contains eight Interprocessor Communication Registers (ICRs). These registers are accessible from both the Local bus and the VMEbus. ICRs 4 – 0 are considered general purpose read/write registers. ICR5 is the VIC64 revision register. The value read from this register indicates the mask revision of the device. ICR6 contains the $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ status of the VIC64. ICR7 provides semaphores for ICRs 5 – 0. These semaphores are set whenever ICRs 5 – 0 are written. In addition, ICR7 also indicates VMEbus mastership and has a mask for $\overline{\text{SYSFAIL}}$. Refer to Section A.2.13 through Section A.2.17 for detailed register descriptions.

A.1.3 Interprocessor Communication Global Switches (ICGSs)

The ICGSs are software switches that may be set over the VMEbus to interrupt a group of VMEbus modules. When the VIC64 issues the global switches, it is performing a VMEbus byte–wide write to the pre–defined global switch address.

If the global switch interrupts are enabled, in the ICGSICR of the VIC64 slave, a local interrupt is generated on a clear–to–set transition of the selected switch. When acknowledged (FCIACK asserted), the slave VIC64 handles the interrupt by returning the status/ID value from the ICGSVBR. See Chapter 9 of Cypress Semiconductor's **VIC068A/VAC068A User's Guide** for details on VIC068A and VIC64 interrupt generation and handling. Once a switch is set, it must be cleared before it can be set again.

A.1.4 Interprocessor Communication Module Switches (ICMSs)

Like the ICGSs, the ICMSs are software switches that may be set over the VMEbus to interrupt the local processor. The module switches, however, are meant to be issued to a specific module. As in the Global switches, the VIC64 issuing the module switches performs a byte–wide write to the pre–defined switch address.

Because the module switches are meant for a specific module, the VIC64 as VMEbus slave (the module whose switch was just set) must assert the $\overline{\text{DTACK}}$. The VIC64 issuing the ICMS need not have its ICFSEL signal asserted.

The interrupt and addressing mechanisms are the same for the ICMSs as they were for the ICGSs. The ICSR may be used to provide monitoring of the module switches. Unlike the global switches, this register may be written by local resources to interrupt the CPU.

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A.2 VIC64 Register Map and Descriptions

This chapter describes the VIC64 internal configuration registers. These registers enable and disable various features of the VIC64. (Refer to the specific sections of the **VIC068A/VAC068A User's Guide** for details on specific features.)

Table A–3, on the next page, provides information on the various reset states of the VIC64 registers. The following notes should be observed regarding this table:

- An asterisk (*) indicates a bit that is not affected by the particular reset.
- An "X" indicates a bit that is affected by the state of a particular VIC64 pin.
- ICR5 is the VIC64 Version register. Its contents will vary depending on the revision of the device being used.

Unless otherwise specified, the reset status is given in this chapter by the values located in the parentheses below each bit field. The (X/X/X) format indicates the Global/Internal/System reset state of each bit or bit field.

When porting code written for the VIC068 to the VIC64 (if D64 transfers will **NOT** be used), it is recommended that all register bits described as "Reserved" in the VIC068 manual be written with a '0'. The following registers have been changed from their definitions in the VIC068 to allow the implementation of D64 transfers in the VIC64:

Register	Name	'C6X Address
Interprocessor Communications Register 5	ICR5	0x00F0 0074
Block Transfer Definition Register	BTDR	0x00F0 00A8
Release Control Register	RCR	0x00F0 00D0
Block Transfer Length Register 2	BTLR2	0x00F0 00E4

A.2.1 VMEbus Interrupter Interrupt Control Register

Name: VIICR

Address: 0x00F0 0000

Description: Provides enabling and IPL level encoding for the local interrupt issued when a VMEbus interrupt is acknowledged.

Bits 2 – 0: (0/*/*) IPL value: Value is inverted and driven onto the IPL lines when an interrupt is acknowledged.

Bits 6 – 3: (1/1/1) Undefined/Reserved. Bits will read as 1's.

Bit 7: (1/1/1) VMEbus interrupt mask: When clear, the VIC64 signals a local interrupt at the acknowledgement of a previously issued VMEbus interrupt. When set, the VIC64 will not issue a local interrupt.

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A.2 VIC64 Register Map and Descriptions (continued)

Table A-3: Model 4290 –VIC64 Register Map with Values After Firmware Loading

'C6x Address	Register	Description	Firmware Loaded Value
0x00F0 0000	VIICR	VMEbus Interrupter Interrupt Control Register	1111 1000
0x00F0 0004	VICR1	VMEbus Interrupt Control Register 1	1111 1000
0x00F0 0008	VICR2	VMEbus Interrupt Control Register 2	1111 1000
0x00F0 000C	VICR3	VMEbus Interrupt Control Register 3	1111 1000
0x00F0 0010	VICR4	VMEbus Interrupt Control Register 4	1111 1000
0x00F0 0014	VICR5	VMEbus Interrupt Control Register 5	1111 1000
0x00F0 0018	VICR6	VMEbus Interrupt Control Register 6	1111 1000
0x00F0 001C	VICR7	VMEbus Interrupt Control Register 7	1111 1000
0x00F0 0020	DMASICR	DMA Status Interrupt Control Register	1111 1000
0x00F0 0024	LICR1	Local Interrupt Control Register 1	1000 1000
0x00F0 0028	LICR2	Local Interrupt Control Register 2	1000 1000
0x00F0 002C	LICR3	Local Interrupt Control Register 3	1000 1000
0x00F0 0030	LICR4	Local Interrupt Control Register 4	1000 1000
0x00F0 0034	LICR5	Local Interrupt Control Register 5	1000 1000
0x00F0 0038	LICR6	Local Interrupt Control Register 6	1000 1000
0x00F0 003C	LICR7	Local Interrupt Control Register 7	1000 1000
0x00F0 0040	ICGSICR	ICGS Interrupt Control Register	1111 1000
0x00F0 0044	ICMSICR	ICMS Interrupt Control Register	1110 1001
0x00F0 0048	EGICR	Error Group Interrupt Control Register	1111 1000
0x00F0 004C	ICGSIVBR	ICGS Interrupt Vector Base Register	1111 1000
0x00F0 0050	ICMSIVBR	ICMS Interrupt Vector Base Register	1111 1000
0x00F0 0054	LIVBR	Local interrupt Vector Base Register	1111 1000
0x00F0 0058	EGIVBR	Error Group Interrupt Vector Base Register	1111 1000
0x00F0 005C	ICSR	Interprocessor Communications Switch Register	0000 0000
0x00F0 0060	ICR0	Interprocessor Communications Register 0	0000 0000
0x00F0 0064	ICR1	Interprocessor Communications Register 1	0010 0010
0x00F0 0068	ICR2	Interprocessor Communications Register 2	0000 0000
0x00F0 006C	ICR3	Interprocessor Communications Register 3	0100 0100
0x00F0 0070	ICR4	Interprocessor Communications Register 4	0000 0000
0x00F0 0074	ICR5	Interprocessor Communications Register 5	0000 0010
0x00F0 0078	ICR6	Interprocessor Communications Register 6	0111 1110
0x00F0 007C	ICR7	Interprocessor Communications Register 7	0000 0000

Table A-3 is continued on the following page.

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A.2 VIC64 Register Map and Descriptions (continued)

Table A-3: Model 4290 –VIC64 Register Map with Values After Firmware Loading (continued)

'C6x Address	Register	Description	Firmware Loaded Value
0x00F0 0080	VIRSR	VMEbus Interrupt Request Status Register	0000 0000
0x00F0 0084	VIVBR1	VMEbus Interrupt Vector Base Register 1	0000 0001
0x00F0 0088	VIVBR2	VMEbus Interrupt Vector Base Register 2	0000 0010
0x00F0 008C	VIVBR3	VMEbus Interrupt Vector Base Register 3	0000 0011
0x00F0 0090	VIVBR4	VMEbus Interrupt Vector Base Register 4	0000 0100
0x00F0 0094	VIVBR5	VMEbus Interrupt Vector Base Register 5	0000 0101
0x00F0 0098	VIVBR6	VMEbus Interrupt Vector Base Register 6	0000 0110
0x00F0 009C	VIVBR7	VMEbus Interrupt Vector Base Register 7	0000 0111
0x00F0 00A0	TTR	Transfer Timeout Register	0110 1000
0x00F0 00A4	LBTR	Local Bus Timing Register	0100 0100
0x00F0 00A8	BTDR	Block Transfer Definition Register	0110 1100
0x00F0 00AC	ICR	Interface Configuration Register	0100 0011
0x00F0 00B0	ARCR	Arbiter/Requester Configuration Register	0110 0000
0x00F0 00B4	AMSR	Address Modifier Source Register	0000 0000
0x00F0 00B8	BESR	Bus Error Status Register	0000 0000
0x00F0 00BC	DMASR	DMA Status Register	0000 0000
0x00F0 00C0	SS0CR0	Slave Select 0 Control Register 0	0001 0010
0x00F0 00C4	SS0CR1	Slave Select 0 Control Register 1	0100 0100
0x00F0 00C8	SS1CR0	Slave Select 1 Control Register 0	0101 0100
0x00F0 00CA	SS1CR1	Slave Select 1 Control Register 1	0100 0100
0x00F0 00D0	RCR	Release Control Register	0100 0000
0x00F0 00D4	BTCR	Block Transfer Control Register	0001 0000
0x00F0 00D8	BTLR1	Block Transfer Length Register 1	0000 0000
0x00F0 00DC	BTLR0	Block Transfer Length Register 0	0000 0000
0x00F0 00E0	SRR	System Reset Register	1111 1111

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.2 VMEbus Interrupt Control Registers 1 – 7

Name: VICR1 – 7

Register	Address	Interrupt
VICR1	**0x00F0 0004**	1
VICR2	**0x00F0 0008**	2
VICR3	**0x00F0 000C**	3
VICR4	**0x00F0 0010**	4
VICR5	**0x00F0 0014**	5
VICR6	**0x00F0 0018**	6
VICR7	**0x00F0 001C**	7

Description: Provides enabling of the VIC64 as VMEbus interrupt handler for any or all of the VMEbus interrupts. Seven registers exist to provide unique masking and IPL values for the seven VMEbus interrupts.

Bits 2 – 0: (0/*/*) IPL value: Value is inverted and driven onto the IPL signals when a VMEbus interrupt is acknowledged.

Bits 6 – 3: (1/1/1) Undefined/Reserved. Bits will read as 1's.

Bit 7: (1/1/1) VMEbus interrupt mask: When clear, the VIC64 acts as a VMEbus interrupt handler by signaling a local interrupt at the specified IPL level. When set, the VIC64 does not handle the VMEbus interrupt and no local interrupt is issued.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.3 DMA Status Interrupt Control Register

Name: DMASICR

Address: **0x00F0 0020**

Description: Provides enabling and IPL–level encoding for the DMA–complete interrupt issued by the VIC64 when any VIC64 local DMA operation completes (successfully or unsuccessfully).

Bits 2 – 0: (0/*/*) IPL value: Value is inverted and driven onto the IPL lines when interrupt is acknowledged.

Bits 6 – 3: (1/1/1) Undefined/Reserved. Bits will read as 1's.

Bit 7: (1/1/1) DMA status interrupt mask: When clear, the VIC64 signals a local interrupt at the completion of any VIC64 local DMA operation. When set, the VIC64 will not issue a local interrupt.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.4 Local Interrupt Control Registers 1 – 7

Name: LICR1 – 7

Register	Address
LICR1	**0x00F0 0024**
LICR2	**0x00F0 0028**
LICR3	**0x00F0 002C**
LICR4	**0x00F0 0030**
LICR5	**0x00F0 0034**
LICR6	**0x00F0 0038**
LICR7	**0x00F0 003C**

Description: Provides enabling, IPL level, and control of local interrupts 1 – 7 ($\overline{\text{LIRQ1 – 7}}$).

Bits 2 – 0: (0/*/*) IPL value: Value is inverted and driven onto the IPL lines when a local interrupt is presented on the $\overline{\text{LIRQ1 – 7}}$ signals and bit 7 of this register is clear (enabled).

Bit 3: (X/X/X) $\overline{\text{LIRQ1 – 7}}$ voltage state: A cleared bit indicates an $\overline{\text{LIRQ1 – 7}}$ signal is asserted at the VIC64.

Bit 4: (0/*/*) Autovector enable: When set, the VIC64 will supply the interrupt status/ID vector for the local interrupt acknowledge cycle. When cleared, the VIC64 will assert the $\overline{\text{LIACK0}}$ signal to indicate a 680x0 "autovector" condition or that the interrupting source should provide the Status/ID vector to the processor.

Bit 5: (0/*/*) Edge/level enable: When cleared, the VIC64 responds to the $\overline{\text{LIRQ1 – 7}}$ as a level–sensitive interrupt. When set, the VIC64 responds to $\overline{\text{LIRQ1 – 7}}$ as an edge–sensitive interrupt.

Bit 6: (0/*/*) Polarity set: When set, the VIC64 responds to interrupts as active High if bit 5 is set (level sensitive) or on a rising edge if bit 5 is cleared (edge sensitive). When cleared, the VIC64 responds to active Low or falling edges.

Bit 7: (1/1/1) Local interrupt mask: When clear, the VIC64 is enabled to handle the corresponding local interrupt asserted on the $\overline{\text{LIRQ1 – 7}}$ signals.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.5 ICGS Interrupt Control Register

Name: ICGSICR

Address: **0x00F0 0040**

Description: Provides enabling and IPL encoding for the four global switch interrupts.

Bits 2 – 0: (0/*/*) IPL Value: Value is inverted and driven onto the IPL signals when a global switch is acknowledged.

Bit 3: (1/1/1) Undefined/Reserved. Bit will read as a 1.

Bit 4: (1/1/1) ICGS0 mask: When clear, the VIC64 will issue and handle a local interrupt when global switch 0 is set.

Bit 5: (1/1/1) ICGS1 mask: When clear, the VIC64 will issue and handle a local interrupt when global switch 1 is set.

Bit 6: (1/1/1) ICGS2 mask: When clear, the VIC64 will issue and handle a local interrupt when global switch 2 is set.

Bit 7: (1/1/1) ICGS3 mask: When clear, the VIC64 will issue and handle a local interrupt when global switch 3 is set.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.6 ICMS Interrupt Control Register

Name: ICMSICR

Address: **0x00F0 0044**

Description: Provides enabling and IPL encoding for the four module switch interrupts.

Bits 2 – 0: (0/*/*) IPL Value: Value is inverted and driven onto the IPL signals when a module switch is acknowledged.

Bit 3: (1/1/1) Undefined/Reserved. Bit will read as a 1.

Bit 4: (1/1/1) ICMS0 mask: When clear, the VIC64 will issue and handle a local interrupt when module switch 0 is set.

Bit 5: (1/1/1) ICMS1 mask: When clear, the VIC64 will issue and handle a local interrupt when module switch 1 is set.

Bit 6: (1/1/1) ICMS2 mask: When clear, the VIC64 will issue and handle a local interrupt when module switch 2 is set.

Bit 7: (1/1/1) ICMS3 mask: When clear, the VIC64 will issue and handle a local interrupt when module switch 3 is set.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.7 Error–Group Interrupt Control Register

Name: EGICR

Address: **0x00F0 0048**

Description: Provides enabling and IPL encoding for the error group interrupts.

Bits 2 – 0: (0/*/*) IPL Value: Value is inverted and driven onto the IPL signals when an error group interrupt is acknowledged.

Bit 3: (X/X/X) $\overline{\text{SYSFAIL}}$ asserted: This bit is set whenever $\overline{\text{SYSFAIL}}$ is detected asserted.

Bit 4: (1/1/1) $\overline{\text{SYSFAIL}}$ interrupt mask: When clear, the VIC64 generates a local interrupt when $\overline{\text{SYSFAIL}}$ is asserted.

Bit 5: (1/1/1) Arbitration timeout interrupt mask: When clear, the VIC64 generates a local interrupt when an arbitration timeout has occurred.

Bit 6: (1/1/1) Write post fail interrupt mask: When clear, the VIC64 generates a local interrupt when a write post operation has failed due to a bus error. For master write posts, an assertion of $\overline{\text{BERR}}$ will trigger an interrupt. For slave write posts, an assertion of $\overline{\text{LBERR}}$ will trigger an interrupt.

Bit 7: (1/1/1) AC Fail interrupt mask: When clear, the VIC64 generates a local interrupt when $\overline{\text{ACFAIL}}$ is detected as asserted.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.8 ICGS Interrupt Vector Base Register

Name: ICGSIVBR

Address: **0x00F0 004C**

Description: Provides the status/ID vector for the global switch interrupts. This register must be written after any VIC64 reset to enable identification encoding for bits 1 – 0.

Bits 1 – 0: (X/X/X) Global switch number (read–only): This value indicates which global switch is pending during a global switch interrupt acknowledge cycle. These bits are used with bits 7 – 2 to pro–vide a unique status/ ID vector for each global switch. The numeric value of this field indicates the switch number. These bits are valid only during the interrupt acknowledge cycle.

Bits 7 – 2: (1/1/1 [3–2]) (0/0/0 [7–4]) Status/ID: These bits are user–definable and are used with bits 1 – 0 to provide a unique global switch interrupt status/ ID vector.

A.2.9 ICMS Interrupt Vector Base Register

Name: ICMSIVBR

Address: 0x00F0 0050

Description: Provides the status/ID vector for the module switch interrupts. This register must be written after any VIC64 reset to enable identification encoding for bits 1 – 0.

Bits 1 – 0: (X/X/X) Module switch number (read–only): This value indicates which module switch is pending during a module switch interrupt acknowledge cycle. These bits are used with bits 7 –2 to provide a unique status/ID vector for each module switch. The numeric value of this field indicates the switch number. These bits are valid only during the interrupt acknowledge cycle.

Bits 7 – 2: (1/1/1 [3–2]) (0/0/0 [7–4]) Status/ID: These bits are user–definable and are used with bits 1 – 0 to provide a unique global switch interrupt sta–tus/ ID vector.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.10 Local Interrupt Vector Base Register

Name: LIVBR

Address: **0x00F0 0054**

Description: Provides the status/ID vector for the local interrupts. This register must be written after any VIC64 reset to enable identification encoding for bits 2 – 0.

Bits 2 – 0: (X/X/X) Local Interrupt number (read–only): This value indicates which local interrupt is pending during a local interrupt acknowledge cycle. These bits are used with bits 7 – 3 to provide a unique status/ ID vector for each local interrupt. The numeric value of this field indicates the local interrupt number. These bits are valid only during the interrupt acknowledge cycle.

Bits 7 – 3: (1/1/1 [3]) (0/0/0 [7–4]) Status/ID: These bits are user–definable and are used with bits 2 – 0 to provide a unique local interrupt status/ID vector.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.11 Error Group Interrupt Vector Base Register

Name: EGIVBR

Address: **0x00F0 0058**

Description: Provides the status/ID vector for the error group interrupts. This register must be written after any VIC64 reset to enable identification encoding for bits 2 – 0.

Bits 2 – 0: (X/X/X) Error/Status Group Interrupt number (read–only): This value indicates which group interrupt is pending during the interrupt acknowledge cycle. These bits are used with bits 7 – 3 to provide a unique status/ID vector for each error group interrupt. These bits are valid only during the interrupt acknowledge cycle.

Bit 2 1 0	Error/Status Interrupt
0 0 0	$\overline{\text{ACFAIL}}$ asserted
0 0 1	Write post failed
0 1 0	Arbitration timeout
0 1 1	$\overline{\text{SYSFAIL}}$ asserted
1 0 0	VMEbus Interrupter interrupt acknowledge
1 0 1	DMA complete
1 1 0	Not used
1 1 1	Not used

Bits 7 – 3: (1/1/1 [3]) (0/0/0 [7–4]) Status/ID: These bits are user–definable and are used with bits 2 – 0 to provide a unique local interrupt status/ID vector.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.12 Interprocessor Communications Switch Register

Name: ICSR

Address: **0x00F0 005C**

Description: Provides setting, clearing, and monitoring of the interprocessor switch interrupts via the local bus. If the switch interrupts are enabled, setting these bits (more precisely, a clear–to–set transition) causes a local interrupt to occur in the same way as if the switch was set over the VMEbus.

Bits 3 – 0: (0/0/0) Module switches: Bits 0, 1, 2, and 3 correspond to ICMSs 0, 1, 2, and 3 respectively.

Bits 7 – 4: (0/*/0) Global switches: Bits 4, 5, 6, and 7 correspond to ICGSs 0, 1, 2, and 3 respectively.

A.2.13 Interprocessor Communication Registers 0 – 4

Name: ICR0 – 4

Register	Address
ICR0	**0x00F0 0060**
ICR1	**0x00F0 0064**
ICR2	**0x00F0 0068**
ICR3	**0x00F0 006C**
ICR4	**0x00F0 0070**

Description: These are general–purpose read/write registers that can be accessed from either the local bus or the VMEbus. The addresses listed above are the local addresses. See Section A.1 of this Appendix for details on accessing these registers from the VMEbus.

Bits 7 – 0: (0/0/0) Data field.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.14 Interprocessor Communication Register 5

Name: ICR5

Address: **0x00F0 0074**

Description: This register provides the VIC64 version/revision number. The address listed above is the local address.

Bits 7 – 0: (Version) VIC64 version/revision (read–only).

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.15 Interprocessor Communication Register 6

Name: ICR6

Address: **0x00F0 0078**

Description: This register provides local or remote reset and $\overline{\text{HALT}}$. The address listed above is the local address.

Bits 1 – 0: (X/1/0 [0]) (X/1/1 [1])

Reset/$\overline{\text{HALT}}$ status (read–only from VMEbus): These bits provide reset/$\overline{\text{HALT}}$ status of the VIC64 and local resources according to the following table:

Bit 1 0	Reset/$\overline{\text{HALT}}$ Status.
0 1	$\overline{\text{HALT}}$ has been asserted longer than 6 ms by a source other then the VIC64. These bits may both be reset by the local CPU to indicate local resources are running and operational.
1 0	The VIC64 has performed a local reset function and the VIC64 is not the system controller. These bits may both be reset by the local CPU to indicate local resources are running and operational.
1 1	Indicates that the CPU has just been released from a system reset.
0 0	Local resources are running and operational. This pattern must be written by the local CPU after a reset condition to indicate that local resources are running and operational.

Bits 5–2: (1/1/1) Undefined/Reserved. Bits will read as 1's.

Bit 6: (1/1/1) $\overline{\text{IRESET}}$ and $\overline{\text{HALT}}$ status (read–only from VMEbus): This bit is set upon assertion of $\overline{\text{IRESET}}$, and/or $\overline{\text{HALT}}$. It is set whether $\overline{\text{HALT}}$ is asserted by external sources or by the VIC64. SYSFAIL is asserted when this bit is set if the SYSFAIL mask bit (ICR7, bit 7, see Section A.2.16) is cleared.

Bit 7: (X/X/X) $\overline{\text{IRESET}}$ status (read–only): On a VMEbus read, this bit indicates that the VIC64 is in a reset state. On a local bus read, this bit is set whenever $\overline{\text{ACFAIL}}$ is asserted.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.16 Interprocessor Communication Register 7

Name: ICR7

Address: **0x00F0 007C**

Description: This register provides semaphores to the five general–purpose interprocessor communication registers (ICR4 – 0, see Section A.2.13). The remaining bits indicate VMEbus master status, generate HALT and RESET, and mask SYSRESET. The address listed above is the local address.

Bits 4 – 0:
(0/*/0 [0–3])
(0/X/0 [4])
ICR4 – 0 semaphores: These bits provide semaphores to the five interprocessor communication registers ICR4 – 0 respectively. Each bit is set when the corresponding ICR is written. These bits can be read or written from the local bus or the VMEbus.

Bit 5:
(X/X/X)
VMEbus master status (read–only): This bit is set whenever the VIC64 is the VMEbus master, and the VIC64 is asserting $\overline{\text{AS}}$. This bit is not set when the VIC64 is VMEbus master to an idle bus in ROR and BCAP release modes. Bit 7 of the BESR may be used to indicate that the VIC64 is VMEbus master when $\overline{\text{AS}}$ is not asserted.

Bit 6:
(0/0/0)
$\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ control: This bit may be used to assert the $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ pins via software. Whenever this bit is set, the VIC64 asserts $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ until this bit is cleared or any reset occurs.

Bit 7:
(0/*/0)
$\overline{\text{SYSFAIL}}$ mask: When set, the VIC64 is prohibited from asserting $\overline{\text{SYSFAIL}}$ in response to bit 6 of ICR6 being set (which, by default, is set after any reset).

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.17 VMEbus Interrupt Request Status Register

Name: VIRSR

Address: **0x00F0 0080**

Description: This register provides status and control of the VMEbus interrupts 7 – 1.

Bit 0: (0/0/0) Register enable/disable: This bit provides enabling and disabling for the remainder of this register.

Bits 7 – 1: (0/*/0) VMEbus interrupt switches: Setting any of these bits asserts the VMEbus $\overline{IRQi}$ signals corresponding to the bit positions, if bit 0 is set during the write. These bits are cleared by setting the appropriate bit and clearing bit 0.

A.2.18 VMEbus Interrupt Vector Base Registers 1 – 7

Name: VIVBR

Register	Address	for IRQ
VIVBR1	**0x00F0 0084**	1
VIVBR2	**0x00F0 0088**	2
VIVBR3	**0x00F0 008C**	3
VIVBR4	**0x00F0 0090**	4
VIVBR5	**0x00F0 0094**	5
VIVBR6	**0x00F0 0098**	6
VIVBR7	**0x00F0 009C**	7

Description: Provides the status/ID vector for the VMEbus interrupts.

Bits 7 – 0: (1/*/1 [0–3]) (0/*/0 [4–7]) Status/ID Vector: These bits provide the status/ID vector for VMEbus interrupt acknowledge cycles. Address 0xA800 0021 corresponds to $\overline{IRQ1}$. These bits are set to a value of 0x0F for global and system resets and are unchanged by internal resets.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.19 Transfer Timeout Register

Name: TTR

Address: **0x00F0 00A0**

Description: Provides control of the local and VMEbus timeout timers.

Bit 0: (0/0/0) Include VMEbus acquisition: When set, the local bus timer will include waiting for VMEbus acquisition. When clear, the local bus timer will stop and reset when the VMEbus is requested.

Bit 1: (0/0/0) Arbitration timeout: When set, the VIC64 as VMEbus arbiter has detected a VMEbus arbitration timeout. This is only used when configured as the VMEbus system controller ($\overline{\text{SCON}}$ asserted).

Bits 4 – 2: Local bus timeout period: Defines the local bus timeout.

Bit 4 3 2	Local Bus Timeout (µs)	
0 0 0	4	
0 0 1	16	
0 1 0	32	(default – state after any reset)
0 1 1	64	
1 0 0	128	
1 0 1	256	
1 1 0	512	
1 1 1	Infinite (timer disabled)	

Bits 7 – 5: VMEbus timeout period: Defines the VMEbus timeout.

Bit 7 6 5	Local Bus Timeout (µs)	
0 0 0	4	
0 0 1	16	
0 1 0	32	
0 1 1	64	(default – state after any reset)
1 0 0	128	
1 0 1	256	
1 1 0	512	
1 1 1	Infinite (timer disabled)	

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.20 Local Bus Timing Register

Name: LBTR

Address: **0x00F0 00A4**

Description: Provides timing control for $\overline{\text{PAS}}$ and $\overline{\text{DS}}$ signals when the VIC64 is local bus master. In the following descriptions, **n** is the binary value specified in the bit fields, and **T** is one CLK64M clock period. Clock latency may add one additional clock period to these times.

Bits 3 – 0: (0/*/*) Minimum $\overline{\text{PAS}}$ asserted time: This field specifies the *minimum* asserted time for the $\overline{\text{PAS}}$ signal whenever the VIC64 is the local bus master. The time is specified by (n+2)T. The actual asserted time depends on a number of factors including local and VMEbus acknowledge timing.

Bit 4: (0/*/*) Minimum $\overline{\text{DS}}$ deasserted time: This field specifics the *minimum* deasserted time for the $\overline{\text{DS}}$ signal whenever the VIC64 is the local bus master. A time of 1T is selected when this bit is clear; 2T is selected when this bit is set.

Bits 7 – 5: (0/*/*) Minimum $\overline{\text{PAS}}$ deasserted time: This field specifies the *minimum* deasserted time for the $\overline{\text{PAS}}$ signal whenever the VIC64 is the local bus master. The time is specified by (n+1)T.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.21 Block Transfer Definition Register

Name: BTDR

Address: **0x00F0 00A8**

Description: Configures master block transfers (both MOVEM and block transfers with local DMA) for boundary crossings, dual–path, and user–defined address modifiers. Refer to Chapter 10 of Cypress Semiconductor's **VIC068A User's Guide**, and the **VIC64 Design Notes** for more details on implementing these features.

Bit 0: (0/0/0) Dual–path enable: When set, the VIC64 is enabled with the dual–path feature during master block transfers with local DMA. External logic is required when this option is enabled.

Bit 1: (0/0/0) AMSR Enable: When set, the VIC64 will issue the AM codes based in the address modifier source register for block transfers. This bit effects the AM codes for block transfers only.

Bit 2: (0/0/0) Local boundary crossing enable: When this bit is set, it enables local address 256–byte boundary crossings during DMA block transfer operations. External logic is required to increment latched address lines when this option is enabled.

Bit 3: (0/0/0) VME boundary crossing enable: When this bit is set, it enables VMEbus address 256–byte boundary crossings during DMA block transfer operations. External logic is required to incre–ment latched address lines when this option is enabled.

Bit 4: (0/0/0) D64 Master Enable: When bit 6 of the Block Transfer Control Register (see Section A.2.32) is set, setting this bit enables VME–bus master operations by the VIC64 in D64 mode.

Bit 5: (0/0/0) Accellerated Block Transfer Enable: When this bit is set, block transfers are accellerated by reducing the DSACK to DTACK time defined in the Slave Select Control Registers by half a CLK64M period for both master and slave block transfers. The resultant delays will range from 1.5 to 8.5 clock periods when this bit is set, or from 2 to 9 periods when this bit is cleared.

Bit 6: (0/0/0) D64 Slave Enable: Setting this bit enables slave operation in D64 Mode.

Bit 7: (0/0/0) Extended Local Boundary Crossing Enable: When this bit is set, it enables local address 2 kByte boundary crossings during D64 Master block transfer operations. External logic is required to increment latched address lines when this option is enabled. For proper operation, the transfer **MUST** be aligned to a 2 kByte boundary.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.22 Interface Configuration Register

Name: ICR

Address: **0x00F0 00AC**

Description: Controls various features of the VIC64 including RMCs, dead–lock signaling, metastablility delays, and the "turbo" feature.

Bit 0: (X/X/X) — SCON value (read–only): Reports the level of the SCON/D64 pin at the last reset. When this pin is held high during reset, the VIC64 is not the VMEbus system controller. When it is held low during reset, the VIC64 is the VMEbus system controller.

Bit 1: (0/0/0) — Turbo enable: When set, the VIC64 accelerates VMEbus transfers by reducing selected timings by one CLK64M clock period. VMEbus protocols may be violated when the turbo mode is enabled (see Section 12.5 of Cypress Semiconductor's **VIC068A/VAC068A User's Guide**).

Bit 2: (0/0/0) — Metastability interval: When set, the VIC64 adds one additional CLK64M clock period of metastability delay on asynchronous inputs (from 3 CLK64M periods to 4).

Bits 4, 3: (0/0/0) — Deadlock signaling: These bits configure deadlock signaling. Bit 4 is used to enable the assertion of HALT and LBERR in addition to the DEDLK signal in deadlock situations. If bit 4 is enabled, bit 3 may be used to prevent the assertion of HALT for RMC deadlocks.

Bit 4 3	Deadlock Signaling
0 X	DEDLK only (default)
1 0	HALT, LBERR, DEDLK
1 1	HALT, LBERR, DEDLK (HALT is not asserted for RMC cycles)

Bit 5: (0/0/0) — RMC control bit 1: When set, the VIC64 will request the VMEbus whenever the RMC is asserted independent of the MWB signal.

Bit 6: (0/0/0) — RMC control bit 2: When set, the VMEbus AS is stretched when RMC is asserted for VMEbus transfers.

Bit 7: (0/0/0) — RMC control bit 3: When set, the VIC64 qualifies the RMC control bits 1 and 2 with the SIZ1/0 signals. If RMC control bits 1 or 2 are set and the first cycle of the RMC transfer is of byte size, the "set" behaviors are not implemented.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.23 Arbiter/Requester Configuration Register

Name: ARCR

Address: **0x00F0 00B0**

Description: This register provides configuration of the fairness timeout and DRAM refresh features. The VMEbus request level is also configured from this register.

Bits 3 – 0: (0/0/0) Fairness timer enable: The VMEbus fair requester is enabled in this bit field according to the following table:

Bits 3 – 0	Timeout Period/Mode
0,0,0,0	Fairness disabled (default)
1,1,1,1	Timeout disabled
All other patterns	2 µs times number

Bit 4: (0/*/*): DRAM refresh: When set, the VIC64 will perform CAS–before–RAS ($\overline{DS}$ before $\overline{PAS}$) refresh functions.

Bits 6, 5: (1/1/1) VMEbus request level: The VMEbus request level is set according to the following table:

Bit 6 5	VMEbus Request Level
0 0	BR0
0 1	BR1
1 0	BR2
1 1	BR3 (default)

Bit 7: (0/0/0) Arbitration mode: When set, the VIC64 performs priority VMEbus arbitration. When clear, the VIC64 performs round–robin arbitration. This bit is only relevant when the VIC64 is configured as the VMEbus system controller ($\overline{SCON}$ asserted at power–up).

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.24 Address Modifier Source Register

Name: AMSR

Address: **0x00F0 00B4**

Description: This register provides the user–definable address modifiers (AM codes) that can be sourced by the VIC64 for VMEbus master cycles, or used in validating AM codes during VMEbus slave cycles.

Bits 5 – 0: (0/0/0) Address modifier code: The AM code that is issued during master cycles or used for qualifying slave cycles. This register is used only when enabled for user–defined AM codes. Otherwise, standard VMEbus AM codes are used.

Bit 6: (0/0/0) AM5 – 3 qualification: When set, the VIC64 uses bits 5 – 3 in qualifying for slave accesses in addition to the address space size information defined by bits 3 and 2 of the SSiCR0s. This bit is over–ridden if bits 3 and 2 of the SSiCR0s are both clear.

Bit 7: (0/0/0) AM2 – 0 generation: When set, the VIC64 issues the AM2 – 0 codes based on the FC2/1 signals. AM5 – 3 will be issued from bits 5 – 3 of this register. This bit is overridden if the VIC64 is configured to issue all AM bits from this register (i. e., ASIZ1 = ASIZ0 = Low).

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.25 Bus Error Status Register

Name: BESR

Address: **0x00F0 00B8**

Description: This register provides $\overline{\text{BERR}}$/$\overline{\text{LBERR}}$, self–access, VMEbus mastership, and timeout status. All bits except bit 7 are flags that must be cleared manually by the local processor after being set by status conditions. If these bits are to be used for a specific operation, it is important that they be cleared prior to starting that operation.

Bit 0: (0/0/0) Local timeout during VMEbus acquisition: This bit, when set, indicates that a local bus timeout has occurred during an attempted acquisition of the VMEbus.

Bit 1: (0/0/0) $\overline{\text{SLSEL1}}$ self–access: This bit is set when the VIC64 is selected by the assertion on the $\overline{\text{SLSEL1}}$ signal, while operating as VMEbus master.

Bit 2: (0/0/0) $\overline{\text{SLSEL0}}$ self–access: This bit is set when the VIC64 is selected by the assertion on the $\overline{\text{SLSEL0}}$ signal, while operating as VMEbus master.

Bit 3: (0/0/0) Local bus timeout: This bit, when set, indicates a local bus timeout occurred without qualification.

Bit 4: (0/0/0) VMEbus timeout: This bit, when set, indicates the VIC64 has signaled a VMEbus timeout. This bit is relevant only if the VIC64 is system controller and the VMEbus timeout is enabled.

Bit 5: (0/0/0) VMEbus bus error: This bit is set when a VMEbus bus error is signaled ($\overline{\text{BERR}}$ asserted).

Bit 6: (0/0/0) Local bus error: This bit is set when a local bus error is signaled a source other then the VIC64 ($\overline{\text{LBERR}}$ asserted to the VIC64).

Bit 7: (X/X/X) VMEbus mastership: This bit is set whenever the VIC64 is VMEbus master.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.26 DMA Status Register

Name: DMASR

Address: **0x00F0 00BC**

Description: This register provides status of a VIC64 DMA transfer. This includes the block transfer with local DMA function and the module–based DMA function. Status bits are included to show various BERR and LBERR statuses and DMA termination statuses.

Bit 0: (0/0/0) Block transfer in progress: This bit, when set, indicates an interleaved block transfer is in progress. Once set, this bit must be cleared manually by writing a 0 (zero) to this bit location, or by resetting the VIC64.

Bit 1: (0/0/0) $\overline{\text{LBERR}}$ during DMA transfer: This bit, when set, indicates a $\overline{\text{LBERR}}$ was signaled during a DMA transfer. Once set, this bit must be cleared manually by writing a 0 (zero) to this bit location, or by resetting the VIC64.

Bit 2: (0/0/0) $\overline{\text{BERR}}$ during DMA transfer: This bit, when set, indicates a BERR was signaled during a DMA transfer. Once set, this bit must be cleared manually by writing a 0 (zero) to this bit location, or by resetting the VIC64.

Bit 3: (0/0/0) Local bus error (read–only): This bit is set when a local bus error is signaled by a source other then the VIC64 ($\overline{\text{LBERR}}$ asserted to the VIC64). This bit is a read–only copy of bit 6 of the BESR (see Section A.2.25).

Bit 4: (0/0/0) VMEbus bus error: This bit is set when a VMEbus bus error is signaled ($\overline{\text{BERR}}$ asserted). This bit is a copy of bit 5 of the BESR (see Section A.2.25).

Bits 5, 6: (1/1/1) Undefined/Reserved. These bits will be read as 1's.

Bit 7: (0/0/0) Master write post information stored: This bit is set whenever master write post information is stored.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.27 Slave Select 0 Control Register 0

Name: SS0CR0

Address: **0x00F0 00C0**

Description: This register provides control of the slave selection 0 facilities of the VIC64. Enabling of the $\overline{\text{LIRQ2}}$ timer interrupt is also configured in this register.

Bits 1 – 0: (0/*/*) Local transfer mode: These bits set the local transfer mode when the VIC64 is local bus master for both slave and master block transfers.

Bit 1 0	Mode
0 0	No support is given for slave block transfers on $\overline{\text{SLSEL0}}$. The VIC64 will $\overline{\text{BERR}}$ any attempt to receive a VMEbus block transfer. Master block transfers with local DMA will not function in this mode.
0 1	Emulate single–cycle transfers on the local bus. In this mode, the VIC64 emulates single–cycle transfers when performing slave block transfers and master block transfers with local DMA. By emulating single–cycle transfers, the VIC64 toggles the $\overline{\text{PAS}}$ for each cycle. $\overline{\text{DSACKi}}$ must toggle for each transfer and not be held asserted.
1 0	Accelerated transfers on the local bus. In this mode, the VIC64 asserts the $\overline{\text{PAS}}$ signal for the entire slave block transfer and master block transfer with local DMA. The $\overline{\text{DSACKi}}$ signals should be held asserted in this mode.
1 1	Undefined/Reserved.

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A.2 VIC64 Register Map and Descriptions (continued)

1.2.27 Slave Select 0 Control Register 0 (continued)

Bits 3 – 2: (0/*/*) — Address space configuration: The $\overline{\text{SLSEL0}}$ address space is configured according to the following table:

Bit 3	Bit 2	Address Space
0	0	A32 (extended) (default)
0	1	A24 (standard)
1	0	A16 (short)
1	1	User defined, uses AMSR

Bit 4: (0/*/*) — D32 enable: D32 slave operations are enabled for $\overline{\text{SLSEL0}}$ when this bit is set. This bit has no effect for enabling D32 master accesses. This bit also controls byte–lane switching for D16 Block transfers. When set $\overline{\text{ISOBE}}$ and $\overline{\text{SWDEN}}$ alternate states thus alternating which D16 bus data is placed. When clear, only $\overline{\text{SWDEN}}$ is asserted for D16 block transfers.

Bit 5: (0/*/*) — Supervisory access: When set, $\overline{\text{SLSEL0}}$ slave accesses are restricted to supervisory accesses. Other accesses are $\overline{\text{BERR}}$ed. Supervisory accesses are checked with the AM(2) signal.

Bits 7–6: (0/0/0) — Periodic interrupt timer enable: These bits enable and determine the frequency of the periodic $\overline{\text{LIRQ2}}$ interrupt. If the VIC64 is to handle this local interrupt, LICR2 must be enabled. The frequencies for this interrupt are given below:

Bit 7	Bit 6	Timer Mode
0	0	Timer disabled (default)
0	1	50 Hz output on $\overline{\text{LIRQ2}}$
1	0	1000 Hz output on $\overline{\text{LIRQ2}}$
1	1	100 Hz output on $\overline{\text{LIRQ2}}$

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.28 Slave Select 0 Control Register 1

Name: SS0CR1

Address: **0x00F0 00C4**

Description: This register provides the various access and acquisition timings for slave transfers and slave block transfers for $\overline{\text{SLSEL0}}$ in addition to data acquisition timing for master block transfers with local DMA.

Bits 3 – 0: (0/*/*) Timing field 0: This bit field establishes the following data access/acquisition timings:

- single–cycle slave access timing for $\overline{\text{SLSEL0}}$ (SAT)
- first cycle of a slave block transfer for $\overline{\text{SLSEL0}}$ (SBAT0)
- first cycle of a master block transfer with local DMA (MBAT0)
- first cycle of a module–based DMA transfer (DMAAT0)

The delays are programmed in multiples of the CLK64M clock period according to the table below.

Bit 3 2 1 0	Delay
0 0 0 0	0
0 0 0 1	2.0
0 0 1 0	2.5
0 0 1 1	3.0
0 1 0 0	3.5
0 1 0 1	4.0
0 1 1 0	4.5
0 1 1 1	5.0
1 0 0 0	5.5
1 0 0 1	6.0
1 0 1 0	6.5
1 0 1 1	7.0
1 1 0 0	7.5
1 1 0 1	8.0
1 1 1 0	8.5
1 1 1 1	9.0

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A.2 VIC64 Register Map and Descriptions (continued)

1.2.28 Slave Select 0 Control Register 1 (continued)

Bits 7 – 4: (0/*/*)

Timing Field 1: This bit field establishes the following data access/acquisition timings:

- second and subsequent cycle of a slave block transfer for SLSEL0 (SBAT1)
- second and subsequent cycle of a master block transfer with local DMA (MBAT1)
- second and subsequent cycle of a module–based DMA transfer (DMAAT1)

The delays are programmed in multiples of the CLK64M clock period according to the table below.

Bit 7 6 5 4	Delay
0 0 0 0	0
0 0 0 1	2.0
0 0 1 0	2.5
0 0 1 1	3.0
0 1 0 0	3.5
0 1 0 1	4.0
0 1 1 0	4.5
0 1 1 1	5.0
1 0 0 0	5.5
1 0 0 1	6.0
1 0 1 0	6.5
1 0 1 1	7.0
1 1 0 0	7.5
1 1 0 1	8.0
1 1 1 0	8.5
1 1 1 1	9.0

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.29 Slave Select 1 Control Register 0

Name: SS1CR0

Address: **0x00F0 00C8**

Description: This register provides control of the slave selection 1 facilities of the VIC64. Master and slave write posting is enabled in this register as well.

Bits 1 – 0: (0/*/*) Local transfer mode: These bits set the local transfer mode when the VIC64 is local bus master for both slave and master block transfers.

Bit 1 0	Mode
0 0	No support is given for slave block transfers on $\overline{\text{SLSEL1}}$. The VIC64 will $\overline{\text{BERR}}$ any attempt to receive a VMEbus block transfer.
0 1	Emulate single–cycle transfers on the local bus. In this mode, the VIC64 emulates single–cycle transfers when performing slave block transfers. By emulating single–cycle transfers, the VIC64 toggles the $\overline{\text{PAS}}$ for each cycle. $\overline{\text{DSACKi}}$ must toggle for each transfer and not be held asserted.
1 0	Accelerated transfers on the local bus. In this mode, the VIC64 asserts the $\overline{\text{PAS}}$ signal for the entire slave block transfer. The $\overline{\text{DSACKi}}$ signals should be held asserted in this mode.
1 1	Undefined/Reserved.

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A.2 VIC64 Register Map and Descriptions (continued)

1.2.29 Slave Select 1 Control Register 0 (continued)

Bits 3 – 2: (0/*/*) Address space configuration: The SLSEL1 address space is configured according to the following table:

Bit 3	2	Address Space
0	0	A32 (extended) (default)
0	1	A24 (standard)
1	0	A16 (short)
1	1	User defined, uses AMSR

Bit 4: (0/*/*) D32 enable: D32 slave operations are enabled for $\overline{\text{SLSEL1}}$ when this bit is set. This bit has no effect for enabling D32 master accesses.

Bit 5: (0/*/*) Supervisory access: When set, $\overline{\text{SLSEL1}}$ slave accesses are restricted to supervisory accesses. Other accesses are $\overline{\text{BERR}}$ed. Supervisory accesses are checked with the AM(2) signal.

Bit 6: (0/0/0) Master write post enable: When set, master write posting is enabled.

Bit 7: (0/0/0) Slave write post enable: When set, slave write posting is enabled.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.30 Slave Select 1 Control Register 1

Name: SS1CR1

Address: **0x00F0 00CA**

Description: This register provides the various access and acquisition timings for slave transfers and slave block transfers for $\overline{\text{SLSEL1}}$.

Bits 3 – 0: (0/*/*) Timing field 0: This bit field establishes the following data access/acquisition timings:

- single–cycle slave access timing for $\overline{\text{SLSEL0}}$ (SAT)
- first cycle of a slave block transfer for $\overline{\text{SLSEL0}}$ (SBAT0)

The delays are programmed in multiples of the CLK64M clock period according to the table at the bottom of this page.

Bits 7 – 4: (0/*/*) Timing field 1: This bit field establishes the second and subsequent cycle of a slave block transfer for SLSEL1 (SBAT1)

The delays are programmed in multiples of the CLK64M clock period according to the table below.

Timing Field 0: Bit 3 2 1 0 Timing Field 1: Bit 7 6 5 4	Delay
0 0 0 0	0
0 0 0 1	2.0
0 0 1 0	2.5
0 0 1 1	3.0
0 1 0 0	3.5
0 1 0 1	4.0
0 1 1 0	4.5
0 1 1 1	5.0
1 0 0 0	5.5
1 0 0 1	6.0
1 0 1 0	6.5
1 0 1 1	7.0
1 1 0 0	7.5
1 1 0 1	8.0
1 1 1 0	8.5
1 1 1 1	9.0

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.31 Release Control Register

Name: RCR

Address: **0x00F0 00D0**

Description: This register configures the VMEbus release mode. The burst count for block transfers with local DMA is also configured in the RCR.

Bits 5 – 0: (0/0/0) Block transfer burst length: The burst length for both MOVEM block transfers and block transfers with local DMA are config–ured in this bit field. The value indicates the number of cycles per block transfer (not the number of bytes). A value of 0 in this bit field indicates the maximum 64 cycles per burst. All other values correspond directly to the burst count.

For MBLT operations (D64 transfers) the burst length is 4 times the contents of this field. A value of 0 in this field when D64 operation is enabled will result in a burst length of 256 (64 x 4) cycles.

Bits 7, 6: (0/0/0) Release mode: This bit field defines the release mode used by the VIC64 when releasing the VMEbus after the completion of a VMEbus transfer.

Bit 7 6	Release Mode
0 0	ROR – Release on Request (default)
0 1	RWD – Release When Done
1 0	ROC – Release on BCLR assertion
1 1	BCAP – VMEbus Capture and Hold

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.32 Block Transfer Control Register

Name: BTCR

Address: **0x00F0 00D4**

Description: The BTCR provides control of the VIC64 block transfers. The local interleave periods and data direction are defined in this register. The enabling bits for all of the VIC64's block transfer modes are located here as well. These enabling bits are mutually exclusive and more than one should not be set at the same time.

Bits 3 – 0: (0/0/0) Interleave period: The interleave period for block transfers is defined here. The interleave period is 250 ns times the value programmed in this bit field.

Bit 4: (0/0/0) Data direction: This bit defines the direction of a block transfer with local DMA (MOVEM data direction determined by the R/W signal). When set, VMEbus block reads occur. When clear, VMEbus block writes occur.

Bit 5: (0/0/0) MOVEM enable: When set, MOVEM transfers are enabled. After this bit is set, the next VMEbus transfer is treated as the start of a VMEbus block transfer. Clearing this bit concludes a MOVEM block transfer in progress. It is important to set this bit immediately before and clear this bit immediately after the actual MOVEM transfer.

Bit 6: (0/0/0) Block transfer with local DMA enable: When set, block transfers with local DMA are enabled. After this bit is set, the next assertion of MWB is considered the initiation cycle of a VMEbus block transfer with local DMA. It is important to set this bit immediately before and clear this bit immediately after the actual block transfer.

Bit 7: (0/0/0) Module–based DMA transfer enable: When set, module–based DMA transfers are enabled. After this bit is set, the next assertion of BLT by external logic is considered the initiation cycle of a module–based DMA transfer. Clearing this bit concludes a module–based DMA transfer in progress. It is important to set this bit immediately before and clear this bit immediately after the actual DMA transfer.

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A.2 VIC64 Register Map and Descriptions (continued)

A.2.33 Block Transfer Length Registers 2 – 0

Name: BTLR2 – 0

Addresses: **0x00F0 00D8** (BTLR1)
0x00F0 00DC (BTLR0)
0x00F0 00E4 (BTLR2)

Description: These registers configure the 24–bit value used as the byte count for block transfers with local DMA. BTLR2 is considered the most significant byte, BTLR1 the middle byte, and BTLR0 the least significant. Bit 0 of BTLR0 must never be set because this implies at least one 8–bit transfer is required to complete the block transfer, Only D16, D32 and D64 block transfers are supported. If bit 0 of BTLR0 is set, the block transfer length is ignored and only one burst is performed.

Bits 7 – 0: (0/0/0) Block transfer length: Defines the block transfer length in bytes. BTLR2 contains the most significant 8 bits of the length, BTLR1 the middle 8 bits, and BTLR0 the least significant byte.

A.2.34 System Reset Register

Name: SRR

Address: **0x00F0 00E0**

Description: The system reset register provides the means to perform a VMEbus system reset (SYSRESET asserted). Writing a value of 0xF0 causes this function to occur. A system reset is also performed within the VIC64.

Bits 7 – 0: (1/1/1) System reset field: Writing this bit field with a value of 0xF0 causes SYSRESET to be asserted for a minimum of 200 ms and a system reset to be performed within the VIC64.

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Appendix B: JTAG Controller Application Note

Included for your reference on the following pages is an Application Note, provided by the courtesy of Texas Instruments, Inc., Houston, TX, about the architecture, operation and programming of their SN74ACT8990 Test Bus Controller, which is used as the JTAG controller on the Model 4290/4291.

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Application Report
SCAA044 - August 2000

Test-Bus Controller SN74ACT8990

Peter Forstner — *Standard Linear & Logic*

ABSTRACT

This application report describes IEEE Std 1149.1 test-bus controller (TBC) SN74ACT8990 from Texas Instruments (TI™). The first part explains the architecture and operation of the TBC; the second part uses examples to explain the programming procedure.

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1 Introduction

There has been a dramatic increase in the complexity of electronic systems as a result of advances in the integration of semiconductors, the introduction of new packaging techniques [surface-mount device (SMD)], and the consequent use of double-sided circuit boards. However, increased component density on circuit boards presents challenges to testability because the number of necessary test vectors increases out of proportion with complexity. By using nail-bed adapters, it is possible to partition the system to be tested, thereby reducing significantly the number of test vectors, although high SMD component density on double-sided boards reduces the number of possible contact areas for nail-bed adapters. Therefore, the escalating problems of testability can be solved only with a completely new concept.

In 1985, leading electronic manufacturers founded the Joint Test Action Group (JTAG) to develop a new and cost-effective test concept. The result of this was IEEE Std 1149.1. This standard requires the use of special test circuits at the inputs and outputs of selected semiconductor components, together with logic to control such test circuits. A 4-wire serial test bus combines the test circuits into a complete test group that is controlled via the test bus. In this way, with only four lines, the complete system can be partitioned and tested.

TI application report EB193 describes these test methods in detail, and presents IEEE Std 1149.1-compatible system controllability observability partitioning environment (SCOPE™) bus drivers from TI. Application report EB203 assumes an understanding of test methods compliant to IEEE Std 1149.1.

The control of an IEEE Std 1149.1-compatible test system usually is performed by a computer. TBC SN74ACT8990, which can be connected to a computer like a normal interface circuit, completely controls the IEEE Std 1149.1 test bus (see Figure 1). The computer first configures the TBC, then loads in parallel the test commands and test vectors. The TBC transfers these commands and vectors to the system, thereby generating the signal sequence required by IEEE Std 1149.1. The processor can read the result in parallel from the TBC, after the test data has addressed the logic to be tested. This application report describes the operation of the TBC, and explains the programming procedure with examples.

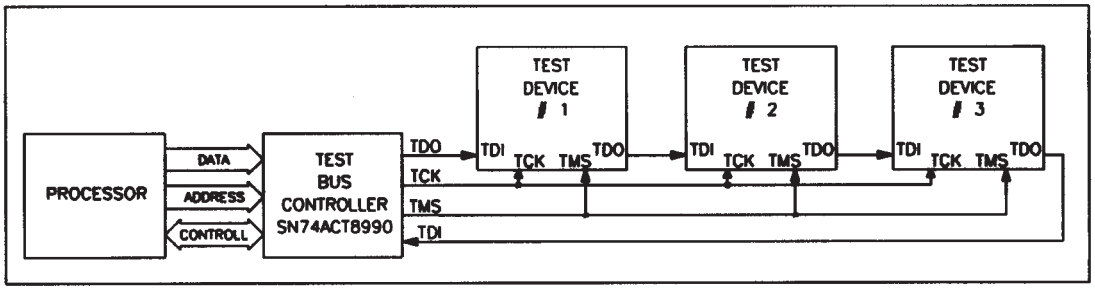


Figure 1. Test System With TBC SN74ACT8990

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To reduce the applications work by the user needed to control IEEE Std 1149.1-compatible test systems, TI offers the computer program Advanced Support System for Emulation and Test (ASSET™) together with a plug-in computer board. TBC SN74ACT8990 is used on this board. ASSET allows easy development of test programs for which the user needs no understanding of the function of the TBC. First, a library with the IEEE Std 1149.1-compatible circuits that are to be used must be assembled. A library with all standard TI components is supplied. Then, the complete system to be tested must be described with components from the library. After the system description, ASSET needs only the test vectors before testing can begin. This system also is suited ideally to supporting the circuit designer during the test phase.

If built-in self-test (BIST) is to be incorporated into an electronic system, TBC SN74ACT8990, in combination with the scan-path selector SN74ACT8999 and a microprocessor, provides an ideal basis (see Figure 2). The main computer can give the microprocessor the signal to start BIST via the IEEE Std 1149.1 test bus. The result of the self-test is communicated from the microprocessor to the main computer.

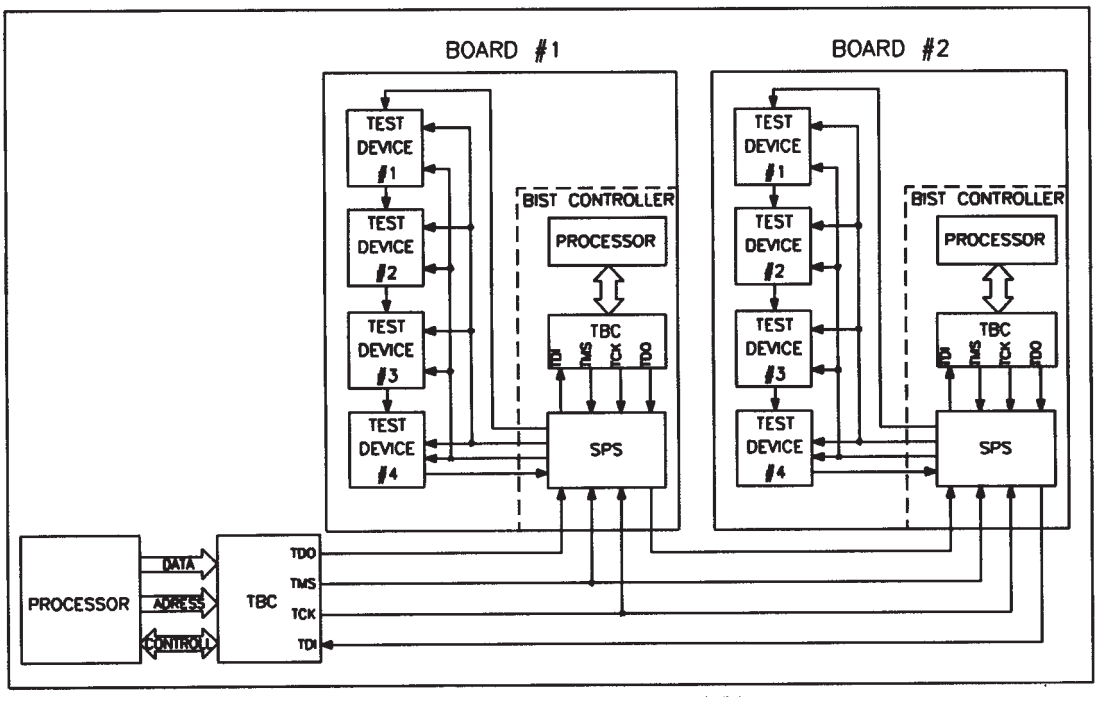


Figure 2. System With Built-In Self-Test (BIST)

If a large system is composed of several subsystems, it is advantageous to have BIST in each subsystem. The self-test then can be implemented simultaneously in all subsystems, resulting in significant reduction of test time.

This is one of the cases in which direct programming of the TBC is necessary, and in which this application report is intended to give assistance.

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2 Hardware

TBC SN74ACT8990 provides the interface between a processor and the IEEE Std 1149.1 test bus. Both interfaces can be operated asynchronously, that is, the clock of the computer does not need to be synchronized with the test clock TCK.

2.1 Processor Interface

The processor interface consists of the following:

- 5-bit address bus (A0–A4)
- 16-bit data bus (D0–D15)
- Read line ($\overline{RD}$)
- Write line ($\overline{WR}$)
- Status line ($\overline{RDY}$)
- Interrupt line ($\overline{INT}$)

The TBC is connected to the processor like a normal interface circuit, whereby the address decoder can be implemented as PAL (see Figure 3). Clock signal TCLK is buffered in the TBC, then transferred to the test system as the TCK signal, which can be derived from an independent clock generator or the processor clock, or be provided from the test system.

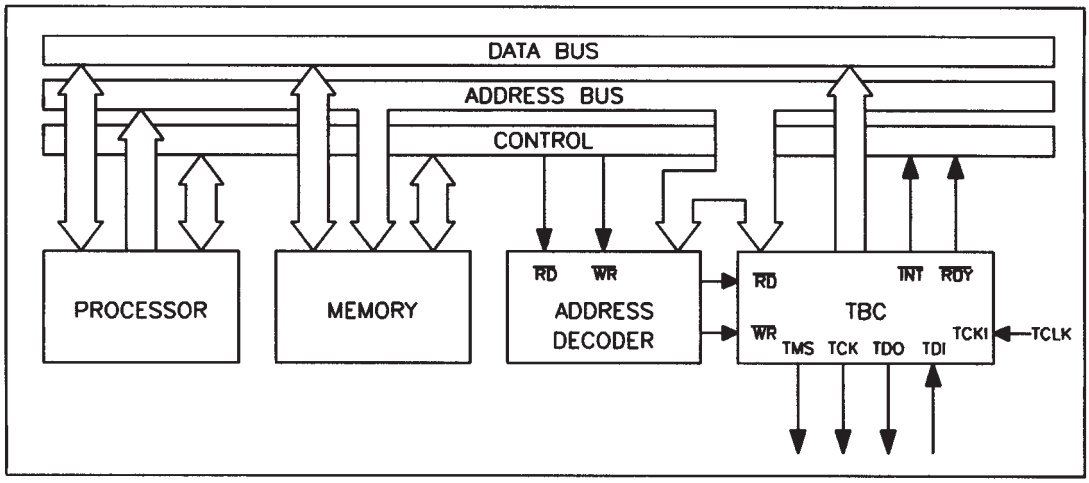


Figure 3. Connection of the TBC to a Microprocessor

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Five address lines can be used to address 24 internal registers:

- Ten control registers
- Two command registers
- Six registers to control internal counters
- Four status registers
- One register for transmit data
- One register for receive data

Sixteen registers can be read and overwritten, seven are readable only, and one register can only be written to. The remaining eight potential registers are not occupied. Section 3, Programming, gives details of the registers. The timing of a write cycle is shown in Figure 4, and a read cycle is shown in Figure 5.

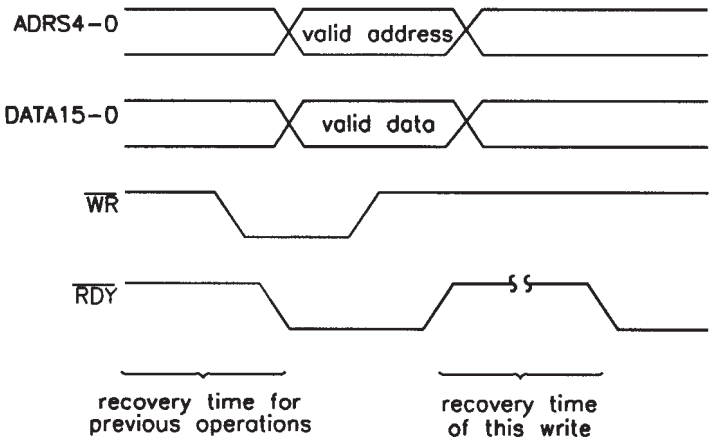


Figure 4. Timing Diagram of Processor Interface When Writing

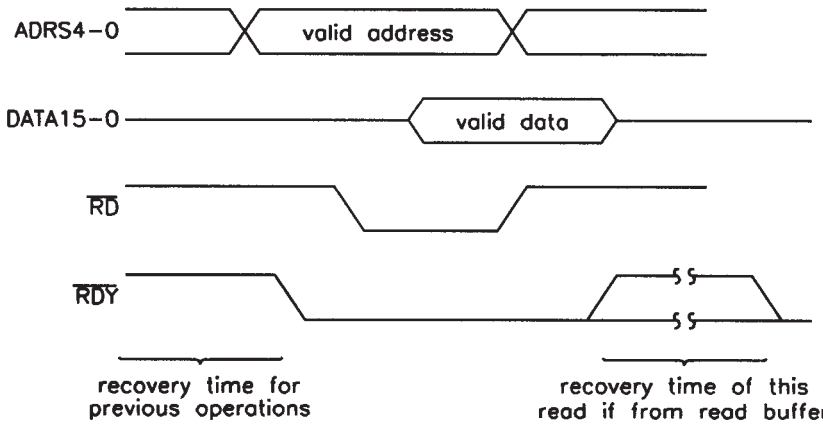


Figure 5. Timing Diagram of Processor Interface When Reading

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2.2 Test Bus Interface

According to IEEE Std 1149.1, the test bus interface consists of:

- One test pulse input (TCKI)
- One test pulse output (TCKO)
- One test data output (TDO)
- Two test data inputs (TDI0, TDI1)
- Two test mode select outputs (TMS0, TMS1)
- Four lines, which can be used as further TMS outputs (TMS2–TMS5), or can be programmed as event inputs/outputs (EVENT0–EVENT3)
- One line, test bus off ($\overline{\text{TOFF}}$), to reset all test outputs to a high-resistance state
- One input, test bus reset ($\overline{\text{TRST}}$), to reset the TBC and all test circuits. The use of this input is optional because the TBC and the test systems have a software reset.

Figure 6 shows the connection of an IEEE Std 1149.1 test system to the TBC. Here, only one TMS signal is needed so that ,in this case, all four event inputs/outputs (EVENT0–EVENT3) are available. Because signals TMS2–TMS5 use the same lines as event inputs/outputs, the number of available event inputs/outputs is reduced if more than two test systems are connected to the TBC (see Figure 7).

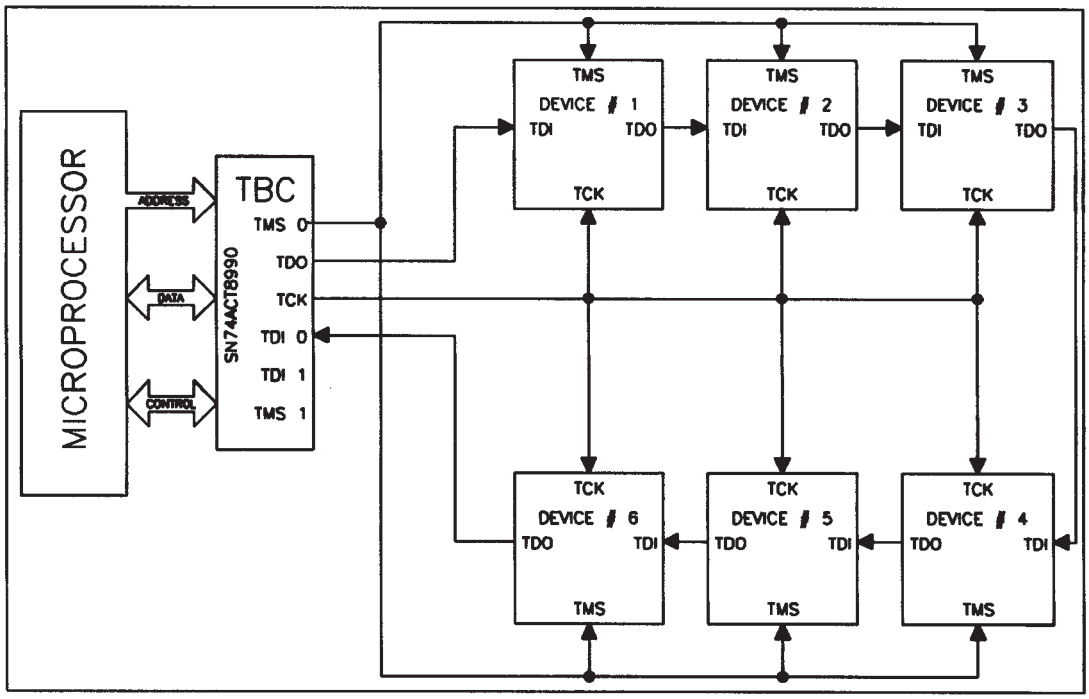


Figure 6. Connection of a IEEE Std 1149.1 Test Bus to the TBC

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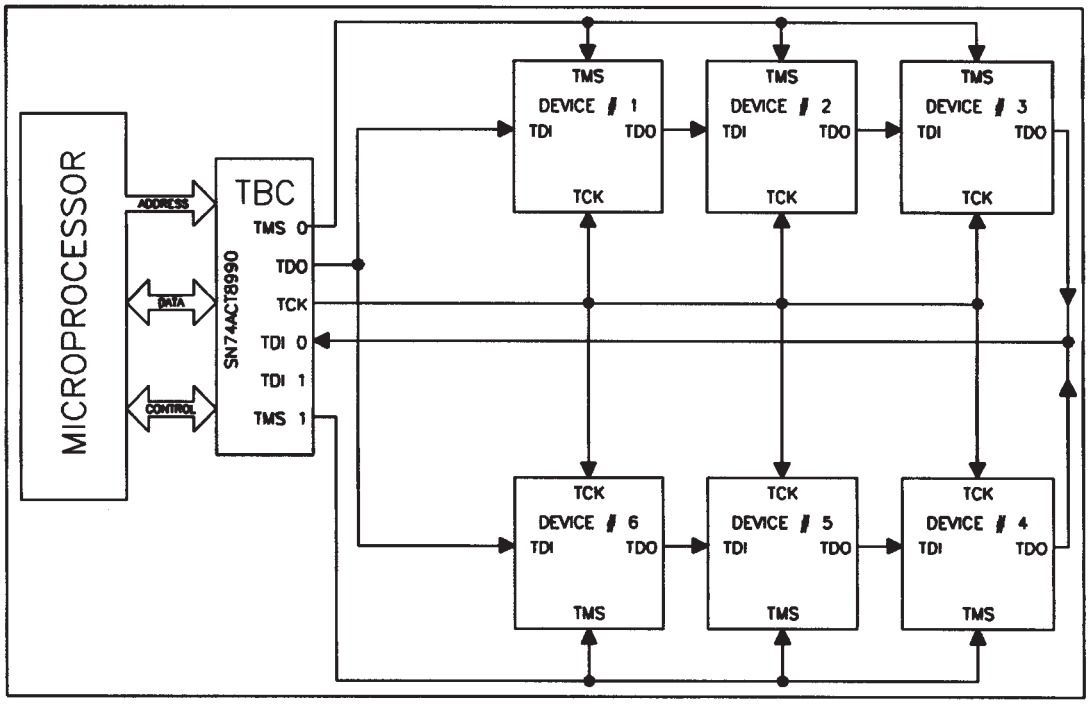


Figure 7. Connection of Two IEEE Std 1149.1 Test Buses to the TBC

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The TDO of several test systems can be connected in parallel and to a TDI input of the TBCs because they are active only during the shift operation (SHIFT-DR, SHIFT-IR) and are otherwise in a high-impedance state. If the test bus signals must be buffered (see Figure 8), the TDO output of the test system can no longer be in the high-impedance state. For this eventuality, two test data inputs (TDI0, TDI1) are available.

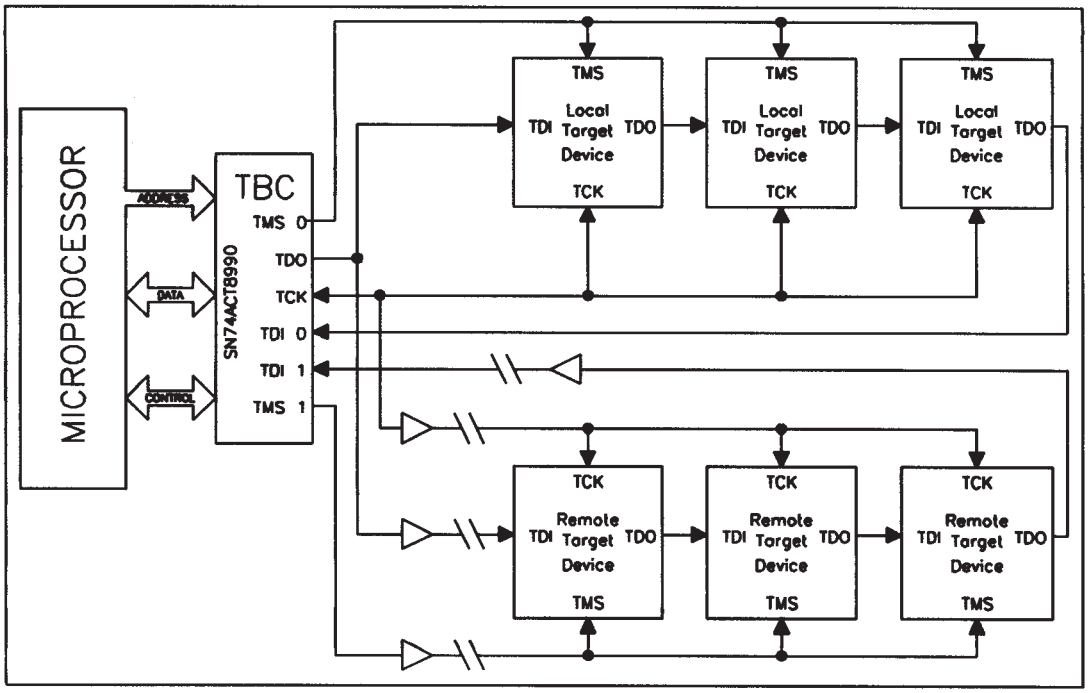


Figure 8. Connection of Several IEEE Std 1149.1 Test Buses to the TBC, With Buffering of the Test Bus Signal

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2.3 Architecture

Figure 9 shows the block diagram of the TBC, consisting of six functional blocks:

- Sequence block
- Serial block
- Event block
- Counter block
- Command block
- Host block

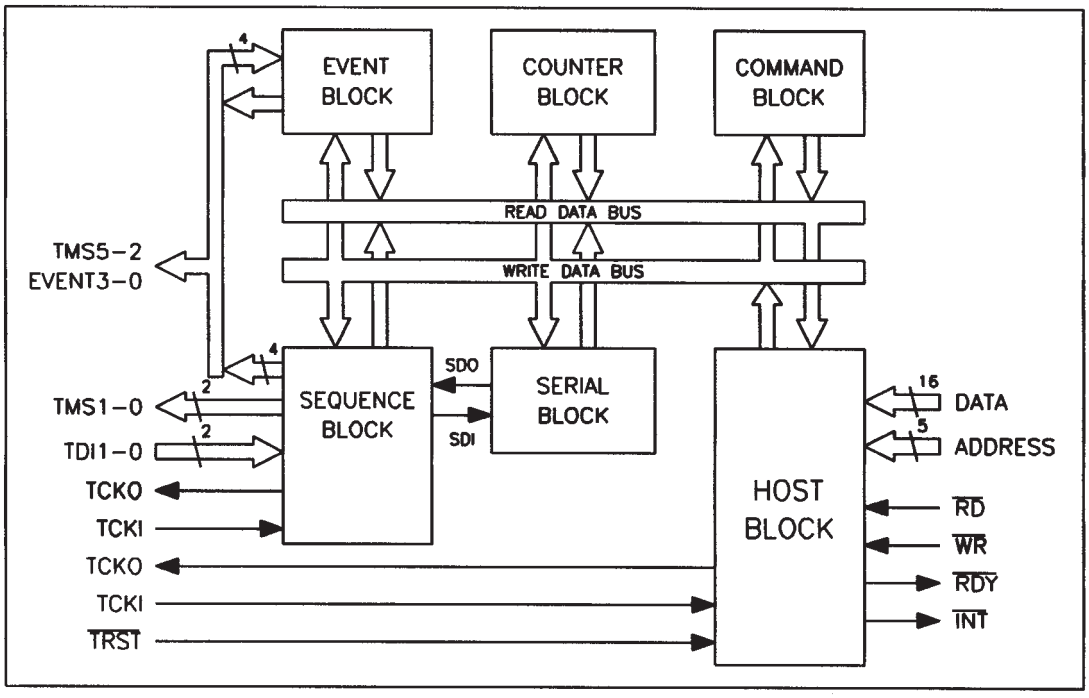


Figure 9. Block Diagram of TBC SN74ACT8990

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2.3.1 Sequence Block

The sequence block (see Figure 10) traces the test system through the status diagram (see Figure 21). During this process, the actual status of the test system is always known. The signals TMS, TDO, and TDI are generated by the sequence block according to IEEE Std 1149.1. During the SHIFT-DR and SHIFT-IR states, it uses the serial data out (SDO) data from the serial block to generate the TDO signal. Additionally, the sequence block transfers the TDI received data over the serial data in (SDI) line to the serial block.

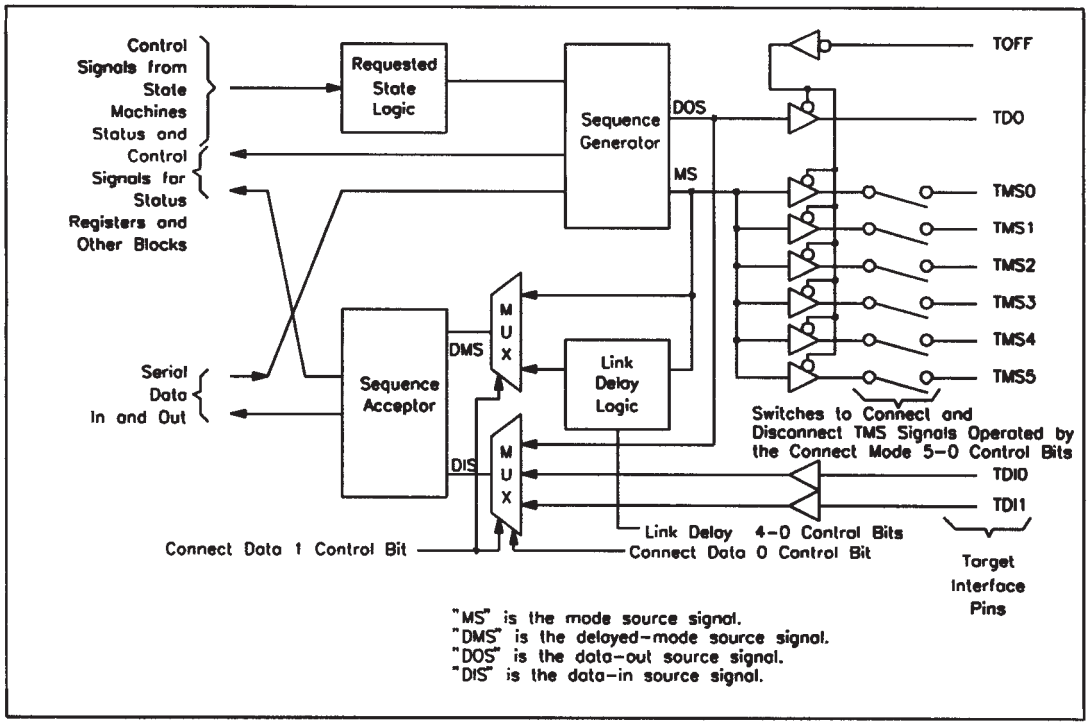


Figure 10. Sequence Block

These programming possibilities are important for the user:

- Choice of the TMS line to be used (TMS0–TMS5)
- Switching of all test bus lines into a high-resistance state
- Choice of the TDI line to be used
- Programmed delay of the test bus signals (link delay)

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The link-delay logic allows a simple way to account for flip-flop chains that are switched in the signals TDO, TDI, and TMS between the TBC and the test board (see Figure 11). These flip-flops can be used, for example, to synchronize signals coming from long lines from the TBC SN74ACT8990 to test boards.

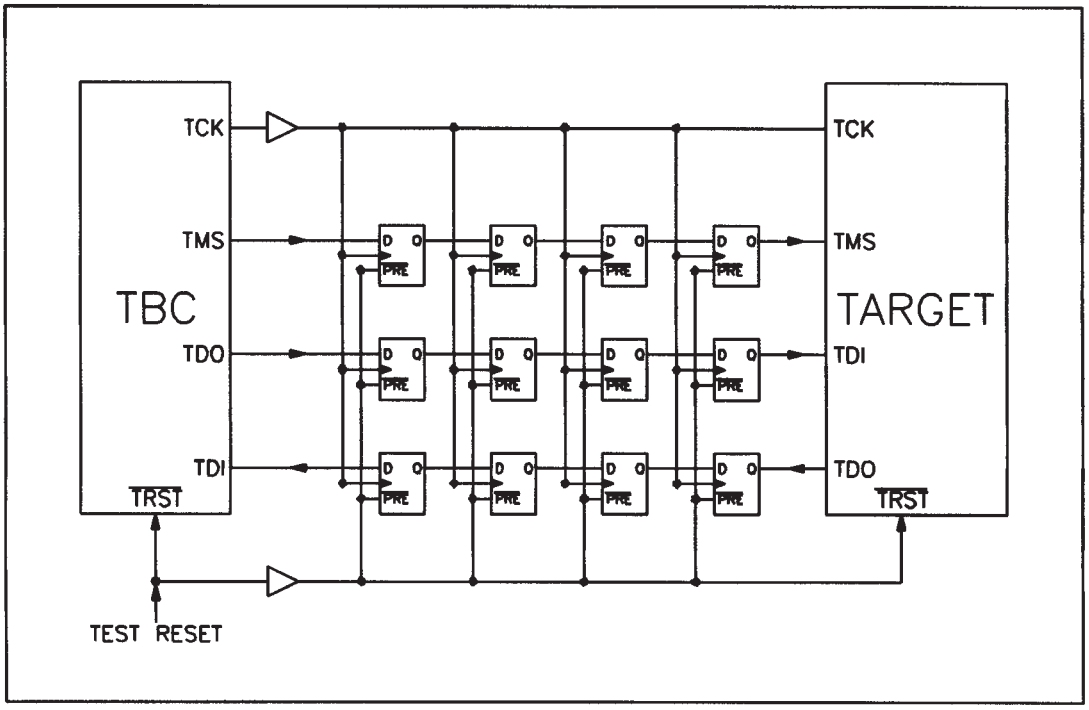


Figure 11. Link-Delay Logic

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2.3.2 Serial Block

An understanding of the operation of the serial block is an important requirement for the application of the TBC (see Figure 12). The serial block supplies the commands and data that are sent to the IEEE Std 1149.1-compatible test boards in the SHIFT-IR and SHIFT-DR states. In the same way, it collects the bits that are read back from the TDO output of the test board.

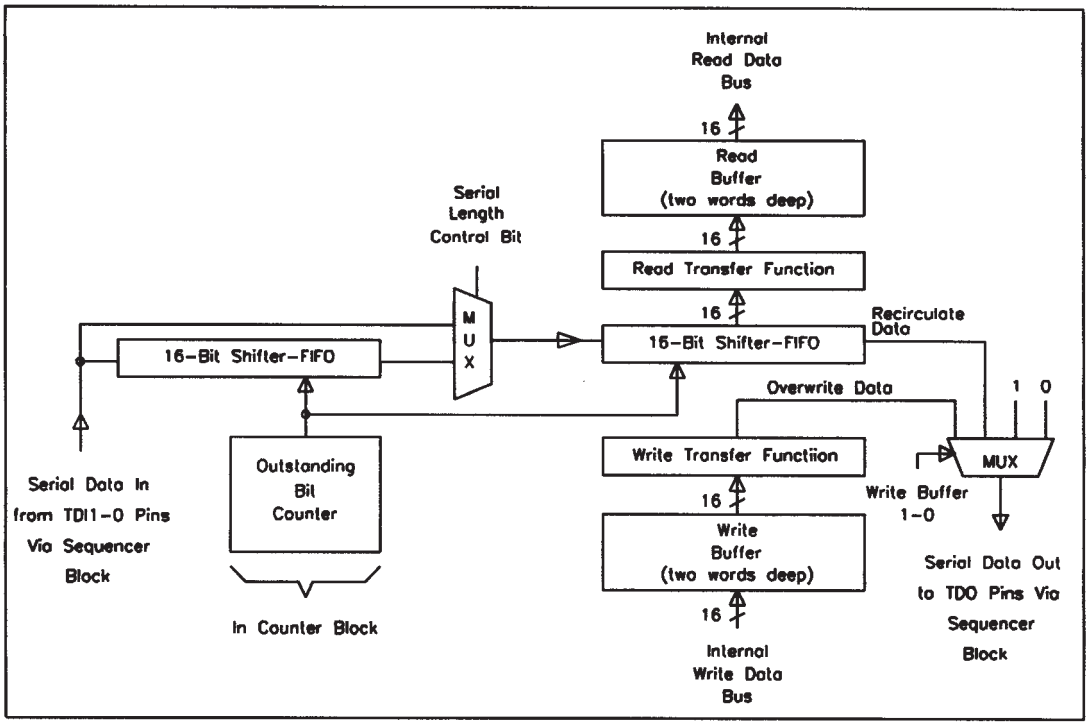


Figure 12. Serial Block

The SDO passes through the following sequence block to reach the test board as the TDO signal. The SDO signal can be chosen from the following via the multiplexer MUX2:

- SDO data derives from the WRITE BUFFER.
- Die SDO data derives from the SHIFTER-FIFO.
- SDO data consists only of ones.
- SDO data consists only of zeros.

The microprocessor writes data and commands into the WRITE BUFFER, which are sent to the test board via the SDO output. This WRITE BUFFER consists of two 16-bit registers. If the computer writes a 16-bit word into the first register, this register can be shifted out immediately via SDO. In the meantime, it is possible to write the next 16-bit word into the second register. The functional control of the register – that is, which register is transferring data and which can be addressed by the computer – is automatically performed by the TBC. The user must only request, via a status register, how many registers of the WRITE BUFFER are empty.

The write transfer function allows the user to choose whether the WRITE BUFFER should be shifted to the right, i.e., starting with the least significant bit (LSB), or to the left, i.e., beginning with the most significant bit (MSB).

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The TDI receiver data from the test board first pass through the sequence block, and then are shifted over the SDI into the SHIFTER-FIFO. The SHIFTER-FIFO is a shift register, whose length can be programmed to 16 bits or 32 bits with the help of the multiplexer MUX1. After reset, the SHIFTER-FIFO is loaded with 1s. All bits that leave the SHIFTER FIFO during a shift process are stored in the READ BUFFER.

The READ BUFFER, like the WRITE BUFFER, consists of two 16-bit registers. The operation is similar to that of the WRITE BUFFER; the only difference is that the data flow is in the reverse direction, i.e., the processor reads the data. The processor can determine via a register how many registers of the READ BUFFERs contain data. Because, as explained previously, the SHIFTER-FIFO is loaded with 1s on reset, the first bits that the computer reads from the READ BUFFER are 16 or 32 1s, depending on length to which the SHIFTER-FIFOs have been programmed. Only then will the first bits arrive from the TDI input.

The bit-by-bit transfer of data from the SHIFTER-FIFO to the READ BUFFER is performed by the read transfer function. It allows the user the following programs:

- Bits are transferred from the right into the WRITE BUFFER, with the first transmitted bit as LSB in the WRITE BUFFER.
- Bits are transmitted from the right into the WRITE BUFFER, with the last transmitted bit as LSB in the WRITE BUFFER.

2.3.3 Event Block

With the help of the event block, external events can be used to influence the test program, or transferred to the control computer from the event block as an interrupt. The operation of the event block is only of interest to those users who want to control the test program in accordance with events. If no such control is required, the following section can be skipped.

Figure 13 shows the block diagram of the event block inputs. Each input has its own event detector, which reacts on recognizing predetermined events. In addition, the two 16-bit backward counters (COUNTER20 and COUNTER21) are available to count events (see Figure 15). These counters also can be configured as two combined 16-bit counters (see Figure 16) and as a 32-bit counter (see Figure 17). The multiplexers of the event blocks allow the programming of a variety of different functions.

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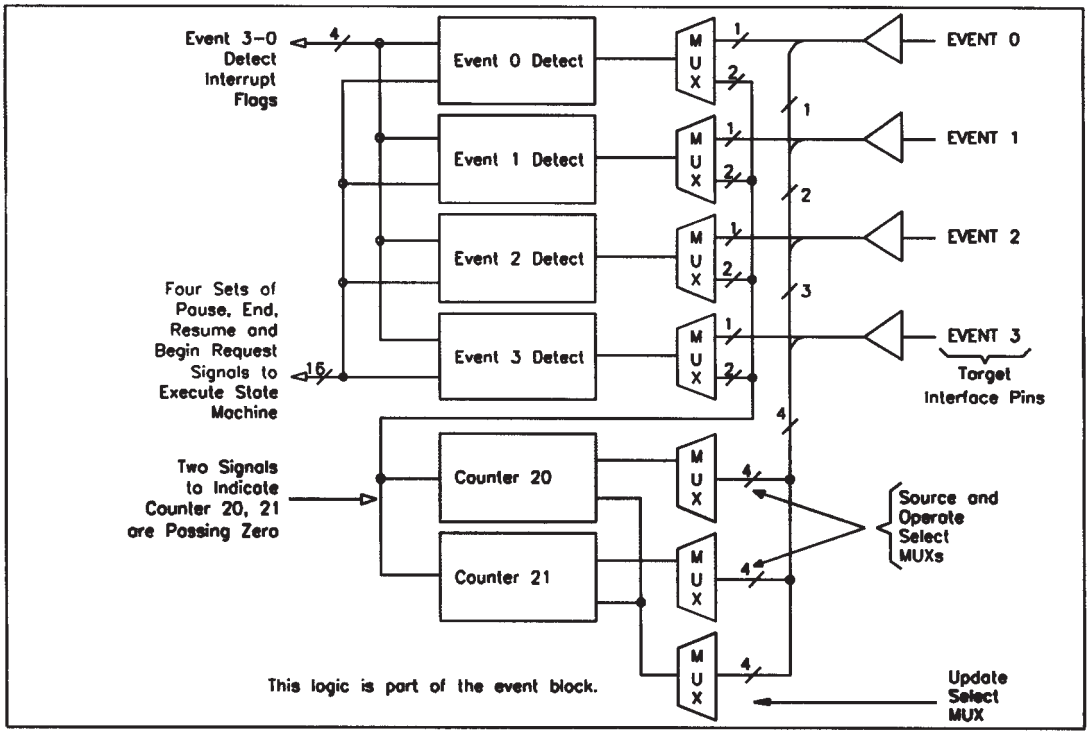


Figure 13. Inputs of the Event Block

For example, the EVENT0 input can be switched directly to the event detector by use of the multiplexer MUX 0. The EVENT DETECTOR 0 is programmed to recognize a particular event, e.g., the arrival of a rising pulse edge. It is, however, also possible to count events that occur at the EVENT0 input only with COUNTER20. After the counter of the COUNTER UPDATE register of the counter blocks (see Figure 18) has been loaded with the required value, on arrival of an event at the EVENT0 input it will be decremented by one. At the zero crossing of COUNTER20, the event detector activates its output.

The control computer has no direct access to COUNTER20 and COUNTER21; however, the COUNTER2 UPDATE register can be written to from the control computer. If COUNTER20 and COUNTER21 are loaded in parallel, this always takes place with the value in the COUNTER2 UPDATE register.

The output circuit of the event block is shown in Figure 14. For each output, two latches are available. One latch stores the required output level, the second latch allows the driver to switch into a high-resistance state and, therefore, to configure the connection as an input.

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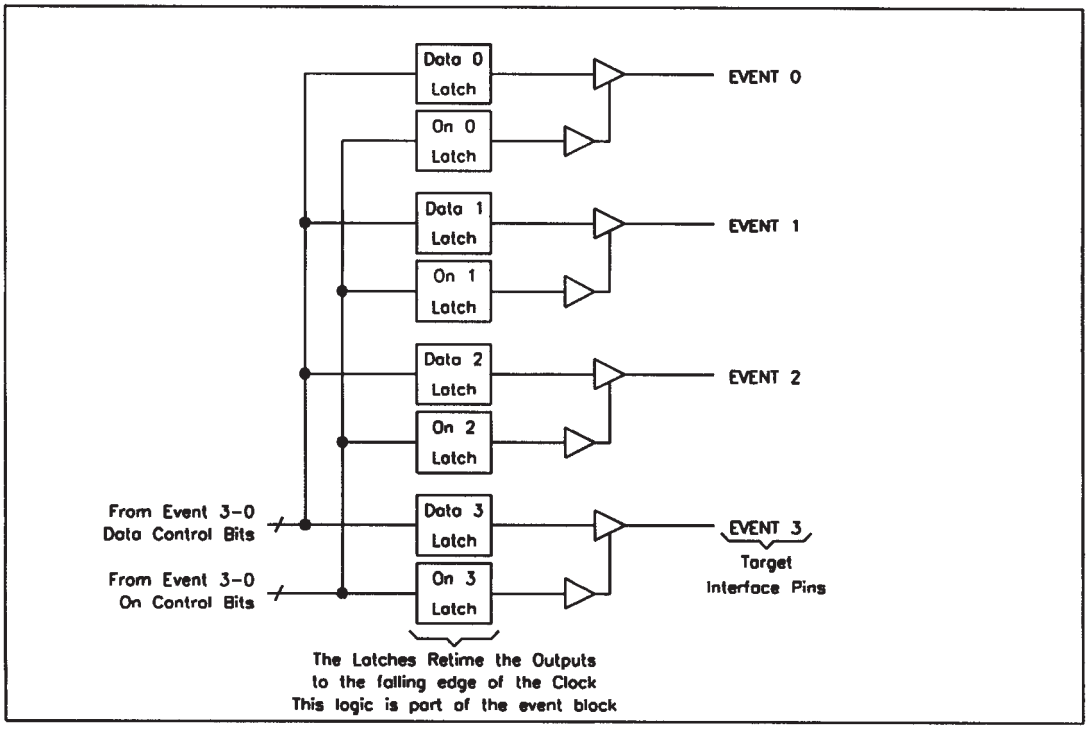


Figure 14. Outputs of the Event Block

COUNTER20 and COUNTER21 can be configured as follows:

- COUNTER20 and COUNTER21 work as separate 16-bit counters.
- COUNTER20 and COUNTER21 work as combined 16-bit counters. In this case, both counters are implemented as separate 16-bit counters, but COUNTER20 is loaded from the COUNTER UPDATE register until COUNTER21 has the first zero crossing. In this case, two events control the event recognition. For example, it can be programmed so that the first event must occur 55 times, and then the second event 12,345 times, before the event detector responds.
- Both counters are connected together to make a 32-bit counter (COUNTER2).

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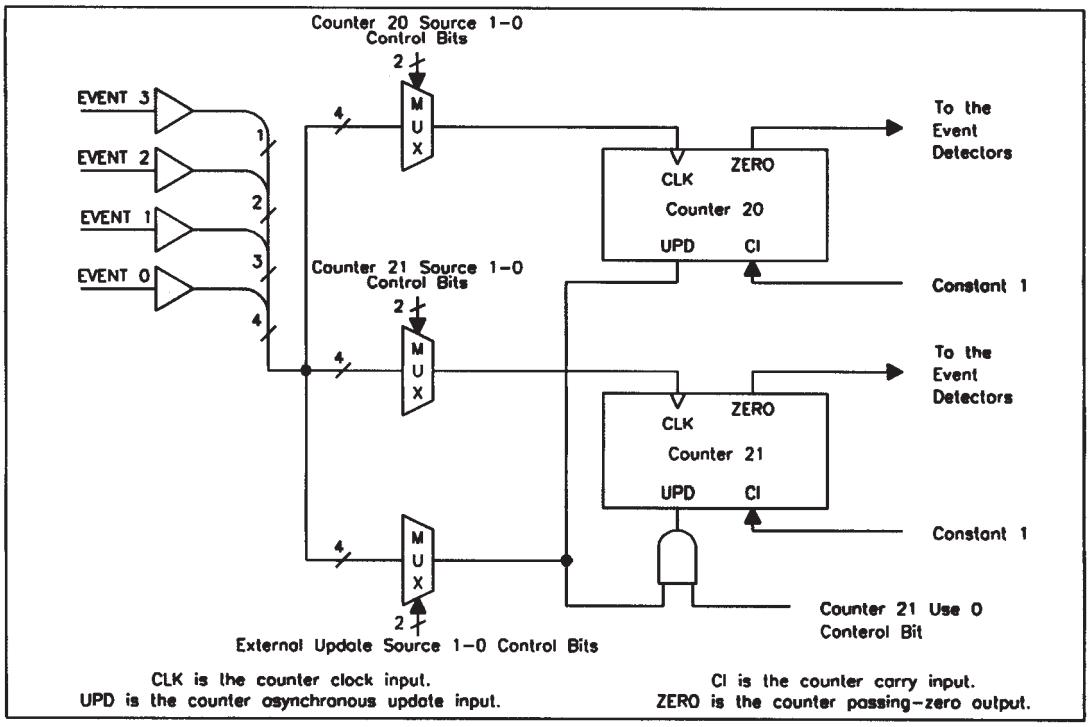


Figure 15. COUNTER20 and COUNTER21 Configured as Separate 16-Bit Counters

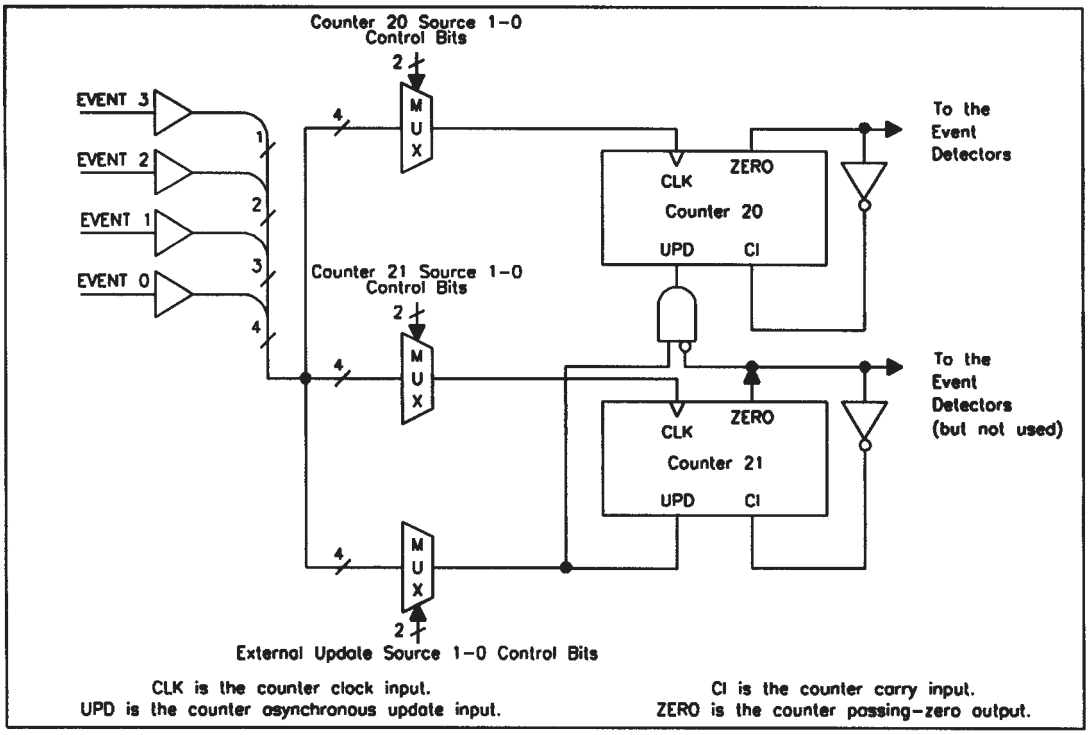


Figure 16. COUNTER20 and COUNTER21 Configured as Combined 16-Bit Counters

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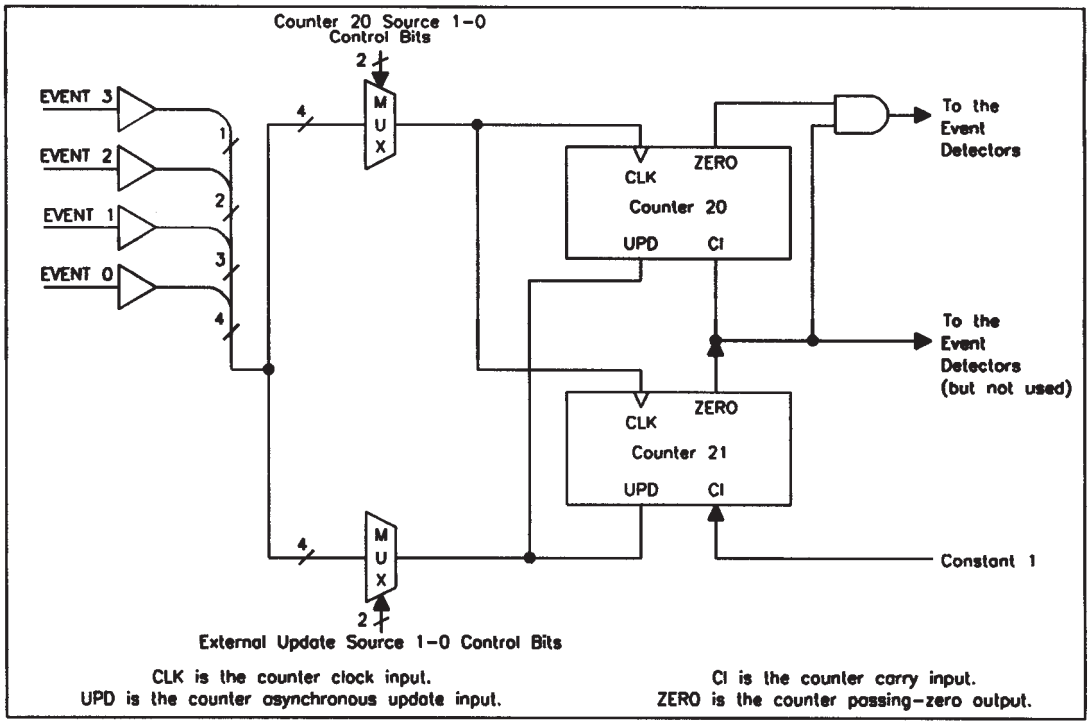


Figure 17. COUNTER20 and COUNTER21 Configured as One 32-Bit Counter (COUNTER2)

2.3.4 Counter Block

The part of the counter block (see Figure 18) that is relevant for the user consists of:

- COUNTER1 UPDATE register
- 32-bit backwards counter (COUNTER1)
- COUNTER1 CAPTURE register

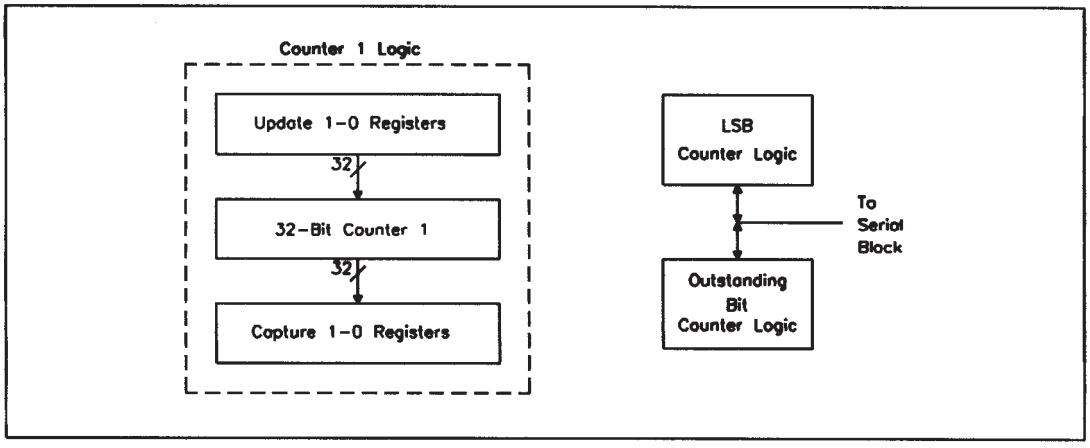


Figure 18. Counter Block

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COUNTER1 is used to count the SHIFT-DR, SHIFT-IR, and RUN-TEST/IDLE states. Also, it is possible to use it to count events. For this purpose, however, COUNTER20 and COUNTER21 are primarily available.

The control computer has no direct access to COUNTER1; it can only write into the COUNTER1 UPDATE register and read the COUNTER1 CAPTURE register. If COUNTER1 is loaded in parallel, this always is done with the value of the COUNTER1 UPDATE register. The actual count state of COUNTER1 can be copied parallel into the COUNTER1 CAPTURE register. From there, the actual count state can pass to the controlling computer.

2.3.5 Command Block

The command block contains two command registers (MAJOR COMMAND and MINOR COMMAND) (see Figure 19). In addition, all status registers are part of this block. The command block, with the command decode logic, controls the command process, with no intervention required by the user.

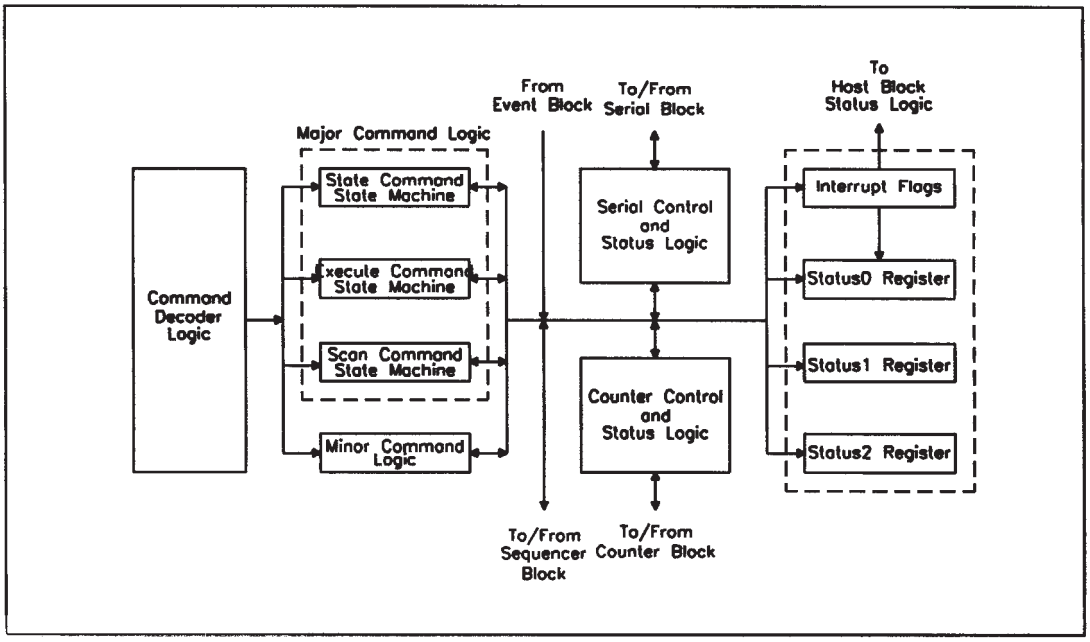


Figure 19. Command Block

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2.3.6 Host Block

The tasks of the host block include data-bus signal conditioning, decoding addresses and control lines, and conditioning interrupts for the control computer. In addition, the host block includes the reset logic and the buffering of the test pulse TCK. This block also performs its functions with no intervention required by the user.

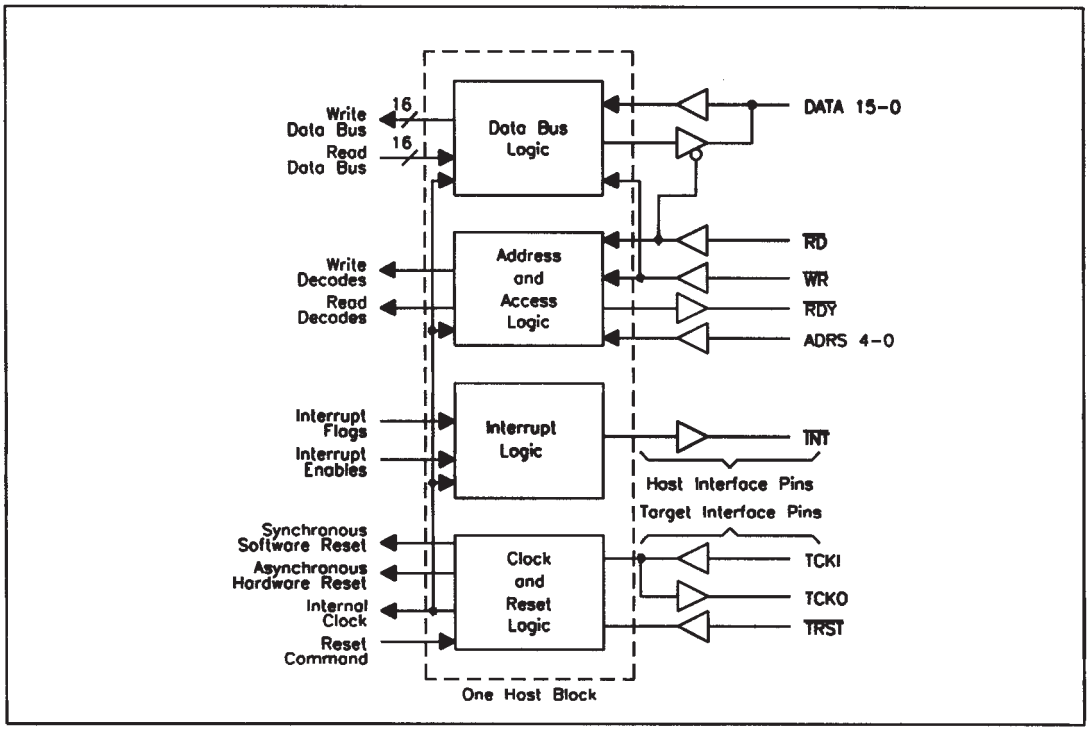


Figure 20. Host Block

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3 Programming

The control computer has access to the functions of the TBC using 24 registers, which are listed in Table 1. The ten control registers configure the TBC. The 32-bit command register is made up of a combination of the MAJOR COMMAND and MINOR COMMAND registers. With the MAJOR COMMAND register, presets of the commands are implemented, while the MINOR COMMAND register controls the execution; the commands are started, interrupted, or terminated. With the four COUNTER UPDATE and two CAPTURE registers, the counters of the event block and the counter block are controlled. The internal state of the TBC can be ascertained over three STATUS registers. The READ BUFFER and WRITE BUFFER are used to exchange data between the test board and the controlling computer.

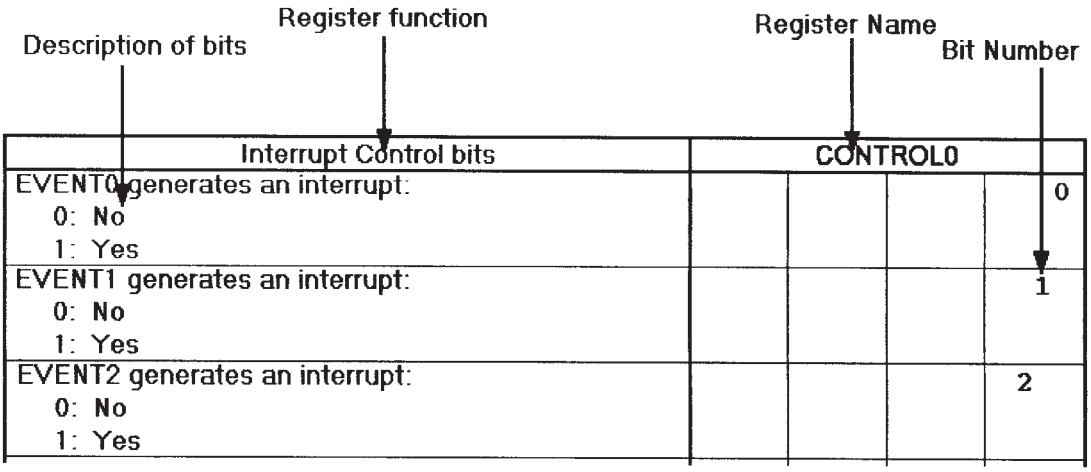
Table 1. Registers of TBC SN74ACT8990

ADR	Register Name	Application	Access
00	CONTROL0	Interrupt Control Bits	Read/Write
01	CONTROL1	Special Function for Production Test	Read/Write
02	CONTROL2	TMS0 .. TMS5 Connections	Read/Write
03	CONTROL3	TMS/EVENT Function, TDO on/off, TMS/TCK Data Format	Read/Write
04	CONTROL4	Delay, Data Format of TDI and TDO pins	Read/Write
05	CONTROL5	EVENT pins Data Output and Direction	Read/Write
06	CONTROL6	Event Choice of EVENT0/1 Inputs	Read/Write
07	CONTROL7	Event Choice of EVENT2/3 Inputs	Read/Write
08	CONTROL8	COUNTER1 Control	Read/Write
09	CONTROL9	COUNTER2 Control	Read/Write
0A	MINOR COMMAND	Replace Interrupt Flag Bits, Control of Test Run, Read Status, load counters and count, Software RESET	Read/Write
0B	MAJOR COMMAND	STATE Command, EXECUTE Command, SCAN Command	Read/Write
0C	COUNTER1 UPDATE0	COUNTER1 Lower Value Word	Read/Write
0D	COUNTER1 UPDATE1	COUNTER1 Higher Value Word	Read/Write
0E	COUNTER2 UPDATE0	COUNTER2 Lower Value Word or COUNTER20	Read/Write
0F	COUNTER2 UPDATE1	COUNTER2 Higher Value Words or COUNTER21	Read/Write
10	STATUS0	Internal States	Read only
11	STATUS1	External Signals and Requests	Read only
12	STATUS2	State of test board and Buffer	Read only
13	STATUS3	not used	Read only
14	CAPTURE0	COUNTER1 Lower Value Word	Read only
15	CAPTURE1	COUNTER1 Higher Value Word	Read only
16	READ BUFFER	Input Buffer for TDI	Read only
17	WRITE BUFFER	Output Buffer for TDO	Write only

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3.1 Registers

In this section, the individual bits of all registers of the TBC are presented in tables. The table heading includes the register name and a short description of the register function. Within the tables, all bits are described individually. The bit numbers are assembled in groups of four bits each to simplify the presentation in hexadecimal form.



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CONTROL0

Interrupt Control bits	CONTROL0			
EVENT0 generates an Interrupt: 0: No 1: Yes				0
EVENT1 generates an Interrupt: 0: No 1: Yes				1
EVENT2 generates an Interrupt: 0: No 1: Yes				2
EVENT3 generates an Interrupt: 0: No 1: Yes				3
The COUNTER1 EXECUTE Flag generates an Interrupt: 0: No 1: Yes			4	
The COUNTER1 SCAN Flag generates an Interrupt: 0: No 1: Yes			5	
NULL			76	
The SUSPEND Flag generates an Interrupt: 0: No 1: Yes		8		
The END Flag generates an Interrupt: 0: No 1: Yes		9		
The RESUME Flag generates an Interrupt: 0: No 1: Yes		A		
The BEGIN SCAN Flag generates an Interrupt: 0: No 1: Yes		B		
The BUFFER ERROR Flag generates an Interrupt: 0: No 1: Yes	C			
The BUFFER READY Flag generates an Interrupt: 0: No 1: Yes	D			
The ABORT Flag generates an Interrupt: 0: No 1: Yes	E			
The FINISH Flag generates an Interrupt: 0: No 1: Yes	F			

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CONTROL1

Special Functions for Production Test	CONTROL1			
Each Bit: 0: Normal operation 1: Test operation for Production Test				3210
Not used			7554	
Each Bit: 0: Normal operation 1: Test operation for Production Test	C	BA98		
Not used	FED			

When using the SN74ACT8990 as controller of a test bus according to IEEE Std 1149.1, all bits of these registers must be set to zero by the user. With the help of these registers, the manufacturer can switch various parts of the component into test operation during production test. This allows a comprehensive, but simple, functional examination of the internal circuitry.

CONTROL2

TMS0 .. TMS5 Connections	CONTROL2			
TMS0 is connected with internal TMS source: 0: No 1: Yes				0
TMS1 is connected with internal TMS source: 0: No 1: Yes				1
TMS2 is connected with internal TMS source: 0: No 1: Yes				2
TMS3 is connected with internal TMS source: 0: No 1: Yes				3
TMS4 is connected with internal TMS source: 0: No 1: Yes			4	
TMS5 is connected with internal TMS source: 0: No 1: Yes			5	
NULL	FEDC	BA98	76	

The component generates a TMS signal internally. This signal can be extracted at the pins TMS0–TMS5. All TMS pins that are not connected to the internal TMS source remain in a static state.

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CONTROL3

Function of the TMS/EVENT pins, Data Format of the TMS and TCK pins	CONTROL3			
TMS2/EVENT0: 0: EVENT Input or Output 1: TMS2 Output				0
TMS3/EVENT1: 0: EVENT Input or Output 1: TMS3 Output				1
TMS4/EVENT2: 0: EVENT Input or Output 1: TMS4 Output				2
TMS5/EVENT3: 0: EVENT Input or Output 1: TMS5 Output				3
TCKO on/off: 0: TCKO Output is switched on 1: TCKO Output is switched off			4	
TDO on/off: 0: TDO Output is switched on 1: TDO Output is switched off			5	
TMS on/off: 0: all TMS Outputs are switched on 1: all TMS Outputs are switched off			6	
EVENT on/off: 0: all EVENT Outputs are switched on 1: all EVENT Outputs are switched off			7	
Output Bit Format: 0000: for operation to IEEE 1149.1 else: for operation with special TI components		BA98		
TCKO Output signal if TCKO Bit D is set to 1: 0: static 0-signal 1: static 1-signal	C			
TCKO Data Format: 0: TCKO is connected with internal TCK source 1: static signal	D			
NULL	FE			

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CONTROL4

Delay, Data Formats of TDI and TDO Pins	CONTROL4			
Delay: 00000 to 11111: with these bits, the LINK DELAY Registers can be set to a delay from 0 to 31 bits length.			4	3210
SHIFTER-FIFO Length: 0: 16 bits 1: 32 bits			5	
TDI Selection: 00, 01: The internal TDO signal is the source for the internal signal TDI 10: The TDI0 Input is the source for the internal signal TDI 11: The TDI1 Input is the source for the internal signal TDI			76	
TDO Sending Data: 00: TDO sends 0's 01: TDO sends 1's 10: TDO sends data of the SHIFTER-FIFO 11: TDO sends data of the WRITE BUFFER		98		
READ BUFFER on/off: 0: The received data is ignored after flowing through the SHIFTER-FIFO 1: The received data is transferred to the READ BUFFER after flowing through the SHIFTER-FIFO		A		
Transfer Format: 0: At data transfer, the LSB is always sent/received first 1: At data transfer, the MSB is always sent/received first		B		
TDI Data Transfer: 0: TDI Data Transfer on leading edge 1: TDI Data Transfer on trailing edge	C			
EVENT Data Transfer: 0: EVENT Data Transfer on leading edge 1: EVENT Data Transfer on trailing edge	D			
NULL	FE			

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CONTROL5

EVENT Pins Output Data and Direction of Flow	CONTROL5			
EVENT0 Output Data: 0: 0-Level 1: 1-Level				0
EVENT1 Output Data: 0: 0-Level 1: 1-Level				1
EVENT2 Output Data: 0: 0-Level 1: 1-Level				2
EVENT3 Output Data: 0: 0-Level 1: 1-Level				3
NULL			7654	
EVENT0 Data Flow Direction: 0: EVENT0 is an input 1: EVENT0 is an output		8		
EVENT1 Data Flow Direction: 0: EVENT1 is an input 1: EVENT1 is an output		9		
EVENT2 Data Flow Direction: 0: EVENT2 is an input 1: EVENT2 is an output		A		
EVENT3 Data Flow Direction: 0: EVENT3 is an input 1: EVENT3 is an output		B		
NULL	FEDC			

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CONTROL6

Event Choice at the EVENT0/1 Inputs	CONTROL6			
EVENT0 sets the SUSPEND REQUEST Flag: 0: No 1: Yes				0
EVENT0 sets the END REQUEST Flag: 0: No 1: Yes				1
EVENT0 sets the RESUME REQUEST Flag: 0: No 1: Yes				2
EVENT0 sets the BEGIN REQUEST Flag: 0: No 1: Yes				3
EVENT0 is synchronous or asynchronous: 0: The recognition of the EVENT0 is asynchronous 1: The recognition of the EVENT0 is synchronous			4	
EVENT0 Masking: 0: The recognition of the EVENT0 always occurs 1: No EVENT0 recognition during CAPTURE-DR, SHIFT-DR, EXIT1-DR, PAUSE-DR, EXIT2-DR, CAPTURE-IR, SHIFT-IR, EXIT1-IR, PAUSE-IR, EXIT2-IR			5	
Asynchronous EVENT0 recognition: 00: Trailing Edge at Input EVENT0 01: Leading Edge at Input EVENT0 10: Zero passing of COUNTER20 11: Zero passing of COUNTER21 Synchronous EVENT0 recognition of 2 successive TCK edges: 00: 1-Level --> 0-Level 01: 0-Level --> 1-Level 10: 0-Level --> 0-Level 11: 1-Level --> 1-Level			76	
EVENT1 sets the SUSPEND REQUEST Flag: 0: No 1: Yes		8		
EVENT1 sets the END REQUEST Flag: 0: No 1: Yes		9		
EVENT1 sets the RESUME REQUEST Flag: 0: No 1: Yes		A		
EVENT1 sets the BEGIN REQUEST Flag: 0: No 1: Yes		B		
EVENT1 is synchronous or asynchronous: 0: The recognition of the EVENT1 is asynchronous 1: The recognition of the EVENT1 is synchronous	C			
EVENT1 Masking: 0: The recognition of the EVENT1 always occurs 1: No EVENT1 recognition during CAPTURE-DR, SHIFT-DR, EXIT1-DR, PAUSE-DR, EXIT2-DR, CAPTURE-IR, SHIFT-IR, EXIT1-IR, PAUSE-IR, EXIT2-IR	D			

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CONTROL6 (Continued)

Asynchronous EVENT1 recognition: 00: Trailing Edge at input EVENT1 01: Leading Edge at input EVENT1 10: Zero passing of COUNTER20 11: Zero passing of COUNTER21 Synchronous EVENT1 recognition of 2 successive TCK edges: 00: 1-Level --> 0-Level 01: 0-Level --> 1-Level 10: 0-Level --> 0-Level 11: 1-Level --> 1-Level	FE			

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CONTROL7

Event Choice of the EVENT2/3 Inputs	CONTROL7			
EVENT2 sets the SUSPEND REQUEST Flag: 0: No 1: Yes				0
EVENT2 sets the END REQUEST Flag: 0: No 1: Yes				1
EVENT2 sets the RESUME REQUEST Flag: 0: No 1: Yes				2
EVENT2 sets the BEGIN REQUEST Flag: 0: No 1: Yes				3
EVENT2 is synchronous or asynchronous: 0: The recognition of the EVENT2 is asynchronous 1: The recognition of the EVENT2 is synchronous			4	
EVENT2 Masking: 0: The recognition of the EVENT2 always occurs 1: No EVENT2 recognition during CAPTURE-DR, SHIFT-DR, EXIT1-DR, PAUSE-DR, EXIT2-DR, CAPTURE-IR, SHIFT-IR, EXIT1-IR, PAUSE-IR, EXIT2-IR			5	
Asynchronous EVENT2 recognition: 00: Trailing Edge at input EVENT2 01: Leading Edge at input EVENT2 10: Zero passing of COUNTER20 11: Zero passing of COUNTER21 Synchronous EVENT2 recognition of 2 successive TCK edges: 00: 1-Level --> 0-Level 01: 0-Level --> 1-Level 10: 0-Level --> 0-Level 11: 1-Level --> 1-Level			76	
EVENT3 sets the SUSPEND REQUEST Flag: 0: No 1: Yes		8		
EVENT3 sets the END REQUEST Flag: 0: No 1: Yes		9		
EVENT3 sets the RESUME REQUEST Flag: 0: No 1: Yes		A		
EVENT3 sets the BEGIN REQUEST Flag: 0: No 1: Yes		B		
EVENT3 is synchronous or asynchronous: 0: The recognition of the EVENT3 is asynchronous 1: The recognition of the EVENT3 is synchronous	C			
EVENT3 Masking: 0: The recognition of the EVENT3 always occurs 1: No EVENT3 recognition during CAPTURE-DR, SHIFT-DR, EXIT1-DR, PAUSE-DR, EXIT2-DR, CAPTURE-IR, SHIFT-IR, EXIT1-IR, PAUSE-IR, EXIT2-IR	D			

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CONTROL7 (Continued)

asynchronous EVENT3 recognition: 00: Trailing Edge at input EVENT3 01: Leading Edge at input EVENT3 10: Zero passing of COUNTER20 11: Zero passing of COUNTER21 synchronous EVENT3 recognition of 2 successive TCK edges: 00: 1-Level --> 0-Level 01: 0-Level --> 1-Level 10: 0-Level --> 0-Level 11: 1-Level --> 1-Level	FE			

CONTROL8

COUNTER1 Control	CONTROL8			
COUNTER1 sets the SUSPEND REQUEST Flag during zero passing: 0: No 1: Yes				0
COUNTER1 sets the END REQUEST Flag during zero passing: 0: No 1: Yes				1
COUNTER1 is loaded by the COUNTER1 UPDATE Register during zero passing: 0: No 1: Yes				2
COUNTER 1 counts 000, 001: never. 010: the clock edge of TCK in RUN-TEST/IDLE state during an EXECUTE command. 011: always when an EXECUTE command is executed. 100, 101: with the EVENT DETECTOR, which is selected with Bits 7 and 6. 110: if an 0-Level exists at the EVENT PIN selected by Bits 7 and 6. 111: if an 1-Level exits at the EVENT PIN selected by Bits 7 and 6.			54	3
COUNTER1 reacts on 00: EVENT DETECTOR0 or the input EVENT0 01: EVENT DETECTOR1 or the input EVENT1 10: EVENT DETECTOR2 or the input EVENT2 11: EVENT DETECTOR3 or the input EVENT3 if the Bits 5 and 4 have the value 100,101,110 or 111. In all other cases the value of these bits is without significance.			76	
not used	FEDC	BA98		

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CONTROL9

COUNTER2 Control	CONTROL9			
COUNTER2 is loaded with an 000: 0-Level at the EVENT0 Input. 001: 1-Level at the EVENT0 Input. 010: 0-Level at the EVENT1 Input. 011: 1-Level at the EVENT1 Input. 100: 0-Level at the EVENT2 Input. 101: 1-Level at the EVENT2 Input. 110: 0-Level at the EVENT3 Input. 111: 1-Level at the EVENT3 Input.				210
COUNTER20 is loaded by the COUNTER2 UPDATE0 Register: 0: Yes 1: No				3
COUNTER20 is loaded during zero passing: 0: No 1: Yes			4	
COUNTER20 counts 000: if there is a trailing edge at the input EVENT0. 001: if there is a leading edge at the input EVENT0. 010: if there is a trailing edge at the input EVENT1. 011: if there is a leading edge at the input EVENT1. 100: if there is a trailing edge at the input EVENT2. 101: if there is a leading edge at the input EVENT2. 110: if there is a trailing edge at the input EVENT3. 111: if there is a leading edge at the input EVENT3.			765	
COUNTER2 can be loaded by an 0: asynchronous signal at the EVENT input. 1: synchronous signal at the EVENT input.		8		
COUNTER20 and COUNTER21 work as 00: separate 16-Bit counters; only COUNTER20 can be loaded by an asynchronous input signal. 01: separate 16-Bit counters; both counters can be loaded by an asynchronous input signal. 10: two tied 16-Bit counter 11: one 32-Bit counter. This counter can be loaded by an asynchronous input signal.		A9		
COUNTER21 is loaded by the COUNTER2 UPDATE1 Register: 0: Yes 1: No		B		
COUNTER21 is loaded at zero passing: 0: No 1: Yes	C			
COUNTER21 counts 000: if there is a trailing edge at the input EVENT0. 001: if there is a leading edge at the input EVENT0. 010: if there is a trailing edge at the input EVENT1. 011: if there is a leading edge at the input EVENT1. 100: if there is a trailing edge at the input EVENT2. 101: if there is a leading edge at the input EVENT2. 110: if there is a trailing edge at the input EVENT3. 111: if there is a leading edge at the input EVENT3.	FED			

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MINOR COMMAND

Replace Interrupt Flag Bit 8 to 15	MINOR COMMAND			
Set/Reset the Interrupt Flag Bit 8: 0: No 1: Yes				0
Set/Reset the Interrupt Flag Bit 9: 0: No 1: Yes				1
Set/Reset the Interrupt Flag Bit 10: 0: No 1: Yes				2
Set/Reset the Interrupt Flag Bit 11: 0: No 1: Yes				3
Set/Reset the Interrupt Flag Bit 12: 0: No 1: Yes			4	
Set/Reset the Interrupt Flag Bit 13: 0: No 1: Yes			5	
Set/Reset the Interrupt Flag Bit 14: 0: No 1: Yes			6	
Set/Reset the Interrupt Flag Bit 15: 0: No 1: Yes			7	
NULL		BA98		
0001: Reset the Interrupt Flag Bits 8 to 15 0011: Set the Interrupt Flag Bits 8 to 15	FEDC			

Replace Interrupt Flag Bits 0 to 5	MINOR COMMAND			
Set/Reset the Interrupt Flag Bit 0: 0: No 1: Yes				0
Set/Reset the Interrupt Flag Bit 1: 0: No 1: Yes				1
Set/Reset the Interrupt Flag Bit 2: 0: No 1: Yes				2
Set/Reset the Interrupt Flag Bit 3: 0: No 1: Yes				3
Set/Reset the Interrupt Flag Bit 4: 0: No 1: Yes			4	
Set/Reset the Interrupt Flag Bit 5: 0: No 1: Yes			5	
NULL		BA98	76	
0000: Reset the Interrupt Flag Bits 0 to 5 0010: Set the Interrupt Flag Bits 0 to 5	FEDC			

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Controlling the Test Operation	MINOR COMMAND			
Set/Reset the SUSPEND REQUEST Flag: 0: No 1: Yes				0
Set/Reset the END REQUEST Flag: 0: No 1: Yes				1
Set/Reset the RESUME REQUEST Flag: 0: No 1: Yes				2
Set/Reset the BEGIN REQUEST Flag: 0: No 1: Yes				3
NULL			4	
Enable start of an EXECUTE Command: 0: No 1: Yes			5	
Canceling a SCAN or EXECUTE Command: 0: No 1: Yes			6	
Enable start of a STATE, SCAN or EXECUTE Command: 0: No 1: Yes			7	
NULL		BA98		
0100: Bits 0 to 3 reset the Flags 0101: Bits 0 to 3 set the Flags	FEDC			

Read status, load counter, and count	MINOR COMMAND			
Load COUNTER1 UPDATE into COUNTER1: 0: No 1: Yes				0
Count COUNTER1: 0: No 1: Yes				1
Load COUNTER1 into the CAPTURE status register: 0: No 1: Yes				2
NULL				3
Load COUNTER2 UPDATE0 into COUNTER20: 0: No 1: Yes			4	
Load COUNTER2 UPDATE1 into COUNTER21: 0: No 1: Yes			5	
Refresh STATUS0, STATUS1 and STATUS2 registers: 0: No 1: Yes			6	
NULL		BA98	7	
0110: Read status, load counter, and count	FEDC			

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Software RESET	MINOR COMMAND			
Reset complete 'ACT8990: 0: No 1: Yes				0
Reset interrupt flags: 0: No 1: Yes				1
Reset READ BUFFER and WRITE BUFFER: 0: No 1: Yes				2
Reset REQUEST flags: 0: No 1: Yes				3
NULL		BA98	7654	
0111: Reset the whole component	FEDC			

MAJOR COMMAND

STATE Command	MAJOR COMMAND			
New state after executing the command: 000, 001: TEST-LOGIC-RESET 010, 011: RUN-TEST/IDLE 100: SHIFT-DR 101: SHIFT-IR 110: PAUSE-DR 111: PAUSE-IR				210
NULL		BA98	7654	3
0001: STATE Command	FEDC			

The STATE command is used to set the test board into a new state. There is no other activity during that command:

- Event recognition, and all counters, are ignored.
- COUNTER1 is ignored and does not count, even if the RUN-TEST/IDLE state occurs.
- Data buffer is ignored and remains unchanged, even if a SHIFT-DR state or a SHIFT-IR state occurs.
- SHIFTER-FIFO is ignored and remains unchanged, even if a SHIFT-DR state or a SHIFT-IR state occurs.
- Execution of the command cannot be suspended.
- To reach the new state, only the temporary states SELECT-DR-SCAN, CAPTURE-DR, EXIT1-DR, UPDATE-DR, SELECT-IR-SCAN, CAPTURE-IR, EXIT1-IR, and UPDATE-IR are used. The sole exception is the start of the TEST-LOGIC-RESET state. In this case, first change to RUN-TEST/IDLE state. Only then will this procedure lead, exclusively, via temporary states, to the new state.

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EXECUTE Command	MAJOR COMMAND			
New state after execution of command: 000, 001: TEST-LOGIC-RESET 010, 011: RUN-TEST/IDLE 100: SHIFT-DR 101: SHIFT-IR 110: PAUSE-DR 111: PAUSE-IR				210
States for execution and suspension of commands: 0: Execution of command in RUN-TEST/IDLE state and suspension in PAUSE-DR state. 1: Execution of command in RUN-TEST/IDLE and suspension of the execution of command in PAUSE-IR state.				3
Suspension or Cancellation of Commands: 00, 01: During zero passing of COUNTER1 the execution of command is suspended or cancelled. 10: The execution of the command is finished after the EXECUTE state has been passed through once. COUNTER1 is not used. 11: The execution of the Command is cancelled after the EXECUTE state has been passed once. COUNTER1 is not used.			54	
Starting and executing the commands: 00, 01: The selected new state is controlled directly. This case corresponds to the STATE COMMAND, but can not be controlled by events. 10: The execution of the command is suspended immediately after the start (SLEEP STATE) 11: The execution of command begins with it's start			76	
SUSPEND and RESUME Flag: 0: If the execution of command is suspended, then the SUSPEND flag is resetted, if the execution of the command is resumed, then the RESUME flag is Reset. 1: If the execution of the command is suspended or resumed, then the SUSPEND flag as well as the RESUME flag are reset.		8		
NULL		BA9		
0010: EXECUTE command	FEDC			

Using the EXECUTE command, a defined number of RUN-TEST/IDLE cycles can be executed. The execution of this command can be suspended and resumed.

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SCAN Command	MAJOR COMMAND			
New state after executing the command: 000, 001: TEST-LOGIC-RESET 010, 011: RUN-TEST/IDLE 100: SHIFT-DR 101: SHIFT-IR 110: PAUSE-DR 111: PAUSE-IR				210
States for execution and suspension of commands: 0: Execution of command in SHIFT-DR state and suspension of execution of command in PAUSE-DR state. 1: Execution of command in SHIFT-IR state and suspension of execution of command in PAUSE-IR state.				3
Suspension and cancellation of commands: 00, 01: During zero passing of COUNTER1 the execution of command is suspended or cancelled. 10: The execution of the command is finished, after the EXECUTE state has been passed through once. COUNTER1 is not used. 11: The execution of the command is cancelled, after the EXECUTE state has been passed through once. COUNTER1 is not used.			54	
NULL		BA98	76	
0011: SCAN Command	FEDC			

Using the SCAN command, a defined number of SHIFT-DR cycles or SHIFT-IR cycles can be executed. The execution of this command can be suspended and resumed.

COUNTER1 UPDATE0

COUNTER1 Lower Value Word	COUNTER1 UPDATE0			
The lower value 16-Bit word of COUNTER1 can be loaded with the contents of this register.	FEDC	BA98	7654	3210

COUNTER1 UPDATE1

COUNTER1 Higher Value Word	COUNTER1 UPDATE1			
The higher value 16-Bit word of COUNTER1 can be loaded with the contents of this register.	FEDC	BA98	7654	3210

The 32-bit COUNTER1 is used for counting the numbers of shift operations with the SCAN command in the SHIFT-DR state and the SHIFT-IR state. Additionally, it is used for counting the RUN-TEST/IDLE cycles during an EXECUTE command. COUNTER1 also is able to count events.

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COUNTER2 UPDATE0

COUNTER2 Lower Value Word or COUNTER20	COUNTER2 UPDATE0			
The lower value 16-Bit Word of COUNTER2 or of COUNTER20 can be loaded with the contents of this register.	FEDC	BA98	7654	3210

COUNTER2 UPDATE1

COUNTER2 Higher Value Word or COUNTER20	COUNTER2 UPDATE1			
The higher value 16-Bit word of COUNTER2 or of COUNTER21 can be loaded with the contents of this register	FEDC	BA98	7654	3210

Both COUNTER20 and COUNTER21 can be used as two independent 16-bit counters (see Figure 15), two combined 16-bit counters (see Figure 16), or as one 32-bit counter (COUNTER2) (see Figure 17). In both cases, they can be used for counting events that occur at the EVENT0–EVENT3 inputs.

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STATUS0

Internal States	STATUS0			
An event occurred at the EVENT DETECTOR0: 0: No 1: Yes				0
An event occurred at the EVENT DETECTOR1: 0: No 1: Yes				1
An event occurred at the EVENT DETECTOR2: 0: No 1: Yes				2
An event occurred at the EVENT DETECTOR3: 0: No 1: Yes				3
Zero passing of COUNTER1: 0: No 1: Yes			4	
Zero passing of COUNTER1 during a SCAN command: 0: No 1: Yes			5	
NULL			76	
The execution of an EXECUTE command is suspended: 0: No 1: Yes		8		
The execution of an EXECUTE Command is finished: 0: No 1: Yes		9		
The execution of an EXECUTE Command is resumed: 0: No 1: Yes		A		
The execution of an EXECUTE Command is started: 0: No 1: Yes		B		
A failure occurred at the READ BUFFER or at the WRITE BUFFER: 0: No 1: Yes	C			
The WRITE BUFFER is empty and the READ BUFFER is full: 0: No 1: Yes Only buffers in use are addressed.	D			
The execution of a command is cancelled: 0: No 1: Yes	E			
The execution of a command is finished: 0: No 1: Yes	F			

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STATUS1

External Signals and Requests	STATUS1			
The Input signal EVENT0 is an 0: 0-Level 1: 1-Level				0
The Input signal EVENT1 is an 0: 0-Level 1: 1-Level				1
The Input signal EVENT2 is an 0: 0-Level 1: 1-Level				2
The Input signal EVENT3 is an 0: 0-Level 1: 1-Level				3
NULL			7654	
A request for suspending an EXECUTE Command exists: 0: No 1: Yes		8		
A request for finishing an EXECUTE Command exists: 0: No 1: Yes		9		
A request for resuming an EXECUTE Command exists: 0: No 1: Yes		A		
A request for starting an EXECUTE Command exists: 0: No 1: Yes		B		
NULL	DC			
State of execution of a command: 0: The execution of an active command is suspended or no command is in process. 1: An active command is in process or the process is finishing.	E			
A command is active: 0: No 1: Yes	F			

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STATUS2

State of the Test Board and of the buffers	STATUS2			
Actual state of Test Board: 0000, 0001: TEST-LOGIC-RESET 0010, 0011: RUN-TEST/IDLE 0100: SHIFT-DR 0101: SHIFT-IR 0110: PAUSE-DR 0111: PAUSE-IR 1000: Temporary state				3210
NULL			7654	
WRITE BUFFER State: 00: both WRITE BUFFERs are empty 01: not used 10: one WRITE BUFFER is empty, one is full 11: both WRITE BUFFERs are full		98		
NULL		BA		
READ BUFFER State: 00: both READ BUFFERs are empty 01: one READ BUFFER is empty, one is full 10: not used 11: both READ BUFFERs are full	DC			
NULL	FE			

STATUS3

Not Used	STATUS3			
NULL	FEDC	BA98	7654	3210

CAPTURE0

COUNTER1 Low Value Word	CAPTURE0			
This register can be loaded with the lower value 16-Bit Word of COUNTER1 and afterwards it can be read.	FEDC	BA98	7654	3210

CAPTURE1

COUNTER1 High Value Word	CAPTURE1			
This register can be loaded with the higher value 16-Bit Word of COUNTER1 and afterwards it can be read.	FEDC	BA98	7654	3210

The actual value of COUNTER1 can be loaded into the CAPTURE0 and CAPTURE1 registers.

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READ BUFFER

Input Buffer for TDI	READ BUFFER			
16-Bit Receive Data	FEDC	BA98	7654	3210

WRITE BUFFER

Output Buffer for TDO	WRITE BUFFER			
16-Bit Transmission Data	FEDC	BA98	7654	3210

3.2 Typical Programming Procedure

Using a test board according to IEEE Std 1149.1, the commands typically are sent first to the test components with IR-SCAN, and the necessary test vectors communicated with subsequent DR-SCANs. Simultaneously, a DR-SCAN reads the system answer from the previous test vector. For a test of the connecting lines, the following procedure is typical:

1. IR-SCAN: command EXTEST for all test components
2. DR-SCAN: shift first test vector in all test components
3. DR-SCAN: read system reply to the first test vector and shift second test vector to all test components
4. DR-SCAN: read system reply to the second test vector and shift third test vector to all test components.
5. Etc.

An IR-SCAN approximates in programming to a DR-SCAN. Only bit 3 in the MAJOR COMMAND register must be programmed to 1 for an IR-SCAN, or to 0 for a DR-SCAN. To implement an IR-SCAN or DR-SCAN under the control of the TBC, the following programming steps are necessary:

1. First, the TBC must be configured using the ten control registers. If this already has been done, only some necessary changes to the configuration might need to be made.
2. The COUNTER1 UPDATE register must be programmed according to the length of the shift register.
3. Using the MAJOR COMMAND, IR-SCAN or DR-SCAN is selected and, subsequently, the MINOR COMMAND starts the execution of the commands.

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4. a) The STATUS register allows control of the status of the WRITE BUFFER. If one of the two buffers is empty, 16 command bits or 16 bits of the test vector must be written into the WRITE BUFFER. These bits are shifted from the TBC, over the TDO line, into the test board. Simultaneously, the TBC collects the bits from the TDI input into the SHIFTER FIFO. During this shifting operation, bits inevitably fall out at the other end of the shift register; these are read into the READ BUFFER via the READ TRANSFER FUNCTION.

   b) If the STATUS register shows that data in the READ BUFFER is available, this data must be read from the READ BUFFER.

   c) Steps 4a and 4b should be continued until all bits in the test board have been written. For the final iteration, usually less than 16 bits need to be shifted. Unneeded bits of the WRITE BUFFER will be ignored by the TBC; excess bits from the READ BUFFER are filled by the TBC with zeros.

5. The last data bits read from the TDI input are now in the SHIFTER-FIFO, and must be transferred into the READ BUFFER in order to proceed from there to the control computer.

Since the TBC continually sends the clock signal TCK to the test board, movement through the status diagram (see Figure 21) can be halted in only one of the six static states:

- TEST-LOGIC-RESET
- RUN-TEST/IDLE
- SHIFT-DR
- PAUSE-DR
- SHIFT-IR
- PAUSE-IR

If an interrupt in the shift cycle is necessary (e.g., the control computer has not yet written the next data in the WRITE BUFFER, or because both READ BUFFERs are full), the TBC changes to the PAUSE-DR or PAUSE-IR state. It remains there until the shift cycle can again proceed. The state in which the test board should wait after executing a command is chosen with the MAJOR COMMAND. In most cases, the RUN-TEST/IDLE state is used. If the PAUSE-DR or PAUSE-IR states are chosen, the fact should be noted that, after ending a command, the UPDATE-DR or UPDATE-IR phases would not proceed.

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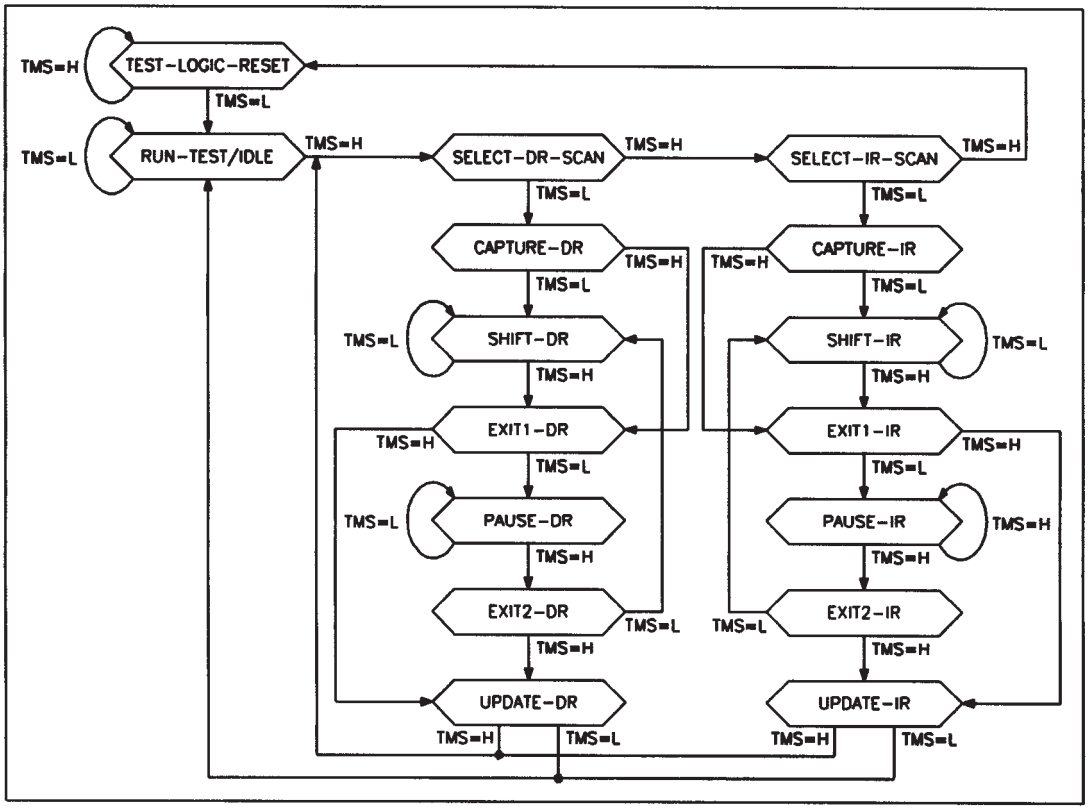


Figure 21. IEEE Std 1149.1 Test Access Port (TAP) Status Diagram

4 Examples

The programming of TBC SN74BCT8244N is demonstrated in the following examples. All examples assume the use of the same test board with two SN74BCT8244N SCOPE octals.

4.1 Example Test Board

All examples in this section are based on the same test board. To simplify an understanding of the examples, this test board consists of two SN74BCT8244N SCOPE octals from TI (see Figure 22). The programming methods used with more complex test boards are basically the same.

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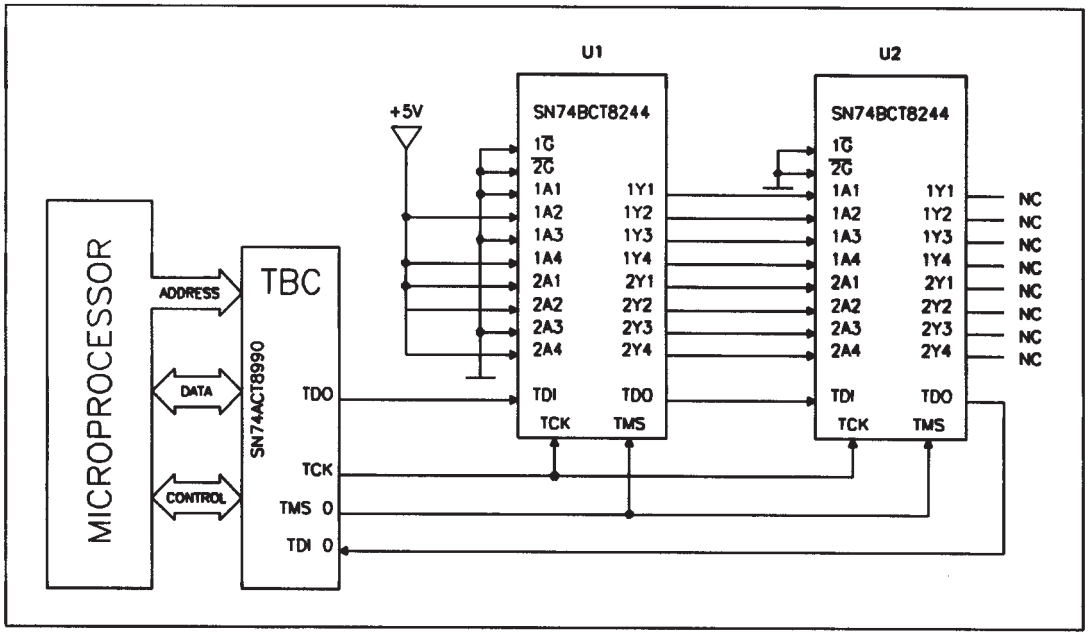


Figure 22. Hardware Example: Two SCOPE Octals SN74BCT8244N

The shift registers of the test boards are in the following states:

- SHIFT-IR state
  - 16-bit INSTRUCTION register (IR)
- SHIFT-DR state
  - 36 boundary scan cells (BSCs)
  - 4-bit BOUNDARY CONTROL register (BCR)
  - 2-bit BYPASS register

4.2 Software Examples

The first examples show the programming of three basic functions:

- Load commands in the test board
- Load test vectors in the test board
- Copy SHIFTER-FIFO in the READ BUFFER

The next example essentially is a combination of the three basic functions:

- EXTEST

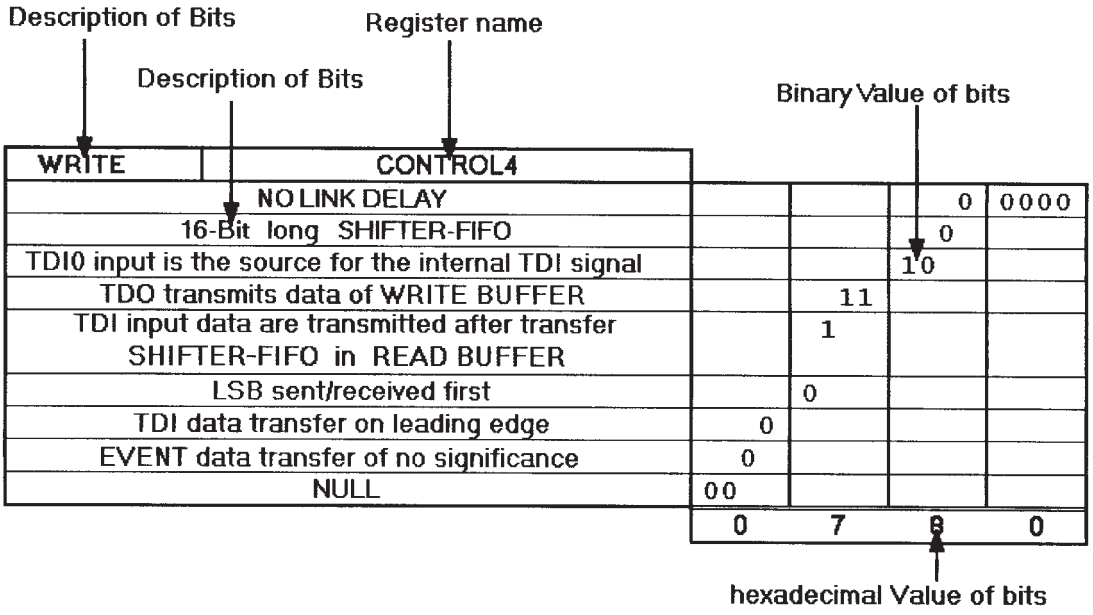
Finally, the pseudo-random pattern generation/parallel signature analysis (PRPG/PSA) is demonstrated with examples, with and without event control:

- PRPG/PSA without event control
- Event-controlled PRPG/PSA

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Each software example commences with a table, giving an overview of the basic functions that are used.

The programming of the registers is explained in detail in the tables. The tables show the register name and the direction of data flow, i.e., whether the register is being written into or read. In addition, descriptions of the individual bits and the resulting bit combinations are included, whether binary or hexadecimal.



4.2.1 Load Commands in Test Board

Nr.	Commands for both SCOPE™ OCTALs	MAJOR COMMAND		Description
		Command execution	Final state	
1	each 8-Bits READBT	IR-SCAN	RUN-TEST/IDLE	Load READBT command in test board

At the beginning of a test, the TBC always should be reset.

Write	MINOR COMMAND			
Complete reset				0001
NULL		0000	0000	
MINOR COMMAND Type: Software RESET	0111			
	7	0	0	1

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After reset of the whole TBC, it should be configured with the ten control registers:

- TDI0 as test data input
- TMS0 as TEST MODE SELECT output
- No interrupt transferred to the control computer
- The TMS2–TMS5/EVENT0–EVENT3 inputs/outputs are made TMS outputs, but are not used, so that the event logic remains unchanged.

Write	CONTROL0				
No interrupt at event					0000
No interrupt with COUNTER1 Flags				00	
NULL				00	
No interrupt from command output flags			0000		
No interrupt from change of a buffer state		00			
No interrupt on ending command		00			
		0	**0**	**0**	**0**

Write	CONTROL1				
No production test operation					0000
NULL				0000	
No production test operation		0	0000		
NULL		000			
		0	**0**	**0**	**0**

Write	CONTROL2				
Switch on TMS0, switch off TMS1..5				00	0001
NULL		0000	0000	00	
		0	**0**	**0**	**1**

Write	CONTROL3				
TMS2..5/EVENT0..3 are TMS outputs (here without significance)					1111
Test pulse output TCK0 is switched on				0	
Test data output TDO is switched on				0	
all TMS outputs are switched on				0	
all EVENT inputs/outputs are switched off				1	
Operation to IEEE 1149.1			0000		
TCKO is connected with the internal TCK source		00			
NULL		00			
		0	**0**	**8**	**F**

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Write	CONTROL4				
No LINK DELAY				0	0000
16-Bit long SHIFTER-FIFO				0	
TDI0 input is the source for the internal TDI signal				10	
TDO transmits data of WRITE BUFFER			11		
TDI input data are transmitted into the READ BUFFER after passing through the SHIFTER-FIFO			1		
The LSB is transmitted or received first			0		
TDI Data transfer at the leading edge		0			
EVENT Data transfer without significance		0			
NULL		00			
		0	**7**	**8**	**0**

Write	CONTROL5				
The EVENT output levels are here without significance					0000
NULL				0000	
The EVENT Data direction is here without significance			0000		
NULL		0000			
		0	**0**	**0**	**0**

Write	CONTROL6				
EVENT0 sets no Flags					0000
No recognition of EVENT0				0000	
EVENT1 sets no flags			0000		
No recognition of EVENT1		0000			
		0	**0**	**0**	**0**

Write	CONTROL7				
EVENT2 sets no Flags					0000
No recognition of EVENT2				0000	
EVENT3 sets no Flags			0000		
No recognition of EVENT3		0000			
		0	**0**	**0**	**0**

Write	CONTROL8				
COUNTER1 does not set the SUSPEND REQUEST Flag					0
COUNTER1 does not set the END REQUEST Flag					0
COUNTER1 is loaded at zero passing by the COUNTER1 UPDATE register					1
COUNTER1 does not count at events or EXECUTE commands				00	0
COUNTER1 does not respond to an event				00	
NULL		0000	0000		
		0	**0**	**0**	**4**

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Write	CONTROL9				
COUNTER2 is not used		0000	0000	0000	0000
		0	0	0	0

After configuration of the TBC with the ten control registers, the full length of the shift register should be loaded into COUNTER1.

Write	COUNTER1 UPDATE0				
Command registers of two SCOPE OCTALs are together 16 bits long ⇒ COUNTER1 lower value bits: 16-1=15		0000	0000	0000	1111
		0	0	0	F

Write	COUNTER1 UPDATE1				
COUNTER1 higher value bits are 0		0000	0000	0000	0000
		0	0	0	0

Write	MINOR COMMAND				
Load COUNTER1 from COUNTER1 UPDATE register					001
NULL					0
No operation with COUNTER2 or Status				000	
NULL			0000	0	
MINOR COMMAND Type: Read status, load counter and count		0110			
		6	0	0	1

With the MAJOR COMMAND, presets are chosen and the MINOR COMMAND starts the shift operation.

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Write	MAJOR COMMAND				
State after completing the command: RUN-TEST/IDLE					011
Execute command in SHIFT-IR and put command in PAUSE-IR state					1
Terminate command at zero passing of COUNTER1				00	
NULL			0000	00	
MAJOR COMMAND Type: SCAN command		0011			
		3	**0**	**0**	**B**

Write	MINOR COMMAND				
All Flags are reset					0000
NULL				0	
Start of a SCAN command				100	
NULL			0000		
MINOR COMMAND Type: Control of the test procedure		0101			
		5	**0**	**8**	**0**

The TBC now is ready to send commands to the test board via TDO, and to receive the status of the test board via TDI.

Before the WRITE BUFFER is written, the status of the WRITE BUFFER must be interrogated.

Write	MINOR COMMAND				
Load COUNTER1 in the CAPTURE register					100
NULL					0
refresh all 3 STATUS registers				100	
NULL			0000	0	
MINOR COMMAND Type: Read status, load counter and count		0110			
		6	**0**	**4**	**4**

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The STATUS2 register now contains the following bit combination:

Read	STATUS2				
test board is in PAUSE-IR state					0111
NULL				0000	
both WRITE BUFFER are empty			00		
NULL			00		
both READ BUFFER are empty		00			
NULL		00			
		0	**0**	**0**	**7**

Write	WRITE BUFFER				
READBT command for SCOPE™ OCTAL U2				1000	1011
READBT command for SCOPE™ OCTAL U1		1000	1011		
		8	**B**	**8**	**B**

As soon as the WRITE BUFFER has been loaded, the TBC begins to shift the data. Since the 16 bits of the WRITE BUFFER exactly match the length of the shift register, the WRITE BUFFER needs no further data. The next step is the reading of the READ BUFFER. For this, the status must be interrogated first, and only when the READ BUFFER is filled with data can it be read out.

Write	MINOR COMMAND				
Load COUNTER1 in the CAPTURE register					100
NULL					0
refresh all 3 STATUS registers				100	
NULL			0000	0	
MINOR COMMAND Type: Read status, load counter and count		0110			
		6	**0**	**4**	**4**

The READ BUFFER can be read out if the STATUS3 register contains the following bit combination:

Read	STATUS2				
Test board is in RUN-TEST/IDLE state					0011
NULL				0000	
both WRITE BUFFER are empty			00		
NULL			00		
one READ BUFFER contains Data		01			
NULL		00			
		1	**0**	**0**	**3**

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The following value now can be read out from the READ BUFFER:

Read	READ BUFFER				
1's of SHIFTER-FIFOs after reset		1111	1111	1111	1111
		F	F	F	F

The status information of the two SCOPE octals is now in the SHIFTER-FIFO. If a test vector is shifted into the test board, the next 16 bits of the READ BUFFER will contain the status information of the two SCOPE octals. If it is required to receive the status information immediately, the contents of the SHIFTER-FIFO must be copied into the READ BUFFER. An example of this is given in section 4.2.3.

4.2.2 Load Test Vector in Test Board

Nr.	Data for both SCOPE™ OCTALs	MAJOR COMMAND		Description
		Command execution	Final state	
1	Each 18 bits test vector	DR-SCAN	RUN-TEST/IDLE	Load test vector

Loading a test vector into the test board differs from loading commands in the following respects:

- Length of the shift register is 36 bits.
- DR-SCAN must be chosen to shift the test vector.

The control registers should be programmed only if they differ from a previous program. Since the DR-SCAN usually follows an IR-SCAN, the control registers do not need to be programmed again. A detailed description of the control register programming is given in section 4.2.1.

Write	CONTROL0	0	0	0	0
Write	CONTROL1	0	0	0	0
Write	CONTROL2	0	0	0	1
Write	CONTROL3	0	0	8	F
Write	CONTROL4	0	7	8	0
Write	CONTROL5	0	0	0	0
Write	CONTROL6	0	0	0	0
Write	CONTROL7	0	0	0	0
Write	CONTROL8	0	0	0	4
Write	CONTROL9	0	0	0	0

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COUNTER1 now must be programmed to the length of the shift register: 36 – 1 = 35 = 0x23.

Write	**COUNTER1 UPDATE0**	**0**	**0**	**2**	**3**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**

With the MAJOR COMMAND, now the DR-SCAN is chosen. The MINOR COMMAND then starts the shifting operation again.

Write	**MAJOR COMMAND**				
State after executing command RUN-TEST/IDLE					011
Execution of command in SHIFT-DR state and suspension of command in PAUSE-DR state					0
Terminate command at zero passing of COUNTER1				00	
NULL			0000	00	
MAJOR COMMAND type: SCAN command		0011			
		3	**0**	**0**	**3**

Write	**MINOR COMMAND**				
All Flags are reset.					0000
NULL				0	
Start of a SCAN command				100	
NULL			0000		
MINOR COMMAND type: Control of test process		0101			
		5	**0**	**8**	**0**

The WRITE BUFFER now can be fed with data again, and the READ BUFFER read out. Reading out STATUS2 register again ensures that the buffer is ready.

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**

Read	**STATUS2**				
Test board is in PAUSE-DR state					0110
NULL				0000	
both WRITE BUFFER are empty			00		
NULL			00		
both READ BUFFER are empty		00			
NULL		00			
		0	**0**	**0**	**6**

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If both WRITE BUFFERs are empty, 2 × 16 bits can be entered immediately.

Write	WRITE BUFFER				
1Y1..1Y4,2Y1..2Y4 Test sample of the SCOPE™ OCTAL U2			0010	0001	
1A1..1A4,2A1..2A4 Test sample of the SCOPE™ OCTAL U2	0100	0011			
	4	3	2	1	

Write	WRITE BUFFER				
1G, 2G Test sample of the SCOPE™ OCTAL U2				00	
1Y1..1Y4,2Y1..2Y4 Test sample of the SCOPE™ OCTAL U1		10	0111	10	
1A1..1A4,2A1..2A2 Test sample of the SCOPE™ OCTAL U1	0101	01			
	5	6	7	8	

If the TBC has shifted out the 32 bits of the WRITE BUFFER via TDO, it reads also 32 bits at the TDI input into the SHIFTER-FIFO, and from there into the READ BUFFER. To be able to shift further data into the test board, at least one 16-bit word from the READ BUFFER must be read next. Via the STATUS2 register, it also must be determined if data is already available.

Write	MINOR COMMAND	6	0	4	4

Read	STATUS2				
Momentary state of the test board				????	
NULL			0000		
Momentary state of WRITE BUFFER		??			
NULL		00			
At least one register of the READ BUFFER is full	?1				
NULL	00				
	3/1	?	0	?	

If this DR-SCAN example occurred before the example from section 4.2.1, the following values can be read from the READ BUFFER:

Read	READ BUFFER				
Status information of SCOPE™ OCTAL U2			1000	0001	
Status information of SCOPE™ OCTAL U1	1000	0001			
	8	1	8	1	

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If the READ BUFFER has been read, then at least 16 bits were shifted through the test board, and, as a result, at least one register of the WRITE BUFFER must be empty. To be safe, the status also can be ascertained before addressing the WRITE BUFFER. Since the shift register is 36 bits long and 32 bits have already been written into the WRITE BUFFER, only 4 bits from the test vector are missing. The remaining 12 bits of the WRITE BUFFER can be occupied with any desired words, because they will not be shifted out into the test board.

Write	WRITE BUFFER				
2A3..2A4 Test sample of the SCOPE™ OCTAL U1					11
1G, 2G Test sample of the SCOPE™ OCTAL U1					00
bits not used anymore		0000	0000	0000	
		0	**0**	**0**	**3**

Finally, the last data from the READ BUFFER must be read out. Status interrogation again ensures that data is available.

Write	MINOR COMMAND	**6**	**0**	**4**	**4**
Read	**STATUS2**	**3/1**	**?**	**0**	**?**
Read	**READ BUFFER**				
1Y1..1Y4,2Y1..2Y4 Test sample of the SCOPE™ OCTAL U2				????	????
1A1..1A4,2A1..2A4 Test sample of the SCOPE™ OCTAL U2		????	????		
		?	**?**	**?**	**?**

Because only four bits have been shifted at the last shift operation, only four bits arrived from the SHIFTER-FIFO to the READ BUFFER.

Write	MINOR COMMAND	**6**	**0**	**4**	**4**
Read	**STATUS2**	**1**	**0**	**0**	**?**
Read	**READ BUFFER**				
1G, 2G Test sample of the SCOPE™ OCTAL U2					??
1Y1..1Y2 Test sample of the SCOPE™ OCTAL U1					??
NULL		0000	0000	0000	
		0	**0**	**0**	**?**

The following 16 bits are still in the SHIFTER-FIFO:

- Six bits: 1Y3–1Y4, 2Y1–2Y4 (test sample of SCOPE octal U1)
- Eight bits: 1A1–1Y4, 2Y1–2Y4 (test sample of SCOPE octal U1)
- Two bits: 1G, 2G (test sample of SCOPE octal U1)

The example in section 4.2.3 shows how these 16 bits can be copied into the READ BUFFER.

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4.2.3 Copy SHIFTER-FIFO Into the Read Buffer

Nr.	Commands and Data for both SCOPE™ OCTALs	MAJOR COMMAND		Description
		Command execution	Final state	
1	-	-	-	Read SHIFTER-FIFO

To copy the contents of the SHIFTER-FIFO into the READ BUFFER, the component must be configured in such a way that the output data of the SHIFTER-FIFO serves as the source for the input data of the SHIFTER-FIFO. Therefore, the FIFO must be connected as a circular memory. Then, the SHIFTER-FIFO will be shifted, according to the program, 16 or 32 times. Because each bit that leaves the SHIFTER-FIFO is copied into the READ BUFFER, the READ BUFFER contains a copy of the SHIFTER-FIFO after this operation.

Write	**CONTROL4**				
No LINK DELAY				0	0000
16-bit long SHIFTER-FIFO				0	
Internal TDO is source for the internal TDI signal				00	
TDO transmits data of the SHIFTER-FIFOs			10		
TDI input data are transmitted after copying the SHIFTER-FIFO into the READ BUFFER			1		
The LSB is transmitted or received first			0		
TDI data taking over at leading edge		0			
EVENT data taking over here without significance		0			
NULL		00			
		0	**6**	**0**	**0**

Write	**COUNTER1 UPDATE0**	**0**	**0**	**0**	**F**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**

Write	**MINOR COMMAND**				
All Flags are reset.					0000
NULL				0	
Start of a SCAN command				100	
NULL			0000		
MINOR COMMAND type: Control of test process		0101			
		5	**0**	**8**	**0**

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The contents of SHIFTER-FIFO can be removed from the READ BUFFER. If this is done as shown in the example in section 4.2.2, the READ BUFFER contains the following bit sample:

Read	READ BUFFER				
1Y3..1Y4,2Y1..2Y4 Test sample of SCOPE™ OCTAL U1				??	????
1A1..1A4,2A1..2A4 Test sample of SCOPE™ OCTAL U1		??	????	??	
1G, 2G Test sample of SCOPE™ OCTAL U1		??			
		?	?	?	?

With this operation, the contents of the SHIFTER-FIFO remain unchanged, and the state of the test board also remains unchanged.

4.2.4 EXTEST

With the three basic functions for the preceding section, an EXTEST for the test board used can be made very easily. The following shifting actions are necessary for this:

Nr.	Commands and data for both SCOPE™ OCTALs	MAJOR COMMAND		Description
		Command execution	Final state	
1	each 8 bits EXTEST	IR-SCAN	RUN-TEST/IDLE	Load command in test board
2	each 18 bits test vector	DR-SCAN	RUN-TEST/IDLE	Load 1st test vector
3	each 18 bits test vector	DR-SCAN	RUN-TEST/IDLE	Read system reply to 1st test vector and load 2nd test vector
4	-	-	-	Read SHIFTER-FIFO

The following tables show the test vectors used and the system reply to this vector that results.

SCOPE™ OCTAL U1			SCOPE™ OCTAL U2		
1G, 2G	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4	1G, 2G	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4
00	11010101	10011110	00	01000011	00100001
00	01011101	11010101	00	10011110	01000011

The necessary program steps for this already have been explained in detail in previous examples, and are summarized here:

First, the TBC is reset and subsequently configured, with the help of the control register.

Write	MINOR COMMAND	7	0	0	1

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1. Load command in test board

Write	CONTROL0	0	0	0	0
Write	CONTROL1	0	0	0	0
Write	CONTROL2	0	0	0	1
Write	CONTROL3	0	0	8	F
Write	CONTROL4	0	7	8	0
Write	CONTROL5	0	0	0	0
Write	CONTROL6	0	0	0	0
Write	CONTROL7	0	0	0	0
Write	CONTROL8	0	0	0	4
Write	CONTROL9	0	0	0	0

Both SCOPE octals are loaded with the command EXTEST. The value to be read from the READ BUFFER is the 1s from the reset SHIFTER-FIFO.

Write	COUNTER1 UPDATE0	0	0	0	F
Write	COUNTER1 UPDATE1	0	0	0	0
Write	MINOR COMMAND	6	0	0	1

Write	MAJOR COMMAND	3	0	0	B
Write	MINOR COMMAND	5	0	8	0

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	0	0	0	7
Write	WRITE BUFFER	0	0	0	0

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	1	0	0	3
Read	READ BUFFER	F	F	F	F

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2. Load first test vector

   The first test vector is shifted into the two SCOPE octals. The first 16-bit word of the READ BUFFER contains the status information, which the SCOPE octals produce on writing in a command. Subsequently, bitmaps are read that were present in the SCOPE octals before the beginning of the test.

Write	COUNTER1 UPDATE0	0	0	2	3
Write	COUNTER1 UPDATE1	0	0	0	0
Write	MINOR COMMAND	6	0	0	1

Write	MAJOR COMMAND	3	0	0	3
Write	MINOR COMMAND	5	0	8	0

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	0	0	0	6
Write	WRITE BUFFER	4	3	2	1
Write	WRITE BUFFER	5	6	7	8

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	3/1	?	0	?
Read	READ BUFFER				
Status information of the SCOPE™ OCTALs U2				1000	0001
Status information of the SCOPE™ OCTALs U1		1000	0001		
		8	1	8	1

Write	WRITE BUFFER	0	0	0	3

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	3/1	?	0	?
Read	READ BUFFER				
1Y1..1Y4,2Y1..2Y4 Test sample of the SCOPE™ OCTAL U2				????	????
1A1..1A4,2A1..2A4 Test sample of the SCOPE™ OCTAL U2		????	????		
		?	?	?	?

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	1	0	0	3
Read	READ BUFFER				
1G, 2G Test sample of the SCOPE™ OCTAL U2					??
1Y1..1Y2 Test sample of the SCOPE™ OCTAL U1					??
NULL		0000	0000	0000	
		0	0	0	?

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3. Read system reply to first test vector and load second test vector

   The next test vector now is shifted into the SCOPE octals. From the READ BUFFER, the rest of the previous bitmap of the SCOPE octals can be read first, and then the system reply of the SCOPE octals to the first test vector.

Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**
Write	**MAJOR COMMAND**	**3**	**0**	**0**	**3**
Write	**MINOR COMMAND**	**5**	**0**	**8**	**0**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**0**	**0**	**0**	**6**
Write	**WRITE BUFFER**	**4**	**3**	**2**	**1**
Write	**WRITE BUFFER**	**5**	**6**	**7**	**8**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**3/1**	**?**	**0**	**?**
Read	**READ BUFFER**				
1Y3..1Y4,2Y1..2Y4 Test sample of the SCOPE™ OCTAL U1				??	????
1A1..1Y4,2Y1..2Y4 Test sample of the SCOPE™ OCTAL U1		??	????	??	
2 Bit: 1G, 2G Test sample of the SCOPE™ OCTAL U1		??			
		?	**?**	**?**	**?**

Write	**WRITE BUFFER**	**0**	**0**	**0**	**3**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**3/1**	**?**	**0**	**?**
Read	**READ BUFFER**				
1Y1..1Y4,2Y1..2Y4 Test sample of the SCOPE™ OCTAL U2				0100	0011
1A1..1A4,2A1..2A4 Test sample of the SCOPE™ OCTAL U2		1001	1110		
		9	**E**	**4**	**3**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**1**	**0**	**0**	**3**
Read	**READ BUFFER**				
1G, 2G Test sample of the SCOPE™ OCTAL U2					00
1Y1..1Y2 Test sample of the SCOPE™ OCTAL U1					01
NULL		0000	0000	0000	
		0	**0**	**0**	**4**

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4. Read SHIFTER-FIFO

   The missing 16 bits of the system reply still are in the SHIFTER-FIFO. To receive these bits, the contents of the SHIFTER-FIFO must be copied into the READ BUFFER.

Write	**CONTROL4**	**0**	**6**	**0**	**0**
Write	**COUNTER1 UPDATE0**	**0**	**0**	**0**	**F**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**
Write	**MINOR COMMAND**	**5**	**0**	**8**	**0**
Write	**CONTROL4**	**0**	**7**	**8**	**0**
Read	**READ BUFFER**				
1Y3..1Y4, 2Y1..2Y4 Test sample of the SCOPE™ OCTAL U1				11	0101
1A1..1A4, 2A1..2A4 Test sample of the SCOPE™ OCTAL U1		01	0111	01	
1G, 2G Test sample of the SCOPE™ OCTAL U1		00			
		1	**7**	**7**	**5**

The EXTEST has been completed. The test vector was written with three shift operations into the test board. In the same way, reading the system reply to the test vector of the READ BUFFER is done in three steps:

3.) 16Bit	2.) 4 Bit	1.) 16 Bit
0001011101110101	0100	1001111001000011

The result is coded into the two SCOPE octals as follows:

SCOPE™ OCTAL U1			SCOPE™ OCTAL U2		
1G, 2G	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4	1G, 2G	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4
00	01011101	11010101	00	10011110	01000011

4.2.5 PRPG/PSA

This example shows how, with the three basic functions, IR-SCAN, DR-SCAN, and read SHIFTER-FIFO, and an additional EXECUTE RUN-TEST/IDLE block, a PRPG/PSA test can be built up. New in this example is the command EXECUTE from the TBC, which can generate a defined number of RUN-TEST/IDLE cycles.

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Nr.	Command and Data for both SCOPE™ OCTALs	MAJOR COMMAND		Description
		Command execution	Final state	
1	each 8 bits SAMPLE	IR-SCAN	RUN-TEST/IDLE	Load initial value
2	each 18 bits test vector	DR-SCAN	RUN-TEST/IDLE	
3	each 8 bits SCANCT	IR-SCAN	RUN-TEST/IDLE	Load BOUNDARY CONTROL register with PRPG/PSA
4	each 2 bits PRPG/PSA	DR-SCAN	RUN-TEST/IDLE	
5	each 8 bits RUNT	IR-SCAN	PAUSE-IR	load RUNT command into common register
6		EXECUTE	PAUSE-IR	execute PRPG/PSA
7	each 8 bits READBT	IR-SCAN	RUN-TEST/IDLE	read result vector
8	each 18 bits next test vector	DR-SCAN	RUN-TEST/IDLE	
9	-	-	-	Load SHIFTER FIFO

The example hardware uses the bit combination 01011101 as the input signal for the component U1. The signature at the inputs of U1 is determined from the bit combination and the initial value used.

The signature at the inputs of U2 is based on the output signal from U1 and the initial value. Only the initial value is decisive for the bit sequence of the PRPG. Now the PRPG and the PSA of both SN74BCT8244N generate the following bit sequences:

PRPG PSA Nr.	SCOPE™ OCTAL U1		SCOPE™ OCTAL U2	
	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4
	11010101	10011110	01000011	00100001
1	10110111	11011111	10111111	00010000
2	10000110	01100111	00010000	10001000
3	00011110	10110011	11101111	01000100
4	10110010	11011001	01000100	10100010
5	00110100	11101100	01111011	11010001
6	01000111	01110110	11010001	11101000
7	01111110	10111011	10011110	01110100
8	11100010	11011101	01110100	10111010
9	00101100	11101110	01100111	01011101
10	11001011	01110111	01011101	10101110

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The following tables show the test vector used as an initial value and the expected system reply to this vector after ten PRPG/PSA cycles:

SCOPE™ OCTAL U1			SCOPE™ OCTAL U2		
1G, 2G	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4	1G, 2G	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4
00	11010101	10011110	00	01000011	00100001
00	11001011	01110111	00	01011101	10101110

First, the TBC must be reset.

Write	MINOR COMMAND	7	0	0	1

1. Load initial values: IR-SCAN sample

Write	CONTROL0	0	0	0	0
Write	CONTROL1	0	0	0	0
Write	CONTROL2	0	0	0	1
Write	CONTROL3	0	0	8	F
Write	CONTROL4	0	7	8	0
Write	CONTROL5	0	0	0	0
Write	CONTROL6	0	0	0	0
Write	CONTROL7	0	0	0	0
Write	CONTROL8	0	0	0	4
Write	CONTROL9	0	0	0	0

Write	COUNTER1 UPDATE0	0	0	0	F
Write	COUNTER1 UPDATE1	0	0	0	0
Write	MINOR COMMAND	6	0	0	1

Write	MAJOR COMMAND	3	0	0	B
Write	MINOR COMMAND	5	0	8	0

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	0	0	0	7
Write	WRITE BUFFER				
SAMPLE command for SCOPE™ OCTAL U2				1000	1011
SAMPLE command for SCOPE™ OCTAL U1		1000	1011		
		8	B	8	B

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	1	0	0	3
Read	READ BUFFER	F	F	F	F

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2. Load initial values: DR-SCAN test vector

Write	COUNTER1 UPDATE0	0	0	2	3
Write	COUNTER1 UPDATE1	0	0	0	0
Write	MINOR COMMAND	6	0	0	1

Write	MAJOR COMMAND	3	0	0	3
Write	MINOR COMMAND	5	0	8	0

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	0	0	0	6
Write	WRITE BUFFER	4	3	2	1
Write	WRITE BUFFER	5	6	7	8

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	3/1	?	0	?
Read	READ BUFFER				
Status information of the SCOPE™ OCTALs U2				1000	0001
Status information of the SCOPE™ OCTALs U1		1000	0001		
		8	1	8	1

Write	WRITE BUFFER	0	0	0	3

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	3/1	?	0	?
Read	READ BUFFER				
1Y1..1Y4,2Y1..2Y4 Test result of the SCOPE™ OCTAL U2				????	????
1A1..1A4,2A1..2A4 Test result of the SCOPE™ OCTAL U2		????	????		
		?	?	?	?

Write	MINOR COMMAND	6	0	4	4
Read	STATUS2	1	0	0	3
Read	READ BUFFER				
1G, 2G Test result of the SCOPE™ OCTAL U2					??
1Y1..1Y2 Test result of the SCOPE™ OCTAL U1					??
NULL		0000	0000	0000	
		0	0	0	?

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3. Load BCR with PRPG/PSA: IR-SCAN SCANCT

Write	**COUNTER1 UPDATE0**	**0**	**0**	**0**	**F**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**

Write	**MAJOR COMMAND**	**3**	**0**	**0**	**B**
Write	**MINOR COMMAND**	**5**	**0**	**8**	**0**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**0**	**0**	**0**	**7**
Write	**WRITE BUFFER**				
SCANCT Command for SCOPE™ OCTAL U2				0000	1111
SCANCT Command for SCOPE™ OCTAL U1		0000	1111		
		0	**F**	**0**	**F**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**1**	**0**	**0**	**3**
Read	**READ BUFFER**				
1Y3..1Y4,2Y1..2Y4 Test result of the SCOPE™ OCTAL U1				??	????
1A1..1Y4,2Y1..2Y4 Test result of the SCOPE™ OCTAL U1		??	????	??	
2 Bit: 1G, 2G Test result of the SCOPE™ OCTAL U1		??			
		?	**?**	**?**	**?**

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4. Load BCR: DR-SCAN 8-bit PRPG/PSA

Write	**COUNTER1 UPDATE0**	**0**	**0**	**0**	**3**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**

Write	**MAJOR COMMAND**	**3**	**0**	**0**	**3**
Write	**MINOR COMMAND**	**5**	**0**	**8**	**0**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**0**	**0**	**0**	**6**
Write	**WRITE BUFFER**				
8 Bit PRPG/PSA Command for SCOPE™ OCTAL U2					11
8 Bit PRPG/PSA Command for SCOPE™ OCTAL U1					11
NULL		0000	0000	0000	
		0	**0**	**0**	**F**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**3/1**	**?**	**0**	**?**
Read	**READ BUFFER**				
1st Byte, Status information of SCOPE™ OCTALs U2					0001
NULL		0000	0000	0000	
		0	**0**	**0**	**1**

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5. Load RUNT command in COMMAND register

Write	**COUNTER1 UPDATE0**	**0**	**0**	**0**	**F**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**

Write	**MAJOR COMMAND**				
State after command execution: PAUSE-IR					111
Execute command in SHIFT-IR and suspension of command execution in PAUSE-IR state					1
Terminate command at zero passing of COUNTER1				00	
NULL			0000	00	
MAJOR COMMAND type: SCAN command		0011			
		3	**0**	**0**	**F**
Write	**MINOR COMMAND**	**5**	**0**	**8**	**0**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**0**	**0**	**0**	**7**
Write	**WRITE BUFFER**				
RUNT command for SCOPE™ OCTAL U2				0000	1001
RUNT command for SCOPE™ OCTAL U1		0000	1001		
		0	**9**	**0**	**9**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**1**	**0**	**0**	**7**
Read	**READ BUFFER**				
2nd Byte, Status information of SCOPE™ OCTAL U2					1000
Status information of SCOPE™ OCTAL U1			1000	0001	
BOUNDARY CONTROL register of SCOPE™ OCTAL U2		??			
BOUNDARY CONTROL register of SCOPE™ OCTAL U1		??			
		?	**8**	**1**	**8**

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6. Implement PRPG/PSA

Before the PRPG/PSA implementation can begin, the configuration of the TBC must be changed. The COUNTER1 is used to count the TCK edges during the RUN-TEST/IDLE states.

Write	CONTROL8				
COUNTER1 does not set the SUSPEND REQUEST Flag					0
COUNTER1 sets the END REQUEST Flag					1
COUNTER1 is loaded by the COUNTER1 UPDATE register at zero passing					1
COUNTER1 does not count at EXECUTE commands in RUN-TEST/IDLE state				01	0
COUNTER1 does not react on any event				00	
NULL		0000	0000		
		0	**0**	**1**	**6**

COUNTER1 is loaded now with the number of RUN-TEST/IDLE cycles. In this case, ten cycles should be made. The register must be programmed with the value (10 – 1) = 9.

Write	**COUNTER1 UPDATE0**	**0**	**0**	**0**	**9**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**

MINOR COMMAND and MAJOR COMMAND start the PRPG/PSA implementation.

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Write	MAJOR COMMAND				
State after executing command: PAUSE-IR					111
Command execution in RUN-TEST/IDLE state and suspension of command in PAUSE-IR state					1
Terminate command at zero passing of COUNTER1				00	
The command implementation starts immediately.				11	
no significance here, since execution is not interrupted			0		
NULL			000		
MAJOR COMMAND type: EXECUTE command		0010			
		2	**0**	**C**	**F**

Write	MINOR COMMAND				
All Flags are reset.					1111
NULL				0	
immediate start of EXECUTE command				100	
NULL			0000		
MINOR COMMAND type: Control of test run		0100			
		4	**0**	**8**	**F**

Write	CONTROL8				
COUNTER1 does not set SUSPEND REQUEST Flag					0
COUNTER1 does not set END REQUEST Flag					0
COUNTER1 is loaded by COUNTER1 UPDATE register at zero passing					1
COUNTER1 does not count events or EXECUTE commands				00	0
COUNTER1 does not react to any event				00	
NULL		0000	0000		
		0	**0**	**0**	**4**

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7. Read result vector: IR-SCAN READBT

To read the result vectors, one of the two commands, READBT or READBN, must be used. Other commands, such as EXTEST or SAMPLE, are written over during the UPIDATE-IR phase, with the result of the PRPG/PSA.

Write	**COUNTER1 UPDATE0**	**0**	**0**	**0**	**F**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**

Write	**MAJOR COMMAND**	**3**	**0**	**0**	**B**
Write	**MINOR COMMAND**	**5**	**0**	**8**	**0**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**0**	**0**	**0**	**7**
Write	**WRITE BUFFER**				
READBT command for SCOPE™ OCTAL U2				1000	1011
READBT command for SCOPE™ OCTAL U1		1000	1011		
		8	**B**	**8**	**B**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**1**	**0**	**0**	**3**
Read	**READ BUFFER**				
Status information of SCOPE™ OCTAL U2				1000	0001
Status information of SCOPE™ OCTAL U1		1000	0001		
		8	**1**	**8**	**1**

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8. Read result vector: DR-SCAN

Write	**COUNTER1 UPDATE0**	**0**	**0**	**2**	**3**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**

Write	**MAJOR COMMAND**	**3**	**0**	**0**	**3**
Write	**MINOR COMMAND**	**5**	**0**	**8**	**0**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**0**	**0**	**0**	**6**
Write	**WRITE BUFFER**	**4**	**3**	**2**	**1**
Write	**WRITE BUFFER**	**5**	**6**	**7**	**8**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**3/1**	**?**	**0**	**?**
Read	**READ BUFFER**				
Status information of SCOPE™ OCTAL U2				1000	0001
Status information of SCOPE™ OCTAL U1		1000	0001		
		8	**1**	**8**	**1**

Write	**WRITE BUFFER**	**0**	**0**	**0**	**3**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**3/1**	**?**	**0**	**?**
Read	**READ BUFFER**				
1Y1..1Y4,2Y1..2Y4 Test result of the SCOPE™ OCTAL U2				1010	1110
1A1..1A4,2A1..2A4 Test result of the SCOPE™ OCTAL U2		0101	1101		
		5	**D**	**A**	**E**

Write	**MINOR COMMAND**	**6**	**0**	**4**	**4**
Read	**STATUS2**	**1**	**0**	**0**	**3**
Read	**READ BUFFER**				
1G, 2G Test result of the SCOPE™ OCTAL U2					00
1Y1..1Y2 Test result of the SCOPE™ OCTAL U1					11
NULL		0000	0000	0000	
		0	**0**	**0**	**C**

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9. Read SHIFTER-FIFO

Write	**CONTROL4**	**0**	**6**	**0**	**0**
Write	**COUNTER1 UPDATE0**	**0**	**0**	**0**	**F**
Write	**COUNTER1 UPDATE1**	**0**	**0**	**0**	**0**
Write	**MINOR COMMAND**	**6**	**0**	**0**	**1**
Write	**MINOR COMMAND**	**5**	**0**	**8**	**0**
Write	**CONTROL4**	**0**	**7**	**8**	**0**
Read	**READ BUFFER**				
1Y3..1Y4, 2Y1..2Y4 Test result of the SCOPE™ OCTAL U1				01	1101
1A1..1A4, 2A1..2A4 Test result of the SCOPE™ OCTAL U1		11	0010	11	
1G, 2G Test result of the SCOPE™ OCTAL U1		00			
		3	**2**	**D**	**D**

The system reply to the test vector is read by the READ BUFFER in three steps:

3.) 16 Bit	2.) 4 Bit	1.) 16 Bit
0011001011011101	1100	0101110110101110

The result, coded in the two SCOPE octals, is given below:

SCOPE™ OCTAL U1			SCOPE™ OCTAL U2		
1G, 2G	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4	1G, 2G	1A1..1A4, 2A1..2A4	1Y1..1Y4, 2Y1..2Y4
00	11001011	01110111	00	01011101	10101110

4.2.6 Event-Controlled PRPG/PSA

This example is a further development of the previous PRPG/PSA example. In this case, however, the PRPG/PSA will start only when a rising edge has arrived five times at the event input EVENT2.

The programming of the TBC is nearly identical with that of the PRPG/PSA example. Only the sixth step, the execution of the PRPG/PSA, is somewhat changed. Therefore, only this sixth step will be explained in detail; all other steps should be taken from the PRPG/PSA example.

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Nr.	Commands and data for both SCOPE™ OCTALs	MAJOR COMMAND		Description
		Command execution	Final state	
1	each 8 bits SAMPLE	IR-SCAN	RUN-TEST/IDLE	Load initial values
2	each 18 bits test vector	DR-SCAN	RUN-TEST/IDLE	
3	each 8 bits SCANCT	IR-SCAN	RUN-TEST/IDLE	Load BOUNDARY CONTROL register with PRPG/PSA
4	each 2 bits PRPG/PSA	DR-SCAN	RUN-TEST/IDLE	
5	each 8 bits RUNT	IR-SCAN	PAUSE-IR	Load RUNT command in command register
6		EXECUTE	PAUSE-IR	execute PRPG/PSA
7	each 8 its READBT	IR-SCAN	RUN-TEST/IDLE	Read result vector
8	each 8 bits next test vector	DR-SCAN	RUN-TEST/IDLE	
9	-	-	-	Read SHIFTER FIFO

4.2.7 Implement PRPG/PSA

Before execution of the PRPG/PSA can begin, the configuration of the TBC must be changed. COUNTER1 is used to count the TCK edges during the RUN-TEST/IDLE state. COUNTER20 counts the events occurring at the EVENT2 input.

Write	CONTROL3				
TMS2/EVENT0 is TMS output (here without significance)					0
TMS3/EVENT1 is EVENT input					1
TMS4 .. TMS5/EVENT2 .. EVENT3 are TMS outputs (here without significance)					00
Test pulse output TCK0 is switched on				0	
Test data output TDO is switched on				0	
All TMS outputs are switched on				0	
All EVENT outputs are switched off				1	
Operation to IEEE 1149.1			0000		
TCKO is connected with internal TCK source		00			
NULL		00			
		0	**0**	**8**	**3**

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Write	CONTROL4				
No LINK DELAY				0	0000
16-Bit long SHIFTER-FIFO				0	
TDI0 input is source for the internal TDI signal				10	
TDO transmits data of the WRITE BUFFER			11		
TDI input data are transmitted into READ BUFFER after passing the SHIFTER-FIFO			1		
The LSB is transmitted/received first			0		
TDI data transfer at leading edge		0			
EVENT data transfer at trailing edge		0			
NULL		00			
		0	**7**	**8**	**0**

Write	CONTROL7				
EVENT2 sets the RESUME REQUEST Flag					0100
Asynchronous recognition of EVENT2				0	
EVENT2 recognition always occurs				0	
Event is detected at zero passing of COUNTER20				10	
EVENT3 sets no Flags			0000		
No recognition of EVENT3		0000			
		0	**0**	**8**	**4**

Write	CONTROL8				
COUNTER1 does not set the SUSPEND REQUEST Flag					0
COUNTER1 sets the END REQUEST Flag					1
COUNTER1 is loaded by the COUNTER1 UPDATE register at zero crossing					1
COUNTER1 counts the test edges during EXECUTE commands in RUN-TEST/IDLE state				01	0
Here without significance, because COUNTER1 does not respond to any EVENT input				00	
NULL		0000	0000		
		0	**0**	**1**	**6**

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Write	CONTROL9				
COUNTER2 is loaded with an 0-Level at input EVENT0 (here without significance, since EVENT0 is switched as TMS2 output)					000
COUNTER20 is loaded by COUNTER2 UPDATE0 register					1
COUNTER20 is not loaded at zero passing				0	
COUNTER20 counts leading edges at the input EVENT2				101	
Loading of COUNTER2 takes place with an asynchronous signal at the event input			0		
COUNTER20 and COUNTER21 work as separate 16-bit counters			00		
COUNTER21 is not used		0000	0		
		0	0	A	8

COUNTER1 now is loaded with the number of RUN-TEST/IDLE cycles.

Write	COUNTER1 UPDATE0	0	0	0	9
Write	COUNTER1 UPDATE1	0	0	0	0
Write	MINOR COMMAND	6	0	0	1

COUNTER20 now is loaded with the number of events. For five events, the value (5 – 1) = 4 is to be programmed.

Write	COUNTER1 UPDATE0	0	0	0	4
Write	COUNTER1 UPDATE1	0	0	0	0
Write	MINOR COMMAND	6	0	3	0

MINOR COMMAND and MAJOR COMMAND start the execution of the PRPG/PSA.

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Write	MAJOR COMMAND				
State after executing the command: PAUSE-IR					111
Execution of command in RUN-TEST/IDLE state and suspension of the execution of command in PAUSE-IR state					1
Terminate command at zero passing of COUNTER1				00	
Execution of command is suspended right after the start (SLEEP STATE)				10	
here of no significance, since the process was not interrupted			0		
NULL			000		
MAJOR COMMAND type: EXECUTE command		0010			
		2	**0**	**8**	**F**

Write	MINOR COMMAND				
All Flags are reset					1111
NULL				0	
Immediate start of EXECUTE Command				100	
NULL			0000		
MINOR COMMAND type: Control of test run		0100			
		4	**0**	**8**	**F**

The TBC now waits for five leading edges at the event input of EVENT2. Only then does PRPG/PSA execution begin. After PRPG/PSA has been completed, the control registers must be reset into the standard state.

Write	**CONTROL0**	**0**	**0**	**0**	**0**
Write	**CONTROL3**	**0**	**0**	**8**	**F**
Write	**CONTROL4**	**0**	**7**	**8**	**0**
Write	**CONTROL7**	**0**	**0**	**0**	**0**
Write	**CONTROL8**	**0**	**0**	**0**	**4**
Write	**CONTROL9**	**0**	**0**	**0**	**0**

The result now can be read out, as given in example PRPG/PSA.

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5 Summary

JTAG has developed a coordinated test concept based on boundary-scan techniques, whose specification is embodied in IEEE Std 1149.1. This allows cost-effective testing of complex electronic systems.

When using boundary-scan test methods according to IEEE Std 1149.1, it is necessary to control this test bus with a computer. For this purpose, TI has made available a suitable peripheral component, the TBC SN74ACT8990. If the ASSET development system from TI is used to develop a test program, the computer program supplied programs the TBC.

BIST systems require direct programming of the TBC. Also in this case, the ASSET system and additional translation programs offer easy and flexible programming solutions.

However, if the register of the TBC must be programmed directly, a detailed understanding of this component and methods of programming it are necessary. The examples in this application report make it easier for the user to undertake direct programming of the TBC.

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