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OPERATING MANUAL

MODEL 4259

Dual-Channel T1/CEPT Transceiver
MIX Module for VMEbus Systems

PENTEK

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818-5900

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Pentek Model 4259 Operating Manual
Revision History

Date	Rev	Applicable Serial #'s	Comments
09/02/94	A	9443011- Forward	Initial manual release
10/10/94	A.1	9443011 - Forward	Corrections in Programming Example (Appendix A): (1) In while statement waiting for activation of receive buffers, (pg. A-11) RCMD should be RCMD/2 (2) In init_interrupt function (pg. A-22), 1st statement should be |= rather than simply =.
11/04/96	B	9443011 - Forward	Separate memory maps for each MIX Baseboard. Update MIX Assembly Appendix to Rev. F. Add Tables and Figures to Table of Contents.

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Chapter 1 - General Information

1.1 System Description

The Model 4259 is a dual-channel, full-duplex, Telecommunication Transceiver MIX module for T1 (PCM-24) or CEPT (E1 or PCM-30) signals. High performance PCM line interface logic is followed by frame encoding/decoding options, a Link Layer controller, and dual port RAM.

1.2 Manual Organization

This chapter provides a general introduction to the Model 4259 and the elements that comprise it. It also lists the device's specifications, and includes a block diagram of the circuit. Chapter 2 supplies information about the configuration jumpers on the two circuit boards that the unit contains, gives procedures for separating and rejoining the boards, and describes the unit's front panel and its connectors. Chapter 3 provides the Memory Map for the 4259, and describes the bitwise configuration of the unit's internal registers. Chapter 4 synthesizes the information presented in the earlier chapters, and gives procedures for programming the device.

Appendix A of this manual provides a sample 'C' language program to work with the Model 4259. Appendix B gives a brief description of the MIX interface, and gives procedures for assembling a stack of MIX modules. Appendix C provides some details about Pentek's family of MIX baseboards, and Appendix D describes some significant differences between the Model 4283 baseboard and the rest of our baseboard products.

Proper programming of this device requires that the user develop a deep familiarity with the components used. Toward that end, a Supplementary Manual has been provided, which including data sheets and User's Guides for all the user-programmable devices used in the Model 4259.

1.3 Line Interface Unit and Framer

Two identical and separate subsystems support each full-duplex line. The line interface unit (LIU) mates with separate transmit and receive transformers providing isolation and impedance matching for 75Ω, 100Ω and 120Ω lines.

The LIU (Brooktree Model Bt8069B) extracts and generates clock and data, and interfaces directly with a frame aligner/generator for either T1 (Brooktree Model BtT9170) or CEPT (Brooktree Model BtP9170), specified when the unit is ordered. The frame aligner/generator device is socketed and can be easily replaced in the field with a pin-compatible device supporting the other standard (available as an option).

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1.4 Link Layer Controller

The Link Layer Controller (Brooktree Model Bt8071A) moves data between channel tables (in the 8k x 16 dual-port RAM) and the framer, so that MIX bus Masters can easily address data for each channel. Each time the Link Layer Controller fills or empties a data buffer, it sends an interrupt signal to the Interrupt Queue FIFO, which stores up to 1k entries. MIX bus Masters read the FIFO to determine which tables need to be serviced. The MIX interface can be interrupted each time an entry is made into the queue FIFO.

1.5 Serial Interface

An auxiliary RS-422 differential serial clock and data interface, with FIFO buffering and interrupt generation to the MIX bus, supports general purpose serial I/O.

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1.6 Specifications

PCM Line Connections:

Inputs

Channels:	2
Coupling:	Transformer
Impedance:	Jumper selectable; 75Ω, 100Ω or 120Ω

Outputs

Channels:	2
Coupling:	Transformer
Impedance:	Jumper selectable; 75Ω, 100Ω or 120Ω

Data Rates

T1 (option 001):	1.544 MBytes/sec
CEPT (option 002):	2.048 Mbytes/sec

Connectors: Two 8-pin RJ-45C telephone connectors and two DB-9 serial I/O connectors on front panel (one of each connector for each channel)

Memory (per channel):

Dual Port SRAM

Size:	8k x 16 each
Type:	IDT 7025
Access:	Link Layer Controller (R/W) and MIX bus Masters (R/W)

Interrupt Queue FIFO

Size:	1k x 8
Type:	IDT 7202
Access:	Link Layer Controller (W) and MIX bus Masters (R)

Serial Data Input FIFO

Size:	1k x 8
Type:	IDT 7202
Access:	Input Serial/Parallel Converter (W) and MIX bus Masters (R)

Serial Data Output FIFO

Size:	1k x 8
Type:	IDT 7202
Access:	MIX bus Masters (W) and O/P Parallel/Serial Converter (R)

MIX Interface:

Dual Port SRAM:	Two 8k x 32 regions (one per channel)
Interrupt Queue FIFO:	Two (redundant) 1k x 32 regions (both regions contain interrupt information from both channels)
Serial I/O FIFOs:	Two 1k x 32 regions (one per channel, output FIFO is written in the same address region as input FIFO is read)

Power: 500 mA @ 5 Volts DC, from MIX bus

Dimensions: Occupies one standard 6U VME slot

Height:	8.89"
Depth:	3.75"
Width:	0.80"

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1.7 Block Diagram

A functional block diagram of the Pentek Model 4259 Dual-Channel T1/CEPT Transceiver MIX module for VMEbus systems is presented in Figure 1-1, below.

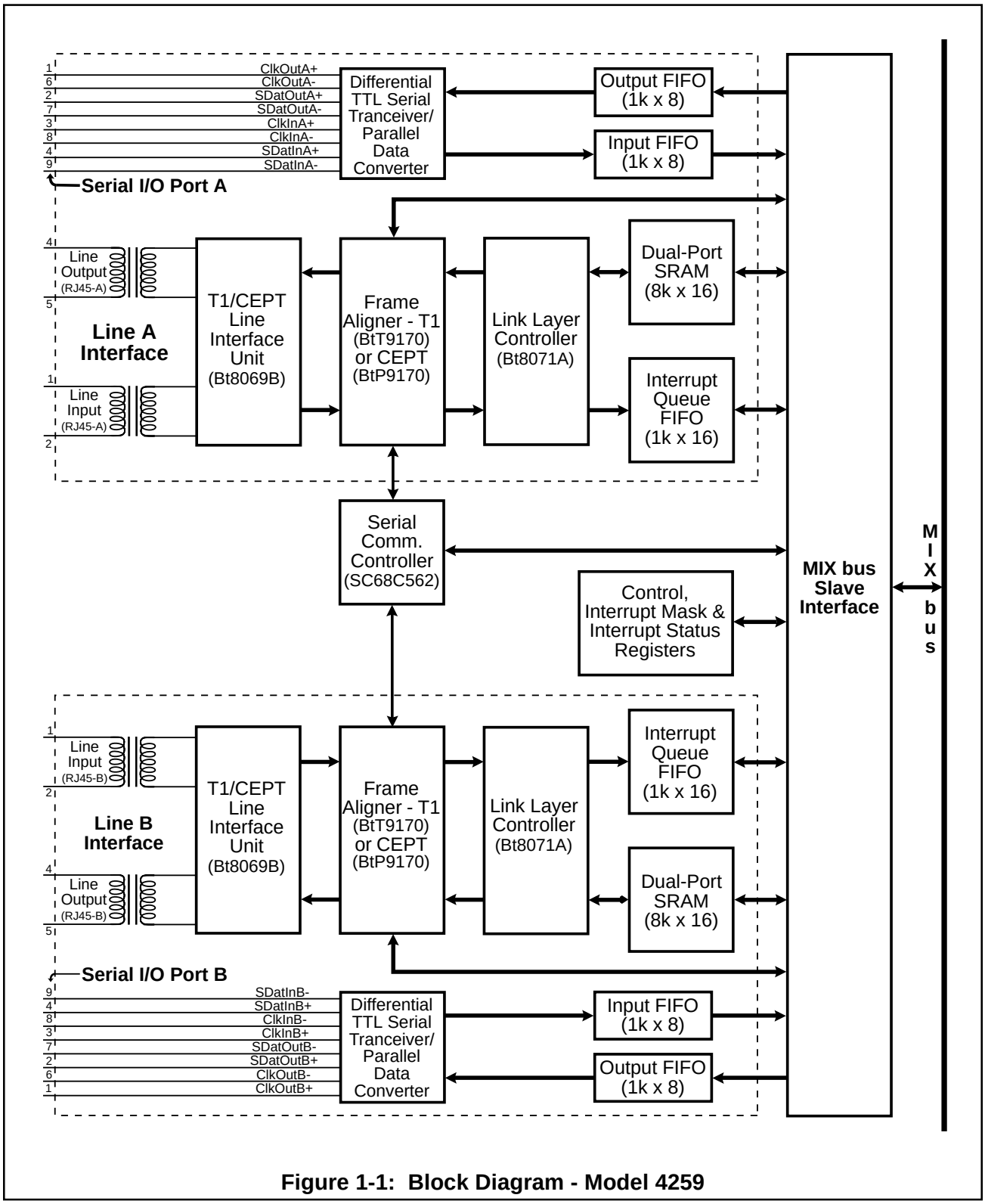


Figure 1-1: Block Diagram - Model 4259

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If you discover any damage, please contact Pentek immediately, at the phone number shown on this manual's title page. Please save the original shipping container and packing material, in case re-shipment is required.

2.2 Jumper Settings

2.2.1 Jumper Block Locations and Functions

On the following pages are drawings of the two circuit boards that comprise the Model 4259, showing the locations of the jumper blocks referred to in the sections below. We refer to the board that contains the MIX bus connector pattern as the MIX board, and the smaller board, mounted on the MIX board, as the Mezzanine board. The MIX board houses the Line A interface, the MIX bus interface, and the Serial Communications Controller. It is shown in Figure 2-2, on the next page. The Mezzanine board, which contains the Line B interface, is shown in Figure 2-3, on the page after next.

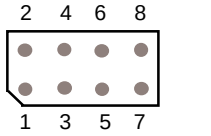


Figure 2-1: Jumper block pin numbering

Figure 2-1, above right, shows the pin numbering for double-row jumper blocks used in the Model 4259. The jumper blocks are used to change the unit's configuration from T1 to CEPT or vice-versa, (the framer chip must also be changed in this conversion) and for CEPT impedance matching. Most of the jumper blocks described in the subsections below are not accessible without separating the two circuit boards. Disassembly and reassembly procedures will be presented in Section 2.3.

NOTE: If you purchased a 4259 Option 001 (T1 configuration), and you never intend to work with CEPT signals, the unit is delivered to you properly configured and **you should never need to change the jumper settings.** Likewise, If you purchased a 4259 Option 002 (CEPT configuration), and you never expect to work with T1 signals or 75Ω CEPT lines, **you should never need to change the jumper settings.**

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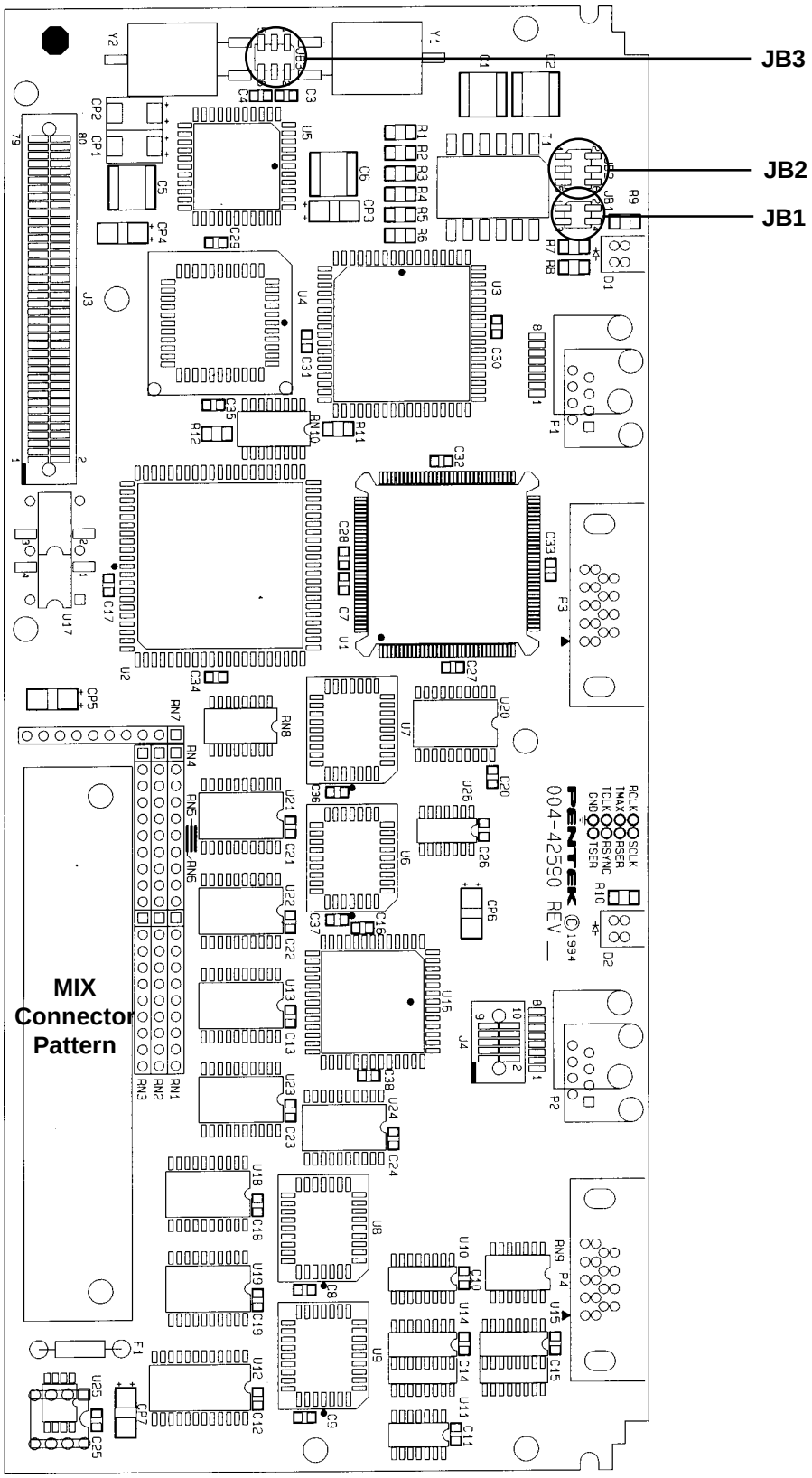


Figure 2-2: Model 4259 MIX board, showing Jumper Block and Connector Locations

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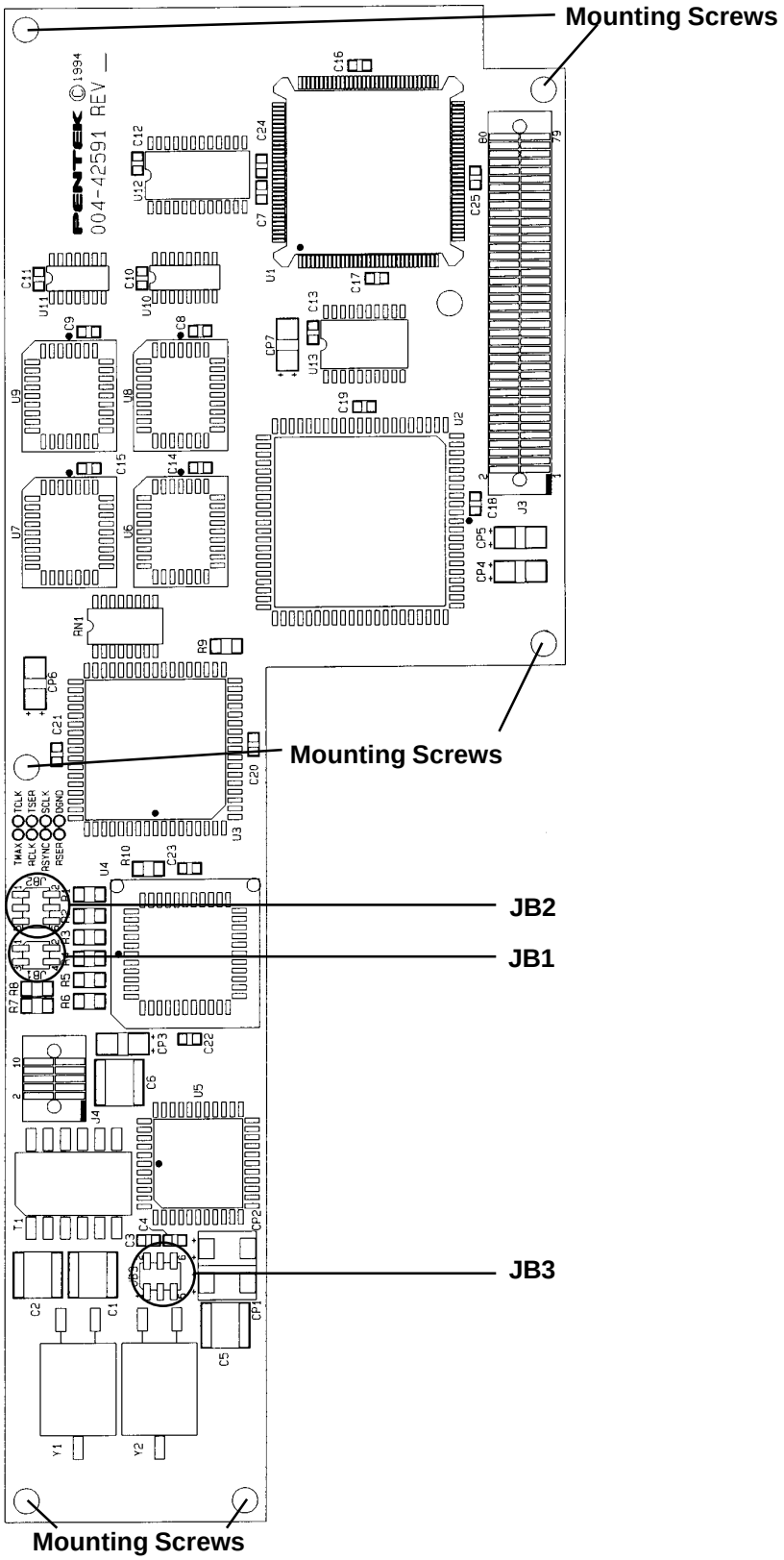


Figure 2-3: Model 4259 Mezzanine board (seen from Component Side), showing Jumper Block, Connector and Mounting Screw Locations

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2.2 Jumper Settings (continued)

2.2.2 Impedance Matching Jumpers - JB1 and JB2, (both boards)

Each channel of the Model 4259 can be configured to drive signals over, and receive signals from, 100Ω T1 lines, 75Ω CEPT lines or 120Ω CEPT lines. Input line impedance matching for line A is accomplished by the setting of jumper block JB1 on the MIX board. Jumper block JB2 on the MIX board is used to match the impedance of Line A's output transformer to your transmission medium. On the Mezzanine board, JB1 is used to match line B's input impedance, and JB2 to match line B's output impedance

For both of the input impedance jumper blocks (JB1 on both boards), a shorting jumper is installed between pins 3 and 4 to match 100Ω T1 lines or 120Ω CEPT lines. This is the default configuration for these jumper blocks. If you will be working with 75Ω CEPT lines, move this jumper such that it is between pins 1 and 2.

For both of the output impedance jumper blocks (JB2 on both boards), a jumper between pins 1 and 2 will provide a suitable output impedance for 100Ω T1 lines. This is the default setting for Option 001. A jumper between pins 3 and 4 will match 120Ω CEPT lines (the Option 002 default), and a jumper between pins 5 and 6 will match 75Ω CEPT lines.

Table 2-1, below, summarizes the usage and settings of the impedance matching jumper blocks.

Table 2-1: Model 4259 - Impedance Matching Jumpers - JB1 and JB2 (both boards)

Line (Board)	Jumper Block (Side)	Line Impedance	Pins
Line A (MIX board)	JB1 (Zin)	75Ω (CEPT)	1 - 2
		100Ω(T1) or 120Ω (CEPT)	3 - 4*†
	JB2 (Zout)	100Ω(T1)	1 - 2*
		120Ω (CEPT)	3 - 4†
		75Ω (CEPT)	5 - 6
Line B (Mezzanine board)	JB1 (Zin)	75Ω (CEPT)	1 - 2
		100Ω(T1) or 120Ω (CEPT)	3 - 4*†
	JB2 (Zout)	100Ω(T1)	1 - 2*
		120Ω (CEPT)	3 - 4†
		75Ω (CEPT)	5 - 6

* - default setting, option 001

† - default setting, option 002

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2.2 Jumper Settings (continued)

2.2.3 Internal Oscillator Frequency Selection - JB3 (both boards)

The next configuration step is the selection of the internal crystal oscillator frequency. The Line Interface Unit (LIU - 8069B) divides the selected crystal frequency by a factor of 4 to arrive at the data rate of the selected standard. Thus, for T1, a 6.176 MHz crystal is used to derive the 1.544 MByte/sec data rate, and the CEPT rate of 2.048 MByte/sec is derived from an 8.192 MHz crystal. One of each of these crystals is installed on each of the 4259's circuit boards. A jumper block, JB3, is provided on each card to select one of the two crystals. Two jumpers must be installed on each block to accomplish this selection. JB3 on the MIX board selects the crystal for line A, and JB3 on the Mezzanine board selects the crystal for line B.

On either card, jumpers on JB3 between pins 1 - 3 and pins 2 - 4 will select the 6.176 MHz crystal, for the 1.544 MByte/sec T1 data rate (this is the default setting for option 001). Jumpers in JB3 between pins 4 - 6 and pins 3 - 5 will select the 8.192 MHz crystal, for the 2.048 CEPT data rate (this is the default setting for option 002).

Table 2-2, below, summarizes the settings of the internal oscillator frequency selection jumper blocks.

Table 2-2: Model 4259 - Internal Oscillator Frequency Selection Jumpers - JB3 (both boards)

Line (Board)	Oscillator Frequency	Data Rate	Pins
Line A (MIX board)	6.176 MHz	1.544 MB/sec (T1)	1 - 3 & 2 - 4 *
Line B (Mezz. board)	8.192 MHz	2.048 MB/sec (CEPT)	1 - 3 & 2 - 4 †

* - default setting, option 001

† - default setting, option 002

2.3 Disassembly and Assembly Procedures

If it turns out that you need to re-configure any or all of the jumpers described in the previous section, it may first be necessary to separate the two circuit boards. Only jumper blocks JB1 and JB2 on the MIX board can be accessed without separating the boards. Procedures for separating and re-attaching the two cards are given in the subsections below.

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2.3 Disassembly and Assembly Procedures (continued)

CAUTION!!

Perform all assembly steps in a static controlled work environment.

2.3.1 Detaching the Mezzanine Board from the MIX Board

The Mezzanine board is mechanically secured to the MIX board by means of six nylon screws. These screws may either be of the Philips- or slotted-head variety. The screw locations are shown in Figure 2-3, on page 11 of this manual. Remove all 6 of these screws and set them aside for use when reassembling the unit.

The electrical connection between the two boards is accomplished by means of two multi-contact connector blocks, J3 (80 pins, at the rear of the unit) and J4 (10 pins, at the front, just behind the Line B I/O connector). The locations of these connectors are shown in Figures 2-2 and 2-3, on pages 10 and 11 of this manual. After the screws are removed, the boards may be separated at these connectors as follows.

To disconnect J3, lay the unit down on your work surface with the Mezzanine board up with the MIX connector pattern nearest you. Place your index fingers just outside the two nylon spacers that support the Mezzanine board, and **gently** push up on the rear edge of the mezzanine board with your thumbs until the J3 connectors disengage. To disconnect J4, grasp the narrow portion of the mezzanine board, in the area of the front panel Line B I/O connector, and **gently** lift straight up. This completes the separation of the boards.

2.3.2 Connecting the Mezzanine Board to the MIX Board

After you have made the necessary changes to the jumper configurations on the two boards (see Section 2.2 for details), you are ready to reassemble the unit. The multi-pin connectors on the Mezzanine board are enclosed in a plastic shroud that serves the dual purpose of protecting the pins from damage and keying the connectors to prevent misalignment. Starting with the J3 connectors (the larger ones, at the rear), align the boards such that the shrouds on the mezzanine board completely overlap the socket blocks on the MIX board. Press down **gently** until the connectors are fully seated. Next, check the alignment of the J4 connectors (the small ones, at the front), and again press down **gently** until the connectors are fully seated. Finally, secure the boards by replacing the six nylon screws. This completes the assembly procedure.

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2.4 Model 4259 Front Panel

Figure 2-4, at the right, shows the layout of the Model 4259's front panel. The panel contains a telephone I/O connector, a serial I/O port connector, and a Red Alarm LED for each line. Line A's connectors and indicator occupy the top half of the panel, and Line B's connectors and indicator are on the bottom half. Each of these items will be discussed in detail in the subsections below.

2.4.1 Telephone I/O Connectors

A standard 8-wire RJ45C telephone socket is provided for each of the phone I/O lines on the Model 4259. The sockets are located below the labels T1/CEPT LINE A and T1/CEPT LINE B. As Figure 2-4 (at the right) indicates, pin 1 is at the bottom of each connector, and pin 8 is at the top. Pin 1 of these is connected to the positive side of the input transformer, and pin 2 is connected to the negative side of the input transformer. Pin 4 is connected to the positive side of the output transformer, and pin 5 is connected to the negative side of the output transformer. All other pins are open. Table 2-3, below, summarizes the pinout of the telephone line I/O connectors.

Table 2-3: Model 4259 - Phone Line I/O (RJ45C) Connector Pinout

Pin #	Connection	Pin #	Connection
1	Receive +	4	Transmit +
2	Receive -	5	Transmit -
Pins 3, 6, 7 and 8 are open			

Table 2-4: Model 4259 - Serial I/O Connector Pinout

Pin #	Connection	Pin #	Connection
1	Serial Clock Out +	6	Serial Clock Out -
2	Serial Data Out +	7	Serial Data Out -
3	External/Serial Clock In +	8	External/Serial Clock In -
4	Serial Data In +	9	Serial Data In -
When using pins 3 or 8 as a single-ended, External Clock input for the Line Interface, use pin 5 as the ground reference.			

2.4.2 Serial I/O Ports

A standard DB-9 connector provides access to the Differential Serial (RS-422) I/O port in each channel of the Model 4259. These connectors are located beneath the labels EXT CLK A - TTL I/O A and EXT CLK B - TTL I/O B. As Figure 2-4 (at the right) indicates, Pins 1 is at the lower left-hand corner of each connector, with pins 1-5 on the left and pins 6 - 9 are on the right, with pin 9 in the upper right-hand corner.

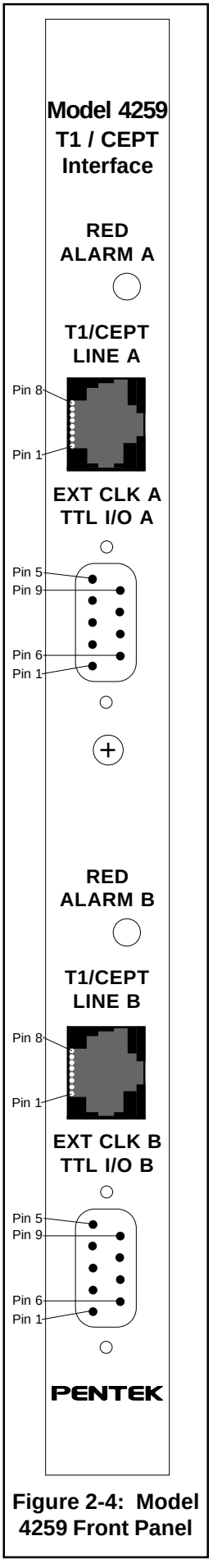


Figure 2-4: Model 4259 Front Panel

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2.4 Model 4259 Front Panel (continued)

2.4.2 Serial I/O Ports (continued)

The differential serial clock output is connected between pins 1 and 6, with the positive signal at pin 1 and the negative at pin 6. The differential serial data stream is connected between pins 2 and 7, with pin 2 carrying the true signal and pin 7 the complement. Differential serial input data is delivered to pins 4 and 9 of this connector, the true signal to pin 4 and the complement to pin 9.

Pins 3 and 8 of these connectors serve a dual input function, depending upon the programming of the device. They may either be used as the differential input clock for serial input stream (positive signal to pin 3, negative to pin 8) or as an external clock input for the phone line interface. When used as the phone line clock, either polarity signal may be delivered to the connector, single-ended, using pin 5 as the ground reference. When used in this manner, the signal applied here should be close to a 50% duty cycle. Use of this feature is programmed in the Link Layer Control register, at MIX address offset 0x0004 0000. See Section 3.4 for further details.

The connections available on these connectors are summarized in Table 2-4, on the previous page.

2.4.3 Line Status/Alarm LED Indicators

Both phone lines on the Model 4259 are equipped with a line status LED indicator. These front panel indicators are labeled RED ALARM A and RED ALARM B, and light to indicate that a given line is either unconnected, out of sync, or that some other problem exists for the line in question. When the line interface is functioning properly, the LED will be turned off.

2.5 Installing the Model 4259 on a MIX Baseboard

For MIX module stack assembly procedures and other important information about Pentek's family of MIX expansion modules, please refer to Appendix B of this manual.

2.6 Installing the Assembly in the VMEbus Card Cage

Appendix B of this manual also covers the installation of the assembled MIX Module stack in the VME card cage.

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Chapter 3: Memory Maps and Register Descriptions

3.1 Programming Overview

The following sections cover access to the Model 4259 from the MIX Baseboard and the issuing of commands for module control and data transfers. There are two cases to be considered, dependent upon the type of Baseboard used. This chapter gives details for Baseboards that use direct MIX addressing, such as Pentek's Models 4200, 4200A, 4201, 4201A, 4202 and 4284. General information on the use of these Baseboards is given in Appendix C. Appendix D gives general information on access to MIX modules from Baseboards that use an Address Page Register, such as Pentek's Model 4283. The Memory Map for the Model 4283 is also included in this chapter.

3.2 Address Maps

The sections below will present address maps for the resources available on the Model 4259, for each type of MIX Baseboard available from Pentek. Each of the eighteen resources will be assigned a symbolic name, by which that resource will be referred to in subsequent sections of the manual. There are four cases to consider, each of which is covered in a separate section.

If the Baseboard you will be using is a Model 4200, 4200A, 4201 or 4201A, use the address map presented in Section 3.2.1. If you will be using your Model 4259 with a Model 4202 Baseboard, use the address map in section 3.2.2. If the Model 4283 will be the MIX Baseboard for your Model 4259, skip to Section 3.2.3, and use the address map found there. Finally, if your 4259 will be mounted on a Model 4284 Baseboard, use the address map in Section 3.2.4.

By convention, the MIX addresses given in this manual are generally given as 8-digit hexadecimal codes, with a space between the first and second four digits, simply for notational convenience. The form is MIX_base+0xYYYY ZZZZ. The leading '0x' is common notation for a hex value in the 'C' programming language.

Since each hex digit represents 4 bits, the 8-digit MIX address represents 32 bits of address. The MIX_base part of the address is dependent upon the Baseboard in use, and is used to select each module by its stack position. This geographical addressing scheme avoids the need for address jumpers and possible conflicts, but requires that software must accommodate the physical placement of modules in the MIX stack.

The exception to this convention will be for the Model 4283 Baseboard, whose TMS320C30 processor only has a 24-bit address bus on the port it uses for the MIX bus. In this case, a page register is used for module selection (as opposed to different base addresses for each module), and the addresses are given as 6-digit hexadecimal codes, of the form 0xYY ZZZZ.

A final point must now be made about MIX nomenclature. Module 0 (or MIX position 0) refers to the closest module to the Baseboard, whether or not it is nested. Module 1 (or MIX position 1) is the module that may be mounted above Module 0, and Module 2 is the device that may be stacked above Module 1.

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3.2 Address Map (continued)

3.2.1 Model 4259 Address Map for the 4200/01 Series Baseboards

Pentek's Models 4200 and 4201 Baseboards use a 16 MHz 68030 processor as the MIX bus controller. The 4200A and 4201A use a 40 MHz 68030. From the 68030's viewpoint, the MIX bus is mapped identically for all four of these Baseboards. The MIX_base address for Module 0 (which may either be nested, sharing the Baseboard's VMEbus slot, or stacked in the adjacent VMEbus slot), is 0xC000 0000. For the next device in the stack, Module 1, the base address is 0xD000 0000. Finally for the last MIX Module in the stack, Module 2, the MIX_base address is 0xE000 0000. Table 3-1, below, gives the physical addresses, in the memory space of the 68030 processor on any of these four Baseboards, that correspond to the symbolic names used to represent the Model 4259's resources in subsequent sections of this manual.

Table 3-1: Model 4259 - Memory Map for Use with Models 4200, 4200A, 4201 and 4201A MIX Baseboards- 68030 View

4200/01 68030 Address	Symbolic Name	Resource
MIX_base+0x0000 0000 - MIX_base+0x0000 00FC	DPR_Buff_A	Dual Port RAM System Buffer A
MIX_base+0x0000 0100 MIX_base+0x0000 1FFC	DP_RAM_A	User Dual Port RAM A
MIX_base+0x0004 0000	LLC_Reg*	Link Layer Control Register
MIX_base+0x0008 0080	Fmr_LIU_A	Framer/LIU A
MIX_base+0x000C 0000	Srl_P_Ctl*	Serial Port Communication Controller
MIX_base+0x0010 0000	Int_Q_FIFO	Interrupt Queue FIFO (Read Only Access)
MIX_base+0x0014 0000	Int_Mask_Reg*	Interrupt Mask/Enable Register
MIX_base+0x0018 0000	Int_Stat_Reg*	Interrupt Status Register (Read Only Access)
MIX_base+0x001C 0000	Srl_FIFO_A	Serial Data FIFO A
MIX_base+0x0800 0000 - MIX_base+0x0800 00FC	DPR_Buff_B	Dual Port RAM System Buffer B
MIX_base+0x0800 0100 - MIX_base+0x0800 1FFC	DP_RAM_B	User Dual Port RAM B
MIX_base+0x0804 0000	LLC_Reg*	Link Layer Control Register
MIX_base+0x0808 0080	Fmr_LIU_B	Framer/LIU B
MIX_base+0x080C 0000	Srl_P_Ctl*	Serial Port Communication Controller
MIX_base+0x0810 0000	Int_Q_FIFO	Interrupt Queue FIFO (Read Only Access)
MIX_base+0x0814 0000	Int_Mask_Reg*	Interrupt Mask/Enable Register
MIX_base+0x0818 0000	Int_Stat_Reg*	Interrupt Status Register (Read Only Access)
MIX_base+0x081C 0000	Srl_FIFO_B	Serial Data FIFO B

MIX_base Address:

If 4259 is in MIX position 0, MIX_base = 0xC000 0000

If 4259 is in MIX position 1, MIX_base = 0xD000 0000

If 4259 is in MIX position 2, MIX_base = 0xE000 0000

* - Dual-Mapped resources - identical register is accessed at either of the listed addresses

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3.2 Address Map (continued)

3.2.1 Model 4259 Address Map for the 4200/01 Series Baseboards (continued)

Note that the 4200 series of VME/MIX Baseboards also support mastering of the MIX bus by Upper MIX Bus Masters (UMBMs), and by VMEbus Masters. For further information about MIX Bus access on these Baseboards in this manner, please refer to Appendix C of this manual (the MIX Baseboard Tutorial), or to the Baseboard's or UMBM's Operating Manual.

3.2.2 Model 4259 Address Map for the Model 4202 Baseboard

Table 3-2: Model 4259 - Memory Map for Use with the Model 4202 MIX Baseboard

VMEbus Address	Symbolic Name	Resource
MIX_base+0x0000 0000 - MIX_base+0x0000 00FC	DPR_Buff_A	Dual Port RAM System Buffer A
MIX_base+0x0000 0100 MIX_base+0x0000 1FFC	DP_RAM_A	User Dual Port RAM A
MIX_base+0x0004 0000	LLC_Reg*	Link Layer Control Register
MIX_base+0x0008 0000	Fmr_LIU_A	Framer/LIU A
MIX_base+0x000C 0000	Srl_P_Ctl*	Serial Port Communication Controller
MIX_base+0x0010 0000**	Int_Q_FIFO	Interrupt Queue FIFO (Read Only Access)
MIX_base+0x0014 0000**	Int_Mask_Reg*	Interrupt Mask/Enable Register
MIX_base+0x0018 0000**	Int_Stat_Reg*	Interrupt Status Register (Read Only Access)
MIX_base+0x001C 0000**	Srl_FIFO_A	Serial Data FIFO A
MIX_base+0x0800 0000 - MIX_base+0x0800 00FC†	DPR_Buff_B	Dual Port RAM System Buffer B
MIX_base+0x0800 0100 - MIX_base+0x0800 1FFC†	DP_RAM_B	User Dual Port RAM B
MIX_base+0x0804 0000†	LLC_Reg*	Link Layer Control Register
MIX_base+0x0808 0000†	Fmr_LIU_B	Framer/LIU B
MIX_base+0x080C 0000†	Srl_P_Ctl*	Serial Port Communication Controller
MIX_base+0x0810 0000†,**	Int_Q_FIFO	Interrupt Queue FIFO (Read Only Access)
MIX_base+0x0814 0000†,**	Int_Mask_Reg*	Interrupt Mask/Enable Register
MIX_base+0x0818 0000†,**	Int_Stat_Reg*	Interrupt Status Register (Read Only Access)
MIX_base+0x081C 0000†,**	Srl_FIFO_B	Serial Data FIFO B

Default MIX_base Address:

If 4259 is in MIX position 0, MIX_base = 0x0000 0000 for A32, or 0x00 0000 for A24

If 4259 is in MIX position 1, MIX_base = 0x1000 0000 for A32, or 0x10 0000 for A24

If 4259 is in MIX position 2, MIX_base = 0x2000 0000 for A32, or 0x20 0000 for A24

* - Dual-Mapped resources - identical register is accessed at either of the listed addresses

† - Paged Addressing Mode must be used to access these registers (D7 in Control Reg = 1) in A24 space

** - MXA23 - MXA20 correspond to D7 - D4 in High Page Register, Module selected by D13 - D12

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3.2 Address Map (continued)

3.2.2 Model 4259 Address Map for the Model 4202 Baseboard (continued)

The Model 4202 is a VMEbus slave-only Baseboard, and contains no processor. This device maps the resources connected to its MIX Bus into VMEbus A32, A24 or A16 slave address space. The VMEbus A32 or A24 base address is programmed into a register in the 4202's A16 interface by a VMEbus Master (the A16 base address is set by switches on the board). This register is cleared at power-up, resulting in a default base address of 0x0000 0000 in A32 space, or 0x00 0000 in A24 space.

In direct addressing mode, the two most significant bits of the VMEbus address (i. e., A31 and A30 in A32 space, A23 and A22 in A24 space or A15 and A14 in A16 space) select a particular 4202 Baseboard, by comparison with the two Least Significant Bits (D1 and D0) of the VMEbus Address Register. The next two VMEbus address bits (i. e., A29 and A28 in A32 space, A21 and A20 in A24 space, or A13 and A12 in A16 space) select among the MIX modules stacked on the 4202. Thus, assuming A32 operation and that the VMEbus Address Register is NOT written to, the MIX_base address for Module 0 is 0x0000 0000. Making the same assumptions, Module 1's MIX_base address is 0x1000 0000 and the MIX_base address for Module 2 is 0x2000 0000.

Table 3-2, at the previous page, presents the memory map for a Model 4259 installed on a Model 4202 Baseboard, assuming direct addressing, A32 or A24 operation, and that nothing has been written to the 4202's VME Address Register. For information about using the Model 4202's Paged Addressing Mode, A16 MIX access, multiple 4202's in the same card cage or Upper MIX Bus Masters, please refer to the Operating Manual for the Model 4202 Baseboard or the UMBM.

3.2.3 Model 4259 Address Map for the Model 4283 Baseboard

On the Model 4283 Baseboard, there are two levels of addressing: 1) selection of the particular expansion module by its stack position and 2) selection of one of the resources within the module.

3.2.3.1 Module Selection

The TMS320C30 selects among MIX Modules by using a two bit field in the Model 4283 Page Register, located at 'C30 address 0x80 0002. These two bits select one of the three possible MIX stack positions according to Table 3-3, on the next page.

Access to some resources on certain MIX modules may require that either or both of the MIX bus A27 (MX_A27) and A21 (MX_A21) bits be set to the logic '1' state. On the 4283 baseboard, these bits are also contained in the Address Page Register. MX_A27 is the D17 bit of this register, and MX_A21 is the D14 bit. Table 3-3 also shows these bits.

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3.2 Address Map (continued)

3.2.3 Model 4259 Address Map for the Model 4283 Baseboard (continued)

Table 3-3: Model 4259 - Module Selection - Model 4283 Page Register - 'C30 Address 0x80 0002							
Page Register Bits>	**D31 - D18**	**D17**	**D16**	**D15**	**D14**	**D13 - D0**	**Example**
Stack Position 0	x	MXA27	1	1	MXA21	x	0x01 8000
Stack Position 1	x		1	0		x	0x01 0000
Stack Position 2	x		0	1		x	0x00 8000
x = other functions							

3.2.3.2 Register Selection Within the Module

Table 3-4: Model 4259 - Memory Map for Use with the Model 4283 MIX Baseboard		
4283 'C30 Address	**Symbolic Name**	**Resource**
0x80 4000 - 0x80 403F	DPR_Buff_A	Dual Port RAM System Buffer A
0x80 4040 - 0x80 47FF	DP_RAM_A	User Dual Port RAM A
0x80 4000[A]	LLC_Reg*	Link Layer Control Register
0x80 4000[B]	Fmr_LIU_A	Framer/LIU A
0x80 4000[C]	Srl_P_Ctl*	Serial Port Communication Controller
0x80 4000[D]	Int_Q_FIFO	Interrupt Queue FIFO (Read Only Access)
0x80 4000[E]	Int_Mask_Reg*	Interrupt Mask/Enable Register
0x80 4000[F]	Int_Stat_Reg*	Interrupt Status Register (Read Only Access)
0x80 4000[G]	Srl_FIFO_A	Serial Data FIFO A
0x80 4000 - 0x80 403F[††]	DPR_Buff_B	Dual Port RAM System Buffer B
0x80 4040 - 0x80 47FF[††]	DP_RAM_B	User Dual Port RAM B
0x80 4000[††,A]	LLC_Reg*	Link Layer Control Register
0x80 4000[††,B]	Fmr_LIU_B	Framer/LIU B
0x80 4000[††,C]	Srl_P_Ctl*	Serial Port Communication Controller
0x80 4000[††,D]	Int_Q_FIFO	Interrupt Queue FIFO (Read Only Access)
0x80 4000[††,E]	Int_Mask_Reg*	Interrupt Mask/Enable Register
0x80 4000[††,F]	Int_Stat_Reg*	Interrupt Status Register (Read Only Access)
0x80 4000[††,G]	Srl_FIFO_B	Serial Data FIFO B

* - Dual-Mapped resources - identical register is accessed at either of the listed addresses

[A - F] - Locations selected by (D13, D12, D11) in Page Register as follows:

[A] - (D13, D12, D11) = (0,0,1) [B] - (D13, D12, D11) = (0,1,0) [C] - (D13, D12, D11) = (0,1,1)

[D] - (D13, D12, D11) = (1,0,0) [E] - (D13, D12, D11) = (1,0,1) [F] - (D13, D12, D11) = (1,1,0)

[G] - (D13, D12, D11) = (1,1,1)

[††] - D17 in Page Register = 1

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3.2 Address Map (continued)

3.2.3 Model 4259 Address Map for the Model 4283 Baseboard (continued)

3.2.3.2 Register Selection Within the Module (continued)

Once the module has been selected, all resources (including the RAM Banks) of the Model 4259 appear in the TMS320C30 address map according to Table 3-4, at the previous page. Accessing these registers is accomplished by simply reading and writing these locations.

The 24-bit addressing scheme accesses 32-bit data locations for the TMS320C30, even though many of the elements correspond to 8-bit or 16-bit devices.

3.2.4 Model 4259 Address Map for the Model 4284 Baseboard

The Model 4284 Baseboard uses a TMS320C40 Digital Signal Processor to master transactions with the MIX bus. The three MIX module locations are each mapped into separate, 64 M-Longword regions of the 'C40's memory space. Module 0's MIX_base address in the 'C40 memory map is 0x2000 0000. The MIX_base address for Module 1 is 0x2400 0000, and the 'C40's MIX_base address for Module 2 is 0x2800 0000. Table 3-5, on the next page, presents the memory map for the eighteen resources on the Model 4259, as seen by the 'C40 processor on the Model 4284 Baseboard.

This Baseboard also supports mastering of the MIX bus by processor modules in the MIX stack, known as UMBM's (Upper MIX Bus Masters). For further details on this type of transaction, please refer to Appendix C of this manual (MIX Baseboard Tutorial), the Model 4284 Operating Manual, or the UMBM's Operating Manual.

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3.2 Address Map (continued)

3.2.3 Model 4259 Address Map for the Model 4284 Baseboard (continued)

Table 3-5: Model 4259 - Memory Map for Use with the Model 4284 MIX Baseboard

4284 'C40 Address	Symbolic Name	Resource
MIX_base+0x0000 0000 - MIX_base+0x0000 003F	DPR_Buff_A	Dual Port RAM System Buffer A
MIX_base+0x0000 0040 MIX_base+0x0000 07FF	DP_RAM_A	User Dual Port RAM A
MIX_base+0x0001 0000	LLC_Reg*	Link Layer Control Register
MIX_base+0x0002 0000	Fmr_LIU_A	Framer/LIU A
MIX_base+0x0003 0000	Srl_P_Ctl*	Serial Port Communication Controller
MIX_base+0x0004 0000	Int_Q_FIFO	Interrupt Queue FIFO (Read Only Access)
MIX_base+0x0005 0000	Int_Mask_Reg*	Interrupt Mask/Enable Register
MIX_base+0x0006 0000	Int_Stat_Reg*	Interrupt Status Register (Read Only Access)
MIX_base+0x0007 0000	Srl_FIFO_A	Serial Data FIFO A
MIX_base+0x0200 0000 - MIX_base+0x0200 003F	DPR_Buff_B	Dual Port RAM System Buffer B
MIX_base+0x0200 0040 - MIX_base+0x0200 07FF	DP_RAM_B	User Dual Port RAM B
MIX_base+0x0201 0000	LLC_Reg*	Link Layer Control Register
MIX_base+0x0202 0000	Fmr_LIU_B	Framer/LIU B
MIX_base+0x0203 0000	Srl_P_Ctl*	Serial Port Communication Controller
MIX_base+0x0204 0000	Int_Q_FIFO	Interrupt Queue FIFO (Read Only Access)
MIX_base+0x0205 0000	Int_Mask_Reg*	Interrupt Mask/Enable Register
MIX_base+0x0206 0000	Int_Stat_Reg*	Interrupt Status Register (Read Only Access)
MIX_base+0x0207 0000	Srl_FIFO_B	Serial Data FIFO B

MIX_base Address:

If 4259 is in MIX position 0, MIX_base = 0x2000 0000

If 4259 is in MIX position 1, MIX_base = 0x2400 0000

If 4259 is in MIX position 2, MIX_base = 0x2800 0000

* - Dual-Mapped resources - identical register is accessed at either of the listed addresses

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3.3 **Dual Port SRAM**- Read/Write @ MIX_base+0x0000 0000 (Line A) and MIX_base+0x0800 0000 (Line B)

The Model 4259 contains two 8k x 16 banks of Dual Ported SRAM, one bank per line interface. Although this memory is 16 bits wide, it is mapped on 32 bit word addresses, to facilitate MIX access. This resource is used together with the Link Layer controller to create the link buffers.

The system buffer for line A starts at MIX address offset 0x0000 0000 (attention byte) and goes to offset 0x0000 00FF (see Link Layer Controller (Bt8071A) data sheet, in Chapter 3 of the Supplementary Manual supplied with your unit, and the Application Note on programming that part in Chapter 4 of the Supplement). For line B, the system buffer extends from MIX offset 0x0800 0000 to MIX offset 0x0800 00FF. The transmit and receive command and data buffers can be linked in the rest of memory. These reside in the region from MIX address offset 0x0000 0100 to MIX address offset 0x0000 1FFF for line A, and from MIX offset 0x0800 0100 to MIX offset 0x0800 1FFF for line B.

NOTE: The user should not access Dual Port RAM Addresses 0x0000 0003 or 0x0000 0004 in line A, or Addresses 0x0800 0003 or 0x0800 0004 in line B, until the Link Layer controller is activated. Doing so will result in either a MIX bus timeout or a lockup.

3.4 **Link Layer Control Register** - Read/Write @ MIX_base+0x0004 0000

The Link Layer Control Register controls the Link Layer Controller and the serial port. It also provides the channel resets. The upper 8 bits control Channel B and the lower 8 bits control Channel A. Table 3-6, below, defines the bit structure of this register. The following subsections describe the functions of the register's bits. This register may also be accessed at address MIX_base+0x0804 0000.

Table 3-6: Model 4259 - Link Layer Control Register - Read/Write @ MIX_base + 0x0004 0000

D15	D14	D13	D12	D11	D10	D9	D8
'1' = Line B Attention	'1' = Line B Reset	'1' = Serial Port B Enable	Serial Clock B Polarity (1=↑)	B Memory Fmt (1=Mot.)	Line B T1/$\overline{\text{CEPT}}$	Line B HCS1	Line B HCS0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
'1' = Line A Attention	'1' = Line A Reset	'1' = Serial Port A Enable	Serial Clock A Polarity (1=↑)	A Memory Fmt (1=Mot.)	Line A T1/$\overline{\text{CEPT}}$	Line A HCS1	Line A HCS0

3.4.1 **Attention Bits** - Bits D15 and D7

These bits activate the attention pulse to the 8071A Link Layer Controller. The user sets the bit to the '1' state and waits for it to return to the '0' state. The bit should not be set until the required data has been entered in the Dual Port RAM. See the application note "Programming the 8071 ISDN/DMI Link Layer Controller's Buffers". Bit D15 is the Attention bit for line B, and bit D7 is the Attention bit for line A.

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3.4 Link Layer Control Register (continued)

3.4.2 Line Interface Reset Bits - Bits D14 and D6

These bits are used to reset the individual channels. The bit is set to the '1' state by the user and will return to the '0' state after the reset is complete. Bit D14 resets the line B interface, and bit D6 resets the line A interface.

3.4.3 Serial Port Enable/External Clock Disable - Bits D13 and D5

When the user wishes to use a given channel's differential TTL serial port, this bit must be set to the '1' state. While the bit is a '1', the port's external clock input may not be used to drive the T1/CEPT LIU (see the Bt8069B data sheet, in Chapter 1 of the Supplementary Manual supplied with the Model 4259).

If, on the other hand, the user needs to drive a given line's LIU from the external clock input, this bit should be cleared to the '0' state. The external signal applied to the clock input pins (see Section 2.4.2 for connection details) should be close to a 50% duty cycle when used to clock the LIU. While the bit is a '0', the Serial I/O port is disabled.

Bit D5 controls this function in Channel A, and bit D13 makes the selection for Channel B.

3.4.4 Serial Clock Polarity - Bits D12 and D4

When a given channel's Serial I/O port is enabled (i. e., when D5 or D13 is set to the '1' state, see Section 3.4.3, above), this bit is used to select the clock edge used to latch bits from the incoming data stream, and to validate the transmitted bits. The user should clear this bit to the '0' if the incoming and outgoing data is to be valid on the falling edge of the external clock signal. It should be set to the '1' state if the data will be valid on the rising edge of the clock. Bit D4 selects the clock polarity for Channel A, and bit D12 makes the selection for Channel B.

3.4.5 Memory Data Format Select - Bits D11 and D3

The Link Layer Controller can be programmed to read data placed in the Dual Port RAM by either Motorola- or Intel-type processors. Motorola-type processors will write the LSB of a data word in bits D15 - D8 of an SRAM address, and the MSB in bits D7 - D0. Intel processors place the LSB in bits D7 - D0, and the MSB in bits D15 - D8.

Clear this bit to the '0' state to make the Link Layer Controller look for the LSB in the lower half of the 16 bit word in Dual Port Memory and MSB in the upper 8 bits (Intel format). If this bit is set to the '1' state, the controller looks for the LSB in the upper 8 bits and the MSB in the lower 8 bits of the Dual Port RAM (Motorola format). Bit D3 controls this feature for Channel A, and bit D11 is used for Channel B.

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3.4 Link Layer Control Register (continued)

3.4.6 T1/$\overline{\text{CEPT}}$ Select - Bits D10 and D2

Setting this bit to the '1' state selects the T1 framing mode for the Link Layer Controller (Bt8071A). If the bit is cleared to the '0' state, it will select the CEPT (PCM30) mode. Bit D2 selects the framing mode for Channel A, and bit D10 makes the selection for Channel B.

3.4.7 Hyperchannel Select - Bits D9 & D8, and D1 & D0

These bits are used to dynamically group individual 64 kbps channels into hyperchannels, allowing the user to allocate bandwidth according to channel requirements. The T1/CEPT select bits (D10 and D12, see Section 3.4.6, above) are also involved in programming the hyperchannel configuration. Table 3-7, below, describes the hyperchannel configuration as a function of the bit settings. See the data sheet and programming note for the Model 8071A Link Layer Controller (in Appendices D and E of this manual, respectively), for more information about the use and programming of the hyperchannel features. Bits D1 & D0 are used to program the hyperchannel mode for Channel A, and bits D9 & D8 are used for Channel B.

Table 3-7: Model 4259 - Hyperchannel Select Bits - Link Layer Control Register - Read/Write @ MIX_base+0x0004 0000

T1/$\overline{\text{CEPT}}$ (D10 or D2)	Hyperchannel Select 1 (D9 or D1)	Hyperchannel Select 0 (D8 or D0)	Channel Selection
x	0	0	All channels are 64 Kbps
1	1	0	Four channels of 384 Kbps (H0)
1	0	1	Single channel of 1.536 Mbps (H11)
0	1	0	Single channel of 1.92 Mbps (H12)
x	1	1	Not valid (reserved)
0	0	1	Not valid (reserved)
For Line B, use D10, D9 and D8 - For Line A, use D2, D1 and D0			

3.5 Frame Aligner and Line Interface Unit - Read/Write @ MIX_base+0x0008 0000 (Line A) and MIX_base+0x0808 0000 (Line B)

See the spec sheets for the BtT9170 (T1 Frame Aligner) or BtP9170 (CEPT Frame Aligner), in Chapter 2 of the Supplementary 4259 Manual, for register locations and definitions. The Line Interface Unit (LIU - 8069B) is programmed through the Frame Aligner.

The BtX9170 registers, as used in the Model 4259, are aligned on longword addresses, (i.

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3.5 Frame Aligner and Line Interface Unit (continued)

e., at addresses ending in 0x0, 0x4, 0x8 or 0xC) to facilitate the use of this device with the TMS320 family of Digital Signal Processors. To comply with this usage, all register address offsets given in the 9170 data sheet must be multiplied by 4, then added to the Framer's base address (MIX_base+0x0008 0000 for line A, MIX_base+0x0808 0000 for line B) to determine the address to use in the 4259.

3.6 Serial Communications Controller - Read/Write @ MIX_base+0x000C 0000

See the User's Guide for the SC68C562, in Chapter 5 of the Supplementary Manual supplied with your unit, for register addresses and definitions. Channel A of the controller is used with Channel A of the 4259 and Channel B of the controller is used with the Channel B of the 4259.

The SC68C562 registers, as used in the Model 4259, are aligned on longword addresses, (i. e., at addresses ending in 0x0, 0x4, 0x8 or 0xC) to facilitate the use of this device with the TMS320 family of Digital Signal Processors. To comply with this usage, all register address offsets given in the 68C562 data sheet must be multiplied by 4, then added to the Controller's base address (MIX_base+0x000C 0000) to determine the address to use in the 4259.

This controller may also be used in conjunction with the Frame Aligner (BtX9170) for advanced manipulation of the extracted link interface. The user must determine if it is appropriate to give priority, in his system, to the extracted link message traffic, over the normal performance report transmission. The SCC is capable of transmitting and receiving HDLC-formatted messages over the Facility Data Link (FDL) in Extended Superframe (ESF) mode **ONLY**.

3.7 Interrupt Queue FIFO - Read Only @ MIX_base+0x0010 0000 (Line A) and MIX_base+0x0810 0000 (Line B)

An entry is made into a line's Interrupt Queue FIFO every time that line's Link Layer Controller issues an interrupt. The Link Layer Controller (LLC) will issue interrupts when it completes the processing of a defined Dual Port RAM data buffer, or when it finishes executing any other command. Table 3-8, below, defines the FIFO's bit structure, and the subsections that follow give more detail on the interpretation of those bits.

Table 3-8: Model 4259 - Interrupt Queue FIFO - Read Only @ MIX_base+0x0Z10 0000*

D15	D14	D13	D12	D11	D10	D9	D8
N/U	N/U	$\overline{\text{Transmit}}$/ Receive Int.	Time Slot # Bit 4	Time Slot # Bit 3	Time Slot # Bit 2	Time Slot # Bit 1	Time Slot # Bit 0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LLC Buffer Status - Bit 7	LLC Buffer Status - Bit 6	LLC Buffer Status - Bit 5	LLC Buffer Status - Bit 4	LLC Buffer Status - Bit 3	LLC Buffer Status - Bit 2	LLC Buffer Status - Bit 1	LLC Buffer Status - Bit 0

*** - Z = 0 for line A, Z = 8 for line B**

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3.7 Interrupt Queue FIFO (continued)

3.7.1 $\overline{\text{Transmit}}$/Receive Interrupt - Bit D13

A '1' in this bit indicates an interrupt from a channel configured as a receiver. A '0' in this bit indicates an interrupt from a channel configured as a transmitter.

3.7.2 Time Slot Number - Bits D12 - D8

These 5 bits contain the binary code for the time slot number of the interrupting channel. The bits are weighted such that D12 is the MSB (D4 in the 5-bit sequence, i.e., 2^4, or 16) and D8 is the LSB (corresponding to D0, 2^0, or 1).

3.7.3 Link Layer Controller Buffer Status Byte - Bits D7 - D0

The low byte of the Interrupt Queue FIFO contains a copy of the status byte contained in the Bt8071A Link Layer Controller (LLC). This is true whether the interrupt came from a transmit channel or a receive channel, or as the result of command or buffer processing completion. Refer to the Bt8071A data sheet, in Chapter 3 of the Supplementary 4259 Manual, for the mode-dependant bit definitions of this byte.

3.8 Interrupt Mask Register - Read/Write @ MIX_base+0x0014 0000

In the Interrupt Mask Register, setting a bit to the '1' state enables the indicated interrupt source, and clearing a bit to the '0' state disables the interrupt source. Channel B's bits are mapped into the upper 8 bits of this 16 bit register, and Channel A's into the lower 8 bits. Table 3-9, below, summarizes the bit assignments in this register, and the subsections that follow describe the functions of these bits. This register may also be accessed at address MIX_base+0x0814 0000.

Table 3-9: Model 4259 - Interrupt Mask Register - Read/Write @ MIX_base + 0x0014 0000

D15	D14	D13	D12	D11	D10	D9	D8
Line B Frame Aligner Mask	N/U	LLC B Queue Mux 1	LLC B Queue Mux 0	Ser Port B Out Mux 1	Ser Port B Out Mux 0	Ser Port B In Mux 1	Ser Port B In Mux 0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Line A Frame Aligner Mask	Ser Comm Ctrl Mask	LLC A Queue Mux 1	LLC A Queue Mux 0	Ser Port A Out Mux 1	Ser Port A Out Mux 0	Ser Port A In Mux 1	Ser Port A In Mux 0

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3.8 Interrupt Mask Register (continued)

3.8.1 Frame Aligner Interrupt Mask - Bits D15 and D7

Setting bit D15 in this register to the '1' state will allow the Frame Aligner in the line B interface to generate a MIX interrupt. Clearing D15 to the '0' state will prevent line B's Frame Aligner from interrupting the MIX bus.

Setting bit D7 in this register to the '1' state will allow the Frame Aligner in the line A interface to generate a MIX interrupt. Clearing D7 to the '0' state will prevent line A's Frame Aligner from interrupting the MIX bus.

3.8.2 Serial Communications Controller Interrupt Mask - Bit D6

Setting bit D6 in this register to the '1' state will allow the Serial Communications Controller to generate MIX interrupts. Clearing D6 to the '0' state will prevent the Serial Communications Controller from interrupting the MIX bus. Because there is only one Serial Communications Controller for both channels, only one mask bit is provided. Data written to D14 of this register will be ignored.

3.8.3 Link Layer Controller Interrupt Queue FIFO Mux Mask - Bits D13 & D12 and D5 & D4

These bits are used to allow certain conditions in the Interrupt Queue FIFOs on the Model 4259 can generate MIX bus interrupts. Bits D13 and D12 determine the MIX interrupt conditions for line B's Link Layer Controller (LLC) Interrupt Queue FIFO. Bits D5 and D4 select the conditions upon which line A's Link Layer Controller Interrupt Queue FIFO can interrupt MIX. Table 3-10, below, lists the settings of these bit pairs and the interrupt conditions they enable.

Table 3-10: Model 4259 - Interrupt Queue FIFO MUX Mask Bits - Interrupt Mask Register - R/W @ MIX_base+ 0x0014 0000

LLC Queue 1	LLC Queue 0	Interrupt MIX when...
0	0	Masked (Interrupt disabled)
0	1	FIFO NOT EMPTY
1	0	FIFO HALF FULL
1	1	FIFO FULL
For line A: Queue 1 = D5, Queue 0 = D4 For line B: Queue 1 = D13, Queue 0 = D12		

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3.8 Interrupt Mask Register (continued)

3.8.4 Serial Port Output FIFO Mux Mask - Bits D11 & D10 and D3 & D2

These bits are used to allow certain conditions in the Serial Port Output FIFOs on the Model 4259 can generate MIX bus interrupts. Bits D11 and D10 determine the MIX interrupt conditions for channel B's Serial Port Output FIFO, and bits D3 and D2 select the condition upon which channel A's Serial Port Output FIFO can interrupt MIX. Table 3-11, below, lists the settings of these bit pairs and the interrupt conditions they enable.

Table 3-11: Model 4259 - Serial Port Out MUX Mask Bits - Interrupt Mask Register - R/W @ MIX_base+ 0x0014 0000

Serial Port Out 1	Serial Port Out 0	Interrupt MIX when...
0	0	Masked (Interrupt disabled)
0	1	FIFO EMPTY
1	0	FIFO HALF FULL
1	1	FIFO FULL
For channel A: Port Out 1 = D3, Port Out 0 = D2 For channel B: Port Out 1 = D11, Port Out 0 = D10		

3.8.5 Serial Port Input FIFO Mux Mask - Bits D9 & D8 and D1 & D0

These bits are used to allow certain conditions in the Serial Port Input FIFOs on the Model 4259 can generate MIX bus interrupts. Bits D9 and D8 determine the MIX interrupt conditions for channel B's Serial Port Input FIFO, and bits D1 and D0 select the condition upon which channel A's Serial Port Input FIFO can interrupt MIX. Table 3-12, below, lists the settings of these bit pairs and the interrupt conditions they enable.

Table 3-12: Model 4259 - Serial Port In Mux Mask Bits - Interrupt Mask Register - R/W @ MIX_base+ 0x0014 0000

Serial Port In 1	Serial Port In 0	Interrupt MIX when...
0	0	Masked (Interrupt disabled)
0	1	FIFO NOT EMPTY
1	0	FIFO HALF FULL
1	1	FIFO FULL
For channel A: Port In 1 = D3, Port In 0 = D2 For channel B: Port In 1 = D11, Port In 0 = D10		

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3.9 **Interrupt Status Register** - Read Only @ MIX_base+ 0x0018 0000

The Interrupt Status Register is used to identify the source(s) of pending interrupts. The sources of Channel B's pending interrupts are identified by bits set to the '1' state in the upper 8 bits of this register (D15 - D8). The sources of Channel A's pending interrupts are identified by bits set to the '1' state in the lower 8 bits. This register is also accessible at address MIX_base+0x0818 0000.

Note that while only those interrupt sources enabled in the Interrupt Mask Register (see Section 3.8) can actually cause a MIX bus interrupt to be generated, the source need not be enabled in the Mask Register for these status bits to be set. Table 3-13, below, identifies which bit in the register identifies an interrupt from what source. The subsections that follow describe the significance of each bit.

Table 3-13: Model 4259 - Interrupt Status Register - Read Only @ MIX_base + 0x0018 0000

D15	D14	D13	D12	D11	D10	D9	D8
Line B Frame Aligner Int.	N/U	LLC B Int Que Half Full	LLC B Int Que Empty	SP Out B FIFO Half Full	SP Out B FIFO Empty	SP In B FIFO Half Full	SP In B FIFO Not Empty
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Line A Frame Aligner Int.	Ser Comm Ctrl Int A & B	LLC A Int Que Half Full	LLC A Int Que Empty	SP Out A FIFO Half Full	SP Out A FIFO Empty	Ser Port In A FIFO Half Full	SP In A FIFO Not Empty

3.9.1 **Frame Aligner Interrupts** - Bits D15 and D7

Bit D15 of the Interrupt Status Register will be set to the '1' state when the Frame Aligner (BtX9170) in the line B interface issues an interrupt. Bit D7 of this register will be set to the '1' state when line A's Frame Aligner issues an interrupt. Either bit will return to the '0' state when the condition that caused the interrupt is no longer true.

3.9.2 **Serial Communications Controller Interrupt** - Bit D6

Bit D6 of the Interrupt Status Register will be set to the '1' state when the Serial Communications Controller issues an interrupt. Since there is only one controller for the two channels, this interrupt serves for both channels A and B. (Bit D14 in this register will always be in the '0' state.) The user must read the controller's internal interrupt status register to determine the condition causing the interrupt and which channel it came from. See the data sheet for the SC68C562, in Chapter 5 of the Supplementary 4259 Manual, for further details. D6 will return to the '0' state when the condition that caused the interrupt is no longer true.

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3.9 Interrupt Status Register (continued)

3.9.3 Link Layer Controller Interrupt Queue FIFO Flags - Bits D13 & D12 and D5 & D4

Bit D13 of the Interrupt Status Register will be set to the '1' state when the Link Layer Controller's Interrupt Queue FIFO in the line B interface becomes half-full. Bit D12 of this register will be set to the '1' state when the last location in the Link Layer Controller's Interrupt Queue FIFO in the line B interface is read (i. e., when the FIFO becomes empty). Bit D5 of the Interrupt Status Register will be set to the '1' state when the Link Layer Controller's Interrupt Queue FIFO in the line A interface becomes half-full. Bit D4 of this register will be set to the '1' state when the last location in the Link Layer Controller's Interrupt Queue FIFO in the line A interface is read.

Note that there is no status bit for the Interrupt Queue FIFO Full condition in either line interface. If either of these FIFOs become full, however, a serious backlog condition is indicated, which would likely merit a reset.

These bits will return to the '0' state when the condition that caused the interrupt is no longer true.

3.9.4 Serial Output Port FIFO Flags - Bits D11 & D10 and D3 & D2

Bit D11 of the Interrupt Status Register will be set to the '1' state when the Serial Output Port FIFO in channel B becomes half-full. Bit D10 of this register will be set to the '1' state when the Serial Output Port FIFO in channel B becomes empty. Bit D3 of the Interrupt Status Register will be set to the '1' state when the Serial Output Port FIFO in channel A becomes half-full. Bit D2 of this register will be set to the '1' state when the first location in the Serial Output Port FIFO in channel A becomes empty.

Note that there is no status bit for the Serial Output Port FIFO Full condition in either channel. This condition is not likely to occur, however, since the user writes the data to these FIFOs and should be aware of how much data they can hold.

These bits will return to the '0' state when the condition that caused the interrupt is no longer true.

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3.9 **Interrupt Status Register** (continued)

3.9.5 **Serial Input Port FIFO Flags** - Bits D9 & D8 and D1 & D0

Bit D9 of the Interrupt Status Register will be set to the '1' state when the Serial Input Port FIFO in channel B becomes half-full. Bit D8 of this register will be set to the '1' state when the first location in the Serial Input Port in channel B is written (i. e., when the FIFO becomes non-empty). Bit D1 of the Interrupt Status Register will be set to the '1' state when the Serial Input Port FIFO in channel A becomes half-full. Bit D0 of this register will be set to the '1' state when the first location in the Serial Input Port FIFO in channel A is written.

Note that there is no status bit for the Serial Input Port FIFO Full condition in either channel. If the Serial Input FIFO Full condition is enabled in the Interrupt Mask Register (see Section 3.8.5), and a read operation of this register does not identify the source, then the Serial Input FIFO has overflowed and the data should be sent again.

These bits will return to the '0' state when the condition that caused the interrupt is no longer true.

3.10 **Serial I/O Port FIFOs** - Read/Write @ MIX_base+0x001C 0000 (Chan A) and MIX_base+0x081C 0000 (Chan B)

Write operations to these addresses send data to the differential TTL serial output port for the indicated channel. The data to be sent out the port is written to the FIFO in byte format by a MIX bus Master. It is first converted into a serial bit stream, then changed from single-ended into differential form before delivery to the output port.

Read operations at these addresses accept data from the differential TTL serial input port for the indicated channel. The differential input serial bit stream delivered to the port is first converted into single-ended form and then into byte format before delivery to the FIFO. The FIFO can be read by any MIX bus Master.

All four of these FIFOs are 8 bits wide and 1k deep.

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Chapter 4: Operating Procedures

4.1 Introduction

This chapter draws upon the information presented earlier in this manual to provide the user with procedures to follow when using the Model 4259. The information presented here assumes that the configuration jumpers on your 4259 have been set according to the requirements of your application (see Chapter 2 for details), and that you have already installed your MIX modules on the Baseboard of your choice (MIX stack assembly instructions are presented in Appendix B). Detailed descriptions of the registers referred to in the sections below were given in Chapter 3.

4.2 Initializing the Model 4259

This section describes a method that may be used to place the 4259 in a known, repeatable and usable state after power-up. The subsections below cover the initialization of the major circuit elements contained in the Model 4259. The procedure given here is illustrated in the code module **`init_59`**, which begins on page A-6 of this manual.

4.2.1 Initializing the Bt8071A Link Layer Controller

The first step in initializing the 4259's Link Layer Controller (Bt8071A) is to clear all the bits in the Link Layer Control Register to the '0' state. This register resides at address MIX_base+0x0004 0000, and may also be accessed at address MIX_base+0x0804 0000. (See Section 3.4 of this manual for a detailed description of the Link Layer Control Register.) If you will only be using a single channel of the 4259, you can clear only the lower 8 bits (D7 - D0) of this register for the line A interface, or only the upper 8 bits for line B (D15 - D8).

After the register has been cleared, the Serial Port Enable and T1/$\overline{\text{CEPT}}$ bits should be configured appropriately for your application. The Serial Port Enable bit (D5 for line A, D13 for line B) also provides the clock source select function for each channel. When this bit is set to the '1' state, the crystal oscillator, internal to the Model 4259, clocks the Line interface Unit (LIU - Bt8069B). When the bit is cleared to the '0' state, a signal applied to the channel's Serial Port connector provides the line clock.

For each line interface in use, the T1/$\overline{\text{CEPT}}$ bit in this register must be set for the appropriate framing mode. This is bit D2 for line A, and bit D10 for line B. The bit must be set to the '1' state for T1 framing mode, or cleared to the '0' state for CEPT (PCM30) framing mode.

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4.2 Initializing the Model 4259 (continued)

4.2.1 Initializing the Link Layer Controller (continued)

Once the proper state for the bits discussed above has been determined, a word should be written to this register that places them in the appropriate states and sets the Reset bits for the lines to be used to the '1' state. Line A's Reset bit is D6, and line B's is D14. The Link Layer Controller will return these bits to the '0' state when it has completed its reset cycle. After writing the Reset command to this register, your program should loop on a read at this address until the Reset bit returns to the '0' state.

For more information about application-dependent initialization of the Bt8071A, please refer to Chapters 3 and 4 of the Model 4259's Supplementary Manual, the 8071 Data Sheet and Application Note.

4.2.2 Initializing the BtT9170 (T1) or BtP9170 (CEPT) Frame Aligner and the Bt8069B Line Interface Unit

Prior to initializing the Framer and Line Interface Unit (LIU), interrupts should be disabled by clearing all bits in the Interrupt Mask Register (at address MIX_base+0x0014 0000 or MIX_base+0x0814 0000) to the '0' state.

The Frame Aligner ICs (BtT9170 or BtP9170, depending on whether the line in question is configured for T1 or CEPT, respectively) require a software reset in order for their internal registers to initialize properly. This is accomplished by setting the Reset bit (D7) in the 9170's internal Control Register #2 (CR2) to the '1' state. The address of this register is MIX_base+0x0008 001C for line A, or MIX_base+0808 001C for line B. Like the bit that initiates the Link Layer Controller's reset cycle, described in the section above, this bit will be returned to the '0' state when the Framer's reset cycle has completed. Thus, after writing the framer reset command, your program should loop on a read at this address until the Reset bit returns to the '0' state.

After completion of the software reset of the Framer, steps may be taken to initially configure the Framer and LIU. Much of the initialization will be application-dependant, and thus beyond the scope of this manual, but there are certain steps that MUST be taken in all cases to use these parts within the framework of the 4259's architecture. First, to assure that the line interface you are using is equipped with the proper Framer part, Control Register #4 (CR4) in the 9170, at address MIX_base+0x0008 0024 for line A, or MIX_base+0x0808 0024 should be read. If the BtT9170 (T1) Framer is installed, the three LSB's of this register (D2 - D0) will all be in the '0' state following a software reset. If the read operation at this address following a software reset returns a non-zero value in any of these bits, then the BtP9170 (CEPT) Framer is installed.

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4.2 Initializing the Model 4259 (continued)

4.2.2 Initializing the Frame Aligner and Line Interface Unit (continued)

After confirming that the 4259 you are addressing contains the Frame Aligner you expect it to, there are certain registers within the 9170 that must be properly initialized. First the Peripheral Active Drive Enable (PADE) bit (bit 5 of CR2 for the T1 framer (T9170), bit 4 of CR3 for the E1 version (P9170)), must be set to the '1' state. This configures the Peripheral I/O ($\overline{\text{PIO0}}$ - $\overline{\text{PIO3}}$) pins as actively driven outputs.

Next, to finalize the configuration of the $\overline{\text{PIOx}}$ pins, the two least significant Peripheral Output Data bits (POD0 and POD1, the two LSB's of CR3 in both devices) must also be set to the '1' state. This makes the $\overline{\text{PIO0}}$ and $\overline{\text{PIO1}}$ pins active low outputs. (These bits are called PTD0 and PTD1 in the P9170 Data Sheet.)

Next, the AIS (Alarm Indication Signal) Detector Select bit (ADS, bit 5 in CR4, for either Framer) is set to the '1' state. This selects the AIS detector within the 9170 as active (as opposed to the detector in the 8069). The Equalization Line Selector Bits (ELS1 - ELS3, the three LSBs of CR4 in both units) must be programmed to match the impedance of the transmission line seen by the 8069. See the CR4 section of the 9170 Data Sheet (in Chapter 2 of the Supplementary Manual) for details.

Finally, the MASTER bit (D7 of CR5 in either framer) must also be set to the '1' state. This configures the $\overline{\text{TS}}$/TMX pin as a Transmit Maximum output (as opposed to a Transmit Sync input).

For more information about application-dependent initialization of the Bt8069B, BtT9170 and/or BtP9170, please refer to Chapters 1 and 2 of the Model 4259's Supplementary Manual, the 8069 Data Sheet and 9170 Data Sheet.

4.3 Working with the Dual-Port SRAM

Use of the dual-ported SRAM in the Model 4259 is essentially unrestricted, aside from the exceptions noted in Section 3.3. Once again, these exceptions are:

1) The first 256 addresses in each line interface's SRAM bank (0x0000 0000 through 0x0000 00FF for line A, and 0x0800 0000 through 0x0800 00FF for line B) are reserved for system buffer use.

2) The user's code should not access Dual Port RAM Addresses 0x0000 0003 or 0x0000 0004 in line A, or Addresses 0x0800 0003 or 0x0800 0004 in line B, until the Link Layer controller is activated. Doing so will result in either a MIX bus timeout or a lock-up.

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4.3 Working with the Dual-Port SRAM (continued)

User code may create as many transmit and receive buffers for commands or data of whatever size is desired, as long as the restrictions above are observed. Buffers may all be of the same size, or each buffer may be of a different size, as dictated by the requirements of your application. For further information, see Chapter 4 of the Model 4259 Supplementary Manual. This is an Application Note regarding buffer programming for the Bt8071A.

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Appendix A: Programming Example

A.1 Introduction

The sample code presented in this appendix was developed on a PC/AT-compatible system, using a Bit3 Model 403 VMEbus adaptor as the Slot 1 controller and the interface between the PC and VME busses. The Pentek Model 4284 was used as the MIX baseboard. This baseboard uses the Texas Instruments' TMS320C40 Digital Signal Processor to master MIX bus transactions and perform calculations.

A header file, **4259.h**, is presented in the following section. This file assigns symbolic names to all pertinent register addresses on the 4259 and internal to the components used in this instrument. The actual 'C' language source file, **4259.c**, appears in Section A.3, beginning on page A-10.

A.2 4259.h - Header File for Model 4259 on Model 4284 Baseboard

Presented below is the header file, **4259.h**, which is **#include**d at the beginning of the **4259.c** program, in the next section of this appendix. Note that because the 4284's 'C40 processor works with a 32-bit addressing scheme, all the MIX address offsets given in the body of this manual are divided by a factor of four when used here (i. e., 'C40 offset = MIX offset/4).

```
/* Header File - 4259.h */

/* defines for the 4284 with the 4259 */
typedef volatile unsigned int uint;
typedef volatile unsigned int voluint;

/* define which module position the 4259 is in */
#define MODULE 0

/* set up module location specific defines */
#if MODULE == 0
#define MOD       0x20000000u                /* MIX module locations */
#define INT_SEL   0x80000u      /* mux mix module 0 int to c40 int 2 */
#endif

#if MODULE == 1
#define MOD       0x24000000u                /* MIX module locations */
#define INT_SEL   0x100000u     /* mux mix module 1 int to c40 int 2 */
#endif

#if MODULE == 2
#define MOD       0x28000000u                /* MIX module locations */
#define INT_SEL   0x200000u     /* mux mix module 2 int to c40 int 2 */
#endif
```

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A.2 4259.h (continued)

```
/* 4259 Memory and Register locations */
#define DPR       0x00000000u                        /* dual port ram */
#define HDLC_REG  0x00010000u  /* hdlc controller (bt8071A) register */
#define FRAMER    0x00020000u                      /* framer (bt9170) */
#define SERCC     0x00030000u     /* serial communication controller */
#define INT_QUE   0x00040000u                  /* hdlc interrupt que */
#define INT_MASK  0x00050000u             /* interrupt mask register */
#define INT_STAT  0x00060000u           /* interrupt status register */
#define PORT      0x00070000u                          /* serial port */

#define CHN_A     0x0000000u
#define CHN_B     0x2000000u
#define STACK     0x80005000u
#define STACK_END 0x80005400u

/* hdlc controller command and data buffer bits */
#define XCMND     0x0000100u
#define XBUF0     0x0000200u
#define XBUF1     0x0001200u
#define RCMND     0x0002100u
#define RBUF0     0x0002200u
#define RBUF1     0x0003200u

#define FC           0x8000
#define FO           0x4000

#define EMPTY        0x1
#define CMND         0x2
#define CF           0x4

#define HDLC_MODE    0x1
#define SIG_MODE     0x2
#define LOOP_MODE    0x4
#define INV_MODE     0x8

#define RATE_MASK    0xff00

/* 4259 HDLC register bit positions and values */
#define HCS0         0x01
#define HCS1         0x02
#define T1_CEPT      0x04
#define MDFS         0x08
#define PORT_CLK_POL 0x10
#define PORT_ENB     0x20
#define RESET        0x40
#define ATTN         0x80

/* channel activation byte constants HDLC  */
#define DEACTIVE     0x00
#define ACTIVE       0x80
#define XMT          0x00
#define RCV          0x20
#define RCV_INT      0x2000
```

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A.2 4259.h (continued)

```
/* 4259 int mask register bit positions and values */
#define PORT_IN0     0x01  /* the 1 and 0 bits work to mask fifo int */
#define PORT_IN1     0x02               /* 0 0 disable all fifo ints */
#define PORT_OUT0    0x04               /* 0 1 int on not empty flag */
#define PORT_OUT1    0x08               /* 1 0 int on half full flag */
#define HDLC_QUE0    0x10                  /* 1 1   int on full flag */
#define HDLC_QUE1    0x20  /* for example PORT_IN1 = 1, PORT_IN0 = 0 */
#define SCC_MASK     0x40  /* would allow the serial port in to int  */
#define FRAMER_MASK  0x80           /* on the in port fifo half full */

/* 4259 int status register bit positions and values */
#define PORT_OUT_EF  0x01
#define PORT_OUT_HF  0x02
#define PORT_IN_EF   0x04
#define PORT_IN_HF   0x08
#define QUE_EF       0x10
#define QUE_HF       0x20
#define SCC_INT      0x40
#define FRAMER_INT   0x80

/* framer 9170 registers and their bits */
#define  MR0      0x00                                  /* MR0 bit map */
#define  RRED     0x80
#define  AISDET   0x40
#define  LOST     0x20
#define  CRCS     0x10
#define  BPVS     0x08
#define  FERR     0x04
#define  RYEL     0x02
#define  COFA     0x01

#define  MR1      0x01                                  /* MR1 bit map */
#define  ALTF     0x80
#define  PMOK     0x40
#define  ODDS     0x20
#define  LBST     0x10
#define  PDV      0x08
#define  RREDPIN  0x04
#define  SC1      0x02
#define  SC2      0x01

#define  MR2      0x02                                  /* MR2 bit map */
#define  TXR      0x80
#define  LINK1    0x40
#define  ES1      0x20
#define  ES0      0x10
#define  PID3     0x08
#define  PID2     0x04
#define  PID1     0x02
#define  PID0     0x01
```

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A.2 4259.h (continued)

```
#define  RPCR     0x03                              /* RPCR bit map */
#define  RXP      0x80
#define  RXQ      0x40
#define  RX5      0x20
#define  RX4      0x10
#define  RX3      0x08
#define  RX2      0x04
#define  RX1      0x02
#define  RX0      0x01

#define  TS0CR    0x04
#define  TPCR     0x04                              /* TPCR bit map */
#define  TXC      0x80
/* unused bit    0x40 */
#define  TX5      0x20
#define  TX4      0x10
#define  TX3      0x08
#define  TX2      0x04
#define  TX1      0x02
#define  TX0      0x01

#define  CR0      0x05                               /* CR0 bit map */
#define  YELMD    0x80
#define  TKLE     0x40
#define  THCR     0x20
#define  RHCR     0x10
#define  FM1      0x08
#define  FM0      0x04
#define  LCM1     0x02
#define  LCM0     0x01

#define  CR1      0x06                               /* CR1 bit map */
#define  REDMD    0x80
#define  OLFRE    0x40
/* unused bit    0x20 */
/* unused bit    0x10 */
/* unused bit    0x08 */
#define  RZSD     0x04
#define  FSE      0x02
#define  SYNL     0x01

#define  CR2      0x07                               /* CR2 bit map */
#define  RTRESET  0x80
#define  RFSR     0x40
#define  PADE     0x20
#define  PER      0x10
#define  MPD      0x08
#define  MPM      0x04
#define  TCE      0x02
#define  CGABIT   0x01
```

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A.2 4259.h (continued)

```
#define  CR3      0x08                          /* CR3 bit map */
#define  U1BIT    0x80
#define  U2BIT    0x40
#define  RBIT     0x20
#define  PMSL     0x10
#define  POD3     0x08
#define  POD2     0x04
#define  POD1     0x02
#define  POD0     0x01


#define  CR4      0x09                          /* CR4 bit map */
#define  TYEL     0x80
#define  SAIS     0x40
#define  ADS      0x20
#define  MODE     0x10
#define  LOOP     0x08
#define  ELS3     0x04
#define  ELS2     0x02
#define  ELS1     0x01

#define  CR5      0x0a                          /* CR5 bit map */
#define  MASTER   0x80
#define  ETNRZ    0x40
#define  PLAUTO   0x20
#define  PLOOP    0x10
#define  EXLPS    0x08
#define  FBYPAS   0x04
#define  LBYPAS   0x02
#define  CBYPAS   0x01

#define  IR       0x0b                           /* IR bit map */
#define  IREG1    0x80
#define  IREG2    0x40
#define  IREG3    0x20
#define  IREG4    0x10
#define  IREG5    0x08
#define  IREG6    0x04
#define  IREG7    0x02
#define  IREG8    0x01

#define  DSR      0x0c                          /* DSR bit map */
/* unused bit     0x80 */
#define  D2A      0x40
#define  D4B      0x20
#define  D4A      0x10
#define  D16D     0x08
#define  D16C     0x04
#define  D16B     0x02
#define  D16A     0x01
```

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A.2 4259.h (continued)

```
#define  AER      0x0d                                  /* AER bit map */
                          /* all bits are the same as MR0 except bit 1 */
#define  SLIP     0x02

#define  IER      0x0e                                   /* IER bit map */
#define  SEC      0x80
#define  RXCODE   0x40
#define  TXCODE   0x20
#define  RXPERM   0x10
#define  RXSIG    0x08
#define  ALARMS   0x04
/* unused bit     0x02 */
#define  ITST     0x01

#define  ICR      0x0f              /* ICR bit map is the same as IER */

#define  PCCR1    0x20                                  /* PCCR bit map */
#define  PCCR2    0x21
#define  PCCR3    0x22
#define  PCCR4    0x23
#define  PCCR5    0x24
#define  PCCR6    0x25
#define  PCCR7    0x26
#define  PCCR8    0x27
#define  PCCR9    0x28
#define  PCCR10   0x29
#define  PCCR11   0x2a
#define  PCCR12   0x2b
#define  PCCR13   0x2c
#define  PCCR14   0x2d
#define  PCCR15   0x2e
#define  PCCR16   0x2f
#define  PCCR17   0x30
#define  PCCR18   0x31
#define  PCCR19   0x32
#define  PCCR20   0x33
#define  PCCR21   0x34
#define  PCCR22   0x35
#define  PCCR23   0x36
#define  PCCR24   0x37

#define  PBIT     0x80
#define  QBIT     0x40
#define  XBIT     0x20
#define  EBIT     0x10
#define  DBIT     0x08
#define  CBIT     0x04
#define  BBIT     0x02
#define  ABIT     0x01
```

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A.2 4259.h (continued)

```
#define  ARSR1    0x40                                  /* RSR bit map */
#define  ARSR2    0x41
#define  ARSR3    0x42
#define  BRSR5    0x44
#define  BRSR6    0x45
#define  BRSR7    0x46
#define  CRSR9    0x48
#define  CRSR10   0x49
#define  CRSR11   0x4a
#define  DRSR13   0x4c
#define  DRSR14   0x4d
#define  DRSR15   0x4e

/* RSR 1, 5, 9, 13 = A, B, C, D for these channels */
#define  CH8      0x80
#define  CH7      0x40
#define  CH6      0x20
#define  CH5      0x10
#define  CH4      0x08
#define  CH3      0x04
#define  CH2      0x02
#define  CH1      0x01

/* RSR 2, 6, 10, 14 =A, B, C, D for these channels */
#define  CH16     0x80
#define  CH15     0x40
#define  CH14     0x20
#define  CH13     0x10
#define  CH12     0x08
#define  CH11     0x04
#define  CH10     0x02
#define  CH9      0x01

/* RSR 3, 7, 11, 15 =A, B, C, D for these channels */
#define  CH24     0x80
#define  CH23     0x40
#define  CH22     0x20
#define  CH21     0x10
#define  CH20     0x08
#define  CH19     0x04
#define  CH18     0x02
#define  CH17     0x01

#define  NEMR1    0x52                                /* NEMR1 bit map */
#define  CRC7     0x80
#define  CRC6     0x40
#define  CRC5     0x20
#define  CRC4     0x10
#define  CRC3     0x08
#define  CRC2     0x04
#define  CRC1     0x02
#define  CRC0     0x01
```

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A.2 4259.h (continued)

```
#define  NEMR2    0x53                          /* NEMR2 bit map */
/* unused bit     0x80*/
/* unused bit     0x40*/
/* unused bit     0x20*/
/* unused bit     0x10*/
#define  CRC11    0x08
#define  CRC10    0x04
#define  CRC9     0x02
#define  CRC8     0x01

#define  NEMR3    0x54                          /* NEMR3 bit map */
#define  FBE7     0x80
#define  FBE6     0x40
#define  FBE5     0x20
#define  FBE4     0x10
#define  FBE3     0x08
#define  FBE2     0x04
#define  FBE1     0x02
#define  FBE0     0x01

#define  NEMR4    0x55                          /* NEMR4 bit map */
#define  SEF1     0x80
#define  SEF0     0x40
/* unused bit     0x20 */
/* unused bit     0x10 */
#define  FBE11    0x08
#define  FBE10    0x04
#define  FBE9     0x02
#define  FBE8     0x01

#define  NEMR5    0x56                          /* NEMR5 bit map */
#define  BPV7     0x80
#define  BPV6     0x40
#define  BPV5     0x20
#define  BPV4     0x10
#define  BPV3     0x08
#define  BPV2     0x04
#define  BPV1     0x02
#define  BPV0     0x01

#define  NEMR6    0x57                          /* NEMR6 bit map */
/* unused bit     0x80 */
/* unused bit     0x40 */
/* unused bit     0x20 */
/* unused bit     0x10 */
#define  BPV11    0x08
#define  BPV10    0x04
#define  BPV9     0x02
#define  BPV8     0x01
```

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A.2 4259.h (continued)

```
#define  FEPR1    0x58                          /* FEPR1 bit map */
#define  G3    0x80
#define  LV    0x40
#define  G4    0x20
#define  U1    0x10
#define  U2    0x08
#define  G5    0x04
#define  SL    0x02
#define  G6    0x01

#define  FEPR2    0x59                          /* FEPR2 bit map */
#define  FE       0x80
#define  SE       0x40
#define  LB       0x20
#define  G1       0x10
#define  R_BIT    0x08
#define  G2       0x04
#define  Nm       0x02
#define  Nl       0x01

#define  FEPR3 0x5a                        /* same bit map as fepr1 */
#define  FEPR4 0x5b                        /* same bit map as fepr2 */
#define  FEPR5 0x5c                        /* same bit map as fepr1 */
#define  FEPR6 0x5d                        /* same bit map as fepr2 */
#define  FEPR7 0x5e                        /* same bit map as fepr1 */
#define  FEPR8 0x5f                        /* same bit map as fepr2 */
```

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A.3 **4259.c** - Sample 'C' Code for the Model 4259 on Model 4284 Baseboard

The sample code presented below initializes a single-timeslot channel for each line interface on the Model 4259, and begins a data exchange between these two channels, in T1 Extended Superframe (ESF) mode.

```
/* 4259.c - Sample code to work with 4259 on a 4284 Baseboard */

#include "4259.h"                                    /* see page A-1 */

/* functions and pointers for the 4284 */
void delay( uint cnt );
void trigger(void);
void disable_int(void);
void enable_int(void);
void led_on(void);
void led_off(void);
void toggle_led(void);
uint in_comm_port(uint port_no, uint *data);
uint out_comm_port(uint port_no, uint data);

voluint *mail_box, *vme_reg, *mix_reg;
voluint rat, rbt, xat, xbt;
voluint *timer1_address, *timer0_address;
voluint *OBuf0, *IBuf0, *OBuf1, *IBuf1;
voluint que_entry, *int_cntrl_reg, **IntService, **Service;
uint *int02_vector;

/* Pointer for the 4259 */
voluint *Dpr, *HDLC, *Framer, *SCC, *Que, *Mask, *Status;

/*********************************************************************/

main()
{
   void init_ptrs(void);
   void init_interrupt(void);
   void init_84(void);
   void init_59(uint chn);
   void init_buf(uint channel);
   void attn(uint channel, uint active, uint tx_rx, uint time_slot);
   void buf_ser(uint *buffer);
   uint i, o, port, control;

   disable_int();

   /* Initialize the 4284 */
   init_ptrs();
   led_off();
   init_interrupt();
   init_84();
```

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A.3 4259.c (continued)

```
   /* initialize 59 */
   init_59(CHN_A);
   init_59(CHN_B);

   /* Initialize the 4259 buffers (memory) */
   /* system buffer */
   /* transmit command buf, transmit data buf */
   /* receive command buf, receive  data buf */
   init_buf( CHN_A );
   init_buf( CHN_B );

   /* enable interrupts */
   enable_int();

   /* activate timeslot */
   attn( CHN_A, ACTIVE, RCV, 2);
   attn( CHN_B, ACTIVE, RCV, 5);

   /* wait until receive buffers are activated */
   while ((*(Dpr + CHN_A + RCMND/2 + 3) & EMPTY) != EMPTY);
   while ((*(Dpr + CHN_B + RCMND/2 + 3) & EMPTY) != EMPTY);

   attn( CHN_A, ACTIVE, XMT, 5);
   attn( CHN_B, ACTIVE, XMT, 2);

   /* turn on led to show 4284 and 4259 have started */
   led_on();

   while(1)
   {
      /* service interrupt buffers */
      if( Service != IntService )
      {
         buf_ser(*Service);
         *Service++ = (uint *)0;

         if( Service == (uint **)STACK_END)
            Service  = (uint **)STACK;
      }
   }
}

/*********************************************************************/
```

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A.3 4259.c (continued)

```
void c_int02(void)
{
   int i;

   toggle_led();                  /* verify the interrupt is working */

   /* look for HDLC controller to empty or fill a data buffer */
   if((*Status & QUE_EF) != QUE_EF)
   {
      que_entry = *(Que + CHN_A);                 /* get a que entry */

      /* process any data buffer que entry */
      if((que_entry & CMND) != CMND
      {
         /* process the que entry, transmit or receive */
         if((que_entry & RCV_INT) == RCV_INT)
         {
            *IntService++ = Dpr + (CHN_A + rat / 2);

            /* reset stack to beginning */
            if( Service == (uint **)STACK_END)
               Service  = (uint **)STACK;

            /* check to see if service stack is overlapping */
            if(IntService == Service)
               mail_box[18] = 0xe1;                /* flag error E1 */
            mail_box[19] = CHN_A + rat / 2;    /* display information */

            /* toggle buffer being used */
            if( rat == RBUF0)
               rat =  RBUF1;
            else rat = RBUF0;
         }
         else
         {
            /* update service stack */
            *IntService++ = Dpr + (CHN_A + xat / 2);

            /* reset stack to beginning */
            if( Service == (uint **)STACK_END)
               Service  = (uint **)STACK;

            /* check to see if service stack is overlapping */
            if(IntService == Service)
               mail_box[18] = 0xe1;                /* flag error E1 */
            mail_box[16] = CHN_A + xat / 2;    /* display information */

            /* toggle buffer being used */
            if( xat == XBUF0)
               xat =  XBUF1;
            else xat = XBUF0;
         }
      }
   }
```

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A.3 4259.c (continued)

```
   /* look for HDLC controller to empty or fill a data buffer */
   if((*Status & (QUE_EF << 8)) != QUE_EF << 8)
   {
      /* get a que entry */
      que_entry = *(Que + CHN_B);

      /* process any data buffer que entry */
      if((que_entry & CMND) != CMND)
      {
         /* process the que entry, transmit or receive */
         if((que_entry & RCV_INT) == RCV_INT)
         {
            *IntService++ = Dpr + (CHN_B + rbt / 2);

            /* reset stack to beginning */
            if( IntService == (uint **)STACK_END)
               IntService  = (uint **)STACK;

            /* check to see if service stack is overlapping */
            if(IntService == Service)
               mail_box[18] = 0xe2;                /* flag error E2 */
            mail_box[19] = CHN_B + rbt / 2;   /* display information */

            /* toggle buffer being used */
            if( rbt == RBUF0)
               rbt  = RBUF1;
            else rbt = RBUF0;
         }
         else
         {
            /* update service stack */
            *IntService++ = Dpr + (CHN_B + xbt / 2);

            /* reset stack to beginning */
            if( IntService == (uint **)STACK_END)
               IntService  = (uint **)STACK;

            /* check to see if service stack is overlapping */
            if(IntService == Service)
               mail_box[18] = 0xe2;                /* flag error E1 */
            mail_box[16] = CHN_B + xbt / 2;   /* display information */

            /* toggle buffer being used */
            if( xbt == XBUF0)
               xbt  = XBUF1;
            else xbt = XBUF0;
         }
      }
   }

   /*************************************************************************/
```

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A.3 4259.c (continued)

```
/* Function to set up pointers and their initial values */
void init_ptrs(void)
{
   int i;

   /* 4284 pointers */
   /* test data out the 4259 and into the 4284  */
   OBuf0 = (uint *)0x80001000u;
   IBuf0 = (uint *)0x80002000u;

   OBuf1 = (uint *)0x80003000u;
   IBuf1 = (uint *)0x80004000u;

   /* interrupt stack and vector */
   Service = (uint **)STACK;
   IntService = (uint **)STACK;
   int02_vector = (uint *)c_int02;

   /* 84 registers */
   vme_reg = (uint *)0x90000000u;
   mix_reg = (uint *)0x10000000u;
   int_cntrl_reg  = (uint *)0x10000003u;
   timer0_address = (uint *)0x100020u;
   timer1_address = (uint *)0x100030u;

   /* PC mail box to monitor the status of the program */
   mail_box = (uint *) 0x80000300u;

   /* Pointer for the 4259 */
   Dpr   = (uint *)(MOD | DPR);
   HDLC  = (uint *)(MOD | HDLC_REG);
   Framer = (uint *)(MOD | FRAMER);
   SCC   = (uint *)(MOD | SERCC);
   Que   = (uint *)(MOD | INT_QUE);
   Mask  = (uint *)(MOD | INT_MASK);
   Status = (uint *)(MOD | INT_STAT);
}

/*********************************************************************/

/* Function to initialize 4284 pointers  */
void init_84(void)
{
   uint i;

   *mix_reg = 0;

   /* creat test data and put in the output buffers */
   for(i = 0; i < 0x800; i++)
   {
      OBuf0[i] = 0xa000 | i;                    /*channel A's data */
      OBuf1[i] = 0xb000 | i;                    /*channel B's data */
   }
```

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A.3 4259.c (continued)

```
   /* zero out service stack */
   for(i = 0; i < 0x400; i++)
   {
      *(Service + i) = (uint *)0;
   }

   /* initalize mail box for the PC */
   mail_box[16] = 0xffffffffu;                    /* PC display 1 */
   mail_box[17] = 0;                              /* PC display 3 */
   mail_box[18] = 0;                              /* PC display 4 */
   mail_box[19] = 0;                              /* PC display 2 */
   mail_box[20] = 0;
   mail_box[20] = 0;
   mail_box[21] = 0;
   mail_box[22] = 0;
   mail_box[23] = 0;                              /* PC display 5 */

   /* set up swing buffer offsets */
   rat = RBUF0;
   xat = XBUF0;

   rbt = RBUF0;
   xbt = XBUF0;
}

/*********************************************************************/

/* Initialize the 4259  */
void init_59(uint chn)
{
   int i;

   /* reset the 4259 and initialize the HDLC controller 8071a */
   if(chn == CHN_A)
   {
      *HDLC &= 0xff00;
      *HDLC |= (RESET | PORT_ENB | T1_CEPT);

      /* wait for 4259 to finish its reset */
      while(((*HDLC) & RESET) == RESET);
   }

   else
   {
      *HDLC &= 0xff;
      *HDLC |= ((RESET | PORT_ENB | T1_CEPT) << 8);

      /* wait for 4259 to finish its reset */
      while(((*HDLC) & (RESET << 8)) == (RESET << 8));
   }
```

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A.3 4259.c (continued)

```
mail_box[16] = *HDLC;

/* mask off all interrupts */
*Mask = 0;

/* Framers require software reset to properly initialize registers */
Framer[chn | CR2] = RTRESET;
while(Framer[chn | CR2] & RTRESET == RTRESET);

/* configure Framer */
if((Framer[chn | CR4] & 0x07) == 0) /* T9170 ELS3-1 resets to zero */
{
   Framer[chn | CR2] = PADE;               /* always set for 4259 */
   Framer[chn | CR3] = POD1 | POD0;  /* controls CB and RESET on LIU */
                                     /* POD0 = CB and POD1 = RESET */
   Framer[chn | CR4] = ADS;             /* See BT8069B spec sheet */
   Framer[chn | CR5] = MASTER;             /* always set for 4259 */
}

else                                        /* P9170 initialization */
{
   if(chn == CHN_A)
   {
      *HDLC &= !T1_CEPT;                 /* P9170 requires E1 mode*/
   }
   else
   {
      *HDLC &=  !(T1_CEPT << 8);
   }
   Framer[chn | CR2] = PADE;               /* always set for 4259 */
   Framer[chn | CR3] = POD1 | POD0;  /* controls CB and RESET on LIU */
                                     /* POD0 = CB and POD1 = RESET */
   Framer[chn | CR4] = ADS | ELS3 | ELS2; /* See BT8069B spec sheet */
   Framer[chn | CR5] = MASTER;             /* always set for 4259 */
}

/* make slave out of the B LIU (8069b) */
if(chn == CHN_B)
   Framer[CHN_B | CR4] |= MODE;

/* clear memory */
for( i = 2; i < 0x1ffe; i++)
{
   *(Dpr + chn + i) = 0;
}
```

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A.3 4259.c (continued)

```
   /* set up system table for the 8071a */
   /* transmit pointers */
   for( i = 0x40; i < 0x60; i++)
   {
      *(Dpr + chn + i) = XCMND;
   }

   /* receive pointers */
   for( i = 0x60; i < 0x80; i++)
   {
      *(Dpr + chn + i) = RCMND;
   }

   /* mask off all interrupts but !que_ef */
   *Mask = (HDLC_QUE0 << 8) | HDLC_QUE0;
}

/*********************************************************************/

/* Initialize the dual port memory */
void init_buf(uint channel)
{
   uint i, *OBuf;

   /* select the source of the output data */
   if( channel == CHN_A )
   OBuf  = OBuf0;
   else OBuf = OBuf1;

   /* transmit command buffer */
   *(Dpr + channel + (XCMND / 2) + 0) = XBUF0;
   *(Dpr + channel + (XCMND / 2) + 1) = 0x0000;
   *(Dpr + channel + (XCMND / 2) + 2) = 0x0000;
   *(Dpr + channel + (XCMND / 2) + 3) = CF | CMND;
   *(Dpr + channel + (XCMND / 2) + 4) = RATE_MASK | HDLC_MODE;

   /* transmit data buffer 0 */
   *(Dpr + channel + (XBUF0 / 2) + 0) = XBUF1;
   *(Dpr + channel + (XBUF0 / 2) + 1) = 0x0808;
   *(Dpr + channel + (XBUF0 / 2) + 2) = 0x0800 | FC | FO;
   *(Dpr + channel + (XBUF0 / 2) + 3) = CF;

   for ( i = 0; i < 0x800 / 2; i++)
   {
      *(Dpr + channel + (XBUF0 / 2) + 4 + i) = *OBuf++;
   }

   /* add last byte flag count to the end of data buffer  */
   *(Dpr + channel + ((XBUF0 + 0x808) / 2)) = 0x0800;
```

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A.3 4259.c (continued)

```
   /* transmit data buffer 1 */
   *(Dpr + channel + (XBUF1 / 2) + 0) = XBUF0;
   *(Dpr + channel + (XBUF1 / 2) + 1) = 0x0808;
   *(Dpr + channel + (XBUF1 / 2) + 2) = 0x0800 | FC | FO;
   *(Dpr + channel + (XBUF1 / 2) + 3) = CF;

   for ( i = 0; i < 0x800 / 2; i++)
   {
      *(Dpr + channel + (XBUF1 / 2) + 4 + i) = *OBuf++;
   }

   /* add last byte flag count */
   *(Dpr + channel + ((XBUF1 + 0x808) / 2)) = 0x0800;

   /* receive command buffer */
   /* NOTE: the 8th byte in the HDLC controller header is not */
   /* used by the 8071a, but by the C40 to tell if this is */
   /* a receive buffer (this byte is stuffed with 0x20 (RCV_INT) */

   *(Dpr + channel + (RCMND / 2) + 0) = RBUF0;
   *(Dpr + channel + (RCMND / 2) + 1) = 0x0000;
   *(Dpr + channel + (RCMND / 2) + 2) = 0x0000;
   *(Dpr + channel + (RCMND / 2) + 3) = CMND | RCV_INT;
   *(Dpr + channel + (RCMND / 2) + 4) = RATE_MASK | HDLC_MODE;

   /* receive data buffer 0 */
   *(Dpr + channel + (RBUF0 / 2) + 0) = RBUF1;
   *(Dpr + channel + (RBUF0 / 2) + 1) = 0x0a08;
   *(Dpr + channel + (RBUF0 / 2) + 2) = 0;
   *(Dpr + channel + (RBUF0 / 2) + 3) = EMPTY | RCV_INT;

   for ( i = 0; i < 0xa00 / 2; i++)
   {
      *(Dpr + channel + (RBUF0 / 2) + 4 + i) = 0;
   }

   /* receive data buffer 1 */
   *(Dpr + channel + (RBUF1 / 2) + 0) = RBUF0;
   *(Dpr + channel + (RBUF1 / 2) + 1) = 0x0a08;
   *(Dpr + channel + (RBUF1 / 2) + 2) = 0;
   *(Dpr + channel + (RBUF1 / 2) + 3) = EMPTY | RCV_INT;

   for ( i = 0; i < 0xa00 / 2; i++)
   {
      *(Dpr + channel + (RBUF1 / 2) + 4 + i) = 0;
   }
}

/*********************************************************************/
```

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A.3 4259.c (continued)

```
/* set up activation byte and start channel */
void attn(uint channel, uint active, uint tx_rx, uint time_slot)
{
   if( channel == CHN_A)
   {
      /* wait until any pending attention pulse clears */
      while(((*HDLC) & ATTN) == ATTN);

      /* set up activation byte and assert the attention to 8071a */
      *(Dpr + channel) = active | tx_rx | time_slot;
      *HDLC |= ATTN;
   }
   else
   {
      /* wait until any pending attention pulse clears */
      while(((*HDLC) & (ATTN << 8)) == (ATTN << 8));

      /* set up activation byte and assert the attention to 8071a */
      *(Dpr + channel) = active | tx_rx | time_slot;
      *HDLC |= (ATTN << 8);
   }
}

/*************************************************************************/

/* data buffer service */
void buf_ser(uint *buffer)
{
   uint i, match = 1;

   /* check to see if the service is needed for xmt or rcv */
   /* this is the byte add to the receive buffer header that */
   /* the c40 uses and the HDLC controller does not */
   if((*(buffer + 3) & RCV_INT) == RCV_INT)
   {
      /* move data to the c40's memory */
      if(buffer == Dpr + (CHN_A + RBUF0 / 2))
      {
         for( i = 0; i < 0x800 / 2; i++)
         {
            IBuf1[i] = buffer[i + 4] & 0xffff;

            /* compare data */
            if(IBuf1[i] != OBuf1[i])
            {
               match = 0;
               mail_box[21] = IBuf1[i];
               mail_box[22] = OBuf1[i];
            }
         }
      }
```

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A.3 4259.c (continued)

```
      else if(buffer == Dpr + (CHN_A + RBUF1 / 2))
      {
         for( i = 0; i < 0x800 / 2; i++)
         {
            IBuf1[i + 0x400] = buffer[i + 4] & 0xffff;

            /* compare data */
            if(IBuf1[i + 0x400] != OBuf1[i + 0x400])
            {
               match = 0;
               mail_box[21] = IBuf1[i + 0x400];
               mail_box[22] = OBuf1[i + 0x400];
            }
         }
      }

      else if(buffer == Dpr + (CHN_B + RBUF0 / 2))
      {
         for( i = 0; i < 0x800 / 2; i++)
         {
            IBuf0[i] = buffer[i + 4] & 0xffff;

            /* compare data */
            if(IBuf0[i] != OBuf0[i])
            {
            match = 0;
            mail_box[21] = IBuf0[i];
            mail_box[22] = OBuf0[i];
            }
         }
      }

      else if(buffer == Dpr + (CHN_B + RBUF1 / 2))
      {
         for( i = 0; i < 0x800 / 2; i++)
         {
            IBuf0[i + 0x400] = buffer[i + 4];

            /* compare data */
            if(IBuf0[i + 0x400] != OBuf0[i + 0x400])
            {
               match = 0;
               mail_box[21] = IBuf0[i + 0x400];
               mail_box[22] = OBuf0[i + 0x400];
            }
         }
      }

   /* count the number of times buffer pass or fail */
   if(match == 1)
      mail_box[17]++;
   else mail_box[23]++;
```

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A.3 4259.c (continued)

```
      /* wait for hdlc controller to finish with buffer */
      while((*(buffer + 3) & EMPTY) == EMPTY);

      /* reset the empty bit to empty for receive buffer */
      *(buffer + 3) = EMPTY | RCV_INT;
   }
   else
   {
      /* transmit data buffer */
      /* move data to the c40's memory */
      if(buffer == Dpr + (CHN_A + XBUF0 / 2))
         for( i = 0; i < 0x800 / 2; i++)
            buffer[i + 4] = OBuf0[i];

      else if(buffer == Dpr + (CHN_A + XBUF1 / 2))
         for( i = 0; i < 0x800 / 2; i++)
            buffer[i + 4] = OBuf0[i + 0x400];

      else if(buffer == Dpr + (CHN_B + XBUF0 / 2))
         for( i = 0; i < 0x800 / 2; i++)
            buffer[i + 4] = OBuf1[i];

      else if(buffer == Dpr + (CHN_B + XBUF1 / 2))
         for( i = 0; i < 0x800 / 2; i++)
            buffer[i + 4] = OBuf1[i + 0x400];

      /* wait for hdlc controller to finish with buffer */
      while((*(buffer + 3) & EMPTY) != EMPTY);

      /* reset the empty bit to not empty for transmit buffer */
      *(buffer + 3) = CF;
   }
}

/*********************************************************************/

void delay ( uint cnt )
{
   int i;

   for ( i=0; i < cnt; i++ );
}

/*********************************************************************/

/* create trigger pulse for software/hardware debug */
void trigger(void)
{
   *timer1_address = 0x302u;
   *timer1_address = 0x306u;
   *timer1_address = 0x302u;
}

/*********************************************************************/
```

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A.3 4259.c (continued)

```
void disable_int(void)
{
   asm(" LDI 0, ST");                          /* disable interrupts */
   asm(" LDI 0, IIE");        /* disable all internal c40 interrupts */
}

/*************************************************************************/

void enable_int(void)
{
   asm(" LDI 2000h, ST");
}

/*************************************************************************/

void init_interrupt(void)
{
   *int_cntrl_reg |= INT_SEL;

   asm(" LDEP IVTP, AR0");
   asm(" LDI @_int02_vector, R0");
   asm(" STI R0, *+AR0(5)");    /* set vector at location 0x4000 0005 */
   asm(" LDI  0b00h, IIF");                    /* enable c40's int 2 */
}

/*************************************************************************/

void led_on(void)
{
   *vme_reg = (*vme_reg) | 0x40;
}

/*************************************************************************/

void led_off(void)
{
   *vme_reg = (*vme_reg) & (~0x40);
}

/*************************************************************************/

void toggle_led(void)
{
   *vme_reg = (*vme_reg) ^ 0x40;
}

/*************************************************************************/
```

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Appendix B: MIX Assembly and Installation Instructions

B.1 Introduction

The connection between Pentek's family of expansion modules and the VMEbus resources is provided by the Modular Interface eXtension (MIX) interface, originally developed by Intel Corporation for Multibus II. The MIX standard defines an electrical and mechanical protocol for a private high-speed 32-bit bus, fully supported with interrupt and control functions. The elements of the MIX system, as implemented by Pentek for VMEbus, are described in this appendix.

B.2 A Glossary of MIX Terms

MIX Baseboard — The primary VME-to-MIX interface board designed for supporting one, two, or three MIX expansion modules. A MIX Stack must contain one, and only one, baseboard.

MIX Expansion Module — A printed circuit board that mounts onto the MIX Baseboard. Expansion modules may provide I/O, Memory or processing resources for the baseboard. An expansion module may have a Slave-only or a Master/Slave MIX interface, and may or may not possess its own VMEbus interface. The terms MIX module and expansion module are used interchangably in this appendix.

VME Board — A self-contained, standalone assembly suitable for plugging into a VME card cage.

MIX Board — The primary Printed Circuit (PC) board within the expansion module (i. e., the board containing the MIX surface mount connector pattern). In some expansion modules, (such as the Pentek Models 4241 and 4244), this is the only PC board.

Mezzanine Board — A secondary PC board attached to the MIX board containing additional circuitry. For example, in the Model 4242, the mezzanine board contains the analog circuitry, including amplifiers, filters, and the A/D and D/A converters.

MIX Bus Master — A device that initiates and controls data transfer cycles over the MIX bus. When this device is the MIX Baseboard, it is referred to as a Lower MIX Bus Master (LMBM). When an expansion module masters a MIX transaction, it is called an Upper MIX Bus Master (UMBM).

MIX bus Slave — A device that participates in, but neither initiates nor controls, a data transaction over the MIX bus.

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B.3 Pentek MIX Baseboards

Pentek offers a variety of MIX baseboards, all of which are full size VMEbus boards in standard 6U format (160 mm x 233 mm) and occupy one standard slot position (0.8 inches of horizontal space) in a VMEbus card cage. Each baseboard has two 96-pin male DIN connectors (P1 and P2) that mate with the corresponding female connectors on the VMEbus backplane. All power for the baseboard, and any expansion modules it may hold, is drawn from the VMEbus through these connectors.

The MIX baseboard features a surface mount contact pattern near the center of the board that supports the MIX interface. This pattern consists of 130 gold-plated pads on the upper and lower surfaces of the baseboard and mounting holes for the MIX connectors.

Pentek's line of MIX baseboards for the VMEbus includes the following devices:

- Model 4200: 68030-based; 16 MHz processor; VMEbus A32/D32 Master/Slave and VSB Master interfaces; up to 4 MB RAM
- Model 4200A: 68030-based; 40 MHz processor; VMEbus A32/D32 Master/Slave and VSB Master interfaces; up to 4 MB RAM
- Model 4201: 68030-based; 16 MHz processor; VMEbus A32/D32 Master/Slave interface; up to 4 MB RAM
- Model 4201A: 68030-based; 40 MHz processor; VMEbus A32/D32 Master/Slave interface; up to 4 MB RAM
- Model 4202: VMEbus A32/D32 Slave-only Interface; maps MIX bus addresses to VMEbus addresses
- Model 4283: DSP-based (TMS320C30); VMEbus A32/D32 Master/Slave interface; up to 8 MB RAM
- Model 4284: DSP-based (TMS320C40); VMEbus A32/D32 Master/Slave interface; up to 16 MB RAM
- Model 4285: DSP-based (Multiple TMS320C40s); VME64 Master/Slave and Auxiliary A32/D32 VMEbus Master interfaces; up to 22 MB RAM

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B.4 Pentek MIX Expansion Modules

Pentek currently offers MIX expansion modules for the VME bus with the following features:

- ❑ Floating Point Digital Signal Processors:
  - ♦ Single and Dual Texas Instruments TMS320C30 Processors
  - ♦ Single, Dual, and Quad Texas Instruments TMS320C40 Processors
  - ♦ Triple AT&T DSP32C Processors
- ❑ A/D Converters
  - ♦ 32 Channel, 16-bit, 12.5 kHz sample rate
  - ♦ 32 Channel, 12- or 14-bit, 125 kHz sample rate
  - ♦ 32 Channel, 16-bit, 100 kHz sample rate with digital filter
  - ♦ Single Channel, 12-bit, 1 MHz sample rate with LC filter
  - ♦ Single Channel, 12-bit, 10 MHz sample rate
  - ♦ Single Channel, 14-bit, 10 MHz sample rate with 'C40 Comm Port output
- ❑ A/D - D/A Converters
  - ♦ 16 Channel, 16-bit, 48 kHz sample rate
  - ♦ 8 Channel, 16-bit, 200 kHz sample rate, with 'C40 Comm Port I/O
  - ♦ Single and Dual Channel, 18-bit, 200 kHz sample rate
  - ♦ Single Channel, 12-bit, 1 MHz sample rate
- ❑ D/A Converter: 32 Channel, 12-bit, 100 kHz sample rate
- ❑ Digital I/O devices
  - ♦ 32-bit Parallel Digital I/O
  - ♦ SCSI-1 Interface
  - ♦ Wide/Fast SCSI-2 Interface
  - ♦ RS-232C Serial Interface
- ❑ Digital Receivers
  - ♦ Four Channel, 12-bit, 70 MHz Digital Drop Receiver
  - ♦ Multiband Digital Drop Receiver
- ❑ Single and Dual Channel T1/CEPT Interface
- ❑ Time Code Reader
- ❑ Prototyping Module

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B.5 MIX Module General Description

Standard MIX modules are 10.3" long x 4.0" deep x 0.8" wide. No electrical or mechanical connection is made between the VMEbus back plane and a standard MIX module, since all power and signal lines are provided through the MIX interface connectors. Each module has its own front panel secured to the card cage with captive hardware. The back ends of standard expansion modules are mechanically secured to the baseboard by means of the MIX connectors.

Some of Pentek's MIX modules differ from the above standards. The Model 4240 MIX prototyping module is somewhat deeper (6.0"), to allow more flexibility for custom circuit construction.

The Model 4270, with four TMS320C40 DSPs can function as either a stand-alone VME Slave board, a MIX Master/Slave module, or both. This unit is therefore a full-size 6U VME board, and draws power from the VME backplane, rather than from the MIX bus. The Model 6102 Octal A/D-D/A Converter has a full VMEbus slave interface as well as a MIX bus slave interface. This, too, is a full-depth MIX card, which engages the P1 and P2 VME connectors and can participate in VMEbus data cycles. On these full-depth MIX modules, the MIX connector pattern is located near the center of the card, rather than at the rear.

The Emitter-Coupled Logic (ECL) input versions of the Digital Receiver modules (Models 4271 and 4272) are also full depth MIX cards. These also draw power from the VMEbus, but cannot participate in any VME data transactions (although they do pass along the daisy-chained signals).

Each MIX module is accessed by the MIX baseboard as a unique memory region, determined by the module's stack position. Separate interrupt and control lines are provided for each stack position.

B.6 MIX Module Stack Assembly Techniques

Two methods are available for installing the first MIX module on the MIX baseboard. The first expansion module may be mounted in the Nested position or in the Non-Nested position. These terms will be defined below.

When the first expansion module is mounted in the Nested position, this module and the MIX baseboard occupy the same VME card cage slot, and share the expansion module's front panel. When the nested assembly technique is used, a full MIX stack (consisting of a baseboard and three expansion modules) occupies only three slots in the VME card cage. This technique leaves an additional slot in the card cage available, so that another VME device may be installed.

When the first expansion module is mounted in the Non-Nested position, the baseboard occupies its own slot in the VMEbus card cage, and has its own front panel. The first expansion module will occupy the slot to the right of the baseboard in the card cage. When the Non-Nested assembly technique is used, a full MIX stack (consisting of a baseboard and three expansion modules) occupies four slots in the VME card cage.

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B.6 MIX Module Stack Assembly Techniques (continued)

The front panels of the Models 4200, 4200A, 4201 and 4201A are very useful for the initial configuration of these baseboards, but in normal use the panel is generally removed. These baseboards will normally utilize the Nested assembly technique to share a common card cage slot with the first MIX expansion module.

MIX Baseboard Model 4202 is most often used without the VME front panel, and with the first expansion module mounted in the Nested position. The Model 4283 can sometimes be used in this manner as well. The Models 4284 and 4285 Baseboards do not support the Nested module installation, and each of these devices will always occupy its own card cage slot.

Full-depth MIX modules can not be Nested on any baseboard, because they must engage the VME backplane and therefore require a card cage slot of their own.

Table B-1 (below) describes which combinations of MIX Baseboards and expansion modules allow for Nested installation.

Table B-1: Expansion Module/Baseboard Nesting Compatibility

A 'Yes' indicates that for the given MIX Baseboard/Module combination, nested installation in stack position 1 is possible.

MIX Modules	Pentek VME/MIX Baseboards					MIX Modules	Pentek VME/MIX Baseboards				
	4200(A)	4201(A)	4202	4283	4284/5*		4200(A)	4201(A)	4202	4283	4284/5*
4240	No	No	No	No	No	**4254**	Yes	Yes	Yes	No	No
4241	Yes	Yes	Yes	Yes	No	**4255**	Yes	Yes	Yes	Yes**	No
4242	Yes	Yes	Yes	No	No	**4256**	Yes	Yes	Yes	Yes	No
4243	Yes	Yes	Yes	No	No	**4257**	Yes	Yes	Yes	No	No
4244	Yes	Yes	Yes	Yes	No	**4258**	Yes	Yes	Yes	No	No
4245	Yes	Yes	Yes	No	No	**4259**	Yes	Yes	Yes	No	No
4246	Yes	Yes	Yes	No	No	**4260**	Yes	Yes	Yes	No	No
4247	Yes	Yes	Yes	No	No	**4270**	No	No	No	No	No
4248	Yes	Yes	Yes	No	No	**4271**	Yes†	Yes†	Yes†	No	No
4249	Yes	Yes	Yes	No	No	**4272**	Yes†	Yes†	Yes†	No	No
4250	Yes	Yes	Yes	No	No	**4273**	Yes	Yes	Yes	No	No
4251	Yes	Yes	Yes	No	No	**4274**	Yes	Yes	Yes	No	No
4252	Yes	Yes	Yes	No	No	**4275**	Yes	Yes	Yes	No	No
4253	Yes	Yes	Yes	No	No	**6102**	No	No	No	No	No

* - MIX Baseboard Models 4284 and 4285 do not support nested installation

** - Model 4255, Option 001, which features shrouded, latching connectors, will not nest on a Model 4283 baseboard

† - The ECL Input versions of these devices connect to VME, and cannot be nested on any baseboard

Regardless of the assembly technique selected, any MIX stack may consist of a baseboard with one, two, or three expansion modules installed upon it. The expansion modules are designed such that, when installed, the component side of the module faces the component side of the the Baseboard.

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B.7 MIX Module Stack Assembly Components

The following subsections describe the mechanical components used to build a MIX stack. Figures B-1 through B-3, on this page and the next, present pictures of these components. Figure B-4, on the page after next, shows how these components are used in the assembly of a MIX stack.

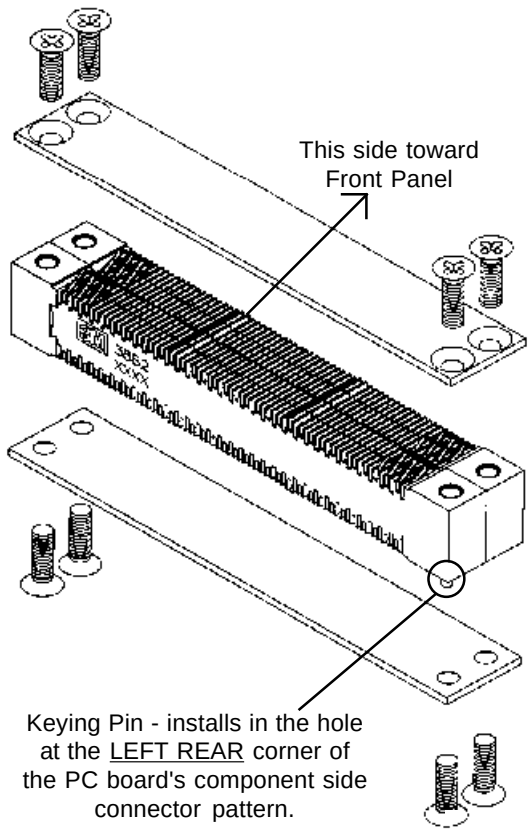


Figure B-1: MIX Baseboard Connector with Stiffeners and Flathead Screws.
Viewed from rear of Baseboard

Manufactured by 3M Electronic Products Division as Part Number X3882-1000, which includes one baseboard connector, two stiffeners and eight screws. This kit is shipped with each Pentek MIX baseboard.

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B.7.1 MIX Baseboard Connector

The MIX baseboard connector attaches a MIX expansion module to a MIX baseboard. The MIX baseboard connector (see Figure B-1, left) is a surface mount bridge between the MIX contact pattern on the baseboard and the matching contact pattern on an expansion module. The baseboard connector is 0.476" tall and has 130 gold-plated spring contacts on both top and bottom surfaces. It also features a keying pin, that fits into a keying hole on the baseboard. Pentek applies bright, orange labels to all MIX connectors, showing the "UP" side of the connector (i. e., toward the next module position) and the side of the connector that faces the front panels.

B.7.2 MIX Stiffener

The MIX stiffener maintains contact pressure between the MIX baseboard connector and the MIX baseboard. Uninstalled, the MIX stiffener is slightly curved and features an insulating polyester film on the surface that touches the MIX contact pattern. The MIX stiffener attaches to the MIX baseboard connector via four flathead screws which pass through the MIX baseboard and into threaded inserts in the MIX baseboard connector. Figure B-1, left,also shows the top and bottom stiffeners and the flathead screws.

When tightening these flathead screws, the torque should not exceed 2 in-lbs or there is a possibility of damaging the threads in the MIX baseboard connector. Pentek offers a special torque driver specifically for tightening the flathead screws (Pentek Model # 2030).

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B.7 MIX Module Stack Assembly Components (continued)

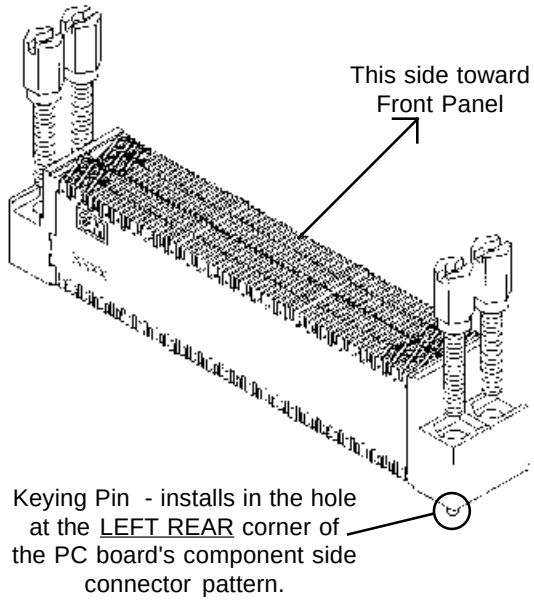


Figure B-2: MIX Stacking Connector with Jackscrews.

Viewed from rear of PC Board

Manufactured by 3M Electronic Products Division as Part Number X3884-0000, which includes one stacking connector and four jackscrews. This kit is shipped with each expansion module.

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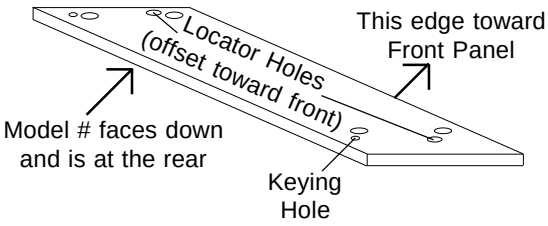


Figure B-3: MIX Spacer Board

Viewed from rear of Baseboard

Manufactured by Tektronix. The 'MIX' spacer board is shipped with every Model 4283 and 4284 baseboard.

B.7.3 MIX Stacking Connector

The MIX stacking connector is used when adding expansion modules to the MIX stack. The stacking connector is similar to the MIX baseboard connector described in Section B.7.1, except that its height is 0.738 inches instead of 0.476 inches and the stacking connector features a step at each end to accommodate the jackscrews (described in Section B.7.5. below). The stacking connector is shown in Figure B-2, left.

B.7.4 MIX Spacer Board

In situations where the first MIX expansion module cannot (or will not) be nested on the baseboard (see Table B-1, page before last), a MIX spacer board (see Figure B-3, below left) must be installed between the MIX baseboard connector and the MIX stacking connector. A MIX spacer board is supplied with every Model 4283 and Model 4284 baseboard, and with the non-nestable MIX modules.

B.7.5 MIX Jackscrews

Each stacking connector attaches to the MIX connector below it via MIX jackscrews (see Figure B-2, above left). The jackscrews pass through the MIX stacking connector, through the MIX expansion board, and into the threaded inserts (or other jackscrews) in the MIX connector below. Each jackscrew has a threaded opening in the head to accept jackscrews from additional MIX components above it. Pentek offers a special torque driver specifically for tightening the MIX jackscrews (Pentek Model # 2031).

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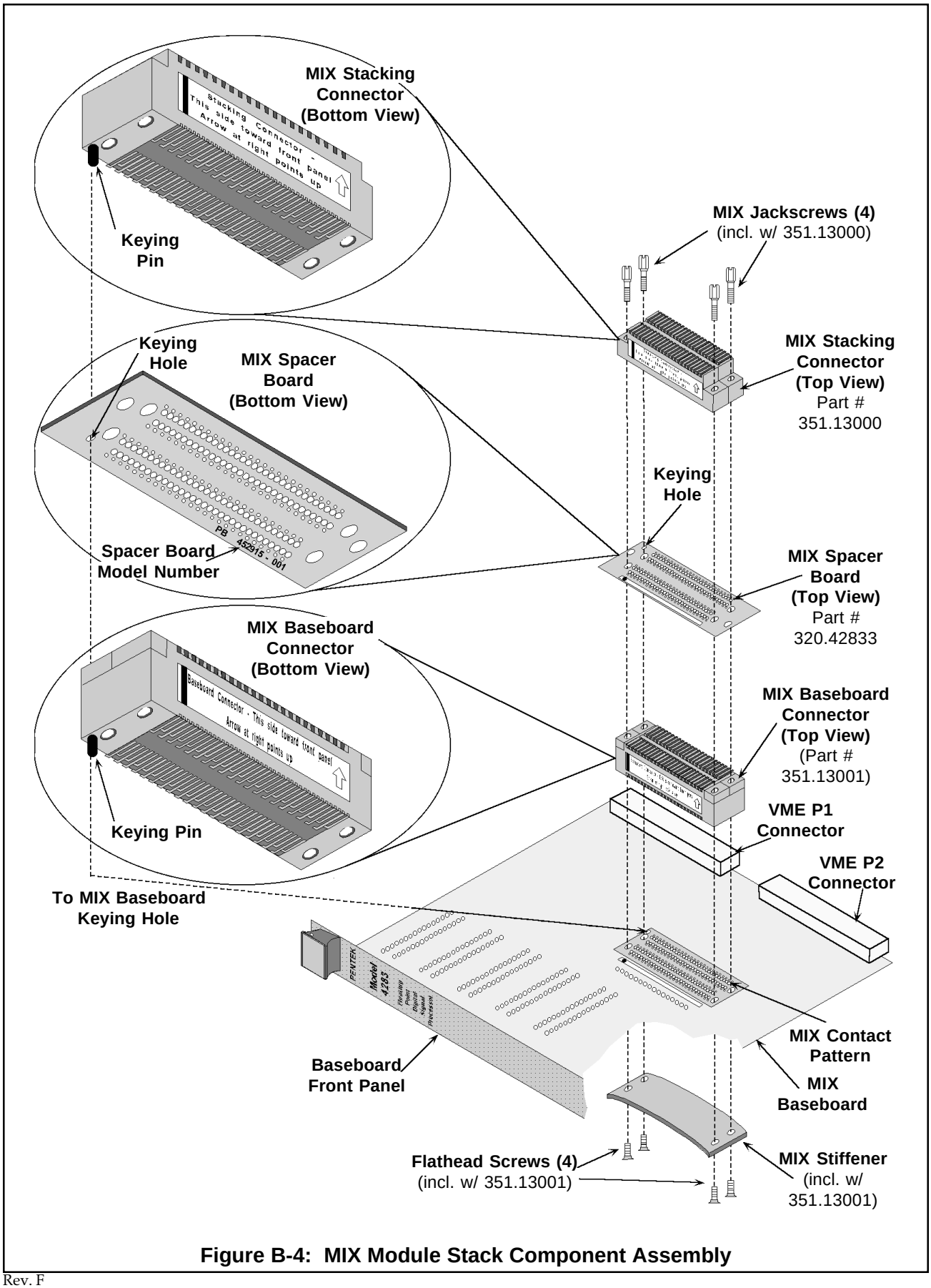


Figure B-4: MIX Module Stack Component Assembly

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B.8 Non-Nested MIX Stack Assembly

While performing these assembly procedures, refer to Figures B-4, B-5 and B-6, on pages B-8, B-11 and B-13, respectively. Expansion module positions are referred to as "MIX stack position 0" for the first module (the module mounted ***closest to the baseboard***), "stack position 1" for the second module, and "stack position 2" for the third module.

Assemble all MIX components in a static controlled environment!



Improper alignment of the MIX components *WILL* cause failure of the MIX interface and very likely damage the boards!

Turn off all power to the card cage before inserting or removing any board(s)!

1) Place a MIX baseboard connector on top of the baseboard's MIX contact pattern. Verify that the black stripes on both orange labels are aligned, and that the baseboard connector's keying pin is seated in the keying hole of the baseboard's contact pattern.

2) Place the insulated (shiny) side of a MIX stiffener against the **BOTTOM** of the baseboard's MIX contact pattern.

3) Insert, but ***do not fully tighten***, four flathead screws through the MIX stiffener, through the baseboard, and begin threading them into the baseboard connector.

4) Tighten the flathead screws ***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B-5A, to draw the baseboard connector against the baseboard's MIX contact pattern.

   NOTE: Do not torque the flathead screws over 2 in-lbs (Pentek Model #2030 Torque Driver may be used).

5) Place a MIX spacer board on top of the MIX baseboard connector such that the black stripes on all three orange labels are aligned.

6) Place a MIX stacking connector over the MIX spacer board such that the black stripes on all four orange labels are aligned. Verify that the stacking connector's keying pin seats properly in the spacer board's keying hole.

7) Insert, but ***do not fully tighten***, four jackscrews through the stacking connector, through the spacer board, and begin threading them into the baseboard connector.

8) Tighten the jackscrews ***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B-5A, to draw the stacking connector against the spacer board's MIX contact pattern.

   NOTE: Do not torque the jackscrews over 5 in-lbs (Pentek Model #2031 Torque Driver may be used).

9) Place the ***first*** expansion module over the stacking connector, with the component side facing ***DOWN***. ***If this installation requires only one expansion module, proceed to step 18*** (see next page).

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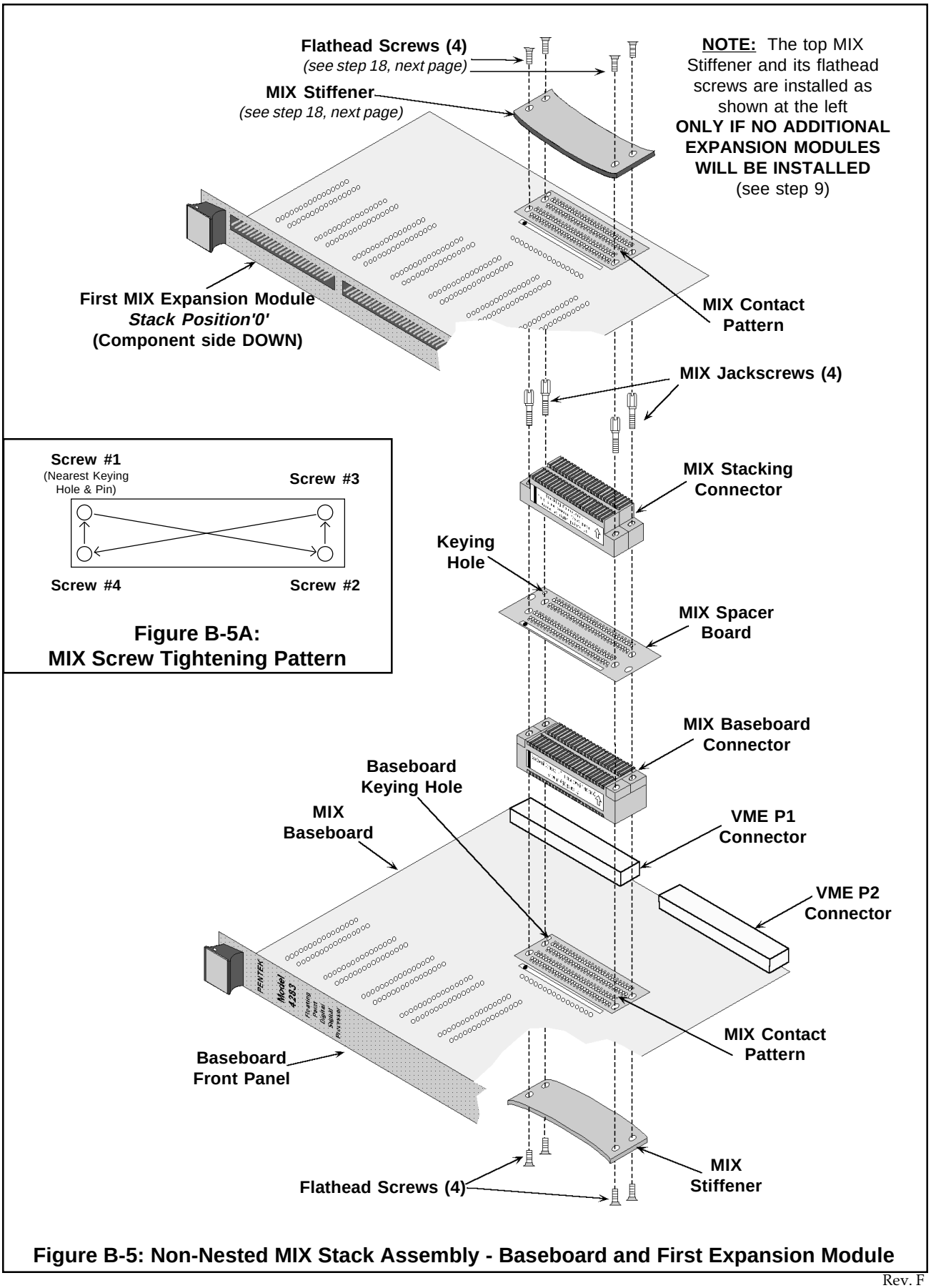


Figure B-5A: MIX Screw Tightening Pattern

Figure B-5: Non-Nested MIX Stack Assembly - Baseboard and First Expansion Module

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B.8 Non-Nested MIX Stack Assembly (continued)

10) Place another stacking connector over the MIX contact pattern on the TOP of the ***first*** expansion module (see Figure B-6, on the next page). Verify that the black stripes on all orange labels are aligned, and that the stacking connector's keying pin seats properly in the expansion module's keying hole.

11) Insert, but ***do not fully tighten***, four jackscrews through the stacking connector, through the ***first*** expansion module, and begin threading them into the stacking connector below the expansion module.

12) Tighten the jackscrews ***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B-5A (on the previous page), to draw the stacking connector against the expansion module.

    NOTE: Do not torque the jackscrews over 5 in-lbs (Pentek Model #2031 Torque Driver may be used).

13) Place the ***second*** expansion module over the stacking connector with the component side facing ***DOWN. If this installation requires only two expansion modules, proceed to step 18***, below.

14) Place another stacking connector over the MIX contact pattern on the TOP of the ***second*** expansion module (see Figure B-6, on the next page). Verify that the black stripes on all orange labels are aligned, and that the stacking connector's keying pin seats properly in the ***second*** expansion module's keying hole.

15) Insert, but ***do not fully tighten***, four jackscrews through the ***third*** stacking connector, through the ***second*** MIX expansion module, and begin threading them into the ***second*** stacking connector.

16) Tighten the jackscrews ***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B-5A (on the previous page), to draw the stacking connector against the expansion module.

    NOTE: Do not torque the jackscrews over 5 in-lbs (Pentek Model #2031 Torque Driver may be used).

17) Place the ***third*** expansion module over the stacking connector, with the component side facing ***DOWN***.

18) Place the insulated (shiny) side of the MIX stiffener against the MIX contact pattern on the TOP of the ***last*** expansion module.

19) Insert, but ***do not fully tighten***, four flathead screws through the MIX stiffener, through the ***last*** expansion module, and begin threading them into the stacking connector below.

20) Tighten the flathead screws ***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B- 5A (on the previous page) to draw the stacking connector against the ***last*** expansion module's MIX contact pattern.

    NOTE: Do not torque the flathead screws over 2 in-lbs (Pentek Model #2030 Torque Driver may be used).

This completes the assembly procedure for a non-nested MIX stack.

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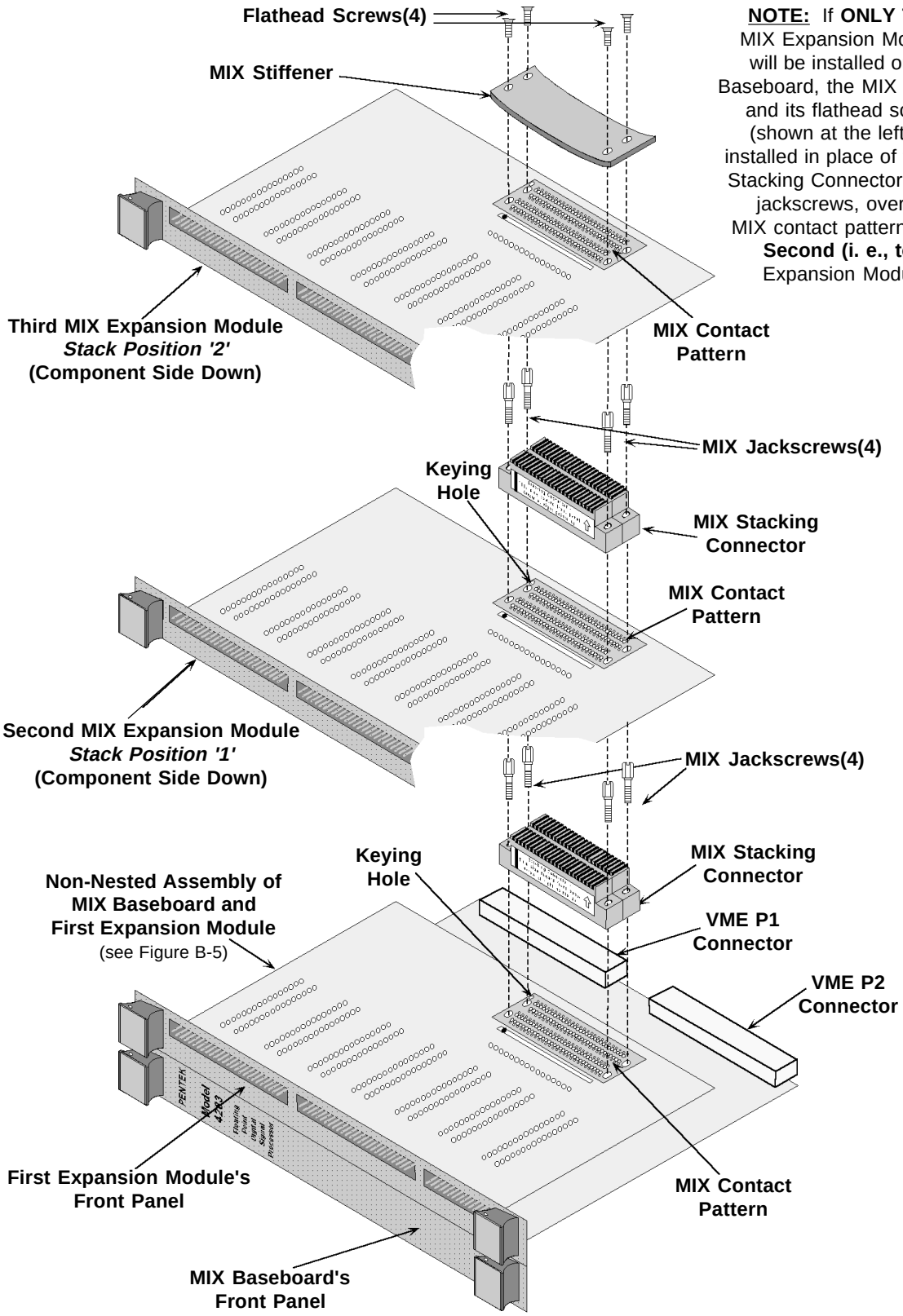


Figure B-6: Non-Nested MIX Stack Assembly - Adding Expansion Modules

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B.9 Nested MIX Stack Assembly

In Nested configurations, the MIX baseboard and the first MIX expansion module occupy the same VMEbus card cage slot. Expansion module positions are still referred to as "MIX stack position 0" for the first module (the module mounted ***closest to the baseboard***), "stack position 1" for the second module, and "stack position 2" for the third module. While performing these assembly procedures, please refer to Figures B-4, B-7, and B-8, on pages B-8, B-15 and B-17, respectively.

Assemble all MIX components in a static controlled environment!

Improper alignment of the MIX components *WILL* cause failure of the MIX interface and very likely damage the boards!

Disconnect all power to the card cage before inserting or removing any board(s)!

1) Place a MIX baseboard connector on top of the baseboard's MIX contact pattern. Verify that the black stripes on both orange labels are aligned, and that the baseboard connector's keying pin is seated in the keying hole of the baseboard's contact pattern.
2) Place the insulated (shiny) side of a MIX stiffener against the **BOTTOM** of the baseboard's MIX contact pattern.
3) Insert, but ***do not fully tighten***, four flathead screws through the MIX stiffener, through the baseboard, and begin threading them into the baseboard connector.
4) Tighten the flathead screws ***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B-7A (at the bottom of this page), to draw the baseboard connector against the baseboard's MIX contact pattern.

   NOTE: Do not torque the flathead screws over 2 in-lbs (Pentek Model #2030 Torque Driver may be used).
5) Place the ***first*** expansion module on the stacking connector, with the component side facing ***DOWN***. ***If this installation requires only one expansion module, proceed to step 14***, on the next page.

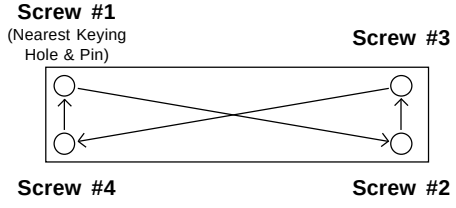


Figure B-7A:
MIX Screw Tightening Pattern

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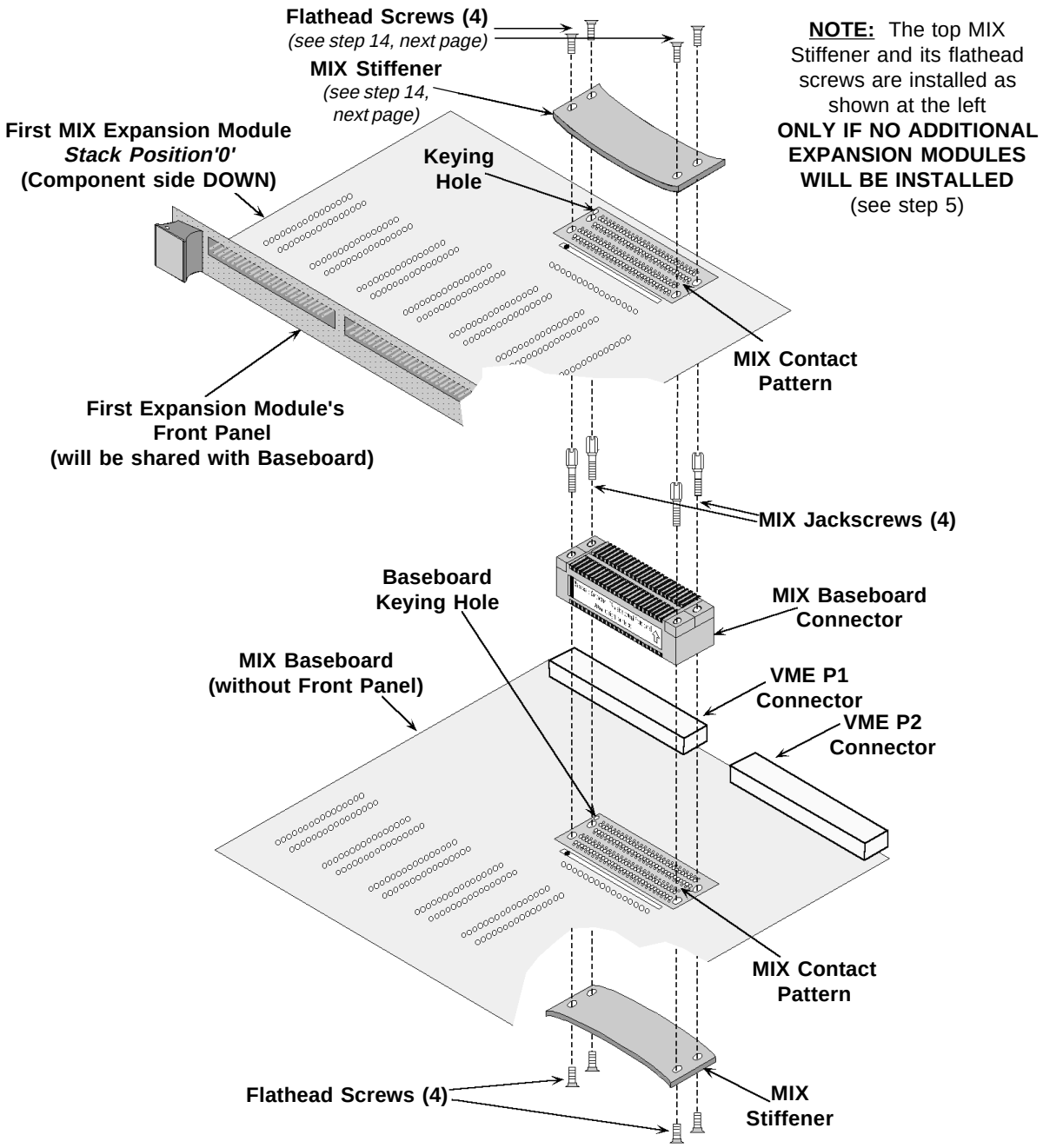


Figure B-7: Nested MIX Stack Assembly - Baseboard and One Expansion Module

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B.9 Nested MIX Stack Assembly (continued)

6) Place a stacking connector over the MIX contact pattern on the TOP of the ***first*** expansion module (see Figure B-8, on the next page). Verify that the black stripes on all orange labels are aligned, and that the stacking connector's keying pin seats properly in the expansion module's keying hole.

7) Insert, but ***do not fully tighten***, four jackscrews through the stacking connector, through the ***first*** expansion module, and begin threading them into the baseboard connector below the expansion module.

8) Tighten the jackscrews ***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B-7A (at the bottom of the page before last), to draw the stacking connector against the expansion module.

   NOTE: Do not torque the jackscrews over 5 in-lbs (Pentek Model #2031 Torque Driver may be used).

9) Place the ***second*** expansion module over the stacking connector with the component side facing DOWN. ***If this installation requires only two expansion modules, proceed to step 14***, below.

10) Place another stacking connector over the MIX contact pattern on the TOP of the ***second*** expansion module (see Figure B-8, on the next page). Verify that the black stripes on all orange labels are aligned, and that the stacking connector's keying pin seats properly in the ***second*** expansion module's keying hole

11) Insert, but ***do not fully tighten***, four jackscrews through the ***second*** stacking connector, through the ***second*** MIX expansion module, and begin threading them into the ***second*** stacking connector.

12) Tighten the jackscrews ***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B-7A (at the bottom of the page before last), to draw the stacking connector against the expansion module.

    NOTE: Do not torque the jackscrews over 5 in-lbs (Pentek Model #2031 Torque Driver may be used).

13) Place the ***third*** expansion module over the stacking connector, with the component side facing ***DOWN***.

14) Place the insulated (shiny) side of the MIX stiffener against the MIX contact pattern on the TOP of the ***last*** expansion module.

15) Insert, but ***do not fully tighten***, four flathead screws through the MIX stiffener, through the ***last*** expansion module, and begin threading them into the stacking connector below.

16) Tighten the flathead screws ***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B-7A (on the page before last), to draw the stacking connector against the ***last*** expansion module's MIX contact pattern.

    NOTE: Do not torque the flathead screws over 2 in-lbs (Pentek Model #2030 Torque Driver can be used).

This completes the assembly procedure for a nested MIX stack.

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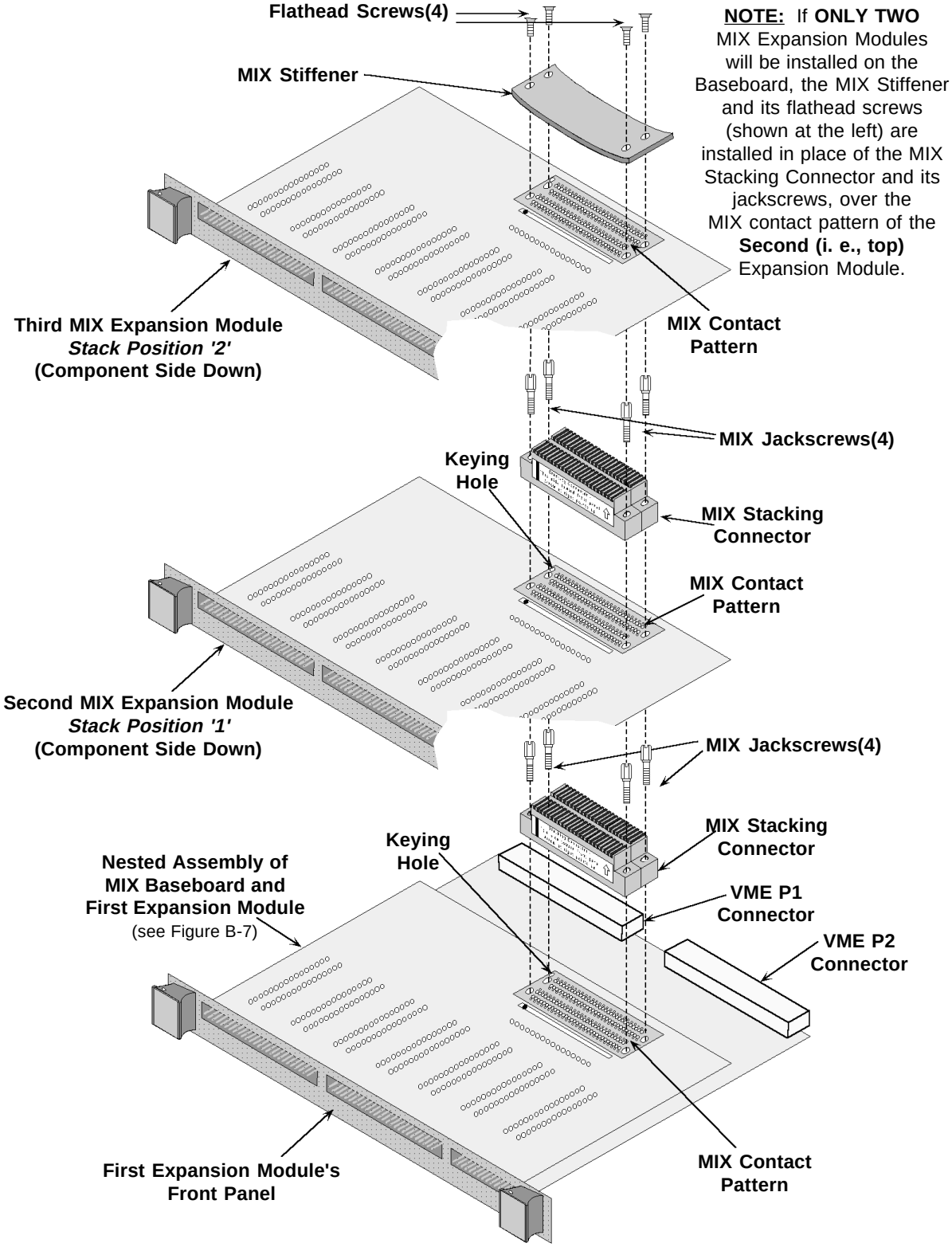


Figure B-8: Nested MIX Stack Assembly - Adding Expansion Modules

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B.10 MIX Stack Disassembly

When disassembling a MIX stack, loosen all screws in the same manner in which they were tightened (***slowly*** and ***evenly***, one turn at a time for each screw in sequence, following the pattern shown in Figure B-7A, at the bottom of page B-14). **This is of particular importance when loosening the flathead screws**, which are stressed by the spring tension of the MIX stiffener. **Failure to observe this precaution may result in property damage or personal injury, caused by flying screws.**

B.11 Installing Ejector Handles on the MIX Module Front Panel

VME card cage ejector handles should be installed on the front panel of any assembly that engages the VMEbus backplane. For nested installations, where the baseboard's front panel is removed, ejector handles must be installed on the front panel of the nested MIX Module. The installation procedure is described below.

Each Ejector Handle and Panel Mounting Bracket assembly mounts to the front panel with one Philips-head screw and nut per handle. Each Philips-head screw threads into hex nuts that are secured in recessed holes within both the top and bottom Ejector Handle and Panel Mounting Bracket. The assembly is illustrated in Figure B-9, on the next page.

1) The Ejector Handles will be mounted on posts on the Panel Mounting Brackets at the top and bottom of the circuit board. These brackets are attached to the front panel with Philips-head screws at the top (and bottom) of the panel, located directly below (and above) the captive card-cage retraining screws. These Philips-head screws are threaded into hex nuts which are recessed within the body of the Panel Mounting Brackets. Locate and remove these two Philips screws. Be sure to retain the nuts, as they will be required to re-install the Ejector Handles.
2) Locate the Ejector Mounting Post on the panel bracket (see Figure B-9, Detail B), which is found on the component side of the MIX module. A slotted-head screw is installed in each post. These screws need not be removed.
3) The top and bottom ejector handles differ from one another in the offset of the arm which will pass through the front panel. Holding the handle with the Cover Plate facing you (i. e., with the arm away from you) the top handle will have this arm offset to the left of center when the arm points down. The bottom handle will have the arm offset to the left of center when the arm points up (see Figure B-9A, at the top of the next page). Identify each handle and mount it in its proper position. It may be necessary to gently flex the circuit board to allow the hole in the handle's mounting arm to engage the bracket's mounting post.
4) Slide the Cover Plates out of the Ejector Handles. This will reveal holes in the backs of the handles (again, see FigureB-9A), through which you can replace the top and bottom front panel retaining screws.
5) Slide the Cover Plates back into the Ejector Handles (see Figure B-9, Detail A)

This completes the Ejector Handle mounting procedure.

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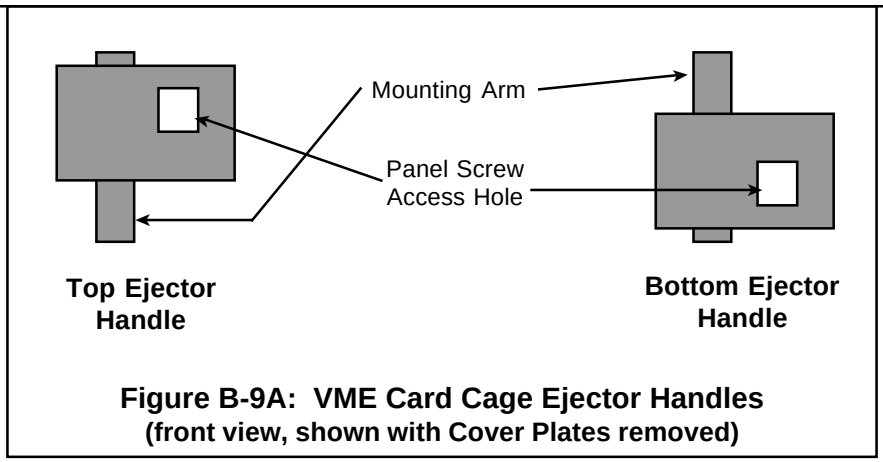


Figure B-9A: VME Card Cage Ejector Handles
(front view, shown with Cover Plates removed)

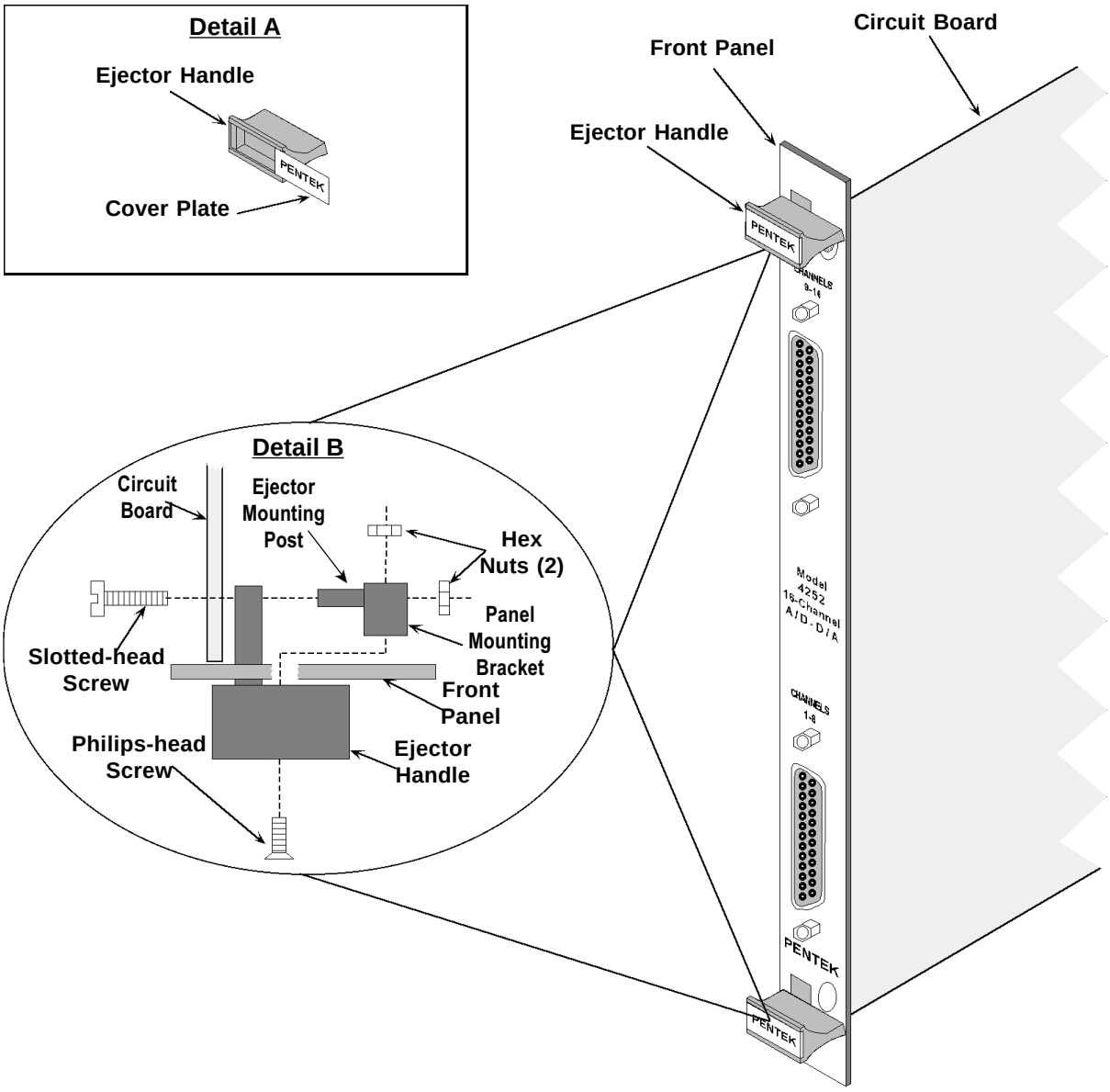


Figure B-9: Installing Ejector Handles on MIX Module Front Panels

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B.12 Linking MIX Module Front Panels and Ejector Handles

After your MIX stack has been assembled according to the instructions above, the front panels of the modules 'float' until they are secured by their captive screws to the VMEbus card cage. Also, the ejector handle on the Baseboard (or the module nested on the Baseboard) is the only mechanism for removing the MIX stack from the card cage.

In order to provide a more secure mechanical assembly when the stack is removed from the card cage, a pair of 'panel links' is provided with your Baseboard. These links may be used to tie all front panels in the stack together. Use of these links is optional, but strongly recommended if the stack will be removed from the card cage frequently.

Additionally, card cage ejector handles may be installed on all MIX module front panels. These ejectors **MUST** be physically secured to the ejectors on the Baseboard front panel, to assure equal pressure is applied along the card cage ejector plate during the ejection process. Installation of ejectors on the module panels is especially recommended if your stack includes any full-depth modules that engage the VME backplane, such as the Model 4270, the Model 6102, or the Models 4271 or 4272, with Option 012.

For the sturdiest configuration possible, the panel links and module ejector handles can be used together. This assembly method provides for both physical links between all module panels and improved ease of system ejection from the card cage. Procedures for the installation of the panel links and module ejector handle links are provided below. Note that, as a general rule, Pentek does not ship MIX modules with ejector handles installed, but the handles are included with the module. The installation procedure for the ejector handles can be found in Section B.11, on page B-18 of this Appendix. If you wish to use both panel and ejector handle links, the ejector handles should be installed on the MIX modules **BEFORE** the panel links.

B.12.1 Panel Links

The panel links are machined aluminum bars that may be snapped off to accommodate 2, 3 or 4 front panels in the MIX stack. Two links are required for each stack assembly: one for the top of the panels and one for the bottom. The top and bottom links are symmetrical, but not identical. The silver link braket is used at the top of the panel, and the gold link bracket is used at the bottom. The links are installed behind the front panels, using the screws that hold the plastic Panel Mounting Brackets to the front panel.

Configuring the links for the number of modules in the stack is achieved by snapping the links at the molded indentations, as shown in Figure B-10, on the next page. Grasp the link on either side of the indentation with two pliers and bend the link to snap it to length.

To use the links to join the front panels of the MIX modules, first assemble the MIX stack, using the MIX connectors as described in the assembly instructions in the preceding sections of this Appendix. If ejector handles will be used on the modules, install them next, as described in Section B-11 of this Appendix. Then, follow the steps listed on the next page.

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B.12 Linking MIX Module Front Panels and Ejector Handles (continued)

B.12.1 Panel Links (continued)

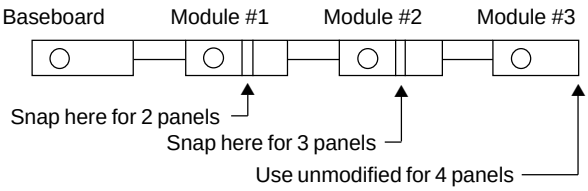


Figure B-10: Panel Links

1) Remove the two cover plates from the ejector handles of the MIX baseboard by sliding them sideways. Lay the MIX stack flat on a work surface with the baseboard on the bottom.

2) Insert a #0 Philips screwdriver through the hollow center of the baseboard ejectors and loosen the 10 mm long, raised flat-head Philips screws (2.5 mm diam. x 0.45 pitch), located directly behind the two ejectors. Remove the nuts from the plastic brackets behind the front panel. Save these nuts for possible future use. (We suggest that you use the zip lock bag the links came in).

3) Loosen these same screws on each of the MIX modules and remove the nuts from their brackets.

4) Place the links behind the top and bottom plastic brackets such that the holes in the links are aligned with the screw holes on the appropriate panels, as indicated by the caption above the link drawing in Figure B-10, above. Again, use the silver bracket at the tops of the panels, and the gold bracket at the bottoms.

5) Gradually tighten all screws in rotation, a few turns at a time, making sure that the panels are aligned at the top and bottom.

6) If you will **NOT** be using module ejectors, replace the two cover plates in the baseboard ejectors. The MIX stack may now be installed in the card cage, without the module ejectors.

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B.12 Linking MIX Module Front Panels and Ejector Handles (continued)

B.12.2 Linked Module Ejector Handles

As mentioned in the introductory remarks of this section, ejector handles installed on MIX module front panels must be physically coupled to the ejector handles on the MIX Baseboard. Beginning around October of 1994, all VMEbus ejector handles shipped by Pentek have had small holes drilled in their sides. Ejectors on each unit may be coupled to those on adjacent units by passing rods through these holes. If you have an older MIX Baseboard or module and wish to use linked ejectors, contact the factory at the phone number shown on this manual's title page, and a set of modified ejector handles will be sent to you.

The parts listed below are supplied with each Pentek VMEbus MIX Baseboard to support this feature. Figure B-11, at the top of the next page, will help you identify each part.

Quantity	Items	Pentek Part Number
2	ID Plate: VME 2 Slots w/ Logo	305.00031
2	ID Plate: VME 3 Slots w/ Logo	305.00033
2	ID Plate: VME 4 Slots w/ Logo	305.00035
2	Metal Bar Shaft: VME Ejector 2 Slots	384.00020
2	Metal Bar Shaft: VME Ejector 3 Slots	384.00030
2	Metal Bar Shaft: VME Ejector 4 Slots	384.00040
6	Retaining Ring: (E) 0.093 Shaft	388.20000
1	Full Size Bottom Panel Link (Gold)	303.00145
1	Full Size Top Panel Link (Silver)	303.00143

The assembly procedures beginning below assume that you have already installed a pair of handles on each module, that the MIX module stack is fully assembled, and that the ID (or blank aluminum) face plates are NOT inserted in the ejector handles.

1) Select a pair of shafts, based on the number of VME card cage slots your MIX stack will occupy.

2) Align the top and bottom rows of Ejector Handles and insert a shaft through each row. Shafts should be inserted such that the ends with two inscribed slots rest inside the Ejector Handles of the Baseboard (or the module nested on the Baseboard).

c) Install two pairs of retaining 'E' rings on the Shafts inside the Baseboard Ejector Handles. One ring is inserted in each of the two slots on the shafts in the top and bottom Ejector Handles. These rings prevent the shafts from sliding by anchoring the shafts inside the Ejector Handles of the Baseboard (or nested module). Figure B-12, page after next, shows an installed shaft with the retaining rings properly positioned.

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B.11 Linking MIX Module Front Panels and Ejector Handles (continued)

B.11.2 Linked Module Ejector Handles (continued)

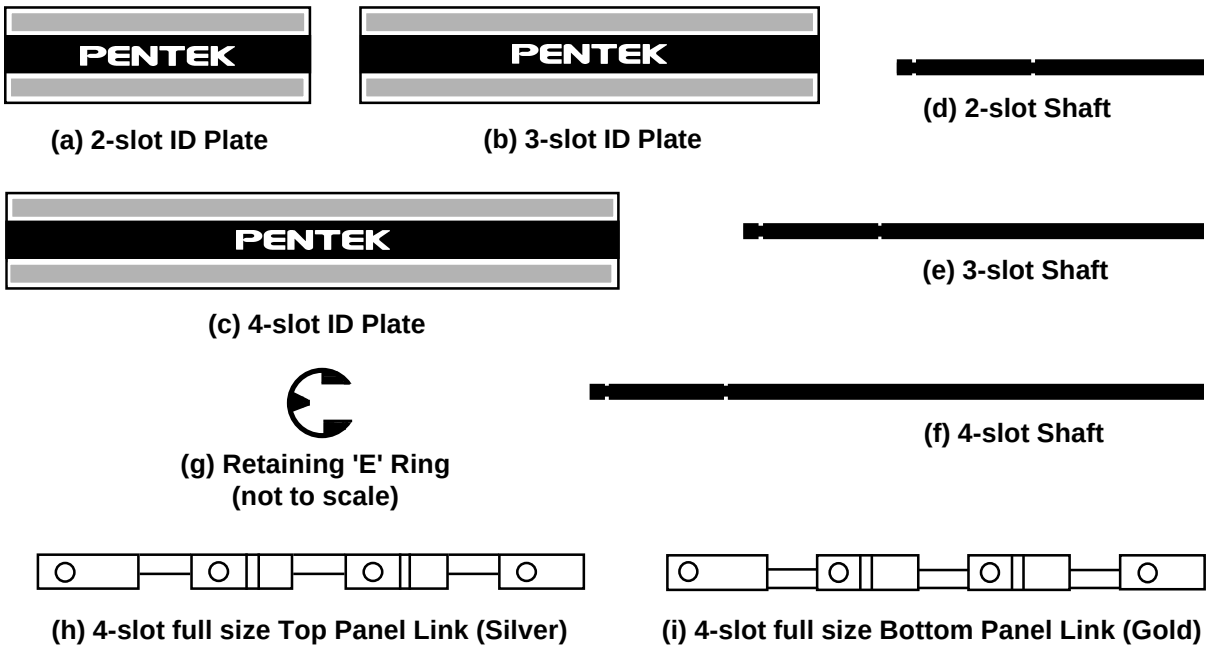


Figure B-11: Linked Module Ejector Parts

d) Select a pair of ID plates (again, based on the number of VME card cage slots your MIX stack will occupy), and install one plate in each row of ejector handles. To install the plates, you may either slide them sideways through all the handles in the row, or position them over the handles and snap them in.

f) The MIX stack may now be installed in the card cage.

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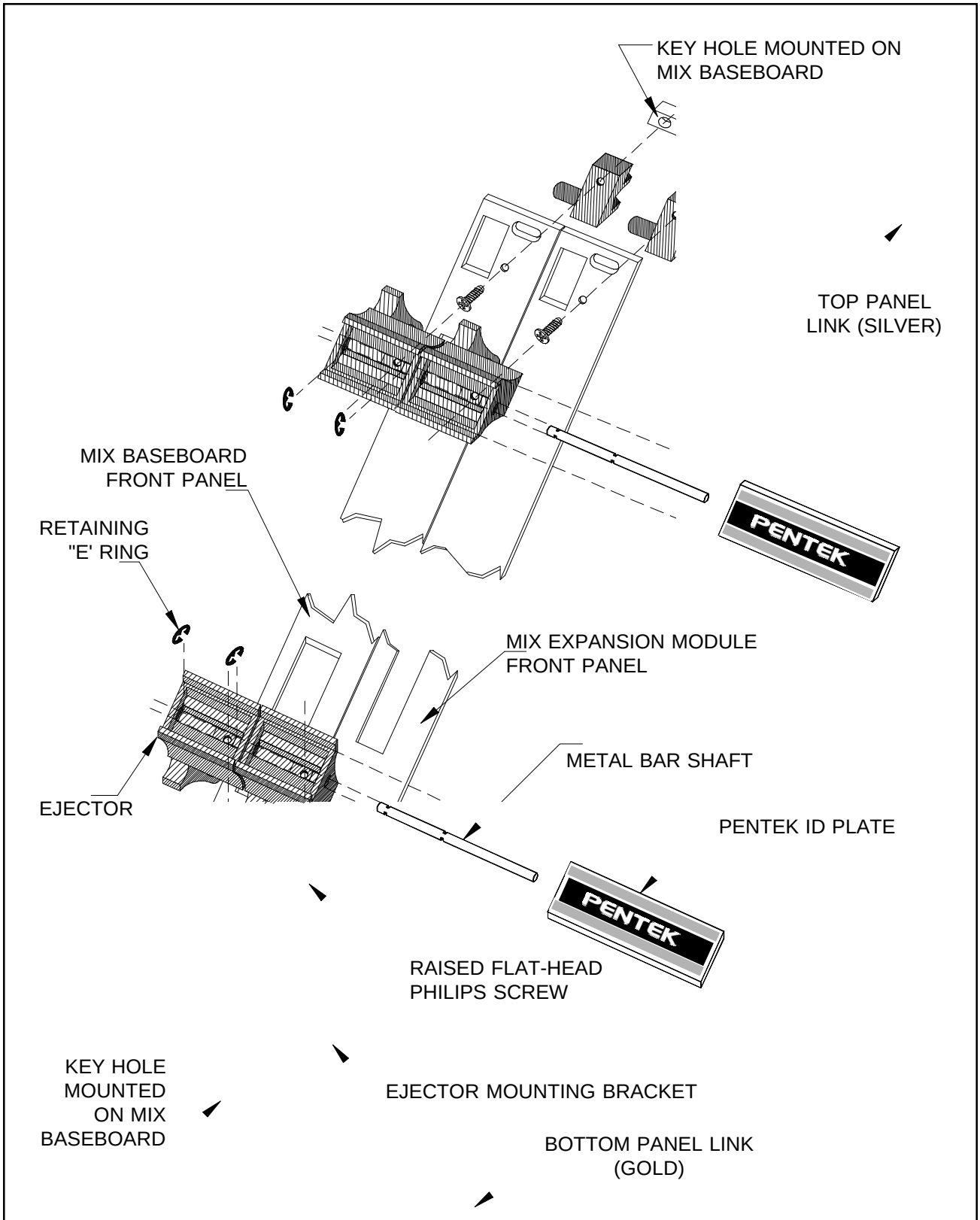


Figure B-12: MIX Stack with Linked Module Ejectors

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B.13 Installing the Assembly into the VMEbus Card Cage

Once the assembly of the MIX baseboard and expansion module(s) has been completed, the assembly can be installed in the card cage.

If linked module ejector handles have not been installed, and the MIX baseboard will be the only portion of the assembly which actually engages in the back plane, then **use only the front panel ejector/handles of the MIX baseboard** (or nested MIX module) - not those of the expansion modules, when inserting and removing the assembly. After inserting the assembly, push in on the top and bottom ejector/handles of the MIX baseboard or nested module ***only*** to fully seat the connectors in the back plane.

If linked ejectors were installed, and if there is more than one unit in the assembly that engages the backplane, apply equal pressure along the length of the linked ejector handles to seat all units in the VMEbus backplane connectors.

Once the assembly is seated, the captive panels screws at the top and bottom of each front panel should be screwed into the top and bottom rails of the card cage.

When removing the assembly, first loosen **ALL** captive screws on the top and bottom of each front panel. Attempting to remove the MIX stack while any module is still secured to the cage will cause damage to the MIX connectors. Then, push the ejector handles of the assembly away from the center of the panel to eject the assembly from the cage. Once disengaged, pull outward on the ejector handles to remove the assembly.

CAUTION !!
TURN OFF ALL POWER TO THE CARD CAGE
BEFORE INSERTING OR REMOVING ANY BOARD

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Appendix C: MIX Baseboard Tutorial

C.1 Introduction

Since any of Pentek's VMEbus MIX modules can be used with any of Pentek's VMEbus MIX baseboards, the module is addressed and controlled in different ways, depending upon the characteristics of the MIX baseboard. Below are some characteristics of each of Pentek's currently-offered MIX baseboards. Understanding how each baseboard functions will lead to a better understanding of how to program the MIX module for maximum performance.

Table C-1, below, shows which interfaces each of Pentek's MIX baseboards supports:

Table C-1: Pentek MIX Baseboard Features

Pentek Model Number	VME Master Interface	VME Mapped Slave Resources		VSB Master Interface	Supports MIX Masters	On Board Processor
		MIXbus	RAM			
4200(A)	Yes	Yes	4 MB SRAM	Yes	Yes	68030
4201(A)	Yes	Yes	4 MB SRAM	No	Yes	68030
4202	No	Yes	None	No	Yes	none
4283	Yes	No	8 MB DRAM	No	No	'C30
4284	Yes	No	16 MB DRAM	No	Yes	'C40
*4285	Yes	Yes	3 MB SRAM	Option 032	Yes	8x'C40

* - The Model 4285 becomes a MIX Baseboard when equipped with Option 031

The table summarizes many of the important features which are analyzed below:

VME Master Interface: Note that all MIX baseboards except for the 4202 have VME master interfaces. On the 4283, 4284 and 4285, this VME master interface is mapped into the address space of a DSP processor chip. The Model 4285 features a VME64 master/slave interface, as well as A32/D32 VMEbus master capabilities. On the 4200 and 4201, the VME master interface is mapped into the address space of the 68030 processor and is also mapped into the MIX bus address space for access by any MIX bus master. See Section C.2.

VME Mapped Slave Resources - MIXbus: This column shows whether or not the MIXbus is addressable from the VMEbus as a slave memory region. Note that this is possible for the 4200, 4201, 4202 and 4285, baseboards but not for the 4283 and 4284 baseboards. In these products, the MIX bus is addressable only from the DSP processor.

VME Mapped Slave Resources - RAM: This column shows the size and type of RAM addressable from the VMEbus as a slave memory region. The 4283 and 4284 present the DRAM to the VMEbus while the 4200, 4201 and 4285 present the SRAM to the VMEbus. The 4202 contains no RAM at all.

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C.1 Introduction (continued)

VSB Master Interface: The Model 4200 has a VSB master interface which is mapped into the address space of the 68030 processor and is also mapped into the MIX bus address space for access by any MIX bus master. See section C.3. The Model 4285 also supports an optional VSB master interface. On this unit, the VSBus can be mastered only by processors on the 4285 board, not by Upper MIX Bus Masters.

Supports MIX Masters: Some MIX modules such as the 'C40 processor products, have the ability to master the MIX bus. This means that they can read or write to other MIX modules and possibly access some features on the baseboard. Note that all of the MIX baseboards except for the Model 4283 support MIX master transfers. See section C.4.

C.2 VMEbus Slave and Master Interfaces

There are two major categories of VMEbus interfaces: 'master' and 'slave'. A 'VMEbus master interface' allows a VME board to initiate read or write cycles with another VMEbus board. The important issue here is that the master device actively drives the control lines (data strobes, address strobes, etc.) on the bus during the memory cycle.

The board that responds to reads or writes by the master is called the 'slave'. The slave presents its memory or registers to the VMEbus as part of the VMEbus address space. Each slave should be assigned a separate region of address space, usually determined by on-board jumpers, so that each slave is separately addressable by any master device. This is done by the system integrator when he sets up the VME system.

A board can have both master and slave interfaces. A single board may have the ability to initiate memory cycles on the VMEbus (master capability), and also present memory or registers which are mapped into VMEbus address space (slave capability). It is actually quite common that a board with a master interface will also have a slave interface.

For example, the Model 4283 has a dual-port RAM addressable from the VMEbus as a slave memory resource. It also has a master interface which allows it to read any VMEbus slave device. These two features are quite separate and distinct sub-systems on the board.

On the other hand, the Model 4202 has only a slave interface which maps the MIXbus onto the VMEbus. All of the memory resources and registers in every MIX module attached to the Model 4202 are now directly addressable as slave memory on the VMEbus.

C.3 VSBus Slave and Master Interfaces

The VSBus is a sub-system bus which uses 64 lines on the VMEbus backplane which are 'reserved' in the VMEbus specification for other applications. It provides a secondary 32-bit data path for transfers between boards supporting this specification, and involves both 'master' and 'slave' interfaces similar to the VMEbus. VSB address and data are multiplexed over the same 32 lines: the address is sent out first and then multiple data transfers to sequential addresses, making block transfers quite efficient.

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C.3 VSBbus Slave and Master Interfaces (continued)

The Pentek Model 4200 includes a VSBbus master interface, which is optional on the Model 4285. These are ideal in applications such as delivering data from an A/D converter MIX module to a VSB slave destination such as a general purpose memory board.

C.4 MIXbus Master Interface and MIXbus Slave Interfaces

Extending the discussion of VMEbus and VSBbus 'master' and 'slave' interfaces leads to a similar definition of those interfaces on the MIXbus. MIXbus master modules can initiate reads and write to other slave resources of the MIXbus. This can include other MIX modules like A/D converters and the shared memory of co-processor modules. The MIX baseboard is always capable of mastering the MIXbus.

Pentek's 'C40 co-processor MIX modules (the Models 4254, 4257 and 4270) can read input data by mastering data transfers from an A/D converter, for example. It can also read or write directly into the global SRAM of a neighboring 4254/57/70. Reading and writing to MIXbus resources is as simple as using the correct address since all MIX modules are mapped into a well-defined address space determined by the stacking position.

All but one of Pentek's MIX baseboards support the operation of master MIX modules - the Model 4283. It only permits the 'C30 on the baseboard to master the MIXbus. This means that all data transfers to and from MIX modules are mastered by the baseboard 'C30 and not by a MIX module. Nevertheless, the Model 4283, Pentek's first baseboard product, has supported thousands of powerful applications.

For all of Pentek's other MIX baseboards, a master MIX module like the Model 4257 can obtain mastership of the MIXbus. When a MIX master module is attached to the Model 4200 or Model 4201, the MIX mastering capability makes the module capable of performing its own VMEbus and (with the 4200) VSBus cycles. See Section C.7 for more discussion.

C.5 Turning a MIX Module into a Slave VMEbus Board with the Model 4202

If your application needs the function of a MIX module in the form of a standard 6U VMEbus card with a simple slave interface, the Model 4202 is the answer. For example, a 32-channel A/D Converter MIX module like the 4248 can be made into a 32-channel A/D Converter single-slot VMEbus board by attaching it to a Model 4202. All of the modules control and status registers and the output FIFO are mapped directly onto the VMEbus. The VMEbus address space occupied by the board is easily set with address switches and jumpers.

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C.6 Using the Model 4202 Baseboard for MIX Master Sub-Systems

Suppose someone needs a 16-channel voice-band A/D converter plus quad 'C40 DSP horsepower to drive a T1 telecom line. In this case, the activity over the VMEbus is minimal, and certainly does not require a VMEbus master interface.

Configuring a system with a Model 4252 A/D, a Model 4270 Quad C40, and a Model 4258 T1 Interface all on a Model 4202 baseboard does the trick! In this 3-slot sub-system, the Quad C40 acting as a MIXbus master moves the input data from the A/D module, processes the data, and sends output data to the T1 module.

C.7 Turning a MIX Module Into a VMEbus Master

Two of Pentek's baseboards allow a master MIX module to become a VMEbus master - the Models 4200 and 4201. In operation, a master MIX module like the Model 4270 issues a read or write to the MIX address space reserved for the VMEbus master interface. In this case, the read or write is transported through to the VMEbus.

Since all four 'C40's in the 4270 can be MIXbus masters, any one of the 'C40 processors in the Model 4270 can freely access any VMEbus slave memory resource.

There are currently three MIX modules with MIXbus master interfaces: Models 4254, 4257, and 4270, with one, two and four 'C40's, respectively. All MIX modules have slave interfaces, even those with master interfaces. These slave interfaces make available to the MIXbus the shared memory, control registers, status registers, and FIFO memories within the modules.

C.8 DMA Controller Functions with the Model 4200/01(A)

Suppose a 32-channel A/D converter board needs to send data to various VMEbus destinations. In this case, the ideal solution is a 32-channel A/D MIX module coupled to a Model 4200, 4200A, 4201 or 4201A baseboard. This family of baseboards, with its VMEbus master interface, contains a powerful DMA controller which is easily configurable from the VMEbus.

First, the A/D converter is initialized for the number of channels, sampling rate, and interrupt conditions (such as FIFO half-full), etc.

Secondly, the DMA controller on the Model 4200/01(A) is initialized for the data source (MIXbus address of the A/D FIFO), the data destination (some VMEbus slave resource address), the number of points to be transferred per block (typically one half the FIFO size), and the initiating event for the DMA transfer (like the FIFO half-full interrupt from the A/D).

Now, when the A/D is released for collecting data, every time the FIFO fills up with 512 points (half-full), those 512 points are automatically delivered to the VMEbus destination without any further intervention.

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C.8 DMA Controller Functions with the Model 4200/01(A) (continued)

This self-contained data mover is simple to use and extremely flexible. Notice that even though there is a 68030 on board, the basic operation of the Model 4200/01(A) does not require the user to perform any CPU or DSP programming. All standard data move schemes are implemented in on-board firmware, and require only the setting of the basic parameters of the data move.

C.9 Programming the 68030 on the 4200/01(A) MIX Baseboards

Many system designers want to program the 68030 processor inside the Model 4200/01(A). No matter how many canned DMA routines exist in the firmware, many applications demand a special software routine executed by the 68030 not easily handled by the firmware. While stressing simplicity of use, this baseboard family was designed to accommodate many such custom applications.

There are three basic memory resources on the Model 4200/01(A):

- The Boot Flash ROM contains the factory supplied firmware for initializing the VMEbus and MIXbus interfaces and standard DMA firmware routines. Normally, this ROM is used as a read-only resource. However, provisions have been made to allow firmware upgrades in the field by sending customers a disk containing the new firmware. Special jumpers on the board permit the Boot Flash ROM to be re-written from the disk file.

- The general purpose static RAM, ranging from 1 to 4 MB, is addressable from the VMEbus, the MIXbus, and the 68030. Programs developed for the 68030 using a generic C cross-compiler on a host computer can be downloaded easily through the VMEbus interface.

- The User Flash ROM permits the user to store a nonvolatile program which can be executed upon power up. This obviates the need to download a program to RAM from a host, a significant benefit in dedicated or embedded stand-alone applications.

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Appendix D: Using the Pentek Model 4283 MIX Baseboard

D.1 Introduction

This section describes the addressing MIX modules when attached to the Model 4283 MIX baseboard. All data and commands to the MIX modules are controlled by the TMS320C30 processor on the Model 4283 baseboard. For more detailed information about the Model 4283, refer to the Model 4283 Operating Manual.

The MIX bus interface on the Model 4283 is implemented by using the expansion bus of the 'C30 processor. This bus has 32 bits of data and 13 bits of address. Therefore, the 'C30 expansion bus can directly access 2^{13} = 8,192 locations of 32-bit words.

This capability of the 'C30 expansion bus is utilized in the MIX bus interface as follows: The least significant address bit of the 'C30 expansion bus drives the A2 bit of the MIX bus, which corresponds to MIX bus address boundary resolution of 32-bit words.

Therefore, the two least significant MIX bus address bits are not driven by the Model 4283 MIX bus interface. Another way of expressing this relationship is that the 'C30 can only access 32-bit MIX bus words on MIX addresses ending with hex digits of 0, 4, 8 and C. Note that consecutive 'C30 expansion bus addresses are spaced at 4-byte increments on the MIX bus. All resources of the MIX module are arranged to match this scheme.

The most significant address bit of the 'C30 expansion bus drives the MIX address line A14. MIX address lines A15 and above are supplied from the Model 4283 Page Register. This is a special register which is written to by the 'C30 prior to MIX bus accesses in order to set up these higher order address bits. The result is that the Model 4283 sees the MIX bus as a set of 'pages' of memory, each containing 32 kbytes, or 8k 32-bit words.

In addition to the upper MIXbus address bits, the Page Register also supplies the Module Select bits. These two bits select which one of the three MIX modules is being accessed.

Most data acquisition MIX modules are not memory-intensive devices and for these units all accesses to the unit occur within the address range of base page (8k x 32 bits). Therefore, the 4283 Page Register need only be changed to select the MIX module.

All accesses to the 8k x 32-bit MIXbus page from the Model 4283 'C30 expansion bus are mapped into a 'C30 CPU address range which starts at location 0x80 4000 and ends at 0x80 5FFF. The MIX bus address references used in the body of the manual have a correspondence to 'C30 addresses in the Model 4283 as shown in the charts on the next pages.

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D.1 Introduction (continued)

Notation used in this section uses conventions followed in the 'C' language where a '0x' prefix designates a hex number. The number of hex digits reflects the range of the number. The MIX address is expressed as an 8-digit number (32 bit range) while the 'C30 addresses are expressed as a 6-digit number (24 bit range). The space in front of the last four digits improves readability.

D.2 Model 4283 MIX Module Selection

Each module is accessed by the TMS320C30 by using a two bit field in the Model 4283 Page Register. The Model 4283 Page Register is a write-only device mapped into the 'C30 address 0x80 0002.

There are a total of 32 bits in the Page Register and only two are used for module selection. When changing these bits, it is recommended that a memory image of the current value of the Page Register be maintained so that only these two bits can be altered. This can be conveniently done by first reading the Page Register, masking bits 15 and 16 to zero, and then 'OR'-ing in the new bits values for bit 15 and 16 as shown in the last column of the chart below.

Bits 15 and 16 select one of three possible MIX stack positions according to Table D-1, below.

Table D-1: Module Selection - Model 4283 Page Register Bits - 'C30 Address 0x80 0002

MIX Stack Position	Z	MIX_base Address (0xZnnn nnnn)	Page Register Bits				'OR'-ed Value for Page Register
			Bits 31 thru 17	Bit 16	Bit 15	Bits 14 thru 0	
Position 1	C	0xCnnn nnnn	x	1	1	x	0x0001 8000
Position 2	D	0xDnnn nnnn	x	1	0	x	0x0001 0000
Position 3	E	0xEnnn nnnn	x	0	1	x	0x0000 8000

The following information describes the entries in the table above:

Stack Position: Stack position 1 is closest to the Model 4283 baseboard (first position)

Stack position 2 is the second or middle stack position

Stack position 3 is the third or last position, farthest away from the Model 4283

Z digit: The Z digit is the module select digit and is the most sigificant MIX address digit. This is the first digit of the MIX_base Address, referenced in the MIX Address Map shown in Chapter 3 of the manual.

x: These bits are involved with other operations of the Model 4283. See the note in the paragraph above and refer to the Model 4283 manual for complete details.

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D.2 Model 4283 MIX Module Selection (continued)

n: MIX-module-specific MIX address hex digits independent of stack position.

D.3 Model 4283 Register Selection within the Module

Once the module has been selected, all registers of the MIX module appear in the 'C30 address map according to Table D-2, below right. Accessing these registers is accomplished by simply reading and writing to these locations.

This addressing corresponds to 32-bit word addresses for the TMS320C30 even though many of the elements may correspond to 8-bit or 16-bit devices.

Although the 'MIX' bus uses byte addressing, the MIX module must be addressed with 32-bit data words as shown in the map. The Model 4283 baseboard conducts only 32-bit accesses and all addresses are located on four-byte MIX bus address boundaries (least significant address digits of 0, 4, 8, or C).

Notation used in the table at the right uses conventions followed in the 'C' language where a '0x' prefix designates a hex number. The number of hex digits reflects the range of the number. The MIX address is expressed as an 8-digit number (32-bit value) while the 'C30 addresses are expressed as a 6-digit number (24-bit value). The space in front of the last four digits improves readability.

Table D-2, at the right, shows the correspondence between several 'C30 addresses for the Model 4283 and the equivalent MIX addresses. Note that the MIX address space for the Model 4283 MIX baseboard begins at 'C30 address 0x80 4000. Each successive 'C30 address represents an increment of 4 in the MIX address.

Table D-2: Address Translation between Model 4283 'C30 Address and MIX Address

MIX Address	'C30 Address
0xZ000 0048	0x80 4012
0xZ000 0044	0x80 4011
0xZ000 0040	0x80 4010
0xZ000 003C	0x80 400F
0xZ000 0038	0x80 400E
0xZ000 0034	0x80 400D
0xZ000 0030	0x80 400C
0xZ000 002C	0x80 400B
0xZ000 0028	0x80 400A
0xZ000 0024	0x80 4009
0xZ000 0020	0x80 4008
0xZ000 001C	0x80 4007
0xZ000 0018	0x80 4006
0xZ000 0014	0x80 4005
0xZ000 0010	0x80 4004
0xZ000 000C	0x80 4003
0xZ000 0008	0x80 4002
0xZ000 0004	0x80 4001
0xZ000 0000	0x80 4000

Z = 'C' for first or bottom MIX stack position
'D' for second or middle MIX stack position
'E' for third or top MIX stack position

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D.3 Model 4283 Register Selection within the Module (continued)

In general, the formulas for hex conversion between a MIX address and an equivalent 'C30 address are given by:

'C30 Address = (MIX Address - 0xZ000 0000) / 4

MIX Address = 0xZ000 0000 + 4 x ('C30 Address - 0x80 4000)

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