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INSTALLATION MANUAL

MODEL 53620

3–Channel 200 MHz A/D, 2–Channel 800 MHz D/A
Cobalt Family VPX Board



PENTEK

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Manual Revision History

Date	Revision	Comments
8/13/10	Preliminary	Initial release.
8/30/10		Sect 2.5, added 71620 PCB jumper block J28.
6/27/11	A	Release manual revision A.
3/15/12	2.0	Revison number upgrade. Updated 53620 assembly, switches, and jum pers for Model 5306 carrier. Sect 2.8.2, revised Crosspoint Switch configuration settings. Sect 2.10.5, revised VPX P2 connector pin map.
4/24/12	2.1	Sect 2.13.1, corrected external clock input voltage limit to +10 dBm.
11/21/12	2.2	Sect 2.9.1, corrected LED D40 to +12V power good, Sect 2.11, added note for Option 703/763.
2/15/13	2.3	Sect 2.9.1, removed D43 from LED list (D43 is a rectifier).
5/31/13	2.4	Sect 2.10.4, corrected pin mapping of VPX P1 connector (E10 & E11 reversed).
9/19/13	2.5	Sect 2.11 & Sect 2.12, added Option 741 installation note and front panel.
4/1/14	2.6	Sect 2.4.2, changed XMC switch SW2−5 default to OFF, factory use only.

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Chapter 1: Introduction

1.1 General Description

Pentek's Cobalt® Family Model 53620 is a multichannel, high−speed analog data converter. Using the VPX 3U card format, the 53620 includes three 200−MHz, 16−bit A/D converters and two 800−MHz D/A upconverters.

The Model 53620 consists of one Pentek Model 71620 XMC module mounted on a Pentek Model 5306 3U VPX carrier, assembled and tested as a single board. It is ready to plug into a chassis with a single 3U VPX slot.

1.2 Features

The Model 53620 includes one 71620 XMC module with the following features

- Three 200−MHz 16−bit A/D converters
- Two 800 MSPS 16−bit D/A converters
- Xilinx® Virtex®−6 FPGA
- Up to 32 MB of QDRII+ SRAM or 2 GB of DDR3 SDRAM
- Clock synthesizer with independent A/D and D/A rates
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express® (PCIe®) Gen 2 interface up to x8 wide
- LVDS connections to the Virtex−6 FPGA for custom I/O
- Rugged and conduction−cooled versions available

1.3 Model 53620 Documentation

This Model 53620 Installation Manual describes the installation and connections for the 53620 VPX assembly. Documentation of the 71620 XMC operation and programming is provided in the supplied Model 71620 Operating Manual, Pentek document #800.71620.

Data sheets for the programmable devices on the Model 71620 are provided in the Pentek Model 7x620 Series Supplemental Manual, part number 809.7x620. This document is available on the CD provided by Pentek, in file **`8097x620.pdf`** (PDF format).

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1.4 Block Diagram

The following is a simplified block diagram of the Model 53620.

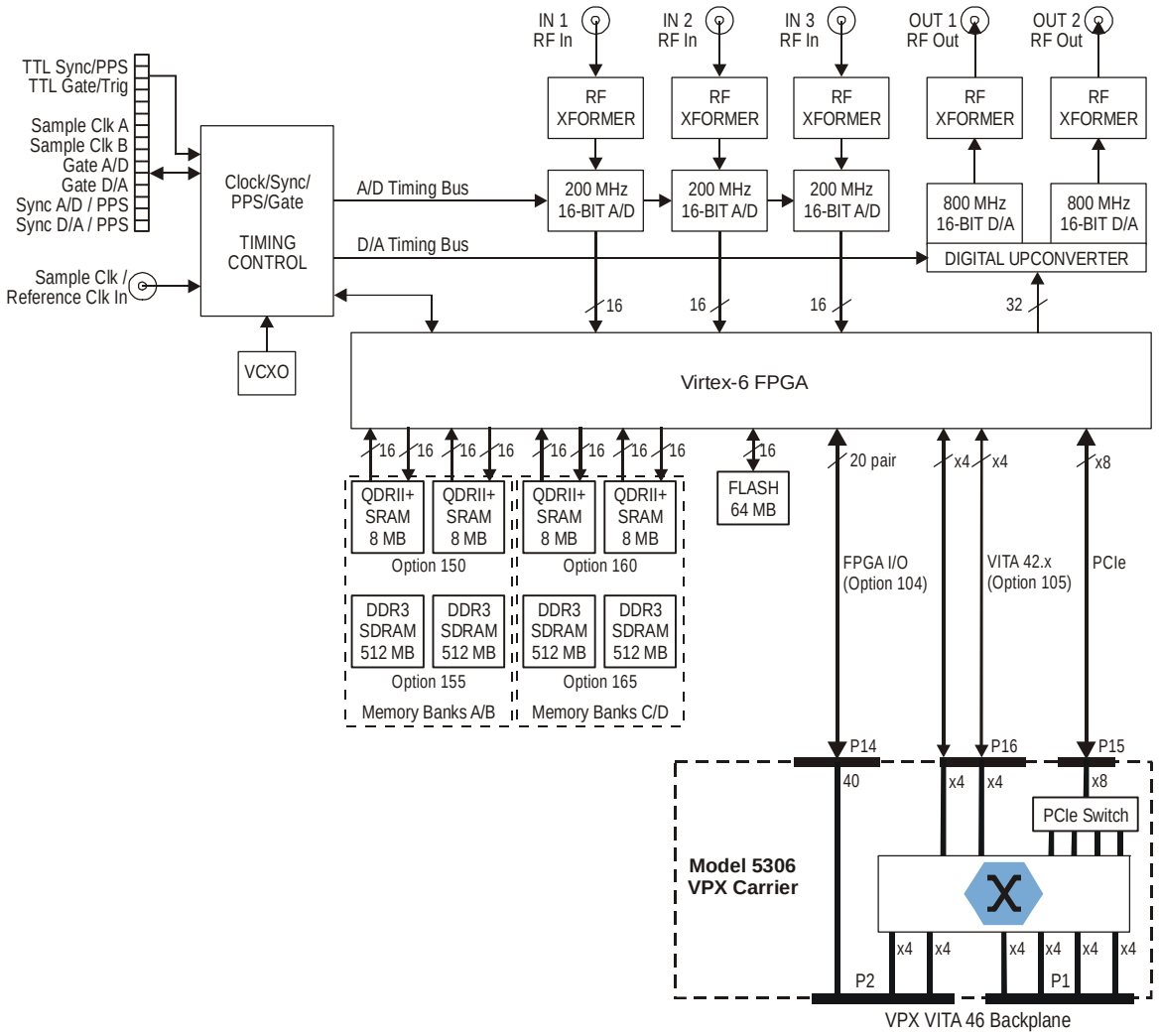


Figure 1–1: Model 53620 Block Diagram

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1.5 Principle of Operation

The Model 53620 consists of one Pentek Model 71620 XMC module mounted on a Pentek Model 5306 VPX carrier, assembled and tested as a single board. It is ready to plug into a chassis with a single 3U VPX slot.

The Model 71620 XMC features a Xilinx Virtex−6 FPGA for signal interfaces and processing. The FPGA is pre−configured to provide signal acquisition buffering functions. This FPGA also provides board interfaces including PCIe and XMC. Custom I/O connections are provided to the FPGA through the optional PMC P14 connector (Option 104). Custom gigabit serial interfaces may be implemented through the optional XMC P16 connector (Option 105).

The 71620 XMC includes three A/D converters and two D/A converters. Three 200−MHz, 16−bit A/D converters provide data to the FPGA, where the data can be formatted, processed, or routed to board resources. Two D/A converters include both interpolation filters and an upconverter stage capable of producing baseband I & Q and quadrature modulation analog output.

The 71620 XMC includes up to 32 MBytes of QDRII+ SRAM, or 2 GBytes of DDR3 SDRAM. This memory is controlled by the FPGA and is organized as two or four banks, depending on the 71620 options ordered. Separate banks (separate address and data per bank) allow simultaneous access to all banks. This memory can be used as data capture, as buffer memory when transferring data between board resources or to off−board resources, or as a memory resource for custom FPGA applications.

The 71620 XMC includes an onboard VCXO and a programmable clock synthesizer for clocking, but can also accept external clocks through front panel connectors. The 71620 is equipped with an LVPECL front panel sync bus that allows synchronizing A/D and D/A processing on multiple modules.

The 5306 VPX carrier features a fabric−transparent Crosspoint Switch, providing connectivity among various board components. The switch provides four x4 gigabit serial paths to the VPX−P1 connector and two x4 gigabit serial paths to the VPX−P2 connector. These are wired in accordance with VITA 46.0 (VPX Baseline Standard specification). The Crosspoint Switch also provides four x4 gigabit serial data paths through a Gen 2 PCIe Switch to the 71620 XMC P15 connector, and two x4 gigabit serial data paths directly to the 71620 XMC P16 connector to support switched interconnect protocols including Serial RapidIO, PCI Express, and Aurora. User I/O is supported with 20 differential pairs from the 71620 PMC P14 connector to the VPX−P2 connector.

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1.6 Specifications

71620 XMC Module Specifications

Refer to the Model 71620 Operating Manual, Pentek document #800.71620

Carrier XMC Interface

Primary XMC Connector:	**J15**, 114−pin XMC standard J15 connector
J15 Connectivity:	One PCIe x8 link to PCI Express Switch
Speed:	x8 link supports data rates up to 5 Gbps
Secondary XMC Connector:	**J16**, 114−pin XMC standard J16 connector, supports VITA 42 standard protocols
J16 Connectivity:	Two x4 links to Crosspoint Switch
Speed:	x4 links support data rates up to 3.125 Gbps

Carrier PMC Interface

PMC Connector:	**J14**, 64−pin PMC standard J14 connector
J14 Connectivity:	40 I/O lines directly wired to VPX−P2 connector for 71620 user I/O

Carrier PCI Express Switch

Device:	PLX® ExpressLane™ PEX 8648 PCI Express Switch
Switching:	48−Lane, 12−Port PCI Express Switch
Data Rates:	2.5/5 Gbps per lane
Interfaces:	
XMC Site J15 Connector:	One PCIe x8 path
Crosspoint Switch:	Four x4 Gbit Serial Ports

Carrier Crosspoint Switch

Device:	Mindspeed® M21148 Crosspoint Switch
Switching Matrix:	48 x 48 ports
Data Rates:	DC to 6.25 Gbps per lane
Interfaces:	
PCI Express Switch:	Four x4 Gbit Serial Ports (to 5 Gbps)
XMC Site J16 Connector:	Two x4 Gbit Serial Ports (to 3.125 Gbps)
VPX−P1 Connector:	Four x4 Gbit Serial Ports (to 3.125 Gbps)
VPX−P2 Connector:	Two x4 Gbit Serial Ports (to 3.125 Gbps)

VPX Interface

Utility Connector:	**P0**, pinout per VITA 46.0
Payload Connector:	**P1**, four x4 Gbit Serial ports to Crosspoint Switch
Module Connector:	**P2**, two x4 Gbit Serial ports to Crosspoint Switch, plus 40 I/O lines to PMC **J14** for 71620 user I/O

Power Consumption

5306 Carrier:	14.5 Watts typ, 17.5 Watts max		
71620 XMC:	**+3.3V**	**VPWR(12V or 5V)**	**Total Power**
XC6VLX130T	2A	1.95A@12V or 4.7A@5V	30 Watts
XC6VLX240T	2.3A	2A@12V or 4.8A@5V	32 Watts

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1.6 Specifications (continued)

Physical

Form Factor: 3U VPX

Weight:

VPX Carrier:	110 grams (3.9 oz)
XMC Module:	Approximately 14 oz (400 grams), with 2−slot heatsink

Environmental

Commercial

Cooling Method:	Forced Air
Operating Temperature:	0° to 50°C
Storage Temperature:	−20° to +90°C
Relative Humidity:	0 to 95% non−condensing

Pentek Ruggedization Level L1 (Option −701)

Cooling Method	Forced Air
Operating Temperature:	0° to +50°C
Storage Temperature:	−40° to +100°C
Relative Humidity:	0 to 95% non−condensing
Sine Vibration:	2g, 20−500 Hz
Random Vibration:	$0.01g^2$, 20−2000 Hz
Shock:	10g, 11mS

Pentek Ruggedization Level L2 (Option −702)

Cooling Method:	Forced Air
Operating Temperature:	−20° to +60°C
Storage Temperature:	−40° to +100°C
Relative Humidity:	
No conformal coating:	0% to 95% non−condensing
Conformal coating (Option 720):	0% to 100% non−condensing
Sine Vibration:	2g, 20−500 Hz
Random Vibration:	$0.04g^2$, 20−2000 Hz
Shock:	20g, 11mS

Pentek Ruggedization Level L3 (Option −703)

Cooling Method (operational):	Conduction Cooled
Operating Temperature:	−40° to +70°C
Storage Temperature:	−50° to +100°C
Relative Humidity:	
No conformal coating:	0% to 95% non−condensing
Conformal coating (Option 720):	0% to 100% non−condensing
Sine Vibration:	10g, 20−2000 Hz
Random Vibration:	$0.1g^2$, 20−2000 Hz
Shock:	30g, 11mS

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking, inspect the unit carefully for possible damage to connectors or components. If any damage is discovered, contact Pentek immediately at (201) 818–5900. Please save the shipping container and packing material in case reshipment is required.

The following figure illustrates the Model 53620 assembly, with the 71620 XMC module mounted onto the 5306 VPX carrier.

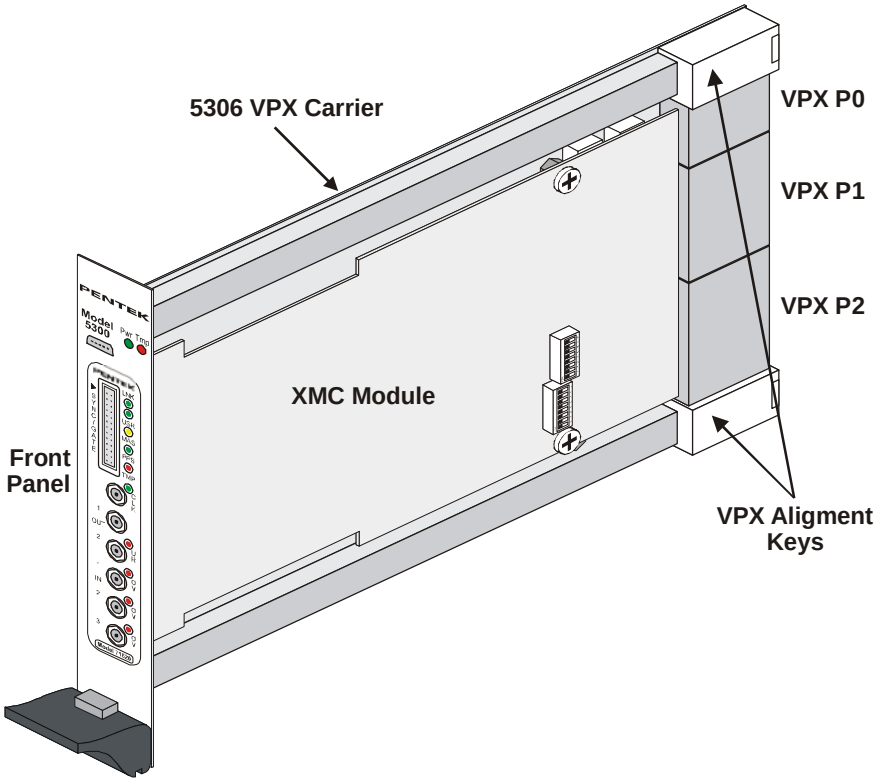


Figure 2–1: Model 53620 VPX Assembly

Note that a cooling assembly/heat–sink may be mounted on the 71620 XMC module as shipped from the factory.

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2.2 Jumper and Switch Settings

The following sections describe user operating parameters that are set by shorting jumpers or DIP switches on the Model 53620.

The shorting jumpers used on the Model 53620 are for 0.020" (0.51 mm) square pins spaced on 0.079" (2.00 mm) centers. These jumpers are NorComp part number 810–002–LP1R001, or equivalent. Pentek's part number for these jumpers is 356.00015.

The Model 53620 assembly includes one Pentek 71620 XMC module mounted on a Pentek Model 5306 VPX carrier as illustrated in Figure 2–1 on the prior page. As shipped, the 71620 XMC module is mounted onto the 5306 carrier.

As shipped from the factory, all jumpers and switches are installed in default positions on your board. The default operating parameters selected may or may not meet your requirements. Before installing your Model 53620 assembly, please review the following sections to determine whether you need to change any of these settings.

- Refer to Section 2.4 for the switch settings and Section 2.5 for the jumper settings on the 71620 XMC module. All switch blocks are accessible in the shipped configuration. If you need to access the jumpers on the XMC, you must first remove the XMC module from the VPX carrier, as described in Section 2.3.

- Refer to Section 2.7 for the jumper settings and Section 2.8 for the switch settings on the VPX carrier. All switch blocks are accessible in the shipped configuration. If you need to access the jumpers on the VPX carrier, you must first remove the XMC module from the VPX carrier, as described in Section 2.3.



Do not change jumpers or switches that are not described in this chapter—those are reserved for factory test and setup purposes only.

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2.3 Removing XMC Module from VPX Carrier

CAUTION

Perform all steps at a static–controlled work workstation.

1) From the solder side of the Model 53620 assembly (side opposite the 71620 XMC), unscrew the four Phillips mounting screws, as identified below.

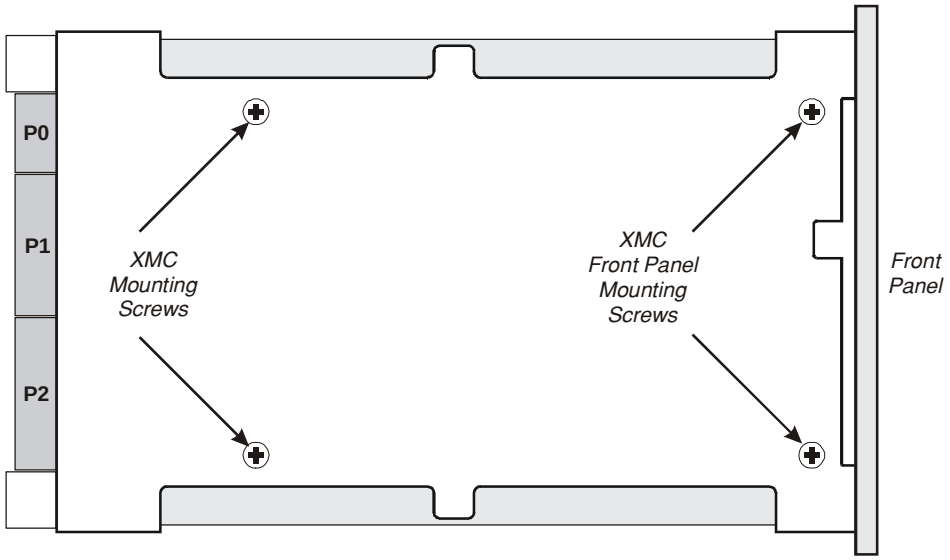


Figure 2–2: Removing 71620 XMC from VPX carrier

2) From the XMC module side, **GENTLY**, pull on the XMC card to disengage the card's connectors from the VPX carrier's XMC connectors.

After jumper or switch changes, replace the XMC onto the VPX carrier as follows.

1) Position the 71620 XMC module's front panel into the VPX carrier's panel opening from behind the VPX carrier slot panel, and align the 71620 XMC module so that the connectors on the XMC card are aligned over the connectors on the VPX carrier.

2) **GENTLY but firmly**, press down on the areas of the XMC opposite the connectors to fully seat the card's connectors into the carrier. The connectors on the XMC should connect smoothly with the corresponding connectors on the carrier.

3) From the solder side of the VPX carrier, secure the XMC to the carrier by screwing the four mounting screws (those removed above) through the VPX carrier into the XMC, as illustrated above.

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2.4 XMC Module Switches

The following subsections describe 71620 XMC module user operating parameters that are set by two DIP switches, identified as **SW1** and **SW2**, on the 71620 main PCB (Pentek part number 320–71600).

Both switch blocks are located on the solder side of the 71620 PCB and are accessible while the 71620 is mounted on the VPX carrier. An assembly drawing of the solder side of the 71620 main PCB is provided below, showing the location of switches **SW1** and **SW2** on the PCB.

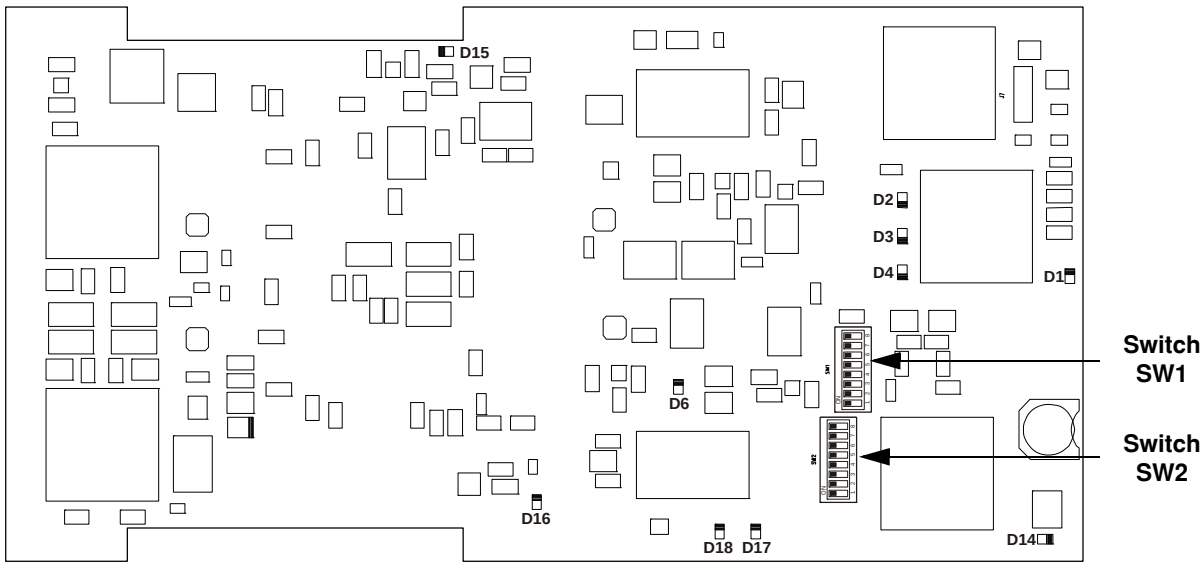


Figure 2–3: Model 71620 Main PCB, Solder Side

Note that several user LEDs are located on the solder side of the 71620 PCB. Refer to Section 2.6, on page 18 for description of these LEDs.

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2.4 XMC Module Switches (continued)

2.4.1 Switch SW1 – FPGA MGT Clock Operation

Switch **SW1** provides user control over the FPGA MGT clocks used for the XMC interface. The following table shows the settings for this switch.

CAUTION

Use ballpoint tip only for setting DIP switches.

DO NOT USE paper clips, tweezers, or any other sharp objects, as they may damage the switch.

Table 2–1: SW1 – FPGA MGT Clock Operation

Switch	Function	ON	OFF
SW1–1	Primary PCIe Clock Frequency **	100 MHz	250 MHz *
SW1–2	Secondary PCIe Clock Frequency	100 MHz	250 MHz *
SW1–3	Auxiliary MGT Clocks (A/B/C) Frequency	See Table 2–2 below	
SW1–4			
SW1–5	Secondary PCIe Clock Disable	Disabled *	Enabled
SW1–6	Auxiliary MGT Clocks (A/B/C) Disable	Disabled *	Enabled
SW1–7	Primary PCIe Clock Source	XMC CLK0 *	250 MHz Crystal
SW1–8	Secondary PCIe Clock Source ***	XMC CLK1	AUX_MGT_CLK_A *

* Factory Default Settings

** Switch **SW1–1** must be **OFF** (250 MHz) position for Pentek factory FPGA code and for any x8 or Gen 2 design.

*** Switch **SW1–8**, when in the **ON** position clock source is the Option 105 XMC P16 connector – if option 105 is not installed switch must be in the **OFF** position.

Table 2–2: Aux MGT Clock Frequency – Switches SW1–3:4

SW1–3	SW1–4	Aux MGT Clk A/B	Aux MGT Clk C
OFF *	OFF *	312.5 MHZ	125 MHz
ON	OFF	156.25 MHz	125 MHz
OFF	ON	125 MHz	156.25 MHz
ON	ON	156.25 MHz	156.25 MHz

* Factory Default Setting

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2.4 XMC Module Switches (continued)

2.4.2 Switch SW2 – FPGA Configuration

Switch **SW2** controls access to the FPGA configuration functions. The following table shows the settings for this switch.

CAUTION

Use ballpoint tip only for setting DIP switches.

DO NOT USE paper clips, tweezers, or any other sharp objects, as they may damage the switch.

Table 2–3: SW2 – FPGA Configuration

Switch	Function	ON	OFF
SW2–1	FLASH Memory Write Protect/Write Enable	Write Protected *	Write Enabled
SW2–2	Factory use only – should always be set to **ON**		
SW2–3	Select Boot Configuration at power on	See Table 2–4 below	
SW2–4			
SW2–5	Factory use only – should always be set to **OFF**		
SW2–6	no function	–	–
SW2–7	XMC JTAG Enable	XMC JTAG	Board JTAG *
SW2–8	Select whether JTAG chain includes Memory	FPGA & Memory	FPGA Only *
	Note: Factory use only – should always be set to **OFF**, FPGA only.		
* Factory Default Settings			

Table 2–4: FPGA Configuration Select – Switches SW2–3:4

SW2–3	SW2–4	Configuration Select (FLASH)
ON *	ON *	Version 0 Boot Code – Gen 1 x8 PCIe
OFF	ON	Version 1 Boot Code – Gen 2 x4 PCIe
ON	OFF	Version 2 Boot Code
OFF	OFF	Version 3 Boot Code
* Factory Default Setting Refer to the 71620 Operating Manual, #800.71620, for FLASH Memory use.		

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2.5 XMC Module Jumpers

The following describes user operating parameters that are set by jumper block **J28** on the 71620 XMC main PCB (Pentek part number 320–71600). This jumper block is located on the connector side of the 71620 PCB. An assembly drawing of the connector side of the PCB is provided below, showing the location of jumper block **J28**.

NOTE: To access **J28**, you must remove the XMC module from the VPX carrier, as described in Section 2.3.

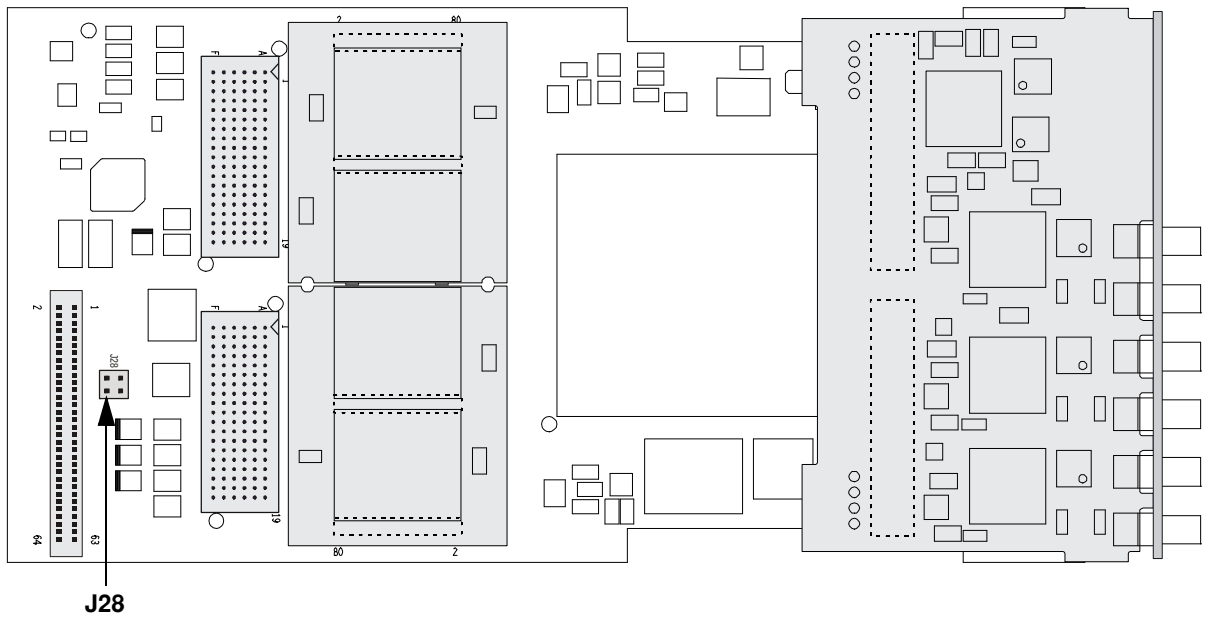


Figure 2–4: Model 71620 PCB Jumpers, Connector Side

Table 2–5: Virtex–6 Program eFUSE Enable – Jumper Block J28

Jumper Pins	Function	Installed	Removed
Pins 1 – 3	Virtex–6 Program eFUSE	Enabled	Disabled *
Pins 2 – 4	no function	–	–
* Factory Default Setting			

Jumper **J28**, pins 1–3, are used to program eFUSE in the Virtex–6 FPGA. Refer to the Xilinx Virtex–6 FPGA Configuration Guide (Xilinx document UG360) for further information about using this capability.

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2.6 XMC Module LEDs

The following describes the 71620 PCB LEDs, labeled **Dnn**, that provide general operating status of the board. These LEDs are positioned on the solder side of the PCB, as illustrated below, and are visible through the heat−sink mounted on the PCB. The use of each LED is indicted in Table 2−6 below.

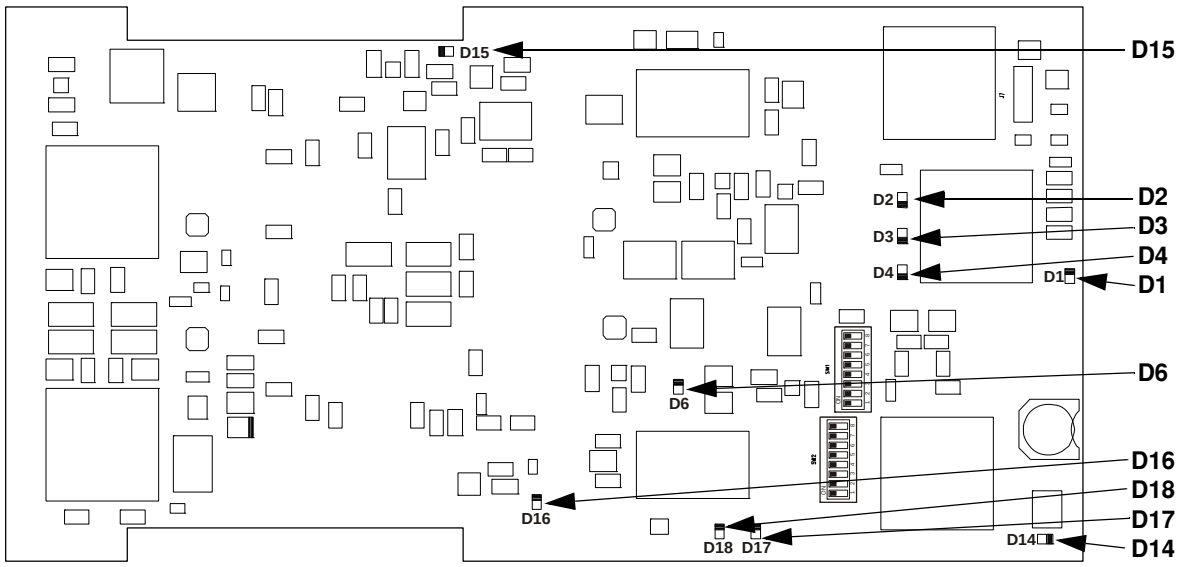


Figure 2−5: Model 71620 PCB LEDs, Solder Side

Table 2−6: PCB LED Use

LED	USE
D1	Yellow LED indicates PCI Express Gen 2 operation
D2 & D3	Yellow LEDs indicate PCI Express Active Lanes:

	x1	x2	x4	x8
D2	Off	On	Off	On
D3	Off	Off	On	On

D4	Green LED indicates PCI Express link has been established
D6	Green LED for user applications
D14	Red LED indicates temperature fault from the main PCB LM83
D15	Red LED indicates temp/volt fault from the System Monitor
D16	Green LED indicates FPGA configuration done
D17	Red LED indicates FPGA configuration error
D18	Yellow LED indicates FPGA configuration active

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2.7 VPX Carrier Jumpers

The following subsections describe operating parameters that are set by shorting jumpers, labeled **JBn** on the 5306 VPX carrier PCB. Refer to Section 2.8 for the DIP switch settings on the carrier PCB.

NOTE: To access all jumpers, you must remove the XMC module from the carrier, as described in Section 2.3.

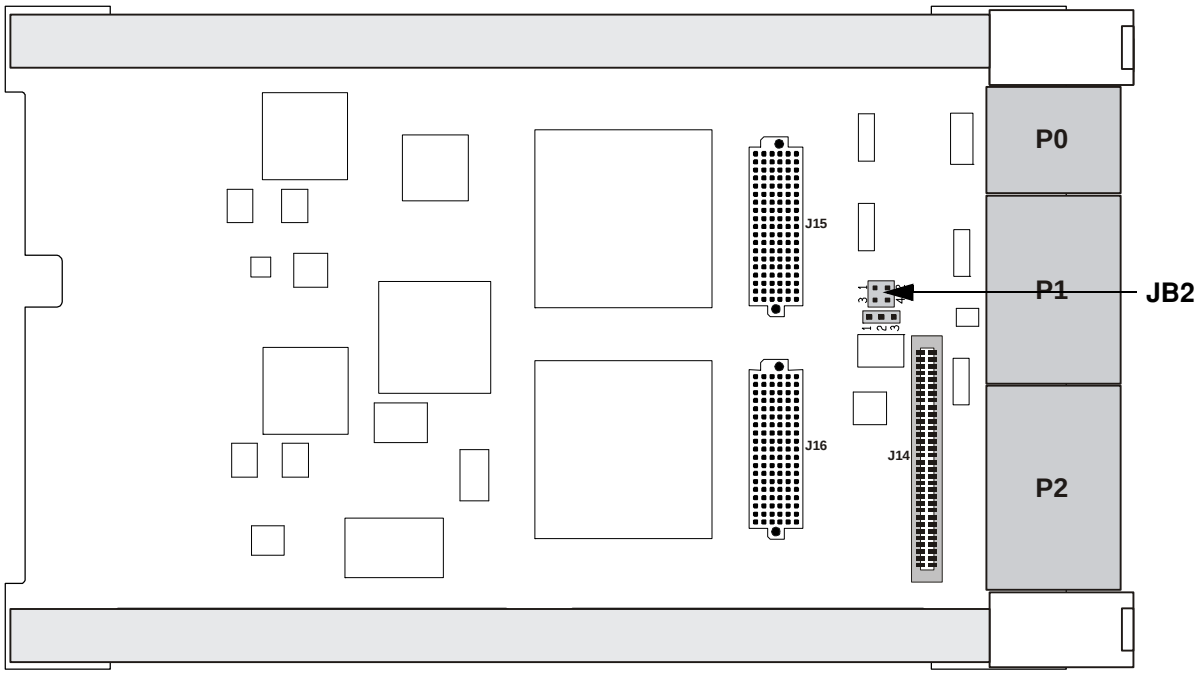


Figure 2–6: Model 5306 VPX Carrier PCB Assembly, Connector Side

Jumper block **JB2** is for factory use only.

Table 2–7: Factory Default Jumpers – Jumper Block JB2

Jumper Position	Jumper State	Function
Pins 1 – 2	Installed *	XMC JTAG JTDI
Pins 3 – 4	Installed *	XMC JTAG JTDO
* Factory Default Settings		

Jumper block **JB3** is reserved for future use.

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2.8 VPX Carrier Switches

The following subsections describe operating parameters that are set by DIP switches, labeled **SWn** on the 5306 VPX carrier PCB. Refer to Section 2.7 for the jumper settings on the carrier PCB.

The following drawing shows the location of all DIP switches, on the solder side of the 5306 carrier PCB.

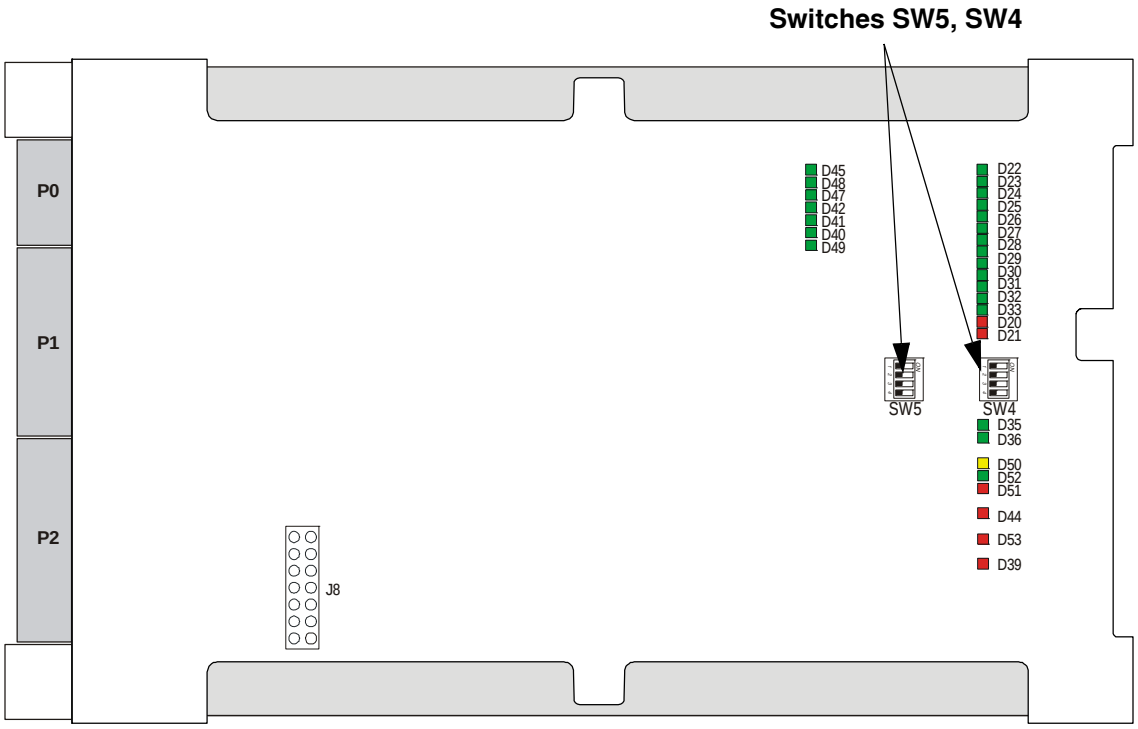


Figure 2–7: Model 5306 VPX Carrier Assembly, Solder Side

Refer to Section 2.9 for descriptions of the carrier PCB LEDs (labeled **Dnn**) depicted in the illustration above.

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2.8 VPX Carrier Switches (continued)

2.8.1 Configuration – Switch SW5

DIP switch **SW5** selects. The following table describes the switch settings.

Table 2–8: Configuration Control – SW5–1:4

Switch	Function	Position	Operating Mode
SW5–1	SPI_PGM_ENAB	OFF *	FLASH memory write inhibited
		ON	FLASH memory write enabled
SW5–2	GA_ENAB	OFF *	Switch SW4 selects configuration (Section 2.8.2)
		ON	Geographical addressing selects configuration
SW5–3	XMC_MVMRO	OFF *	XMC MVMRO Enabled
		ON	XMC MVMRO Disabled
SW5–4	VPX Clock	ON *	On–board oscillator
		OFF	VPX backplane clock
* Factory Default Setting			

2.8.2 Crosspoint Switch Routing – Switch SW4

NOTE: Switch **SW4** is valid only when switch **SW5–2** (above) is set **OFF**.

DIP switch **SW4** selects a Crosspoint Switch routing configuration, stored in Flash memory, that will load on power–up. Five default configurations are provided for the Model 53620. The switch settings for each of these configurations are shown in the following table, and each routing path is illustrated on the following pages.

Table 2–9: Crosspoint Switch Routing – SW4

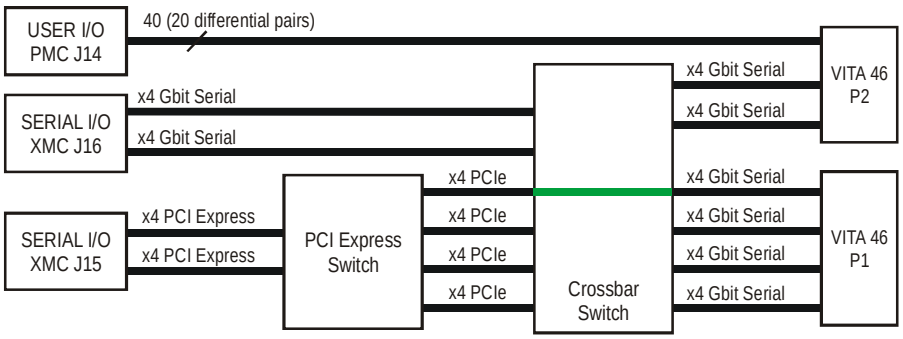
User Configuration	SW4				VPX P1 Interface	VPX P2 Interface
	4	3	2	1		
n0000 *	ON	ON	ON	ON	One PCIe x4 link: 0–3	none
n0001	ON	ON	ON	OFF	Two PCIe x4 links: 0–3, 4–7	none
n0010	ON	ON	OFF	ON	One PCIe x4 link: 0–3	XMC P16 two x4 links: 0–3, 4–7
n0011	ON	ON	OFF	OFF	Two PCIe x4 links: 0–3, 4–7	XMC P16 two x4 links: 0–3, 4–7
n0100	ON	OFF	ON	ON	Four PCIe x4 links: 0–3, 4–7, 8–11, 12–15	XMC P16 two x4 links: 0–3, 4–7
* Factory Default Setting User Configuration, MSB n = switch SW5–4 setting, Section 2.8.1 (0 = On–board oscillator, 1 = VPX clock)						

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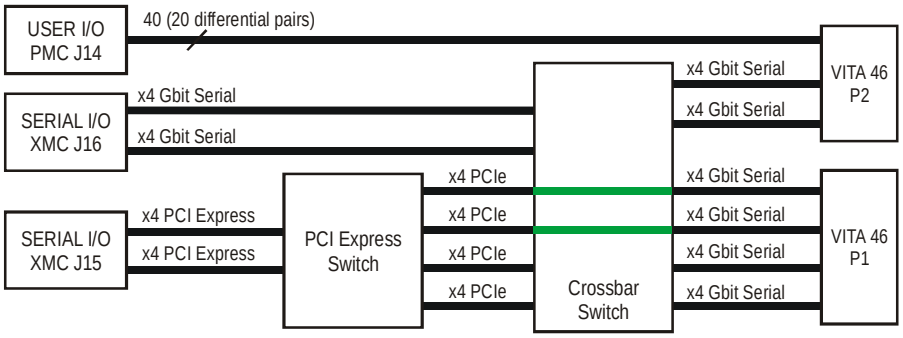
2.8 VPX Carrier Switches (continued)

2.8.2 Crosspoint Switch Routing (continued)

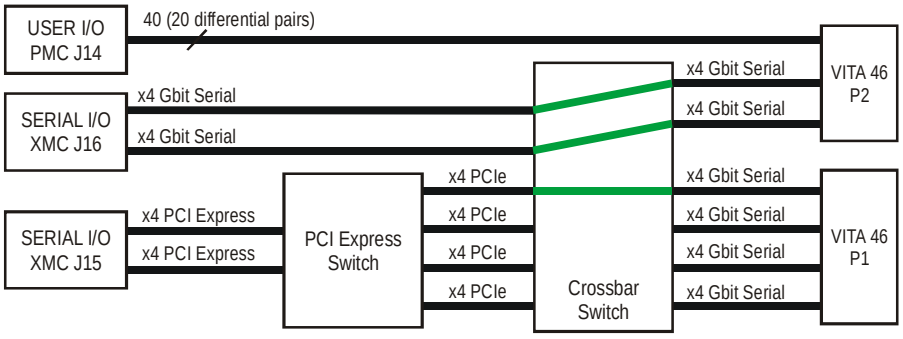
1) Configuration n0000 – one PCIe x4 link between XMC P15 and VPX P1; no connection between XMC P16 and VPX P2.



2) Configuration n0001 – two PCIe x4 links between XMC P15 and VPX P1; no connection between XMC P16 and VPX P2.



3) Configuration n0010 – one PCIe x4 link between XMC P15 and VPX P1; two x4 links between XMC P16 and VPX P2.

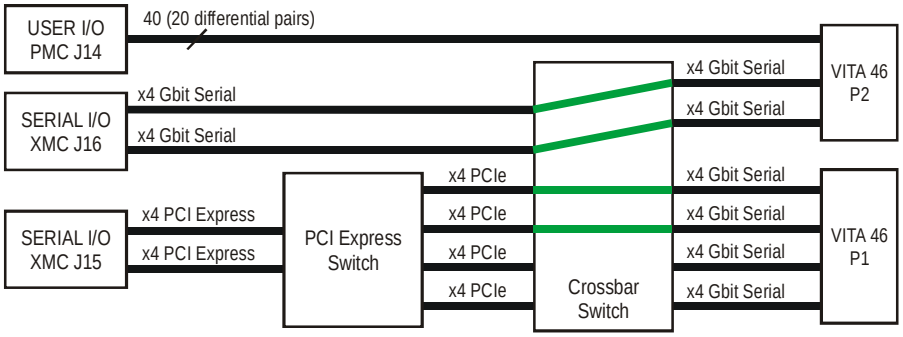


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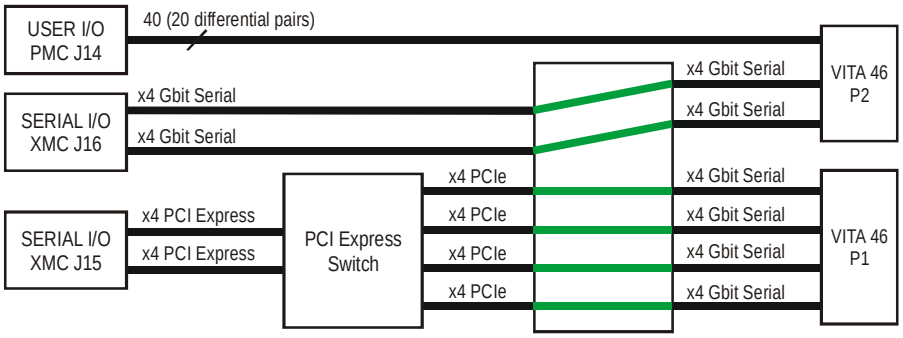
2.8 VPX Carrier Switches (continued)

2.8.2 Crosspoint Switch Routing (continued)

4) Configurations n0011 – two PCIe x4 links between XMC P15 and VPX P1; two x4 links between XMC P16 and VPX P2.



5) Configuration n0100 – four PCIe x4 links between XMC P15 and VPX P1; two x4 links between XMC P16 and VPX P2.



For alternate configurations, please contact Pentek.

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2.9 VPX Carrier LEDs

The following subsections describe the LEDs, labeled **Dnn** on the 5306 VPX carrier PCB, that provide general operating status for the board. Most LEDs are located on the sol–der side of the PCB. The following PCB drawing shows the location of all LEDs.

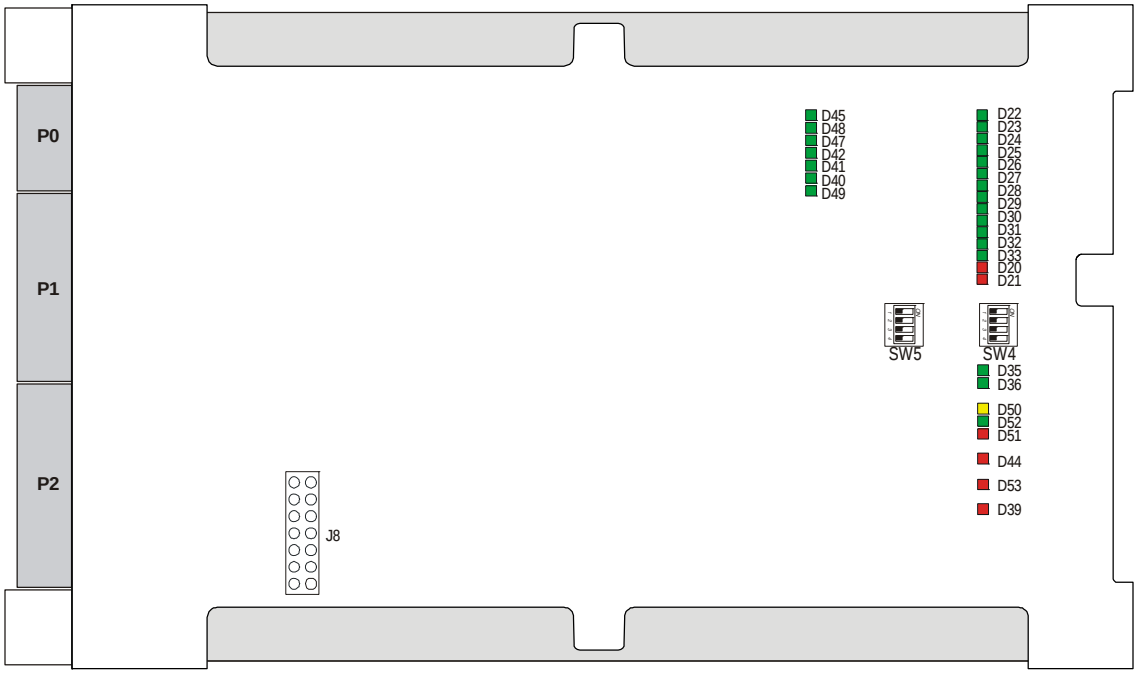


Figure 2–8: Model 5306 VPX Carrier Assembly, Solder Side

2.9.1 Power LEDs

The following LEDs indicate power applied to board resources.

LED	Indication
D40	Green LED indicates +12V power good
D41	Green LED indicates +5V power good
D42	Green LED indicates +3.3V power good
D45	Green LED indicates +1.2V power good
D47	Green LED indicates +2.5V power good
D48	Green LED indicates +1.8V power good
D49	Green LED indicates 5/12V power good to XMC Site

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2.9 VPX Carrier LEDs (continued)

2.9.2 PCI Express LEDs

The following LEDs indicate PCI Express Bus (PEX8648) activity.

LED	Indication
D20	Red LED indicates PCIe interrupt (PEX8648 INT A)
D21	Red LED indicates PCIe is not functioning properly (FATAL ERR)
D22	Green LED indicates activity on PEX8648 Port 0
D23	Green LED indicates activity on PEX8648 Port 1
D24	Green LED indicates activity on PEX8648 Port 2
D25	Green LED indicates activity on PEX8648 Port 3
D26	Green LED indicates activity on PEX8648 Port 4
D27	Green LED indicates activity on PEX8648 Port 5
D28	Green LED indicates activity on PEX8648 Port 6
D29	Green LED indicates activity on PEX8648 Port 7
D30	Green LED indicates activity on PEX8648 Port 8
D31	Green LED indicates activity on PEX8648 Port 9
D32	Green LED indicates activity on PEX8648 Port 10
D33	Green LED indicates activity on PEX8648 Port 11

2.9.3 Miscellaneous LEDs

LED	Indication
D35	Green LED indicates reference clock detected
D36	Green LED indicates input clock detected
D39	Red LED indicates board is in reset
D44	Red LED indicates Crosspoint Switch alarm or overtemperature *
D50	Yellow LED indicates Crosspoint Switch cannot be programmed
D51	Red LED indicates Crosspoint Switch programming error
D52	Green LED indicates Crosspoint Switch programming done
D53	Red LED indicates I2C bus acknowledge error
* LED **D44** and front panel Tmp LED (Section 2.12.2) can be programmed for either overtemp or Crosspoint Switch alarm – that is, when one indicates temperature, the other indicates Crosspoint Switch alarm	

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2.10 VPX Carrier Connectors

The following subsections describe the signal connectors on the 5306 VPX carrier PCB. Refer to Figure 2–6 on page 19 for the location of these connectors on the carrier PCB. The following is a simplified block diagram of the VPX carrier, showing the signal routing of the PMC, XMC, and VPX connectors.

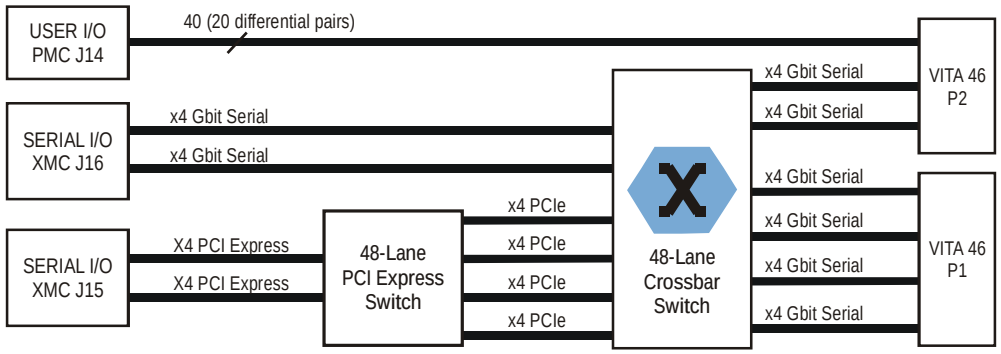


Figure 2–9: VPX Carrier Block Diagram

2.10.1 XMC Connectors

The 5306 VPX carrier provides two XMC connectors, designated **J15** and **J16** on the carrier PCB. **J15** provides one x8 (or two x4) PCI Express link between the XMC and the carrier. **J16** provides two x4 Gbit serial links between the XMC and the carrier for 71620 Option 105 Serial I/O.

Depending on the setting of switch **SW4** (Section 2.8.1), the carrier can route these data links from the XMC **J15** and **J16** connectors to the VPX **P1** and **P2** connectors. Refer to Sections 2.10.4 and 2.10.5 for the pin mapping of the VPX **P1** and **P2** connections.

2.10.2 PMC Connector

The 5306 VPX carrier provides one 64–pin PMC connector, designated **J14** on the carrier PCB. **J14** provides 40 pins defined as 'User I/O' to support custom PMC **J14** connectivity. On the VPX carrier, 20 differential pairs are directly wired from PMC **J14** to the VPX **P2** connector for user I/O.

Option 104 for the Model 71620 provides 20 signal pairs from FPGA spare pins to PMC connector **P14**. These connections are programmed for low–voltage differential signals (LVDS) in 71620 Option 104 default configura–tion. Refer to the supplied Model 71620 Operating Manual, 800.71620, for description of these **P14** signals. Refer to Section 2.10.5 for the pin mapping of the 5306 carrier PMC **J14** to VPX **P2** connections.

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2.10 VPX Carrier Connectors (continued)

2.10.3 VPX P0 Utility Connector

The VPX **P0** connector is pinned out in accordance with the VITA 46.0–2007 VPX Baseline Standard Specification. This connector is designated for Power Inputs, Geographical Address Inputs, System Management, System Reset, Reference Clock, NVMRO, and JTAG Signals per the VITA standard.

2.10.4 VPX P1 Payload Connector

The VPX **P1** connector routes full duplex VPX links from the Crosspoint Switch, as identified in Section 2.8.1. The following table shows how these are mapped for the 71620 XMC configurations.

Table 2–10: VPX P1 Connector Pin Mapping

Pin	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	nc	GND	P1-TD00_N	P1-TD00_P	GND	P1-RD00_N	P1-RD00_P
2	GND	P1-TD01_N	P1-TD01_P	GND	P1-RD01_N	P1-RD01_P	GND
3	nc	GND	P1-TD02_N	P1-TD02_P	GND	P1-RD02_N	P1-RD02_P
4	GND	P1-TD03_N	P1-TD03_P	GND	P1-RD03_N	P1-RD03_P	GND
5	SYS_CON_N	GND	P1-TD04_N	P1-TD04_P	GND	P1-RD04_N	P1-RD04_P
6	GND	P1-TD05_N	P1-TD05_P	GND	P1-RD05_N	P1-RD05_P	GND
7	nc	GND	P1-TD06_N	P1-TD06_P	GND	P1-RD06_N	P1-RD06_P
8	GND	P1-TD07_N	P1-TD07_P	GND	P1-RD07_N	P1-RD07_P	GND
9	nc	GND	P1-TD08_N	P1-TD08_P	GND	P1-RD08_N	P1-RD08_P
10	GND	P1-TD09_N	P1-TD09_P	GND	P1-RD09_N	P1-RD09_P	GND
11	nc	GND	P1-TD10_N	P1-TD10_P	GND	P1-RD10_N	P1-RD10_P
12	GND	P1-TD11_N	P1-TD11_P	GND	P1-RD11_N	P1-RD11_P	GND
13	nc	GND	P1-TD12_N	P1-TD12_P	GND	P1-RD12_N	P1-RD12_P
14	GND	P1-TD13_N	P1-TD13_P	GND	P1-RD13_N	P1-RD13_P	GND
15	nc	GND	P1-TD14_N	P1-TD14_P	GND	P1-RD14_N	P1-RD14_P
16	GND	P1-TD15_N	P1-TD15_P	GND	P1-RD15_N	P1-RD15_P	GND

PCI Express lanes are designated by P1_TDxx/P1_RDxx, where xx is the lane number.
P1_TD[00:15] – PCIe Transmit data from 5306 Crosspoint Switch to VPX bus (differential pairs).
P1_RD[00:15] – PCIe Receive data from VPX bus to 5306 Crosspoint Switch (differential pairs).

Note that the definition and utilization of these signals is dependent on the backplane wiring of the VPX slot and the 5306 Crosspoint Switch routing selected in Section 2.8.2.

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2.10 VPX Carrier Connectors (continued)

2.10.5 VPX P2 Module Connector

The VPX **P2** connector routes user I/O directly from the PMC **J14** connector, as described in Section 2.10.1, plus switched XMC **P16** connector signals from the Crosspoint Switch, as identified in Section 2.8.1. The following table shows the pin mapping of the VPX **P2** connector.

Table 2–11: VPX P2 Connector Pin Mapping

Pin	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	LVDS_OUT7_P	GND	P16_T0_N	P16_T0_P	GND	P16_R0_N	P16_R0_P
2	GND	P16_T1_N	P16_T1_P	GND	P16_R1_N	P16_R1_P	GND
3	LVDS_OUT7_N	GND	P16_T2_N	P16_T2_P	GND	P16_R2_N	P16_R2_P
4	GND	P16_T3_N	P16_T3_P	GND	P16_R3_N	P16_R3_P	GND
5	LVDS_OUT8_P	GND	P16_T4_N	P16_T4_P	GND	P16_R4_N	P16_R4_P
6	GND	P16_T5_N	P16_T5_P	GND	P16_R5_N	P16_R5_P	GND
7	LVDS_OUT8_N	GND	P16_T6_N	P16_T6_P	GND	P16_R6_N	P16_R6_P
8	GND	P16_T7_N	P16_T7_P	GND	P16_R7_N	P16 R7_P	GND
9	LVDS_IN7_P	GND	LVDS_IN0_N	LVDS_IN0_P	GND	LVDS_OUT0_N	LVDS_OUT0_P
10	GND	LVDS_IN1_N	LVDS_IN1_P	GND	LVDS_OUT1_N	LVDS_OUT1_P	GND
11	LVDS_IN7_N	GND	LVDS_IN2_N	LVDS_IN2_P	GND	LVDS_OUT2_N	LVDS_OUT2_P
12	GND	LVDS_IN3_N	LVDS_IN3_P	GND	LVDS_OUT3_N	LVDS_OUT3_P	GND
13	LVDS_IN8_P	GND	LVDS_IN4_N	LVDS_IN4_P	GND	LVDS_OUT4_N	LVDS_OUT4_P
14	GND	LVDS_IN5_N	LVDS_IN5_P	GND	LVDS_OUT5_N	LVDS_OUT5_P	GND
15	LVDS_IN8_N	GND	LVDS_IN6_N	LVDS_IN6_P	GND	LVDS_OUT6_N	LVDS_OUT6_P
16	GND	LVDS_IN_CLK_N	LVDS_IN_CLK_P	GND	LVDS_OUT_CLK_N	LVDS_OUT_CLK_P	GND

LVDS_IN[0:8, CLK] – Option 104 input data, differential pairs, to PMC J14 connector.
LVDS_OUT[0:8, CLK] – Option 104 output data, differential pairs, from PMC J14 connector.
P16_T[0:7] – XMC P16 Serial I/O Transmit data from Crosspoint Switch to VPX bus (differential pairs).
P16_R[0:7] – XMC P16 Serial I/O Receive data from VPX bus to Crosspoint Switch (differential pairs).

Note that the definition and utilization of these signals is dependent on the backplane wiring of the VPX slot and the 5306 Crosspoint Switch routing selected in Section 2.8.2.

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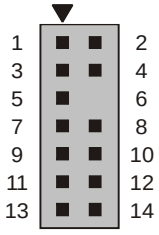
2.10 VPX Carrier Connectors (continued)

2.10.6 Pentek JTAG Connector

The Pentek JTAG **J8** connector provides a connection to download programs and to perform boundary–scan tests on VPX carrier devices. This connector is reserved for Pentek factory use only. The pinout for this 14–pin header is given in the following table.

Table 2–12: Pentek JTAG J8 Connector

Signal	Pin Number		Pin Number	Signal
TMS	1		2	TRST_N
TDI	3		4	GND
+3.3 V	5		6	No Pin
TDO	7		8	GND
No Connection	9		10	No Connection
TCK	11		12	GND
No Connection	13		14	No Connection



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2.11 Installing the Model 53620 in a VPX Card Cage

The Model 53620 is designed to operate in VPX systems. The carrier conforms to the 3U height VPX card format as per VITA 46.0 (VPX Baseline Standard specification).

CAUTION

REMOVE POWER to the VPX system backplane before installation!

To install the Model 53620 assembly in your VPX system:

1) Orient the VPX chassis on your work surface such that the front panel faces you.

2) Select a vacant VPX slot in which to install the Model 53620 assembly, and remove the blank cover plate on the front panel.

NOTE: If your Model 53620 has Option 741 you must use a 5HP width (1") VPX slot as illustrated in Figure 2–10 on the next page.

NOTE: The user should be aware that "any" vacant VPX slot may not work with the Model 53620. It is dependent on the backplane wiring of the VPX slot and the 5306 Crosspoint switch configuration selected (Sections 2.8.2).

3) Before touching the Model 53620 assembly, touch the case of your VPX chassis's power supply, to discharge any static electrical charge that may have accumulated on you. Then, remove the 53620 assembly from its anti–static packaging.

4) Install the card's connecting edge into the selected VPX slot.

NOTE: Be certain that the card edge is properly aligned with the VPX connector. Gentle pressure should be sufficient to seat the card edge in the connector.

DO NOT ATTEMPT TO FORCE THE CARD INTO THE SLOT!
If excessive force is necessary, then the card is probably misaligned. Damage to either the VPX motherboard or the VPX carrier will be the most likely result of attempts at forced installations.

5) After the 53620 assembly is fully and properly seated in the VPX connector, secure the card's front panel to the VPX chassis with the ejector.

Note

If your Model 53620 has Option 763 or Option 703 for mounting in a conduction–cooled VPX chassis, a 3/32" hex key (Pentek part # 900.10153) is provided to tighten the chassis locking nuts illustrated at the top and bottom of the Option 763/703 front panels in Figure 2–11 on page 32.

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2.12 VPX Carrier Front Panel

The 5306 VPX carrier front panel, illus–trated at the right, accepts the front panel of the 71620 XMC module installed on the carrier. See Section 2.13, on page 33 for description of the 71620 XMC front panel.

For a standard Model 53620, the VPX car–rier front panel is 4HP width (0.8"). For a Model 53620 with Option 741, the VPX carrier front panel is 5HP width (1").

The carrier front panel includes two LEDs labeled **Pwr** and **Tmp**, a recessed reset button (reserved for Pentek factory use), and a 5–pin Micro–USB receptacle. The following subsections describe these indi–cators and connectors.

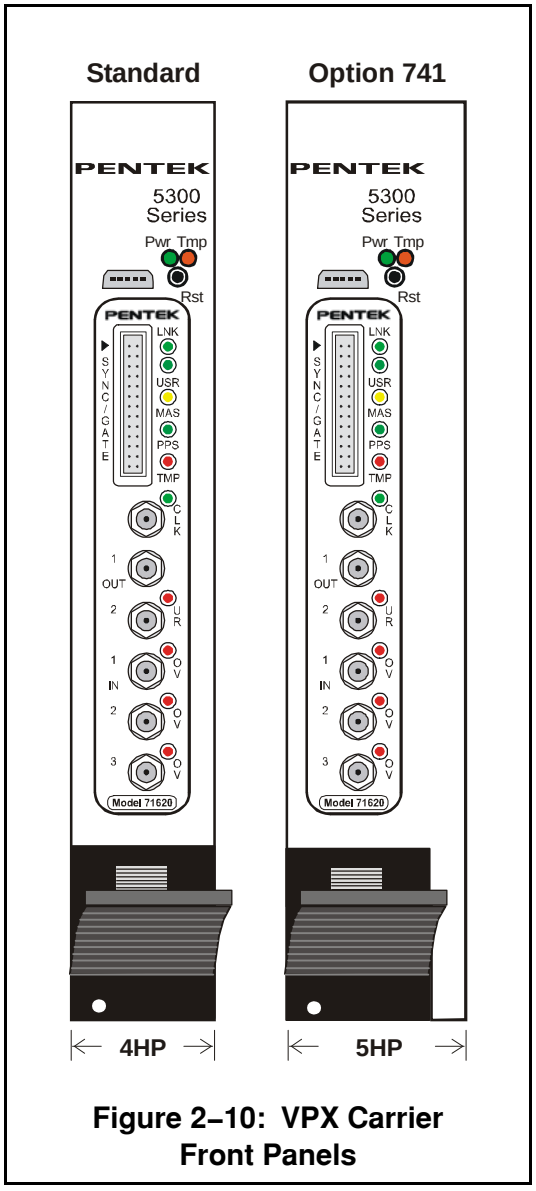


Figure 2–10: VPX Carrier Front Panels

2.12.1 Power LED

The green LED labeled **Pwr**, located at the top of the front panel, illuminates when power is applied to the 5306 carrier. This illuminates the same as LED **D73** on the PCB, described in Section 2.9.1.

2.12.2 Temperature LED

The red LED labeled **Tmp**, located to the right of the **Pwr** LED, illuminates when any of the 5306 carrier temperature sensors indicates an overtem–perature condition, or a Crosspoint Switch alarm. This illuminates opposite to LED **D44**, Section 2.9.3 – that is, when one indicates temperature, the other indicates Crosspoint Switch alarm.

2.12.3 Micro–USB Connector

The front panel includes one 5–pin Micro–USB receptacle (female) for con–figuration programming. This connector is reserved for Pentek factory use; contact Pentek for further information.

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2.12 VPX Carrier Front Panel (continued)

2.12.4 Conduction–cooled Carrier Options

When the Model 53620 is ordered for mounting in a conduction–cooled VPX chassis, the front panel is changed. Two different Options are available for conduction–cooled operation.

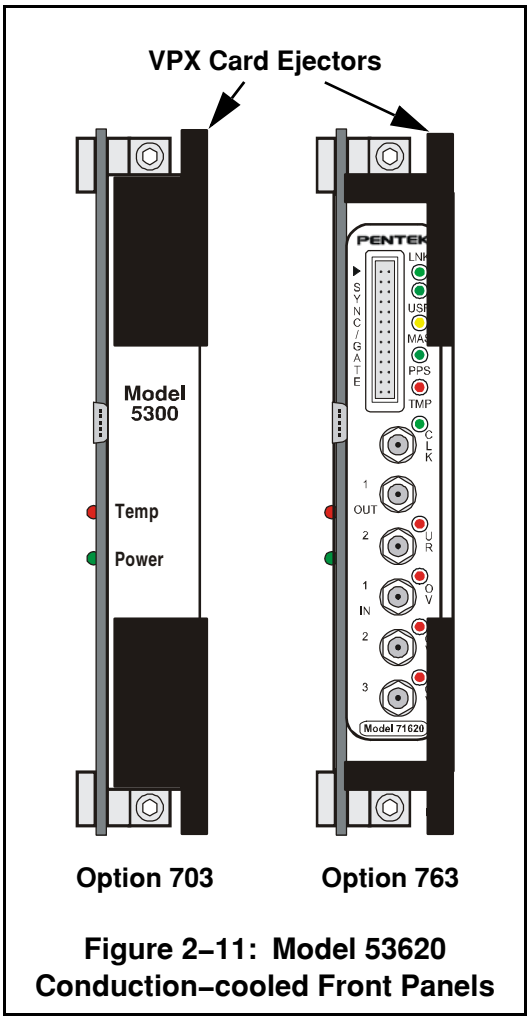


Figure 2–11: Model 53620 Conduction–cooled Front Panels

- ❑ Option 703

  With Model 53620 Option 703, the front panel of the 71620 module is not available, as shown at the left side of the figure at the right.

NOTE: Special connection hardware is available for the coaxial connectors on the 71620 front panel. Call Pentek for further information.

- ❑ Option 763

  With Model 53620 Option 763, the front panel of the 71620 module is accessible, as shown at the right side of the figure at the right. The VPX card ejectors cover only a small portion of the 71620 panel LEDs, and all 71620 panel connectors are available.

Note that with either of these options, two LEDs labeled **Power** and **Temp**, and the 5–pin Micro–USB receptacle are accessible on the 5306 carrier PCB to the left of the panel. These are the same as the **Pwr** and **Tmp** LEDs and USB connector described on the prior page for the standard 5306 carrier front panel.

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2.13 XMC Panel Connections

The 71620 XMC front panel, illustrated at the right, fits into the slot opening on the VPX carrier (Section 2.12).

The front panel includes six SSMC coaxial connectors for input/output of clock and analog signals, and a 26–pin Sync Bus input/output connector. These connectors are described in the following subsections.

The front panel also includes ten LED indicators. These are described in Section 2.14, on page 36.

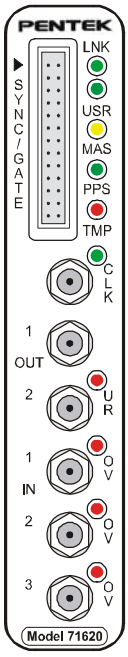


Figure 2–12: Model 71620 Front Panel

2.13.1 Clock Input Connector CLK

The front panel has one SSMC coaxial connector, labeled **CLK**, for input of an external sample clock. The external clock signal must be a sine wave or square wave of +0 dBm to +10 dBm, with a frequency range from 10 to 800 MHz.

The external clock input can be used as the sample clock for the A/D and D/A converters. This input is enabled using the Sync Bus Control Register 1 (see Model 71620 Operating Manual). The selected clock source is input to a CDC7005 Clock Synthesizer that generates separate output clocks, each programmable as sub–multiples of the input frequency. One CDC7005 clock (Y0) provides ADC timing, one clock (Y1) provides DAC timing.

CAUTION

Take care that the ADC clock never exceeds the ADS5485 rated clock speed during any change of frequency with the input clock signal.

– If you are increasing the external input frequency, first reprogram the appropriate CDC7005 divider so that the ADS5485 clock does not exceed 200 MHz.

– If you are decreasing the input frequency, do not reprogram the CDC7005 divider until the input has been reprogrammed so that the ADS5485 clock does not exceed 200 MHz.

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2.13 XMC Panel Connections (continued)

2.13.2 Analog Output Connectors **OUT 1, 2**

The front panel has two SSMC coaxial connectors for analog signal outputs, labeled **OUT 1** and **2**, one for each DAC5688 output.

The analog output signal is within the range of +4 dBm. This output is driven by an RF transformer into 50Ω output impedance.

2.13.3 Analog Input Connectors **IN 1, 2, 3**

The front panel has three SSMC coaxial connectors for analog signal inputs, labeled **IN 1, 2**, and **3**, one for each ADC input channel.

The analog input signal has a full−scale level of +8 dBm. Each input drives an RF transformer, with 50Ω input impedance.

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2.13 XMC Panel Connections (continued)

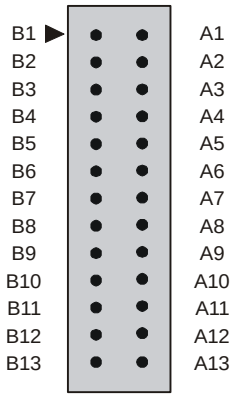
2.13.4 Sync Bus Connector SYNC/GATE

The 26–pin Sync Bus front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the Low–Voltage Positive Emitter–Coupled Logic (LVPECL) Sync Bus. When the 71620 is a bus Master, these pins output LVPECL Sync Bus signals to other slave units. When the 71620 is a bus Slave, these pins input LVPECL signals from a bus Master. This connector also provides two Low–Voltage TTL (LVTTL) Gate/Sync inputs.

The following table shows the **SYNC/GATE** connector pin configuration. The mating 26–pin connector is Pentek part # 353.02607 (ERNI # 214346).

Table 2–13: SYNC/GATE Connector Pins

Signal	Pin		Pin	Signal
LVTTL GATE/TRIG	B1		A1	GND
LVTTL SYNC/PPS	B2		A2	GND
LVPECL GATE A–	B3		A3	LVPECL GATE A+
GND	B4		A4	GND
LVPECL SYNC A–	B5		A5	LVPECL SYNC A+
GND	B6		A6	GND
LVPECL CLK A–	B7		A7	LVPECL CLK A+
GND	B8		A8	GND
LVPECL GATE B–	B9		A9	LVPECL GATE B+
GND	B10		A10	GND
LVPECL SYNC B–	B11		A11	LVPECL SYNC B+
GND	B12		A12	GND
LVPECL CLK B–	B13		A13	LVPECL CLK B+





When connecting LVPECL Sync Bus pins to additional Model 71620 modules, the LVPECL pins on the LAST unit must be terminated. Pentek includes a terminating board, part # 004.71504, with your shipment for this purpose.



The LVTTL GATE/TRIG and SYNC/PPS signals are 5V tolerant but they must NOT have any negative voltage applied. They are terminated with a 392–Ohm resistor to 3.3V and a 392–Ohm resistor to ground.

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2.14 XMC Panel LEDs

The 71620 XMC front panel has ten LED indicators, as illustrated in Figure 2–12.

2.14.1 Link LED LNK

The green **LNK** LED illuminates when a valid link has been established over the PCIe interface.

2.14.2 User LED USR

The green **USR** LED is for user applications. Refer to the LED Control Register, Model 71620 Operating Manual, for control of this LED.

2.14.3 Master LED MAS

The yellow **MAS** LED illuminates when this Model 71620 is set as the sync bus Master (see Sync Bus Control Register 1, Model 71620 Operating Manual). When only a single 71620 is used, it must be a Master.

2.14.4 PPS LED PPS

The green **PPS** LED illuminates when a valid PPS signal is detected and will blink at the rate of the PPS signal.

2.14.5 Over Temperature LED TMP

The red **TMP** LED illuminates when an over–temperature or over–voltage condition is indicated by any of the temperature/voltage sensors on the Model 71620 PCB.

2.14.6 Clock LED CLK

The green **CLK** LED illuminates when a valid sample clock is detected. For reference clock mode, this LED indicates lock to the reference clock.

2.14.7 DAC Underrun LED UR

The red **UR** underrun LED illuminates when the DAC FIFO is out of data (underrun).

2.14.8 ADC Overload LEDs OV

There are three red **OV** overload LEDs, one for each A/D input. Use the ADC Data Control Register, Model 71620 Operating Manual, to select the signal source for each LED, either an overload in the associated ADS5485, or an ADC FIFO overrun.

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