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OPERATING MANUAL

MODEL 6102

8 Channel, 250 kHz, 16 bit,
'C40 Comm Port Compatible,
A/D - D/A Converter,
VMEbus Board / MIX Module

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Pentek Model 6102 Operating Manual - Revision History

Date	Rev	Applicable Serial #'s	Comments
06/11/96	Preliminary	9615001 - Forward	Pre-release version
06/14/96	Preliminary	9615001 - Forward	Initial product release - MIX support added to Sample Code in Appendix A - revised Sec. A.4 and added Sec. A.5.
08/19/96	Preliminary	9615001 - Forward	DAC Output Voltage Spec is ± 2.5V into 50Ω, (± 5.0 V into Hi-Z) - this changes Specs in Sec. 1.6 and Sec. 2.4.2.1 (Analog Outputs).
03/10/97	A	9710001 - Forward	A/D converters changed from AD7882 to ADS7811. Sample rate for both A/D and D/A increased to 250 kHz. Other associated changes in A/D performance specs. DAC output spec changed to ± 2.5V into 1 kΩ (± 5.0 V into Hi-Z). Mention Opt. 007 (± 10.0 V into Hi-Z). Add Sec. 2.4.4, re:Front Panels for Options 001 & 004. Add memory map for use w/4285 MIX Baseboard Adapter (Sec. 3.3.5). MIX Appendices redesignated as X, Y & Z (as opposed to B, C & D).
04/10/97	A.1	9710001 - Forward	When one channel in a pair is configured for Single Comm Port, the other can transact with MIX/VME - this changes NOTEs in Secs. 3.4.11.and 3.4.20. Calibration was removed when the A/Ds were changed - this changes the names of the two registers that affected calibration, removes Sec. 3.4.11.2, consolidates section 3.4.11.1 into 3.4.11, and changes Tables 3-22 and 3-25 and Sec. 3.4.12.2.
11/21/97	B	9710001 - Forward	D/A Trigger Control Register entries had been omitted from Table of Contents - replace them. Additional Specs added to Sec. 1.6 re: the A/D (taken from published ADS7811 Data). 2's Complement data representation examples also added to Specs. Sec. 2.4.3 - 6102 Comm Ports will force token and turn around "real" 'C40 Comm Ports - this is mentioned in the body text, but the Caution ststement is still kept. Register Descriptions broken out into three sections - one covers bus interactions, the 2nd covers the A/D registers and the 3rd the D/A registers. Corrections to Table 3-17 & Table 3-29 re: Trigger Type Bits - 0 = Edge Trigger, 1 = Level Trigger. Other references to these bits were already correct. Clock.Reference input signal must not be in low state for any more than 2.5 µs - add this to Sec. 2.4.1.2, & Sec. 3.5.8.2. Sample Ctr. Pre-Load fields cannot be programmed to acquire only a single sample - add this info to Sec. 3.5.8.3 & Sec. 3.6.7.2, and give work-around. Table 3-44 & Table 3-49 added to Sec. 3.7 & Sec. 3.8 (Reading & Writing data) giving examples of 2's complement format.
09/10/98	B.1	9710001 - Forward	Add Zin spec for Option 009. Add notes in Table 2-1 and Sec. 2.4.1.1 describing Option 009. Add notes in Sec. 3.5.8.2 and Sec. 3.6.7 indicating that external clock reference is selected at power-up. Change headings in Table 3-49 from "Input" to"Output". Add Appendix B (Errata). Change references to Appendices X, Y and Z to refer to the MIX Tutorial Manual (Pentek part # 800.00001).
09/28/98	B.2	9710001 - Forward	Corrected frequency at which external clock signal's duty cycle must be adjusted to meet the 2.5 μs maximum low-state limit - 200 kHz, not 400 kHz. This affects Sec. 2.4.1.2 & Sec. 3.5.8.2.

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Chapter 1: Overview

1.1 General Description

The Pentek Model 6102 is a high-performance, 8-channel, A/D - D/A converter for VMEbus data acquisition, control, and DSP applications. It offers differential inputs to the A/D section, and each of the A/D and D/A converters features 16-bit resolution and Sampling Frequencies up to 250 kHz.

The Model 6102 features a full VMEbus slave interface. It is also a full-depth MIX module, which means that it can interface directly with a DSP processor using the Intel MIX mezzanine bus. This 32-bit bus allows up to three MIX modules to be attached to a MIX baseboard such as the Pentek 428x series of DSP MIX Baseboards, or to the 4200 series of VME/MIX Baseboards.

The standard Model 6102 stores digitized data for each channel of both the A/D and D/A sections in independent, 1 ksample FIFO buffers. In units equipped with Option 002, FIFO depth for the D/A section is 16 ksamples. In units equipped with Option 003, FIFO depth for the A/D section is 16 ksamples. We can also configure the device as a D/A-only board (Option 001) or as an A/D-only board (Option 004). (Note that the Option 004 configuration **does NOT include** the MIX interface.)

The Model 6102 is ideal for real-time process control applications in which latency and loop delay must be minimized. As each sample is converted, it is immediately available to the interface because of the near-zero fall-through time of the FIFOs. Thus, the processor can address each channel directly, one sample at a time.

1.2 Three I/O Interfaces

Digital I/O data can come from, or be sent to, the VMEbus, the MIX bus, or the front panel TMS320C4x-compatible Comm Ports. Each of the eight Comm Ports supports a pair of converters. Four Comm Ports carry data from the A/D converters, and the other four deliver data to the D/As.

Both the VMEbus and the MIX bus interfaces feature full memory-mapped slave access to all data FIFOs, interrupt controls, Sample Rate Generators and control registers. All input and output FIFOs can be configured, under software control, to interrupt the MIX bus or the VMEbus on full, half-full, or empty conditions.

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1.3 Versatile Sample Clock Generation

The four internal Sample Rate Generators can supply independent Sampling Clocks for each of the A/D and D/A converters. The Rate Generators can be referenced to an external, TTL-level signal from the front panel connector, or to an internal, 20 MHz crystal oscillator. The external signal can also be delivered by a differential, open-collector driver. The on-card oscillator is socketed, allowing you to select a custom reference frequency for your own applications.

Each of the eight Sample Clock Generators includes an independent, 16-bit, programmable frequency divider. This configuration supports up to four different Sampling Rates for the four pairs of A/D converters, and up to four different rates for the four pairs of D/A converters. Each channel pair may be programmed for Sampling Rates up to 250 kHz.

1.4 Triggering

Independent, front panel, TTL-level Trigger inputs for the A/D and D/A sections allow data collection or generation to be initiated by positive- or negative-edge transitions, or to be gated by logic levels. The Triggering signal may also be delivered by a differential, open-collector driver. Triggering by software command is also supported.

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1.5 Block Diagram

Figure 1-1, below, shows the block diagram for the Pentek Model 6102, 8 Channel, 250-kHz, 16-bit, 'C40 Comm Port-compatible, A/D - D/A Converter, VMEbus board/MIX Module.

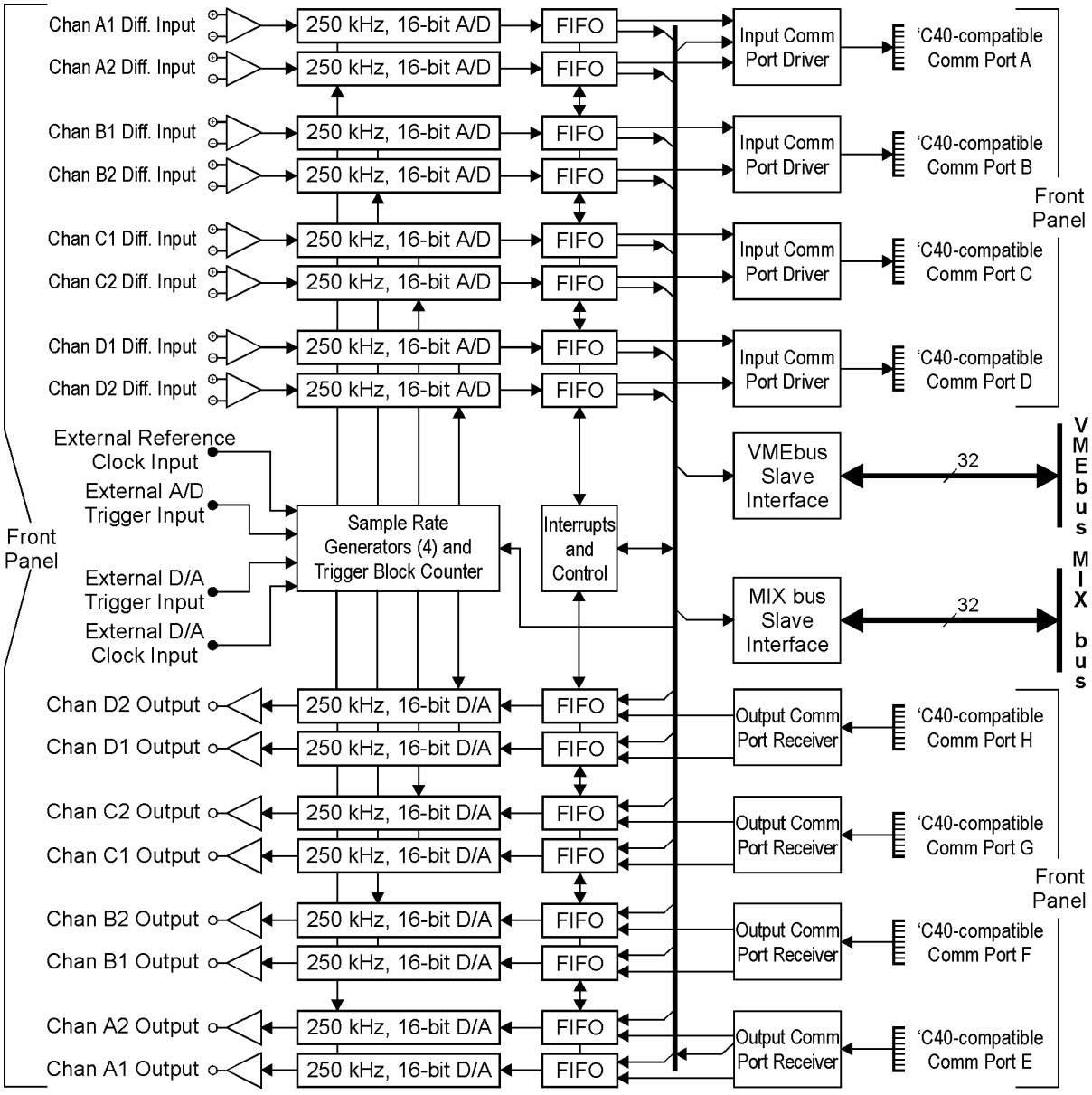


Figure 1-1: Model 6102 Block Diagram

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1.6 Specifications

Input Channels

Quantity:	8
Channel Enables:	Any channel can be enabled or disabled
Input Type:	
Standard:	Differential, +/– inputs
Option 009:	Single-Ended
Input Impedance:	
Standard:	
Each Input to Ground:	100 kΩ
Each Input to its Complement:	Customizable (contact factory)
Option 009:	1 MΩ
Full Scale Voltage:	± 5.0 Volts (differential) (Neither input should exceed ±10.0 Volts with respect to ground for linear operation.)
Common Mode Rejection:	>60 dB @ 60 Hz

A/D Converters

Quantity:	8
Type:	Burr-Brown ADS7815
Sampling Rate:	DC to 250 kHz
Resolution:	16 bits
Total Harmonic Distortion:	90 dB below full scale, minimum
Intermodulation Distortion:	85 dB below full scale, minimum
Spur-Free Dynamic Range:	>84 dB
Signal to Noise Ratio:	>75 dB @ f_{sample} = 250 kHz

Input FIFO Buffers

Quantity:	8 (one per A/D channel)
Size (samples):	
Standard:	1024
Option 001:	16,384

Output Channels

Quantity:	8
Channel Enables:	Any channel can be enabled or disabled
Output Type:	Single-Ended
Output Impedance:	50Ω
Full Scale Voltage:	± 2.5 Volts into 1 kΩ load ± 5.0 Volts into high impedance

D/A Converters

Quantity:	8
Type:	Analog Devices AD569
Sampling Rate:	DC to 250 kHz
Resolution:	16 bits
Total Harmonic Distortion:	-55 dB @ 2 kHz, 10 V_{p-p} amplitude -40 dB @ 20 kHz, 10 V_{p-p} amplitude
Glitch Energy:	120nV/sec, typ. (500nV/sec., max)

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1.6 Specifications (continued)

Output FIFO Buffers

Quantity:	8 (one per A/D channel)
Size (samples):	
Standard:	1024
Option 001:	16,384

Sampling Rate Control

Sample Clock Reference:	
Internal:	20 MHz (±100 ppm)
External:	Front panel, optically isolated TTL input, 15 MHz max.
Sample Clock Frequency Dividers:	
Quantity:	4 (one for each A/D pair, not dedicated)
Programming:	Each divides internal or external reference by N, where N = 1 to 65,536
External D/A Clock Input:	Front panel, optically isolated TTL input, 250 kHz max.

Trigger / Gate Control

Trigger/Gate Input:	Front panel, optically isolated TTL-compatible input, VMEbus or MIX bus accessible control bit.
Trigger Mode:	Positive or negative edge (programmable) starts conversion.
Gate Mode:	Logic '0' or '1' (programmable) starts conversion, other state stops conversion.
Sample Counter:	Sample counter generates an interrupt to VMEbus or MIX bus after acquisition of every Nth sample (N = 2 to 256).

Comm Port Interface

Quantity:	8 (4 dedicated input ports, each supporting one pair of D/A converters, 4 dedicated ouptut ports, each supporting one pair of A/D converters).
Compatiblity:	Texas Instruments TMS320C40 communication ports
Connector:	16-pin, pin compatible with most Pentek 'C40 products, (for use with Pentek Model 4285 Comm Port, adaptor cable [Pentek #2115] is required) - standard 3M connector (3M #50166-B000).
Data & Control Lines:	8 data + 4 control lines
Transfer Format:	Data is always sent as four 8-bit bytes, forming a 32-bit 'C40 longword, @ 15 MB/sec, max.
Standard (Dual) Port Mode	
Transfers:	Each Comm Port handles data for 1 or 2 A/D or D/A channels in Packed or Non-Packed mode.
Non-Packed:	One 16-bit sample left justified in 32-bit longword; only one channel enabled per pair.
Packed:	Two 16-bit samples in 32-bit longword.

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1.6 Specifications (continued)

Comm Port Interface (continued)

Combined Port Mode

Transfers:	One Input Comm Port handles data for up to 8 A/D channels. One Output Comm Port handles data for up to 8 D/A channels. Both ports deliver data in Non-Packed mode (One 16-bit sample, left justified in 32-bit longword). Three LSBs indicate Channel ID.
Data Representation:	Two's Complement
Coding:	16 bits, left justified in 32-bit field
+ Full Scale:	0x7FFF 0000
Zero:	0x0000 0000
- Full Scale	0x8000 0000

VMEbus Interface

Type:	Slave, A32 / D32 / I1-7
Transfers:	BLT (block level transfers), 16k range per FIFO
Control Registers:	Sampling Clock divisors, Trigger/Gate control, Interrupt Mask, channel enables, Clock source, Comm Port modes, FIFO resets, A24/A32 base address, Interrupt Vector register.
Status Registers:	Interrupt status, FIFO flags, Trigger status
Memory Map:	All FIFOs, control registers, and status registers are mapped into A16 space. FIFOs also mapped into A24/A32 space.
Maskable Interrupts:	FIFO status (full, half-full, or not-empty conditions), Trigger status and Sample Counter.

$\overline{DS}$ - $\overline{DTACK}$ Delays

Assertion:	240 nsec
Deassertion:	90 nsec

MIX Bus Interface

Type:	Slave , 32-bit
Control Registers	Sampling Clock divisors, Trigger/Gate control, Interrupt Mask, channel enables, Clock source, Comm Port modes, FIFO resets, MIX interface control.
Status Registers:	Interrupt status, FIFO flags, Trigger status
Memory Map:	All FIFOs, control registers, and status registers
Maskable Interrupts:	FIFO status (full, half-full, or not-empty conditions), Trigger status and Sample Counter.

Power

+ 5 V_{DC}	2.6 A max.
+12 V_{DC}	450 mA max.
– 12 V_{DC}	450 mA max.

Dimensions 6U VME board, single slot

	Inches	mm
Height:	9.2	233.5
Depth:	6.3	160.0
Panel Width:	0.8	20.3

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If you discover any damage, contact Pentek immediately at the phone number shown on the title page of this manual. Please save the original shipping container and packing material in case return shipment is required.

The Model 6102 contains two printed-circuit (PC) assemblies. The board with the VMEbus P1 and P2 connectors (Pentek part # 004.61023) contains the VME interface to both assemblies and the A/D converters. The other board (Pentek part # 004.61021), which has the MIX connector pattern, contains the MIX interface for both assemblies and the D/A converters. Drawings of the component sides of both PC assemblies are shown in Figure 2-2, on page 16 and Figure 2-3, on page 17.

2.2 VMEbus A16 Base Address Switches

Three separate address spaces are defined for the VMEbus environment: A16, A24, and A32. Each device in your VMEbus card cage must have a unique address in any address space in which it is to be accessible. On the Model 6102, two rotary switches set the A16_base address (i. e., the lowest address it occupies in the A16 region). These switches, SW1 and SW2, are located at the top rear of the VME board, with SW1 adjacent to the VME P1 connector, and SW2 directly to the left of SW1. Figure 2-1, below, shows the switches set for the A16_base address of 0xC800. Figure 2-2, on page 16, is a drawing of the Model 6102 VME board, showing the location of these switches.



Figure 2-1: Model 6102 - Rotary Switches

Each position on these 16-position rotary switches denotes a hex digit (0 - F) that defines four bits of the 6102's A16_base address. SW2 defines the four most significant bits (MSBs) of the address (A15 - A12) and SW1 defines the next four address bits (A11 - A8). Thus, with 16 settings available on each of two switches, you can select one of 256 different addresses for any 6102.

Throughout this manual, all VMEbus addresses are given as offsets from the assigned base address. For example, the A24 and A32 base addresses for the 6102 are defined by writing to a register at address A16_base+0x24.

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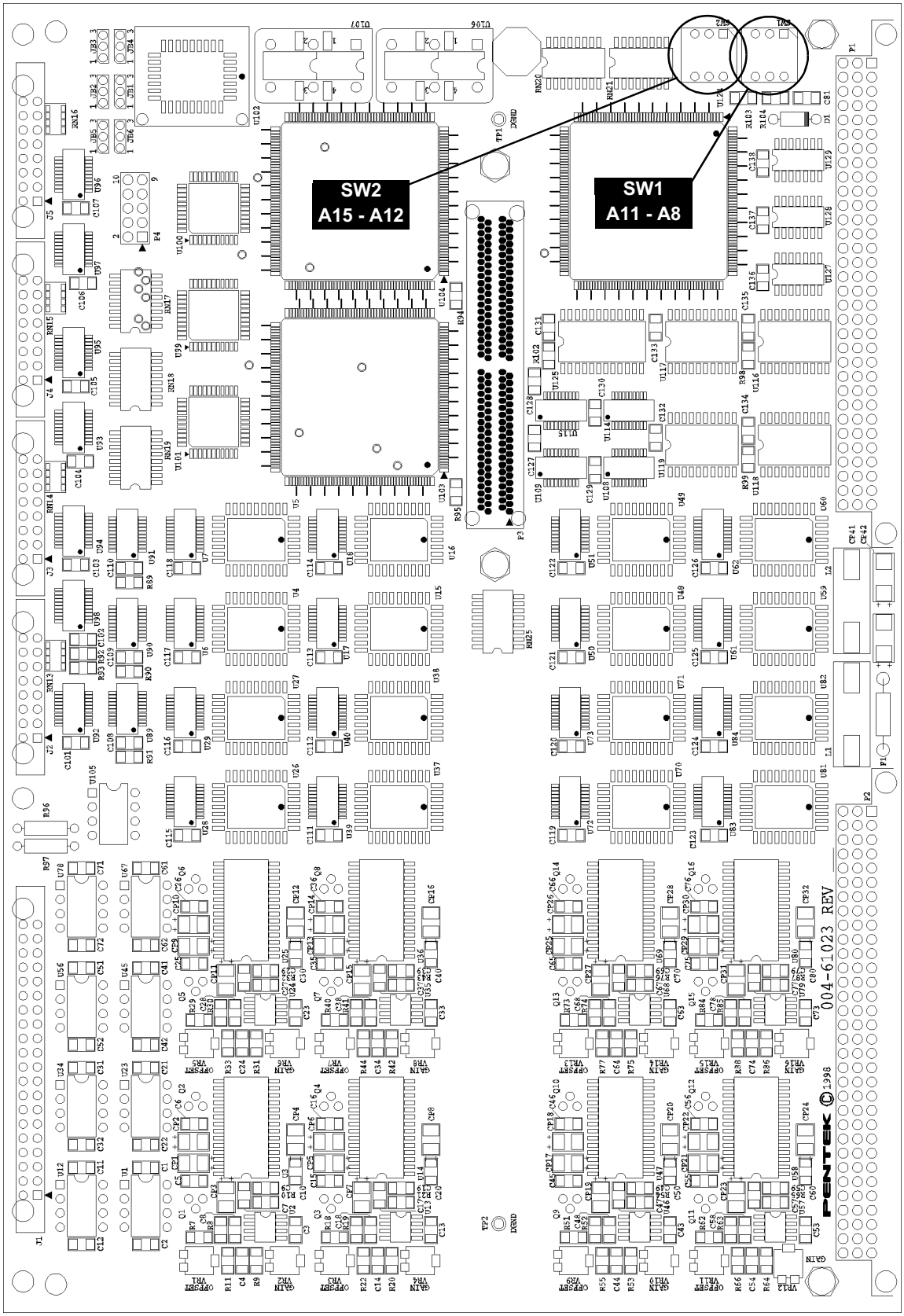


Figure 2-2: Model 6102 VME Board - Rotary Switch Locations

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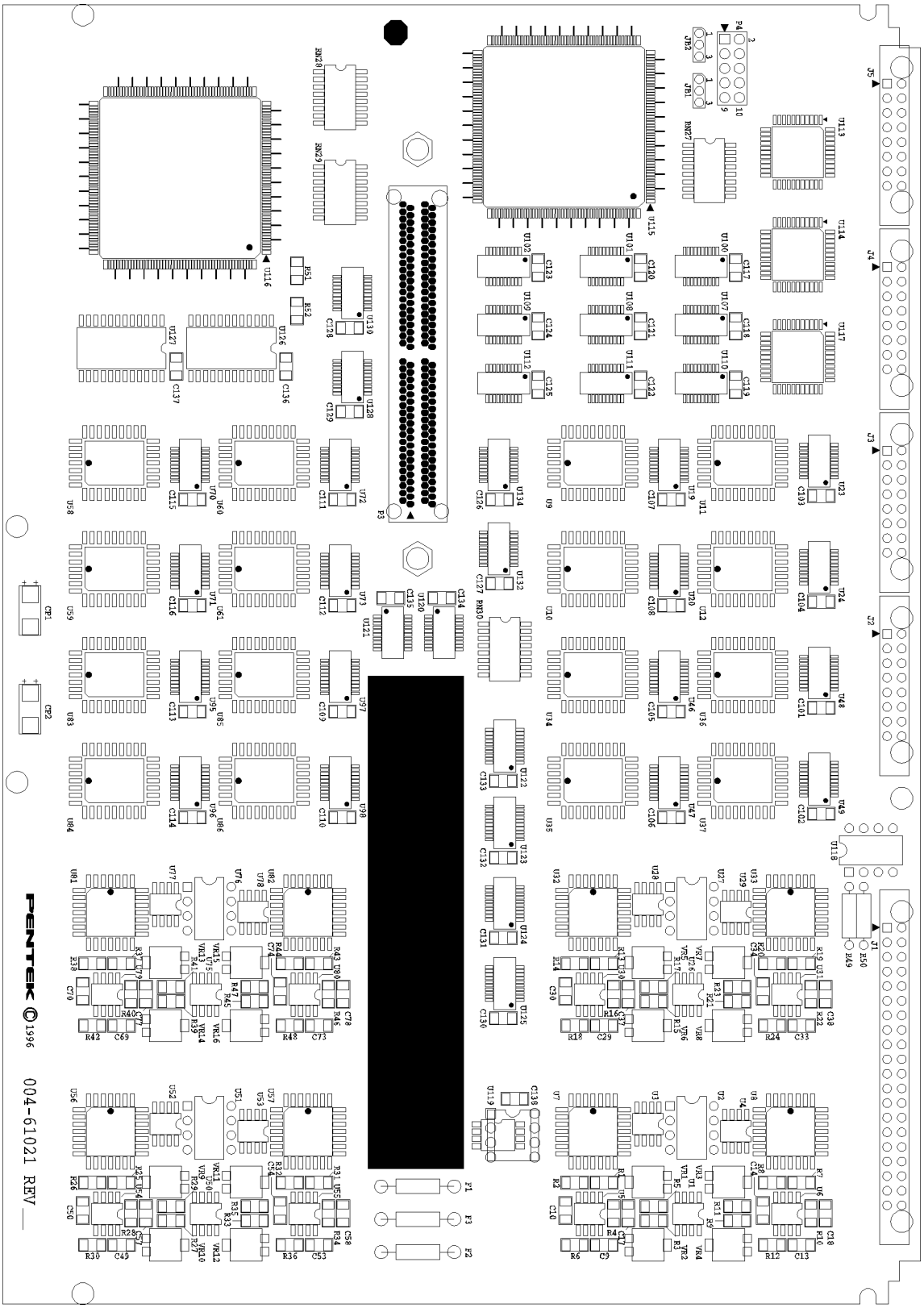


Figure 2-3: Model 6102 MIX Board

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2.3 Jumper Settings

Although there are a few jumper blocks on the Model 6106 PC board, all of them are set at the factory during assembly, test, and calibration.

CAUTION!!
Do not change any of the jumper settings on this device.

2.4 Model 6102 Front Panel

Figure 2-4, right, shows the Model 6102 front panel. It contains eight connectors for the TMS320C40-compatible Comm Ports. Four of these port connectors (those labeled COMM A, COMM B, COMM C and COMM D) are hardwired to deliver data collected by the 6102's A/D converters to a 'C40 processor (or a compatible input port). We refer to these as the Input Comm Ports because they carry data from the 6102's Analog Input stage. The other four port connectors (those labeled COMM E, COMM F, COMM G, and COMM H) are hardwired to accept data from a 'C40 processor (or a compatible output port), and pass this data to the 6102's D/A converters. Because these ports drive the 6102's Analog Output section, we call them the Output Ccomm Ports.

The Model 6102's front panel also contains two connectors for Analog I/O signals. The connector at the lower left of the panel is for the Analog signal Inputs, the External Reference Clock and the Trigger Input for the A/D section. The one at the lower right is for the Analog signal Outputs and the External Clock and Trigger Inputs for the D/A section. All of the connectors mentioned above, and the signals they carry, are described in the subsections below.

NOTE: When connecting ribbon cable connectors to the Model 6102, be aware that pin 1 for all front panel connectors is toward the **CENTER** of the panel.

2.4.1 Analog Input Connector

A non-shrouded, 40-pin male header (two rows of 20 pins each), located at the bottom left of the Model 6102's front panel provides connections for the eight differential Analog Input signals to the A/D converters. This connector also contains pins for the External Clock Reference and A/D Trigger Input signals, and a Clock Output signal.

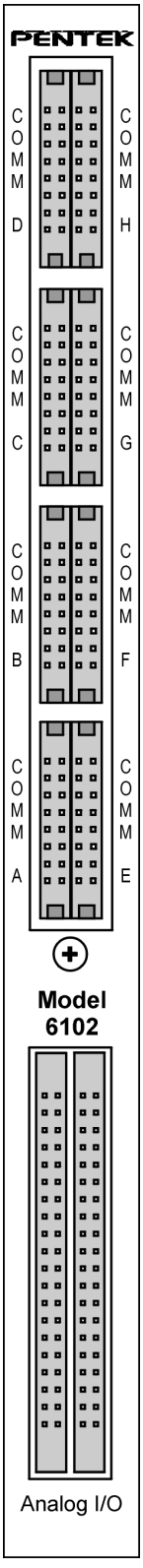


Figure 2-4: Model 6102 Front Panel

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2.4 Model 6102 Front Panel (continued)

2.4.1 Analog Input Connector (continued)

The mating connector is a 40-pin, dual-inline ribbon cable type socket connector on a 0.1 x 0.075 grid. An example of this type of connector is 3M's part number 50140-B000 (Pentek's part # is 353.04009), and the optional strain relief is 3M #3448-50140 (Pentek part # 353.04010). The cable used with this type of connector is an .050-pitch flat ribbon cable, such as 3M #3365/40 (Pentek part # 378.64000).

Characteristics of the signals applied to the inputs, and available at the output, of this connector are discussed in subsections beginning on the next page. Table 2-1 (below right) gives the pinout of the Analog Input connector. Figure 2-5 (below left) shows the pin numbering schemes for this connector and for the adjacent analog output connector (discussed in Section 2.4.2).

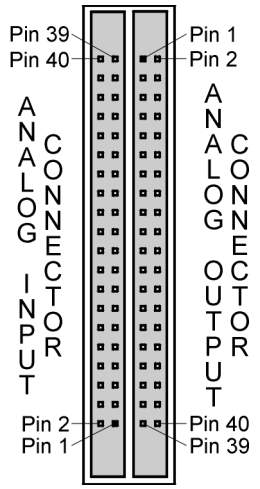


Figure 2-5: Model 6102 Analog I/O Connectors Pin Numbering

Table 2-1: Model 6102 Analog Input Connector - Pin Assignments

Differential Analog Input Signals					
Pin #	**Channel**	**Signal**	**Pin #**	**Channel**	**Signal**
1	A1	+In	2	A1	-In
3	A1	Sig. Gnd.	4	A1	Sig. Gnd.
5	A2	+In	6	A2	-In
7	A2	Sig. Gnd.	8	A2	Sig. Gnd.
9	B1	+In	10	B1	-In
11	B1	Sig. Gnd.	12	B1	Sig. Gnd.
13	B2	+In	14	B2	-In
15	B2	Sig. Gnd.	16	B2	Sig. Gnd.
17	C1	+In	18	C1	-In
19	C1	Sig. Gnd.	20	C1	Sig. Gnd.
21	C2	+In	22	C2	-In
23	C2	Sig. Gnd.	24	C2	Sig. Gnd.
25	D1	+In	26	D1	-In
27	D1	Sig. Gnd.	28	D1	Sig. Gnd.
29	D2	+In	30	D2	-In
31	D2	Sig. Gnd.	32	D2	Sig. Gnd.

Clock and Trigger Signals			
Pin #	**Signal**	**Pin #**	**Signal**
33	Ground	34	Ground
35	Clock1 Out	36	Ground
37	Clk. Ref. In Source (+)	38	Clk. Ref. In Sink (-)
39	A/D Trig. In Source (+)	40	A/D Trig. In Sink (-)

NOTE: For Option 009, the pins designated as "-In" in this table are all connected to signal ground

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2.4 Model 6102 Front Panel (continued)

2.4.1 Analog Input Connector (continued)

2.4.1.1 Analog Input Signals

The eight differential Analog Input channels of the Model 6102 are called Channels A1, A2, B1, B2, C1, C2, D1 and D2. The input connector contains four pins associated with each of the eight channels. These pins are a positive input (+In), a negative input (–In), and two signal grounds (Sig. Gnd.).

Figure 2-6, below, shows the differential input network used in the Model 6102. Each of the differential input pins for a given channel sees an impedance of approximately 100 kΩ to signal ground. (The signal ground for each channel is connected to the card cage ground (i. e., power and digital ground) at a single point near the A/D converter in each input circuit.) Provisions have been made for the installation of a differential termination, but no resistor is normally installed in this location. If a differential termination is needed, the impedance may be specified when new units are ordered.

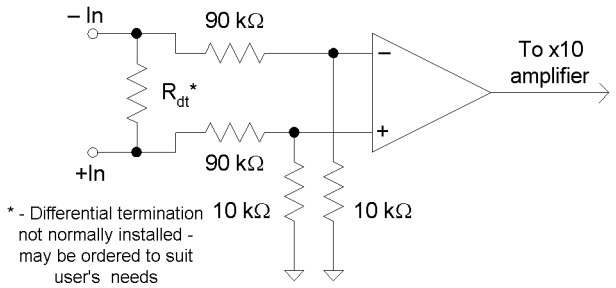


Figure 2-6: Model 6102: Analog Input Circuit

Each input line has a x10 attenuator (the 90 kΩ and 10 kΩ resistors). The gain of the next amplifier stage (not shown) compensates for the attenuation, so the signal path to the A/D converter provides unity gain. The design of this stage takes advantage of the small-signal bandwidth properties of the differential amplifier, and allows for a full-scale differential input voltage of ± 5 V. To maintain linear operation, the maximum input voltage at each differential input with respect to signal ground is ± 10.0 V_{DC}.

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2.4 Model 6102 Front Panel (continued)

2.4.1 Analog Input Connector (continued)

2.4.1.1 Analog Input Signals (continued)

NOTES: (1) For units equipped with Option 007 (± 10 V full scale inputs), all voltages listed at the bottom of the previous page and in the examples below are doubled.

(2) For units equipped with Option 009 (Single-ended, 1 MΩ input impedance), the -inputs are connected to signal ground, the 90 kΩ series resistor on the +input is replaced with 0Ω, and the 10 kΩ resistor to ground is replaced with 1 MΩ.

For example, each of the following differential input combinations will produce a full-scale positive data output from the ADC:

	+ input	– input	comment
a)	+ 10.0 V	+ 5.00 V	+ in @ max. pos.
b)	+ 7.50 V	+ 2.50 V	
c)	+ 5.00 V	0.00 V	
d)	+ 2.50 V	– 2.50 V	
e)	0.00 V	– 5.00 V	
f)	– 2.50 V	– 7.50 V	
g)	– 5.00 V	– 10.0 V	– in @ max. neg.

Similarly, each of the following differential input combinations will produce a full-scale negative data output from the ADC:

	+ input	- input	comment
a)	+ 5.00 V	+ 10.0 V	– in @ max. pos.
b)	+ 2.50 V	+ 7.50 V	
c)	0.00 V	+ 5.00 V	
d)	– 2.50 V	+ 2.50 V	
e)	– 5.00 V	0.00 V	
f)	– 7.50 V	– 2.50 V	
g)	– 10.0 V	– 5.00 V	+ in @ max. neg.

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2.4 Model 6102 Front Panel (continued)

2.4.1 Analog Input Connector (continued)

2.4.1.2 Clock Reference and A/D Trigger Inputs

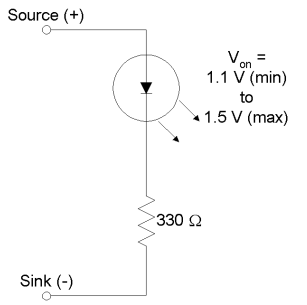


Figure 2-7: Model 6102 - External Reference Clock and Trigger Input Circuits

The Clock Reference and A/D Trigger inputs on the Model 6102 are optically coupled. The pins labeled Source (+) in Table 2-1 drive the anodes of LEDs contained within an opto-coupler IC. The pins labeled Sink (–) are resistive connections to the cathodes. The equivalent input circuit is shown in Figure 2-7, left.

These input circuits can accept standard TTL-level signals (logic '0' < + 0.8 V_{DC}, logic '1' > + 2.0 V_{DC}) at the Source (+) pins. When driven in this manner, **the Sink (–) pins must be grounded**, preferably at the driver's end of the cable that carries the signal. They may also be driven by open-collector, differential drivers. In this case, the non-inverted signal is connected to the Source (+) input, and the inverted signal is connected to the Sink (–) input. Figure 2-7 provides the information needed to calculate the current required to switch the diode.

You can program the 6102 such that the Clock Reference input signal on the Analog Input connector drives the Sample Rate Dividers for all A/D and D/A converters (see Section 3.5.8.2 for programming details). The input's opto-coupler will not pass signal frequencies in excess of 15 MHz. Regardless of the frequency of this signal, however, it must not remain in the low state for more than 2.5 µs. For signal frequencies below 200 kHz, adjust the duty cycle to meet this requirement.

You can also program the 6102 such that the Trigger Input signal on the Analog Input connector initiates the Sampling process for the Model 6102's A/D converters **ONLY**. There is a separate Trigger input for the D/A converters on the Analog Output connector (see Section 2.4.2.2). Refer to Section Section 3.5.2 (A/D Trigger Control Register) for programming details.

2.4.1.3 Clock1 Output

The signal available on pin 35 of the Analog Input connector on the front panel of the Model 6102 is a TTL-level (logic '0' < + 0.8 V_{DC}, logic '1' $\geq$ + 2.0 V_{DC}) pulse train at the frequency of the Clock1 signal. The width of the active high pulse is equal to one cycle of the Clock Reference frequency (e. g., 50 nsec if the 20 MHz crystal oscillator is used as the Reference). For further information about programming the Clock1 divider, see Section 3.5.1 of this manual. This signal has adequate drive capacity to handle a load equivalent to two 74LS-type inputs.

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2.4 Model 6102 Front Panel (continued)

2.4.2 Analog Output Connector

A non-shrouded, 40-pin male header (two rows of 20 pins each), located at the bottom right of the Model 6102's front panel, provides connections for the eight analog output signals from the D/A converters. This connector also contains pins for the External Clock and Trigger Input signals to the D/A section, and pins for a Clock Output signal.

The same mating connector is used here as for the Analog Input connector. Please refer to Section 2.4.1, on page 19 for details about the mating connector.

Characteristics of the signals available at the outputs, and applied to the inputs, of this connector are discussed in subsections beginning at the bottom of this page. Table 2-2, below, gives the pinout of the Analog Output connector. Figure 2-5, on page 19 shows the pin numbering schemes for this connector and for the adjacent Analog Input connector (discussed in Section 2.4.1).

Table 2-2: Model 6102 Analog Output Connector - Pin Assignments

Clock and Trigger Signals			
Pin #	**Signal**	**Pin #**	**Signal**
1	D/A Trig. In Source (+)	2	D/A Trig. In Sink (-)
3	D/A Clk. In Source (+)	4	D/A Clk. In Sink (-)
5	Clock4 Out	6	Ground
7	Ground	8	Ground

Analog Output Signals					
Pin #	**Channel**	**Signal**	**Pin #**	**Channel**	**Signal**
9	D2	Sig. Gnd.	10	D2	Sig. Gnd.
11	D2	Out	12	D2	Sig. Gnd.
13	D1	Sig. Gnd.	14	D1	Sig. Gnd.
15	D1	Out	16	D1	Sig. Gnd.
17	C2	Sig. Gnd.	18	C2	Sig. Gnd.
19	C2	Out	20	C2	Sig. Gnd.
21	C1	Sig. Gnd.	22	C1	Sig. Gnd.
23	C1	Out	24	C1	Sig. Gnd.
25	B2	Sig. Gnd.	26	B2	Sig. Gnd.
27	B2	Out	28	B2	Sig. Gnd.
29	B1	Sig. Gnd.	30	B1	Sig. Gnd.
31	B1	Out	32	B1	Sig. Gnd.
33	A2	Sig. Gnd.	34	A2	Sig. Gnd.
35	A2	Out	36	A2	Sig. Gnd.
37	A1	Sig. Gnd.	38	A1	Sig. Gnd.
39	A1	Out	40	A1	Sig. Gnd.

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2.4 Model 6102 Front Panel (continued)

2.4.2 Analog Output Connector (continued)

2.4.2.1 Analog Outputs

The output voltage range of the D/A section of the Model 6102 is from – 2.5 V_{DC} to + 2.5 V_{DC} into a 1 kΩ load (– 5.0 V_{DC} to + 5.0 V_{DC} into a high impedance). The output voltage for any given channel at any given time is proportional to the data code written into that channel's D/A FIFO for that time period. Please refer to Section 3.8 for details about FIFO programming.

2.4.2.2 D/A Clock and Trigger Inputs

The D/A Clock and Trigger Inputs on the Model 6102 are optically coupled. The pins labeled Source (+) in Table 2-2 drive the anodes of LEDs contained within an opto-coupler IC. The pins labeled Sink (–) are resistive connections to the cathodes. The equivalent input circuit is shown in Figure 2-7, on page 22.

These input circuits can accept standard TTL-level signals (logic '0' $\leq$ + 0.8 V_{DC}, logic '1' $\geq$ + 2.0 V_{DC}) at the Source (+) pins. When driven in this manner, **the Sink (–) pins must be grounded**, preferably at the driver's end of the cable that carries the signal. They may also be driven by open collector, differential drivers. In this case, the non-inverted signal is connected to the Source (+) input, and the inverted signal is connected to the Sink (–) input. Figure 2-7 provides the information needed to calculate the current required to switch the diode.

The D/A Clock Input signal on the Analog Output connector may be used to Clock data into the D/A converters directly (see Section 3.6.7 for D/A Clock source selection details). This signal **CANNOT** be frequency divided. The frequency of the signal applied to this input should not exceed 250 kHz, and the duty cycle should remain between 40% and 60% (i. e., the signal should approximate a square wave).

The 6102 may be programmed to use D/A Trigger Input signal on the Analog Output connector to initiate the sampling process for the Model 6102's D/A converters **ONLY**. There is a separate trigger input for the A/D converters on the Analog Input connector (see Section 2.4.1.2). Refer to Section 3.6.1 for programming details.

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2.4 Model 6102 Front Panel (continued)

2.4.2 Analog Output Connector (continued)

2.4.2.3 Clock4 Output

The signal available on pin 5 of the Analog Output connector on the front panel of the Model 6102 is a TTL-level (logic '0' < + 0.8 V_{DC}, logic '1' ≥ + 2.0 V_{DC}) pulse train, at the frequency of the Clock4 signal. The width of the active high pulse is equal to one cycle of the Clock Reference frequency (e. g., 50 nsec if the 20 MHz crystal oscillator is used as the reference). For further information about programming the Clock4 divider, see Section 3.5.1 of this manual. This signal has adequate drive capacity to handle a load equivalent to two 74LS-type inputs.

2.4.3 Comm Port Connectors (COMM A - COMM H)

The eight connectors on the top half of the front panel of the Model 6102 are 16-pin, dual-inline, ribbon cable connectors for the TMS320C40-compatible Comm Ports. These ports provide an alternative to the VMEbus and/or the MIX bus for exchanging data with the Model 6102's input and output buffers, in applications where a 'C40 processor will handle the data. **Comm Ports A, B, C, and D are the Input Ports** (because they carry input data to a 'C40). **They are hardwired as outputs from the 6102 (to deliver data to a 'C40 Comm Port configured as an input) and CANNOT be configured as inputs to the 6102.** These ports may be connected to the default Output Ports (port 0, 1, or 2) of a 'C40 board, as they will force the token and switch the port to an input. Comm Port A carries data from A/D pair A, Port B carries data from A/D pair B, Port C from A/D pair C, and Port D from A/D pair D. **Comm Ports E, F, G, and H are the Output Ports** (because they carry output data from a 'C40). **They are hardwired as inputs to the 6102 (to receive data from a 'C40 Comm Port configured as an output), and CANNOT be configured as outputs from the 6102.** Comm Port E carries data for D/A pair A, Port F carries data for D/A pair B, Port G for D/A pair C, and Port H for D/A pair D. For details about programming the 6102 to use these ports, please refer to Section 3.5.5, Section 3.5.6, Section 3.6.4, and Section 3.6.5.

CAUTION!!

Never connect Comm Ports A, B, C or D on the Model 6102 to another Comm Port that is configured as an output. Serious damage to the output drivers on one or both units will result.

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2.4 Model 6102 Front Panel (continued)

2.4.3 Comm Port Connectors (continued)

Figure 2-8, below left, shows the Comm Port pin assignments. The connector is keyed to prevent improper insertion.

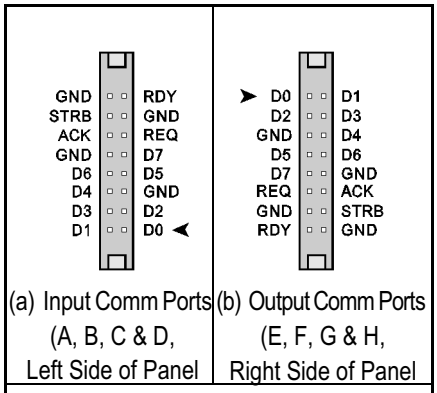


Figure 2-8: Model 6102 - Comm Port Pinouts

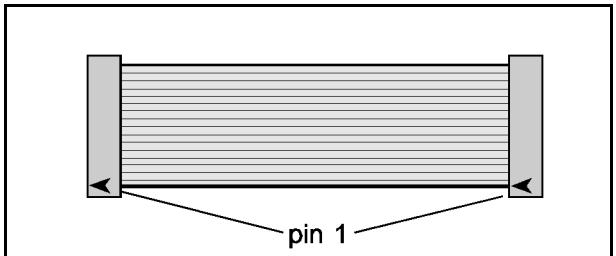


Figure 2-9: Comm Port Cable (Model 2104)

You can assemble your own Comm Port cable, or you can purchase one from Pentek.

Pentek ships every Model 6102 with eight mating connectors (3M #50116-B000, Pentek part # 353.01605) and the optional strain reliefs (3M #3448-50116, Pentek part # 353.01606). Using these connectors, a 3M hand press with locator plate #3443-110 and a standard 16-conductor, 0.050 pitch, flat ribbon cable such as 3M #3365/16 (Pentek part # 378.61600), you can easily assemble a Comm Port cable and configure it to minimize excess cable length for any given interconnect pattern. To maintain consistent assembly techniques, be sure to connect pin 1 of each socket at the end of the cable to pin 1 of the ribbon cable. Pin 1 of the cable is identified by its colored stripe.

If you prefer to purchase purchase a cable, two pre-assembled Comm Port cables up to 18" long are available from Pentek. (Specify the desired cable length when ordering.) The Model 2104 cable mates with the connector on Models 4284, 4270, 4269, 4257 and 4254. The Model 2115 cable mates with the connector on Model 4285. Figure 2-9, above right, shows a typical Comm Port cable.

Each of the twelve signal lines on the Comm Ports is equipped with a series 24Ω resistor to properly match the characteristic impedance of the flat ribbon wiring used in the Comm Port cables.

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2.4 Jumper Settings (continued)

2.4.4 Optional Front Panels for the Model 6102

Option 001 for the Pentek's Model 6102 eliminates the eight A/D converters from the package. The 61023 PC assembly, which normally houses the A/Ds is still included, as this board also contains the VMEbus interface and the Internal Clock Reference oscillator.

The elimination of the A/D circuitry also causes some changes in the layout of the 6102's front panel in this configuration. The Comm Port connectors for the A/D stage (COMM A through COMM D) have been removed. Also the 40-pin analog-input connector has been replaced by a 6-pin connector. A mating connector (Pentek part # 353.06000, Berg # 71600-406) is also included. Figure 2-10, right, shows the new arrangement of the panel, Figure 2-11, below left, gives the pin numbering scheme used for this connector, and Table 2-3, below, gives the connector's pinout.

Option 004 for Pentek's Model 6102 eliminates both the eight D/A converter channels and the MIX interface. In this unit, the 61021 mezzanine board is removed. The front panel for this unit (not shown) would look like the one shown in Figure 2-3, with all the connectors on the right side (COMM E - COMM H and the Analog Output connector) removed.

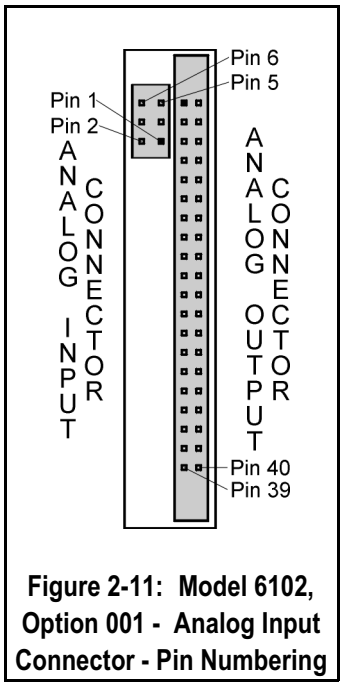


Figure 2-11: Model 6102, Option 001 - Analog Input Connector - Pin Numbering

Table 2-3: Model 6102, Option 001 - Analog Input Connector - Pin Assignments

Clock Signals			
Pin #	**Signal**	**Pin #**	**Signal**
6	N/C	5	N/C
4	Clk. Ref. In Sink (-)	3	Clk.Ref.In Source (+)
2	Ground	1	Clock 1 Out

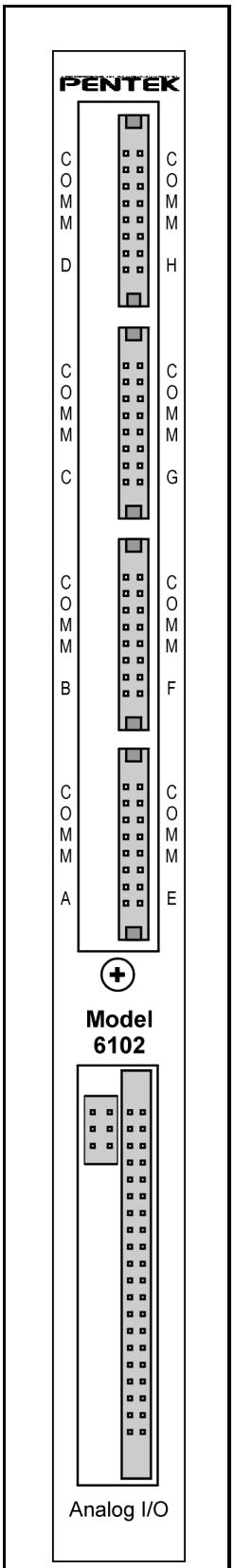


Figure 2-10: Model 6102, Option 001 - Front Panel

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2.5 Installing the Model 6102 in the VMEbus Card Cage

You can use the Model 6102 as either a stand-alone VMEbus card or as a full-depth MIX module. To use this device as a MIX module, you must first install it on a MIX baseboard. See Chapter 1 of the manual entitled "Pentek MIX Tutorial" for MIX stack assembly instructions. Please note that because **full-depth MIX modules** like the Model 6102 must connect to the VMEbus, they **cannot be mounted in the nested position**.

To install either the MIX stack containing the 6102 or the 6102 itself in the VMEbus card cage, **first turn the card-cage power off**. Next, align the upper and lower card edges (of all the MIX modules) with the card cage guides for however many card cage slots the system will occupy. Push evenly on the ejector handles at the top and bottom of the front panel(s) until the panel(s) seats flush against the cage's upper and lower mounting rails. Secure the unit by tightening the upper and lower captive retaining screws at the top and bottom of the front panel(s).

CAUTION!!

Never insert the Model 6102 into a card cage while the power is on.

2.6 Removing the Model 6102 from the VMEbus Card Cage

To remove the Model 6102 (or the MIX stack that contains it) from the VMEbus card cage, **first turn the card-cage power off**. Next, loosen the upper and lower retaining screws (from all the panels in the MIX stack). These are captive screws and will remain attached to the panel(s) after they have disengaged from the mounting rails. Gently push both ejector handles apart, i. e., away from the center of the panel(s), until the unit (or assembly) unseats itself from the card cage connectors. Then pull the unit (or assembly) outward to remove it from the cage.

CAUTION!!

Never remove the Model 6102 from a card cage while the power is on.

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Chapter 3: Memory Maps and Register Descriptions

3.1 Programming Overview

The Model 6102 is controlled by commands sent over the VMEbus or the MIX bus to memory-mapped control registers. This chapter describes each of these registers in detail. The 6102 acts as a slave device on both the VMEbus and the MIX bus.

With respect to the VMEbus, each of the control registers and data FIFOs is mapped into the VMEbus A16 memory space. Access to this address space is determined by the A16 base address switches, which are described in Section 2.2. All control register addresses are given as offsets from the base address defined by the settings of these switches. The form used is A16_base+0xYZ, where YZ is the hexadecimal offset from the base address. This chapter includes a VMEbus meory map to all the Model 6102's registers.

As a MIX bus slave, the Model 6102's MIX_base address is determined by the type of MIX baseboard it is mounted on, and the stack position it occupies on that baseboard. There are two general types of baseboards to be considered: those that use direct MIX addressing (e. g., Pentek's Models 4200/01(A), 4202, 4284 and 4285) and those that use a page register (e. g., Pentek's Model 4283). General information on the use of direct addressing baseboards is given in Chapter 2 of the manual entitled "Pentek MIX Tutorial". Chapter 3 of that manual gives general information on access to MIX modules from baseboards that use an address page register. MIX bus memory maps for use with all Pentek baseboards are also included in this chapter. (Note that the Model 6102 Option 004 does not include a MIX interface.)

Each of the eight A/D converters on the Model 6102 stores the data it acquires in a separate bank of FIFO memory. Similarly, signal generation data for each of the eight D/A channels in the 6102 is written to, and stored in, its own FIFO memory bank. When accessing a FIFO bank, each read or write operation at the FIFO address results in the acquisition or storage of a new data sample. The data FIFOs are the only VMEbus resources on the Model 6102 that are mapped into regions other than A16 space. The A24 and A32 interfaces provide support for block mode data transfers, which are not supported in A16 space. You define the base address(es) for A24 and/or A32 access by writing to a register in A16 space. On the MIX bus side, the FIFO interface is also available in two address regions. Each FIFO is accessible at a single MIX address when the MIX address bit A27 is cleared to the logic '0' state (as in VMEbus A16 space), or in a 256 kByte address range when MXA27 is set to the logic '1' state (as in VMEbus A24/A32 space). When using the data FIFOs in block transfer mode, an access at any address within the given FIFOs address range accesses the next available sample location.

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3.2 VMEbus Address Modifier Codes

There are three addressing modes defined for VMEbus transfers: 32-bit, 24-bit and 16-bit. These modes support a variety of bus devices ranging from simple I/O functions with only a few memory locations to large RAM arrays with hundreds of Megabytes of storage. The addressing mode used for a given transaction is determined by a special 6-bit code that is placed on six dedicated VMEbus lines by the current bus master. This code is known as the Address Modifier, or AM, code. The VMEbus specification defines the usage of certain AM codes as shown in Table 3-1, below. The Model 6102 responds only to those codes shown in the table in the *italic* typeface.

Table 3-1: VMEbus Address Modifier Codes

AM Code	Function
0x3F	***A24 - Standard Supervisory Block Transfer***
0x3E	A24 - Standard Supervisory Program Access
0x3D	***A24 - Standard Supervisory Data Access***
0x3B	***A24 - Standard Nonprivileged Block Transfer***
0x3A	A24 - Standard Nonprivileged Program Access
0x39	***A24 - Standard Nonprivileged Program Access***
0x2D	***A16 - Short Supervisory Access***
0x29	***A16 - Short Nonprivileged Access***
0x0F	***A32 - Extended Supervisory Block Transfer***
0x0E	A32 - Extended Supervisory Program Access
0x0D	***A32 - Extended Supervisory Data Access***
0x0B	***A32 - Extended Nonprivileged Block Transfer***
0x0A	A32 - Extended Nonprivileged Program Access
0x09	***A32 - Extended Nonprivileged Data Access***
0x10 through 0x1F	User Defined
All Others	Reserved

NOTE: The Model 6102 responds to the Address Modifier codes shown in the ***italic*** typeface **ONLY!**

3.3 Slave Address Maps

Table 3-2, on page 31, gives the VMEbus slave memory address map for the resources available on the Model 6102 in A16 space. Most of these resources are accessible for both read and write operations. The exceptions are the eight A/D FIFOs and the four status registers, which are accessible for read operations only; and the Eight D/A FIFOs and the Counter Re-Sync address, which are accessible only for write operations. To access these registers, the bus master that conducts the read or write cycle must select A16 address space by using AM code 2D or 29 (see Table 3-1, above). The 16 FIFOs are accessed in A16/D32 mode. All other A16 resources are accessed in D16 mode. All resources on the Model 6102 are mapped on 4-byte boundaries, i. e., the least-significant hex address digit is either 0, 4, 8, or C. This simplifies master access to the board by DSP-based devices that use 32-bit addressing, such as Pentek's Models 4283, 4284 and 4285.

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3.3 Slave Address Maps (continued)

Table 3-2: Model 6102 - VMEbus A16 Slave Address Map			
Address (hex)	**Access**	**Full name of Resource**	**Symbolic Address**
A16_base+0x00	D32: R. O.	A/D FIFO - Channel A1	AD_FIFO_A1
A16_base+0x04	D32: R. O.	A/D FIFO - Channel A2	AD_FIFO_A2
A16_base+0x08	D32: R. O.	A/D FIFO - Channel B1	AD_FIFO_B1
A16_base+0x0C	D32: R. O.	A/D FIFO - Channel B2	AD_FIFO_B2
A16_base+0x10	D32: R. O.	A/D FIFO - Channel C1	AD_FIFO_C1
A16_base+0x14	D32: R. O.	A/D FIFO - Channel C2	AD_FIFO_C2
A16_base+0x18	D32: R. O.	A/D FIFO - Channel D1	AD_FIFO_D1
A16_base+0x1C	D32: R. O.	A/D FIFO - Channel D2	AD_FIFO_D2
A16_base+0x20	D16: R/W	VMEbus Control Register	V_Ctrl
A16_base+0x24	D16: R/W	VMEbus A32/A24 Address Register	V_Addr
A16_base+0x28	D16: R/W	VMEbus Interrupt Mask Register	V_Int_Mask
A16_base+0x2C - 3C	—	Reserved	—
A16_base+0x40	D16: R/W	Sample Clock 1 Rate Divider	Clk1_Div
A16_base+0x44	D16: R/W	Sample Clock 2 Rate Divider	Clk2_Div
A16_base+0x48	D16: R/W	Sample Clock 3 Rate Divider	Clk3_Div
A16_base+0x4C	D16: R/W	Sample Clock 4 Rate Divider	Clk4_Div
A16_base+0x50	D16: R/W	A/D Trigger Control Register	AD_Trig_Ctrl
A16_base+0x54	D16: R. O.	Status Register - A/D Pairs A and B	AD_Stat_AB
A16_base+0x58	D16: R. O.	Status Register - A/D Pairs C and D	AD_Stat_CD
A16_base+0x5C	D16: R/W	Interrupt Mask Register - A/D Pairs A and B	AD_Mask_AB
A16_base+0x60	D16: R/W	Interrupt Mask Register - A/D Pairs C and D	AD_Mask_CD
A16_base+0x64	D16: R/W	A/D Data Format Register	AD_Data_Fmt
A16_base+0x68	D16: R/W	A/D Single Mode Comm Port Enable Register	AD_Sgl_Com_En
A16_base+0x6C	D16: R/W	A/D FIFO Reset Register	AD_FIFO_Rst
A16_base+0x70	D16: R/W	A/D Clock Select and Sample Counter Register	AD_CkSl_SCt
A16_base+0x74	D16: W. O.	Clock Divider Re-Sync Address	Clk_Div_Sync
A16_base+0x78	D16: R/W	A/D Trigger Re-Arm Control Register	AD_Arm_Ctrl
A16_base+0x7C	—	Reserved	—
A16_base+0x80	D32: W. O.	D/A FIFO - Channel A1	DA_FIFO_A1
A16_base+0x84	D32: W. O.	D/A FIFO - Channel A2	DA_FIFO_A2
A16_base+0x88	D32: W. O.	D/A FIFO - Channel B1	DA_FIFO_B1
A16_base+0x8C	D32: W. O.	D/A FIFO - Channel B2	DA_FIFO_B2
A16_base+0x90	D32: W. O.	D/A FIFO - Channel C1	DA_FIFO_C1
A16_base+0x94	D32: W. O.	D/A FIFO - Channel C2	DA_FIFO_C2
A16_base+0x98	D32: W. O.	D/A FIFO - Channel D1	DA_FIFO_D1
A16_base+0x9C	D32: W. O.	D/A FIFO - Channel D2	DA_FIFO_D2
A16_base+0xA0 - CC	—	Reserved	—
A16_base+0xD0	D16: R/W	D/A Trigger Control Register	DA_Trig_Ctrl
A16_base+0xD4	D16: R. O.	Status Register - D/A Pairs A & B	DA_Stat_AB
A16_base+0xD8	D16: R. O.	Status Register - D/A Pairs C & D	DA_Stat_CD
A16_base+0xDC	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_AB
A16_base+0xE0	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_CD
A16_base+0xE4	D16: R/W	D/A Data Format Register	DA_Data_Fmt
A16_base+0xE8	D16: R/W	D/A Single Mode Comm Port Enable Register	DA_Sgl_Com_En
A16_base+0xEC	D16: R/W	D/A FIFO Reset Register	DA_FIFO_Rstl
A16_base+0xF0	D16: R/W	D/A Clock Select and Sample Counter Register	DA_CkSl_SCt
A16_base+0xF4	D16: R/W	D/A Trigger Re-Arm Control Register	DA_Arm_Ctrl
A16_base+0xF8 - FC	—	Reserved	—

NOTE: The A16_base address is determined by the settings of rotary switches SW1 and SW2. See Figure 2-1 for the physical location of these switches on the Model 6102 PC board, and Section 2.2 for switch setting information.

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3.3 Slave Address Maps (continued)

All VMEbus addresses are expressed in hexadecimal notation, as offsets from the A16_base address. This address is determined by the settings of the two 16-position rotary switches, SW1 and SW2 (see Section 2.2). The A16 memory space occupied by this device is a 256 byte block starting at the A16_base address. All accesses within this region will cause the 6102 to handshake with the VMEbus, and **no other VMEbus device may be mapped within this same 256 byte region of A16 address space**. If more than one 6102 will be used in the same card cage, the A16 Base Address switches must be set to give each board a unique address.

Most of the Model 6102's slave resources are accessible from both the VMEbus and the MIX bus, at identical offsets from the base address for the bus in question. To simplify reference to these resources, each is assigned a symbolic address, which is listed in addition to the physical address in each memory map. These symbolic addresses are used in all subsequent sections of this manual whenever we refer to the address of a resource. For example, in our discussion of the Clock Divider Re-Synchronizing feature, we use the symbolic address Clk_Div_Sync, rather than listing the physical addresses (A16_base+0x74 from the VMEbus, MIX_base+0x74 on a 4200/01(A) baseboard, 0x80 401D on a 4283 baseboard and MIX_base+0x1D on a 4284 or 4285 baseboard, or for an upper MIX bus master (UMBM) on a 4202 baseboard).

As the previous paragraph indicates, when the Model 6102 is operated as a MIX bus slave, its base address is dependent upon the baseboard used. The MIX_base address is also dependent upon the device's position in the MIX stack. The subsections that follow present address maps for the resources available on the Model 6102 for each type of MIX baseboard available from Pentek. Each of the slave resources is assigned a symbolic name, which this manual uses in reference to the resource in subsequent sections. There are five cases to consider, each of which is covered in a separate section.

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3.3 Slave Address Maps (continued)

If the baseboard you are using is a Model 4200, 4200A, 4201 or 4201A, use the address map presented in Section 3.3.1. If you are using your Model 6102 with a Model 4202 baseboard, use the address map in Section 3.3.2. If the Model 4283 is the MIX baseboard for your Model 6102, skip to Section 3.3.3 and use the address map found there. If your 6102 is mounted on a Model 4284 baseboard, use the address map in Section 3.3.4. Finally, if you are using a Model 4285 equipped with a MIX baseboard adapter with your Model 6102, refer to Section 3.3.5 for addressing information.

By convention, the MIX addresses presented in the tables generally appear as eight-digit hexadecimal codes, with a space between the first and second four digits for notational clarity. The form is MIX_base+0xYYYY ZZZZ. The leading '0x' is common notation for a hex value in the 'C' programming language.

Since each hex digit represents four bits, the eight-digit MIX address represents 32 bits of address. As stated above, the MIX_base part of the address is dependent upon the baseboard in use, and is used to select each module by its stack position. This geographical addressing scheme avoids the need for address jumpers and possible conflicts, but requires the software to accommodate the physical placement of modules in the MIX stack.

The exception to this convention is for the Model 4283 baseboard, whose TMS320C30 processor only has a 24-bit address bus on the port it uses for the MIX bus. In this case, a page register is used for module selection (as opposed to different base addresses for each module), and the addresses are given as six-digit hexadecimal codes of the form 0xYY ZZZZ.

A final point must now be made about MIX nomenclature. Module 0 (or MIX position 0) refers to the closest module to the baseboard, whether or not it is nested. Module 1 (or MIX position 1) is the module that may be mounted above Module 0, and Module 2 is the device that may be stacked above Module 1.

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3.3 Slave Address Maps (continued)

3.3.1 Model 6102 MIX Address Map for 4200/01(A) Baseboard

Pentek Models 4200 and 4201 baseboards use a 16 MHz 68030 processor as the MIX bus controller. The 4200A and 4201A use a 40 MHz 68030. From the 68030's viewpoint, the MIX bus is mapped identically for all four of these baseboards. The MIX_base address for Module 0 (which may be nested, sharing the baseboard's VMEbus slot, or stacked in the adjacent slot), is 0xC000 0000. For the next device in the stack, Module 1, the base address is 0xD000 0000. Finally, for the last MIX module in the stack, Module 2, the MIX_base address is 0xE000 0000. Table 3-3, on the next page, gives the physical addresses in the memory space of the baseboard's 68030 processor, and the corresponding symbolic names that represent the Model 6102's slave resources in subsequent sections of this manual.

Note that the 4200 series of VME/MIX Baseboards also support mastering of the MIX bus by Upper MIX Bus Masters (UMBMs), and by other VMEbus masters. For further information about MIX bus access on these baseboards in this manner, please refer to Chapter 2 of the "Pentek MIX Tutorial", or to the baseboard's or UMBM's operating manual.

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3.3 Slave Address Maps (continued)

3.3.1 Model 6102 MIX Address Map for 4200/01(A) Baseboard (continued)

Table 3-3: Model 6102 - MIX Slave Address Map for 4200/01(A) (68030 View)

Address (hex)	Access	Full name of Resource	Symbolic Address
MIX_base+0x00	D32: R. O.	A/D FIFO - Channel A1	AD_FIFO_A1
MIX_base+0x04	D32: R. O.	A/D FIFO - Channel A2	AD_FIFO_A2
MIX_base+0x08	D32: R. O.	A/D FIFO - Channel B1	AD_FIFO_B1
MIX_base+0x0C	D32: R. O.	A/D FIFO - Channel B2	AD_FIFO_B2
MIX_base+0x10	D32: R. O.	A/D FIFO - Channel C1	AD_FIFO_C1
MIX_base+0x14	D32: R. O.	A/D FIFO - Channel C2	AD_FIFO_C2
MIX_base+0x18	D32: R. O.	A/D FIFO - Channel D1	AD_FIFO_D1
MIX_base+0x1C	D32: R. O.	A/D FIFO - Channel D2	AD_FIFO_D2
MIX_base+0x20 - 3C	—	Reserved	—
MIX_base+0x40	D16: R/W	Sample Clock 1 Rate Divider	Clk1_Div
MIX_base+0x44	D16: R/W	Sample Clock 2 Rate Divider	Clk2_Div
MIX_base+0x48	D16: R/W	Sample Clock 3 Rate Divider	Clk3_Div
MIX_base+0x4C	D16: R/W	Sample Clock 4 Rate Divider	Clk4_Div
MIX_base+0x50	D16: R/W	A/D Trigger Control Register	AD_Trig_Ctrl
MIX_base+0x54	D16: R. O.	Status Register - A/D Pairs A and B	AD_Stat_AB
MIX_base+0x58	D16: R. O.	Status Register - A/D Pairs C and D	AD_Stat_CD
MIX_base+0x5C	D16: R/W	Interrupt Mask Register - A/D Pairs A and B	AD_Mask_AB
MIX_base+0x60	D16: R/W	Interrupt Mask Register - A/D Pairs C and D	AD_Mask_CD
MIX_base+0x64	D16: R/W	A/D Data Format Register	AD_Data_Fmt
MIX_base+0x68	D16: R/W	A/D Single Mode Comm Port Enable Register	AD_Sgl_Com_En
MIX_base+0x6C	D16: R/W	A/D FIFO Reset Register	AD_FIFO_Rst
MIX_base+0x70	D16: R/W	A/D Clock Select and Sample Counter Register	AD_CkSl_SCt
MIX_base+0x74	D16: W. O.	Clock Divider Re-Sync Address	Clk_Div_Sync
MIX_base+0x78	D16: R/W	A/D Trigger Re-Arm Control Register	AD_Arm_Ctrl
MIX_base+0x7C	—	Reserved	—
MIX_base+0x80	D32: W. O.	D/A FIFO - Channel A1	DA_FIFO_A1
MIX_base+0x84	D32: W. O.	D/A FIFO - Channel A2	DA_FIFO_A2
MIX_base+0x88	D32: W. O.	D/A FIFO - Channel B1	DA_FIFO_B1
MIX_base+0x8C	D32: W. O.	D/A FIFO - Channel B2	DA_FIFO_B2
MIX_base+0x90	D32: W. O.	D/A FIFO - Channel C1	DA_FIFO_C1
MIX_base+0x94	D32: W. O.	D/A FIFO - Channel C2	DA_FIFO_C2
MIX_base+0x98	D32: W. O.	D/A FIFO - Channel D1	DA_FIFO_D1
MIX_base+0x9C	D32: W. O.	D/A FIFO - Channel D2	DA_FIFO_D2
MIX_base+0xA0	D16: R/W	MIX Control Register	MX_Ctrl
MIX_base+0xA4	D16: W. O.	MIX Interrupt Clear Address	MX_Int_Clr
MIX_base+0xA8 - CC	—	Reserved	—
MIX_base+0xD0	D16: R/W	D/A Trigger Control Register	DA_Trig_Ctrl
MIX_base+0xD4	D16: R. O.	Status Register - D/A Pairs A & B	DA_Stat_AB
MIX_base+0xD8	D16: R. O.	Status Register - D/A Pairs C & D	DA_Stat_CD
MIX_base+0xDC	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_AB
MIX_base+0xE0	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_CD
MIX_base+0xE4	D16: R/W	D/A Data Format Register	DA_Data_Fmt
MIX_base+0xE8	D16: R/W	D/A Single Mode Comm Port Enable Register	DA_Sgl_Com_En
MIX_base+0xEC	D16: R/W	D/A FIFO Reset Register	DA_FIFO_Rstl
MIX_base+0xF0	D16: R/W	D/A Clock Select and Sample Counter Register	DA_CkSl_SCt
MIX_base+0xF4	D16: R/W	D/A Trigger Re-Arm Control Register	DA_Arm_Ctrl
MIX_base+0xF8 - FC	—	Reserved	—

MIX_base Address:
If 6102 is in MIX position 0, MIX_base = 0xC000 0000
If 6102 is in MIX position 1, MIX_base = 0xD000 0000
If 6102 is in MIX position 2, MIX_base = 0xE000 0000

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3.3 Slave Address Maps (continued)

3.3.2 Model 6102 MIX Address Map for the Model 4202 Baseboard

The Model 4202 is a VMEbus slave-only baseboard and contains no processor. Usually, this device is used with standard MIX modules (which do not have VMEbus interfaces of their own) to map the resources connected to its MIX Bus into VMEbus A32, A24 or A16 slave address space. The Model 6102, however, is a full-depth MIX module with a full VMEbus slave interface of its own. Because of this, the only reasonable way to use a 6102 on a 4202 baseboard would be in conjunction with an Upper MIX Bus Master (UMBM), such as the Pentek Models 4270, 4257 or 4254. All of these devices contain TMS320C40 processors, which may gain master access to the MIX bus when mounted on a Model 4202 baseboard.

When MIX slave devices are accessed by a UMBM on a Model 4202 baseboard, the MIX_base address for the slave in MIX position 0 is 0xC000 0000. The MIX_base address of a slave in MIX position 1 in this configuration would be 0xC400 0000, and 0xC800 0000 would be the MIX_base address for a position 2 slave. The above applies without regard to the stack position of the UMBM.

Table 3-4, on the next page, presents the slave memory map for a Model 6102 installed on a Model 4202 baseboard, assuming that the 4202's MIX bus is mastered by a 'C40 Processor MIX module.

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3.3 Slave Address Maps (continued)

3.3.2 Model 6102 MIX Address Map for the Model 4202 Baseboard (continued)

Table 3-4: Model 6102 - MIX Slave Address Map for UMBM on a 4202 Baseboard

Address (hex)	Access	Full name of Resource	Symbolic Address
MIX_base+0x00	D32: R. O.	A/D FIFO - Channel A1	AD_FIFO_A1
MIX_base+0x01	D32: R. O.	A/D FIFO - Channel A2	AD_FIFO_A2
MIX_base+0x02	D32: R. O.	A/D FIFO - Channel B1	AD_FIFO_B1
MIX_base+0x03	D32: R. O.	A/D FIFO - Channel B2	AD_FIFO_B2
MIX_base+0x04	D32: R. O.	A/D FIFO - Channel C1	AD_FIFO_C1
MIX_base+0x05	D32: R. O.	A/D FIFO - Channel C2	AD_FIFO_C2
MIX_base+0x06	D32: R. O.	A/D FIFO - Channel D1	AD_FIFO_D1
MIX_base+0x07	D32: R. O.	A/D FIFO - Channel D2	AD_FIFO_D2
MIX_base+0x08 - 0F	—	Reserved	—
MIX_base+0x10	D16: R/W	Sample Clock 1 Rate Divider	Clk1_Div
MIX_base+0x11	D16: R/W	Sample Clock 2 Rate Divider	Clk2_Div
MIX_base+0x12	D16: R/W	Sample Clock 3 Rate Divider	Clk3_Div
MIX_base+0x13	D16: R/W	Sample Clock 4 Rate Divider	Clk4_Div
MIX_base+0x14	D16: R/W	A/D Trigger Control Register	AD_Trig_Ctrl
MIX_base+0x15	D16: R. O.	Status Register - A/D Pairs A and B	AD_Stat_AB
MIX_base+0x16	D16: R. O.	Status Register - A/D Pairs C and D	AD_Stat_CD
MIX_base+0x17	D16: R/W	Interrupt Mask Register - A/D Pairs A and B	AD_Mask_AB
MIX_base+0x18	D16: R/W	Interrupt Mask Register - A/D Pairs C and D	AD_Mask_CD
MIX_base+0x19	D16: R/W	A/D Data Format Register	AD_Data_Fmt
MIX_base+0x1A	D16: R/W	A/D Single Mode Comm Port Enable Register	AD_Sgl_Com_En
MIX_base+0x1B	D16: R/W	A/D FIFO Reset Register	AD_FIFO_Rstl
MIX_base+0x1C	D16: R/W	A/D Clock Select and Sample Counter Register	AD_CkSl_SCt
MIX_base+0x1D	D16: W. O.	Clock Divider Re-Sync Address	Clk_Div_Sync
MIX_base+0x1E	D16: R/W	A/D Trigger Re-Arm Control Register	AD_Arm_Ctrl
MIX_base+0x1F	—	Reserved	—
MIX_base+0x20	D32: W. O.	D/A FIFO - Channel A1	DA_FIFO_A1
MIX_base+0x21	D32: W. O.	D/A FIFO - Channel A2	DA_FIFO_A2
MIX_base+0x22	D32: W. O.	D/A FIFO - Channel B1	DA_FIFO_B1
MIX_base+0x23	D32: W. O.	D/A FIFO - Channel B2	DA_FIFO_B2
MIX_base+0x24	D32: W. O.	D/A FIFO - Channel C1	DA_FIFO_C1
MIX_base+0x25	D32: W. O.	D/A FIFO - Channel C2	DA_FIFO_C2
MIX_base+0x26	D32: W. O.	D/A FIFO - Channel D1	DA_FIFO_D1
MIX_base+0x27	D32: W. O.	D/A FIFO - Channel D2	DA_FIFO_D2
MIX_base+0x28	D16: R/W	MIX Control Register	MX_Ctrl
MIX_base+0x29	D16: W. O.	MIX Interrupt Clear Address	MX_Int_Clr
MIX_base+0x2A - 33	—	Reserved	—
MIX_base+0x34	D16: R/W	D/A Trigger Control Register	DA_Trig_Ctrl
MIX_base+0x35	D16: R. O.	Status Register - D/A Pairs A & B	DA_Stat_AB
MIX_base+0x36	D16: R. O.	Status Register - D/A Pairs C & D	DA_Stat_CD
MIX_base+0x37	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_AB
MIX_base+0x38	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_CD
MIX_base+0x39	D16: R/W	D/A Data Format Register	DA_Data_Fmt
MIX_base+0x3A	D16: R/W	D/A Single Mode Comm Port Enable Register	DA_Sgl_Com_En
MIX_base+0x3B	D16: R/W	D/A FIFO Reset Register	DA_FIFO_Rstl
MIX_base+0x3C	D16: R/W	D/A Clock Select and Sample Counter Register	DA_CkSl_SCt
MIX_base+0x3C	D16: R/W	D/A Trigger Re-Arm Control Register	DA_Arm_Ctrl
MIX_base+0x3E - 3F	—	Reserved	—
MIX_base Address If 6102 is in MIX position 0, MIX_base = 0xC000 0000 If 6102 is in MIX position 1, MIX_base = 0xC400 0000 If 6102 is in MIX position 2, MIX_base = 0xC800 0000			

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3.3 Slave Address Maps (continued)

3.3.3 Model 6102 MIX Address Map for the Model 4283 Baseboard

On the Model 4283 baseboard, there are two levels of addressing:
1) Selection of the particular expansion module by its stack position; and
2) Selection of one of the resources within the module.

3.3.3.1 Module Selection

The TMS320C30 selects among MIX Modules by using a 2-bit field in the Model 4283 Page Register, located at 'C30 address 0x80 0002. These two bits select one of the three possible MIX stack positions according to Table 3-5, below.

Table 3-5: Model 6102 - Module Selection - Model 4283 Page Register - 'C30 Address 0x80 0002

Page Register Bits>	D31-D18	D17	D16	D15	D14	D13-D0	Example
Stack Position 0	x	MXA27	1	1	MXA21	x	0x01 8000
Stack Position 1	x		1	0		x	0x01 0000
Stack Position 2	x		0	1		x	0x00 8000
x = other functions							

Access to some resources on certain MIX modules may require that either or both of the MIX bus A27 (MX_A27) and A21 (MX_A21) bits be set to the logic '1' state. On the 4283 baseboard, these bits are also contained in the Address Page Register. MX_A27 is the D17 bit of this register, and MX_A21 is the D14 bit. Table 3-5 also shows these bits.

3.3.3.2 Register Selection Within the Module

Once the module has been selected, all the slave resources (including the FIFO banks) of the Model 6102 appear in the TMS320C30 address map according to Table 3-6, shown on the next page. Accessing these registers is accomplished by simply reading and writing these locations. The 24-bit addressing scheme accesses 32-bit data locations for the TMS320C30, even though many of the elements correspond to 16-bit devices.

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3.3 Slave Address Maps (continued)

3.3.3 Model 6102 MIX Address Map for the Model 4283 Baseboard (continued)

3.3.3.2 Register Selection Within the Module (continued)

Table 3-6: Model 6102 - MIX Slave Address Map for Model 4283 Baseboard

4283 'C30 Address	Access	Full name of Resource	Symbolic Address
0x80 4000	D32: R. O.	A/D FIFO - Channel A1	AD_FIFO_A1
0x80 4001	D32: R. O.	A/D FIFO - Channel A2	AD_FIFO_A2
0x80 4002	D32: R. O.	A/D FIFO - Channel B1	AD_FIFO_B1
0x80 4003	D32: R. O.	A/D FIFO - Channel B2	AD_FIFO_B2
0x80 4004	D32: R. O.	A/D FIFO - Channel C1	AD_FIFO_C1
0x80 4005	D32: R. O.	A/D FIFO - Channel C2	AD_FIFO_C2
0x80 4006	D32: R. O.	A/D FIFO - Channel D1	AD_FIFO_D1
0x80 4007	D32: R. O.	A/D FIFO - Channel D2	AD_FIFO_D2
0x80 4008 - F	—	Reserved	—
0x80 4010	D16: R/W	Sample Clock 1 Rate Divider	Clk1_Div
0x80 4011	D16: R/W	Sample Clock 2 Rate Divider	Clk2_Div
0x80 4012	D16: R/W	Sample Clock 3 Rate Divider	Clk3_Div
0x80 4013	D16: R/W	Sample Clock 4 Rate Divider	Clk4_Div
0x80 4014	D16: R/W	A/D Trigger Control Register	AD_Trig_Ctrl
0x80 4015	D16: R. O.	Status Register - A/D Pairs A and B	AD_Stat_AB
0x80 4016	D16: R. O.	Status Register - A/D Pairs C and D	AD_Stat_CD
0x80 4017	D16: R/W	Interrupt Mask Register - A/D Pairs A and B	AD_Mask_AB
0x80 4018	D16: R/W	Interrupt Mask Register - A/D Pairs C and D	AD_Mask_CD
0x80 4019	D16: R/W	A/D Data Format Register	AD_Data_Fmt
0x80 401A	D16: R/W	A/D Single Mode Comm Port Enable Register	AD_Sgl_Com_En
0x80 401B	D16: R/W	A/D FIFO Reset Register	AD_FIFO_Rst
0x80 401C	D16: R/W	A/D Clock Select and Sample Counter Register	AD_CkSl_SCt
0x80 401D	D16: W. O.	Clock Divider Re-Sync Address	Clk_Div_Sync
0x80 401E	D16: R/W	A/D Trigger Re-Arm Control Register	AD_Arm_Ctrl
0x80 401F	—	Reserved	—
0x80 4020	D32: W. O.	D/A FIFO - Channel A1	DA_FIFO_A1
0x80 4021	D32: W. O.	D/A FIFO - Channel A2	DA_FIFO_A2
0x80 4022	D32: W. O.	D/A FIFO - Channel B1	DA_FIFO_B1
0x80 4023	D32: W. O.	D/A FIFO - Channel B2	DA_FIFO_B2
0x80 4024	D32: W. O.	D/A FIFO - Channel C1	DA_FIFO_C1
0x80 4025	D32: W. O.	D/A FIFO - Channel C2	DA_FIFO_C2
0x80 4026	D32: W. O.	D/A FIFO - Channel D1	DA_FIFO_D1
0x80 4027	D32: W. O.	D/A FIFO - Channel D2	DA_FIFO_D2
0x80 4028	D16: R/W	MIX Control Register	MX_Ctrl
0x80 4029	D16: W. O.	MIX Interrupt Clear Address	MX_Int_Clr
0x80 402A - 33	—	Reserved	—
0x80 4034	D16: R/W	D/A Trigger Control Register	DA_Trig_Ctrl
0x80 4035	D16: R. O.	Status Register - D/A Pairs A & B	DA_Stat_AB
0x80 4036	D16: R. O.	Status Register - D/A Pairs C & D	DA_Stat_CD
0x80 4037	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_AB
0x80 4038	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_CD
0x80 4039	D16: R/W	D/A Data Format Register	DA_Data_Fmt
0x80 403A	D16: R/W	D/A Single Mode Comm Port Enable Register	DA_Sgl_Com_En
0x80 403B	D16: R/W	D/A FIFO Reset Register	DA_FIFO_Rstl
0x80 403C	D16: R/W	D/A Clock Select and Sample Counter Register	DA_CkSl_SCt
0x80 403C	D16: R/W	D/A Trigger Re-Arm Control Register	DA_Arm_Ctrl
0x80 403E - 3F	—	Reserved	—

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3.3 Slave Address Maps (continued)

3.3.4 Model 6102 MIX Address Map for the Model 4284 Baseboard

The Model 4284 baseboard uses a TMS320C40 Digital Signal Processor to master transactions with the MIX bus. The three MIX module locations are each mapped into separate, 64 M-Longword regions of the 'C40's memory space. Module 0's MIX_base address in the 'C40 memory map is 0x2000 0000. The MIX_base address for Module 1 is 0x2400 0000, and the 'C40's MIX_base address for Module 2 is 0x2800 0000. Table 3-7, on the next page, presents the memory map for the slave resources on the Model 6102 as seen by the 'C40 processor on the Model 4284 baseboard.

This baseboard also supports mastering of the MIX bus by processor modules in the MIX stack, known as Upper MIX Bus Mmasters (UMBMs). For further details on this type of transaction, please refer to Chapter 2 of the "Pentek MIX Tutorial", the Model 4284 Operating Manual, or the UMBM's Operating Manual.

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3.3 Slave Address Maps (continued)

3.3.4 Model 6102 MIX Address Map for the Model 4284 Baseboard (continued)

Table 3-7: Model 6102 - MIX Slave Address Map for Model 4284 Baseboard

'C40 Address	Access	Full name of Resource	Symbolic Address
MIX_base+0x00	D32: R. O.	A/D FIFO - Channel A1	AD_FIFO_A1
MIX_base+0x01	D32: R. O.	A/D FIFO - Channel A2	AD_FIFO_A2
MIX_base+0x02	D32: R. O.	A/D FIFO - Channel B1	AD_FIFO_B1
MIX_base+0x03	D32: R. O.	A/D FIFO - Channel B2	AD_FIFO_B2
MIX_base+0x04	D32: R. O.	A/D FIFO - Channel C1	AD_FIFO_C1
MIX_base+0x05	D32: R. O.	A/D FIFO - Channel C2	AD_FIFO_C2
MIX_base+0x06	D32: R. O.	A/D FIFO - Channel D1	AD_FIFO_D1
MIX_base+0x07	D32: R. O.	A/D FIFO - Channel D2	AD_FIFO_D2
MIX_base+0x08 - 0F	—	Reserved	—
MIX_base+0x10	D16: R/W	Sample Clock 1 Rate Divider	Clk1_Div
MIX_base+0x11	D16: R/W	Sample Clock 2 Rate Divider	Clk2_Div
MIX_base+0x12	D16: R/W	Sample Clock 3 Rate Divider	Clk3_Div
MIX_base+0x13	D16: R/W	Sample Clock 4 Rate Divider	Clk4_Div
MIX_base+0x14	D16: R/W	A/D Trigger Control Register	AD_Trig_Ctrl
MIX_base+0x15	D16: R. O.	Status Register - A/D Pairs A and B	AD_Stat_AB
MIX_base+0x16	D16: R. O.	Status Register - A/D Pairs C and D	AD_Stat_CD
MIX_base+0x17	D16: R/W	Interrupt Mask Register - A/D Pairs A and B	AD_Mask_AB
MIX_base+0x18	D16: R/W	Interrupt Mask Register - A/D Pairs C and D	AD_Mask_CD
MIX_base+0x19	D16: R/W	A/D Data Format Register	AD_Data_Fmt
MIX_base+0x1A	D16: R/W	A/D Single Mode Comm Port Enable Register	AD_Sgl_Com_En
MIX_base+0x1B	D16: R/W	A/D FIFO Reset Register	AD_FIFO_Rst
MIX_base+0x1C	D16: R/W	A/D Clock Select and Sample Counter Register	AD_CkSl_SCt
MIX_base+0x1D	D16: W. O.	Clock Divider Re-Sync Address	Clk_Div_Sync
MIX_base+0x1E	D16: R/W	A/D Trigger Re-Arm Control Register	AD_Arm_Ctrl
MIX_base+0x1F	—	Reserved	—
MIX_base+0x20	D32: W. O.	D/A FIFO - Channel A1	DA_FIFO_A1
MIX_base+0x21	D32: W. O.	D/A FIFO - Channel A2	DA_FIFO_A2
MIX_base+0x22	D32: W. O.	D/A FIFO - Channel B1	DA_FIFO_B1
MIX_base+0x23	D32: W. O.	D/A FIFO - Channel B2	DA_FIFO_B2
MIX_base+0x24	D32: W. O.	D/A FIFO - Channel C1	DA_FIFO_C1
MIX_base+0x25	D32: W. O.	D/A FIFO - Channel C2	DA_FIFO_C2
MIX_base+0x26	D32: W. O.	D/A FIFO - Channel D1	DA_FIFO_D1
MIX_base+0x27	D32: W. O.	D/A FIFO - Channel D2	DA_FIFO_D2
MIX_base+0x28	D16: R/W	MIX Control Register	MX_Ctrl
MIX_base+0x29	D16: W. O.	MIX Interrupt Clear Address	MX_Int_Clr
MIX_base+0x2A - 33	—	Reserved	—
MIX_base+0x34	D16: R/W	D/A Trigger Control Register	DA_Trig_Ctrl
MIX_base+0x35	D16: R. O.	Status Register - D/A Pairs A & B	DA_Stat_AB
MIX_base+0x36	D16: R. O.	Status Register - D/A Pairs C & D	DA_Stat_CD
MIX_base+0x37	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_AB
MIX_base+0x38	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_CD
MIX_base+0x39	D16: R/W	D/A Data Format Register	DA_Data_Fmt
MIX_base+0x3A	D16: R/W	D/A Single Mode Comm Port Enable Register	DA_Sgl_Com_En
MIX_base+0x3B	D16: R/W	D/A FIFO Reset Register	DA_FIFO_Rstl
MIX_base+0x3C	D16: R/W	D/A Clock Select and Sample Counter Register	DA_CkSl_SCt
MIX_base+0x3C	D16: R/W	D/A Trigger Re-Arm Control Register	DA_Arm_Ctrl
MIX_base+0x3E - 3F	—	Reserved	—
MIX_base Address If 6102 is in MIX position 0, MIX_base = 0x2000 0000 If 6102 is in MIX position 1, MIX_base = 0x2400 0000 If 6102 is in MIX position 2, MIX_base = 0x2800 0000			

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3.3 Slave Address Maps (continued)

3.3.5 Model 6102 Address Map for the Model 4285 MIX Baseboard Adapter

When the Model 4285 is equipped with one of the MIX Expansion Bus Adapters (Options 031 or 036), all eight of its 'C40 processors can access modules on the MIX bus via the 4285's Main bus. Additionally, four of the processors (A, B, E, and F) have a separate access path to devices on the MIX bus via their Global I/O expansion ports. Separate control registers are provided for each of these five interfaces to the MIX bus. Two addressing modes, Normal and Compressed, are available for any of these access paths.

The control registers mentioned above each provide a 5-bit address page field. For this baseboard, however, the page setting is NOT used to determine which MIX module is being addressed (i. e., the direct addressing method is used). The mapping of the page field onto the address bus is a function of the selected addressing mode. For complete details, refer to the Operating Manual for the Model 4285 Adapter Boards (Pentek part # 800.42851). For purposes of this operation summary, we will say that in Normal Addressing Mode, page bit 2 is used to assert the MXA27 address bit, while in Compressed Mode, MXA27 is asserted by 'C40 Global Address bit GA20.

Table 3-8, on the next page, presents the memory map for the slave resources on the Model 6102, as seen by the 'C40 processors on the Model 4285 baseboard. The table also provides the MIX_base addresses, in the memory spaces of the 'C40 processors, for the Expansion bus and Global I/O access paths. For further information on the use of the 4285 as a MIX baseboard, please refer to the 4285 Adapter Board's Operating Manual.

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3.3 Slave Address Maps (continued)

3.3.5 Model 6102 Address Map for the 4285 MIX Baseboard Adapter (continued)

Table 3-8: Model 6102 - Slave Address Map for Model 4285 MIX Baseboard Adapter

'C40 Address	Access	Full name of Resource	Symbolic Address
MIX_base+0x00	D32: R. O.	A/D FIFO - Channel A1	AD_FIFO_A1
MIX_base+0x01	D32: R. O.	A/D FIFO - Channel A2	AD_FIFO_A2
MIX_base+0x02	D32: R. O.	A/D FIFO - Channel B1	AD_FIFO_B1
MIX_base+0x03	D32: R. O.	A/D FIFO - Channel B2	AD_FIFO_B2
MIX_base+0x04	D32: R. O.	A/D FIFO - Channel C1	AD_FIFO_C1
MIX_base+0x05	D32: R. O.	A/D FIFO - Channel C2	AD_FIFO_C2
MIX_base+0x06	D32: R. O.	A/D FIFO - Channel D1	AD_FIFO_D1
MIX_base+0x07	D32: R. O.	A/D FIFO - Channel D2	AD_FIFO_D2
MIX_base+0x08 - 0F	—	Reserved	—
MIX_base+0x10	D16: R/W	Sample Clock 1 Rate Divider	Clk1_Div
MIX_base+0x11	D16: R/W	Sample Clock 2 Rate Divider	Clk2_Div
MIX_base+0x12	D16: R/W	Sample Clock 3 Rate Divider	Clk3_Div
MIX_base+0x13	D16: R/W	Sample Clock 4 Rate Divider	Clk4_Div
MIX_base+0x14	D16: R/W	A/D Trigger Control Register	AD_Trig_Ctrl
MIX_base+0x15	D16: R. O.	Status Register - A/D Pairs A and B	AD_Stat_AB
MIX_base+0x16	D16: R. O.	Status Register -A/D Pairs C and D	AD_Stat_CD
MIX_base+0x17	D16: R/W	Interrupt Mask Register - A/D Pairs A and B	AD_Mask_AB
MIX_base+0x18	D16: R/W	Interrupt Mask Register - A/D Pairs C and D	AD_Mask_CD
MIX_base+0x19	D16: R/W	A/D Data Format Register	AD_Data_Fmt
MIX_base+0x1A	D16: R/W	A/D Single Mode Comm Port Enable Register	AD_Sgl_Com_En
MIX_base+0x1B	D16: R/W	A/D FIFO Reset Register	AD_FIFO_Rst
MIX_base+0x1C	D16: R/W	A/D Clock Select and Sample Counter Register	AD_CkSl_SCt
MIX_base+0x1D	D16: W. O.	Clock Divider Re-Sync Address	Clk_Div_Sync
MIX_base+0x1E	D16: R/W	A/D Trigger Re-Arm Control Register	AD_Arm_Ctrl
MIX_base+0x1F	—	Reserved	—
MIX_base+0x20	D32: W. O.	D/A FIFO - Channel A1	DA_FIFO_A1
MIX_base+0x21	D32: W. O.	D/A FIFO - Channel A2	DA_FIFO_A2
MIX_base+0x22	D32: W. O.	D/A FIFO - Channel B1	DA_FIFO_B1
MIX_base+0x23	D32: W. O.	D/A FIFO - Channel B2	DA_FIFO_B2
MIX_base+0x24	D32: W. O.	D/A FIFO - Channel C1	DA_FIFO_C1
MIX_base+0x25	D32: W. O.	D/A FIFO - Channel C2	DA_FIFO_C2
MIX_base+0x26	D32: W. O.	D/A FIFO - Channel D1	DA_FIFO_D1
MIX_base+0x27	D32: W. O.	D/A FIFO - Channel D2	DA_FIFO_D2
MIX_base+0x28	D16: R/W	MIX Control Register	MX_Ctrl
MIX_base+0x29	D16: W. O.	MIX Interrupt Clear Address	MX_Int_Clr
MIX_base+0x2A - 33	—	Reserved	—
MIX_base+0x34	D16: R/W	D/A Trigger Control Register	DA_Trig_Ctrl
MIX_base+0x35	D16: R. O.	Status Register - D/A Pairs A & B	DA_Stat_AB
MIX_base+0x36	D16: R. O.	Status Register - D/A Pairs C & D	DA_Stat_CD
MIX_base+0x37	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_AB
MIX_base+0x38	D16: R/W	Interrupt Mask Register - D/A Pairs A & B	DA_Mask_CD
MIX_base+0x39	D16: R/W	D/A Data Format Register	DA_Data_Fmt
MIX_base+0x3A	D16: R/W	D/A Single Mode Comm Port Enable Register	DA_Sgl_Com_En
MIX_base+0x3B	D16: R/W	D/A FIFO Reset Register	DA_FIFO_Rstl
MIX_base+0x3C	D16: R/W	D/A Clock Select and Sample Counter Register	DA_CkSl_SCt
MIX_base+0x3C	D16: R/W	D/A Trigger Re-Arm Control Register	DA_Arm_Ctrl
MIX_base+0x3E - 3F	—	Reserved	—

MIX_base Address for Expansion Bus	**MIX_base Address for Global I/O Bus**
If 6102 is in MIX position 0, MIX_base = 0x9000 0000	If 6102 is in MIX position 0, MIX_base = 0xC800 0000
If 6102 is in MIX position 1, MIX_base = 0x9020 0000	If 6102 is in MIX position 1, MIX_base = 0xC820 0000
If 6102 is in MIX position 2, MIX_base = 0x9040 0000	If 6102 is in MIX position 2, MIX_base = 0xC840 0000

NOTE: MXA27 is asserted via page bit 2 in Normal addressing mode, or via 'C40 address bit GA20 in Compressed addressing mode.

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3.4 Bus Control Register Descriptions

The subsections beginning below describe the contents and functions of the resources on the Models 6102 that are associated specifically with how the device interacts with either the VMEbus or the MIX bus. The VMEbus specific registers will be discussed first, followed by the MIX bus specific registers. In general, the registers that deal with VME operatiopn are not accessible from the MIX bus, and those that control MIX bus interaction cannot be accessed from VME.

3.4.1 VMEbus Control Register - R/W @ A16_base+0x20

The VMEbus control register on the Model 6102 contains an 8-bit field for the device's VME Interrupt Vector, a 3-bit field to define the device's VME IRQ level, a Board Reset bit, and four Interrupt Status bits. The bit arrangement in this register is given in Table 3-9, below. The subsections beginning below the table give operating details about the fields and bits in the register.

NOTE: This register **CANNOT** be accessed from the MIX bus.

Table 3-9: Model 6102 - VMEbus Control Register - R/W @ A16_base+0x20

Bit #	D15*	D14*	D13*	D12*	D11	D10	D9	D8
Bit Name	D/A C & D Interrupt Status	D/A A & B Interrupt Status	A/D C & D Interrupt Status	A/D A & B Interrupt Status	Board Reset	VMEbus IRQ Level		
Bit Function	1 = Int. Pending 0 = No Int.	1 = Int. Pending 0 = No Int.	1 = Int. Pending 0 = No Int.	1 = Int. Pending 0 = No Int.	1 = Reset Now 0 = No Action	See Table 3-10, page 46		
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	VMEbus Interrupt Vector Address							
Bit Function	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0
*These bits are read only.								

3.4.1.1 FIFO Interrupt Status Bits - D15 (D/A pairs C & D), D14 (D/A pairs A & B), D13 (A/D pairs C & D), and D12 (A/D pairs A & B) - Read Only

One of these four read-only bits is set when a VME interrupt is issued by the 6102. Reading this register indicates which of the four Interrupt Mask Registers passed the interrupt. When the condition that caused the interrupt is no longer true, the associated bit (i. e., D15, D14, D13 or D12 in this register) reads back in the logic '0' state (i. e., these bits are not latched).

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3.4 Bus Control Register Descriptions (continued)

3.4.1 VMEbus Control Register (continued)

3.4.1.1 FIFO Interrupt Status Bits (continued)

If the D15 bit in this register is set to the logic '1' state when the register is read, then the interrupt came from one of the conditions enabled by the Interrupt Mask Register for D/A pairs C and D (at address DA_Mask_CD). If the D14 bit is set to the logic '1' state, then the interrupt was caused by an enabled condition in the Interrupt Mask Register for D/A pairs A and B (at address DA_Mask_AB). Note that the function of these two bits is not affected by the state of the VME D/A Mask Enable bit (D1) in the VMEbus Interrupt Mask register (at address A16_base+0x28).

If the D13 bit in this register is set to the logic '1' state when the register is read, then the interrupt came from one of the conditions enabled by the Interrupt Mask Register for A/D pairs C and D (at address AD_Mask_CD). If the D12 bit is set to the logic '1' state, then the interrupt was caused by an enabled condition in the Interrupt Mask Register for A/D pairs A and B (at address AD_Mask_AB). Note that the function of these two bits is not affected by the state of the VME A/D Mask Enable bit (D0) in the VMEbus Interrupt Mask register (at address A16_base+0x28).

In either of the cases described above, the Interrupt Status Register for the corresponding Mask Register should be read to determine the exact cause of the interrupt. The Status Register for A/D pairs A and B is at address AD_Stat_AB, and the Status Register for A/D pairs C and D is at address AD_Stat_CD. The Status Register for D/A pairs A and B is at address DA_Stat_AB, and the Status Register for D/A pairs C and D is at address DA_Stat_CD.

Each of these four bits reflects the logical OR of the current states of **all** the interrupt conditions enabled by its respective Mask Register. This means that **all enabled interrupt conditions** for a given group of data converters (i. e., the A & B A/D pairs, the C & D A/D pairs, the A & B D/A pairs or the C & D D/A pairs) **MUST be cleared BEFORE exiting the Interrupt Service Routine**. If the ISR exits before the bit is cleared (by clearing **all** enabled conditions), that group of converters will not be able to generate subsequent interrupts.

Any attempt to write to these four bits will be ignored. In other words, write operations to the VMEbus Control Register with data greater than or equal to 0x1000 will not cause the D15, D14, D13, or D12 bits to be set, nor will write operations with data less than 0x1000 clear these bits.

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3.4 Bus Control Register Descriptions (continued)

3.4.1 VMEbus Control Register (continued)

3.4.1.2 Board Reset Bit - D11

Setting the D11 bit in the Model 6102's VMEbus Control Register to the logic '1' state will execute a Board Reset cycle. The board will be held in the Reset state for as long as this bit remains in the logic '1' state. The Board Reset function should be implemented as a toggle, i. e., this bit should first be set to the logic '1' state, then cleared back to the logic '0' state.

The Reset cycle caused by the activation of this bit clears all 16 data FIFOs, all counters, and all of the slave registers except for the VMEbus Control Register (in which the bit is contained) and the VMEbus Address Register (at address A16_base+0x24). The contents of those registers are unaffected by the Reset.

3.4.1.3 VME Interrupt Request Level Bits - D10 through D8

Table 3-10: Model 6102 - IRQ Level Settings - VMEbus Control Register, Bits D10 through D8

D10	D9	D8	IRQ Lev.
0	0	0	Disabled
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

This 3-bit field determines the Interrupt Request (IRQ) level on which the Model 6102 can issue interrupts to the VMEbus. The VMEbus specification defines seven IRQ levels, IRQ1 through IRQ7. Each corresponds to a separate line on the VMEbus.

To select the IRQ level on which the 6102 can interrupt the bus, write the binary equivalent of the level's number to this 3-bit field. D10 is the most significant bit (i. e., its binary weight is 4), and D8 is the least significant bit (binary weight = 1). This is also the binary code to which the 6102 will respond during the VMEbus Interrupt Acknowledge (IACK) cycle by placing its IACK Vector Address (see Section 3.4.1.4) on the VME data bus.

Clearing all three of these bits to the logic '0' state disables the 6102 as a VMEbus interrupter, because there is no VMEbus line associated with IRQ level 0. Table 3-10, at the left, gives the settings for this bit field for the seven defined IRQ levels.

3.4.1.4 VMEbus IACK Vector Address Bits - D7 through D0

The eight least significant bits in the Model 6102's VMEbus Control Register store the IACK Vector Address. This address is placed on the VME data bus when the 6102 responds to the Interrupt Handler during the IACK cycle. Table 3-9 shows the correspondence between the bits in this register and their destination VME databus lines (bit VA7 is placed on VME D7, etc.).

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3.4 Bus Control Register Descriptions (continued)

3.4.2 VMEbus A32/A24 Address Register - R/W @ A16_base+0x24

The Model 6102 occupies no memory in VME A32 space or A24 space until a write operation to the VMEbus A32/A24 Address Register is performed. The only resources on the 6102 that can be accessed in these regions are the sixteen data FIFOs, which are also accessible in A16 space. The A32 and A24 regions, however, support block mode data transfers, which are not defined in A16 space. This register provides 11 bits to define the A32 base address, three bits to define the A24 base address, one bit to enable A24 access, and a word swap bit. Table 3-11, below, shows the register's bit structure. Detailed descriptions of the bits and fields contained in the register are given in the subsections that begin below the table.

NOTE: This register **CANNOT** be accessed from the MIX bus.

Table 3-11: Model 6102 - VMEbus A24/A32 Address Register - R/W @ A16_base+0x24

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5
Bit Name	VMEbus A32 Base Address										
Bit Function	A31	A30	A29	A28	A27	A26	A25	A24			

Bit #	D4	D3	D2	D1	D0
Bit Name	A24 Enable	VMEbus A24 Address			VME Word Swap
Bit Function	1 = Enable 0 = Disable	A23	A22	A21	1 = Swap 0 = No Swap

3.4.2.1 A32 Base Address Field - Bits D15 through D5

To allow access to the data stored in the Model 6102's FIFO memories in A32 space, the desired base address must be written to the 11 most significant bits of this register. These bits define the upper three hex digits of the 8-digit hex address for A32 access (the lower five digits of the base address are all zeros). There are two restrictions on selecting a base address for A32 space:

1) The 6102 occupies 2 MBytes of A32 memory space. You must select a unique base address so that there is no other device in the card cage that occupies any of the same memory space.

2) Because only 11 bits are provided, the third hex digit of the base address must be even (0, 2, 4, 6, 8, A, C or E). This allows you to select from among 2,048 different base addresses (0x0000 0000 through 0xFFE0 0000).

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3.4 Bus Control Register Descriptions (continued)

3.4.2 VMEbus A32/A24 Address Register (continued)

3.4.2.2 A24 Enable Bit - Bit D4

A24 VME access to the Model 6102 is disabled when this bit is cleared to the logic '0' state, which is its power-up default value. To enable access to the acquired data in A24 space, set this bit to the logic '1' state. If A24 access is enabled, the 6102 will have a 2 MByte presence in BOTH A24 space and A32 space.

3.4.2.3 A24 Base Address Field - Bits D3 through D1

The upper hex digit of the A24 VME base address for the Model 6102 is defined by the settings of these three bits. Because only three bits are provided, there are only eight possible settings for the A24 base address, which are listed in Table 3-12, below. If A24 access is enabled (see Section 3.4.2.2, above), the 6102 will occupy 2 MB of A24 memory space. No other device's resources may occupy any addresses within the selected 2 MByte region.

Table 3-12: Model 6102 - Valid A24 Base Address Settings - VMEbus A32/A24 Address Register, Bits D3- D1

D3 (A23)	D2 (A22)	D1 (A21)	A24_base Address
0	0	0	0x00 0000
0	0	1	0x20 0000
0	1	0	0x40 0000
0	1	1	0x60 0000
1	0	0	0x80 0000
1	0	1	0xA0 0000
1	1	0	0xC0 0000
1	1	1	0xE0 0000

3.4.2.4 Word Swap Bit - D0

The Word Swap bit allows Intel type processors to access the 6102's memory by setting the D0 bit in this register to the logic '1' state. The bit should remain in the default logic '0' state if you are working with a Motorola-type host. This is a very common function in VME cards. Remember that Intel and Motorola processors address words differently. With an Intel host, the upper 16 bits of the 32-bit longword are stored at locations with the VME address line A1 = 1; a Motorola host stores those same bits at locations with A1 = 0.

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3.4 Bus Control Register Descriptions (continued)

3.4.2 VMEbus A32/A24 Address Register (continued)

3.4.2.5 VMEbus A32/A24 Address Map

After any write access to this register, the Model 6102 occupies a 2 MByte region in VMEbus A32 space. If the A24 Enable bit (D4) in this register is set to the logic '1' state, the unit will occupy 2 MByte regions in both A24 and A32 spaces. Remember that the bus master must use different AM codes for A32 and/or A24 accesses than the one used in A16 space. (For a list of allowable AM codes, see Table 3-1.) The only resources that are accessible in A32 or A24 space are the data FIFO memories. The advantage of using A24 or A32 space for readout of the FIFOs is that block transfer is supported in these regions, but is not supported in A16 space.

The offset for each channel's data storage memory is the same in both memory spaces. Table 3-13, below, gives the memory map for these resources in both A32 space and A24 space. Each FIFO occupies a 256 kByte region beginning at the address given in the table. Note that any read (or write) operation conducted at any address within a given FIFO's 256 kByte region accesses the FIFO's input (or output) port. In other words, all accesses to a given FIFO really occur at the same physical location, regardless of the address used. The term VME_base indicates either the A32 base address or the A24 base address, depending upon the region in which the access is conducted.

Table 3-13: Model 6102 - VMEbus A32/A24 Slave Address Map

Start Address (hex)	Access	Resource	Start Address (hex)	Access	Resource
VME_base+0x00 0000	D32: R. O.	A/D Data - Ch. A1	VME_base+0x10 0000	D32: W. O.	D/A Data - Ch. A1
VME_base+0x02 0000	D32: R. O.	A/D Data - Ch. A2	VME_base+0x12 0000	D32: W. O.	D/A Data - Ch. A2
VME_base+0x04 0000	D32: R. O.	A/D Data - Ch. B1	VME_base+0x14 0000	D32: W. O.	D/A Data - Ch. B1
VME_base+0x06 0000	D32: R. O.	A/D Data - Ch. B2	VME_base+0x16 0000	D32: W. O.	D/A Data - Ch. B2
VME_base+0x08 0000	D32: R. O.	A/D Data - Ch. C1	VME_base+0x18 0000	D32: W. O.	D/A Data - Ch. C1
VME_base+0x0A 0000	D32: R. O.	A/D Data - Ch. C2	VME_base+0x1A 0000	D32: W. O.	D/A Data - Ch. C2
VME_base+0x0C 0000	D32: R. O.	A/D Data - Ch. D1	VME_base+0x1C 0000	D32: W. O.	D/A Data - Ch. D1
VME_base+0x0E 0000	D32: R. O.	A/D Data - Ch. D2	VME_base+0x1E 0000	D32: W. O.	D/A Data - Ch. D2

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3.4 Bus Control Register Descriptions (continued)

3.4.3 VMEbus Interrupt Mask Register - R/W @ A16_base+0x28

This register contains only two active bits. These bits must be set to the logic '1' state to allow their respective Interrupt Mask Registers to pass interrupts to the VMEbus. If the D1 bit of this register is cleared to the logic '0' state, then enabled interrupt conditions associated with the D/A FIFOs will not interrupt the VMEbus. If the D0 bit of this register is cleared to the logic '0' state, then enabled interrupt conditions associated with the A/D FIFOs will not interrupt the VMEbus.

Clearing both of these bits to the logic '0' state has the same effect as clearing all three IRQ level bits in the VMEbus Control Register. Either of these actions prevents any enabled interrupt conditions on the Model 6102 from asserting an interrupt on the VMEbus. Table 3-14, below, summarizes the contents of the VMEbus Interrupt Mask Register.

This register **CANNOT** be accessed from the MIX bus.

Table 3-14: Model 6102 - VMEbus Interrupt Mask Register - R/W @ A16_base+0x28

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Not Used						VME D/A Mask Enable	VME A/D Mask Enable
Bit Function	Not Applicable						1 = Enable 0 = Disable	1 = Enable 0 = Disable

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3.4 Bus Control Register Descriptions (continued)

3.4.4 MIX Control Register - R/W @ MX_Ctrl

The MIX Control Register on the Model 6102 contains a pair of bits to enable the Interrupt Mask Registers, Board Reset bit, and four Interrupt Status bits. Table 3-15, below, shows the bit arrangement in this register. The subsections beginning below the table give operating details about the bits in the register.

NOTE: This register **CANNOT** be accessed from the VMEbus.

Table 3-15: Model 6102 - MIX Control Register - R/W @ MX_Ctrl

Bit #	D7*	D6*	D5*	D4*	D3	D2	D1	D0
Bit Name	D/A C & D Interrupt Status	D/A A & B Interrupt Status	D/A C & D Interrupt Status	D/A A & B Interrupt Status	Reserved	Board Reset	MIX D/A Mask Enable	MIX A/D Mask Enable
Bit Function	1 = Int.Pending 0 = No Int.	1 = Int.Pending 0 = No Int.	1 = Int.Pending 0 = No Int.	1 = Int.Pending 0 = No Int.	Always Clear to 0	1 = Reset Now 0 = No Action	1 = Enable 0 = Disable	1 = Enable 0 = Disable

* - These bits are Read Only.

3.4.4.1 FIFO Interrupt Status Bits - D7 (D/A pairs C & D), D6 (D/A pairs A & B), D5 (A/D pairs C & D), and D4 (A/D pairs A & B) - Read Only

When the 6102 issues a MIX interrupt, it sets one of these four read-only bits. Reading this register indicates which of the four Interrupt Mask Registers passed the interrupt. When the condition that caused the interrupt is no longer true, the associated bit (i. e., D7, D6, D5, or D4 in this register) reads back in the logic '0' state (i. e., these bits are not latched).

If the D7 bit in this register is set to the logic '1' state when the register is read, then the interrupt came from one of the conditions enabled by the Interrupt Mask Register for D/A pairs C and D (at address DA_Mask_CD). If the D6 bit is set to the logic '1' state, then the interrupt was caused by an enabled condition in the Interrupt Mask register for D/A pairs A and B (at address DA_Mask_AB). Note that the function of these two bits is not affected by the state of the MIX D/A Mask Enable bit (D1) in this register.

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3.4 Bus Control Register Descriptions (continued)

3.4.4 MIX Control Register (continued)

3.4.4.1 FIFO Interrupt Status Bits (continued)

If the D13 bit in this register is set to the logic '1' state when the register is read, then the interrupt came from one of the conditions enabled by the Interrupt Mask Register for A/D pairs C and D (at address AD_Mask_CD). If the D12 bit is set to the logic '1' state, then the interrupt was caused by an enabled condition in the Interrupt Mask Register for A/D pairs A and B (at address AD_Mask_AB). Note that the function of these two bits is not affected by the state of the MIX A/D Mask Enable bit (D0) in this register.

In either of the cases described above, the Interrupt Status Register for the corresponding Mask Register should be read to determine the exact cause of the interrupt. The Status Register for A/D pairs A and B is at address AD_Stat_AB, and the Status Register for A/D pairs C and D is at address AD_Stat_CD. The Status Register for D/A pairs A and B is at address DA_Stat_AB, and the Status Register for D/A pairs C and D is at address DA_Stat_CD.

Each of these four bits reflects the logical OR of the current states of all the interrupt conditions enabled by its respective Mask Register. This means that (if the appropriate Mask Enable bit is set to the logic '1' state) **ALL enabled interrupt conditions** for a given group of data converters (i. e., the A and B A/D pairs, the C and D A/D pairs, the A and B D/A pairs, or the C and D D/A pairs) **MUST be cleared BEFORE exiting the Interrupt Service Routine**. If the ISR exits before the bit is cleared (by clearing all enabled conditions), that group of converters will not be able to generate subsequent interrupts.

Any attempt to write to these four bits will be ignored. In other words, write operations to the MIX Control Register with data greater than or equal to 0x10 will not set the D7, D6, D5, or D4 bits, nor will write operations with data less than 0x10 clear these bits.

3.4.4.2 Board Reset Bit - D2

Setting the D2 bit in the Model 6102's MIX Control Rregister to the logic '1' state executes a Board Reset cycle. The board will be held in the Reset state for as long as this bit remains in the logic '1' state. The Board Reset function should be implemented as a toggle, i. e., this bit should first be set to the logic '1' state, then cleared back to the logic '0' state.

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3.4 Bus Control Register Descriptions (continued)

3.4.4 MIX Control Register (continued)

3.4.4.2 Board Reset Bit (continued)

The Reset cycle caused by the activation of this bit clears all 16 data FIFOs, all counters, and all of the slave registers except for the VMEbus control register (at address V_Ctrl) and the VMEbus address register (at address V_Addr). The contents of those registers (neither of which is accessible from the MIX bus) is unaffected by the Reset.

3.4.4.3 Interrupt Mask Enable Bits - D1 (D/A Masks) & D0 (A/D Masks)

These bits must be set to the logic '1' state to allow their respective Interrupt Mask Registers to pass interrupts to the MIX bus. If the D1 bit of this register is cleared to the logic '0' state, then enabled interrupt conditions associated with the D/A FIFOs will not interrupt the MIX bus. If the D0 bit of this register is cleared to the logic '0' state, then enabled interrupt conditions associated with the A/D FIFOs will not interrupt the MIX bus.

Clearing both of these bits to the logic '0' state has the same effect for the MIX bus as clearing all three IRQ level bits in the VMEbus Control Register has for the VMEbus. Either of those actions will prevent any enabled interrupt conditions on the Model 6102 from asserting an interrupt on the associated bus.

3.4.5 MIX Interrupt Clear Address - W. O. @ MX_Int_Clr

Writing any data to this address will clear any pending MIX interrupts. Note that if any interrupt condition that is enabled in the Interrupt Mask register for any pair of converters is still true when this address is written, another MIX interrupt will be generated immediately. The Interrupt Service Routine (ISR) should therefore read all Status Registers and make sure all enabled interrupt conditions are cleared before writing to this address. Note that the data written to this address is not used and is therefore trivial.

NOTE: This address **CANNOT** be accessed from the VMEbus.

3.5 A/D Control Register Descriptions

The subsections beginning at the top of the next page cover the registers that control the operation of the Model 6102's A/D Converters. These registers are all accessible via both the VMEbus and MIX bus interfaces.

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3.5 A/D Control Register Descriptions (continued)

3.5.1 Sample Clock Rate Dividers - R/W @ Clk1_Div, Clk2_Div, Clk3_Div & **Clk4_Div**

There are four, independent Sample Rate Generators on the Model 6102, each of which can be programmed for a different Sample Clock Rate. To accommodate this feature, four separate clock dividers are provided, each at a separate address. The programming of the A/D and D/A Clock Select and Sample Counter Registers (at addresses AD_CkSl_SCt, for the A/D converters (see Section 3.5.8), and DA_CkSl_SCt, for the D/A converters (see Section 3.6.7)) determines which divider provides the Sample Clock signal for which pair of converters. Those registers also determine whether the dividers are driven by the internal, 20 MHz crystal oscillator or by the External Clock Reference input (pins 37 and 38 of the front panel Analog Input Connector), which will accept frequencies up to 15 MHz.

These 16-bit dividers divide the frequency of the selected signal by a value equal to the binary quantity with which they are programmed plus one. This allows for a frequency division range from 1 to 65,536. Thus, the Sample Clock's frequency, f_{samp}, is a function of the value programmed into its Clock Divider and the frequency of that divider's selected Clock signal. The equation is:

$$f_{samp} = f_{ref} \div (N + 1)$$

where: f_{samp} = the Sample Clock frequency,
f_{ref} = the frequency of the Reference Clock signal selected to drive the divider,
and, $0 \leq N \leq 65{,}535$ = the number written to the Sample Clock Divider's address

The Sample Clock signal for A/D pair A is always provided by the output of the Sample Clock 1 Rate Divider (Clk1). The Sample Clock 1 Rate Divider's symbolic address is Clk1_Div. The Sample Clock signal for A/D pair B may be provided by Clk1 or by the output of the Sample Clock 2 Rate Divider (Clk2). The Sample Clock 2 Rate Divider's symbolic address is Clk2_Div. The Sample Clock signal for A/D pair C may be provided by Clk1 or by the output of the Sample Clock 3 Rate Divider (Clk3). The Sample Clock 3 Rate Divider's symbolic address is Clk3_Div. The Sample Clock signal for A/D pair D may be provided by Clk1, Clk3, or the output of the Sample Clock 4 Rate Divider (Clk4). The Sample Clock 4 Rate Divider's address is Clk4_Div. As stated previously, the sources of the Sample Clock signals for A/D pairs B, C, and D are selected in the A/D Clock Select and Sample Counter Register at symbolic address AD_CkSl_SCt.

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3.5 A/D Control Register Descriptions (continued)

3.5.1 Sample Clock Rate Dividers (continued)

The Sample Clock signal for D/A pairs A and B may be provided by either Clk1, Clk2, Clk4 or the External D/A Clock signal (pins 3 and 4 of the front panel Analog Output connector). The Sample Clock signal for D/A pairs C and D may be provided by either Clk1, Clk3, Clk4 or the External D/A Clock signal. As stated previously, the sources of the Sample Clock signals for all four D/A pairs are selected in the D/A Clock Select and Sample Counter Register at symbolic address DA_CkSl_SCt.

The maximum Sample Clock Rate for the Model 6102 is 250 kHz. This means that if the internal 20 MHz crystal oscillator is selected as the Reference Clock source for a particular divider, that divider must be programmed to divide by at least 80 (i. e., a number greater than or equal to 79 (0x4F) must be written to that divider's address).

3.5.2 A/D Trigger Control Register - R/W @ AD_Trig_Ctrl

The 16-bit A/D Trigger Control Register provides four types of Triggering controls for each of the four A/D pairs on the Model 6102. One bit for each channel pair resets (or deactivates) that pair's Trigger circuit. Another bit for each pair acts as a software Trigger. A third bit for each pair determines whether the Trigger circuit is edge or level sensitive, and a fourth bit for each pair sets the slope of the signal to which the Trigger circuit for that pair will respond. Table 3-16, below, describes the bit structure of this register. The subsections beginning on the next page provide operational details about the functions of the register's bits.

Table 3-16: Model 6102 - A/D Trigger Control Register - R/W @ AD_Trig_Ctrl

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Ext_AD_Trig_Slope_D	Ext_AD_Trig_Slope_C	Ext_AD_Trig_Slope_B	Ext_AD_Trig_Slope_A	Ext_AD_Trig_Type_D	Ext_AD_Trig_Type_C	Ext_AD_Trig_Type_B	Ext_AD_Trig_Type_A
Bit Function	1 = Positive 0 = Negative				1 = Edge 0 = Level			
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	AD_Soft_Trigger_D	AD_Soft_Trigger_C	AD_Soft_Trigger_B	AD_Soft_Trigger_A	AD_Trigger_Reset_D	AD_Trigger_Reset_C	AD_Trigger_Reset_B	AD_Trigger_Reset_A
Bit Function	1 = Trigger Now 0 = External Trigger Enable				1 = Reset 0 = Ready			

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3.5 A/D Control Register Descriptions (continued)

3.5.2 A/D Trigger Control Register (continued)

3.5.2.1 A/D External Trigger Slope Select Bits - D15 (A/D pair D), D14 (A/D pair C), D13 (A/D pair B), and D12 (A/D pair A)

These four bits, in combination with the A/D External Trigger Type Select bits (see Section 3.5.2.2, on the next page) allow the A/D channel pairs on the Model 6102 to respond to either a high or low Trigger level, or a rising or falling Trigger edge. When the External A/D Trigger input for a channel pair is enabled (i. e., when that pair's Software Trigger bit (see Section 3.5.2.3) is cleared to the logic '0' state), setting the Slope Select bit for that pair to the logic '1' state programs the pair to trigger on either a rising edge or a logic high Trigger signal. If the Slope Select bit is in the logic '0' state and the External A/D Trigger input is enabled, the pair will respond to either a falling edge or a logic low Trigger signal. **The Trigger Reset bit for the associated channel pair must be held in the logic '1' state while any of these bits is being manipulated to prevent false triggering** (see Section 3.5.2.4). Whether the Trigger responds to an edge or a level depends on the state of the pair's A/D External Trigger Type Select bit. Table 3-17, below, summarizes the combined effects of the Slope Select and Type Select bits.

Table 3-17: Model 6102 - A/D External Trigger Control Bits

A/D Trigger Stimulus	Slope Bit (D15: pair D, D14: pair C, D13: pair B, D12: pair A)	Type Bit (D11: pair D, D10: pair C, D9: pair B, D8: pair A)
Low Level	0	0
Falling Edge	0	1
High Level	1	0
Rising Edge	1	1

NOTE: When Level mode is selected, the state indicated in the table starts acquisition, and the opposite state stops acquisition.

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3.5 A/D Control Register Descriptions (continued)

3.5.2 A/D Trigger Control Register (continued)

3.5.2.2 A/D External Trigger Type Select Bits - D11 (A/D pair D), D10 (A/D pair C), D9 (A/D pair B), and D8 (A/D pair A)

These four bits, in combination with the A/D External Trigger Slope Select bits (see Section 3.5.2.1, on the previous page) allow the A/D channel pairs on the Model 6102 to respond to either a high or low Trigger level, or a rising or falling Trigger edge. When the External A/D Trigger input for a channel pair is enabled (i. e., when that pair's Software Trigger bit (see Section 3.5.2.3) is cleared to the logic '0' state), clearing the Trigger Type Select bit for that pair to the logic '0' state will program that pair to Trigger on either a high or low logic level. In this mode, one logic level (the one selected by the Slope Select bit - see Section 3.5.2.1) at the Trigger input will start the acquisition process (i. e., Trigger the channel pair), and the other level will stop sampling (i. e., reset the pair's Trigger). To put it another way, the External A/D Trigger input acts as an enable or gating signal for the sampling process in level-sensitive mode. If the Type Select bit is set to the logic '1' state and the External A/D Trigger input is enabled, the pair will Trigger on either a rising or falling edge. **The Trigger Reset bit for the associated channel pair must be held in the logic '1' state while any of these bits is being manipulated to prevent false triggering** (see Section 3.5.2.4). Whether the pair responds to a positive or negative stimulus depends upon the state of that pair's A/D External Trigger Slope Select bit (see Section 3.5.2.1). Table 3-17, at the bottom of the previous page, summarizes the combined effects of the A/D Slope Select and Type Select bits.

3.5.2.3 A/D Software Trigger Bits - D7 (A/D pair D), D6 (A/D pair C), D5 (A/D pair B), and D4 (A/D pair A)

These four bits activate the A/D Trigger of the Model 6102 through software. Setting one of these bits to the logic '1' state will Trigger the associated A/D channel pair and begin data acquisition.

To allow a given A/D channel pair to respond to the External A/D Trigger input on the front panel Analog Input connector, the associated A/D Software Trigger bit must be held in the logic '0' state.

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3.5 A/D Control Register Descriptions (continued)

3.5.2 A/D Trigger Control Register (continued)

3.5.2.4 A/D Trigger Reset Bits - D3 (A/D pair D), D2 (A/D pair C), D1 (A/D pair B), and D0 (A/D pair A)

Setting one of these four bits to the logic '1' state resets the Trigger circuitry for the associated A/D channel pair, thus stopping the data acquisition process. No data can be acquired by a given channel pair until the associated A/D Trigger Reset bit is cleared to the logic '0' state.

Before manipulating the A/D External Trigger Slope Select and/or Type Select bit for a given channel, set the associated A/D Trigger Reset bit to the logic '1' state to prevent a false trigger from being generated for that A/D channel pair during programming. Once the Slope and Type Select bits are in their desired states, the Reset bit can be cleared back to logic '0'. Then, the next occurrence of the selected signal type (see Table 3-17, on page 56) at the External A/D Trigger input will start the data acquisition process.

3.5.3 A/D Status Registers - R. O. @ AD_Stat_AB (A/D pairs A & B) and AD_Stat_CD (A/D pairs C & D)

There are two Status Registers associated with the A/D converters on the Models 6102; one for the FIFO and status flags for A/D pairs A and B (at address AD_Stat_AB), and another for A/D pairs C and D (at AD_Stat_CD). The structure of these two registers is nearly identical, the only difference being a bit that reflects the A/D Sample Counter Zero status contained in the register for A/D channel pairs A and B. Interrupt Handlers can read these registers to determine the source of an interrupt, or a bus master can poll the flags in this register to see when data is available.

With the exception of the A/D Sample Counter Zero Status bit, none of the bits in the A/D Status Registers is latched, i. e., the bits always reflect the current state of the associated flag or condition. The A/D Status Registers are cleared when the 6102 is reset, but are **NOT** cleared when the registers are read (again, the A/D Sample Counter Zero Status bit is an exception, see Section 3.5.3.5). Table 3-18, on the next page, gives the bit structure of the two A/D status registers. The subsections following the table provide details about the interpretation of the status bits.

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3.5 A/D Control Register Descriptions (continued)

3.5.3 A/D Status Registers (continued)

Table 3-18: Model 6102 - A/D Status Registers

A/D Pairs A and B - R.O. @ AD_Stat_AB								
Bit #	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Bit Name	AD_Trigger_Status_B	AD_B2_FIFO_Half_Full	AD_B2_FIFO_Empty	AD_B2_FIFO_Full	Not Used	AD_B1_FIFO_Half_Full	AD_B1_FIFO_Empty	AD_B1_FIFO_Full
Bit Function	1 = Triggered 0 = Armed	1 = False 0 = True			Always Reads 0	1 = False 0 = True		
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	AD_Trigger_Status_A	AD_A2_FIFO_Half_Full	AD_A2_FIFO_Empty	AD_A2_FIFO_Full	AD_Samp_Ctr_Zero_Status	AD_A1_FIFO_Half_Full	AD_A1_FIFO_Empty	AD_A1_FIFO_Full
Bit Function	1 = Triggered 0 = Armed	1 = False 0 = True			1 = True 0 = False	1 = False 0 = True		
A/D Pairs C and D - R.O. @ AD_Stat_CD								
Bit #	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Bit Name	AD_Trigger_Status_D	AD_D2_FIFO_Half_Full	AD_D2_FIFO_Empty	AD_D2_FIFO_Full	Not Used	AD_D1_FIFO_Half_Full	AD_D1_FIFO_Empty	AD_D1_FIFO_Full
Bit Function	1 = Triggered 0 = Armed	1 = False 0 = True			Always Reads 0	1 = False 0 = True		
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	AD_Trigger_Status_C	AD_C2_FIFO_Half_Full	AD_C2_FIFO_Empty	AD_C2_FIFO_Full	Not Used	AD_C1_FIFO_Half_Full	AD_C1_FIFO_Empty	AD_C1_FIFO_Full
Bit Function	1 = Triggered 0 = Armed	1 = False 0 = True			Always Reads 0	1 = False 0 = True		

3.5.3.1 A/D Trigger Status Bits - D7 (A/D pair A) & D15 (A/D pair B) @ AD_Stat_AB, and D7 (A/D pair C) & D15 (A/D pair D) @ AD_Stat_CD

The Trigger Status bit for a given A/D pair is set to the logic '1' state while that pair is in the process of acquiring data (i. e., Triggered). This condition can generate a VME or MIX interrupt if it is enabled in the appropriate A/D Interrupt Mask Register (see Section 3.5.4.1). If the Trigger Status bit for a given A/D pair is in the logic '0' state when the A/D Status Register is read, then that channel is not acquiring data and its Trigger circuit is armed.

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3.5 A/D Control Register Descriptions (continued)

3.5.3 A/D Status Registers (continued)

3.5.3.2 A/D FIFO Half-Full Flag Bits - D2 (A/D A1), D6 (A/D A2), D10 (A/D B1), & D14 (A/D B2) @ AD_Stat_AB, and D2 (A/D C1), D6 (A/D C2), D10 (A/D D1) & D14 (A/D D2) @ AD_Stat_CD

The Half-Full flag bit for a given A/D channel is cleared to the logic '0' (true) state when at least 512 samples (8,192 samples in units equipped with Option 001) have been collected by that channel. In real-time applications, this is generally the condition (A/D FIFO Half-Full) used to initiate a FIFO readout cycle. This condition can generate a VME or MIX interrupt if it is enabled in the appropriate A/D Interrupt Mask Register (see Section 3.5.4.2). When the FIFO for a given A/D channel contains less than 512 (8,192 for Option 003) samples, this bit is set to the logic '1' (false) state.

3.5.3.3 A/D FIFO Empty Flag Bits - D1 (A/D A1), D5 (A/D A2), D9 (A/D B1), & D13 (A/D B2) @ AD_Stat_AB, and D1 (A/D C1), D5 (A/D C2), D9 (A/D D1) & D13 (A/D D2) @ AD_Stat_CD

The Empty flag bit for a given A/D channel is cleared to the logic '0' (true) state when the FIFO for that channel contains no data. In applications where it is desirable to read samples out as soon as they are acquired, look for this flag to be set to the logic '1' (false) state. This indicates that the FIFO for a given channel contains at least one sample. This condition (A/D FIFO **NOT** Empty) can generate a VME or MIX interrupt if it is enabled in the appropriate A/D Interrupt Mask Register (see Section 3.5.4.3).

3.5.3.4 A/D FIFO Full Flag Bits - D0 (A/D A1), D4 (A/D A2), D8 (A/D B1), & D12 (A/D B2) @ AD_Stat_AB, and D0 (A/D C1), D4 (A/D C2), D8 (A/D D1) & D12 (A/D D2) @ AD_Stat_CD

The Full flag bit for a given A/D channel is cleared to the logic '0' (true) state when there is no room in the FIFO to collect more data. This condition can generate a VME or MIX interrupt if it is enabled in the appropriate A/D Interrupt Mask Register (see Section 3.5.4.4). In real time applications, you can use this bit to indicate that the data readout rate has failed to keep up with the data acquisition rate. As long as this flag remains in the logic '1' (false) state, there is room for at least one more sample in the associated A/D channel's FIFO.

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3.5 A/D Control Register Descriptions (continued)

3.5.3 A/D Status Registers (continued)

3.5.3.5 A/D Sample Counter Zero Status Bit - D3 @ AD_Stat_AB

This bit is set to the logic '1' state when the A/D Sample Counter reaches its zero count. This condition can generate a VME or MIX interrupt if it is enabled in the A/D Interrupt Mask Register for A/D's A & B (see Section 3.5.4.5). The A/D Sample Counter is a modulo-down counter, which means that it counts from a given initial value to zero, then reloads its initial value and repeats the cycle in an infinite loop, until it is reset or otherwise interrupted. The A/D Sample Counter's initial value is written to the lower eight bits of the A/D Clock Select and Sample Counter Register at address AD_CkSl_SCt (see Section 3.5.8.3).

This bit is latched when set so that when the Interrupt Handler or bus master reads the A/D Status Register, the information is still available even though the counter may have advanced. Reading the A/D Status Register clears this bit back to the logic '0' state.

3.5.4 A/D Interrupt Mask Registers - R/W @ AD_Mask_AB (A/D pairs A & B) and AD_Mask_CD (A/D pairs C & D)

There are two Interrupt Mask Registers associated with the A/D Converters on the Model 6102; one for A/D pairs A and B (at symbolic address AD_Mask_AB), and another for A/D pairs C and D (at symbolic address AD_Mask_CD). The bits in this register are set to the logic '1' state to allow a given condition to generate an interrupt. If a given bit in this register is cleared to the logic '0' state, interrupts for the associated condition are masked, or disabled.

The Model 6102 can deliver interrupts to the VMEbus, the MIX bus, or both. In general, it is advisable to select one interface or the other for interrupt handling. Interrupts that are enabled in this register can be prevented from asserting themselves on the MIX bus by clearing the MIX A/D Mask Enable bit in the MIX Control Register (D0 @ MX_Ctrl) to the logic '0' state. Interrupts that are enabled in this register can be prevented from asserting themselves on the VMEbus by clearing the VME A/D Mask Enable bit in the VMEbus Interrupt Mask Register (D0 @ V_Int_Mask) to the logic '0' state.

The structure of these registers is quite similar to the A/D Status Registers. Like the A/D Status Registers, they are nearly identical. The D3 bit serves different purposes in these two registers. In the register for A/D pairs A and B, D3 is the Mask bit for the A/D Sample Counter interrupt. In the register for A/D pairs C and D, the D3 bit replaces the output data from all eight A/D channels with a digital ramp generator (i. e., a 16-bit "up" counter) to enable a data path test.

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3.5 A/D Control Register Descriptions (continued)

3.5.4 A/D Interrupt Mask Registers (continued)

Table 3-19, below, gives the bit structure of these registers. The subsections beginning on the next page describe the conditions you can use to generate interrupts to the VMEbus or the MIX bus.

Table 3-19: Model 6102 - A/D Interrupt Mask Registers

A/D Pairs A and B - R/W @ AD_Mask_AB								
Bit #	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Bit Name	AD_Trigger_Int_B	AD_B2_FIFO_Half_Full	AD_B2_FIFO_Not_Empty	AD_B2_FIFO_Full	Not Used	AD_B1_FIFO_Half_Full	AD_B1_FIFO_Not_Empty	AD_B1_FIFO_Full
Bit Function	1 = Enabled 0 = Masked				Not Applicable	1 = Enabled 0 = Masked		
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	AD_Trigger_Int_A	AD_B1_FIFO_Half_Full	AD_B1_FIFO_Not_Empty	AD_B1_FIFO_Full	AD_Sample_Ctr_Interrupt	AD_A1_FIFO_Half_Full	AD_A1_FIFO_Not_Empty	AD_A1_FIFO_Full
Bit Function	1 = Enabled 0 = Masked							
A/D Pairs C and D - R.O. @ AD_Mask_CD								
Bit #	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Bit Name	AD_Trigger_Int_D	AD_D2_FIFO_Half_Full	AD_D2_FIFO_Not_Empty	AD_D2_FIFO_Full	Not Used	AD_D1_FIFO_Half_Full	AD_D1_FIFO_Not_Empty	AD_D1_FIFO_Full
Bit Function	1 = Enabled 0 = Masked				Not Applicable	1 = Enabled 0 = Masked		
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	AD_Trigger_Int_C	AD_C2_FIFO_Half_Full	AD_C2_FIFO_Not_Empty	AD_C2_FIFO_Full	Not Used	AD_C1_FIFO_Half_Full	AD_C1_FIFO_Not_Empty	AD_C1_FIFO_Full
Bit Function	1 = Enabled 0 = Masked				Not Applicable	1 = Enabled 0 = Masked		

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3.5 A/D Control Register Descriptions (continued)

3.5.4 A/D Interrupt Mask Registers (continued)

3.5.4.1 A/D Trigger Interrupt Mask Bits - D7 (A/D pair A) & D15 (A/D pair B) @ AD_Mask_AB, and D7 (A/D pair C) D15 & (A/D pair D) @ AD_Mask_CD

Setting one of these bits to the logic '1' state will generate an interrupt when the associated A/D channel pair is Triggered (i. e., when data acquisition begins for that pair of converters). The Triggered condition will also set the A/D Trigger Status bit (in the A/D Status Register - see Section 3.5.3.1) associated with that channel pair to the logic '1' state. Clearing any of these bits to the logic '0' state will prevent an interrupt from occurring when the associated channel pair is Triggered.

3.5.4.2 A/D FIFO Half-Full Mask Bits - D2 (A/D A1), D6 (A/D A2), D10 (A/D B1), & D14 (A/D B2) @ AD_Mask_AB, and D2 (A/D C1), D6 (A/D C2), D10 (A/D D1) & D14 (A/D D2) @ AD_Mask_CD

Setting one of these bits to the logic '1' state will generate an interrupt when the FIFO for the associated A/D channel contains at least 512 samples (8,192 for units equipped with Option 003). This condition will also clear the A/D FIFO Half-Full Status bit for the associated channel to the logic '0' (true) state (see Section 3.5.3.2). The A/D FIFO Half-Full condition will not generate an interrupt if the Mask bit associated with that channel is cleared to the logic '0' state.

3.5.4.3 A/D FIFO Not Empty Mask Bits - D1 (A/D A1), D5 (A/D A2), D9 (A/D B1), & D13 (A/D B2) @ AD_Mask_AB, and D1 (A/D C1), D5 (A/D C2), D9 (A/D D1) & D13 (A/D D2) @ AD_Mask_CD

Setting one of these bits to the logic '1' state will generate an interrupt when the FIFO for the associated A/D channel contains at least one sample. This condition will also set the FIFO Empty Status bit for the associated channel to the logic '1' (false) state (see Section 3.5.3.3). The A/D FIFO Not Empty condition will not generate an interrupt if the Mask bit associated with that channel is cleared to the logic '0' state.

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3.5 A/D Control Register Descriptions (continued)

3.5.4 A/D Interrupt Mask Registers (continued)

3.5.4.4 A/D FIFO Full Mask Bits - D0 (A/D A1), D4 (A/D A2), D8 (A/D B1), & D12 (A/D B2) @ AD_Mask_AB, and D0 (A/D C1), D4 (A/D C2), D8 (A/D D1) & D12 (A/D D2) @ AD_Mask_CD

Setting one of these bits to the logic '1' state will generate an interrupt when the FIFO for the associated A/D channel is filled to its capacity (1,024 samples for standard units, 16,384 samples for units equipped with Option 003). This condition will also clear the A/D FIFO Full Status bit for the associated channel to the logic '0' (true) state (see Section 3.5.3.4). The A/D FIFO Full condition will not generate an interrupt if the Mask bit associated with that channel is cleared to the logic '0' state.

3.5.4.5 A/D Sample Counter Interrupt Mask Bit - D3 @ AD_Mask_AB

Set this bit to the logic '1' state to generate an interrupt each time the A/D Sample Counter reaches its zero count. The occurrence of the Sample Counter's zero count will latch the A/D Sample Counter Sero Status bit (D3) in the Status Register for A/D pairs A and B (address AD_Stat_AB) to the logic '1' state (see Section 3.5.3.5). The A/D Sample Counter interrupt will not occur if this bit is cleared to the logic '0' state.

3.5.4.6 Digital A/D Test Ramp Bit - D3 @ AD_Mask_CD

This is the only bit in either of these two registers that is not associated with interrupts. It allows you to perform a data path test, with a known data pattern, by replacing the A/D converters in the data path with a digital ramp generator.

Setting this bit to the logic '1' state disables all eight A/D channels on the Model 6102. The A/D converters are replaced in their respective data paths by eight 16-bit counters. These counters all start at zero and simply count up to their roll-over value and repeat the process. In this test mode, the output data from these counters is passed to the A/D FIFOs and is treated like any other A/D data from that point on.

To use the A/D converters on the Model 6102 to acquire data from the signals applied to the front panel Analog Input connector, this bit must be cleared to the logic '0' state.

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3.5 A/D Control Register Descriptions (continued)

3.5.5 A/D Data Format Register - R/W @ AD_Data_Fmt

This register consists of four 4-bit fields, each associated with how the data from the FIFOs for a given A/D pair is handled. The functions of these bit fields include: the selection of the bus (VME or MIX) or the Comm Port as the destination of the FIFO's data; whether or not the data is packed; and other details about the order in which the acquired data samples are presented at the selected destination. Table 3-21, below, describes the bit structure of the 6102's A/D Data Format Register, gives the valid settings for each 4-bit field, and briefly describes how each setting affects the routing and presentation of the data. The subsections following the table present detailed descriptions of each data presentation mode.

Table 3-20: Model 6102 - A/D Data Format Register - R/W @ AD_Data_Fmt

A/D Pair D	D15	D14	D13	D12	A/D Data Destination, Ordering Mode, Channels Enabled, and Packing Mode
A/D Pair C	D11	D10	D9	D8	
A/D Pair B	D7	D6	D5	D4	
A/D Pair A	D3	D2	D1	D0	
Hex Code	Bit Settings				
0x0	0	0	0	0	Dest = VME/MIX, Channel Ordered, Both Chans Packed
0x1	0	0	0	1	Dest = VME/MIX, Time Ordered, Both Chans Non-Packed
0x2	0	0	1	0	Reserved - Do Not Use
0x3	0	0	1	1	Dest = VME/MIX, Time Ordered, Ch2: Non-Packed, Ch1: Packed
0x4	0	1	0	0	Reserved - Do Not Use
0x5	0	1	0	1	Dest = VME/MIX, Time Ordered, Ch2: Packed, Ch1: Non-Packed
0x6	0	1	1	0	Reserved - Do Not Use
0x7	0	1	1	1	Dest = VME/MIX, Time Ordered, Both Chans Packed
0x8	1	0	0	0	Dest = Comm, Channel Ordered, Both Chans Packed
0x9	1	0	0	1	Dest = Comm, Ch2 Only, Time Ordered, Non-Packed
0xA	1	0	1	0	Reserved - Do Not Use
0xB	1	0	1	1	Dest = Comm, Ch2 Only, Time Ordered, Packed
0xC	1	1	0	0	Reserved - Do Not Use
0xD	1	1	0	1	Dest = Comm, Ch1 Only, Time Ordered, Non-Packed
0XE	1	1	1	0	Reserved - Do Not Use
0xF	1	1	1	1	Dest = Comm, Ch1 Only, Time Ordered, Packed

NOTE: Write 0x1 to a given 4-bit field before writing the desired hex code, to initialize the data-formatting state machine for that channel pair.

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3.5 A/D Control Register Descriptions (continued)

3.5.5 A/D Data Format Register (continued)

NOTE: Before changing the configuration for a given channel pair, the four-bit field in this register associated with that pair must first be set to 0x1 (0,0,0,1) to initialize the A/D channel pair's data formatting state machine. In other words, whatever the desired final contents of this register may be, any field whose contents are to be changed at all must first be changed to 0x1, and then to the desired state.

3.5.5.1 A/D Data Destination Bits - D15 (A/D Pair D), D11 (A/D Pair C), D7 (A/D Pair B) and D3 (A/D Pair A)

When one of these four bits is set to the logic '1' state, acquired data in the FIFOs for the associated A/D channel pair is output on that channel pair's front panel Comm Port connector. If your application would be better suited by reading the data over the VMEbus or the MIX bus, clear the bit(s) associated with the channel(s) to be read over the bus to the logic '0' state.

The third possible path for output data is to route the data from several or all active A/D channels to the Comm Port usually associated with A/D pair A. This is known as Single A/D Comm Port mode. The other Comm Port mode, in which each A/D pair drives its own Comm Port, is alternately referred to as Standard A/D Comm Port mode and Dual A/D Comm Port mode.

For Single A/D Comm Port mode, the Destination bits for the channels to be output on the single port must be cleared to the logic '0' state (i. e., the bus-mode setting). When we discuss data formats available over the A/D Comm Ports in this section, we are referring to the standard or Dual mode Comm Port configuration. Single Mode A/D Comm Port data formats are discussed in Section 3.5.6.

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3.5 A/D Control Register Descriptions (continued)

3.5.5 A/D Data Format Register (continued)

3.5.5.2 A/D Data Packing

Data is always read from the Model 6102 as a 32-bit longword. This applies whether reading the data from the VMEbus, the MIX bus, or the Comm Port. When an A/D pair's 4-bit field in the Data Format Register is programmed for a normal or Non-Packed format, each longword associated with the pair that is read from the 6102 contains one data sample, left justified in the 32-bit field. When an A/D pair's 4-bit field in the Data Format register is programmed for a Packed format, each longword associated with that pair will contain two data samples, and each sample is left justified in a 16-bit field. Table 3-21, below, contains examples of Packed and Non-Packed data formats.

Table 3-21: Model 6102 - A/D Data Ordering and Packing Formats (Bus and Dual Comm Modes)

Channel Ordered Mode (Always Packed)					
D31		**D16**	**D15**		**D0**
(MSB)	Channel 2, Sample N	(LSB)	(MSB)	Channel 1, Sample N	(LSB)
Time Ordered Mode - Packed					
D31		**D16**	**D15**		**D0**
(MSB)	Channel X, Sample N+1	(LSB)	(MSB)	Channel X, Sample N	(LSB)
Time Ordered Mode - Non-Packed					
D31		**D16**	**D15**		**D0**
(MSB)	Channel X, Sample N	(LSB)	Indeterminate		

NOTE: **In time-ordered packed mode, avoid reading an empty FIFO**. In most situations, an attempt to read an empty FIFO will result in an extension of the data cycle, because the FIFO Empty flag holds off the $\overline{\text{DTACK}}$ signal until data is available. However, in Time ordered Packed mode, a holding register follows the FIFO in the data path. The Empty flag goes false as soon as the first sample reaches the FIFO, which causes the $\overline{\text{DTACK}}$ to occur before both samples are available for transfer.

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3.5 A/D Control Register Descriptions (continued)

3.5.5 A/D Data Format Register (continued)

3.5.5.3 A/D Data Ordering

The longwords that are read from the 6102's A/D FIFOs contain data that can be sorted or ordered by Channel or by Time. Channel ordered data can only be delivered in Packed format, while Time ordered data may be Packed or Non-Packed.

When the 4-bit field in the A/D Data Format Register associated with a given channel pair selects Channel ordering, and either the VMEbus or the MIX bus as the data's destination, all data for both channels in the pair is available at the Channel 1 FIFO address. The Channel 2 FIFO address will contain meaningless data in this configuration, and should not be read.

Channel ordering is the only method of reading data from both A/D channels in a given pair over the Comm Port. When the Channel ordered longword is read (either over the Comm Port or over a bus interface), the Channel 2 sample is in the upper 16 bits of the longword, and Channel 1's data is in the lower 16 bits. Channel ordered data is illustrated in the top portion of Table 3-21, on the previous page.

When Time ordering is selected by the 4-bit field in the A/D Data Format Register associated with a given channel pair, there is a major difference between the data available over either bus interface and the data available over the Comm Port. Only one channel from a given pair can deliver data to the pair's Comm Port. The Time ordered data from the selected channel can be formatted in either Packed or Non-Packed mode.

The channel available via the Comm Port is determined by the contents of the 4-bit field associated with the given A/D pair. Any data acquired by the other channel when the field is programmed for Comm Port output in Time ordered mode is **unavailable** via any interface (VME, MIX, Dual-mode port or Single-mode port). Refer to Table 3-20, on page 65, for details on setting the bit fields to select combinations of channel and format.

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3.5 A/D Control Register Descriptions (continued)

3.5.5 A/D Data Format Register (continued)

3.5.5.3 A/D Data Ordering (continued)

On the other hand, when you select the VMEbus or MIX bus as the destination for Time ordered data, not only can you obtain data from both A/D channels, but you gain a great deal of formatting flexibility. You can program the 4-bit field for a given channel pair so that both channels deliver either Packed or Non-Packed data. Additionally, you can program the field so that either A/D channel delivers Packed data while the other channel's data is Non-Packed. Again, Table 3-20 gives the details on programming the bit fields for specific output modes. The two lower sections of Table 3-21, on page 67, illustrate the placement of data samples in the longword in Packed and Non-Packed Time ordered modes.

3.5.6 Single Mode A/D Comm Port Enable Register

- R/W @ AD_Sgl_Com_En

This register provides eight bits, to enable the Single Comm Port mode for each of the eight A/D channels on the Model 6102. In Single Comm Port mode, any combination of the device's eight channels can be made to send their output data to the Comm Port that is nominally assigned to A/D pair A (the one nearest the bottom of the front panel). To enable this output mode for a given channel, the most significant bit in the 4-bit field associated with the channel's pair in the A/D Data Format Register must be cleared to the logic '0' state. Also, the bit in this register associated with the channel in question must be set to the logic '1' state. Table 3-22, below, tells which bit enables which channel. Before writing any new data to this register, all its bits must be cleared to the logic '0' state to initialize the Single Comm Port state machine. In other words, write 0x0 to this register **before** writing the desired channel-enabling code.

Table 3-22: Model 6102 - Single Mode A/D Comm Port Enable Register - R/W @ AD_Sgl_Com_En

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	AD_Chan_ D2_Enable	AD_Chan_ D1_Enable	AD_Chan_ C2_Enable	AD_Chan_ C1_Enable	AD_Chan_ B2_Enable	AD_Chan_ B1_Enable	AD_Chan_ A2_Enable	AD_Chan_ A1_Enable
Bit Function	1 = Enable Channel for Single A/D Comm Port Mode 0 = Disable Channel for Single A/D Comm Port Mode							

NOTES: (1) To initialize the A/D Single Comm Port state machine, write 0x0 to this register before writing the desired value.
(2) In the Data Format Register, select VME/MIX as the destination for the Single Comm Port channels.

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3.5 A/D Control Register Descriptions (continued)

3.5.6 Single Mode A/D Comm Port Enable Register (continued)

Packed data is not supported by the Model 6102 for Single Comm Port mode. This means that many of the formatting options listed in Table 3-21 are not available for the A/D channels that are directed to the Single A/D Comm Port. Thus, if you enable the Single A/D Comm Port feature for both channels from a given A/D channel pair, the only valid formatting selection you can make in that pair's field in the A/D Data Format Register is Option 1 (Time ordered and Non-Packed for both channels). You may also select Option 3 or 5 if only one of the A/D pair's channels is directed to the Single Comm Port. If you select one of these options, the Non-Packed channel (Channel 2 for option 3, Channel 1 for option 5) must be the one that sends its data to the Single Comm Port interface.

When you select the Time ordered, Non-Packed A/D data format, a Channel Identification field is included with each longword sent over the port in Single A/D Comm Port mode, in addition to the sample data. The three LSBs identify the specific A/D channel that the sample came from. Table 3-23, below, illustrates the data format and shows the placement of the channel ID field. The ID field contents are defined in Table 3-24, at the bottom of this page.

Table 3-23: Model 6102 - A/D Data Format (Single Comm Mode)

Time Ordered Mode - Non-Packed		
D31 - D16	**D15 - D3**	**D2 - - - - - - D0**
(MSB) Channel X, Sample N (LSB)	Indeterminate	Channel ID*

* **NOTE:** See Table 3-24, below, for Channel ID Field definitions

Table 3-24: Model 6102 Channel ID Field Definitions for Single A/D Comm Port Mode

Hex	D2	D1	D0	A/D Channel
0x0	0	0	0	A1
0x1	0	0	1	A2
0x2	0	1	0	B1
0x3	0	1	1	B2
0x4	1	0	0	C1
0x5	1	0	1	C2
0x6	1	1	0	D1
0x7	1	1	1	D2

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3.5 A/D Control Register Descriptions (continued)

3.5.6 Single Mode A/D Comm Port Enable Register (continued)

NOTES: 1) The same Sample Clock source **MUST** Clock all A/D channels read in Single A/D Comm Port mode. This assures that each channel in the scan path has data available when expected.

2) You can have some channels send their data to the Single Comm Port interface, others to a bus interface, and still others to their own Dual Comm Port interface. (The exception to remember is that if either channel in a given pair uses the Single Port interface, the other must also use the Single Port or must go unused.) This is where the configurations that have one A/D channel in a given pair Packed and the other channel Non-Packed may be handy. Remember that data bound for the Single Comm Port interface must be Non-Packed. Because the Comm Port connector for A/D channel pair A is the one used for the Single A/D Comm Port interface, you cannot configure Channels A1 and A2 for Dual Comm Port operation while any other A/D channels are configured for Single Port mode.

3.5.7 A/D FIFO Reset Register - R/W @ AD_FIFO_Rst

The A/D FIFO Reset Register contains one bit to clear each A/D channel's FIFO of all data. Clearing a bit to the logic '0' state resets the associated A/D channel's FIFO. The FIFO will be held in the reset state (i. e., no data can be collected) for as long as the associated bit remains at a logic '0'. Thus, the A/D FIFO reset function should be implemented as a toggle, i. e., the appropriate bit should be cleared to the logic '0' state to reset the FIFO, then set back to logic '1' to release the FIFO for data collection. Table 3-25, below, shows which bit is used to reset which A/D channel's FIFO.

Table 3-25: Model 6102 - A/D FIFO Reset Register - R/W @ AD_FIFO_Rst

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	AD_FIFO_ D2_Reset	AD_FIFO_ D1_Reset	AD_FIFO_ C2_Reset	AD_FIFO_ C1_Reset	AD_FIFO_ B2_Reset	AD_FIFO_ B1_Reset	AD_FIFO_ A2_Reset	AD_FIFO_ A1_Reset
Bit Function	1 = Release FIFO and enable data collection 0 = Reset FIFO and disable data collection							
NOTE: Toggle the appropriate bit(s) to implement the reset function.								

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3.5 A/D Control Register Descriptions (continued)

3.5.8 A/D Clock Select and Sample Counter Register - R/W @ AD_CkSl_SCt

The Model 6102 is equipped with four separate Sample Clock Generation circuits, each of which may be driven by the on-board, 20 MHz, crystal oscillator, or by a Clock Reference Input signal applied at the front panel Analog Input connector. These four Sample Clock Generator circuits are essentially simple frequency dividers, and are referred to as Clk1, Clk2, Clk3 and Clk4. Section 3.5.1 discusses these Sample Clock Rate dividers (see page 54). The A/D Clock Select and Sample Counter Register provides four bits that select which of the four rate dividers provides the Sample Clock to which A/D pair. Four more bits in this register are used to select which Reference Clock signal is applied to which rate divider. This register's other eight bits hold the initial value for the A/D Sample Counter, which can be used to interrupt the VMEbus or the MIX bus after a programmed number of samples have been acquired. Table 3-26, below, shows the bit arrangement within the A/D Clock Select and Sample Counter Register. The subsections beginning belowthe table give detailed descriptions of the functions of those bits.

Table 3-26: Model 6102 - A/D Clock Select and Sample Counter Register - R/W @ AD_CkSl_SCt

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	A/Ds_D_ Clk_Sel_1	A/Ds_D_ Clk_Sel_0	A/Ds_C_ Clk_Sel	A/Ds_B_ Clk_Sel	Clk4_Ref _Select	Clk3_Ref _Select	Clk2_Ref _Select	Clk1_Ref _Select
Bit Function	1,1 = Clk4 1,0 = Clk3	0,1 = Reserved 0,0 = Clk1	1 = Clk3 0 = Clk1	1 = Clk2 0 = Clk1	1 = Internal Crystal Oscillator 0 = External Clock Input			
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	A/D Sample Counter Preload Field							
Bit Function	Initial and Modulus Value for A/D Sample Counter							

3.5.8.1 A/D Clock Source Select Bits - D15 & D14 (A/D pair D), D13 (A/D pair C), and D12 (A/D pair B)

There are four A/D Converter pairs on the Model 6102, and there are four separate Sample Clock sources. The Sample Clock sources are referred to as Clk1, Clk2, Clk3 and Clk4. A/D pair A can only be Clocked by Clk1. A/D pair B can be programmed to use either Clk1 or Clk2 as its Sample Clock. To select Clk1, so that A/D pairs A and B are Clocked by the same signal (the default condition after a reset), clear bit D12 in this register to the logic '0' state. To select Clk2, so that these two pairs are clocked independently, set bit D12 in this register to the logic '1' state.

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3.5 A/D Control Register Descriptions (continued)

3.5.8 A/D Clock Select and Sample Counter Register (continued)

3.5.8.1 A/D Clock Source Select Bits (continued)

By manipulating the state of bit D13 in this register, you can have A/D pair C take its Clock signal from either Clk1 or Clk3. To select Clk1 (the reset default), clear D13 to the logic '0' state. To select Clk3, set D13 to the logic '1' state.

By manipulating the states of bits D15 and D14 in this register, you can have A/D pair D take its Clock signal from one of three different sources. To select Clk1 as A/D pair D's Sample Clock, clear both bits to the logic '0' state (again, this is the reset default condition). To select Clk3, set D15 to the logic '1' state and clear D14 to logic '0'. Clk4 is selected when both bits are set to the logic '1' state. Clk2 cannot drive A/D pair D, and the state D15=0 and D14=1 is reserved and should not be used.

3.5.8.2 Clock Divider Reference Select Bits - D11 (Clk4), D10 (Clk3), D9 (Clk2), and D8 (Clk1)

The four Sample Clock divider circuits, referred to in the section above as Clk1, Clk2, Clk3 and Clk4, can all be programmed to accept a Reference Clock signal from the 20 MHz crystal oscillator on the 6102 PC board or from an external signal applied between pins 37 and 38 of the front panel Analog Input connector. The maximum frequency for the external signal is 15 MHz. At frequencies below 200 kHz, the duty cycle must be adjusted such that the signal does not remain in the low state for more than 2.5 µs/cycle. Bit D11 in this register selects the Reference signal for Clk4, D10 for Clk3, D9 for Clk2, and D8 for Clk1. In all cases, setting the bit to the logic '1' state selects the on-board crystal oscillator, and clearing the bit to the logic '0' state selects the external signal source.

NOTE: These bits default to the logic '0' state at power-up, selecting the external signal as the reference.

3.5.8.3 A/D Sample Counter Pre-Load Field - Bits D7 through D0

You can use the Sample Counter on the Model 6102 to generate a VMEbus or MIX bus interrupt upon the capture of every N^{th} sample ($2 \leq N \leq 256$). To enable this function, set the D3 bit in the Interrupt Mask Register for A/D channel pairs A and B, at address AD_Mask_AB, to the logic '1' state. The value (N-1) is programmed into the eight LSBs at address AD_Cksl_SCt to generate an interrupt when the N^{th} sample is taken.

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3.5 A/D Control Register Descriptions (continued)

3.5.8 A/D Clock Select and Sample Counter Register (continued)

3.5.8.3 A/D Sample Counter Pre-Load Field (continued)

NOTE: The A/D Sample Counter Pre-Load Field cannot be programmed to generate an interrupt after the acquisition of only one sample. In situations where you want to acquire one sample and then Re-Arm the Trigger, we offer the following alternative suggestion. Program the channel(s) to accept an undivided External Reference Clock (see Section 3.5.1 and Section 3.5.8.1) and fire the channel's Software Trigger bit in the A/D Trigger Control Register at address AD_Trig_Ctrl (see Section 3.5.2.3). Then, pulse the Reference Clock Input instead of the A/D Trigger Input. The channel's A/D FIFO Not Empty Interrupt can then be used instead of the Sample Counter interrupt to start the processing routine for the single acquired sample.

The sample counter is an 8-bit modulo-down counter. It counts from a preset value (the modulus) down to zero, then returns to the initial value and starts counting down again. If you enable the counter's interrupt, it will occur whenever the counter reaches its zero state. Because the clock pulse that brings the counter to the zero count will also cause the acquisition of a sample, the value written to this field must be one count less than the number of samples to be obtained before the interrupt is generated.

If you select different sample rates for the four A/D pairs, the A/D Sample Counter will count the samples collected by A/D pair A.

3.5.9 Clock Divider Re-Synchronizing Address - W.O. @ Clk_Div_Sync

This address does not correspond to an actual register on the Model 6102. Rather, writing any data to this address causes an action to be taken. The data used in the write operation is unused, and therefore trivial.

When this address is written to, all the Sample Clock Rate Dividers are re-synchronized to the Clk1 divider. This assumes that all four dividers are Clocked by (i. e., referenced to) the same source. The next Sample Clock edge after this register is written to occurs simultaneously for all four Clock circuits, regardless of the possible differences in their Sample Rate programming.

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3.5 A/D Control Register Descriptions (continued)

3.5.9 Clock Divider Re-Synchronizing Address (continued)

This address should not be written to while the A/D converters are gathering data or while the D/A converters are generating signals, as it may cause a Clock glitch to occur at the Clk2, Clk3, or Clk4 output(s). This might lead to an invalid data sample being stored in one or more A/D FIFOs, or to a discontinuity in one or more D/A output signals. Use this address only during initialization or at the end of a data acquisition and/or signal generation sequence to assure that all four divider circuits start out in the same phase.

3.5.10 A/D Trigger Re-Arm Register - R/W @ AD_Arm_Ctrl

This register contains only four active bits, one for each A/D channel pair. To enable automatic Re-Arming of a given A/D channel pair's Trigger circuit when the number of samples programmed into the A/D Sample Counter (see Section 3.5.8.3) have been acquired, set the associated bit to the logic '1' state. Clearing the associated bit to the logic '0' state disables the automatic Re-Arm function. The upper four bits of this register are reserved, and should always be written as '0'.

If the automatic Re-Arm function is enabled, data acquisition will stop after the programmed number of samples has been acquired. The device will wait for the next Trigger to resume the Sampling process. If the automatic Re-Arming function is disabled, acquisition will continue uninterrupted after the programmed number of samples has been acquired.

Table 3-27, below, tells which bit in this register controls the automatic Re-Arm function for which A/D channel pair in the Model 6102.

Table 3-27: Model 6102 - A/D Trigger Re-Arm Register - R/W @ AD_Arm_Ctrl

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved				A/D_pair_ D_Re-Arm	A/D_pair_ C_Re-Arm	A/D_pair_ B_Re-Arm	A/D_pair_ A_Re-Arm
Bit Function	Always Write '0'				1 = Re-Arm A/D Trigger when A/D Sample Counter reaches zero. 0 = Continue sampling when A/D Sample Counter reaches zero.			

3.6 D/A Control Register Descriptions

The subsections beginning at the top of the next page cover the registers that control the operation of the Model 6102's D/A Converters. These registers are all accessible via both the VMEbus and MIX bus interfaces.

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3.6 D/A Control Register Descriptions (continued)

3.6.1 D/A Trigger Control Register - R/W @ DA_Trig_Ctrl

The 16-bit D/A Trigger Control Register provides four types of Triggering controls for each of the four D/A pairs on the Model 6102. One bit for each channel pair resets (or deactivates) that pair's Trigger circuit. Another bit for each pair acts as a software Trigger. A third bit for each pair determines whether the Trigger circuit is edge or level sensitive, and a fourth bit for each pair sets the slope of the signal to which the Trigger circuit for that pair will respond. Table 3-28, below, describes the bit structure of this register. The subsections beginning on the next page provide operational details about the functions of the register's bits.

Table 3-28: Model 6102 - D/A Trigger Control Register - R/W @ DA_Trig_Ctrl

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Ext_DA_Trig_Slope_D	Ext_DA_Trig_Slope_C	Ext_DA_Trig_Slope_B	Ext_DA_Trig_Slope_A	Ext_DA_Trig_Type_D	Ext_DA_Trig_Type_C	Ext_DA_Trig_Type_B	Ext_DA_Trig_Type_A
Bit Function	1 = Positive 0 = Negative				1 = Edge 0 = Level			
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DA_Soft_Trigger_D	DA_Soft_Trigger_C	DA_Soft_Trigger_B	DA_Soft_Trigger_A	DA_Trigger_Reset_D	DA_Trigger_Reset_C	DA_Trigger_Reset_B	DA_Trigger_Reset_A
Bit Function	1 = Trigger Now 0 = External Trigger Enable				1 = Reset 0 = Ready			

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3.6 D/A Control Register Descriptions (continued)

3.6.1 D/A Trigger Control Register (continued)

3.6.1.1 D/A External Trigger Slope Select Bits - D15 (D/A pair D), D14 (D/A pair C), D13 (D/A pair B), and D12 (D/A pair A)

These four bits, in combination with the D/A External Trigger Type Select bits (see Section 3.6.1.2, on the next page) allow the D/A channel pairs on the Model 6102 to respond to either a high or low Trigger level, or a rising or falling Trigger edge. When the External D/A Trigger input for a channel pair is enabled (i. e., when that pair's Software Trigger bit (see Section 3.6.1.3) is cleared to the logic '0' state), setting the Slope Select bit for that pair to the logic '1' state programs the pair to trigger on either a rising edge or a logic high Trigger signal. If the Slope Select bit is in the logic '0' state and the External D/A Trigger input is enabled, the pair will respond to either a falling edge or a logic low Trigger signal. **The Trigger Reset bit for the associated channel pair must be held in the logic '1' state while any of these bits is being manipulated to prevent false triggering** (see Section 3.6.1.4). Whether the Trigger responds to an edge or a level depends on the state of the pair's D/A External Trigger Type Select bit. Table 3-29, below, summarizes the combined effects of the Slope Select and Type Select bits.

Table 3-29: Model 6102 - D/A External Trigger Control Bits

D/A Trigger Stimulus	Slope Bit (D15: pair D, D14: pair C, D13: pair B, D12: pair A)	Type Bit (D11: pair D, D10: pair C, D9: pair B, D8: pair A)
Low Level	0	0
Falling Edge	0	1
High Level	1	0
Rising Edge	1	1

NOTE: When Level mode is selected, the state indicated in the table starts signal generation, and the opposite state stops generation.

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3.6 D/A Control Register Descriptions (continued)

3.6.1 D/A Trigger Control Register (continued)

3.6.1.2 D/A External Trigger Type Select Bits - D11 (D/A pair D), D10 (D/A pair C), D9 (D/A pair B), and D8 (D/A pair A)

These four bits, in combination with the D/A External Trigger Slope Select bits (see Section 3.6.1.1, on the previous page) allow the D/A channel pairs on the Model 6102 to respond to either a high or low Trigger level, or a rising or falling Trigger edge. When the External D/A Trigger input for a channel pair is enabled (i. e., when that pair's Software Trigger bit (see Section 3.6.1.3) is cleared to the logic '0' state), clearing the Trigger Type Select bit for that pair to the logic '0' state will program that pair to Trigger on either a high or low logic level. In this mode, one logic level (the one selected by the Slope Select bit - see Section 3.6.1.1) at the Trigger input will start the signal generation process (i. e., Trigger the channel pair), and the other level will stop signal generation (i. e., reset the pair's Trigger). To put it another way, the External D/A Trigger input acts as an enable or gating signal for the signal generation process in level-sensitive mode. If the Type Select bit is set to the logic '1' state and the External D/A Trigger input is enabled, the pair will Trigger on either a rising or falling edge. **The Trigger Reset bit for the associated channel pair must be held in the logic '1' state while any of these bits is being manipulated to prevent false triggering** (see Section 3.6.1.4). Whether the pair responds to a positive or negative stimulus depends upon the state of that pair's D/A External Trigger Slope Select bit (see Section 3.6.1.1). Table 3-29, at the bottom of the previous page, summarizes the combined effects of the D/A Slope Select and Type Select bits.

3.6.1.3 D/A Software Trigger Bits - D7 (D/A pair D), D6 (D/A pair C), D5 (D/A pair B), and D4 (D/A pair A)

These four bits activate the D/A Trigger of the Model 6102 through software. Setting one of these bits to the logic '1' state will Trigger the associated D/A channel pair and begin signal generation.

To allow a given D/A channel pair to respond to the External D/A Trigger input on the front panel Analog Output connector, the associated D/A Software Trigger bit must be held in the logic '0' state.

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3.6 D/A Control Register Descriptions (continued)

3.6.1 D/A Trigger Control Register (continued)

3.6.1.4 D/A Trigger Reset Bits - D3 (D/A pair D), D2 (D/A pair C), D1 (D/A pair B), and D0 (D/A pair A)

Setting one of these four bits to the logic '1' state resets the Trigger circuitry for the associated D/A channel pair, thus stopping the dignal generation process. No data can be converted by a given channel pair until the associated D/A Trigger Reset bit is cleared to the logic '0' state.

Before manipulating the D/A External Trigger Slope Select and/or Type Select bit for a given channel, set the associated D/A Trigger Reset bit to the logic '1' state to prevent a false trigger from being generated for that D/A channel pair during programming. Once the Slope and Type Select bits are in their desired states, the Reset bit can be cleared back to logic '0'. Then, the next occurrence of the selected signal type (see Table 3-29, on page 77) at the External D/A Trigger input will start the signal generation process.

3.6.2 D/A Status Registers - R. O. @ DA_Stat_AB (D/A pairs A & B), and DA_Stat_CD (D/A pairs C & D)

There are two Status Registers associated with the D/A converters on the Models 6102; one for the FIFO and status flags for D/A pairs A and B (at address DA_Stat_AB), and another for D/A pairs C and D (at DA_Stat_CD). The structure of these two registers is nearly identical, the only difference being a bit that reflects the D/A Sample Counter Zero status contained in the register for D/A channel pairs A and B. Interrupt Handlers can read these registers to determine the source of an interrupt, or a bus master can poll the flags in this register to see when data is available.

With the exception of the D/A Sample Counter Zero Status bit, none of the bits in the D/A Status Registers is latched, i. e., the bits always reflect the current state of the associated flag or condition. The D/A Status Registers are cleared when the 6102 is reset, but are **NOT** cleared when the registers are read (again, the D/A Sample Counter Zero Status bit is an exception, see Section 3.6.2.5). Table 3-30, on the next page, gives the bit structure of the two D/A status registers. The subsections following the table provide details about the interpretation of the status bits.

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3.6 D/A Control Register Descriptions (continued)

3.6.2 D/A Status Registers (continued)

Table 3-30: Model 6102 - D/A Status Registers

D/A Pairs A and B - R.O. @ DA_Stat_AB								
Bit #	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Bit Name	DA_Trigger _Status_B	DA_B2_FIFO _Half_Full	DA_B2_FIFO _Empty	DA_B2_FIFO _Full	Not Used	DA_B1_FIFO _Half_Full	DA_B1_FIFO _Empty	DA_B1_FIFO _Full
Bit Function	1 = Triggered 0 = Armed	1 = False 0 = True			Always Reads 0	1 = False 0 = True		
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DA_Trigger _Status_A	DA_A2_FIFO _Half_Full	DA_A2_FIFO _Empty	DA_A2_FIFO _Full	DA_Samp_Ctr _Zero_Status	DA_A1_FIFO _Half_Full	DA_A1_FIFO _Empty	DA_A1_FIFO _Full
Bit Function	1 = Triggered 0 = Armed	1 = False 0 = True			1 = True 0 = False	1 = False 0 = True		
D/A Pairs C and D - R.O. @ DA_Stat_CD								
Bit #	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Bit Name	DA_Trigger _Status_D	DA_D2_FIFO _Half_Full	DA_D2_FIFO _Empty	DA_D2_FIFO _Full	Not Used	DA_D1_FIFO _Half_Full	DA_D1_FIFO _Empty	DA_D1_FIFO _Full
Bit Function	1 = Triggered 0 = Armed	1 = False 0 = True			Always Reads 0	1 = False 0 = True		
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DA_Trigger _Status_C	DA_C2_FIFO _Half_Full	DA_C2_FIFO _Empty	DA_C2_FIFO _Full	Not Used	DA_C1_FIFO _Half_Full	DA_C1_FIFO _Empty	DA_C1_FIFO _Full
Bit Function	1 = Triggered 0 = Armed	1 = False 0 = True			Always Reads 0	1 = False 0 = True		

3.6.2.1 D/A Trigger Status Bits - D7 (D/A pair A) & D15 (D/A pair B) @ DA_Stat_AB, and D7 (D/A pair C) & D15 (D/A pair D) @ DA_Stat_CD

The Trigger Status bit for a given D/A pair is set to the logic '1' state while that pair is in the process of generating signals (i. e., Triggered). This condition can generate a VME or MIX interrupt if it is enabled in the appropriate D/A Interrupt Mask Register (see Section 3.6.3.1). If the Trigger Status bit for a given D/A pair is in the logic '0' state when the D/A Status Register is read, then that channel is not generating signals and its Trigger circuit is armed.

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3.6 D/A Control Register Descriptions (continued)

3.6.2 D/A Status Registers (continued)

3.6.2.2 D/A FIFO Half-Full Flag Bits - D2 (D/A A1), D6 (D/A A2), D10 (D/A B1), & D14 (D/A B2) @ DA_Stat_AB, and D2 (D/A C1), D6 (D/A C2), D10 (D/A D1), & D14 (D/A D2) @ DA_Stat_CD

The Half-Full flag bit for a given D/A channel is set to the logic '1' (false) state when space is available to write at least 512 samples (8,192 samples in units equipped with Option 001) into that channel's FIFO. In real-time applications, this is generally the condition (D/A FIFO Half-Full) used to initiate a FIFO write cycle (i. e., FIFO **NOT** Half-Full). This condition can generate a VME or MIX interrupt if it is enabled in the appropriate D/A Interrupt Mask Register (see Section 3.6.3.2). When the FIFO for a given D/A channel contains more than 512 (8,192 for Option 003) samples, this bit is cleared to the logic '0' (true) state.

3.6.2.3 D/A FIFO Empty Flag Bits - D1 (D/A A1), D5 (D/A A2), D9 (D/A B1), & D13 (D/A B2) @ DA_Stat_AB, and D1 (D/A C1), D5 (D/A C2), D9 (D/A D1), & D13 (D/A D2) @ DA_Stat_CD

The Empty flag bit for a given D/A channel is cleared to the logic '0' (true) state when the FIFO for that channel contains no data. This condition can generate a VME or MIX interrupt if it is enabled in the appropriate D/A Interrupt Mask Register (see Section 3.6.3.3). In real time applications, you can use this bit to indicate that the data write rate has failed to keep up with the sample output rate. As long as this flag remains in the logic '1' (false) state, there is at least one more new sample in the associated D/A channel's FIFO to provide fresh input for the DAC. Note that the last sample in a given channel's D/A FIFO will be reused until new data is written to the FIFO, to prevent transients in the D/A output.

3.6.2.4 D/A FIFO Full Flag Bits - D0 (D/A A1), D4 (D/A A2), D8 (D/A B1), & D12 (D/A B2) @ DA_Stat_AB, and D0 (D/A C1), D4 (D/A C2), D8 (D/A D1), & D12 (D/A D2) @ DA_Stat_CD

The Full flag bit for a given D/A channel is set to the logic '1' (false) state when space is available in the FIFO to write more data. This condition (D/A FIFO **NOT** Full) can generate a VME or MIX interrupt if it is enabled in the appropriate D/A Interrupt Mask Register (see Section 3.6.3.4). When this flag is in the logic '0' (true) state, there is no space available for new samples in the associated D/A channel's FIFO. D/A FIFO Full is generally the desired initial condition for signal generation scenarios.

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3.6 D/A Control Register Descriptions (continued)

3.6.2 D/A Status Registers (continued)

3.6.2.5 D/A Sample Counter Zero Status Bit - D3 @ DA_Stat_AB

This bit is set to the logic '1' state when the D/A Sample Counter reaches its zero count. This condition can generate a VME or MIX interrupt if it is enabled in the D/A Interrupt Mask Register for D/A's A & B (see Section 3.6.3.5). The D/A Sample Counter is a modulo-down counter, which means that it counts from a given initial value to zero, then reloads its initial value and repeats the cycle in an infinite loop, until it is reset or otherwise interrupted. The D/A Sample Counter's initial value is written to the lower eight bits of the D/A Clock Select and Sample Counter Register at address DA_CkSl_SCt (see Section 3.6.7.2).

This bit is latched when set so that when the Interrupt Handler or bus master reads the D/A Status Register, the information is still available even though the counter may have advanced. Reading the D/A Status Register clears this bit back to the logic '0' state.

3.6.3 D/A Interrupt Mask Registers - R/W @ DA_Mask_AB (D/A pairs A & B), and DA_Mask_CD (D/A pairs C & D)

There are two Interrupt Mask Registers associated with the D/A Converters on the Model 6102; one for D/A pairs A and B (at symbolic address DA_Mask_AB), and another for D/A pairs C and D (at symbolic address DA_Mask_CD). The bits in this register are set to the logic '1' state to allow a given condition to generate an interrupt. If a given bit in this register is cleared to the logic '0' state, interrupts for the associated condition are masked, or disabled.

The Model 6102 can deliver interrupts to the VMEbus, the MIX bus, or both. In general, it is advisable to select one interface or the other for interrupt handling. Interrupts that are enabled in this register can be prevented from asserting themselves on the MIX bus by clearing the MIX D/A Mask Enable bit in the MIX Control Register (D1 @ MX_Ctrl) to the logic '0' state. Interrupts that are enabled in this register can be prevented from asserting themselves on the VMEbus by clearing the VME D/A Mask Enable bit in the VMEbus Interrupt Mask Register (D1 @ V_Int_Mask) to the logic '0' state.

The structure of these registers is quite similar to the D/A Status Registers. Like the D/A Status Registers, they are nearly identical. The only difference between the two is the D3 bit, which is unused in the Mask Register for D/A pairs C and D. In the Mask Register for D/A pairs A and B, D3 is the Mask bit for the D/A Sample Counter interrupt.

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3.6 D/A Control Register Descriptions (continued)

3.6.3 D/A Interrupt Mask Registers (continued)

Table 3-31, below, gives the bit structure of these registers. The subsections beginning below the table describe the conditions you can use to generate interrupts to the VMEbus or the MIX bus.

Table 3-31: Model 6102 - D/A Interrupt Mask Registers

D/A Pairs A and B - R/W @ DA_Mask_AB								
Bit #	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Bit Name	DA_Trigger_Int_B	DA_B2_FIFO_Not_Half_Full	DA_B2_FIFO_Empty	DA_B2_FIFO_Not_Full	Not Used	DA_B1_FIFO_Not_Half_Full	DA_B1_FIFO_Empty	DA_B1_FIFO_Not_Full
Bit Function	1 = Enabled 0 = Masked				Not Applicable	1 = Enabled 0 = Masked		
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DA_Trigger_Int_A	DA_B1_FIFO_Not_Half_Full	DA_B1_FIFO_Empty	DA_B1_FIFO_Not_FullI	DA_Sample_Ctr_Interrupt	DA_A1_FIFO_Not_Half_Full	DA_A1_FIFO_Empty	DA_A1_FIFO_Not_Full
Bit Function	1 = Enabled 0 = Masked							
D/A Pairs C and D - R.O. @ DA_Mask_CD								
Bit #	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Bit Name	DA_Trigger_Int_D	DA_D2_FIFO_Not_Half_Full	DA_D2_FIFO_Empty	DA_D2_FIFO_Not_Full	Not Used	DA_D1_FIFO_Not_Half_Full	DA_D1_FIFO_Empty	DA_D1_FIFO_Not_Full
Bit Function	1 = Enabled 0 = Masked				Not Applicable	1 = Enabled 0 = Masked		
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	DA_Trigger_Int_C	DA_C2_FIFO_Not_Half_Full	DA_C2_FIFO_Empty	DA_C2_FIFO_Not_Full	Not Used	DA_C1_FIFO_Not_Half_Full	DA_C1_FIFO_Empty	DA_C1_FIFO_Not_Full
Bit Function	1 = Enabled 0 = Masked				Not Applicable	1 = Enabled 0 = Masked		

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3.6 D/A Control Register Descriptions (continued)

3.6.3 D/A Interrupt Mask Registers (continued)

3.6.3.1 D/A Trigger Interrupt Mask Bits - D7 (D/A Pair A) & D15 (D/A Pair B) @ DA_Mask_AB, and D7 (D/A Pair C) & D15 (D/A Pair D) @ DA_Mask_CD

Setting one of these bits to the logic '1' state will generate an interrupt when the associated D/A channel pair is Triggered (i. e., when signal generation begins for that pair of converters). The Triggered condition will also set the D/A Trigger Status bit (in the D/A Status Register - see Section 3.6.2.1) associated with that channel pair to the logic '1' state. Clearing any of these bits to the logic '0' state will prevent an interrupt from occurring when the associated channel pair is Triggered.

3.6.3.2 D/A FIFO Not Half-Full Mask Bits - D2 (D/A A1), D6 (D/A A2), D10 (D/A B1), & D14 (D/AD B2) @ DA_Mask_AB, and D2 (D/A C1), D6 (D/A C2), D10 (D/A D1) & D14 (D/A D2) @ DA_Mask_CD

Setting these bits to the logic '1' state generates an interrupt when the FIFO for the associated D/A channel contains less than 512 (8,192 for units equipped with Option 002) samples. This condition also sets the D/A FIFO Half-Full status bit for the associated channel to the logic '1' (false) state (see Section 3.6.2.2). The D/A FIFO Not Half-Full condition will not generate an interrupt if the Mask bit associated with that D/A channel is cleared to the logic '0' state.

3.6.3.3 D/A FIFO Empty Mask Bits - D1 (D/A A1), D5 (D/A A2), D9 (D/A B1), & D13 (D/A B2) @ DA_Mask_AB, and D1 (D/A C1), D5 (D/A C2), D9 (D/A D1), & D13 (D/A D2) @ DA_Mask_CD

Setting these bits to the logic '1' state generates an interrupt when the FIFO for the associated D/A channel contains no new samples. This condition also sets the D/A FIFO Empty status bit for the associated channel to the logic '0' (true) state (see Section 3.6.2.3). The D/A FIFO Empty condition will not generate an interrupt if the Mask bit associated with that D/A channel is cleared to the logic '0' state.

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3.6 D/A Control Register Descriptions (continued)

3.6.3 D/A Interrupt Mask Registers (continued)

3.6.3.4 D/A FIFO Not Full Mask Bits - D0 (D/A A1), D4 (D/A A2), D8 (D/A B1),& D12 (D/A B2) @ DA_Mask_AB, and D0 (D/A C1), D4 (D/A C2), D8 (D/A D1), & D12 (D/A D2) @ DA_Mask_CD

Seting these bits are set to the logic '1' state generates an interrupt whenever there is space left in the FIFO for the associated D/A channel to write at least one sample. This condition also sets the D/A FIFO Full status bit for the associated channel to the logic '1' (false) state (see Section 3.6.2.4). The D/A FIFO Not Full condition will not generate an interrupt if the Mask bit associated with that channel is cleared to the logic '0' state.

3.6.3.5 D/A Sample Counter Interrupt Mask Bit - D3 @ AD_Mask_AB

Setting this bit to the logic '1' state generates an interrupt each time the D/A Sample Counter reaches its zero count. The occurrence of the Sample Counter's zero count latches the D/A Sample Counter Zero Status bit (D3) in the Status Register for D/A pairs A and B (address DA_Stat_AB) to the logic '1' state (see Section 3.6.2.5). The D/A Sample Counter interrupt will not occur if this bit is cleared to the logic '0' state.

3.6.4 D/A Data Format Register - R/W @ DA_Data_Fmt

This register consists of four 4-bit fields, each associated with how you must format the data written to the FIFOs for a given D/A pair. The functions of these bit fields include: the selection of the bus (VME or MIX) or the Comm Port as the source of the FIFO's data; whether or not the data is packed; and other details about the order in which the signal generation samples are sent to the FIFO. Table 3-32, at the top of the next page, describes the bit structure of the 6102's D/A Data Format Register, gives the valid settings for each 4-bit field, and briefly describes how each setting affects the format in which the FIFO expects to find the data. The subsections following the table present detailed descriptions of each data formatting mode.

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3.6 D/A Control Register Descriptions (continued)

3.6.4 D/A Data Format Register (continued)

Table 3-32: Model 6102 - D/A Data Format Register - R/W @ DA_Data_Fmt

D/A Pair D	D15	D14	D13	D12	D/A Data Source, Ordering Mode, Channels Enabled, and Packing Mode
D/A Pair C	D11	D10	D9	D8	
D/A Pair B	D7	D6	D5	D4	
D/A Pair A	D3	D2	D1	D0	
Hex Code	Bit Settings				
0x0	0	0	0	0	Source = VME/MIX, Channel Ordered, Both Chans Packed
0x1	0	0	0	1	Source = VME/MIX, Time Ordered, Both Chans Non-Packed
0x2	0	0	1	0	Reserved - Do Not Use
0x3	0	0	1	1	Source = VME/MIX, Time Ordered, Ch2: Non-Packed, Ch1: Packed
0x4	0	1	0	0	Reserved - Do Not Use
0x5	0	1	0	1	Source = VME/MIX, Time Ordered, Ch2: Packed, Ch1: Non-Packed
0x6	0	1	1	0	Reserved - Do Not Use
0x7	0	1	1	1	Source = VME/MIX, Time Ordered, Both Chans Packed
0x8	1	0	0	0	Source = Comm, Channel Ordered, Both Chans Packed
0x9	1	0	0	1	Source = Comm, Ch2 Only, Time Ordered, Non-Packed
0xA	1	0	1	0	Reserved - Do Not Use
0xB	1	0	1	1	Source = Comm, Ch2 Only, Time Ordered, Packed
0xC	1	1	0	0	Reserved - Do Not Use
0xD	1	1	0	1	Source = Comm, Ch1 Only, Time Ordered, Non-Packed
0XE	1	1	1	0	Reserved - Do Not Use
0xF	1	1	1	1	Source = Comm, Ch1 Only, Time Ordered, Packed

NOTE: If the data source for a given channel is either the VME or MIX (hex code 0 - 7), the formatting state machine must be initialized by writing 0x1 to that channel's 4-bit field before writing the desired code (e. g., to select mode 5, write 1, then 5). If the data source for a given channel is the Comm Port (hex code 8 - F), the state machine is initialized by first writing the lower 3 bits of the desired code with the upper bit cleared (0), then writing the actual code (e. g., to select mode B, write 3, then B).

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3.6 D/A Control Register Descriptions (continued)

3.6.4 D/A Data Format Register (continued)

3.6.4.1 D/A Data Source Bits - D15 (D/A Pair D), D11 (D/A Pair C), D7 (D/A Pair B), and D3 (D/A Pair A)

When one of these four bits is set to the logic '1' state, signal generation data written to the FIFOs for the associated D/A channel pair will be taken from that channel pair's front panel Comm Port connector. If your application would be better suited by writing the data over the VMEbus or the MIX bus, clear the bit(s) associated with the channel(s) to be written over the bus to the logic '0' state.

The third possible path for input data is to write the data for several or all active D/A channels to the Comm Port usually associated with D/A pair A. This is known as Single D/A Comm Port mode. The other Comm Port mode, in which each D/A pair receives data from its own Comm Port, is alternately referred to as Standard D/A Comm Port mode and Dual D/A Comm Port mode.

For Single D/A Comm Port mode, the Source bits for the channels to receive their data from the single port must be cleared to the logic '0' state (i. e., the bus-mode setting). When we discuss data formats compatible with the D/A Comm Ports in this section, we are referring to the standard or Dual mode Comm Port configuration. Single Mode D/A Comm Port data formats are discussed in Section 3.6.5.

3.6.4.2 D/A Data Packing

Data is always written to the Model 6102 as a 32-bit longword. This applies whether writing the data over VMEbus, over the MIX bus, or over the Comm Port. When a D/A pair's 4-bit field in the Data Format Register is programmed for a normal or Non-Packed format, each longword written to the 6102 that is associated with that D/A pair must contain one data sample, left justified in the 32-bit field. When a D/A pair's 4-bit field in the Data Format Register is programmed for a Packed format, each longword associated with that pair must contain two data samples. Table 3-33, at the top of the next page, contains examples of the Packed and Non-Packed data formats you must use when writing data to the 6102.

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3.6 D/A Control Register Descriptions (continued)

3.6.4 D/A Data Format Register (continued)

3.6.4.2 D/A Data Packing (continued)

Table 3-33: Model 6102 - D/A Data Ordering and Packing Formats (Bus and Dual Comm Modes)					
Channel Ordered Mode (Always Packed)					
D31 - **D16**			**D15** - **D0**		
(MSB)	Channel 2, Sample N	(LSB)	(MSB)	Channel 1, Sample N	(LSB)
Time Ordered Mode - Packed					
D31 - **D16**			**D15** - **D0**		
(MSB)	Channel X, Sample N+1	(LSB)	(MSB)	Channel X, Sample N	(LSB)
Time Ordered Mode - Non-Packed					
D31 - **D16**			**D15** - **D0**		
(MSB)	Channel X, Sample N	(LSB)	Unused - fill with zeros		

3.6.4.3 D/A Data Ordering

The data in the longwords that are written to the 6102's D/A FIFOscan be sorted or ordered by Channel or by Time. Channel ordered data must always be written in Packed format, while Time ordered data may be Packed or Non-Packed.

When the 4-bit field in the D/A Data Format Register associated with a given channel pair selects Channel ordering, and either the VMEbus or the MIX bus as the data's source, all data for both channels in the pair must be written to the Channel 1 FIFO address. In this configuration, the upper 16 bits of the longword written to the Channel 1 address is placed in the Channel 2 FIFO by the hardware. Data written to the Channel 2 FIFO address in this configuration will be ignored.

Channel ordering is the only method of writing data for both D/A channels in a given pair over the Comm Port. When writing the Channel ordered longword (either over the Comm Port or over a bus interface), the Channel 2 sample must be placed in the upper 16 bits of the longword, and Channel 1's data must be in the lower 16 bits. Channel ordered data is illustrated in the top portion of Table 3-33, above.

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3.6 D/A Control Register Descriptions (continued)

3.6.4 D/A Data Format Register (continued)

3.6.4.3 D/A Data Ordering (continued)

When Time ordering is selected by the 4-bit field in the D/A Data Format Register associated with a given channel pair, there is a major difference between how data must be written over either bus interface and how it must be written over the Comm Port. Only one channel from a given pair can be selected to receive Time ordered data from the pair's Comm Port. The Time ordered data from the selected channel can be formatted in either Packed or Non-Packed mode.

The channel that will take the data from the Comm Port is determined by the contents of the 4-bit field associated with the given D/A pair. When the field is programmed for Comm Port input in Time ordered mode **no data can be sent to the other channel in the pair** via any interface (VME, MIX, Dual-mode port or Single-mode port). This means that the non-selected channel cannot generate a signal when the Comm Port is the source of Time ordered data. Refer to Table 3-32, on page 86, for details on setting the bit fields to select combinations of channel and format.

On the other hand, when you select the VMEbus or MIX bus as the source of Time ordered data, not only can data be sent to both D/A channels, but a great deal of formatting flexibility is provided. The 4-bit field for a given D/A channel pair can be programmed such that both channels accept Packed data. Both D/A channels can also be programmed to accept Non-Packed data. Additionally, the field can be programmed such that either D/A channel accepts Packed data while the other channel's data is Non-Packed. Again, Table 3-32, on page 86, gives the details on programming the bit fields for specific input modes. The two lower sections of Table 3-33, at the top of the previous page, show where data samples must be placed in the longword in Packed and Non-Packed Time ordered modes.

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3.6 D/A Control Register Descriptions (continued)

3.6.5 Single Mode D/A Comm Port Enable Register - R/W @ DA_Sgl_Com_En

This register provides eight bits to enable the Single D/A Comm Port mode for each of the eight D/A channels on the Model 6102. In Single Comm Port mode, you can have any combination of the device's eight D/A channels receive their input data from the Comm Port that is nominally assigned to D/A pair A (on the bottom right of the front panel, labeled COMM E).

To enable this input mode for a given channel, the most significant bit in the 4-bit field associated with that channel's pair in the D/A Data Format Register must be cleared to the logic '0' state. Also, the bit in this register associated with the channel in question must be set to the logic '1' state. Table 3-34, below, tells which bit enables which channel. Before writing any new data to this register, you must clear all its bits to the logic '0' state to initialize the Single D/A Comm Port state machine. In other words, write 0x0 to this register **before** writing the desired channel-enabling code.

Table 3-34: Model 6102 - Single Mode D/A Comm Port Enable Register - R/W @ DA_Sgl_Com_En

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DA_Chan_ D2_Enable	DA_Chan_ D1_Enable	DA_Chan_ C2_Enable	DA_Chan_ C1_Enable	DA_Chan_ B2_Enable	DA_Chan_ B1_Enable	DA_Chan_ A2_Enable	DA_Chan_ A1_Enable
Bit Function	1 = Enable Channel for Single D/A Comm Port Mode 0 = Disable Channel for Single D/A Comm Port Mode							

NOTES: (1) To initialize the D/A Single Comm Port state machine, write 0x0 to this register before writing the desired value.
(2) In the Data Format Register, select VME/MIX as the source for the Single Comm Port channels.

The Packed data formatting options are not supported by the Model 6102 for the Single Comm Port mode. This means that many of the formatting options listed in Table 3-32 are not available for the D/A channels that will be receiving data from the Single D/A Comm Port. Thus, if the Single D/A Comm Port feature is enabled for both channels from a given D/A channel pair, the only valid formatting selection you can make in that pair's field in the D/A Data Format Register (see Section 3.6.4) is option 1 (Time ordered and Non-Packed for both channels). You may also select Option 3 or 5 if only one of the D/A pair's channels is driven by the Single Comm Port. If you select one of these options, the Non-Packed channel (Channel 2 for option 3, Channel 1 for option 5) must be the one that gets its data from the Single Comm Port interface.

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3.6 D/A Control Register Descriptions (continued)

3.6.5 Single Mode D/A Comm Port Enable Register (continued)

When you select the Time ordered, Non-Packed D/A data format, a Channel Identification field (in addition to the sample data) must be included with each longword sent over the port in Single D/A Comm Port mode. The three LSBs identify the specific D/A channel for which the sample is intended. Table 3-35, below, illustrates the data format and shows where you must place the Channel ID field. The ID field contents are defined in Table 3-36, also below.

Table 3-35: Model 6102 - D/A Data Format (Single Comm Mode)

Time Ordered Mode - Non-Packed		
D31 - D16	**D15 - D3**	**D2 - - - - - - D0**
(MSB) Channel X, Sample N (LSB)	Unused - fill with zeros	Channel ID*
* **NOTE:** See Table 3-36, below, for Channel ID Field definitions		

Table 3-36: Model 6102 Channel ID Field Definitions for Single D/A Comm Port Mode

Hex	D2	D1	D0	D/A Channel
0x0	0	0	0	A1
0x1	0	0	1	A2
0x2	0	1	0	B1
0x3	0	1	1	B2
0x4	1	0	0	C1
0x5	1	0	1	C2
0x6	1	1	0	D1
0x7	1	1	1	D2

NOTES: 1) The same Sample Clock source **MUST** Clock all D/A channels written in Single D/A Comm Port mode. This assures that each channel in the scan path has data available when expected.

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3.6 D/A Control Register Descriptions (continued)

3.6.5 Single Mode D/A Comm Port Enable Register (continued)

NOTES: (continued) 2) You can have some channels get their data from the Single Comm Port interface, others from a bus interface, and still others from their own Dual Comm Port interface. (The exception to remember is that if either channel in a given pair uses the Single Port interface, the other must also use the Single Port or must go unused.) This is where the configurations that have one D/A channel in a given pair Packed and the other channel Non-Packed may be handy. Remember that data written to the Single Comm Port interface must be Non-Packed. Because the Comm Port connector for D/A channel pair A is the one used for the Single D/A Comm Port interface, you cannot configure Channels A1 and A2 for Dual Comm Port operation while any other D/A channels are configured for Single Port mode.

3.6.6 D/A FIFO Reset Register - R/W @ DA_FIFO_Rst

The D/A FIFO Reset Register contains one bit to clear each D/A channel's FIFO of all data. Clearing a bit to the logic '0' state resets the associated D/A channel's FIFO. The FIFO will be held in the reset state (i. e., no data can be accepted by that FIFO) for as long as the associated bit remains at a logic '0'. Thus, the D/A FIFO reset function should be implemented as a toggle, i. e., the appropriate bit should be cleared to the logic '0' state to reset the FIFO, then set back to logic '1' to release the FIFO for data collection. Table 3-37, below, shows which bit is used to reset which D/A channel's FIFO.

Table 3-37: Model 6102 - D/A FIFO Reset Register - R/W @ DA_FIFO_Rst

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DA_FIFO_ D2_Reset	DA_FIFO_ D1_Reset	DA_FIFO_ C2_Reset	DA_FIFO_ C1_Reset	DA_FIFO_ B2_Reset	DA_FIFO_ B1_Reset	DA_FIFO_ A2_Reset	DA_FIFO_ A1_Reset
Bit Function	1 = Release FIFO and enable data collection 0 = Reset FIFO and disable data collection							
NOTE: Toggle the appropriate bit(s) to implement the reset function.								

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3.6 D/A Control Register Descriptions (continued)

3.6.7 D/A Clock Select and Sample Counter Register - R/W @ DA_CkSl_SCt

The Model 6102 is equipped with four separate Sample Clock Generation circuits, each of which may be driven by the on-board, 20 MHz crystal oscillator or by a Reference Clock Input signal applied at the front panel Analog Input connector. These four Sample Clock Generator circuits are essentially simple frequency dividers, and are referred to as Clk1, Clk2, Clk3 and Clk4. Section 3.5.1 discusses these Sample Clock Rate Dividers. The A/D Clock Select and Sample Counter Register (see Section 3.5.8) provides four bits that select which clock signal is applied to which Rate Divider (see Table 3-26).

NOTE: The A/D Clock Select and Sample Counter Register is also used to select the internal crystal oscillator or an externally applied signal as the reference source for the Sample Clock Rate Dividers, and that the default selection is the extearnal reference.

The front panel Analog Output connector provides yet another input for a Clock signal. Only the D/A Converters can be clocked by this signal, and its frequency cannot be divided. The upper eight bits of the D/A Clock Select and Sample Counter Register allow you to select either this external Clock signal or one of the four on-card frequency dividers as the Sample Clock source for each D/A Converter pair on the 6102. This register's lower eight bits hold the initial value for the D/A Sample Counter, which you can use to interrupt the VMEbus or the MIX bus after a programmed number of samples have been converted. Table 3-38, below, shows the bit arrangement within the D/A Clock Select and Sample Counter Register. The subsections following the table give detailed descriptions of the functions of those bits.

Table 3-38: Model 6102 - D/A Clock Select and Sample Counter Register

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	D/As_D_ Clk_Sel_1	D/As_D_ Clk_Sel_0	D/As_C_ Clk_Sel_1	D/As_C_ Clk_Sel_0	D/As_B_ Clk_Sel_1	D/As_B_ Clk_Sel_0	D/As_A_ Clk_Sel_1	D/As_A_ Clk_Sel_0
Bit Function	1,1 = Ext Clk 1,0 = Clk4	0,1 = Clk3 0,0 = Clk1	1,1 = Ext Clk 1,0 = Clk4	0,1 = Clk3 0,0 = Clk1	1,1 = Ext Clk 1,0 = Clk4	0,1 = Clk2 0,0 = Clk1	1,1 = Ext Clk 1,0 = Clk4	0,1 = Clk2 0,0 = Clk1
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2'**	**D1**	**D0**
Bit Name	D/A Sample Counter Preload Field							
Bit Function	Initial and Modulus Value for D/A Sample Counter							

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3.6 D/A Control Register Descriptions (continued)

3.6.7 D/A Clock Select and Sample Counter Register (continued)

3.6.7.1 D/A Clock Source Select Bits - D15 & D14 (D/A pair D), D13 & D12 (D/A pair C), D11 & D10 (D/A pair B), and D9 & D8 (D/A pair A)

There are four D/A converter pairs on the Model 6102, and there are five choices for their Sample Clock sources. The on-card Sample Clock sources are referred to as Clk1, Clk2, Clk3 and Clk4. The fifth source is the signal applied between pins 3 and 4 of the front panel's Analog Output connector. If the external signal is selected, that signal's frequency will be the Sample Rate (i. e., the external signal's frequency cannot be divided).

Two bits are provided for selecting the Sample Clock source for each pair of D/A converters. This means that you may select from among four of the five sources for each D/A pair. D/A pairs A and B may be Clocked by Clk1, Clk2, Clk4 or the external D/A Clock. D/A pairs C and D can select from Clk1, Clk3, Clk4 or the external D/A Clock. Table 3-38, on the previous page, tells which two-bit bit field you use to select the source for which D/A pair, and how to set the bits to select a given source.

3.6.7.2 D/A Sample Counter Pre-Load Field - Bits D7 through D0

You can use the D/A sample counter on the Model 6102 to generate a VMEbus or MIX bus interrupt upon the conversion of every Nth sample ($2 < N < 256$). You enable the interrupt by setting the D3 bit in the Interrupt Mask Register for D/A channel pairs A and B, at address DA_Mask_AB, to the logic '1' state. To generate an interrupt when the N^{th} sample is taken, program the value (N-1) into the eight LSBs at address DA_CkSl_SCt.

NOTE: The D/A Sample Counter Pre-Load Field cannot be programmed to generate an interrupt after the conversion of only one sample. In situations where you want to write and convert one sample and then Re-Arm the Trigger, we offer the following alternative suggestion. Program the channel(s) to accept an External Clock (see Section 3.6.7.1, above) and fire the channel's Software Trigger bit in the D/A Trigger Control Register at address DA_Trig_Ctrl (see Section 3.6.1.3). Then, pulse the D/A Clock Input instead of the D/A Trigger Input. The channel's D/A FIFO Empty Interrupt can then be used instead of the Sample Counter interrupt to start the routine to write the next sample.

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3.6 D/A Control Register Descriptions (continued)

3.6.7 D/A Clock Select and Sample Counter Register (continued)

3.6.7.2 D/A Sample Counter Pre-Load Field (continued)

The sample counter is an 8-bit modulo-down counter. It counts from a preset value (the modulus) down to zero, then returns to the initial value and starts counting down again. If you enable the counter's interrupt, it will occur whenever the counter reaches its zero state. Because the clock pulse that brings the counter to the zero count will also cause the conversion of a sample, the value written to this field must be one count less than the number of samples to be converted before the interrupt is generated.

If you select different sample rates for the four D/A pairs, the D/A Sample Counter will count the samples converted by D/A pair A.

3.6.8 D/A Trigger Re-Arm Register - R/W @ DA_Arm_Ctrl

This register contains only four active bits, one for each D/A channel pair. To enable automatic Re-Arming of a given D/A channel pair's Trigger circuit when the number of samples programmed into the D/A Sample Counter (see Section 3.6.7.2) have been converted, set the associated bit to the logic '1' state. Clearing the associated bit to the logic '0' state disables the automatic Re-Arm function. The upper four bits of this register are reserved, and should always be written as '0'.

If the automatic Re-Arm function is enabled, signal generation will stop after the programmed number of samples have been converted. The device will wait for the next Trigger to resume the Sampling process. If the automatic Re-Arming function is disabled, signal generation will continue uninterrupted after the programmed number of samples has been converted.

Table 3-39, below, tells which bit in this register controls the automatic Re-Arm function for which D/A channel pair in the Model 6102.

Table 3-39: Model 6102 - D/A Trigger Re-Arm Register - R/W @ DA_Arm_Ctrl

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved				D/A_pair_D_Re-Arm	D/A_pair_C_Re-Arm	D/A_pair_B_Re-Arm	D/A_pair_A_Re-Arm
Bit Function	Always Write '0'				1 = Re-Arm D/A Trigger when D/A Sample Counter reaches zero. 0 = Continue sampling when D/A Sample Counter reaches zero.			

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3.7 Reading A/D Data From the Model 6102

There are several ways to read data acquired by the 6102's A/D converters. The interface over which the data is read may be the VMEbus, the MIX bus, or the Comm Port interface. When reading over the VMEbus, the data may be accessed in A16 space, A24 space, or A32 space. The VME readout interface is treated as a FIFO in all three memory regions. Block mode transfers can be used in A32 and/or A24 space if the appropriate AM code is used (0x0F or 0x0B in A32 space, 0x3F or 0x3B in A24 space - see Table 3-1). Block mode transfers are also suppported over the MIX bus. When reading from the Comm Port interface, each A/D pair can send data to its own port. Alternatively, any or all active channels can direct their data to a single port. Regardless of the interface used, the data can be formatted in Packed or Non-Packed mode, and can be ordered by Time or by Channel (note that Single A/D Comm Port mode does not support data packing). Combinations of these features are also permissible. Section 3.5.5, beginning on page 65 and Section 3.5.6, beginning on page 69, provide further information about programming the 6102 to select the destination and format of the data collected in the A/D FIFOs. The tables from those sections are reproduced here. Table 3-40, below, tells how to program the bit fields in the A/D Data Format Register to select a particular destination and format for a given A/D pair's data. Table 3-41, on the next page, illustrates the data formats used for readout over the VMEbus, the MIX bus, and the dual-A/D Comm Port interfaces. Table 3-42 and Table 3-43, also on the next page, show the data format used for the Single A/D Comm Port interface, and define the Channel ID field used in that mode.

Table 3-40: Model 6102 - A/D Data Format Register - R/W @ AD_Data_Fmt

A/D Pair D	D15	D14	D13	D12	A/D Data Destination, Ordering Mode, Channels Enabled, and Packing Mode
A/D Pair C	D11	D10	D9	D8	
A/D Pair B	D7	D6	D5	D4	
A/D Pair A	D3	D2	D1	D0	
Hex Code	Bit Settings				
0x0	0	0	0	0	Dest = VME/MIX, Channel Ordered, Both Chans Packed
0x1	0	0	0	1	Dest = VME/MIX, Time Ordered, Both Chans Non-Packed
0x2	0	0	1	0	Reserved - Do Not Use
0x3	0	0	1	1	Dest = VME/MIX, Time Ordered, Ch2: Non-Packed, Ch1: Packed
0x4	0	1	0	0	Reserved - Do Not Use
0x5	0	1	0	1	Dest = VME/MIX, Time Ordered, Ch2: Packed, Ch1: Non-Packed
0x6	0	1	1	0	Reserved - Do Not Use
0x7	0	1	1	1	Dest = VME/MIX, Time Ordered, Both Chans Packed
0x8	1	0	0	0	Dest = Comm, Channel Ordered, Both Chans Packed
0x9	1	0	0	1	Dest = Comm, Ch2 Only, Time Ordered, Non-Packed
0xA	1	0	1	0	Reserved - Do Not Use
0xB	1	0	1	1	Dest = Comm, Ch2 Only, Time Ordered, Packed
0xC	1	1	0	0	Reserved - Do Not Use
0xD	1	1	0	1	Dest = Comm, Ch1 Only, Time Ordered, Non-Packed
0XE	1	1	1	0	Reserved - Do Not Use
0xF	1	1	1	1	Dest = Comm, Ch1 Only, Time Ordered, Packed

NOTE: Write 0x1 to a given 4-bit field before writing the desired hex code, to initialize the data-formatting state machine for that channel pair.

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3.7 Reading Data From the Model 6102 (continued)

Table 3-41: Model 6102 - A/D Data Ordering and Packing Formats (Bus and Dual Comm Modes)					
Channel Ordered Mode (Always Packed)					
D31 - D16			**D15 - D0**		
(MSB)	Channel 2, Sample N	(LSB)	(MSB)	Channel 1, Sample N	(LSB)
Time Ordered Mode - Packed					
D31 - D16			**D15 - D0**		
(MSB)	Channel X, Sample N+1	(LSB)	(MSB)	Channel X, Sample N	(LSB)
Time Ordered Mode - Non-Packed					
D31 - D16			**D15 - D0**		
(MSB)	Channel X, Sample N	(LSB)	Indeterminate		

Table 3-42: Model 6102 - A/D Data Format (Single Comm Mode)					
Time Ordered Mode - Non-Packed					
D31 - D16			**D15 - D3**	**D2 - - - - - - D0**	
(MSB)	Channel X, Sample N	(LSB)	Indeterminate	Channel ID*	
* **NOTE:** See Table 3-24, below, for Channel ID Field definitions					

Table 3-43: Model 6102 Channel ID Field Definitions for Single A/D Comm Port Mode

Hex	D2	D1	D0	A/D Channel
0x0	0	0	0	A1
0x1	0	0	1	A2
0x2	0	1	0	B1
0x3	0	1	1	B2
0x4	1	0	0	C1
0x5	1	0	1	C2
0x6	1	1	0	D1
0x7	1	1	1	D2

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3.7 Reading Data From the Model 6102 (continued)

Data samples are written to the FIFOs by the A/D converters, left-justified, in 16-bit, 2's-complement format. Negative input voltages are indicated by data samples with a '1' in the MSB. Table 3-44, below, shows the 32-bit hex-equivalent value of the data read from the FIFO indicating various analog input voltages near positive full-scale, near zero, and near negative full-scale. The listings in the table assume that data is not Packed. Note that the zeros listed in the least significant bits are actually indeterminate for Non-Packed data (see Table 3-21). Packed data would contain an additional 16-bit sample, left justified in the lower 16-bit field.

Table 3-44: Model 6106 - A/D FIFO Data for Various Input Signal Conditions

Input	A/D FIFO Data	Input	A/D FIFO Data	Input	A/D FIFO Data
+Full Scale	0x7FFF 0000	3 LSBs above Zero	0x0003 0000	6 LSBs above -Full Scale	0x8006 0000
1 LSB below +Full Scale	0x7FFE 0000	2 LSBs above Zero	0x0002 0000	5 LSBs above -Full Scale	0x8005 0000
2 LSBs below +Full Scale	0x7FFD 0000	1 LSB above Zero	0x0001 0000	4 LSBs above -Full Scale	0x8004 0000
3 LSBs below +Full Scale	0x7FFC 0000	Zero	0x0000 0000	3 LSBs above -Full Scale	0x8003 0000
4 LSBs below +Full Scale	0x7FFB 0000	1 LSB below Zero	0xFFFF 0000	2 LSBs above -Full Scale	0x8002 0000
5 LSBs below +Full Scale	0x7FFA 0000	2 LSBs below Zero	0xFFFE 0000	1 LSBs above -Full Scale	0x8001 0000
6 LSBs below +Full Scale	0x7FF9 0000	3 LSBs below Zero	0xFFFD 0000	-Full Scale	0x8000 0000

NOTE: The listings above assume Non-Packed data, and the LSBs are actually indeterminate rather than zero. Packed data would have another 16-bit sample left-justified in the lower 16-bit field.

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3.8 Writing D/A Data to the Model 6102

There are several ways to write the data used by the 6102's D/A converters to generate analog output signals. The three interfaces over which the data may be written are the VMEbus, the MIX bus, and the Comm Port interface. When writing over the VMEbus, the FIFOs may be accessed in A16 space, A24 space, or A32 space. Block mode transfers may be used in A32 and/or A24 space if the appropriate AM code is used (0x0F or 0x0B in A32 space, 0x3F or 0x3B in A24 space - see Table 3-1). Block mode transfers are also suppported over the MIX bus. When writing over the Comm Port interface, each D/A pair can take data from its own port. Alternatively, any or all active channels can get their data from a single port. The data sent to the FIFOs can be formatted in Packed or Non-Packed mode, and can be ordered by Time or by Channel (note that Single D/A Comm Port mode does not support data packing). Combinations of these features are also permissible. Section 3.6.4 and Section 3.6.5 provide further information about programming the 6102 to select the source and format of the data written to the D/A FIFOs. The tables from those sections are reproduced here. Table 3-45, below, tells how to program the bit fields in the D/A Data Format Register to select a particular source and format for a given D/A pair's data. Table 3-46, on the next page, illustrates the data formats used when writing data over the VMEbus, the MIX bus, and the Dual D/A Comm Port interfaces. Table 3-47 and Table 3-48, also on the next page, show the data format used for the Single D/A Comm Port interface, and define the Channel ID field used in that mode.

Table 3-45: Model 6102 - D/A Data Format Register - R/W @ DA_Data_Fmt

D/A Pair D	D15	D14	D13	D12	D/A Data Source, Ordering Mode, Channels Enabled, and Packing Mode
D/A Pair C	D11	D10	D9	D8	
D/A Pair B	D7	D6	D5	D4	
D/A Pair A	D3	D2	D1	D0	
Hex Code	Bit Settings				
0x0	0	0	0	0	Source = VME/MIX, Channel Ordered, Both Chans Packed
0x1	0	0	0	1	Source = VME/MIX, Time Ordered, Both Chans Non-Packed
0x2	0	0	1	0	Reserved - Do Not Use
0x3	0	0	1	1	Source = VME/MIX, Time Ordered, Ch2: Non-Packed, Ch1: Packed
0x4	0	1	0	0	Reserved - Do Not Use
0x5	0	1	0	1	Source = VME/MIX, Time Ordered, Ch2: Packed, Ch1: Non-Packed
0x6	0	1	1	0	Reserved - Do Not Use
0x7	0	1	1	1	Source = VME/MIX, Time Ordered, Both Chans Packed
0x8	1	0	0	0	Source = Comm, Channel Ordered, Both Chans Packed
0x9	1	0	0	1	Source = Comm, Ch2 Only, Time Ordered, Non-Packed
0xA	1	0	1	0	Reserved - Do Not Use
0xB	1	0	1	1	Source = Comm, Ch2 Only, Time Ordered, Packed
0xC	1	1	0	0	Reserved - Do Not Use
0xD	1	1	0	1	Source = Comm, Ch1 Only, Time Ordered, Non-Packed
0XE	1	1	1	0	Reserved - Do Not Use
0xF	1	1	1	1	Source = Comm, Ch1 Only, Time Ordered, Packed

To initialize the data-formatting state machine for a given channel pair: If data source is VME or MIX, write 0x1 to a given 4-bit field befor writing the desired hex code; if data source is Comm Port, write desired code with upper three bits cleared before writing the desired hex code.

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3.8 Writing Data to the Model 6102 (continued)

Table 3-46: Model 6102 - D/A Data Ordering and Packing Formats (Bus and Dual Comm Modes)					
Channel Ordered Mode (Always Packed)					
D31 - D16			**D15 - D0**		
(MSB)	Channel 2, Sample N	(LSB)	(MSB)	Channel 1, Sample N	(LSB)
Time Ordered Mode - Packed					
D31 - D16			**D15 - D0**		
(MSB)	Channel X, Sample N+1	(LSB)	(MSB)	Channel X, Sample N	(LSB)
Time Ordered Mode - Non-Packed					
D31 - D16			**D15 - D0**		
(MSB)	Channel X, Sample N	(LSB)	Unused - fill with zeros		

Table 3-47: Model 6102 - D/A Data Format (Single Comm Mode)				
Time Ordered Mode - Non-Packed				
D31 - D16			**D15 - D3**	**D2 - - - - - - D0**
(MSB)	Channel X, Sample N	(LSB)	Unused - fill with zeros	Channel ID*
* **NOTE:** See Table 3-36, below, for Channel ID Field definitions				

Table 3-48: Model 6102 Channel ID Field Definitions for Single D/A Comm Port Mode

Hex	D2	D1	D0	D/A Channel
0x0	0	0	0	A1
0x1	0	0	1	A2
0x2	0	1	0	B1
0x3	0	1	1	B2
0x4	1	0	0	C1
0x5	1	0	1	C2
0x6	1	1	0	D1
0x7	1	1	1	D2

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3.8 Writing Data to the Model 6102 (continued)

Data samples for the D/A converters must be written to their respective FIFOs, left-justified, in 16-bit, 2's-complement format. Negative input voltages are indicated by data written with a '1' in the MSB. Table 3-49, below, shows the 32-bit hex-equivalent value of the data you must write to the FIFO to obtain various analog output voltages near positive full-scale, near zero, and near negative full-scale. The listings in the table assume that data is not Packed. Note that the zeros listed in the least significant bits are actually unused for Non-Packed data (see Table 3-33). Packed data would contain an additional 16-bit sample, left justified in the lower 16-bit field.

Table 3-49: Model 6106 - D/A FIFO Data for Various Analog Output Voltages

Output	D/A FIFO Data	Output	D/A FIFO Data	Output	D/A FIFO Data
+Full Scale	0x7FFF 0000	3 LSBs above Zero	0x0003 0000	6 LSBs above -Full Scale	0x8006 0000
1 LSB below +Full Scale	0x7FFE 0000	2 LSBs above Zero	0x0002 0000	5 LSBs above -Full Scale	0x8005 0000
2 LSBs below +Full Scale	0x7FFD 0000	1 LSB above Zero	0x0001 0000	4 LSBs above -Full Scale	0x8004 0000
3 LSBs below +Full Scale	0x7FFC 0000	Zero	0x0000 0000	3 LSBs above -Full Scale	0x8003 0000
4 LSBs below +Full Scale	0x7FFB 0000	1 LSB below Zero	0xFFFF 0000	2 LSBs above -Full Scale	0x8002 0000
5 LSBs below +Full Scale	0x7FFA 0000	2 LSBs below Zero	0xFFFE 0000	1 LSBs above -Full Scale	0x8001 0000
6 LSBs below +Full Scale	0x7FF9 0000	3 LSBs below Zero	0xFFFD 0000	-Full Scale	0x8000 0000

NOTE: The listings above assume Non-Packed data, and the LSBs are actually unused, rather than zero. Packed data would have another 16-bit sample left-justified in the lower 16-bit field.

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Appendix A: Programming Examples

A.1 Introduction

This chapter contains four 'C' language source files. The first two and the last are header files. ad6102.h defines register addresses and contents for the A/D section (see Section A.2, below), and da6102.h does the same for the D/A section (see Section A.3, beginning on Page A-4). To select the type of MIX baseboard you are using and the MIX stack position of the Model 6102, initialize constants in the file mod.h (see Section A.5, beginning on Page A-20) prior to compiling. This file (**mod.h**) initializes several symbolic constants used by the other files included here, and is intended as a general purpose header file for use with all Pentek MIX modules. These three header files are **#include**d p6102.c.

The file p6102.c (see Section A.4, beginning on Page A-4) uses the VMEbusbmaster and Comm Port controller capabilities of a Pentek Model 4284 TMS320C40 processor board to initialize, control, and take data from a Model 6102. You can direct data to the VME-bus interface, the MIX bus interface, or the Comm Ports. Set constants prior to compiling to allow the Comm Port interface to operate in Single or Dual port mode, to select Time or Channel ordering, and to turn Packed data mode on or off.

A.2 ad6102.h

```
#define A16          0xff00                        /* A16 base address */
#define BASE         A16/4
#define VMEBUS       (0xb0000000 | BASE)    /*  VMEbus access address */
#define FIFO_SIZE    1024          /* 1024 is standard, 16384 optional */
#define NUM_SAMPLES  2048 /* number of samples for processing algorithm */
#define FREQ         0x01312D00L          /* 20 MHz for internal clock */
#define SAMPLFREQ    0x000061A8L           /* 100 kHz for this example */
#define ENABLE_A24   0x10                            /* A24 enable bit */
#define VME          1
#define MIX          2
#define COMM         3

/* Slave Address Map */
#define AD_FIFO_A1      0x0
#define AD_FIFO_A2      0x1
#define AD_FIFO_B1      0x2
#define AD_FIFO_B2      0x3
#define AD_FIFO_C1      0x4
#define AD_FIFO_C2      0x5
#define AD_FIFO_D1      0x6
#define AD_FIFO_D2      0x7

#define V_CTRL          0x08
#define V_ADDR          0x09
#define V_INT_MASK      0x0A
```


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A.2 **ad6102.h** (continued)

```
#define CLK1_DIV              0x10
#define CLK2_DIV              0x11
#define CLK3_DIV              0x12
#define CLK4_DIV              0x13

#define AD_TRIG_CTRL          0x14
#define AD_STAT_AB            0x15
#define AD_STAT_CD            0x16
#define AD_MASK_AB            0x17
#define AD_MASK_CD            0x18
#define AD_DATA_FMT           0x19
#define AD_SGL_COM_EN         0x1A
#define AD_FIFO_RST           0x1B
#define AD_CKSL_SCT           0x1C
#define CLK_DIV_SYNC          0x1D
#define AD_ARM_CTRL           0x1E

#define MX_CTRL               0x28
#define MX_INT_CLR            0x29

/* Interrupts on the 4284 */
#define INTR_STAT_CNTRL_REG   0x10000002L
#define INTR_ROUT_REG         0x10000003L

/* bits definitions for VME Interrupts */
#define  VME_IRQ_A            0x00000001L
#define  VME_IRQ_B            0x00000002L
#define  VME_IRQ_C            0x00000004L

/* VMEbus IACK level Codes 1-7 */
#define IACK_LEV1             0xa0000001
#define IACK_LEV2             0xa0000002
#define IACK_LEV3             0xa0000003
#define IACK_LEV4             0xa0000004
#define IACK_LEV5             0xa0000005
#define IACK_LEV6             0xa0000006
#define IACK_LEV7             0xa0000007

/* Clock Select bits for Sample Clock Register */
#define INTERNAL_SEL          0x00000f00
#define EXTERNAL_SEL          0x00000000
                           /* the above values are for all 4 Clk_Refs */
#define CLK1_REF              0x00000100
#define CLK2_REF              0x00000200
#define CLK3_REF              0x00000300
#define CLK4_REF              0x00000400

#define INT_TRIGGER           0xfff0
#define EXT_TRIGGER           0xff00
```


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A.2 **ad6102.h** (continued)

```
/* DIGITAL COUNTER BIT */
#define DIG_TEST_RAMP          0x08

/* bit definitions for the Status Register and Interrupt Masks -
                                                    for A/Ds and D/As */
#define A1_FIFO_FULL           0x00000001
#define A1_FIFO_EMPTY          0x00000002
#define A1_FIFO_HALF_FULL      0x00000004
#define SAMPLE_CTR_INTERRUPT   0x00000008
#define A2_FIFO_FULL           0x00000010
#define A2_FIFO_EMPTY          0x00000020
#define A2_FIFO_HALF_FULL      0x00000040
#define TRIGGER_STATUS_A       0x00000080

#define B1_FIFO_FULL           0x00000100
#define B1_FIFO_EMPTY          0x00000200
#define B1_FIFO_HALF_FULL      0x00000400
#define B2_FIFO_FULL           0x00001000
#define B2_FIFO_EMPTY          0x00002000
#define B2_FIFO_HALF_FULL      0x00004000
#define TRIGGER_STATUS_B       0x00008000

#define C1_FIFO_FULL           0x00000001
#define C1_FIFO_EMPTY          0x00000002
#define C1_FIFO_HALF_FULL      0x00000004
#define C2_FIFO_FULL           0x00000010
#define C2_FIFO_EMPTY          0x00000020
#define C2_FIFO_HALF_FULL      0x00000040
#define TRIGGER_STATUS_C       0x00000080

#define D1_FIFO_FULL           0x00000100
#define D1_FIFO_EMPTY          0x00000200
#define D1_FIFO_HALF_FULL      0x00000400
#define D2_FIFO_FULL           0x00001000
#define D2_FIFO_EMPTY          0x00002000
#define D2_FIFO_HALF_FULL      0x00004000
#define TRIGGER_STATUS_D       0x00008000

/* VMEbus IRQ Levels in the VMEbus Control Register  */
#define IRQ_LEVEL_1            0x100
#define IRQ_LEVEL_2            0x200
#define IRQ_LEVEL_3            0x300
#define IRQ_LEVEL_4            0x400
#define IRQ_LEVEL_5            0x500
#define IRQ_LEVEL_6            0x600
#define IRQ_LEVEL_7            0x700

/* channel pair used */
#define PAIR_A                 0
#define PAIR_B                 1
#define PAIR_C                 2
#define PAIR_D                 3
```


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A.3 da6102.h

```
/* Slave Address Map */
#define DA_FIFO_A1      0x20
#define DA_FIFO_A2      0x21
#define DA_FIFO_B1      0x22
#define DA_FIFO_B2      0x23
#define DA_FIFO_C1      0x24
#define DA_FIFO_C2      0x25
#define DA_FIFO_D1      0x26
#define DA_FIFO_D2      0x27

#define DA_TRIG_CTRL    0x34
#define DA_STAT_AB      0x35
#define DA_STAT_CD      0x36
#define DA_MASK_AB      0x37
#define DA_MASK_CD      0x38
#define DA_DATA_FMT     0x39
#define DA_SGL_COM_EN   0x3A
#define DA_FIFO_RST     0x3B
#define DA_CKSL_SCT     0x3C
#define DA_ARM_CTRL     0x3D
```

A.4 p6102.c

```
#include                <intpt40.h>
#include                "ad6102.h"
#include                "da6102.h"
#include                "mod.h"
#include                <math.h>

/* define the type of  Access */
#define INTERRUPTS      1
#define DA_ENABLE       0
#define IOTEST          0         /* quick I/O test, use w/o interrupts */
#define RAMP_GENERATOR  0

#define                 MIXACC
#if MIXACC
   #define MODE         MOD
#else
   #define MODE         VMEBUS
#endif

/* active channel definition */
#define CHAN_A1         1
#define CHAN_A2         2
#define CHAN_B1         3
#define CHAN_B2         4
#define CHAN_C1         5
#define CHAN_C2         6
#define CHAN_D1         7
#define CHAN_D2         8
```


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A.4 **p6102.c** (continued)

```
#define ACTIVE_CHAN     CHAN_A1

/* Data Format Register bit definitions */
#define VME_BOTH_PACK         0x0
#define VME_TIME_BOTH_NONPACK 0x1
#define VME_TIME_CH1_PACK     0x3
#define VME_TIME_CH2_PACK     0x5
#define VME_TIME_BOTH_PACK    0x7
#define COMM_BOTH_PACK        0x8
#define COMM_TIME_CH2_NONPACK 0x9
#define COMM_TIME_CH2_PACK    0xB
#define COMM_TIME_CH1_NONPACK 0xD
#define COMM_TIME_CH1_PACK    0xF
#define FORMAT                VME_TIME_BOTH_NONPACK
                             /* VME_ prefix also used for MIX Access) */

#define CLOCK              INTERNAL_SEL
#define TRIGGER            INT_TRIGGER
#define SINGLE_MODE_COMM   0
#define PRELOAD            1       /* Sample Counter Interrupt switch */
#define PRLVAL             8

#define COMM_PORTIN        3  /* c40 Comm Port number used by the 4284 */
#define COMM_PORTOUT       2

#define PROCESS_DATA       0
#define DISPLAY_DATA       0
       /* use the display only if you have the PC based video program */

unsigned int count,pack,access_mode,com_portin,com_portout,data_format;
unsigned int active_chan,chan_ordered,low_word,clock_select;

/* 4284 pointers */
volatile unsigned int *timer0_address;
volatile unsigned int *timer1_address;
unsigned int *c40_control, *c40_reg, *vme_reg;

/* pointers for interrupt routine */
unsigned int *IntrStat,*IntRout,*intr_mask,*val_ivpt;
unsigned int active_pair,status_mask,A16_base;
unsigned int divider,flag;
long *Buffer,temp;             /* pointer at 80002000 to look at data */

/* 6102 A/D registers */
unsigned int *VmeControl,*VmeAddress,*VmeInterrupts,*MixControlReg;
unsigned int *Sample1Div,*Sample2Div,*Sample3Div,*Sample4Div;
unsigned int *TriggerControl,*StatusRegAB,*StatusRegCD;
unsigned int *StatusReg,*InterruptMask,*MixInterruptClear;
unsigned int *InterruptMaskAB,*InterruptMaskCD,*DataFormat,*SingleMode;
unsigned int *FifoReset,*ClockSelect,*ClockResync,*Ad_ReArm;
volatile unsigned int *FifoA1,*FifoA2,*FifoB1,*FifoB2;
volatile unsigned int *FifoC1,*FifoC2,*FifoD1,*FifoD2,*Fifo;
```


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A.4 **p6102.c** (continued)

```
/* 6102 D/A registers */
unsigned int *DaTriggerControl,*DaStatusRegAB,*DaStatusRegCD;
unsigned int *DaStatusReg,*DaInterruptMask;
unsigned int *DaInterruptMaskAB,*DaInterruptMaskCD,*DaDataFormat;
unsigned int *DaSingleMode,*DaFifoReset,*DaClockSelect,*DaTrigger_ReArm;

volatile unsigned int *FifoOutA1,*FifoOutA2,*FifoOutB1,*FifoOutB2;
volatile unsigned int *FifoOutC1,*FifoOutC2,*FifoOutD1,*FifoOutD2;
volatile unsigned int *FifoOut

int samples[2048];
unsigned int test;

/* interrupt handlers and pointers */
unsigned int *int01_vector;
void c_int01();
void InitialInterrupt();

/* Data proccessing functions */
void Get_Data();
extern double data_buf[];                    /* defined in fft_c4.asm */

main()
{
   int i,k;
   asm("   LDI    0,ST");               /* Disable global interrupts */
   InitMode();
   InitPtrs();
   Init6102();                                  /* program the 6102 */

   #if INTERRUPTS
      *InterruptMaskAB = 0x0;
      *InterruptMaskCD = 0x0;
      #if MIXACC
         *MixControlReg = 0x1;
      #else
         *VmeInterrupts = 0x1;
      #endif
      #if DA_ENABLE
         *DaInterruptMaskAB = 0x0;
         *DaInterruptMaskCD = 0x0;
      #endif
   #endif

   for(i=0; i<FIFO_SIZE; i++)
      *Buffer++ = 0;                          /* initialize buffer */
   Buffer = Buffer - FIFO_SIZE;
```


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A.4 **p6102.c** (continued)

```
   #if INTERRUPTS
      IntrStat = (unsigned int*) INTR_STAT_CNTRL_REG;
      *(unsigned int *) INTR_ROUT_REG = *(unsigned int *) INTR_ROUT_REG
               | VME_IRQ_A | MIX_IRQ_0; /* VME Interrupt 4, MIX_int_0 */
      InitialInterrupts();
      *TriggerControl = TRIGGER;                    /* trigger point */
      #if DA_ENABLE
         *DaTriggerControl = TRIGGER;
      #endif
      while(1);
   #else
      *TriggerControl = TRIGGER;
      #if DA_ENABLE
         *DaTriggerControl = TRIGGER;
      #endif
      while(1)
      {
         for(i=0;i<32;i++)
            *FifoOut = *Buffer;
         Get_Data();
         #if PROCESS_DATA                      /* Perform Complex FFT */
            ProcessData(samples,data_buf,1024);
         #endif
         #if DISPLAY_DATA                   /* Scale Data for Display */
            DisplayData(data_buf,1024);
         #endif
         *FifoReset = 0x0000;                     /* reset all FIFOs */
         *FifoReset = 0x00ff;                   /* release all FIFOs */
      }
   #endif
}

InitPtrs()
{
   /* 4284 registers */
   c40_control       = (unsigned int *)0x00100000u;
   c40_reg           = (unsigned int *)0x10000000u;
   vme_reg           = (unsigned int *)0x90000000u;
   timer0_address    = (unsigned int *)0x100020u;
   timer1_address    = (unsigned int *)0x100030u;
   Buffer            = (long *)0x80002000u;

   /* 6102 registers */
   VmeControl        = (unsigned int *) (V_CTRL | VMEBUS);
   VmeAddress        = (unsigned int *) (V_ADDR | VMEBUS);
   VmeInterrupts     = (unsigned int *) (V_INT_MASK | VMEBUS);
   MixControlReg     = (unsigned int *) (MX_CTRL | MOD);
   MixInterruptClear = (unsigned int *) (MX_INT_CLR | MOD);
   Sample1Div        = (unsigned int *) (CLK1_DIV | MODE);
   Sample2Div        = (unsigned int *) (CLK2_DIV | MODE);
   Sample3Div        = (unsigned int *) (CLK3_DIV | MODE);
   Sample4Div        = (unsigned int *) (CLK4_DIV | MODE);
```


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A.4 **p6102.c** (continued)

```
   InitAdPtrs();
   InitDaPtrs();
   #if PROCESS_DATA/* Initialize tables for fft processing */
      InitFFTTables(FIFO_SIZE);
   #endif
}

Init6102()
{
   int i;
   Init4284();
   A16_base = BASE;

   switch(active_chan)
   {
      case CHAN_A1:
         Fifo = FifoA1;
         FifoOut = FifoOutA1;
         status_mask = A1_FIFO_HALF_FULL;
         active_pair = PAIR_A;
      break;

      case CHAN_A2:
         if(chan_ordered == 1)
         {
            Fifo = FifoA1;
            FifoOut = FifoOutA1;
         }
         else
         {
            Fifo = FifoA2;
            FifoOut = FifoOutA2;
         }
         status_mask = A2_FIFO_HALF_FULL;
         active_pair = PAIR_A;
      break;

      case CHAN_B1:
         Fifo = FifoB1;
         FifoOut = FifoOutB1;
         active_pair = PAIR_B;
         status_mask = B1_FIFO_HALF_FULL;
      break;
```


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A.4 **p6102.c** (continued)

```
        case CHAN_B2:
           if(chan_ordered == 1)
           {
              Fifo = FifoB1;
              FifoOut = FifoOutB1;
           }
           else
           {
              Fifo = FifoB2;
              FifoOut = FifoOutB2;
           }
           active_pair = PAIR_B;
           status_mask = B2_FIFO_HALF_FULL;
        break;

     case CHAN_C1:
           Fifo = FifoC1;
           FifoOut = FifoOutC1;
           active_pair = PAIR_C;
           status_mask = C1_FIFO_HALF_FULL;
        break;

        case CHAN_C2:
           if(chan_ordered == 1)
           {
              Fifo = FifoC1;
              FifoOut = FifoOutC1;
           }
           else
           {
              Fifo = FifoC2;
              FifoOut = FifoOutC2;
           }
           active_pair = PAIR_C;
           status_mask = C2_FIFO_HALF_FULL;
        break;

        case CHAN_D1:
           Fifo = FifoD1;
           FifoOut = FifoOutD1;
           active_pair = PAIR_D;
           status_mask = D1_FIFO_HALF_FULL;
        break;
```


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A.4 **p6102.c** (continued)

```
      case CHAN_D2:
         if(chan_ordered == 1)
         {
            Fifo = FifoD1;
            FifoOut = FifoOutD1;
         }
         else
         {
            Fifo = FifoD2;
            FifoOut = FifoOutD2;
         }
         active_pair = PAIR_D;
         status_mask = D2_FIFO_HALF_FULL;
      break;

      default:
         Fifo = FifoA1;
         FifoOut = FifoOutA1;
      active_pair = PAIR_A;
      status_mask = A1_FIFO_HALF_FULL;
      break;
   }

   *(vme_reg) = 0x2900;                /* A16 mode and LED off (4284) */
   ctl_setup(active_pair,A16_base);
}
/*********************************************************************/
/*                      SETUP CONTROL REGISTERS                      */
/*********************************************************************/
ctl_setup(active_pair, base)
unsigned int active_pair, base;
{
   unsigned int i;
   *VmeControl = 0x0800;                              /* reset 6102 */
   *VmeControl = 0x0000;                             /* release 6102 */

   #if INTERRUPTS
      *VmeControl |= 0x400;                           /* route IRQ4 */
   #endif

   *VmeAddress = 0x081e;                /* A32=0800 0000  A24=e0 0000*/
   *TriggerControl = 0xffff;                /* hold trigger in reset */
   *ClockSelect = 0xf000 | clock_select;       /* CLK select int clk */

   #if PRELOAD
      *ClockSelect |= PRLVAL;
   #endif

   *Sample1Div = 0x0000 | divider;             /* divide by 1 rate 1 */
   *Sample2Div = 0x0000 | divider;             /* divide by 1 rate 2 */
   *Sample3Div = 0x0000 | divider;             /* divide by 1 rate 3 */
   *Sample4Div = 0x0000 | divider;             /* divide by 1 rate 4 */
```


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A.4 **p6102.c** (continued)

```
   *DataFormat = 0x1111;             /* reset all FIFO state machines */
   *SingleMode = 0x0;                  /* initialize single comm port */

switch (active_pair)
   {
      case PAIR_A:
         *DataFormat = 0x1110 | FORMAT;
              /* set pair A for bus, both chans, time ordered, nopack */
         #if SINGLE_MODE_COMM
            *SingleMode = 0x1;           /* channel A1 in single mode */
         #endif
         StatusReg = StatusRegAB;
         InterruptMask = InterruptMaskAB;
      break;

      case PAIR_B:
         *DataFormat = 0x1101 | (FORMAT  << 4);
              /* set pair B for bus, both chans, time ordered, nopack */
         #if SINGLE_MODE_COMM
            *SingleMode = 0xf;   /* channel B2 thru A1 in single mode */
         #endif
         StatusReg = StatusRegAB;
         InterruptMask = InterruptMaskAB;
      break;

      case PAIR_C:
         *DataFormat = 0x1011 | (FORMAT << 8);
              /* set pair C for bus, both chans, time ordered, nopack */
         #if SINGLE_MODE_COMM
            *SingleMode = 0x1f;/* channel C1 thru A1 in single mode */
         #endif
         StatusReg = StatusRegCD;
         InterruptMask = InterruptMaskCD;
      break;

      case PAIR_D:
         *DataFormat = 0x0111 | (FORMAT << 12);
              /* set pair D for bus, both chans, time ordered, nopack */
         #if SINGLE_MODE_COMM
            *SingleMode = 0x40;/* channel d1 in single mode */
         #endif
         StatusReg = StatusRegCD;
         InterruptMask = InterruptMaskCD;
      break;

      default:
         *DataFormat = 0x111D;
            /* set pair A for comm, chan 1 only, time ordered, nopack */
      break;
   }
```


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A.4 **p6102.c** (continued)

```
#if PRELOAD
   *InterruptMaskAB |= SAMPLE_COUNTER_INTERRUPT;
#endif

#if RAMP_GENERATOR
   *InterruptMaskCD |= DIG_TEST_RAMP;
#endif

#if DA_ENABLE                                          /* D/A setup */
   *DaDataFormat = 0x1111;        /* reset all FIFO state machines */
   *DaSingleMode = 0x0;             /* initialize single comm port */

   switch (active_pair)
   {
      case PAIR_A:
         *DaDataFormat = 0x1110 | FORMAT;
           /* set pair A for bus, both chans, time ordered, nopack */
         #if SINGLE_MODE_COMM
            *DaSingleMode = 0x1;      /* channel A1 in single mode */
         #endif
         DaStatusReg = DaStatusRegAB;
         DaInterruptMask = InterruptMaskAB;
      break;

      case PAIR_B:
         *DaDataFormat  = 0x1101 | (FORMAT  << 4);
           /* set pair B for bus, both chans, time ordered, nopack */
         #if SINGLE_MODE_COMM
            *DaSingleMode = 0xf;/* channel B1 thru A1 in single mode */
         #endif
         DaStatusReg = DaStatusRegAB;
         DaInterruptMask = InterruptMaskAB;
      break;

      case PAIR_C :
         *DaDataFormat = 0x1011 | (FORMAT << 8);
           /* set pair C for bus, both chans, time ordered, nopack */
         #if SINGLE_MODE_COMM
            *DaSingleMode = 0x1f;/* channel C1 thru A1 in single mode */
         #endif
         DaStatusReg  = DaStatusRegCD;
         DaInterruptMask = InterruptMaskCD;
      break;

      case PAIR_D:
         *DaDataFormat = 0x0111 | (FORMAT << 12);
           /* set pair D for bus, both chans, time ordered, nopack */
         #if SINGLE_MODE_COMM
            *DaSingleMode = 0x40;/* channel d1 in single mode */
         #endif
         DaStatusReg = DaStatusRegCD;
         DaInterruptMask = InterruptMaskCD;
      break;
```


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A.4 **p6102.c** (continued)

```
            default:
               *DaDataFormat = 0x111d;
               /* set pair A for comm, chan 1 only, time ordered, nopack */
            break;
         }

         #if PRELOAD
            *DaInterruptMaskAB |= SAMPLE_COUNTER_INTERRUPT;
         #endif
      #endif
      *FifoReset = 0x0000;                          /* reset A/D FIFOs */
      *FifoReset = 0x00ff;                        /* release A/D FIFOs */

      *ClockResync = 0x0000;                    /* resync all rate divs */
      #if DA_ENABLE
         *DaFifoReset = 0x0000;                     /* reset D/A FIFOs */
         *DaFifoReset = 0x00ff;                   /* release D/A FIFOs */
      #endif
   }
   /*********************************************************************/

   void get_comm_data(portin, portout)
   unsigned int portin,portout;
   {
      unsigned int *comm_port_rdy, *comm_port_data, i,j;
      unsigned int *comm_port_out; *data;
      comm_port_rdy  =(unsigned int *)((portout * 16) + 0x100040u);
      comm_port_data =(unsigned int *)((portin  * 16) + 0x100041u);
      comm_port_out  =(unsigned int *)((portout * 16) + 0x100042u);
      for(i=0; i<count; i++)
      {
         *Buffer = *comm_port_data;
         #if DA_ENABLE
            *comm_port_out = *Buffer;
            test = *DaStatusReg;
         #endif
         Buffer = Buffer + 1;
      }

   void InitialInterrupts()
   {
      int01_vector = (unsigned int *) c_int01;
      *val_ivpt = ivtp_value();
      install_int_vector(int01_vector,3);
      load_iif(0x00004B99);/* enable EIIOF0 */
      INT_ENABLE();
      #if PRELOAD
         *InterruptMaskAB |= SAMPLE_COUNTER_INTERRUPT;
      #else
         *InterruptMask = status_mask ;                    /* half full */
      #endif
   }
```


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A.4 **p6102.c** (continued)

```
void c_int01()
{
   unsigned long dump;
   unsigned int *comm_rdy,*comm_data;
   unsigned int i,preval;
   #if PRELOAD
      *TriggerControl = 0xffff;                    /* hold it in reset */
      #if DA_ENABLE
         *DaTriggerControl = 0xffff;
      #endif

      #if MIXACC
         *MixInterruptClear = 0x0;   /* clear penteding MIX interrupt */
         dump = *MixControlReg ;    /* determine the interrupt source */
      #else
         *(unsigned int *) 0x90000000L &= 0xfffffff6;/* set D1 and D2 */
         dump = *(unsigned int *) IACK_LEV4;/* dummy read starts the IACK */
         *intr_mask = *IntrStat;    /* determine the interrupt source */
         dump = *StatusReg;                /* clear the interrupt bit */
      #endif


/*********************************************************************/
   /********************** add DSP code here **********************/
/*********************************************************************/

      comm_rdy  = (unsigned int *) ((com_portin * 16) + 0x100040u);
      comm_data = (unsigned int *) ((com_portin * 16) + 0x100041u);
      if(pack ==1)
         preval = PRLVAL/2;
      else
         preval = PRLVAL;

      for(i=0; i<preval; i++)
      {
         while((*comm_rdy & 0x00000f00) == 0);
         *Buffer++ = *comm_data;
      }
      Buffer = Buffer - preval;
      *TriggerControl = 0xfff0;

      #if DA_ENABLE
         *DaTriggerControl = 0xfff0;
      #endif
      #else                                          /* PRELOAD false */
      #if MIXACC
         *MixInterruptClear = 0x0;   /* clear penteding MIX interrupt */
         dump = *MixControlReg ;    /* determine the interrupt source */
      #else
         *InterruptMask = 0x0;/* initiate an IACK cycle */
         *(unsigned int *) 0x90000000L &= 0xfffffff6;/* set D1 and D2 */
         dump = *(unsigned int *) IACK_LEV4;/* dummy read starts the IACK */
         *intr_mask = *IntrStat;    /* determine the interrupt source */
```


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A.4 **p6102.c** (continued)

```
/*********************************************************************/
   /******************** add DSP code here ***********************/
/*********************************************************************/

      #endif

   Get_Data();
      #if PROCESS_DATA                          /* Perform Complex FFT */
         ProcessData(samples,data_buf,1024);
      #endif

      #if DISPLAY_DATA                       /* Scale Data for Display */
         DisplayData(data_buf,1024);
      #endif

      *FifoReset      = 0x0000;
      *FifoReset      = 0x00ff;
      *ClockResync    = 0x0000;
      *InterruptMask  = status_mask;
      *TriggerControl = 0xfff0;                     /* trigger point */

      #if DA_ENABLE
         *DaTriggerControl = 0xfff0;
      #endif
   #endif
}

led_on()                                              /* LED on 4284 */
{
   *vme_reg = ((*vme_reg) | 0x40);
}

led_off()                                             /* LED on 4284 */
{
   *vme_reg = ((*vme_reg) & (~0x40));
}

toggle_led()                                          /* LED on 4284 */
{
   *vme_reg = ((*vme_reg) ^ 0x40);
}

trigger()
{
   *timer1_address = 0x302u;
   *timer1_address = 0x306u;
   *timer1_address = 0x302u;
}
```


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A.4 **p6102.c** (continued)

```
void Get_Data()
{
   int i,k;
   #if IOTEST
      while(1)
      {
   #endif

   while((*StatusReg & status_mask) != 0);      /* wait for half full */

   for(k=0; k<4; k++)
   {
      while((*StatusReg & status_mask) != 0);
      if (access_mode == COMM)
         get_comm_data(com_portin, com_portout);
      else
      {
         for(i=0; i<count; i++)
         {
            *Buffer = *Fifo;
            #if DA_ENABLE
               *FifoOut = *Buffer;
            #endif
            Buffer = Buffer + 1;
         }
      }
   }

   test = *DaStatusReg;
   Buffer = Buffer - count*4;
   #if IOTEST
      }
   #else
      if((pack == 1) && (chan_ordered != 1))
      {
         for(i=0; i<NUM_SAMPLES; i++)
         {
            temp = *Buffer++;
            samples[i] = ((temp << 16) >> 16);
            i++;
            samples[i] = (temp >> 16);
         }
         Buffer = Buffer - FIFO_SIZE;
      }
```


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A.4 **p6102.c** (continued)

```
      else
      {
         for(i=0; i<NUM_SAMPLES; i++)
         {
            temp = *Buffer++;
            if(low_word == 1)
               samples[i] = ((temp << 16) >> 16);
            else
               samples[i] = (temp >> 16);
         }
         Buffer = Buffer - NUM_SAMPLES;
      }
   #endif
}

void InitMode()
{
   flag = 0;
   if ((FORMAT == VME_TIME_BOTH_NONPACK)
      || (FORMAT == COMM_TIME_CH2_NONPACK)
         || (FORMAT == COMM_TIME_CH1_NONPACK)
            || (FORMAT == VME_BOTH_PACK)
               || (FORMAT == COMM_BOTH_PACK))
   {
      count = 512;
      pack  = 0;
   }

   else
   {
      count = 256;
      pack = 1;
   }

if ((FORMAT == COMM_BOTH_PACK)
      || (FORMAT == COMM_TIME_CH2_NONPACK)
         || (FORMAT ==  COMM_TIME_CH2_PACK)
            || (FORMAT ==  COMM_TIME_CH1_NONPACK)
               || (FORMAT ==  COMM_TIME_CH1_PACK)
                  || ( SINGLE_MODE_COMM == 1))
      access_mode = COMM;
   else
      access_mode = VME;       /* Note: This could also be MIX access */

   if((FORMAT == COMM_BOTH_PACK) || (FORMAT == VME_BOTH_PACK))
      chan_ordered = 1;
   if((ACTIVE_CHAN == CHAN_A1) || (ACTIVE_CHAN == CHAN_B1)
      || (ACTIVE_CHAN == CHAN_C1)  || (ACTIVE_CHAN == CHAN_D1))
      low_word = 1;
```


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A.4 **p6102.c** (continued)

```
   divider = (unsigned int) ((FREQ/SAMPLFREQ) - 1);
   com_portin = COMM_PORTIN;
   com_portout = COMM_PORTOUT;
   clock_select = CLOCK;
   active_chan = ACTIVE_CHAN;
}

Init4284()
{
   *(c40_control)   = 0x3D9EC000u;             /* External ready only */
   *(c40_control+4) = 0x3DEF4000u;             /* External ready only */
   flag = 0;                 /* test flag for first preload interrupt */
   *timer1_address = 0x302u;
   *(vme_reg) = 0x3d00;                /* A24 mode and LED off (4284) */
   *(c40_reg) = 0x0;                  /* Set up for MIX control lines */
   *(c40_reg+2) = 0x30;                      /* Set VME IRQ level to 3 */
   *(c40_reg+3) = 0x00004000;     /* Block all interrupts except Host */
   *timer1_address = 0x302u;
   led_off();
}

InitAdPtrs()
{
   TriggerControl    = (unsigned int *) (AD_TRIG_CTRL | MODE);
   StatusRegAB       = (unsigned int *) (AD_STAT_AB | MODE);
   StatusRegCD       = (unsigned int *) (AD_STAT_CD | MODE);
   InterruptMaskAB   = (unsigned int *) (AD_MASK_AB | MODE);
   InterruptMaskCD   = (unsigned int *) (AD_MASK_CD | MODE);
   DataFormat        = (unsigned int *) (AD_DATA_FMT | MODE);
   SingleMode        = (unsigned int *) (AD_SGL_COM_EN_CC | MODE);
   FifoReset         = (unsigned int *) (AD_FIFO_RST_CAL | MODE);
   ClockSelect       = (unsigned int *) (AD_CKSL_SCT | MODE);
   ClockResync       = (unsigned int *) (CLK_DIV_SYNC | MODE);
   AdRearm           = (unsigned int *) (AD_ARM_CTRL | MODE);
   FifoA1            = (unsigned int *) (AD_FIFO_A1 | MODE);
   FifoA2            = (unsigned int *) (AD_FIFO_A2 | MODE);
   FifoB1            = (unsigned int *) (AD_FIFO_B1 | MODE);
   FifoB2            = (unsigned int *) (AD_FIFO_B2 | MODE);
   FifoC1            = (unsigned int *) (AD_FIFO_C1 | MODE);
   FifoC2            = (unsigned int *) (AD_FIFO_C2 | MODE);
   FifoD1            = (unsigned int *) (AD_FIFO_D1 | MODE);
   FifoD2            = (unsigned int *) (AD_FIFO_D2 | MODE);
}
```


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A.4 **p6102.c** (continued)

```
InitDaPtrs()
{
   DaTriggerControl  = (unsigned int *) (DA_TRIG_CTRL | MODE);
   DaStatusRegAB     = (unsigned int *) (DA_STAT_AB | MODE);
   DaStatusRegCD     = (unsigned int *) (DA_STAT_CD | MODE);
   DaInterruptMaskAB = (unsigned int *) (DA_MASK_AB | MODE);
   DaInterruptMaskCD = (unsigned int *) (DA_MASK_CD | MODE);
   DaDataFormat      = (unsigned int *) (DA_DATA_FMT | MODE);
   DaSingleMode      = (unsigned int *) (DA_SGL_COM_EN | MODE);
   DaFifoReset       = (unsigned int *) (DA_FIFO_RST | MODE);
   DaClockSelect     = (unsigned int *) (DA_CKSL_SCT | MODE);
   DaTriggerReArm    = (unsigned int *) (DA_ARM_CTRL | MODE);
   FifoOutA1         = (unsigned int *) (DA_FIFO_A1 | MODE);
   FifoOutA2         = (unsigned int *) (DA_FIFO_A2 | MODE);
   FifoOutB1         = (unsigned int *) (DA_FIFO_B1 | MODE);
   FifoOutB2         = (unsigned int *) (DA_FIFO_B2 | MODE);
   FifoOutC1         = (unsigned int *) (DA_FIFO_C1 | MODE);
   FifoOutC2         = (unsigned int *) (DA_FIFO_C2 | MODE);
   FifoOutD1         = (unsigned int *) (DA_FIFO_D1 | MODE);
   FifoOutD2         = (unsigned int *) (DA_FIFO_D2 | MODE);
}
```


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A.5 mod.h

```
/* mod.h -  This file determines the MIX Module's base address based on
            the processor which is running the program, the MIX
            Baseboard, and the MIX stack position being addressed.

   Note: This file only supports the following DSP processor boards:
         4283          4254             4257
         4284          4270             4285

   Defining the Baseboard:
      Set the appropriate BB_42XX constant to a 1 and the others to 0

   Running programs on a 4270, 4254, or 4257 Mix Module
      Set the MM_4270 constant if processor is on the 4270
      Set the MM_425X constant if processor is on the 4257

   Running program on the 4285, 4284 or 4283
      Clear the MM_4270 and MM_425X constants

   Specifying the MIX Module stack position of Mix Module being addressed
      For Mix stack position 0, set MOD to MOD0_ADDR
      For Mix stack position 1, set MOD to MOD1_ADDR
      For Mix stack position 2, set MOD to MOD2_ADDR

   Running programs on the 4283 Mix Baseboard(Setting the Page Register)
      To select Mix stack position 0, set MOD_SELECT to MOD0_SELECT
      To select Mix stack position 1, set MOD_SELECT to MOD1_SELECT
      To select Mix stack position 2, set MOD_SELECT to MOD2_SELECT */

/* Define BaseBoard Type */
#define BB_4283             0
#define BB_4284             0
#define BB_4285             1
#define BB_4200             0
#define BB_4201             0
#define BB_4202             0

/* Define Mix Module Type - Only if program is to be executed
                            on a Mix Module Processor */
#define MM_4270             0
#define MM_425X             1

/* Specify Mix Module Position of module being addressed */
#define MOD                 MOD1_ADDR

#if MM_4270 | MM_425X
   /* Specify MIX STACK Position for the 4270 or 425X processor boards */
   #define MIX_POS          0
#endif

#if BB_4283
   /* The 4283 Selects the Mix Module being addressed with a Page Register */
   #define MOD_SELECT       MOD1_SELECT
#else
   #define MOD_SELECT       MOD    /* Only being set to keep code similar */
#endif
```


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A.5 **mod.h** (continued)

```
#if BB_4285
   /* The 4285 has 2 independent paths for accessing the MIX bus resources:
      The Expansion Bus and the Global I/O bus.

      Note: The Expansion Bus may be mastered by any of the on-card 'C40
            processors or by off-card VMEbus masters.  The Global I/O Bus
            can be mastered only by 'C40 processors A, B, E or F.

      Note: MIX interrupts are not supported over the Global I/O Bus */

   #define EXP_BUS          1
   #define GLOB_BUS         0
#endif

/* BaseBoard = 4283 - This BaseBoard does not support Upper Mix Bus Masters */
#if BB_4283
   /* The 4283 Baseboard uses a page register to select which Mix Module
      is being accessed */
   #define  MOD0_SELECT     0x18000
   #define  MOD1_SELECT     0x10000
   #define  MOD2_SELECT     0x8000

   #define  MOD0_ADDR       0x00804000
   #define  MOD1_ADDR       0x00804000
   #define  MOD2_ADDR       0x00804000

   /* Some Mix Modules require the setting of Address Bit 27   */
   /* This is selected in the Page Register for this baseboard */
   #define D17_DATA_BIT       0x00020000

   /* Address Bit in address which corresponds to A27 -
      This is unused by 4283 */
   #define A27_ADDR_BIT    0x00000000

#endif
```


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A.5 **mod.h** (continued)

```
/* BaseBoard = 4284 */
#if BB_4284

   #if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257 */

      #define MOD0_ADDR    0xC0000000
      #define MOD1_ADDR    0xC4000000
      #define MOD2_ADDR    0xC8000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT 0x02000000

   #else                   /* No Mix Module */

      #define MOD0_ADDR    0x20000000
      #define MOD1_ADDR    0x24000000
      #define MOD2_ADDR    0x28000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT 0x02000000
   #endif

#endif

/* BaseBoard = 4200 or 4201 */
#if BB_4200 | BB_4201

   #if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257 */

      #define MOD0_ADDR    0xF0000000
      #define MOD1_ADDR    0xF4000000
      #define MOD2_ADDR    0xF8000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT 0x02000000

   #else                   /* No Mix Module */

      #define MOD0_ADDR    0xC0000000
      #define MOD1_ADDR    0xD0000000
      #define MOD2_ADDR    0xE0000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT 0x02000000
   #endif

#endif
```


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A.5 **mod.h** (continued)

```
/* BaseBoard = 4202  */
#if BB_4202

   #if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257 */

      #define MOD0_ADDR    0xC0000000
      #define MOD1_ADDR    0xC4000000
      #define MOD2_ADDR    0xC8000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT 0x02000000
   #endif

#endif


/* BaseBoard = 4285 */
#if BB_4285

   #if MM_4270 | MM_425X   /* Mix Module = 4270, 4254, or 4257 */
      #define MOD0_ADDR    0xC0000000
      #define MOD1_ADDR    0xC4000000
      #define MOD2_ADDR    0xC8000000

      /* Address Bit in address which corresponds to A27 */
      #define A27_ADDR_BIT      0x02000000

   #else                   /* No Mix Module */

      #if EXP_BUS
         #define MOD0_ADDR    0x90000000
         #define MOD1_ADDR    0x90200000
         #define MOD2_ADDR    0x90400000

         /* Address Bit in address which corresponds to A27 */
         #define A27_ADDR_BIT 0x00100000
      #endif

      #if GLOB_BUS
         #define MOD0_ADDR    0xC8000000
         #define MOD1_ADDR    0xC8200000
         #define MOD2_ADDR    0xC8400000

         /* Address Bit in address which corresponds to A27 */
         #define A27_ADDR_BIT 0x00100000
      #endif

   #endif

#endif
/************************* End of File ****************************/
```


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Appendix B: Model 6102 Errata

B.1 Introduction

This appendix documents known discrepancies in the current configuration of the Model 6102. These issues may be addressed by future ECOs.

B.2 VMEbus Access to the D/A FIFOs

VMEbus access to the Model 6102's D/A FIFOs is available in A16 space **ONLY**. A24 and A32 VME access is not supported in the current configuration of this device. Consequently, block write operations to these FIFOs (which are not supported in A16 space by VME specification) are likewise unavailable.

B.3 Bit Reversal in D/A FIFO Reset Register

The intended functions of two of the bits in the Model 6102's D/A FIFO Reset Register were reversed. Table 3-37, on page 92 of this manual (in Section 3.6.6), documents the intended bit configuration. Bits D2 and D3 in this register were reversed in the actual design. Thus, bit D2 is used to reset D/A B2's FIFO, and bit D3 will reset the FIFO for D/A B1. A corrected version of Table 3-37 appears below, as Table B-1. The corrections are shown in **boldface** type.

Table B-1: Model 6102 - D/A FIFO Reset Register - R/W @ DA_FIFO_Rst

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DA_FIFO_ D2_Reset	DA_FIFO_ D1_Reset	DA_FIFO_ C2_Reset	DA_FIFO_ C1_Reset	DA_FIFO_ **B1**_Reset	DA_FIFO_ **B2**_Reset	DA_FIFO_ A2_Reset	DA_FIFO_ A1_Reset
Bit Function	1 = Release FIFO and enable data collection 0 = Reset FIFO and disable data collection							
NOTE: Toggle the appropriate bit(s) to implement the reset function.								

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B.4 Pipeline Delay

The minimum pipeline delay, from the time a sample is read from the A/D to the time that sample can be output by the D/A, is three (3) sample periods. This is caused by the two-stage register at the input of the AD569 DACs used on the Model 6102, and cannot be eliminated in the hardware. We do, however, have a recommendation to minimize the effects of this delay.

In situations where minimizing delay is critical to your application, the D/A sample rate should be set as high as possible. Although the 16-bit settling time of the AD569 DAC is typically 3 μs (corresponding to a 333 kHz sample rate), it can be operated (at decreased accuracy) at sample rates as high as 1 MHz. In such a case, the effective analog output update rate is determined by the rate at which data is written into the D/A FIFO. Because the output data is latched, each data value written to the FIFO is held at the DAC's output until a new sample is written. Samples can be written to the D/A FIFO at a rate determined by the A/D sample rate or by a timing pulse generated by the controlling DSP. This scenario is essentially a sacrifice of the D/A FIFO (which effectively becomes one sample deep when used in this manner) for minimal delay.

Additionally, when seeking to minimize the 6102's pipeline delay, the FIFOs should be enabled via absolute pointer writes, not by function calls or structure redirections, as both of those operations have additional overhead. The inner data processing loop needs to be carefully designed so that any operations to be performed between the acquisition of an A/D sample and the delivery of the processed sample to the D/A are completed before the next sample appears at the A/D output.

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