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OPERATING MANUAL

PENTEK MODEL 6216

Dual A/D Converter and Digital Receiver
VIM Module for Pentek VIM Motherboards

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Pentek Model 6216 Operating Manual – Revision History

Date	Rev	Applicable Serial #'s	Comments
02/11/99	Preliminary	9905001 – Forward	Inital release.
02/18/99	Preliminary	9905001 – Forward	Corrected tables 3–11 and 3–12; added section3.8.1, "Loading the 12–bit Gain Control Word"
03/29/99	Preliminary	9905001 – Forward	Added additional table and page information to table 3–1. Added table 3–12 about Full Scale values. Various minor typographical corrections.
05/17/99	Preliminary	9905001 – Forward	Section 3.3, Tables 3–2 and 3–3 also App. B, table B–1 changed D01 bit designation to reserved
06/28/99	Preliminary	9905001 – Forward	Section 1.7, added a "Gain Range" description to the Specification Section; describes difference of standard unit and Option 102. Table 3–12, corrected heading to state Option 102 instead of Option 101..
07/01/99	Preliminary	9905001 – Forward	Section 1.7, added Power Requirement description to the Specification Section
03/24/00	A	9905001 – Forward	Complete re–format – many tables removed & replaced w/ text. All referenes to 4290/91 changed to VIM motherboard, and non–address specific references to 'C6x changed to VIM motherboard processor. Updated & corrected Block Diagram. Sec. 1.7. Corrected supply currents. Internal Oscillator is 64 MHz, not 65. Corrections to Fig. 2–4. Note that Gain values given in Table 3–6 for PGA do not account for filter insertion loss. Add Tables 3–9 describing format/packing of output data & 3–10, A/D output coding. Improved description of signal levels/limits for EXT CLK IN. Improved description of control interface to GC1012. Re–arrange Appendices – Move EEPROM format to Appendix D; Make Graychip data sheet Appendix A; Add AD603 Data Sheet as Appendix B; LTC1451 Data Sheet is Appendix C; Old Appendix B (Programming Example) now covered in ReadyFlow Manual for 6216 (Pentek part # 801.62160)
4/9/01	B	9905001 – Forward	Sec. 2.3.1 – recommend that Ext. Clock In be 2V p–p in amplitude. Add Sec. 2.3.1.1, on Duty Cycle Sensitivity. Sec. 2.4 – add part #'s for Sync Bus/SPort mating connector. Sec 2.4.1 – mention that Sync Bus can support 8 units, & Model 9190 can sync up to 80 units. Add Sec. 2.4.1.5, on Sync Bus Compatibility. Sec. 2.4.2 – Better description of how Serial Port signals are passed from Motherboard to FP connector, less text in subsections. Sec. 2.4.3 – $\overline{\text{TTL–SYNC}}$ pulse must be at least 2 sample clocks wide. Sec. 3.10 – SYNC Generate Reg is R/W, not R. O. Sec. 3.11.3 – Added note in Table 3–17 stating that setting the FLIP bit inverts the DDR's Q output.

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Chapter 1: Overview

1.1 General Description

Pentek's Model 6216 is a VIM−2 Digital Drop Receiver (DDR) module (devices of this type are also often referred to as Digital Down Converters, or DDCs), designed to be attached directly to any of Pentek's DSP− or RISC−based VIM motherboards, such as Pentek Models 4290, 4291 and 4292. It forms a complete 2−channel software radio system including tuning, filtering and demodulation.

Two Model 6216s may be attached to any VIM−compatible processor board to form a 4−channel software radio which utilizes all four processors while occupying only one VMEbus slot. Alternately, the Model 6216 may be combined with another VIM−2 module to provide additional I/O functions.

1.2 Input Section

Each channel includes an analog front end which employs a wideband input amplifier followed by a programmable gain amplifier. It accommodates wideband analog inputs between 5 kHz and 80 MHz, at full−scale levels of −20 dBm to +10 dBm. Analog inputs are accepted through front panel SMA connectors.

An anti−aliasing filter removes out−of−band frequency components and can be tailored for specific signal types. The standard factory−supplied lowpass filter has a cutoff frequency of 25 MHz. The programmable−gain amp and filter may be bypassed to support undersampling applications.



Option 102 provides full scale levels of −30 dBm to 0 dBm and a filter cut−off frequency of 30 MHz.

1.3 A/D Converters

Each channel employs an Analog Devices AD6640 12–bit A/D converter capable of sampling rates up to 65 MHz. The A/D sample clock can be derived from an internal 64 MHz crystal oscillator or from an external reference supplied to another front panel SMA connector.



1)Due to packaging constraints the internal oscillator is not user–replaceable. Currently available are Options 020 (65 MHz) and 021 (60 MHz). If other clock frequencies are required, contact Pentek for custom oscillators.

2)The maximum sampling rate can ONLY be achieved using an external reference signal, unless the internal oscillator is replaced.

Both A/D converters operate synchronously from the same sampling clock to support multichannel applications (such as direction finding) where phase between channels must be maintained.

1.4 Digital Drop Receivers

The output of each A/D converter feeds a GC1012A programmable downconverter. This device is designed for wideband output operation, with decimation values ranging from 2 to 64, for output bandwidths as high as 25 MHz.

The output section delivers direct I and Q complex outputs to the mezzanine FIFO of the VIM Motherboard. A bypass MUX provides a direct path from the A/D converter output directly into the FIFO buffer for direct capture of input data at rates up to 65 MHz.

A front panel ribbon cable bus allows multiple 6216s to share a common sample clock and synchronize the phase of digital receivers across modules.

1.5 Connection to VIM Motherboard

Both 16–bit parallel output data ports (ports A and B) from the Model 6216 flow into the FIFO structures on the VIM motherboard. A control path from each motherboard processor permits direct programming of the GC1012A functions including tuning, decimation, output formatting, filter control and filter coefficients.

1.6 Simplified Block Diagram

Figure 1–1, below, provides a simplified block diagram of the Model 6216.

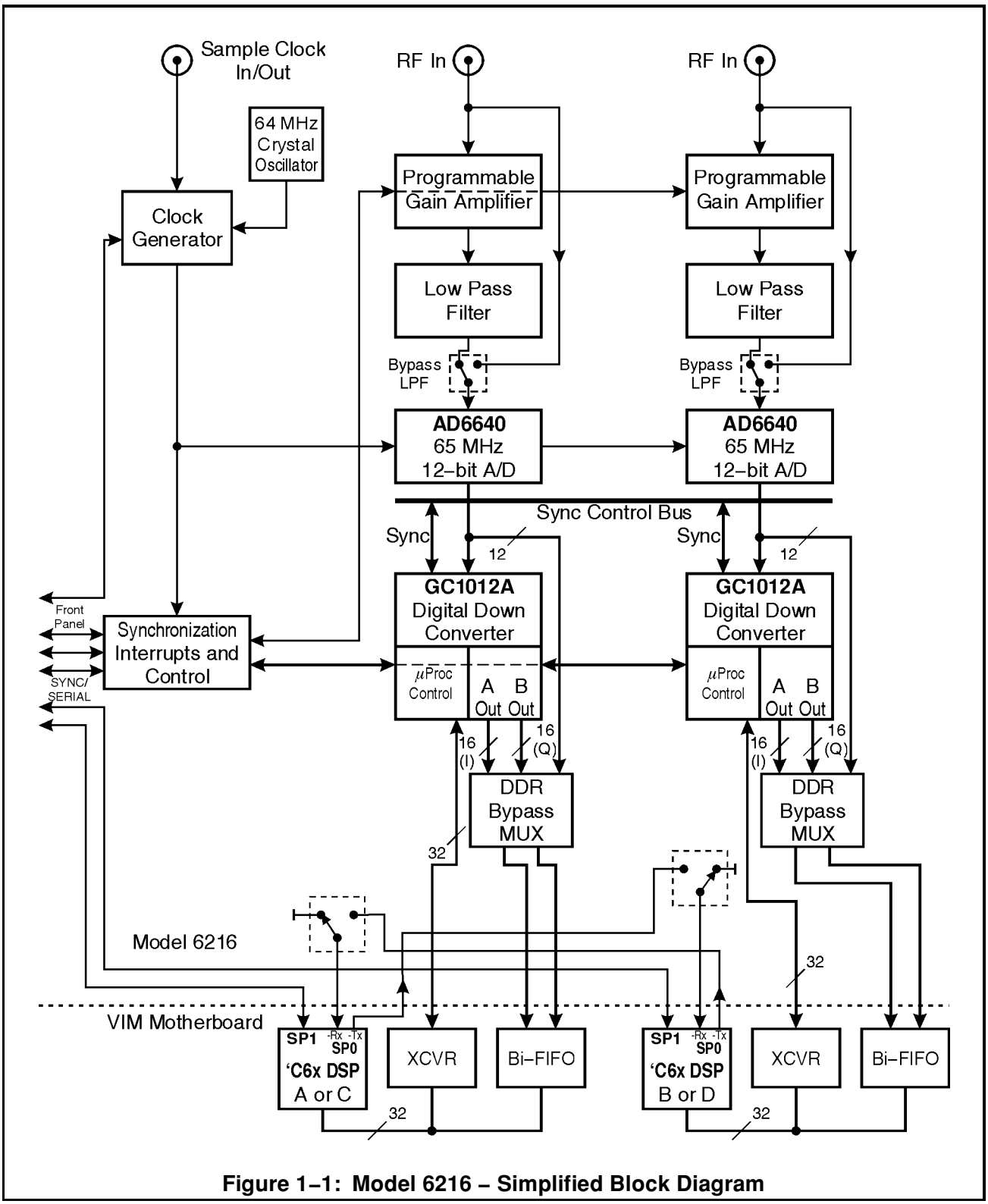


Figure 1–1: Model 6216 – Simplified Block Diagram

1.7 Specifications

The specifications below are typical, at 25°C ambient temperature, with + 5 V_{DC} and ± 12 V_{DC} power supplies within ± 1 % of nominal, unless otherwise specified.

Input Channels

Quantity:	2
Input Type:	Single−ended, non inverting
Input Impedance:	
Standard:	50 Ω
Option 101:	650 kΩ
Full Scale Voltage:	± 1.0 Volts

Input Amp/Filter

Quantity:	2 (one per A/D Channel)
Amplifier #1	
Type:	Fixed gain Burr Brown OPA642
Bandwidth:	80 MHz
Bypass:	None
Amplifier #2	
Type:	Analog Devices AD603* Programmable Gain Amp controlled by 12−bit D/A (Linear Technology LTC1451†)
Bandwidth:	25 MHz
Bypass:	Programmable (includes filter)
Gain (full scale):	
Standard:	10 dBm to −20 dBm
Option 102:	0 dBm to −30 dBm

* – Data Sheet included as Appendix C, courtesy of Analog Devices Inc., Norwood, MA.
† – Data Sheet included as Appendix D, courtesy of Linear Technology Corp., Milpitas, CA.

Anti−Aliasing Filter	
Type:	Fixed frequency low pass − 5 pole Chebyshev
Passband (−3 dB):	
Standard:	25 MHz
Option 030:	30 MHz
Passband Flatness:	± 1 dB
Stopband:	80 MHz
Stopband Attenuation:	> 60 dB
Bypass:	Programmable (includes P. G. Amp)

A/D Converter:

Device:	Analog Devices AD6640**
Quantity:	2
Sampling Rate:	6.5 MHz min, 65 MHz max.
Coupling:	AC, 5 kHz cut in
Clock Source:	Selectable − Onboard crystal oscillator or front panel external clock.
Resolution:	12 bits

** – Data Sheet included as Appendix B, courtesy of Analog Devices Inc., Norwood, MA.

1.7 Specifications (continued)

Signal Purity

Front End Performance w/ Programmable Amp

Harmonic Distortion:	–60 dB
Signal/Noise Ratio (30 MHz)	–50 dB
Spur Free Dynamic Range:	–65 dB
Crosstalk:	–60 dB @ 1 MHz

Front End Performance w/o Programmable Amp

Harmonic Distortion:	–70 dB
Signal/Noise Ratio (30 MHz)	–60 dB
Spur Free Dynamic Range:	–70 dB
Crosstalk:	–60 dB @ 1 MHz

Sample Rate Control

Clock Source:

Internal:	Onboard crystal oscillator
Standard:	64 MHz
Option 020:	65 MHz
Oprion 021:	60 MHz
External:	Front Panel Low–Voltage Differential Signal (LVDS) 65 MHz max.
Sample Rate Divider:	internal or external source can be divided by 1, 2, 4, 8, or 10 .

Digital Receiver

Device:	Graychip GC1012A*
Quantity:	2
Data Source:	Associated A/D (A/D 1 to DDR 1, A/D 2 to DDR 2)
Clock Source:	Same as associated A/D source.
Bypass:	Under software control, each DDR can be bypassed individually to provide A/D output to the BI–FIFO interface.
Sync:	Provided through VIM motherboard–driven control register or via front panel connector.

* – Data Sheet included as Appendix A, courtesy of Graychip, Inc.., Palo Alto, CA.

Front Panel

Analog Input:	2 SMA Connectors (1 per channel)
Sample Clock:	Multipin connector (programmable as input or output – differential LVDS compatible only) and 1 SMA connector (also LVDS only)
Sync:	Multipin connector (programmable as input or output – differential LVDS compatible only) and one TTL input
VIM Motherboard Functions	Provides access to VIM Motherboard XDS connec–tor and status LEDs
VIM Motherboard Reset:	Front panel control

1.7 Specifications (continued)

Power Requirements:

+5 V_{DC}
Min. (idle): 760 mA
Max. (loaded): 3000 mA

+12 V_{DC}
Min. (idle): 750 mA
Max. (loaded): 750 mA

−12 V_{DC}
Min. (idle): 500 mA
Max. (loaded): 500 mA

Dimensions:

VIM−2 Module
Height: 114 mm (4.5−in.)
Depth: 82 mm (3.25−in.)
Width: 20 mm (0.8−in.)

Chapter 2: Installation and Connections

2.1 Inspection

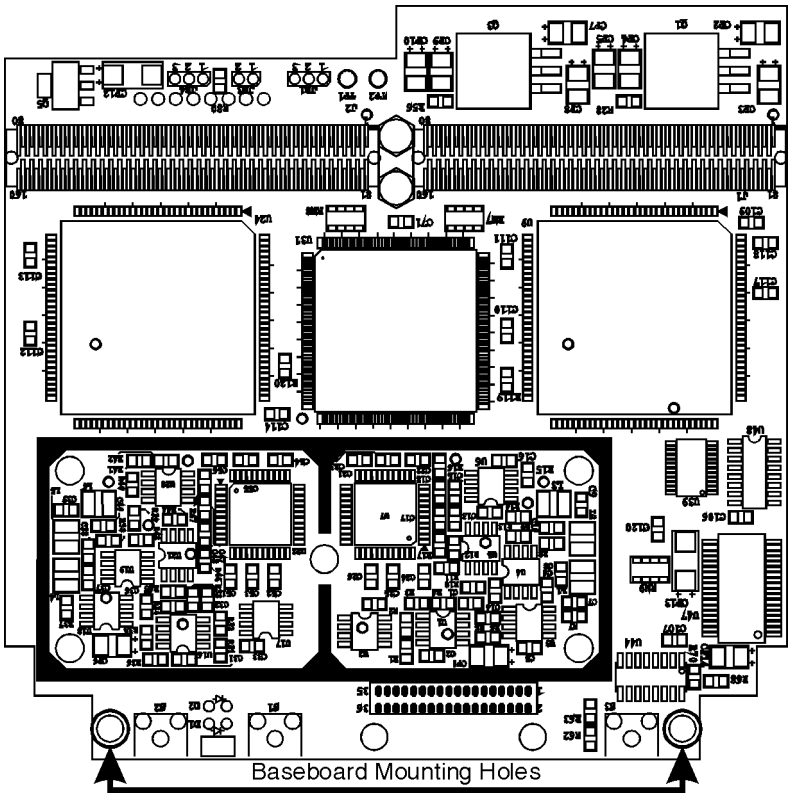
After unpacking the unit, inspect it carefully for possible damage to connectors or components. If any damage is discovered, please contact Pentek immediately at (201) 818–5900. Also, please save the original shipping container and packing material in case reshipment is required.

2.2 Jumper Blocks

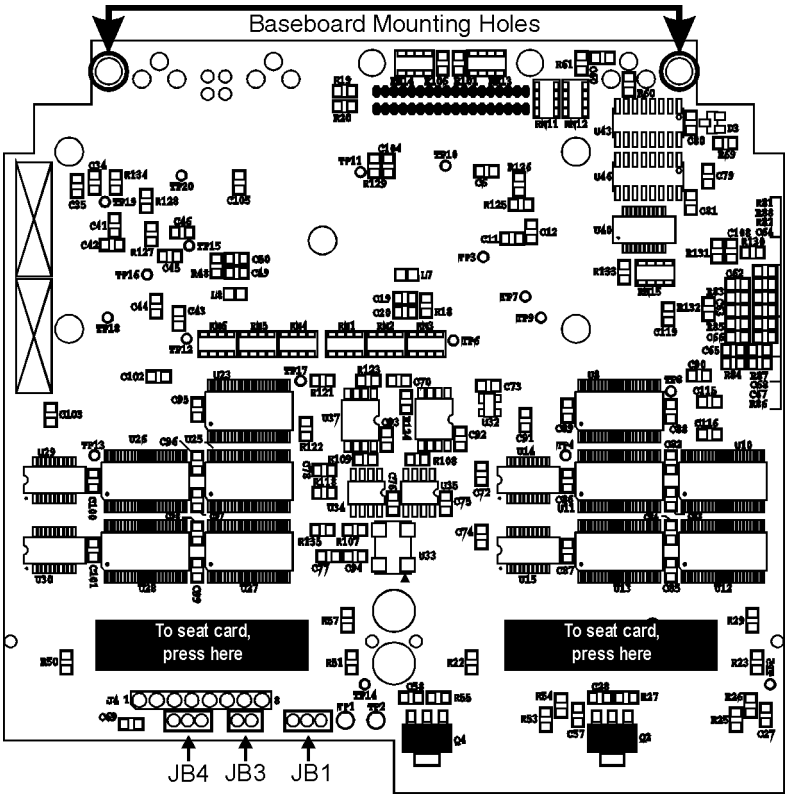
The Model 6216 PC board contains several jumper blocks. Figure 2–1, on the next page, shows all jumper block locations. Please be aware that all of the jumpers are configured at the factory for proper operation and should not be moved. Table 2–1, below, provides the factory jumper settings for reference, or in case you suspect that they have been tampered with.

Table 2–1: Model 6216 – Factory Jumper Settings

Jumper Block	Factory Setting
JB1	Pins 1–2
JB3	Jumper ON (pins 1–2)
JB4	Pins 2–3



(a) Component Side



(b) Solder Side

Figure 2–1: Model 6216 PC Board, Showing Jumper Blocks & Mounting Holes

2.3 Model 6216 Front Panel Features

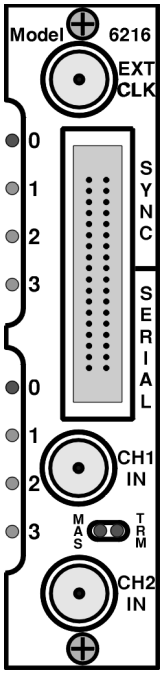


Figure 2–2: Model 6216 – Front Panel

The Model 6216's front panel is shown in Figure 2–2, at the right. This panel occupies one of the VIM module positions available on a VIM motherboard's front panel. If the Model 6216 is the only mezzanine board installed, the other half of the motherboard's panel may be filled with a blank, supplied with the motherboard. Available on the Model 6216's front panel are three SMA connectors, one for each channel's analog input signal and a third for an external clock signal. Two indicator LEDs associated with the 6216's Sync Bus interface are visible between the two analog input connectors, and four LED's associated with each motherboard processor that can access the module can be seen through cutouts on the left side of the panel. The panel's most prominent feature is the 36–pin Sync Bus – Serial I/O connector, which will be covered in Section 2.4. The other panel features mentioned above will all be discussed in the subsections that begin below.

2.3.1 External Clock Input – EXT CLK

The threaded, coaxial SMA connector nearest the top of the Model 6216's front panel is provided for the application of an external clock signal. This signal can be used as the sample clock signal for the 6216's A/D converters.

The External Clock Input circuit used on Pentek's Model 6216 is designed to accept Low–Voltage Differential Signals (LVDS). The impedance presented by the external clock input is 50 Ω. The applied signal is AC coupled via 0.1 µF to the + input of an LVDS line receiver. This input is diode–protected to ground and +3.3 V, and biased at +1.65 V (the – input of the receiver is also biased at +1.65 V). LVDS devices can typically react to differential input signal swings as low as 250 mV, or, when used in a single–ended manner (as in this case), to signal levels as low as 100 mV above, or 20 mV below, the bias voltage. For most applications, Pentek recommends that the signal applied to this connector be a square or sine wave, with 2 V p–p amplitude, at frequencies up to 65 MHz. Figure 2–3, at the top of the next page, shows the equivalent circuit for the Model 6216's EXT CLK input.

2.3.1.1 Duty Cycle Sensitivity

The A/D converter used on the Model 6216 is the AD6640, from Analog Devices. The graphs presented in the AD6640 Data Sheet (see Appendix B) indicate that the ADC is relatively insensitive to duty cycle variations between 40% and 65%. Figure 17 in the Data Sheet shows the SNR and Spurious performance at varying duty cycles for a 2.2 MHz analog input signal sampled at 65 MHz. Under these conditions, the performance seems quite good.

2.3 Model 6216 Front Panel Features (continued)

2.3.1 External Clock Input (continued)

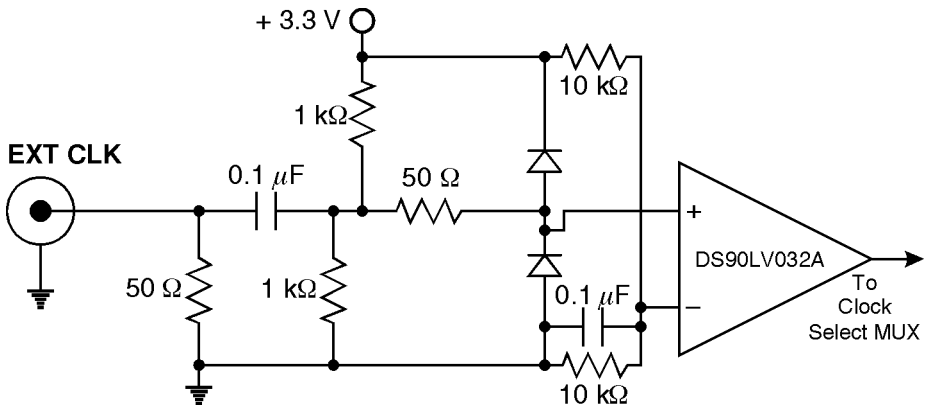


Figure 2–3: Model 6216 – External Clock Input Circuit

2.3.1.1 Duty Cycle Sensitivity (continued)

Our experience with this device under different conditions, however, has not been quite so favorable. We have found that if the device is operated at sample rates of 60 MHz or more, with an input signal that is offset slightly from the sample rate (e. g., sampling a 60.05 MHz signal at a 60 MHz sample rate), significant conversion errors can occur at the ADC's output if the duty cycle varies even marginally from 50%.

Referring to the AD6640's switching specifications for the ENCODE input (this is where the sample clock signal is delivered), we see that the minimum high and low pulse widths at that input are both 6.5 nsec. Bearing that in mind, consider that a perfect square wave at 65 MHz has a half–cycle time slightly less than 7.7 nsec. Now bring that perfect square wave into the real world, where such things as rise and fall time exist, and you can see how it might become difficult NOT to violate the 6.5 nsec pulse width specification at the maximum sample rate.

There is a significant amount of signal conditioning and selection circuitry between the 6216's EXT CLK input and the AD6640's ENCODE input. This tends to cause a small amount of difference between the duty cycle of the signal you deliver to the front panel connector and the duty cycle of the signal we deliver to the ADC. So, even if you know that your EXT CLK input signal has a duty cycle of 50% $\pm$ 0.00001%, that's probably not what the ADC sees.

2.3 Model 6216 Front Panel Features (continued)

2.3.1 External Clock Input (continued)

2.3.1.1 Duty Cycle Sensitivity (continued)

Now that we've given you what seems to be some bad news, we'll follow with the good news. We have ONLY seen the AD6640's duty cycle sensitivity become a problem in the very specific situation where the sample rate is relatively high ($\geq$ 60 MHz), AND the analog input signal's frequency is very close to the absolute sample rate or a multiple thereof. In such cases, the apparent output signal from the A/D is an alias of the difference frequency, and contains a relatively high number of samples per cycle. The problem is easily visible in real−time plots of the A/D output, as glitches in the output signal. Should your application require that you operate your 6216 in this manner, we make the following recommendations:

1) DO NOT use the internal oscillator as your clock source, as there is no way to control the internal clock's duty cycle. Instead, apply and select an external clock signal with a variable duty cycle.

2) Before attempting any serious data acquisition, monitor and plot the A/D output in real time, and adjust the duty cycle of the clock input until the glitches disappear.

2.3.2 Analog Inputs – CH1 IN, CH2 IN

The two threaded, coaxial SMA connectors nearest the bottom of the Model 6216's front panel are the Analog Input Connectors. The analog inputs are terminated in 50 Ω, and directly coupled to the non−inverting inputs of OPA642 Operational Amplifiers. The maximum input signal swing for linear operation is ± 1 V (i. e., 2 V_{P-P}). The amplifier's bandwidth is 80 MHz, but because the Model 6216's maximum sample rate is 65 MHz (64 MHz if the internal crystal oscillator is used as the sample clock), the bandwidth of signals applied to these inputs should be limited to 32.5 MHz (32 MHz if the internal crystal oscillator is used as the sample clock), or to one half of the programmed sample rate, unless your application requires undersampling.

2.3.3 Indicator LEDs

A total of ten LED's are visible through the front panel of the Model 6216. Two of these are associated with the 6216's Sync Bus interface. These are located between the Analog Input Connectors, slightly to the right of the center of the panel. The other eight are general purpose indicators controlled by the processors on the VIM motherboard, and are visible through the cutouts at the left side of the 6216's front panel. These will all be discussed in the sub−sections that begin at the top of the next page.

2.3 Model 6216 Front Panel Features (continued)

2.3.3 Indicator LEDs (continued)

2.3.3.1 Sync Bus Master LED – MAS

The red MAS LED, the leftmost one near the panel's center, indicates that the Sync Bus master function has been enabled for the 6216 in question. This means that the 6216 on whose panel this LED is lit will be the one that provides the Sync signals to all other VIM modules connected to the Sync Bus. Any Sync Bus MUST have **one and only one** master, and it should physically be located at the opposite end of the Sync Cable from the Sync Terminator (see Section 2.3.3.2, below). This LED will be illuminated whenever the D0 bit in the 6216's Control Register (see Section 3.4) is set to the logic '1' state. It will be turned off when that bit is cleared to the logic '0' state.

2.3.3.2 Sync Bus Terminator LED – TRM

The red TRM LED, the rightmost one near the panel's center, indicates that the Sync Bus Master termination has been enabled for the 6216 in question. This means that the 6216 on whose panel this LED is lit will be the one that provides the terminating resistors for the Sync signals generated by the Sync Bus master. Any Sync Bus MUST have **one and only one** terminator, and it should physically be located at the opposite end of the Sync Cable from the Sync master (see Section 2.3.3.1, above). This LED will be illuminated whenever the D1 bit in the 6216's Control Register (see Section 3.4) is set to the logic '1' state. It will be turned off when that bit is cleared to the logic '0' state.

2.3.3.3 Motherboard LEDs – 0, 1, 2 & 3

Visible through cutouts at the left side of the Model 6216's front panel are two groups of four LEDs controlled by the processors on the VIM motherboard. Each group of four LEDs contains one red LED (labeled 0) and 3 green LEDs (labeled 1, 2 & 3), and they are under the control of one of the motherboard's processors. Depending upon the position in which the VIM module is installed on the motherboard, the four LEDs nearest the top of the panel are controlled by either Processor A or Processor C, and the four at the bottom are controlled by either Processor B or Processor D. For further details about these indicators, please refer to your VIM motherboard's Operating Manual.

2.4 Sync Bus – Serial I/O Connector

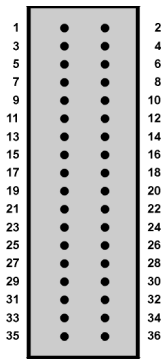


Figure 2–4: Model 6216 – Front Panel Sync Bus – Serial I/O Connector Pin Numbering

Accessible through each Model 6216's front panel is a 36–pin serial connector (3M part #81036–500203, Pentek part # 354.03610), several pins of which are connected to (and driven by) the VIM motherboard's serial ports. The mating connector is 3M part # 83036–6006 or an equivalent, Pentek part # 353.03605. Also included on this connector are signals used for synchronizing multiple units. Table 2–2, at the bottom of this page, contains the pinouts and description of this connector, whose pin numbering scheme is shown in Figure 2–4, at the right.

2.4.1 Signals for Synchronizing Multiple Boards

The following LVDS (Low–Voltage Differential Signaling) signals make up the sync bus; MCLK, GSYNC, SSYNC, and ASYNC. The sub–sections that begin on the page after next describe each of these signals. Figure 2–5, on the next page, shows a block diagram of the Sync and Clock signal sources.

Table 2–2: Model 6216 – Sync Bus – Serial I/O Pinouts

Pin	Signal	Pin	Signal
1	Ground	2	MCLK
3	$\overline{\text{MCLK}}$	4	Ground
5	GSYNC	6	$\overline{\text{GSYNC}}$
7	SSYNC	8	$\overline{\text{SSYNC}}$
9	ASYNC	10	$\overline{\text{ASYNC}}$
11	Ground	12	N/C
13	N/C	14	Ground
15	$\overline{\text{TTL–SYNC}}$	16	Ground
17	P0–CLKR1	18	Ground
19	P0–FSR1	20	P0–DR1
21	P0–CLKS1	22	Ground
23	P0–CLKX1	24	Ground
25	P0–FSX1	26	P0–DX1
27	P1–CLKR1	28	Ground
29	P1–FSR1	30	P1–DR1
31	P1–CLKS1	32	Ground
33	P1–CLKX1	34	Ground
35	P1–FSX1	36	P1–DX1

Up to eight (8) 6216's can be operated synchronously by cabling these connectors together. Further details about how this is accomplished are provided in the subsections beginning on the page after next, and in Sections 3.4 and 3.10. If your application requires more than 8 units synchronized units, Pentek's Model 9190 can be used to synchronize up to eighty (80) 6216s.

2.4 Sync Bus – Serial I/O Connector (continued)

2.4.1 Signals for Synchronizing Multiple Boards (continued)

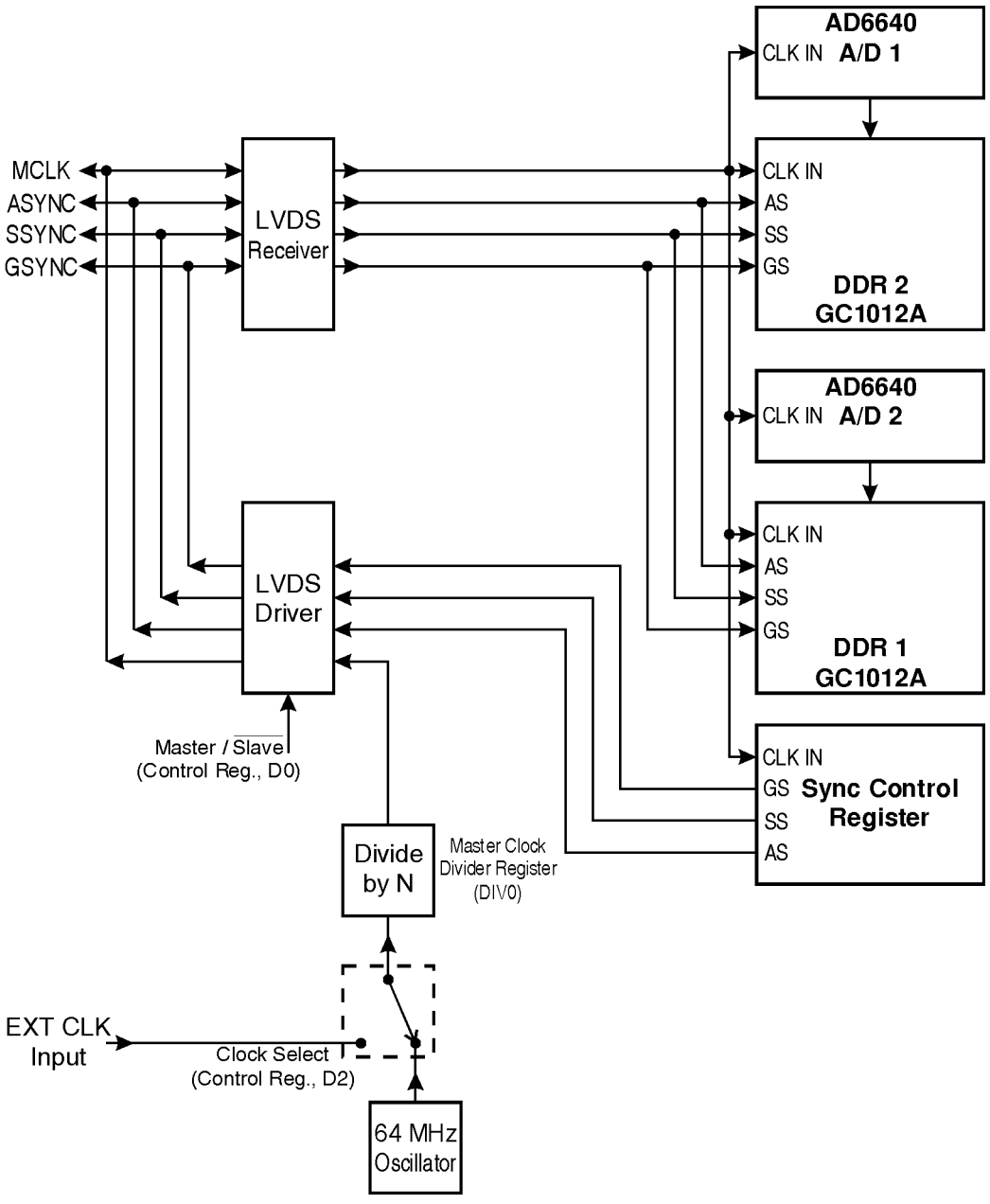


Figure 2–5: Model 6216 – Block Diagram of Clock and Sync Signal Sources

Note

DDR 1 is controlled by VIM Motherboard Processor A or C, and DDR2 is controlled by Processor B or D, depending upon where the VIM module is installed on the motherboard.

2.4 Sync Bus – Serial I/O Connector (continued)

2.4.1 Signals for Synchronizing Multiple Boards (continued)

2.4.1.1 MCLK, $\overline{\text{MCLK}}$

This signal is used as the sample clock for the A/D converters. When the Model 6216 is configured as a master, this is an LVDS output at the A/D sample clock rate. If the board is configured for an external clock, then the original source for this signal is the **EXT CLK** SMA input connector. Otherwise, the on–board crystal oscillator is used as the frequency source. The frequency of MCLK is equal to the external or crystal frequency divided by the contents of the Master Clock Divider register (see Section 3.5).

When configured as a slave, this signal is a differential LDVS input and will be used as the A/D sample clock, instead of the board's own external clock input or on–board oscillator. This is how several boards are able to sample synchronously from the same reference clock source.

2.4.1.2 ASYNC, $\overline{\text{ASYNC}}$

This is the accumulator sync signal to the GC1012A. The accumulator sync is provided to synchronously change tuning frequencies. This sync can be used to load a new tuning frequency into the frequency register and/or clear the frequency accumulator of the DDR. If the board is configured as a Sync bus master, then this is a differential LVDS output. If the Model 6216 is configured as a Sync bus slave, this signal is a differential LVDS input.

2.4.1.3 SSYNC, $\overline{\text{SSYNC}}$

This signal is the system synchronization pulse for the GC1012A. It can synchronize all timers, accumulators and control counters. When in the DDR bypass mode it can also be used to synchronize the VIM motherboard's input FIFOs and the FIFO write rate dividers for multiple channels and boards. If the board is configured as a Sync bus master, then this is a differential LVDS output. If the Model 6216 is configured as a Sync bus slave, this signal is a differential LVDS input.

2.4.1.4 GSYNC, $\overline{\text{GSYNC}}$

This is the gain sync signal to the GC1012A. The gain sync is provided to synchronously change gain settings of the DDR. If the board is configured as a Sync bus master, then this is a differential LVDS output. If the Model 6216 is configured as a Sync bus slave, this signal is a differential LVDS input.

2.4 Sync Bus – Serial I/O Connector (continued)

2.4.1 Signals for Synchronizing Multiple Boards (continued)

2.4.1.5 Compatibility with Other Products' Sync Buses

At the time of this manual's publication, Pentek manufactures four devices that use the same physical connector to implement a Sync bus and Serial I/O port. These are the Models 6216 and 6210 Digital Reciver/ADCs, the Model 6211 A/D Converter, and the Model 6229 Digital Transmitter/DAC. The serial port implementations are identical across these four products. However, if you simply take a length of 36−wire ribbon cable and crimp a 36−pin insulation−displacement connector at either end, you'll be connecting the serial port transmitters to other transmitters, and the receivers to other reveivers. Such configurations are clearly to be avoided, so any required serial port interconnections will have to be made via some sort of breakout box or board, reminiscent of the RS−232 implementations that we all remember from the good(?) old days.

Cables that are intended to connect only the Sync busses of these devices can b e constructed using two or more 36−pin IDC connectors (3M part # 83036−6006 or an equivalent, Pentek part # 353.03605), and a 16−wire ribbon cable connecting pins 1 − 16 on all connectors. One should be aware, however, that there are some differences in the Sync bus implementations across these devices. The paragraphs that follow will comment on the interoperability of the Sync busses among these four products.

The Model 6210 is a Narrowband Digital Receiver and A/D converter. Its ADC stage is also identical to the Model 6216's , but it uses Intersil's HSP50214 Down−Converter instead of the Graychip GC1012 used in this product. There are several differences between the synchronizing features of these two devices, most notably that synchronization occurs on the rising edge of the sync signals on the 6210, and on the falling edge of these signals on the 6216. Thus, 6210s and 6216s CANNOT be synchronized with one another. The Model 6211 is essentially identical to the 6210, but it lacks any digital receiver stage. Nonetheless, this device also synchronizes on the rising edge of its SYNC signal, and is thus also incompatible with the 6216.

The Model 6229's Sync bus, on the other hand, is completely compatible in both directions with the 6216's. While the 6229 does not respond to either the GSYNC or ASYNC signals as a Sync bus slave, it can generate these signals as a master. Therefore, the a system involving synchronized 6216s and 6229s could be implemented with either a 6216 or a 6229 as the Sync bus master.

2.4 Sync Bus – Serial I/O Connector (continued)

2.4.2 Serial Port Signals

The signals listed in the subsections below are associated with the VIM motherboard's Serial Ports. If the Model 6216 is installed above (i. e., controlled by) Processors A & B on the VIM motherboard, then Processor A's serial port 1 is P0, and Processor B's serial port 1 is P1. If the Model 6216 is installed above VIM motherboard Processors C & D, then Processor C's serial port 1 is P0, and Processor D's serial port 1 is P1 All these signals are delivered directly from the 6210's VIM Motherboard connector to the front panel Sync Bus – Serial I/O Connector via a small series resistor (47 Ω), and are pulled up to +5 V via 8.2 kΩ on the I/O connector side of the series resistor.

2.4.2.1 P0–CLKR1, P1–CLKR1

These are the Serial Port Receive Clock Signals from the VIM motherboard.

2.4.2.2 P0–FSR1, P1–FSR1

These are the Serial Port Receive Frame Sync signals from the VIM motherboard.

2.4.2.3 P0–CLKS1, P1–CLKS1

These are the Serial Port External Clock Source signals from the VIM motherboard.

2.4.2.4 P0–DR1, P1–DR1

These are the Serial Port Receive Data signals from the VIM motherboard.

2.4.2.5 P0–CLKX1, P1–CLKX1

These are the Serial Port Transmit Clock signals from the VIM motherboard.

2.4.2.6 P0–FSX1, P1–FSX1

These are the Serial Port Transmit Frame Sync signals from the VIM motherboard.

2.4.2.7 P0–DX1, P1–DX1

These are the Serial Port Transmit Data signals from the VIM motherboard.

2.4 Sync Bus/Serial I/O Connector (continued)

2.4.3 TTL−$\overline{\text{SYNC}}$

This signal is a single−ended, TTL compatible sync input. Those sync signals that are not disabled by the Sync Mask bits in the Control Register will be created in slave units on the rising edge of this signal. The signal applied to this input must be a logic high in its quiescent state, and the negative−going sync pulse applied here must be at least two sample clock periods wide. If left unconnected, this pin is pulled to a high logic level.

2.5 Installing the Model 6216 on a VIM Motherboard

Pentek's VIM motherboard ship with two blank panels where optional VIM modules, such as the Model 6216, can be installed. This section provides directions for removing blank panels, and installing the Model 6216, or other VIM modules.

CAUTION

Perform all assembly steps at an anti–static workstation.

Tools required for all procedures:

1) #1 philips screwdriver

2) flat–blade screwdriver (blade width 5/16–in. or less)

2.5.1 Preparing the VIM Module for Installation

1) Remove the blank insert from the position in which your VIM module will be installed by removing the two countersunk philips screws from the top & bottom of the insert.

2) Remove the front panel from the VIM module by removing the two countersunk philips screws from the top & bottom of the panel.

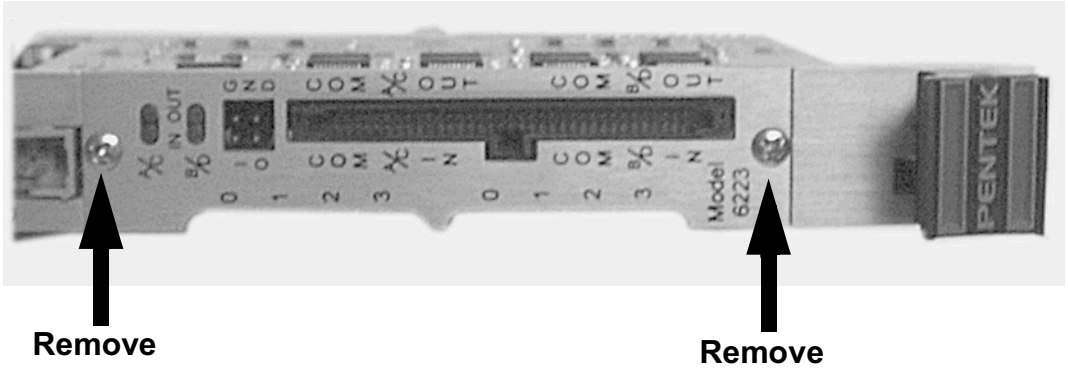


Figure 2–6: VIM Module Countersunk Screws

2.5 Installing the Model 6216 on a VIM Motherboard (continued)

2.5.1 Preparing the VIM Module for Installation (continued)

3) Remove the two shipping brackets that were used to mount the front panel to the VIM module, by removing the two pan−head philips screws from the solder side of the VIM module. These brackets may be discarded or saved to use to store the panel on the VIM module if and when it is removed from the VIM motherboard.

4) At the rear of the VIM module, on the component side, is a nylon spacer with a nylon screw threaded into it.

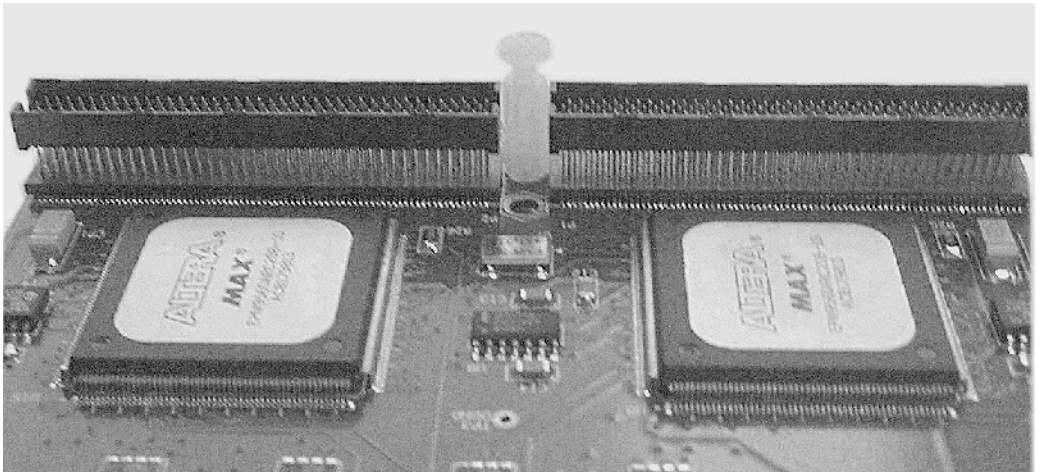


Figure 2−7: VIM Module Nylon Spacer

a) Remove the nylon screw threaded into the spacer from the component side. Set this screw aside, as it will be used when installing the VIM module on the motherboard.

b) The spacer should be installed in the hole BEHIND the VIM connectors (i. e., farthest from the front panel's location). If the spacer is installed in the front hole, reposition it by removing the nylon screw on the SOLDER side of the VIM module, and threading it back into the spacer through the rear−most hole.

2.5 Installing the Model 6216 on a VIM Motherboard (continued)

2.5.2 Installing the VIM Module on the VIM Motherboard

1) With the VIM motherboard's component side (the one with the mezzanine connectors) up, and the connectors on the VIM module face down, align the P1 and P2 connectors on the VIM module with the pair of connectors corresponding to the desired location on the motherboard (e. g., P11 and P14 at the top of the 4290, or P8 and P4, at the bottom).

2) **GENTLY but firmly**, press down on the areas of the VIM module opposite both connectors, to fully seat the VIM module's connectors in the motherboard's. If you meet with significant resistance, check the connector alignment. Misalignment can cause bent pins or break connector housings, so **NEVER APPLY EXCESSIVE FORCE**.

3) After seating the connectors, secure the front of the VIM module to the motherboard by threading two pan−head philips screws through the holes in the front of the solder side of the VIM module into the threaded holes in motherboard's panel brackets.

4) Turn the assembly over, such that the mezzanine board is on the work surface and the solder side of the VIM motherboard is face up.

5) Secure the rear of the VIM module to the motherboard using the nylon screw you removed earlier through the rear mounting hole on the motherboard, threaded into the nylon spacer on the VIM module.

6) Attach the VIM module's front panel to the motherboard using two countersunk philips screws, passed through the holes at the top and bottom of the VIM panel and threading them into the threaded holes in the motherboard's panel brackets.

7) If an additional VIM module is to be installed, repeat this procedure in the other module location on the motherboard.

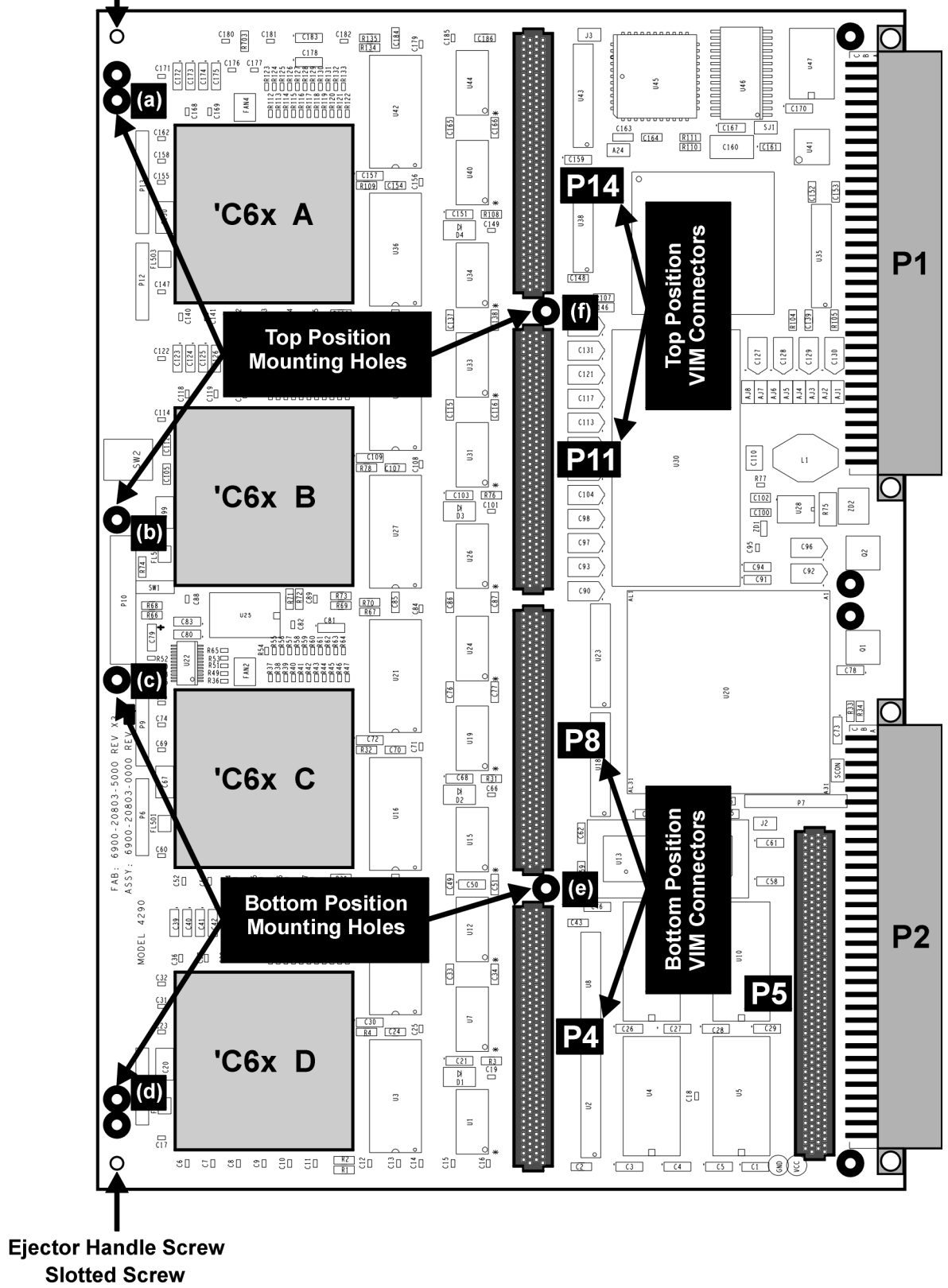


Figure 2–8: Model 4290 VIM Motherboard – Connectors & Mounting Holes

Chapter 3: Memory Map and Register Descriptions

3.1 Overview

This section covers access to the Model 6216 from the VIM motherboard. Memory maps to VIM module resources are given from the motherboard processor's viewpoint, and details are provided describing the use of each resource.

3.2 Model 6216 Memory Map

Table 3–1, below, provides a complete memory map for the Model 6216 mezzanine board. The subsections that follow the table provide detailed information about each register.

Table 3–1: Model 6216 Memory Map

'C6X Address	Register Description	Mnemonic	Access	Additional Info
0x0032 0000	ID EEPROM Readout	EEPROM	R. O.	Appendix E
0x0032 0004 – 0x0032 001C	Reserved	—	N/A	N/A
0x0032 0020*	Control Register*	CONTROL	R/W	Section 3.4
0x0032 0024*	Master Clock Divider*	MCLKDIV	R/W	Section 3.5
0x0032 0028	BIFO Decimation Register	BIFODIV	R/W	Section 3.6
0x0032 002C	Programmable Gain Amplifier	GAIN	R/W	Section 3.7
0x0032 0030	Data Format / Signal Path Register	DATA_CONTROL	R/W	Section 3.8
0x0032 0034	Reserved	—	N/A	N/A
0x0032 0038	Serial Port 0 Connection Register	SPORT_CONTROL	R/W	Section 3.9
0x0032 003C*	Sync Generate Register*	SYNC	R/W	Section 3.10
0x0032 0040	DDR Frequency Byte 0	Freq_Byte_0 (LSB)	R/W	Section 3.11.1
0x0032 0044	DDR Frequency Byte 1	Freq_Byte_1	R/W	
0x0032 0048	DDR Frequency Byte 2	Freq_Byte_2	R/W	
0x0032 004C	DDR Frequency Byte 3	Freq_Byte_3 (MSB)	R/W	
0x0032 0050	DDR Sync Mode Register	SYNC_MODE	R/W	Section 3.11.2
0x0032 0054	DDR Filter Mode Register	FILTER_MODE	R/W	Section 3.11.3
0x0032 0058	DDR Gain Fraction	GAIN_CONTROL	R/W	Section 3.11.4
0x0032 005C	DDR Gain Exponent	GAIN_EXPONENT	R/W	
0x0032 0060	DDR Output Mode Register	OUTPUT_MODE	R/W	Section 3.11.5
0x0032 0064	DDR Output Status Register	OUTPUT_STATUS	R/W	Section 3.11.6
0x0032 0068	DDR One–Shot Register	ONE_SHOT	W. O.	Section 3.11.7
0x0032 006C	DDR Checksum Register	CHECKSUM	R. O.	Section 3.11.8
0x0032 0070	DDR I Output Byte 0	I_OUT_BYTE_0	R. O.	Section 3.11.9
0x0032 0074	DDR I Output Byte 1	I_OUT_BYTE_1	R. O.	
0x0032 0078	DDR Q Output Byte 0	Q_OUT_BYTE_0	R. O.	
0x0032 007C	DDR Q Output Byte 1	Q_OUT_BYTE_1	R. O.	

* – These registers are accessible only to Processor A or Processor C on the VIM motherboard, depending upon the position in which the VIM module is installed.

3.3 ID EEPROM Readout Register – R. O. @ 'C6x Address 0x0032 0000

The format for the code stored by Pentek in this EEPROM is listed in Appendix E of this manual. The format is provided for VIM module designers. Neither the format nor this register is intended for general use.

3.4 Control Register – R/W @ 'C6x Address 0x0032 0020

The Control Register allows you to configure the Model 6216 as a master or slave on the sync bus and to toggle the on–board sync bus termination. It also provides a bit that selects the source of the clock as internal or external, a bit to divide the the frequency of the signal that will be used as the PROCCLK for the DDR by 2 (this is necessary if that signal's frequency exceeds 55 MHz), and a bit to synchronize the operation of the BIFO on the motherboard. All bits in the Control Register default to the logic '0' state. The Control Register is accessible only to Processor A or Processor C on the VIM mother–board, depending upon the position in which the module is installed. Neither Proces–sor B nor Processor D on a VIM motherboard can ever access this register. Table 3–2, below, shows the contents of the Model 6216's Control Register. The subsections that begin below the table give detailed descriptions of the bits in this register.

Table 3–2: Model 6216 – Control Register – R/W @ 'C6x Address 0x0032 0020

Bit #	D31 – D8							
BitName	Reserved							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Reserved	GSYNC _Mask	ASYNC _Mask	SSYNC _Mask	BIFO_ Disable	Ext_Clk _Enable	Term_ Enable	Master/ $\overline{\text{Slave}}$
Bit Function	Write '0' Mask on Reads	0 = Disabled (Masked) 1 = Enabled			1 = Disable 0 = Enable	1 = Ext Clk 0 = Crystal	1 = Term 0 = No Term	1 = Master 0 = Slave
All bits default to the logic '0' state at power–up and resets.								

3.4.1 GSYNC Mask – Bit D6

This bit is used to enable or disable the generation of the GSYNC pulse. When this bit is cleared to the logic '0' state (its default condition), GSYNC genera–tion is enabled, and writing to the Sync Generate Register (see Section 3.10) will create a GSYNC pulse. When this bit is set to the logic '1' state, GSYNC generation is disabled, and writing the Sync Generate register will not create a GSYNC pulse.

3.4 Control Register (continued)

3.4.2 ASYNC Mask – Bit D5

This bit is used to enable or disable the generation of the ASYNC pulse. When this bit is cleared to the logic '0' state (its default condition), ASYNC generation is enabled, and writing to the Sync Generate Register (see Section 3.10) will create an ASYNC pulse. When this bit is set to the logic '1' state, ASYNC generation is disabled, and writing the Sync Generate register will not create an ASYNC pulse.

3.4.3 SSYNC Mask – Bit D4

This bit is used to enable or disable the generation of the SSYNC pulse. When this bit is cleared to the logic '0' state (its default condition), SSYNC generation is enabled, and writing to the Sync Generate Register (see Section 3.10) will create an SSYNC pulse. When this bit is set to the logic '1' state, SSYNC generation is disabled, and writing the Sync Generate register will not create an SSYNC pulse.

3.4.4 BIFO Disable – Bit D3

This bit is used to synchronize the mezzanine BIFOs on VIM motherboards across multiple channels. This is accomplished by first setting this bit on each channel to be synchronized to the logic '1' state, then resetting the motherboard's BIFO. When this bit is subsequently cleared to the logic '0' state (its default condition), no data is written to the BIFO until the next rising edge of the SSYNC signal (see Section 2.4.1.3, on page 21). In this manner, data acquisition in all channels connected to the Sync Bus is started simultaneously. This bit **MUST** be cleared to the logic '0' state for normal operation.

3.4.5 External Clock Enable – Bit D2

This bit determines which signal will drive the Model 6216's Master Clock Divider (see Section 3.5). When this bit is set to the logic '1' state, the signal applied to the front panel **EXT CLK** connector is selected. When this bit is cleared to the logic '0' state (its default condition), the on–board, 64 MHz crystal oscillator is selected.

3.4.6 Termination Enable – Bit D1

This bit is set to the logic '1' state to connect termination resistors to the Model 6216's Sync bus. This should be done ONLY on the slave Model 6216 that is at the opposite end of the Sync Bus from the Sync Bus master, or on a stand–alone device that is not connected to the external Sync Bus. On all other devices, clear this bit to the logic '0' state (the default), to disconnect the terminators.

3.4 Control Register (continued)

3.4.7 Master / Slave – Bit D0

Set this bit to the logic '1' state to configure a Model 6216 as a Sync bus master. This bit must also be set to the logic '1' state on any Model 6216 that will not be connected to a Sync Bus. To configure a Model 6216 as a Sync Bus slave, clear this bit to the logic '0' state (its default condition).

3.5 Master Clock Divider – R/W @ 'C6x Address 0x0032 0024

The Master Clock Divider register divides the master clock signal (provided by the on–card, 64 MHz oscillator or the front panel **EXT CLK** connector, see Section 3.4.5) by the quantity written to the lower byte (D7 – D0) of this register, plus one. This register should **ONLY** be written with all zeros (the register's default condition) or odd numbers, such that the actual number that the master clock frequency is divided by is either 1 or an even number. The output of this divider is applied to the ENCODE inputs of the AD6640 A/D converter, and to the front end of the HSP50214 DDR. For example, when the low byte of this register contains all zeros (their default condition), the master clock signal will be passed to the A/D's ENCODE inputs and the DDR front end unaltered (i. e., divided by 1). However, if the internal oscillator is selected, and the low byte of this register contains the quantity 7, the A/D's ENCODE frequency (and the DDR's front–end processing frequency) will be 8 MHz (64 MHz ÷(7+1)).

Like the Control Register, the Master Clock Divider is only accessible from Processor A or Processor C on the VIM motherboard, depending upon the position in which the module is installed. Neither Processor B nor Processor D on a VIM motherboard can ever access this register. Table 3–3, below, illustrates the contents of the Model 6216's Master Clock Divider Register.

Table 3–3: Model 6216 – Master Clock Divider – R/W @ 'C6x Address 0x0032 0024

Bit #	**D31 – D8**							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	MSB –––––––––––––––––––––––––––––––––––––LSB							
Function	Main Clock is divided by the quantity in this field +1 to produce the Master clock for the ADC & DDR. This field MUST be written with either an odd number, or zero.							
All bits default to the logic '0' state at power–up and resets.								

3.6 BIFO Decimation Register – R/W @ 'C6x address 0x0032 0028

The Master Clock, described in Section 3.5, on the previous page, may be further divided to create the Write Enable signal for the VIM motherboard's mezzanine BIFO. 8 bits are provided for this frequency division, in this register. Each channel (i. e., each processor on the motherboard that can access this module) has its own unique version of this register, to allow the two channels to operate at different rates. This divider works in a manner similar to the the Master Clock Divider. The BIFO Write Rate is equal to the Master Clock rate divided by the 8–bit value in this register plus one. Also, the valid data values for this 8–bit field are restricted to odd numbers (which will result in even divisors) and zero (which gives a divisor of one, and is the register's default condition). Table 3–4, below, shows the contents of this register.

Table 3–4: Model 6216 – Motherboard BIFO Decimation Register – R/W @ 'C6x Address 0x0032 0028

Bit #	**D31 – D8**							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	MSB– –LSB							
Function	BIFO Write Rate divisor							
All bits default to the logic '0' state at power–up and resets. The Reference Clock is divided by the quantity in this register +1 to produce the Write Enable for the Motherboard's BIFO. This 8–bit field MUST be written with either an odd number, or zero. All bits default to the logic '0' state at power–up and resets.								

3.7 Programmable Gain Amplifier (GAIN) – R/W @ 'C6x Address 0x0032 002C

This register controls the Model 6216's Pragrammable–Gain Amplifier (PGAmp), shown in Figure 1–1, on page 9. This register is only functional if the PGAmp has not been bypassed (see Section 3.8.3). The amplifier is the Analog Devices Model AD603, and its gain control voltage is provided by a D/A converter, specifically the LTC1451, from Linear Technology. Appendix C of this manual is the data sheet for the amplifier, and Appendix D contains the data sheet for the D/A. Both provide complete block diagrams, specifications and other pertinent information. The DAC is programmed by serially shifting in a 12–bit data word. As shown in Table 3–5, below, the 3 active bits in this register provide a chip select for the DAC, a bit to toggle to create the serial shift clock, and a data bit. When reset, and when powered on, all 3 of these bits default to the logic '0' state.

Table 3–5: Model 6216 – Programmable Gain Amplifier Register – R/W @ 'C6x 0x0032 002C

Bit #	D31 – D3	D2	D1	D0
Bit Name	Reserved	Chip_ Select	Data_ In	Serial _Clock
Bit Function	Write with Zeros, Mask when Reading	1 = Not Selected 0 = Load Data	Data to be shifted	Toggle for shift clock
All bits default to the logic '0' state at power–up and resets.				

3.7.1 Loading the 12–bit Gain Control Word

The Gain Control Register is used to serially load the 12–bit gain control word (GCW) into the LTC1451 DAC, which provides a gain control voltage for the input amplifier. The gain control word is loaded into the DAC, MSB first, by first clearing the Chip Select bit (D2) to the logic '0' state, then toggling the Serial_Clock bit (D0) for each bit of the gain control word, stored in this register's Input_Data bit, D1. The bits that comprise the gain control word are latched on the rising edge (i. e., the logic '1' to logic '0' transition) of the Serial_Clock bit. The DAC's output voltage is updated on the rising edge (i. e., the logic '0' to logic '1' transition) of the Chip_Select bit. The complete sequence for writing the 12–bit word to the DAC involves 26 write operations to this register. A complete write sequence is shown in Table 3–7, at the bottom of the next page.

A sample program for loading the control word into the DAC is provided in the ReadyFlow Board Support Package for the Model 6216. The Gain Control Word for 0 dB gain is 250 (decimal), or 0xFA (hex). The gain control resolution is approximately 0.04 dB per LSB of the control word. Thus, incrementing or decremeting the control word by 25 decimal changes the gain of the amplifier by 1 dB. Table 3–6, at the top of the next page, shows the Gain Control Word value that shoud be loaded into the LTC1451 for full scale input amplitudes of +10 dBm to –20 dBm (or with option 102, 0 to –30 dBm) in 10 dBm increments.

When calculating the required gain for your application, remember to take into account the input low–pass filter, which may have an insertion loss of up to 5 dB.

3.7 Programmable Amplifier Gain (continued)

3.7.1 Loading the 12–bit Gain Control Word (continued)

Table 3–6: Model 6216 – Gain Control Word vs. Full Scale Input Amplitude

Gain Control Word		Full Scale Input Amplitude (Standard)	Full Scale Input Amplitude (Option 102)
Decimal	Hex		
250	0x00FA	10 dBm	0 dBm
500	0x01F4	0 dBm	–10 dBm
750	0x02EE	–10 dBm	–20 dBm
1000	0x03E8	–20 dBm	–30 dBm

NOTE: The values given in this table **DO NOT** take into account the insertion loss of the low–pass input filter, which may be as high as 5 dB.

Table 3–7: Model 6216 – Sequence for Loading Gain Control Word

Write #	Description	D2	D1	D0
–	Initial state. Chip select asserted (default power–up state).	0	0	0
1	De–assert chip select.	1	0	0
2	Assert chip select & setup bit 11, MSB of the GCW.	0	(GCW bit 11)	0
3	Latch bit 11, MSB of the GCW.	0	(GCW bit 11)	1
4	Setup bit 10 of the GCW.	0	(GCW bit 10)	0
5	Latch bit 10 of the GCW.	0	(GCW bit 10)	1
6	Setup bit 09 of the GCW.	0	(GCW bit 9)	0
7	Latch bit 09 of the GCW.	0	(GCW bit 9)	1
8	Setup bit 08 of the GCW.	0	(GCW bit 8)	0
9	Latch bit 08 of the GCW.	0	(GCW bit 8)	1
10	Setup bit 07 of the GCW.	0	(GCW bit 7)	0
11	Latch bit 07 of the GCW.	0	(GCW bit 7)	1
12	Setup bit 06 of the GCW.	0	(GCW bit 6)	0
13	Latch bit 06 of the GCW.	0	(GCW bit 6)	1
14	Setup bit 05 of the GCW.	0	(GCW bit 5)	0
15	Latch bit 05 of the GCW.	0	(GCW bit 5)	1
16	Setup bit 04 of the GCW.	0	(GCW bit 4)	0
17	Latch bit 04 of the GCW.	0	(GCW bit 4)	1
18	Setup bit 03 of the GCW.	0	(GCW bit 3)	0
19	Latch bit 03 of the GCW.	0	(GCW bit 3)	1
20	Setup bit 02 of the GCW.	0	(GCW bit 2)	0
21	Latch bit 02 of the GCW.	0	(GCW bit 2)	1
22	Setup bit 01 of the GCW.	0	(GCW bit 1)	0
23	Latch bit 01 of the GCW.	0	(GCW bit 1)	1
24	Setup bit 00, LSB of the GCW.	0	(GCW bit 0)	0
25	Latch bit 00, LSB of the GCW.	0	(GCW bit 0)	1
26	De–assert chip select.	1	0	0

3.8 Data Format / Signal Path Register (DATA) – R/W @ 'C6x Address 0x0032 0030

Each Motherboard Processor that can access this module has a separate version of this register, which contains four active bits. There are bits used to determine whether the data delivered to the motherboard is from the A/D or the DDR and whether the programmable gain amplifier and low–pass, anti aliasing filter are in the signal path before the A/D. The other two bits determine whether or not the data applied to the DDR input is pre–decimated by a factor of two, and (if the DDR is bypassed) whether or not the A/D's output data is packed. Table 3–8, below, shows the layout of the Model 6216's Data Format/Signal Path Register, and the subsections that begin below the table describe how the bits are used.

Table 3–8: Model 6216 – Data Format / Signal Path Register – R/W @ 'C6x 0x0032 0030

Bit #	D 3 1 – D 4	D3	D2	D1	D0
Bit Name	Reserved	DDR_In_ Dec_x2	Pack_ Mode	LPF/PGAmp Bypass	DDR_ Bypass
Bit Function	Write with Zeros, Mask when Reading	1 = Decimate 0 = No Dec	1 = Pack 0 = No Pack	1 = Bypass 0 = Use	1 = Use DDR 0 = A/D Only
All bits default to the logic '0' state at power–up and resets.					

3.8.1 Decimate DDR Input by 2 – Bit D3

When this bit is set to the logic '1' state, the data delivered to the DDR by the A/D converter is decimated by a factor of 2 (i. e., all even–numbered samples are dropped). This is required if the HSP50214's internal Cascaded Integrator–Comb (CIC) filter is bypassed (i. e., if bit D6 in the Control Word 0 Register in the DDR is set to the logic '1' state). When this bit is cleared to the logic '0' state (its default condition), all data convetred by the A/D is delivered to the DDR (i. e., no samples are dropped).

3.8.2 Pack Mode – Bit D2

This bit is functional ONLY if the DDR is bypassed, and the 6216 is delivering raw A/D data to the VIM motherboard (i. e., if the D0 bit in this register is cleared to the logic '0' state). If the preceding statement is true, then when this bit is set to the logic '1' state, each 32–bit longword delivered to the motherboard's BIFO by the 6216's A/D will contain two consecutive 12–bit data samples, left–justified in each 16–bit field. In this case, the low word of each longword contains the earlier sample.

If the DDR is bypassed (D0 in this register contains a '0') and this bit is cleared to the logic '0' state (the default condition), then each 32–bit word delivered to the VIM motherboard by the 6216 will contain a single 12–bit A/D sample, left justified in the lower 16–bit word.

3.8 Data Format / Signal Path Register (continued)

3.8.2 Pack Mode (continued)

If the DDR is in the 6216's data path between the A/D and the VIM mother–board (i. e., if D0 in this register is set to the logic '1' state), then the state of this bit is ignored, and the operating mode of the HSP50214 determines the output data format (see Appendix A, the GC1012A data sheet, for details about setting the operating mode of the DDR). If the DDR operates in Com–plex mode, each 32–bit word delivered from the 6216's DDR to the mother–board BIFO contains a 16–bit Q (quadrature or imaginary) sample in the upper word (D31 – D16), and a 16 bit I (in–phase or real) sample in the lower word (D15 – D0). If the DDR operates in Real–Only mode, each 32–bit word delivered from the 6216's DDR to the motherboard BIFO contains only one 16–bit I sample, in the low word. In all unpacked formats, the data in the upper word is indeterminate.

All data delivered to the motherboard BIFO by the 6216 is in signed 2's com–plement format, with the MSB of the data sample set to the logic '1' state to indicate negative data values. Table 3–9, below, illustrates the available for–mats for output data from the Model 6216.

Table 3–9: Model 6216 – Output Data to Motherboard BIFO – Packing Formats

Packed A/D Data (D2 = 1, D0 = 0)						
O/P Word #	**D31 – – – – – – – – – – – – – D20**		**D19 - D16**	**D15 – – – – – – – – – – – – – D4**		**D3 - D0**
1	(MSB)	A/D Sample #2 (LSB)	? ?	(MSB)	A/D Sample #1 (LSB)	? ?
2	(MSB)	A/D Sample #4 (LSB)	? ?	(MSB)	A/D Sample #3 (LSB)	? ?
Unpacked A/D Data (D2 = 0, D0 = 0)						
O/P Word #	**D31 – – – – – – – – – – – – – – – – – – D16**			**D15 – – – – – – – – – – – – – D4**		**D3 - D0**
1	Indeterminate			(MSB)	A/D Sample #1 (LSB)	??
2	Indeterminate			(MSB)	A/D Sample #2 (LSB)	??
Complex DDR Data (D2 = X, D0 = 1)						
O/P Word #	**D31 – – – – – – – – – – – – – – – – – – D16**			**D15 – – – – – – – – – – – – – – – – – – D0**		
1	(MSB)	DDR Q Sample #1 (LSB)		(MSB)	DDR I Sample #1	(LSB)
2	(MSB)	DDR Q Sample #2 (LSB)		(MSB)	DDR I Sample #2	(LSB)
Real DDR Data (D2 = X, D0 = 1)						
O/P Word #	**D31 – – – – – – – – – – – – – – – – – – D16**			**D15 – – – – – – – – – – – – – – – – – – D0**		
1	Indeterminate			(MSB)	DDR I Sample #1	(LSB)
2	Indeterminate			(MSB)	DDR I Sample #2	(LSB)
?? = Indeterminate, X = Don't Care						

3.8 Data Format / Signal Path Register (continued)

3.8.2 Pack Mode (continued)

When the DDR's are byassed, output data by the Model 6216's A/D converters is encoded in true 12–bit 2's complement format, with the remaining 4 bits of the 16–bit word in which the sample resides indeterminate. The MSB (D15) is used as a sign bit and indicates a negative input voltage when set to the logic '1' state. The maximum negative input voltage (–1 V_{DC} for the standard input signal range) results in an output data code of 1000 0000 0000 xxxx (0x800x), while an input exactly one step above half–scale (≅ + 490 mV_{DC}) produces an output code of all 12 active bits cleared to the logic '0' state. A full–scale positive input voltage (+1 V_{DC}) produces an output data code of 0111 1111 1111 xxxx (0x7FFx). Table 3–10, below, provides the output data coding scheme used by the Model 6211.

Table 3–10: Model 6216 – A/D Output Data Coding

Step (Decimal)	Input Voltage (DC, Nominal)	Binary Output Code (D15 – D0)	Hexadecimal Output Code
0	–1.00000 V	1000 0000 0000 xxxx	0x800x
1	–0.99951 V	1000 0000 0001 xxxx	0x801x
2	–0.99902 V	1000 0000 0010 xxxx	0x802x
⋮	⋮	⋮	⋮
2046	–0.00049 V	1111 1111 1110 xxxx	0xFFEx
2047	0.00000 V	1111 1111 1111 xxxx	0xFFFx
2048	+0.00049 V	0000 0000 0000 xxxx	0x000x
2049	+0.00098 V	0000 0000 0001 xxxx	0x001x
⋮	⋮	⋮	⋮
4093	+0.99902 V	0111 1111 1101 xxxx	0x7FDx
4094	+0.99951 V	0111 1111 1110 xxxx	0x7FEx
4095	+1.00000 V	0111 1111 1111 xxxx	0x7FFx
x = Indeterminate			

3.8.3 Programmable–Gain Amplifier & Low–Pass Filter Bypass – Bit D1

When this bit is set to the logic '1' state, the analog input signal is routed around the programmable–gain amplifier and the low–pass, anti aliasing filter. This allows the full bandwidth of the input signal to be delivered to the A/D converter, which is necessary in undersampling applications. For applications where undersampling is not required and it is desirable to eliminate frequency components above the Nyquist limit that may be present in the input signal, clear this bit to the logic '0' state to place the low–pass filter and programmable–gain amplifier in the signal path.

3.8 Data Format / Signal Path Register (continued)

3.8.4 DDR Bypass – Bit D0

This bit allows the Model 6216 to function as a simple A/D converter, by routing the output data directly to the BIFO on the VIM motherboard. A/D data will bypass the Intersil HSP50214 DDR chip when this bit is cleared to the logic '0' state (its default condition). When this bit is set to the logic '1' state, the DDR is placed in the data path between the A/D converter and the moth–erboard's BIFO, and all of the Model 6216's digital receiver functions are available.

3.9 Serial Port 0 Connection Register (SPORT) – R/W @ 'C6x Address 0x0032 0038

The Serial Port 0 Connection Register (SPORT) determines whether or not the receive section of the controlling motherboard processor's serial port 0 is connected to the transmit section of the other processor's serial Port 0. Each processor on the VIM motherboard that can access a given 6216 has a separate version of this register, whose power–up default state is both bits cleared to the logic '0' state.

Figure 1–1, on page 9 contains the block diagram of the Model 6216 and shows the only serial connection possible using this register. Table 3–11, below, shows the register's layout & summarizes the function of its lone bit–field. The connection made by setting both of the bits in this field is defined in more detail in the subsection below the table.

Table 3–11: Model 6216 – Serial Port Connection Register – R/W @ 'C6x 0x0032 0038

Bit #	D31 – D2	D1	D0
Bit Name	Reserved	SPort_Source_1	SPort_Source_0
Bit Function	Write with Zeros, Mask when Reading	1, 1 = Other Processor 1, 0 = Reserved*	0, 1 = Reserved* 0, 0 = Not Connected

All bits default to the logic '0' state at power–up and resets.
* – **DO NOT USE** these settings on the Model 6216

3.9.1 The Other Processor's Serial Port 0 Transmit Section (D1 = 1, D0 = 1)

When a processor on the VIM motherboard sets both bits in this register to the logic '1' state, the receiver portion of that processor's Serial Port 0 will be con–nected to the transmit section other processor's Serial Port 0.

3.9 Serial Port 0 Connection Register (continued)

3.9.2 Reserved Settings (D1 = 1 , D0 = 0 and D1 = 0, D0 =1)

The bits in this field should **ALWAYS** be in identical states. Configurations in which these 2 bits are in opposite states are undefined on the Model 6216, and should therefore be avoided.

3.9.3 Not Connected (D1 = 0, D0 = 0)

When a processor on the VIM motherboard clears both bits in this register to the logic '0' state, the receiver section of that processor's Serial Port 0 is not connected to any other device.

3.10 SYNC Generate Register (SYNC) – R/W @ 'C6x Address 0x0032 003C

Any write operation to this register will cause the generation of any of the 3 Sync pulses (GSYNC, ASYNC, SSYNC) that are not masked by their respective bits in the 6216's Control Register (see Sections 3.4.1, 3.4.2, and 3.4.3). The data associated with the write operation is neither used nor stored and is therefore trivial. The next rising clock edge after the Sync pulses have been generated will clear the register, which will cause reads of this address to return a '0'. In the interval between the write operation (i. e., the Sync request) and the clock edge that clears the register, reads of this address will return a non−zero value. Thus, this register may be polled by application software to determine when the Sync generate operation has been completed.

This register is accessible only to Processor A or Processor C on the VIM motherboard, depending upon the position in which the module is installed. Neither Processor B nor Processor D on a VIM motherboard can ever access this register.

3.11 Processor Interface to the Graychip GC1012A DDR

The subsections that follow summarize the contents of the 16 registers within the GC1012A DDR chip that can be accessed by the processors on the VIM motherboard. Complete descriptions of these registers can be found in Appendix A of this manual, the GC1012A Data Sheet.

3.11.1 DDR Frequency Registers – R/W @ 'C6x Addresses 0x0032 0040, 0x0032 0044, 0x0032 0048 and 0x0032 004C

These four registers store the 28 bit frequency tuning word for the GC1012A. Bit 0 (i. e., D0 in Byte 0) is the LSB, and bit 27 (D3 in Byte 3) is the MSB. These registers are illustrated in Tables 3–12 – 3–15, on the next page. The value of the frequency word (FREQ) written to these registers tu tune the GC1012A to a desired frequency (F) is calculated according to the following equation:

$$FREQ = 2^{28}\ F/(\text{clock rate})$$

3.11 Processor Interface to the Graychip GC1012A DDR (continued)

3.11.1 DDR Frequency Registers (continued)

Table 3–12: Model 6216 – DDR Frequency, Byte 0 – R/W @ 'C6x Address 0x0032 0040								
Bit #	**D31 – D8**							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	FREQ_7	FREQ_6	FREQ_5	FREQ_4	FREQ_3	FREQ_2	FREQ_1	FREQ_0
Function	Least Significant Byte of the GC1012A's 28–bit frequency word (FREQ)							
All bits default to the logic '0' state at power–up and resets.								

Table 3–13: Model 6216 – DDR Frequency, Byte 1 – R/W @ 'C6x Address 0x0032 0044								
Bit #	**D31 – D8**							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	FREQ_15	FREQ_14	FREQ_13	FREQ_12	FREQ_11	FREQ_10	FREQ_9	FREQ_8
Function	2nd Byte of the GC1012A's 28–bit frequency word (FREQ)							
All bits default to the logic '0' state at power–up and resets.								

Table 3–14: Model 6216 – DDR Frequency, Byte 2 – R/W @ 'C6x Address 0x0032 0048								
Bit #	**D31 – D8**							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	FREQ_23	FREQ_22	FREQ_21	FREQ_20	FREQ_19	FREQ_18	FREQ_17	FREQ_16
Function	3rd Byte of the GC1012A's 28–bit frequency word (FREQ)							
All bits default to the logic '0' state at power–up and resets.								

Table 3–15: Model 6216 – DDR Frequency, Byte 3 – R/W @ 'C6x Address 0x0032 004C				
Bit #	**D31 – D4**			
Name	Not Used			
Function	Write with 0's, Mask when Reading			
Bit #	**D3**	**D2**	**D1**	**D0**
Name	FREQ_27	FREQ_26	FREQ_25	FREQ_24
Function	Four Most Significant Bits of the GC1012A's 28–bit frequency word (FREQ)			
All bits default to the logic '0' state at power–up and resets.				

3.11 Processor Interface to the Graychip GC1012A DDR (continued)

3.11.2 DDR Sync Mode Register – R/W @ 'C6x Address 0x0032 0050

The GC1012A's Sync Mode register controls the action of the SSYNC and ASYNC strobes, and how they affect the chip's internal timers, counters, and accumulators. A complete description of these bits can be found in Section 3.2 of the GC1012A Data Sheet, which includes a block diagram to illustrate their operation. Table 3–16, below, summarizes the contents of the Sync Mode Register.

Table 3–16: Model 6216 – DDR Sync Mode Register – R/W @ 'C6x Address 0x0032 0050

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	SS_MUX	TEST	SS_DIAG	AS_FREQ	LD_FREQ	AS_MUX	AS_ON	SS_OFF
Function	1 = SS 0 = TC	1 = 2^8 0 = 2^{20}	1 = Enable 0 = Disable	1 = Sync Load 0 = Async Load	1 = Load 0 = Hold	1 = SS 0 = AS	1 = Enable 0 = Disable	1 = Disable 0 = Enable
All bits default to the logic '0' state at power–up and resets.								

3.11.3 DDR Filter Mode Register – R/W @ 'C6x Address 0x0032 0054

The Filter Mode Register controls filtering, output formatting and the diagnostic input mode. A complete description of these bits can be found in Section 3.3 of the GC1012A Data Sheet, which includes a figure illustrating the combined effects of the REAL, OFFSET and FLIP bits. Table 3–17, below, summarizes the contents of the Filter Mode Register.

Table 3–17: Model 6216 – DDR Filter Mode Register – R/W @ 'C6x Address 0x0032 0054

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	DIAG	FLIP	OFFSET	REAL	N/U	DEC_2	DEC_1	DEC_0
Function	1 =Enable 0 = Disable	1 = Flip* 0 = No Flip	1 = Offset 0 = No Offset	1 = Real Output 0 = Complex Output	Write with '0', Mask on Reads	1,1,1 = FCK/64 1,1,0 = FCK/32 1,0,1 = FCK/16 1,0,0 = FCK/8 The above values are the Complex output rate for a given clock rate. The Real output rate for a given decimation setting is 2x the Complex rate, and DEC settings of 0 or 1 are undefined for Real output.	0,1,1 = FCK/4 0,1,0 = FCK/2 0,0,1 = FCK 0,0,0 = FCK	
All bits default to the logic '0' state at power–up and resets. * – When the FLIP bit is setto the logic '1' state, the Q output of the DDR will be inverted.								

3.11 Processor Interface to the Graychip GC1012A DDR (continued)

3.11.4 DDR Gain Control Registers – R/W @ 'C6x Addresses 0x0032 0058 and 0x0032 005C

These two registers are used to set the output gain of the GC1012A. The gain of the device is calculated according to the following formula:

$$GAIN = 2^{(S-B)} \times (1+F/256)$$

where **F** is the value stored in the 8–bit Gain Fraction Register, **S** is the value stored in he Gain Exponent Register's 4 LSBs (the 4 MSBs are used for other control and status functions), and **B** is the Base Gain setting, a function of the decimation mode. These registers are summarized in Tables 3–18 and 3–19, below. For further details, please refer to Section 3.4 of the GC1012A Data Sheet.

Table 3–18: Model 6216 – DDR Gain Fraction Register – R/W @ 'C6x Address 0x0032 0058

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	F7	F6	F5	F4	F3	F2	F1	F0
Function	The 8–bit Gain Fraction, F							
All bits default to the logic '0' state at power–up and resets.								

Table 3–19: Model 6216 – DDR Gain Exponent Register – R/W @ 'C6x Address 0x0032 005C

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7***	**D6***	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	KA_MODE	KA_CK	KA_DISABLE	GS_MODE	S3	S2	S1	S0
Function	1 = Power Down 0 = Active	Keep–Alive Clock Monitor (~ 1 kHz)	1 = Disable 0 = Enable	1 = Sync 0 = Async	The 4–bit Gain Exponent, S			
All bits default to the logic '0' state at power–up and resets. * – These bits are Read Only								

3.11 Processor Interface to the Graychip GC1012A DDR (continued)

3.11.5 DDR Output Mode Register – R/W @ 'C6x Address 0x0032 0060

The GC1012A's Output Mode Register controls the device's Output Format. Its content is summarized in Table 3–20, below. For a detailed description of these bits, please refer to Section 3.5 of the GC1012A Data Sheet, in Appendix A.

Table 3–20: Model 6216 – DDR Output Mode Register – R/W @ 'C6x Address 0x0032 0060

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7***	**D6***	**D5***	**D4***	**D3**	**D2**	**D1**	**D0**
Name	R16*	R14*	R12*	R10*	N/U	WS_MODE	WS_POL	IQ_MUX
Function	1 = 16-bit O/P 0 = See Other bits	1 = 14-bit O/P 0 = See Other bits	1 = 12-bit O/P 0 = See Other bits	1 = 10-bit O/P 0 = See Other bits	Write '0' Mask on Reads	1 = Square 0 = Pulse	0 = Pos 1 = Neg	1= Mux I & Q on I out 0 = No Mux
All bits default to the logic '0' state at power–up and resets. * – **One and only one** of these 4 bits **must** be set to the logic '1' state.								

3.11.6 DDR Output Status Register – R/W @ 'C6x Address 0x0032 0064

This register contains flags and status information for the output samples. Its contents are summarized in Table 3–21, below. For a detailed description of these bits, please refer to Section 3.6 of the GC1012A Data Sheet, in Appendix A.

Table 3–21: Model 6216 – DDR Output Status Register – R/W @ 'C6x Address 0x0032 0064

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6***	**D5**	**D4**	**D3**	**D2**	**D1***	**D0**
Name	Power_ Down	OVERFLOW	OFLOW_ ENABLE	OFLOW_ MODE	N/U	INT_ ENABLE	MISSED	$\overline{\text{READY}}$
Function	1 = Standby 0 = Active	1 = True 0 = False	1 = Enable 0 = Disable	1 = Pulse 0=OVERFLOW	Write '0' Mask on Reads	1 = Enable 0 = Disable	1 = True 0 = False	1 = Not Ready 0 = Ready
All bits default to the logic '0' state at power–up and resets. * – These bits are Read/Clear – Set by chip, cleared by user – Writing '1' to these bits has no effect.								

3.11 Processor Interface to the Graychip GC1012A DDR (continued)

3.11.7 DDR One–Shot Register – W. O. @ 'C6x Address 0x0032 0068

Any write to this address generates a pulse on the GC1012A's $\overline{OS}$ pin. The data written is neither used nor stored and is therefore trivial.

3.11.8 DDR Checksum Register – R. O. @ 'C6x Address 0x0032 006C

This read–only register stores the checksums generated in the diagnostic mode. The 8 bit checksum is generated as a non–linear feedback accumulation of the BS, FS, I, and Q output bits. The current checksum is stored in this register and the checksum generator is cleared whenever the internal sync goes low. The register is summarized in Table 3–22, below.

Table 3–22: Model 6216 – DDR Checksum Register – R. O. @ 'C6x Address 0x0032 006C

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	Chk_7	Chk_6	Chk_5	Chk_47	Chk_3	Chk_2	Chk_1	Chk_0
Function	The 8–bit checksum							
All bits default to the logic '0' state at power–up and resets.								

3.11 Processor Interface to the Graychip GC1012A DDR (continued)

3.11.9 DDR Output Registers – R. O. @ 'C6x Addresses 0x0032 0070, 0x0032 0074 0x0032 0078, and 0x0032 007C

The 16–bit I and Q output samples are stored in their respective output register pairs. The contentof these registers is summarized in Tables 3–23 – 3–26, below. For a detailed description of these registers, please refer to Section 3.9 of the GC1012A Data Sheet, in Appendix A.

Table 3–23: Model 6216 – DDR I Output, Byte 0 – R/W @ 'C6x Address 0x0032 0070

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
Function	The 8 LSB's of the real (In–phase) portion of the GC1012A's Complex Output samples							
All bits default to the logic '0' state at power–up and resets.								

Table 3–24: Model 6216 – DDR I Output, Byte 1 – R/W @ 'C6x Address 0x0032 0074

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	I_15	I_14	I_13	I_12	I_11	I_10	I_9	I_8
Function	The 8 MSB's of the real (In–phase) portion of the GC1012A's Complex Output samples							
All bits default to the logic '0' state at power–up and resets.								

Table 3–25: Model 6216 – DDR Q Output, Byte 0 – R. O. @ 'C6x Address 0x0032 0078

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Function	The 8 LSB's of the imaginary (Quadrature) portion of the GC1012A's Complex Output samples							
All bits default to the logic '0' state at power–up and resets.								

Table 3–26: Model 6216 – DDR Q Output, Byte 1 – R. O. @ 'C6x Address 0x0032 007C

Bit #	D31 – D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	Q_15	Q_14	Q_13	Q_12	Q_11	Q_10	Q_9	Q_8
Function	The 8 MSB's of the imaginary (Quadrature) portion of the GC1012A's Complex Output samples							
All bits default to the logic '0' state at power–up and resets.								

Appendix A: Graychip GC1012A – Digital Tuner Chip

Included for your reference on the following pages is the data sheet for the GC1012A Dig–ital Tuner Chip, provided by the courtesy of Graychip, Inc., Palo Alto, CA. Please note that this device is referred to as a Digital Drop Receiver (DDR) in the body of this manual, whreras the manufacturer uses the term Digital Tuner. These are application–oriented terms, used to refer to devices that perform essentially identical functions.

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GC1012A

DIGITAL TUNER CHIP

DATASHEET

Revision 0.1

February 18, 1998

This datasheet contains information which may be changed at any time without notice.

REVISION HISTORY

This datasheet is revised from the GC1012 datasheet to reflect the changes in the GC1012A replacement.

Revision	Date	Description
0.0	18 Feb 1998	First GC1012A datasheet. Major changes in specifications. Bits 5,6,7 of register 7 and bit 7 of register 9 changed to reflect new power down/keepalive modes.
0.1	?	Page 8: Pin pitch P on drawing corrected to 0.8mm. Table was correct.

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GC1012A DATASHEET

1.0 FUNCTIONAL DESCRIPTION

Fabricated in high speed CMOS technology, the GC1012A chip is an all digital tuner which can downconvert and band limit signals from wide band digitized sources. At full rate operation (80 MHz input rate), the input bandwidth can be up to 40 MHz wide. Any signal within the input bandwidth can be down-converted to zero frequency, low pass filtered, and output at a reduced sample rate. The chip's output can be formatted as either a complex data stream, or as a real data stream. The complex samples are output at rates equal to $F_O=F_{CK}/D$, where F_O is the output rate, D is 1, 2, 4, 8, 16, 32 or 64 and F_{CK} is the input sample (clock) rate. The real output rates are $F_O=2F_{CK}/D$ for D equal to 2, 4, 8, 16, 32, or 64.

The signal is low pass filtered to remove out of band energy before the sample rate is decreased. The filter's out of band rejection is over 75 dB and its passband ripple is less than 0.2 dB peak to peak. The passband of the output filter covers 80% of the output bandwidth.

The 28 bit accumulator in the chip's digital oscillator circuit provides a tuning accuracy equal to the input clock rate divided by 2^{28}. The tuning resolution at a clock rate of 50 MHz is less than 0.2 Hz giving a tuning accuracy of +/- 0.1 Hz. The phase noise in the oscillator is low enough to provide a spur free dynamic range of over 75 dB.

The chip's output circuit allows the user to select a real or complex data output format, to select spectral inversion, or to offset the output spectrum by half of the output sample rate. The output's signal gain can be adjusted in 0.03 dB steps. The word size of the output samples are either 10, 12, 14, or 16 bits.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of an 8 bit data I/O port, a 4 bit address port, a read/$\overline{\text{write}}$ bit, and a control select strobe.

I and Q output registers can be read from the control port to allow an external processor to monitor or process the chip's output samples. These registers are valuable for monitoring the chip's output power in order to set and adjust gain levels.

1.1 KEY FEATURES

- 80 million samples per second input rate
- 0.1 Hz tuning resolution
- >75 dB dynamic range
- Programmable output bandwidth
- 12 bit inputs, 10, 12, 14, or 16 bit outputs
- Real or complex output formats
- Built in strobe/sync generator
- Symmetric rounding used throughout
- Gain adjust in 0.03 dB steps
- Microprocessor interface for control, output, and diagnostics
- Power down mode
- Auto power down with clock loss detection
- Built in diagnostics
- 3.25W power at 50 MHz, 5 volts
- 850 mW at 30 MHz, 3.3 volts
- 120 pin quad flat pack package

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1.2 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1

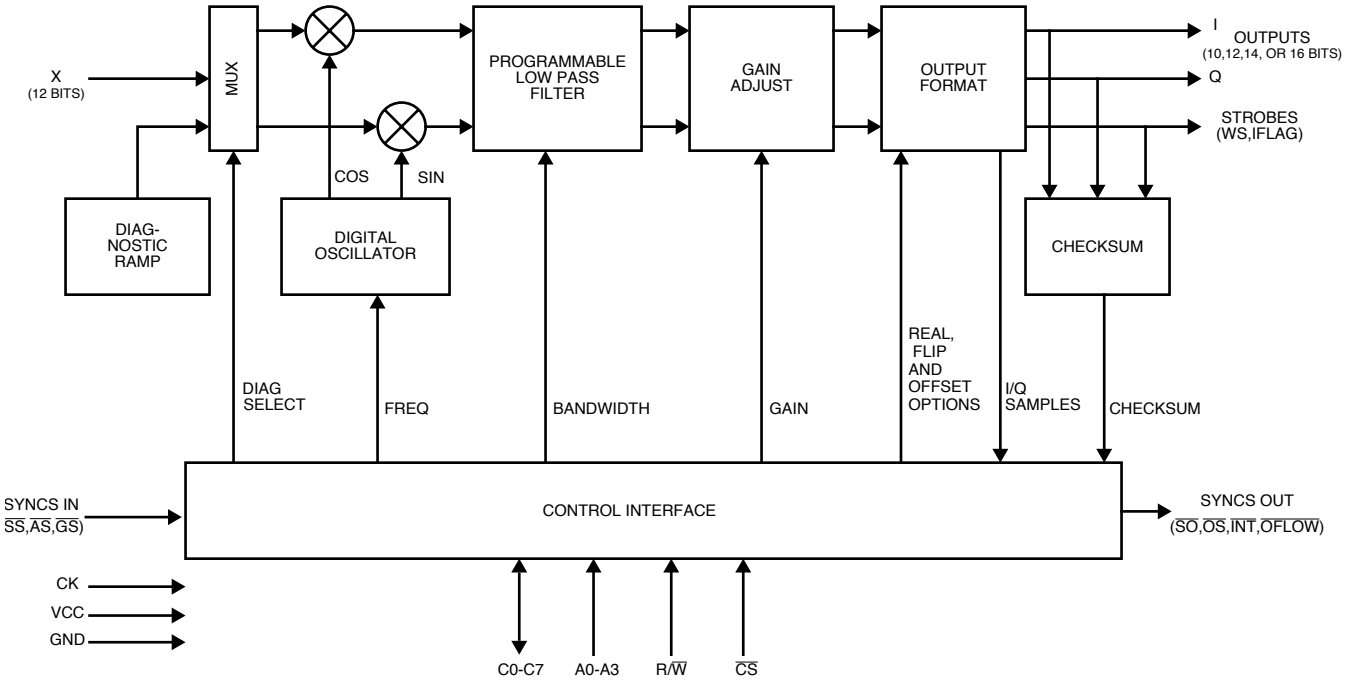


Figure 1. GC1012A Block Diagram

Each of these functions are described below.

1.3 CONTROL INTERFACE

The control interface performs four major functions: It allows an external processor to configure the chip, it allows an external processor to capture and read output samples from the chip, it allows an external processor to perform diagnostics, and it generates internal synchronization strobes.

The chip is configured by writing control information into 8 bit control registers within the chip. The contents of these control registers and how to use them are described in Section 3. The registers are written to or read from using the **C[0:7]**, **A[0:3]**, **R/$\overline{W}$**, and **$\overline{CS}$** pins. Each control register has been assigned a unique address within the chip. An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:3]** to the desired register address, setting the **R/$\overline{W}$** pin low, setting **D[0:7]** to the desired value and then pulsing **$\overline{CS}$** low.

To read from a control register the processor must set **A[0:3]** to the desired address, set **R/$\overline{W}$** high, and then set **$\overline{CS}$** low. The chip will then drive **C[0:7]** with the contents of the selected register. After the processor has read the value from **C[0:7]** it should set **$\overline{CS}$** high. The **C[0:7]** pins are turned off (high impedance) whenever **$\overline{CS}$** is high or **R/$\overline{W}$** is low. The chip will only drive these pins when **$\overline{CS}$** is low and **R/$\overline{W}$** is high.

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Control register addresses 12, 13, 14, and 15 are reserved to allow an external processor to read output samples from the chip. Addresses 12 and 13 are the I-registers which store the16 bit in-phase part of the output sample. Addresses 14 and 15 are the Q-registers which store the quadrature part. In the real mode the I registers store the even-time output samples and the Q registers store the odd-time output samples. Output ready and missed flags are provided in control register 9 in order to synchronize the storing and reading of the output samples. An interrupt output pin is also provided on the chip which can be used to interrupt the external processor when a new sample is ready. See the description of control register 9 in Section 3.6 for more details. The setup, hold and pulse width requirements for control read or write operations are given in Section 4.4.

Checksums are read from the chip during diagnostics using address 11. More details on the diagnostic modes is given in Section 1.11.

Address 10 is used to generate a one-shot pulse on the **$\overline{\text{OS}}$** output pin. This pulse can be used to synchronize the output timing and/or frequency oscillators of multiple GC1012A chips.

The control interface also generates the chip's internal sync strobes. The user may select to synchronize the chip using an external sync strobe (**$\overline{\text{SS}}$**), or use the chip's internal sync counter. The internal sync counter can be synchronized to **$\overline{\text{SS}}$**, or left to free run (See **SS_OFF** in Section 3.2). The period of the internal sync counter can be either 256 clocks or 2^{20} clocks. The 256 clock period is intended to be used for chip test purposes only. The internal sync counter is used during diagnostics to clear the data paths and strobe the checksum generator. The internal sync counter can also be used to periodically re-synchronize all of the counters in the chip during normal operating modes.

1.4 DIGITAL OSCILLATOR

The digital oscillator generates sine and cosine sequences which are used to mix the desired signal down to zero frequency. The digital oscillator contains a 28 bit frequency register, a 28 bit frequency accumulator, and a sine-cosine generator. The tuning frequency of the oscillator is set by loading a 28 bit frequency word from the control registers into the frequency register. If the frequency register is set to the word **FREQ**, then the tuning frequency will be: $\text{Frequency} = \frac{\text{Sample Rate}}{2^{28}}\textbf{FREQ}$. The tuning frequency should be set to the middle of the desired output bandwidth.

The frequency word **FREQ** is stored into the control registers at control addresses 0,1,2 and 3. The 28 bit word is then transferred into the frequency register using one of the following methods:

(1) The frequency register is always loading (the frequency changes immediately as the frequency word is loaded into the control registers).

(2) The frequency register is loaded when the user sets a control register bit.

(3) The frequency register is synchronously loaded when the accumulator sync strobe (**$\overline{\text{AS}}$**) goes low.

(4) The frequency register is synchronously loaded when the system sync strobe (**$\overline{\text{SS}}$**) goes low.

See Section 3.2 for more details on the frequency load modes.

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The 28 bit frequency word is accumulated in the 28 bit frequency accumulator. The frequency accumulator will normally free run, but can be synchronously cleared by either the system sync (**$\overline{\mathbf{SS}}$**) or the accumulator sync (**$\overline{\mathbf{AS}}$**). The accumulator clear modes are controlled by bits in control register 4. See Section 3.2 for details.

The upper 13 frequency accumulator bits are used to generate the oscillator's sine and cosine outputs. These sines and cosines are generated to 12 bit accuracy. The oscillator's peak spur levels are below -75 dB.

1.5 MIXER

The mixer multiplies the 12 bit input samples by the 12 bit sine and cosine values coming from the digital oscillator. An input signal at the oscillator's tuning frequency will be centered at zero frequency after passing through the mixer. The mixer outputs are rounded to 13 bits using the "round-to-even" rounding algorithm. The "round-to-even" algorithm prevents a DC rounding bias by detecting fractions which are exactly equal to 0.5 and rounding them up half of the time and rounding them down half of the time. The choice to round up or down is made so as to always give an even result.

1.6 PROGRAMMABLE LOW PASS FILTER

The mixer's output is filtered using a programmable bandwidth low pass filter. The filter allows the output sample rate to be reduced by a factor of **D** = 2, 4, 8, 16, 32, or 64. The value of **D** is set using control register 5. The filter can be bypassed by setting **D** equal to 1. This allows the chip to be used as a mixer without any output filtering.

The low pass filter is a finite impulse response (FIR) filter with linear phase, 0.13 dB peak to peak ripple and over 75 dB of out of band rejection. The 2 dB output bandwidth is +/- $0.4F_S$ (80% usable bandwidth) where F_S is the complex output rate. The 0.1 dB bandwidth is +/- 0.36 F_S (72% usable bandwidth).

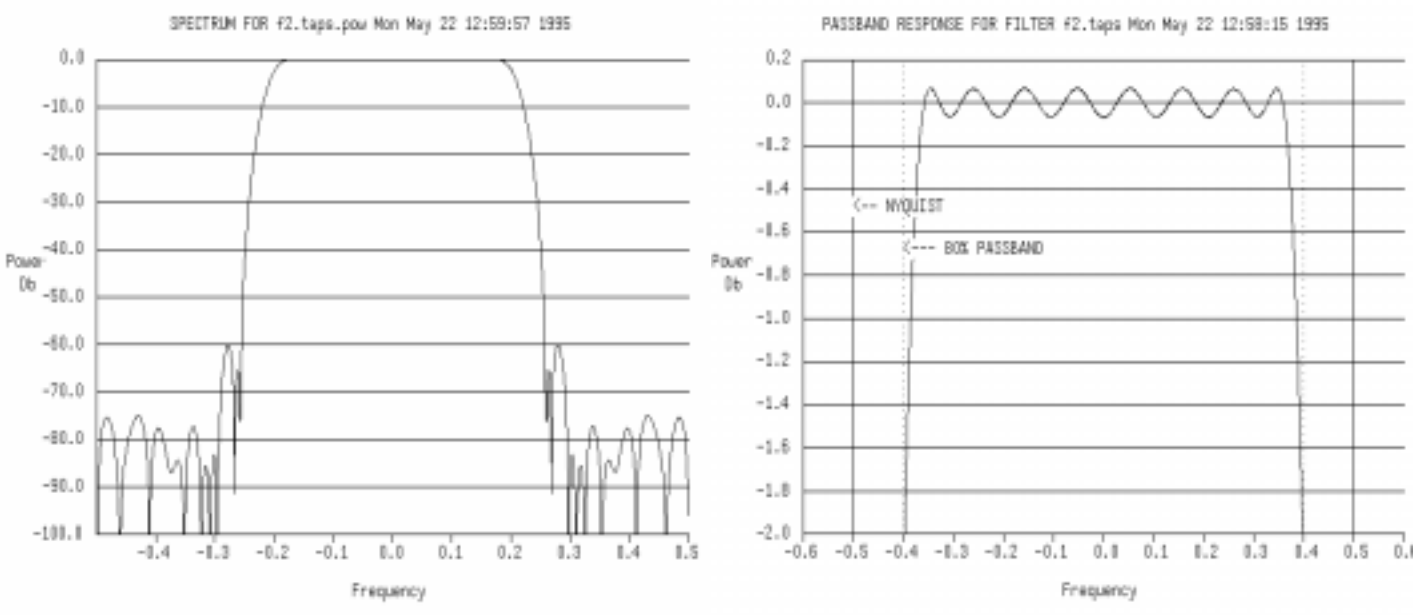
The coefficients for the 40 tap decimate by 2 filter are:

-12	-42	-52	7	85	46	-110	-145	82	276
39	-396	-293	434	714	-273	-1400	-409	3115	6462
6462	3115	-409	-1400	-273	714	434	-293	-396	39
276	82	-145	-110	46	85	7	-52	-42	-12

The coefficients for the other filters are available from GRAYCHIP.

Figure 2 shows the spectral response of the decimate by 2 low pass filter. The decimate by 4, 8, 16, 32 and 64 filters are similar. Figure 2(a) shows the overall frequency response prior to decimation.Note that the filter rolls off quickly to 60 dB and is down below 75 dB in the region which aliases back into the passband. Figure 2(b) shows the 0.13 dB ripple in the passband.

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(a) Overall (b) Passband

Figure 2. Filter Response

1.7 GAIN

The programmable bandwidth filter is followed by a gain circuit which adjusts the output level in 0.03 dB steps. The gain is controlled by the power of two gain value **S** and the fractional gain value **F**. The input to output gain of the chip is equal to $\mathbf{G} = 2^{(\mathbf{S}-B)}(1+\mathbf{F}/256)$, where **S** ranges from 0 to 15, **F** ranges from 0 to 255, and **B** is the base gain setting for each value of **D**. The base gain setting **B** gives a unity input to output gain for the chip, i.e., a 12 bit constant going into the chip will come out in the 12 MSBs of the 16 bit output word. The values of **B** are:

D	**B**
1	6
2	5
4	4
8	3
16	2
32	1
64	0

The **S** and **F** gain settings are double buffered so that they can be applied synchronously. A new gain setting takes effect either when **S** is loaded, or, if the GS_MODE control bit is used, when the $\overline{\mathbf{GS}}$ strobe is received.

The gain settings and GS_MODE bit are stored in control registers 6 and 7.

Overflow detection circuitry detects overflow conditions in the gain output words and saturates the samples to plus or minus full scale. Overflows are reported in the STATUS register and on the $\overline{\mathbf{OFLOW}}$ output pin. The overflow status can be used to detect if the gain settings are too high.

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1.8 OUTPUT FORMATTING

The output format circuit allows the user to flip the output spectrum, to offset the spectrum by one-fourth the Nyquist rate, to convert the complex output stream to a real one at twice the rate, to round the samples to 10, 12, 14 or16 bits, and to multiplexes the I and Q samples together. These options are set using control register 8.

A word strobe (**WS**) is generated as an output clock signal. The **WS** strobe is either one clock cycle wide or is a 50% duty cycle clock. The polarity of **WS** is programmable.

The I and Q samples can be multiplexed together onto the I output pins by using the IQMUX mode. The **IFLAG** output pin is used in this mode to identify when the I words are being output. The **WS** strobe rate is doubled in this mode. The Q output pins are cleared in this mode.

Only the I output pins are used in the real mode. The Q pins are cleared. The output spectrum is centered from 0 to $F_O/2$ in the real mode. The spectrum is centered from $-F_O/2$ to $+F_O/2$ in the complex mode. The OFFSET control allows the spectrum to be centered from 0 to F_O.

The output format circuitry is synchronized by the $\overline{\textbf{SS}}$ input sync. This allows one to synchronize the output timing of multiple GC1012A chips.

1.9 POWER DOWN AND KEEPALIVE MODES

Unused chips in a system can be powered down by setting the POWER_DOWN control bit in register 9 (See Section 3.6). This reduces the internal clock rate down to 1 KHz to minimize the power consumed by the chip while still refreshing the internal dynamic nodes at a suitable rate.

The chip includes a “keepalive” circuit which detects when the clock has stopped for more than 2 milliseconds. The chip will automatically go into the power down mode if clock loss is detected. The keepalive detection circuit can be disabled by setting bit 5 in register 7 (See Section 3.4). NOTE: The chip will draw up to an Amp of current if the clock is stopped and the keepalive circuit is disabled.

1.10 THE ONE SHOT PULSE GENERATOR

The chip can generate a one-shot pulse which is output on the $\overline{\textbf{OS}}$ pin by writing to address 10. The pulse can be connected to the $\overline{\textbf{SS}}$, $\overline{\textbf{AS}}$, or $\overline{\textbf{GS}}$ sync input pins of GC1012A chips (including itself) to synchronize the output timing, frequency oscillators, or gain settings of multiple chips.

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1.11 DIAGNOSTICS

An input ramp generator, a sync period generator, and a checksum generator are provided on the chip in order to run diagnostic tests. Diagnostics are performed by turning on the ramp generator, enabling the diagnostic syncs, letting the chip operate for at least 4 sync periods, reading the checksum and comparing it to its predicted value. A new checksum is generated every sync period. The input ramp sequence is the same for every sync period and the chip is re-initialized at the beginning of each sync period so that each checksum should be the same once the chip's data path has been flushed. The chip requires at least 3 sync periods to flush, so the fourth and following checksums should be valid. The test is then repeated for several different tuning frequencies, decimation settings, and output modes.

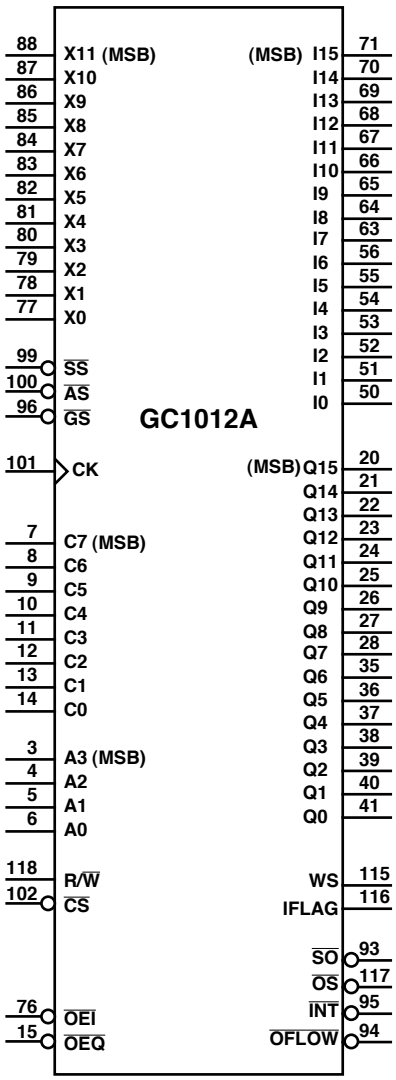
The sync period is 2^{20} clocks, or approximately 1 million clock cycles, so four sync periods will be about 4 million clocks. This represents a delay of less than 15 milliseconds for a clock rate of 60 MHz.

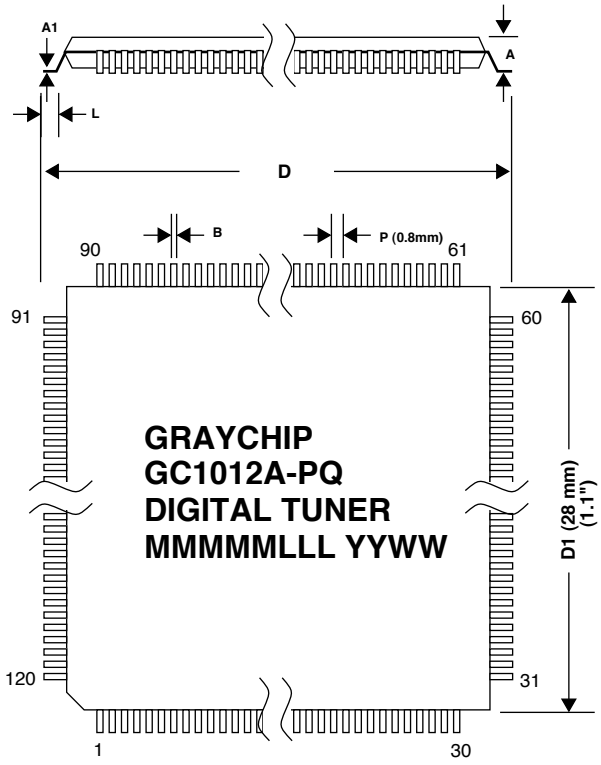
The following table lists the expected checksums for four test configurations. All values are in HEX.

CONTROL REGISTER	TEST 1	TEST 2	TEST 3	TEST 4
FREQ (REG 0,1,2,3)	0000101	0F0F0F0	55AA55A	AA55AA5
SYNC MODE (REG 4)	A9	A9	A9	A9
FILTER MODE (REG 5)	82	93	E4	D7
GAIN FRACTION (REG 6)	AA	55	00	FF
GAIN EXPONENT (REG 7)	5	4	3	0
OUTPUT (REG 8)	16	46	21	80
EXPECTED CHECKSUMS (REG 11)	64	50	A7	03

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2.0 PIN DESCRIPTIONS





120 PIN QUAD FLAT PACK PACKAGE

GC1012A-PQ = Enhanced Thermal Plastic Package
GC1012A-CQ = Ceramic Package

Package Markings: **MMMMM = Mask Code**
LLL = Lot Number
YYWW = Date Code

DIMENSION		PLASTIC	CERAMIC
D	(width pin to pin)	31.2 mm (1.228")	32.0 mm (1.260")
D1	(width body)	28.0 mm (1.102")	28.0 mm (1.102")
P	(pin pitch)	0.8 mm (0.031")	0.8 mm (0.031")
B	(pin width)	0.35 mm (0.014")	0.35 mm (0.014")
L	(leg length)	0.88 mm (0.035")	0.70 mm (0.028")
A	(height)	4.07 mm (0.160")	3.25 mm (0.128")
A1	(pin thickness)	0.17 mm (0.007")	0.2 mm (0.008")

VCC PINS: 2,16,17,29,32,33,43,44,47,48,58,59,62,74,75,89,91,97, 104,105,106,109,110,114,119

GND PINS: 1,18,19,30,31,34,42,45,46,49,57,60,61,72,73,90,92,98, 103,107,108,111,112,113,120

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

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SIGNAL	DESCRIPTION
X[0:11]	**INPUT DATA.** Active high The 12 bit two's complement input samples. New samples are clocked into the chip on the rising edge of the clock. The input data rate is assumed to be equal to the clock rate.
CK	**CLOCK INPUT.** Active high The clock input to the chip. The **X**, **$\overline{SS}$**, **$\overline{GS}$** and **$\overline{AS}$** signals are clocked into the chip on the rising edge of this clock. The **I**, **Q**, **WS**, **IFLAG**, **$\overline{OS}$**, **$\overline{OFLOW}$** and **$\overline{SO}$** signals are clocked out on the rising edge of this clock.
$\overline{SS}$	**SYSTEM SYNC**. Active low The sync input to the chip. All timers, accumulators, and control counters are, or can be, synchronized to **$\overline{SS}$**. Bits in control register 4 (see Section 3.2) determine the operation of **$\overline{SS}$**. This sync is clocked into the chip on the rising edge of the clock.
$\overline{AS}$	**ACCUMULATOR SYNC**. Active low The accumulator sync is provided to synchronously change tuning frequencies. This sync can be used to load a new tuning frequency into the frequency register and/or to clear the frequency accumulator. This signal is clocked into the chip on the rising edge of the clock.
$\overline{GS}$	**GAIN SYNC**. Active low The gain sync is provided to synchronously change gain settings. This signal is clocked into the chip on the rising edge of the clock.
I[0:15]	**IN-PHASE OUTPUT DATA**. Active high The I part of each complex output sample is output as a 16 bit word on this pin. The bits are clocked out on the rising edge of the clock.
$\overline{OEI}$	**IN-PHASE OUTPUT ENABLE**. Active low The **I[0:15]** output pins are put into a high impedance state when this pin is high.
Q[0:15]	**QUADRATURE OUTPUT DATA**. Active high The Q part of each complex output sample is output as a 16 bit word on this pin. The bits are clocked out on the rising edge of the clock.
$\overline{OEQ}$	**QUADRATURE OUTPUT ENABLE**. Active low The **Q[0:15]** output pins are put into a high impedance state when this pin is high.
WS	**WORD STROBE**. Programmable active high or low level This strobe is output synchronous with the **I** and **Q** data words. The strobe occurs once per bit and is either one clock wide or has a 50% duty cycle. The high/low polarity of the strobe is programmable. See Section 3.5 for details.
IFLAG	**IN-PHASE STROBE**. Active high This strobe identifies the in-phase half of a complex pair when the outputs are in the IQ_MUX mode. See Section 3.5 for details. This signal is high when the I-half is output and is low when the Q-half is output.
$\overline{SO}$	**SYNC OUT**. Active low This signal is either a delayed version of the input system sync **$\overline{SS}$**, or, if SS_MUX in control register 4 is set, is the internally generated sync which has a period of 2^{20} clocks.
$\overline{INT}$	**INTERRUPT OUT**. Active low This signal is the READY flag from control register 9. This interrupt goes active when a new output sample is ready in control registers 12, 13, 14, and 15.
$\overline{OS}$	**ONE SHOT STROBE**. Active low This output is a one-shot sync strobe generated by writing to control address 10. The strobe is one clock cycle wide.
$\overline{OFLOW}$	**OVERFLOW FLAG**. Active low This signal goes low when an overflow is detected in the gain circuit. The signal will either pulse low for one clock cycle or will stay low depending upon the state of the OFLOW_MODE bit in control register 9.
C[0:7]	**CONTROL DATA I/O BUS**. Active high This is the 8 bit control data I/O bus. Control register data is loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{CS}$** is low and **R/$\overline{W}$** is high.
A[0:3]	**CONTROL ADDRESS BUS**. Active high These pins are used to address the 16 control registers within the chip. Each of the 16 control registers within the chip are assigned a unique address. A control register can be written to or read from by setting **A[0:3]** to the register's address.
R/$\overline{W}$	**READ/$\overline{WRITE}$ CONTROL**. High for read, low for write This pin determines if the control bus cycle is a read or write operation. The pin is high for a read and is low for a write.
$\overline{CS}$	**CONTROL STROBE**. Active low This control strobe enables the read or write operation. The contents of the register selected by **A[0:3]** will be output on **C[0:7]** when **R/$\overline{W}$** is high and **$\overline{CS}$** is low. If **R/$\overline{W}$** is low when **$\overline{CS}$** goes low, then the selected register will be loaded with the contents of **C[0:7].**

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3.0 CONTROL REGISTERS

The chip is configured and controlled through the use of 16 eight bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{CS}$**, **R/$\overline{W}$**, **A[0:3]**, and **C[0:7]**) described in the previous section. The register names and their addresses are:

ADDRESS	NAME	ADDRESS	NAME
0	FREQ byte 0	8	Output Mode
1	FREQ byte 1	9	Status
2	FREQ byte 2	10	One Shot
3	FREQ byte 3	11	Checksum
4	Sync mode	12	I-output byte 0
5	Filter mode	13	I-output byte 1
6	Gain Fraction	14	Q-output byte 0
7	Gain Exponent	15	Q-output byte 1

The following sections describe each of these registers. The type of each register bit is either R or R/W indicating whether the bit is read only or read/write. All bits are active high.

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3.1 FREQUENCY WORD REGISTERS

Registers 0, 1, 2, and 3 contain the 28 bit frequency tuning word. Bit 0 is the LSB, bit 27 is the MSB.

ADDRESS 0: FREQUENCY BYTE 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[0:7]	Byte 0 (least significant) of frequency word

ADDRESS 1: FREQUENCY BYTE 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[8:15]	Byte 1 of frequency word

ADDRESS 2: FREQUENCY BYTE 2

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[16:23]	Byte 2 of frequency word

ADDRESS 3: FREQUENCY BYTE 3

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**FREQ**[24:27]	4 most significant bits of the frequency word
4-7	R/W	-	unused

If the desired tuning frequency is **F**, then the frequency word should be set to:

$$\mathbf{FREQ} = 2^{28}\mathbf{F}/(\text{clock rate})$$

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3.2 SYNC MODE REGISTER

The sync mode register controls the action of the **$\overline{SS}$** and **$\overline{AS}$** sync strobes and how they affect the chip's internal timers, counters, and accumulators.

ADDRESS 4: Sync Mode Register

BIT	TYPE	NAME	DESCRIPTION
0 (LSB)	R/W	SS_OFF	This bit disables the **$\overline{SS}$** input.
1	R/W	AS_ON	Enables the accumulator sync **$\overline{AS}$**. Normally the frequency accumulator will free run. This bit causes the frequency accumulator to be initialized to the contents of the frequency register when **$\overline{AS}$** goes low. **$\overline{SS}$**, instead of **$\overline{AS}$**, will reset the accumulator if AS_MUX is set and **$\overline{SS}$** is not disabled by SS_OFF.
2	R/W	AS_MUX	Use **$\overline{SS}$** for the accumulator sync. The **$\overline{AS}$** input is ignored and the **$\overline{SS}$** strobe is used in its place when this bit is set and **$\overline{SS}$** is not disabled by SS_OFF. (See AS_ON and AS_FREQ).
3	R/W	LD_FREQ	Load the frequency register in the digital oscillator with the contents of the frequency word registers. If left on, this bit will cause the frequency register to load whenever a frequency word register is changed.
4	R/W	AS_FREQ	Enables the synchronous frequency load mode. When this bit is set and **$\overline{AS}$** goes low, the frequency register will be synchronously loaded with the contents of the frequency control registers. **$\overline{SS}$**, instead of **$\overline{AS}$**, will load the frequency register if AS_MUX is set and **$\overline{SS}$** is not disabled by SS_OFF.
5	R/W	SS_DIAG	Enables diagnostic syncs. This bit routes the internal sync to the checksum generator and to all accumulators and control counters within the chip. This forces the chip to re-initialize at the start of every sync period. The internal sync period will be 2^{20} clocks if SS_MUX is set, otherwise it will be determined by the period of an externally provided **$\overline{SS}$** strobe.
6	R/W	TEST	Shortens the internal sync counter period from 2^{20} clocks to 2^{8} clocks. This mode is used to test chips at the factory.
7 (MSB)	R/W	SS_MUX	Use the sync counter's terminal count strobe for the internal sync instead of the sync input **$\overline{SS}$**. The internal sync is output on the **$\overline{SO}$** pin.

The operation of these control bits are illustrated in Figure 3.

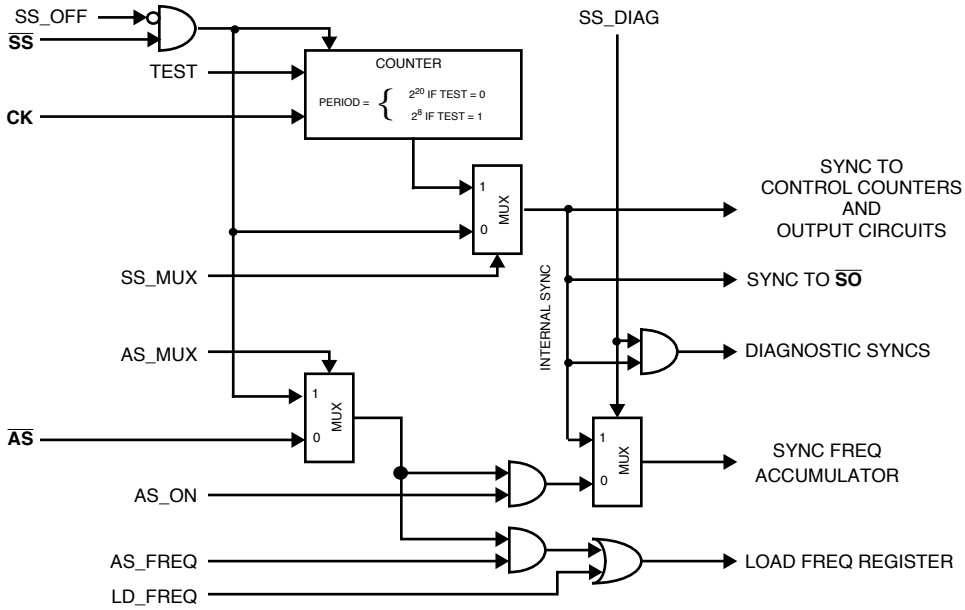


Figure 3. Sync Controls

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3.3 FILTER MODE REGISTER

This register controls filtering, output formatting and the diagnostic input mode.

ADDRESS 5: Filter Mode Register

BIT	TYPE	NAME	DESCRIPTION
0-2	R/W	**DEC[0:2]**	The decimation mode. The output sample rate is set using **DEC** according to the following table:

DEC	Fo COMPLEX (REAL = 0)	Fo REAL (REAL = 1)
0 or 1	F_{CK}	?
2	$F_{CK}/2$	F_{CK}
3	$F_{CK}/4$	$F_{CK}/2$
4	$F_{CK}/8$	$F_{CK}/4$
5	$F_{CK}/16$	$F_{CK}/8$
6	$F_{CK}/32$	$F_{CK}/16$
7	$F_{CK}/64$	$F_{CK}/32$

Where F_{CK} is the input rate and Fo is the output rate.

3	R/W	-	Unused.
4	R/W	REAL	Output real samples instead of complex samples. The output spectrum is centered from 0 to $F_O/2$ where F_O is the output rate (see **DEC** above for the REAL mode). NOTE: The FLIP bit described below is active low in the real mode.
5	R/W	OFFSET	Offset the complex output spectrum. Used in the complex output mode (REAL=0) to force the output spectrum to be centered at $F_O/2$, where F_O is the output sample rate (see **DEC** above for the COMPLEX mode). This mode is useful for single-sideband AM signals because it moves the lower band edge up to zero frequency where it belongs. The upper half of the spectrum will appear as negative frequencies.
6	R/W	FLIP	Flip the output spectrum. This bit inverts the output spectrum. In the complex mode the spectrum is flipped about zero. In the real mode the spectrum is flipped about $F_O/4$, where F_O is the real mode's output sample rate. In the complex mode FLIP=1 flips the spectrum. In the real mode FLIP=0 flips the spectrum.
7	R/W	DIAG	Use the diagnostic ramp for the input to the chip instead of the **X** input. The ramp counts from -2048 to +2047 and then starts over again.

The effect on the output spectrum of the REAL, OFFSET and FLIP bits is illustrated in the following diagram. (F_O is the output sample rate)

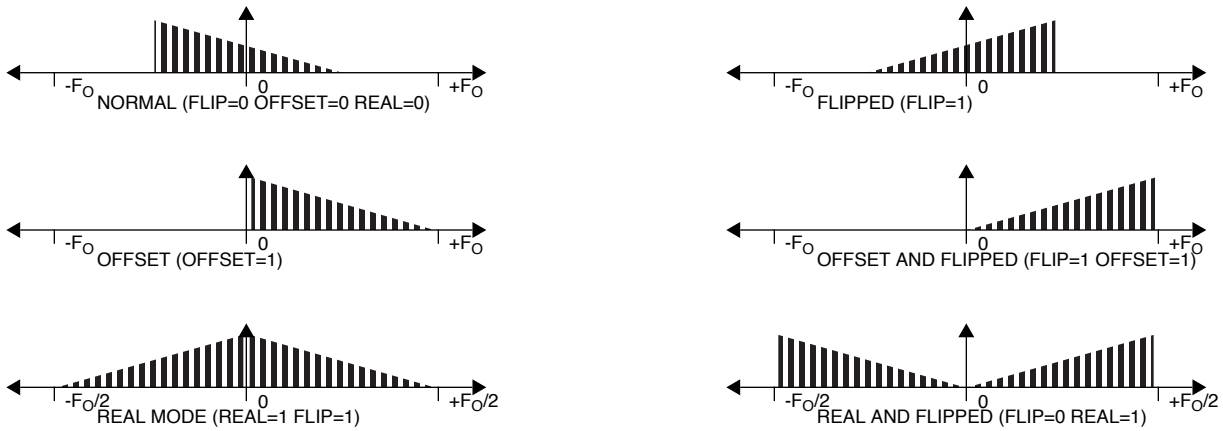


Figure 4. Output Spectral Formats

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3.4 GAIN CONTROL REGISTERS

These registers set the output gain.

ADDRESS 6: Gain Control Register

BIT	TYPE	NAME	DESCRIPTION
0–7	R/W	**F[0:7]**	The 8 bit gain fraction.

ADDRESS 7: Gain Exponent Register

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**S[0:3]**	The 4 bit gain exponent.
4	R/W	GS_MODE	Turns on the synchronous gain mode. See below.
5	R/W	KA_DISABLE	Provided for testability. Turns off the clock loss detect function in the keepalive circuit. This bit powers up low and should be kept low.
6	R	KA_CK	A read only bit which monitors the 1 KHz (approximate) clock used in the power down mode (See bit 7, address 9, Section 3.6).
7	R	KA_MODE	This bit will read back high if the chip is in the power down mode, either due to the loss of clock, or by setting bit 7 in register 9.

The chip's input to output gain is set using **F** and **S** according to the formula:

$$GAIN = 2^{(\mathbf{S}-\mathbf{B})}(1+\mathbf{F}/256)$$

where **B** is the base gain setting which is a function of the decimation mode of the chip. The unity gain setting (**S**=**B** and **F**=0) means that a 12 bit DC input will show up in the upper 12 bits of the 16 bit output.

The values of **B** are:

DEC	B
0 or 1	6
2	5
3	4
4	3
5	2
6	1
7	0

The GS_MODE control bit determines when new gain settings are applied to the output. New gain settings are double buffered so that they can be synchronized with the output words. If GS_MODE is low, then the gain settings are applied to the output samples immediately after **S** has been loaded. If GS_MODE is high, then the new gain settings are not used until $\overline{\mathbf{GS}}$ goes low.

NOTE: The gain settings must be loaded in the correct order- **F** first and then **S**. The circuit detects new gain settings by sensing when **S** is loaded. this means that **S** must be loaded even if one only wishes to change **F**.

Bits 5, 6, and 7 of this register were unused R/W bits in the original GC1012 chip. Applications using the GC1012A as a GC1012 replacement should ignore these bits when reading address 7.

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3.5 OUTPUT MODE REGISTER

The output mode register controls the output formatting.

ADDRESS 8: Output mode register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	IQ_MUX	The IQ_MUX control is used in the complex mode to multiplex the I and Q output words onto the **I[0:15]** output pins. Normally the I and Q halves are output on separate ports. When this bit is high, the halves are multiplexed together so that the I half is output first, followed by the Q half. The word strobe (**WS**) rate is doubled in this mode. The **IFLAG** output signal is used in this mode to identify the I half of each complex pair. The **Q[0:15]** output pins are forced low in this mode.
1	R/W	WS_POL	Changes the polarity of **WS**.
2	R/W	WS_MODE	Changes the mode of **WS**. Normally **WS** pulses high during the clock cycle before an **I** or **Q** output transition. This bit changes **WS** so that it is a 50% duty cycle clock with its rising edge in the middle of each output period
3	R/W	-	Unused
4	R/W	R10	Round the output samples to the 10 bits MSBs of the output word.
5	R/W	R12	Round the output samples to the 12 bits MSBs of the output word.
6	R/W	R14	Round the output samples to the 14 bits MSBs of the output word.
7	R/W	R16	Round the output samples to the 16 bits MSBs of the output word.

One and only one of the rounding options should be selected. Unused LSBs are cleared.

The IQ_MUX and WS_MODE controls are illustrated in the timing diagrams shown in Figure 5. Note that the polarity shown for **WS** can be changed using the WS_POL control.

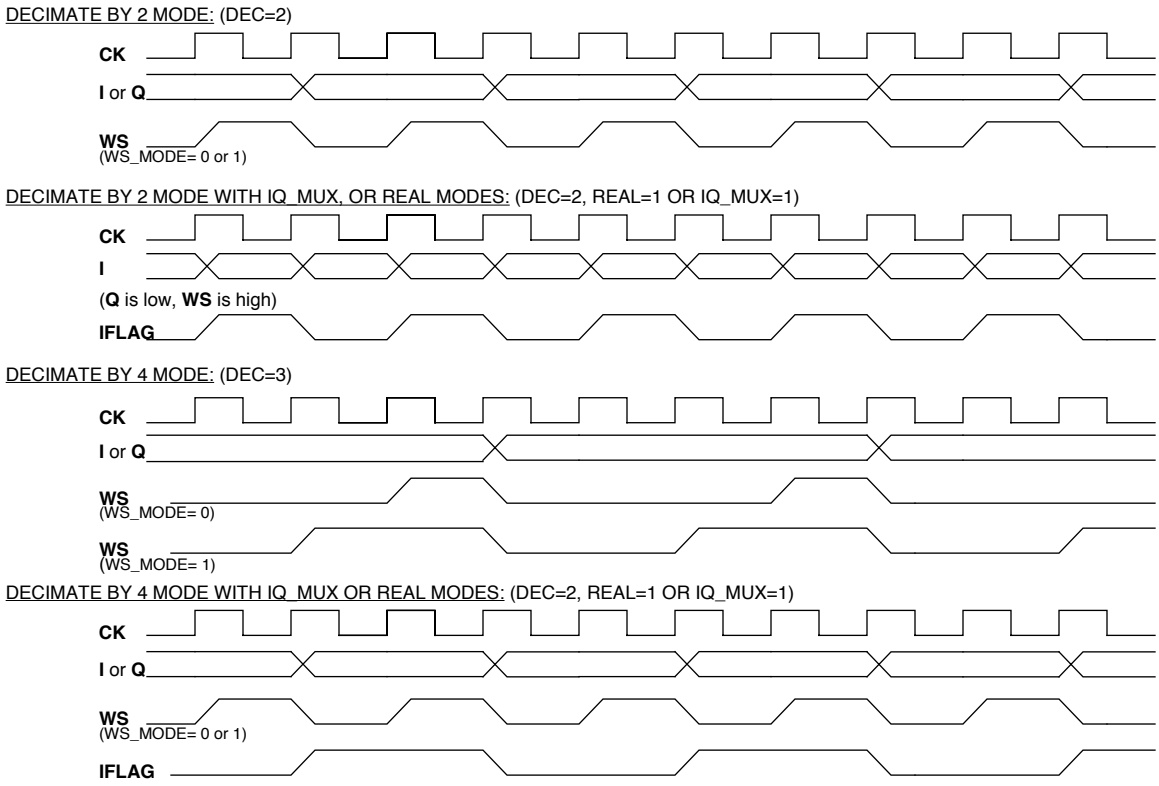


Figure 5. Timing For Output Modes

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3.6 OUTPUT STATUS REGISTER

This register contains flags and status information for the output samples.

ADDRESS 9: Output Status Register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	READY	Tells the chip that the user is ready to capture an output sample. The chip clears this bit when it has captured the sample. See Notes below.
1	R/Clear	MISSED	The chip sets this bit high if a new output sample was ready but the user had not set READY high. This lets the user know if a sample has been missed. This bit is cleared by writing a 0 to the bit. Attempting to write a 1 to this bit does nothing.
2	R/W	INT_ENABLE	This bit is used to turn on the interrupt output. If this bit is off the **$\overline{\text{INT}}$** output pin is forced high. When this bit is high the **$\overline{\text{INT}}$** output pin is equal to READY. When READY goes low, meaning that a new sample has been captured, the **$\overline{\text{INT}}$** pin will go low. If **$\overline{\text{INT}}$** is tied to a processor's interrupt input, then the processor will be interrupted whenever a new sample is ready.
3	R/W	-	Unused
4	R/W	OFLOW_MODE	This bit sets the mode of the **$\overline{\text{OFLOW}}$** output. When OFLOW_MODE is low the **$\overline{\text{OFLOW}}$** output is an inverted version of OVERFLOW (see bit 6 below). If OFLOW_MODE and OFLOW_ENABLE are high, then the **$\overline{\text{OFLOW}}$** output pulses low for one clock cycle each time there is an overflow.
5	R/W	OFLOW_ENABLE	This bit enables the overflow modes. If this bit is low, then OVERFLOW (see bit 6 below) will not be set and the **$\overline{\text{OFLOW}}$** output will not go low. This bit does not affect the overflow detection and saturation logic in the gain circuit.
6	R/Clear	OVERFLOW	The chip sets this bit when an overflow occurs and OFLOW_ENABLE is turned on. This bit can be used to indicate if the gain is set too high. This bit stays high until the user clears it. The bit is cleared by writing a 0 to it. Attempting to write a 1 to this bit does nothing.
7	R/W	POWER_DOWN	This bit is used to put the chip into a power down (standby) mode. In this mode the internal clock rate is reduced to approximately 1 KHz. All control register settings are preserved, but the output data will be invalid.

The READY signal is used to capture output samples and to read them into an external processor. The user captures outputs by setting the READY bit and then waiting for the bit to be cleared by the chip. When the bit goes low the processor can read the samples out of the I and Q output registers described in section 3.9. The processor can wait for READY to go low by either continuously reading this register, or it can use the interrupt output **$\overline{\text{INT}}$** to tell it when the sample is ready. To use the interrupt output mode the user must tie the **$\overline{\text{INT}}$** output pin from the chip to an interrupt input of the processor. The processor can then capture samples by setting READY and then setting INT_ENABLE (INT_ENABLE should be set after READY in order to avoid a spurious interrupt due to the interrupt being enabled before READY has settled to its high state). The processor will be interrupted when READY goes low again. When it is interrupted the processor can turn off INT_ENABLE, read the I/Q outputs, and then start over again.

The MISSED flag is provided to let the processor know if it has taken too long to read the I/Q samples before rearming the READY bit. If the processor wants to use the MISSED flag it should clear the flag the first time it sets the READY bit and then check it after setting the READY bit thereafter. The READY bit is set and the MISSED bit cleared by writing a 01(hex) to this register. The READY bit is set and the MISSED bit is left alone by writing a 03(hex) to this register.

NOTE: The READY bit will not be cleared if the sample is captured while the user is setting the READY bit. This will cause the READY bit to stay high after the output is captured and will not allow the chip to capture any more samples until the bit is cleared and set again. The user can detect this incorrect "ready" state by always clearing the MISSED bit when setting the READY bit. The incorrect state is detected if MISSED goes high when READY is high. The work-around to guarantee capturing an output sample is to always clear READY before setting it.

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3.7 ONE SHOT ADDRESS

The one shot pulse is generated on the **$\overline{OS}$** pin by writing to address 10. This is a write-only address and the data written to it is irrelevant.

ADDRESS 10: ONE SHOT

3.8 CHECKSUM REGISTER

This read-only register stores the checksums generated in the diagnostic mode.

ADDRESS 11: CHECKSUM

BIT	TYPE	NAME	DESCRIPTION
0-7	R	CHECK[0:7]	The 8 bit checksum. The checksum is generated as a non-linear feedback accumulation of the **BS**, **FS**, **I**, and **Q** output bits. The current checksum is stored in this register and the checksum generator is cleared whenever the internal sync goes low (see SS_MUX in Section 3.2 for the modes of the internal sync).

3.9 I AND Q OUTPUT REGISTERS

These registers are used to capture output samples.

ADDRESS 12: I-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[0:7]**	Least significant 8 bits of the **I** output.

ADDRESS 13: I-Output Byte 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[8:15]**	Most significant 8 bits of the **I** output.

ADDRESS 14: Q-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**Q[0:7]**	Least significant 8 bits of the **Q** output.

ADDRESS 15: Q-Output Byte 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**QI[8:15]**	Most significant 8 bits of the **Q** output.

The user reads the **I** and **Q** outputs through these read-only registers. The captured samples can be used for gain control, analysis, display, or diagnostics.

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4.0 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Table 1: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	7	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.7	V_{CC}+0.7	V	
Storage Temperature	T_{STG}	-65	150	°C	
Lead Soldering Temperature (10 seconds)			300	°C	
Clock Rate	F_{CK}	1		KHz	1

Notes:

1. Below 1 KHz the keepalive circuit will power down the chip. If the keepalive circuit is disabled (bit 5, address 7) and the clock is stopped, he chip will draw up to one Amp of power supply current for approximately 10 seconds. After 10 seconds the current will go down to below 50 mAmps.

4.2 RECOMMENDED OPERATING CONDITIONS

Table 2: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	3.0	5.5	V	
Temperature Ambient, no air flow	T_A	-40	+85	°C	1
Junction Temperature	T_J		140	°C	1

Notes:

1. Thermal management is required to keep T_J below MAX for full rate operation. See Table 3 below.

4.3 THERMAL CHARACTERISTICS

Table 3: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	GC1012A-CQ			GC1012A-PQ			UNITS
		2 Watts	4 Watts	6 Watts	2 Watts	4 Watts	6 Watts	
Theta Junction to Ambient	θja	29	16	15	18	11	10	°C/W
Theta Junction to Case	θjc	8	7	6	4	4	4	°C/W

Note: Air flow will reduce θ**ja** and is highly recommended.

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4.4 DC CHARACTERISTICS

All parameters are industrial temperature range of -40 to 85 ^{o}C ambient unless noted.:

Table 4: DC Operating Conditions

PARAMETER	SYMBOL	Vcc = 3.3V		Vcc = 5 V		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Voltage input low	V_{IL}		0.8		0.8	V	1
Voltage input high	V_{IH}	2.0		2.5		V	2
Input current (V_{IN} = 0V)	I_{IN}	Typical +/- 50				uA	2
Voltage output low (I_{OL} = 4mA)	V_{OL}		0.5		0.5	V	2
Voltage output high (I_{OH} = -4mA)	V_{OH}	2.4	3.3	3.0	5	V	2
Data input capacitance (All inputs except **CK** and **C[0:15]**)	C_{IN}	Typical 4				pF	1
Clock input capacitance (**CK** input)	C_{CK}	Typical 10				pF	1
Control data capacitance (**C[0:15]** I/O pins)	C_{CON}	Typical 6				pF	1

Notes:

1. Controlled by design and process and not directly tested. Verified on initial parts evaluation.
2. Each part is tested at 85^{o}C for the given specification.

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4.5 AC CHARACTERISTICS

Table 5: AC Characteristics (-40 TO +85°C Ambient, unless noted)

PARAMETER	SYMBOL	3.3V +/- 5%		5 V +/- 5%		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Clock Frequency	F_{CK}	0.01	45	0.01	80	MHz	2, 3, 4
Clock low period (Below V_{IL})	t_{CKL}	8		5		ns	1
Clock high period (Above V_{IH})	t_{CKH}	8		5		ns	1
Data setup before **CK** goes high (**X, SS, AS** or **GS**)	t_{SU}	4		2		ns	1
Data hold time after **CK** goes high	t_{HD}	0		0		ns	1
Data output delay from rising edge of **CK**. (**I, Q, WS, IFLAG, OS, OFLOW, SO**	t_{DLY}	2	13	2	9	ns	1, 5
Data to tristate delay (**I** or **Q** to hiZ from **OEI** or **OEQ**)	t_{DZ}	2	5	2	5		1
Tristate to data output delay (**I** or **Q** valid from **OEI** or **OEQ**)	t_{ZD}	3	13	3	9	ns	1, 5
Control Setup before **CS** goes low (**A**, **R/W** during read, and **A**, **R/W**, **C** during write)	t_{CSU}	10		10		ns	1
Control hold after **CS** goes high (**A**, **R/W** during read, and **A**, **R/W**, **C** during write)	t_{CHD}	10		10		ns	1
Control strobe (**CS**) pulse width (Write operation)	t_{CSPW}	60		30		ns	1,6
Control output delay **CS** low to **C** (Read Operation)	t_{CDLY}		120		90	ns	1,6
Control tristate delay after **CS** goes high	t_{CZ}		20		10	ns	1
Quiescent supply current (V_{IN}=0 or V_{CC}, F_{CK} = 1KHz)	I_{CCQ}		200		200	uA	1
Supply current (F_{CK} =45MHz)	I_{CC}		386		585	mA	1, 7

Notes:

1. Controlled by design and process and not directly tested. Verified on initial part evaluation.
2. Each part is tested at 25 deg C for the given specification.
3. Temperature range is verified by lot sampling.
4. The chip may not operate properly at clock frequencies below MIN and MAX.
5. Capacitive output load is 20pf. Delays are measured from the rising edge of the clock to the output level rising above V_{IH} or Falling below V_{IL}.
6. Capacitive output load is 80pf.
7. Current changes linearly with voltage and clock speed. Icc (MAX) $= \left(\frac{VCC}{5}\right)\left(\frac{F_{CK}}{45M}\right)585\text{mA}$

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5.0 APPLICATION NOTES

5.1 POWER AND GROUND CONNECTIONS

The GC1012A chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC} and GND pins. If possible the GC1012A chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 and 0.1 μf) adjacent to each GC1012A chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors adjacent to each V_{CC} and GND pair.

IMPORTANT

The GC1012A chip may not operate properly if these power and ground guidelines are violated.

5.2 STATIC SENSITIVE DEVICE

The GC1012A chip is fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments.

5.3 80 MHZ OPERATION

Care must be taken in generating the clock when operating the GC1012A chip at its full 80 MHz clock rate. The user must insure that the clock is above 2 volts for at least 5 nanoseconds and is below 1 volt for at least 5 nanoseconds. At 80 MHz the clock period is only 12.5 nanoseconds so that the clock must have a duty cycle of exactly 50%, and the rise and fall times can only be 1.25 nanoseconds each. One must also be careful to prevent clock undershoot below ground. An ideal clock at 80 MHz would be a square wave with a low voltage of 0.5 volts and a high voltage of 2.5 volts.

5.4 REDUCED VOLTAGE OPERATION

The power consumed by the GC1012A chip can be greatly reduced by operating the chip at the lowest V_{CC} voltage which will meet the application's timing requirements. When operating at a reduced voltage, GRAYCHIP recommends driving the GC1012A chip inputs with 5 volt to 3 volt interface chips.

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5.5 SYNCHRONIZING MULTIPLE GC1012A CHIPS

A system containing a bank of GC1012A chips will need to be synchronized so that the output frames from each chip are aligned, and, if desired, so that their frequency accumulators are running synchronously. The GC1000 Input Switch chip has built in sync counters which are designed specifically for this purpose. If the GC1000 chip is not used, then the one-shot strobe (see Section 3.7) can be used. The bank of chips should be interconnected so that the **$\overline{\text{OS}}$** pin of one GC1012A chip is tied to the **$\overline{\text{SS}}$** input of all of the chips. The one-shot strobe mode can then be used to simultaneously synchronize all of the chips. The **$\overline{\text{OS}}$** pin of a second GC1012A chip should be tied to the **$\overline{\text{AS}}$** input of all of the chips. The one-shot mode of the second chip can be used to synchronize the frequency accumulators whenever the tuning frequency has been changed.

5.6 PROCESSING COMPLEX DATA

Two GC1012A chips can be used to process complex input data by using one chip to process the I-input data and the other to process the Q-input data. If the two chips are synchronized as discussed above, then the complex output stream can be reconstructed by adding and subtracting the I and Q outputs of the two chips. A programmable gate array chip such as from XILINX would be ideal for this post-processing. The configuration for processing complex data is illustrated in Figure 6.

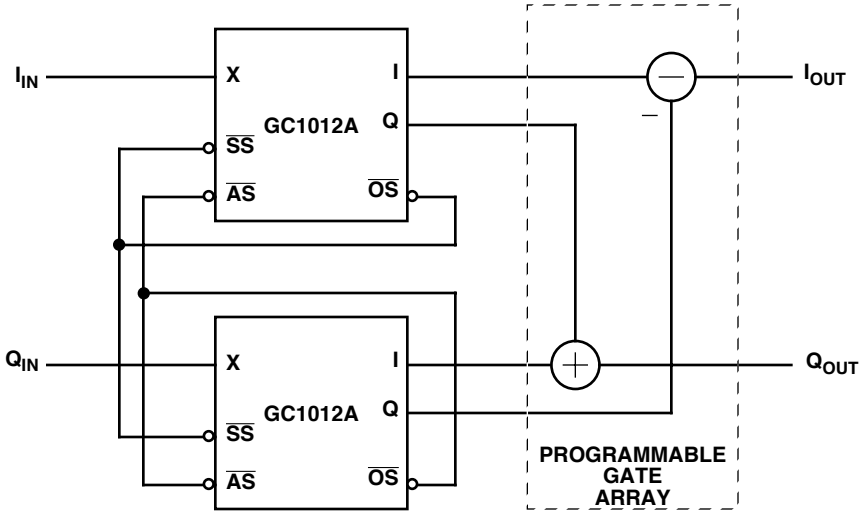


Figure 6. Processing Complex Input Data

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5.7 EXAMPLE RECEIVER ARCHITECTURE

An example digital receiver architecture using the GC1012A chip is shown in Figure 7.

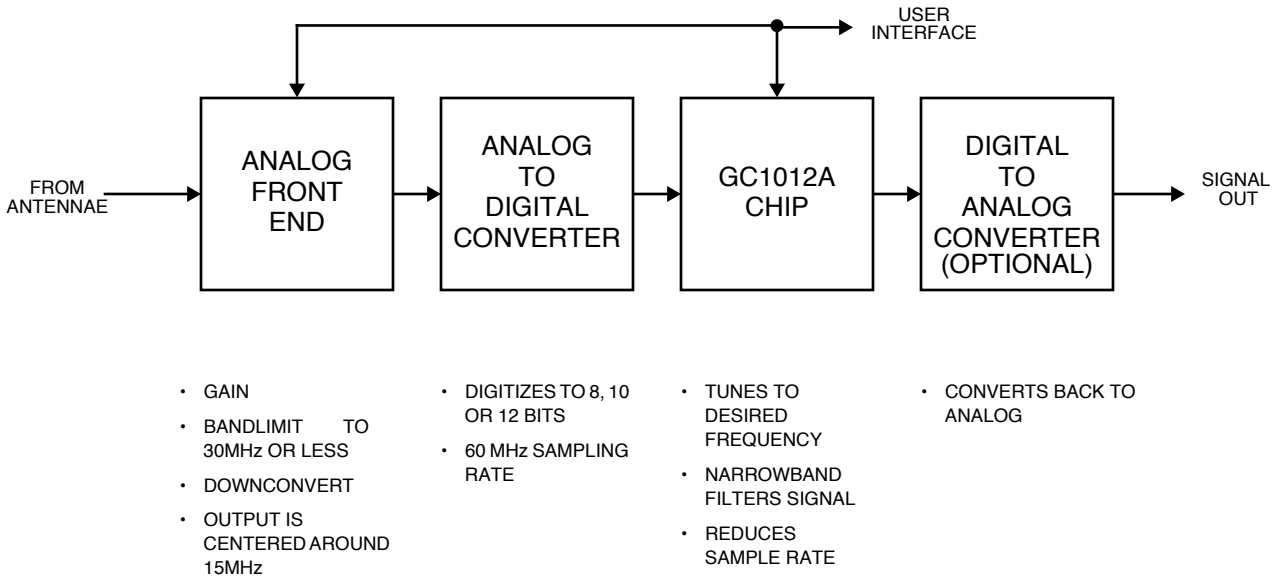


Figure 7. Example Digital Receiver Architecture

The receiver contains an analog front end which downconverts up to 30MHz of radio spectrum to an IF frequency around 15MHz[1]. It also adjusts the gain of the signal so that it fills the dynamic range of the analog to digital converter (ADC). The ADC digitizes the signal using up to 12 bits of resolution at a sampling rate up to 60 MHZ. The GC1012A chip tunes, downconverts, and narrowband filters desired frequencies from within the 30 MHz band. The GC1012A output can either be converted back to analog or kept in its digital state for subsequent signal processing.

1. Note that the HF spectrum (1 to 30MHz) can be digitized directly.

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5.8 LATENCY THROUGH THE GC1012A

Two latencies are of interest, the latency from a step function in to a step function out (midpoint), and the latency from a step function until the end of the “ringing” in the step function output (endpoint). These latencies are:

Table 6: Latency

Output Mode	Midpoint	Endpoint	Values of D (decimation)
Real	41 + 20D	41 + 40D	1, 2, 4, 8, 16 and 32
Complex	35 + 10D	35 + 20D	2, 4, 8, 16, 32 and 64

Another latency of interest is the delay from SS input to stable WS. The WS strobe becomes stable and is low after 9 clocks, before 9 clocks the WS is unknown and may go high at any time. The delay until the first valid high WS is a function of decimation. For decimate by 2 the delay from SS is 10 clocks, for 4 the delay is 12 clocks, for 8 the delay is 16 clocks and for decimation ratios of 16, 32 and 64 the delay is 24 clocks. WS is high at clock 24 for all decimations.

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Appendix B: Analog Devices AD6640 – 12–Bit, 65 MSPS IF Sampling A/D Converter

Included for your reference on the following pages is the data sheet for the AD6640 12–bit, 65 Megasample/second IF sampling Analog to Digital Converter, provided by the courtesy of Analog Devices Inc., Norwood, MA.

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12-Bit, 65 MSPS IF Sampling A/D Converter

AD6640

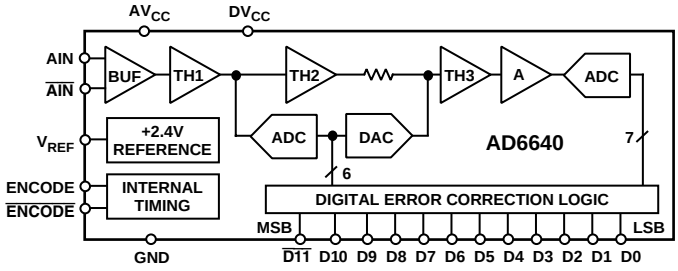
FEATURES

65 MSPS Minimum Sample Rate
80 dB Spurious-Free Dynamic Range
IF-Sampling to 70 MHz
710 mW Power Dissipation
Single +5 V Supply
On-Chip T/H and Reference
Twos Complement Output Format
3.3 V or 5 V CMOS-Compatible Output Levels

APPLICATIONS

Cellular/PCS Base Stations
Multichannel, Multimode Receivers
GPS Anti-Jamming Receivers
Communications Receivers
Phased Array Receivers

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD6640 is a high speed, high performance, low power, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference are included on-chip to provide a complete conversion solution. The AD6640 runs on a single +5 V supply and provides CMOS-compatible digital outputs at 65 MSPS.

Specifically designed to address the needs of multichannel, multimode receivers, the AD6640 maintains 80 dB spurious-free dynamic range (SFDR) over a bandwidth of 25 MHz. Noise performance is also exceptional; typical signal-to-noise ratio is 68 dB.

The AD6640 is built on Analog Devices' high speed complementary bipolar process (XFCB) and uses an innovative multipass architecture. Units are packaged in a 44-terminal Plastic Thin Quad Flatpack (TQFP) specified from –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate is 65 MSPS.
2. Fully differential analog input stage specified for frequencies up to 70 MHz; enables "IF Sampling."
3. Low power dissipation: 710 mW off a single +5 V supply.
4. Digital outputs may be run on +3.3 V supply for easy interface to digital ASICs.
5. Complete Solution: reference and track-and-hold.
6. Packaged in small, surface mount, plastic 44-terminal TQFP.

REV. 0

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AD6640–SPECIFICATIONS

DC SPECIFICATIONS (AV_{CC} = +5 V, DV_{CC} = +3.3 V; T_{MIN} = –40°C, T_{MAX} = +85°C)

Parameter	Temp	Test Level	AD6640AST Min	Typ	Max	Units
RESOLUTION				12		Bits
ACCURACY						
No Missing Codes	+25°C	I		GUARANTEED		
Offset Error	Full	VI	–10	3.5	+10	mV
Gain Error	Full	VI	–10	4.0	+10	% FS
Differential Nonlinearity (DNL)[1]	+25°C	I	–1.0	±0.5	+1.5	LSB
Integral Nonlinearity (INL)[1]	Full	V		±1.25		LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		50		ppm/°C
Gain Error	Full	V		100		ppm/°C
POWER SUPPLY REJECTION (PSRR)	Full	V		±0.5		mV/V
REFERENCE OUT (V_{REF})[2]	Full	V		2.4		V
ANALOG INPUTS (AIN, $\overline{AIN}$)[3]						
Analog Input Common-Mode Range[4]	Full	V		V_{REF} ± 0.05		V
Differential Input Voltage Range	Full	V		2.0		V p-p
Differential Input Resistance	Full	IV	0.7	0.9	1.1	kΩ
Differential Input Capacitance	+25°C	V		1.5		pF
POWER SUPPLY						
Supply Voltage						
AV_{CC}	Full	VI	4.75	5.0	5.25	V
DV_{CC}	Full	VI	3.0	3.3	5.25	V
Supply Current						
IA_{VCC} (AV_{CC} = 5.0 V)	Full	VI		135	160	mA
ID_{VCC} (DV_{CC} = 3.3 V)	Full	VI		10	20	mA
POWER CONSUMPTION	Full	VI		710	865	mW

NOTES
[1]ENCODE = 20 MSPS
[2]If V_{REF} is used to provide a dc offset to other circuits, it should first be buffered.
[3]The AD6640 is designed to be driven differentially. Both AIN and $\overline{AIN}$ should be driven at levels V_{REF} ± 0.5 volts. The input signals should be 180 degrees out of phase to produce a 2 V p-p differential input signal. See Driving the Analog Inputs section for more details.
[4]Analog input common-mode range specifies the offset range the analog inputs can tolerate in dc-coupled applications (see Figure 35 for more detail).

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AV_{CC} = +5 V, DV_{CC} = +3.3 V; T_{MIN} = –40°C, T_{MAX} = +85°C)

Parameter	Temp	Test Level	AD6640AST Min	Typ	Max	Units
LOGIC INPUTS (ENC, $\overline{ENC}$)[1]						
Encode Input Common-Mode Range[2]	Full	IV	0.2		2.2	V
Differential Input Voltage	Full	IV	0.4			V p-p
Single-Ended Encode					10	V p-p
Logic Compatibility[3]				TTL/CMOS		
Logic "1" Voltage	Full	VI	2.0		5.0	V
Logic "0" Voltage	Full	VI	0		0.8	V
Logic "1" Current (V_{INH} = 5 V)	Full	VI	500	650	800	µA
Logic "0" Current (V_{INL} = 0 V)	Full	VI	–400	–320	–200	µA
Input Capacitance	+25°C	V		2.5		pF
LOGIC OUTPUTS ($\overline{D11}$–D0)[4]						
Logic Compatibility				CMOS		
Logic "1" Voltage (DV_{CC} = +3.3 V)	Full	VI	2.8	DV_{CC} – 0.2		V
Logic "0" Voltage (DV_{CC} = +3.3 V)	Full	VI		0.2	0.5	V
Logic "1" Voltage (DV_{CC} = +5.0 V)	Full	IV	4.5	DV_{CC} – 0.3		V
Logic "0" Voltage (DV_{CC} = +5.0 V)	Full	IV		0.35	0.5	V
Output Coding				Twos Complement		

NOTES
[1]Best dynamic performance is obtained by driving ENC and $\overline{ENC}$ differentially. See Encoding the AD6640 section for more details. Performance versus ENC/$\overline{ENC}$ power is shown in Figure 18 under Typical Performance Characteristics.
[2]For dc-coupled applications, Encode Input Common-Mode Range specifies the common-mode range the encode inputs can tolerate when driven differentially by minimum differential input voltage of 0.4 V p-p. For differential input voltage swings greater than 0.4 V p-p, the common-mode range will change. The minimum value insures that the input voltage on either encode pin does not go below 0 V. The maximum value insures that the input voltage on either encode pin does not go below 2.0 V or above AV_{CC} (e.g., for a differential input swing of 0.8 V, the min and max common-mode specs become 0.4 V and 2.4 V respectively).
[3]ENC or $\overline{ENC}$ may be driven alone if desired, but performance will likely be degraded. Logic Compatibility specifications are provided to show that TTL or CMOS clock sources will work. When driving only one encode input, bypass the complementary input to GND with 0.01 µF.
[4]Digital output load is one LCX gate.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS[1] (AV_{CC} = +5 V, DV_{CC} = +3.3 V; ENCODE & $\overline{ENCODE}$ = 65 MSPS; T_{MIN} = –40°C, T_{MAX} = +85°C)

Parameter (Conditions)	Temp	Test Level	AD6640AST Min	Typ	Max	Units
Maximum Conversion Rate	Full	VI	65			MSPS
Minimum Conversion Rate[2]	Full	IV			6.5	MSPS
Aperture Delay (t_A)	+25°C	V		400		ps
Aperture Uncertainty (Jitter)	+25°C	V		0.3		ps rms
ENCODE Pulsewidth High[3]	+25°C	IV	6.5			ns
ENCODE Pulsewidth Low	+25°C	IV	6.5			ns
Output Delay (t_{OD}) DV_{CC} +3.3 V/5.0 V[4]	Full	IV	8.5	10.5	12.5	ns

NOTES
[1]All switching specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially.
[2]A plot of Performance vs. Encode is shown in Figure 16 under Typical Performance Characteristics.
[3]A plot of Performance vs. Duty Cycle (Encode = 65 MSPS) is shown in Figure 17 under Typical Performance Characteristics.
[4]Outputs driving one LCX gate. Delay is measured from differential crossing of ENC, $\overline{ENC}$ to the time when all output data bits are within valid logic levels.
Specifications subject to change without notice.

AC SPECIFICATIONS[1] (AV_{CC} = +5 V, DV_{CC} = +3.3 V; ENCODE & $\overline{ENCODE}$ = 65 MSPS; T_{MIN} = –40°C, T_{MAX} = +85°C)

Parameter (Conditions)		Temp	Test Level	AD6640AST Min	Typ	Max	Units
SNR							
Analog Input	2.2 MHz	+25°C	V		68		dB
@ –1 dBFS	15.5 MHz	+25°C	I	64	67.7		dB
	31.0 MHz	+25°C	V		67.5		dB
	69.0 MHz	+25°C	V		66		dB
SINAD							
Analog Input	2.2 MHz	+25°C	V		68		dB
@ –1 dBFS	15.5 MHz	+25°C	I	63.5	67.2		dB
	31.0 MHz	+25°C	V		67.0		dB
	69.0 MHz	+25°C	V		65.5		dB
Worst Harmonic[2] (2nd or 3rd)							
Analog Input	2.2 MHz	+25°C	V		80		dBc
@ –1 dBFS	15.5 MHz	+25°C	I	74	80		dBc
	31.0 MHz	+25°C	V		79.5		dBc
	69.0 MHz	+25°C	V		78.5		dBc
Worst Harmonic[2] (4th or Higher)							
Analog Input	2.2 MHz	+25°C	V		85		dBc
@ –1 dBFS	15.5 MHz	+25°C	I	74	85		dBc
	31.0 MHz	+25°C	V		85		dBc
	69.0 MHz	+25°C	V		84		dBc
Multitone SFDR (w/Dither)[3]							
Eight Tones @ –20 dBFS		Full	V		90		dBFS
Two-Tone IMD Rejection[4]							
F1, F2 @ –7 dBFS		Full	V		80		dBc
Analog Input Bandwidth[5]		+25°C	V		300		MHz

NOTES
[1]All ac specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially.
[2]For a single test tone at –1 dBFS, the worst case spectral performance is typically limited by the direct or aliased 2nd or 3rd harmonic. If a system is designed such that the 2nd and 3rd harmonics fall out-of-band, overall performance in the band of interest is typically improved by 5 dB. Worst Harmonic (4th or Higher) includes 4th and higher order harmonics and all other spurious components. Reference Figure 12 for more detail.
[3]See Overcoming Static Nonlinearities with Dither section for details on improving SFDR performance. To measure SFDR, eight tones from 14 MHz to 18 MHz (0.5 MHz spacing) are swept from –20 dBFS to –90 dBFS. An open channel at 16 MHz is used to monitor SFDR.
[4]F1 = 14.9 MHz, F2 = 16 MHz.
[5]Specification is small signal bandwidth. Plots of Performance versus Analog Input Frequency are shown in Figures 10, 11 and 12. Sampling wide bandwidths (5 MHz–15 MHz) should be limited to 70 MHz center frequency.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Min	Max	Units
ELECTRICAL			
AV_{CC} Voltage	0	7	V
DV_{CC} Voltage	0	7	V
Analog Input Voltage	0	AV_{CC}	V
Analog Input Current		25	mA
Digital Input Voltage (ENCODE)	0	AV_{CC}	V
Digital Output Current	–10	10	mA
ENVIRONMENTAL[2]			
Operating Temperature Range (Ambient)	–40	+85	°C
Maximum Junction Temperature		+150	°C
Lead Temperature (Soldering, 10 sec)		+300	°C
Storage Temperature Range (Ambient)	–65	+150	°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (44-terminal TQFP); θ_{JA} = 55°C/W.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C; sample tested at temperature extremes.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6640AST	–40°C to +85°C (Ambient)	44-Terminal TQFP (Thin Quad Plastic Flatpack)	ST-44
AD6640ST/PCB		Evaluation Board with AD6640AST	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6640 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

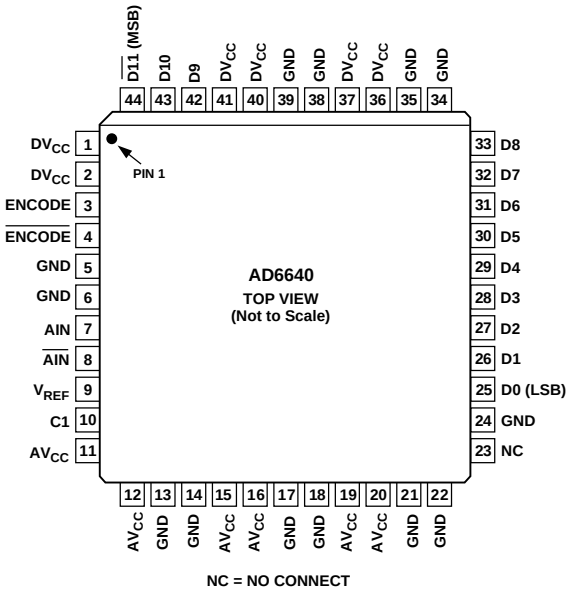


PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1, 2, 36, 37, 40, 41	DV_{CC}	+3.3 V/+5 V Power Supply (Digital). Powers output stage only.
3	ENCODE	Encode Input. Data conversion initiated on rising edge.
4	$\overline{\text{ENCODE}}$	Complement of ENCODE. Drive differentially with ENCODE or bypass to Ground for single-ended clock mode. See Encoding the AD6640 section.
5, 6, 13, 14, 17, 18, 21, 22, 24, 34, 35, 38, 39	GND	Ground.
7	AIN	Analog Input.
8	$\overline{\text{AIN}}$	Complement of Analog Input.
9	V_{REF}	Internal Voltage Reference. Nominally +2.4 V. Bypass to Ground with 0.1 µF + 0.01 µF microwave chip capacitor.
10	C1	Internal Bias Point. Bypass to ground with 0.01 µF capacitor.
11, 12, 15, 16, 19, 20	AV_{CC}	+5 V Power Supply (Analog).
23	NC	No Connect.
25	D0 (LSB)	Digital Output Bit (Least Significant Bit).
26–33	D1–D8	Digital Output Bits.
42, 43	D9–D10	Digital Output Bits.
44	$\overline{\text{D11}}$ (MSB)[1]	Digital Output Bit (Most Significant Bit).

NOTE
[1]Output coded as twos complement.

PIN CONFIGURATION



DEFINITION OF SPECIFICATIONS

Analog Bandwidth (Small Signal)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in logic "1" state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable Encode duty cycle.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (always related back to converter full scale).

Worst Harmonic
The ratio of the rms signal amplitude to the rms value of the worst harmonic component, reported in dBc.

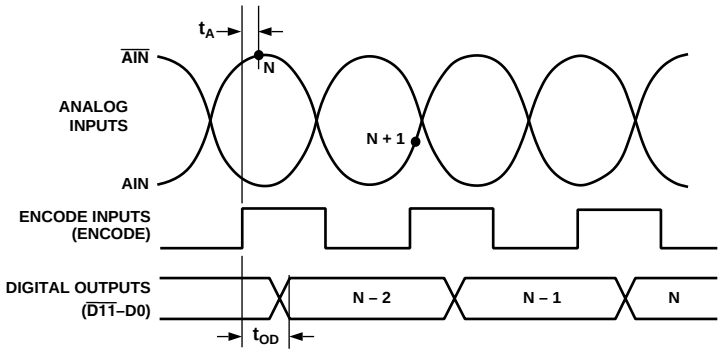


Figure 1. Timing Diagram

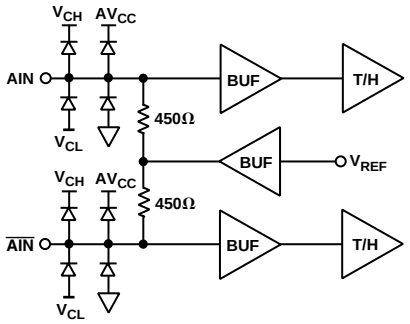


Figure 2. Analog Input Stage

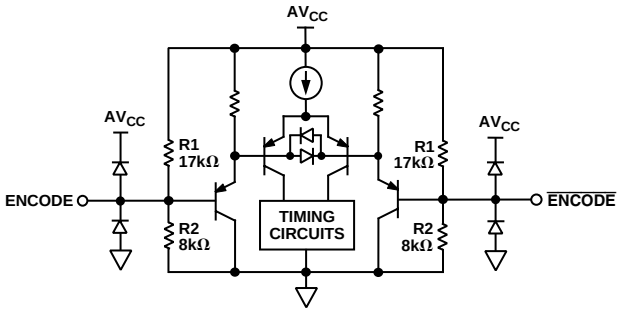


Figure 3. Encode Inputs

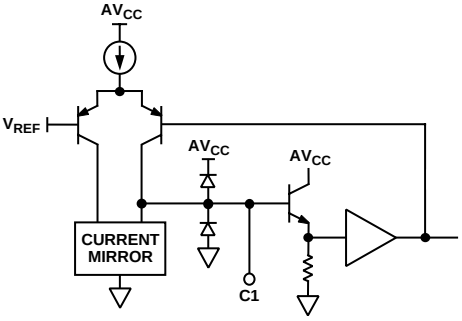


Figure 4. Compensation Pin, C1

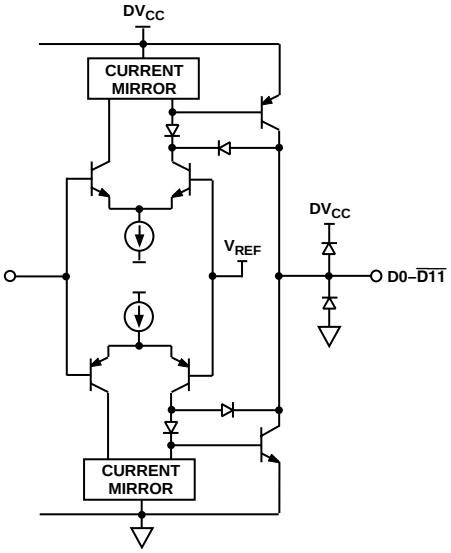


Figure 5. Digital Output Stage

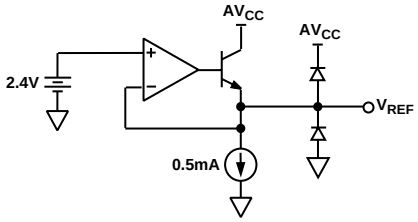


Figure 6. 2.4 V Reference

AD6640–Typical Performance Characteristics

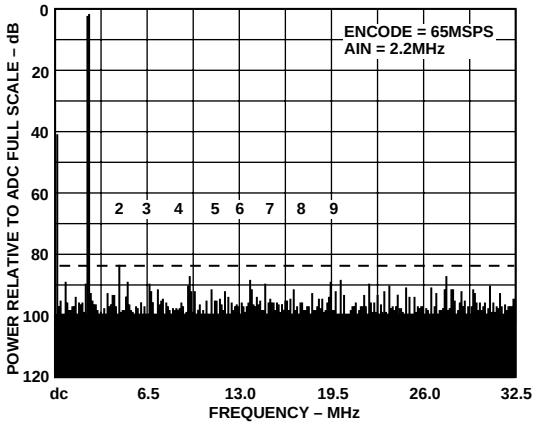


Figure 7. Single Tone at 2.2 MHz

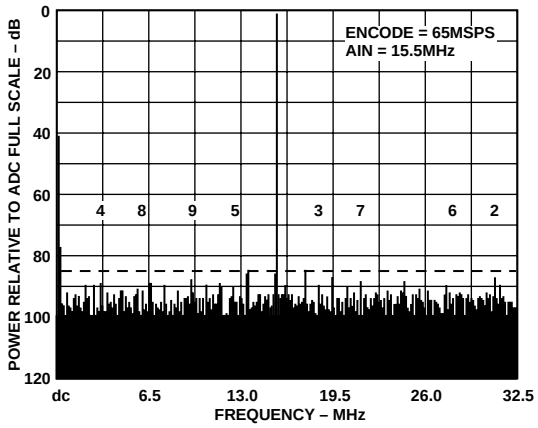


Figure 8. Single Tone at 15.5 MHz

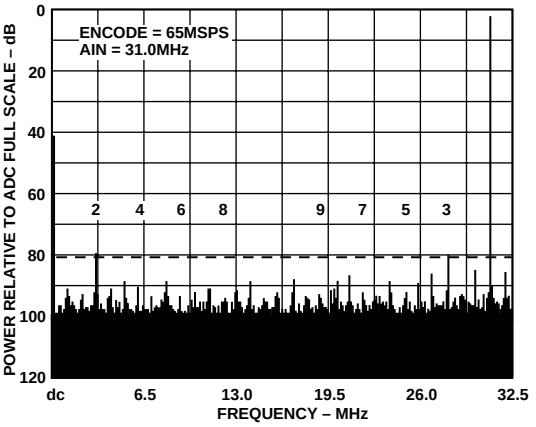


Figure 9. Single Tone at 31.0 MHz

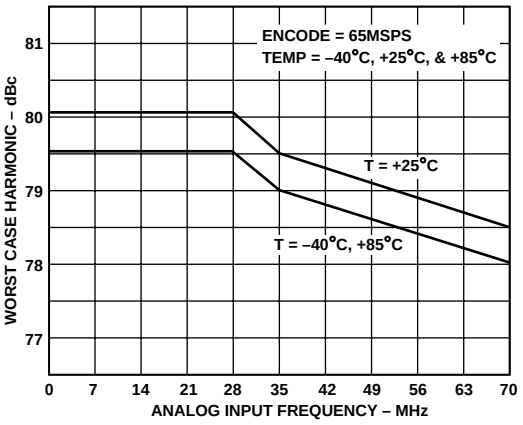


Figure 10. Harmonics vs. AIN

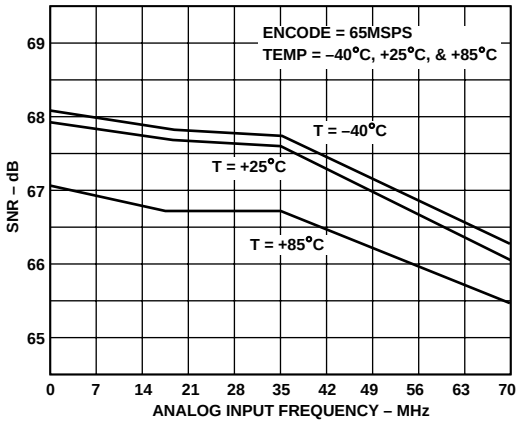


Figure 11. Noise vs. AIN

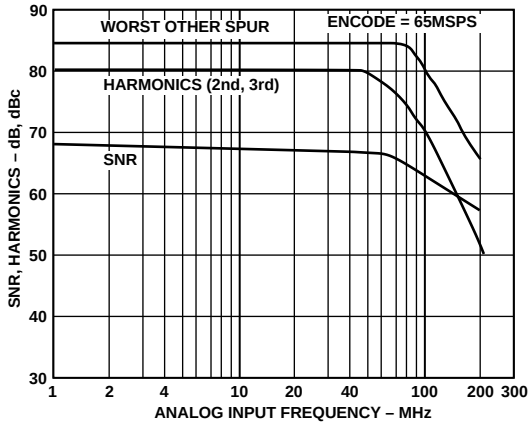


Figure 12. Harmonics, Noise vs. AIN

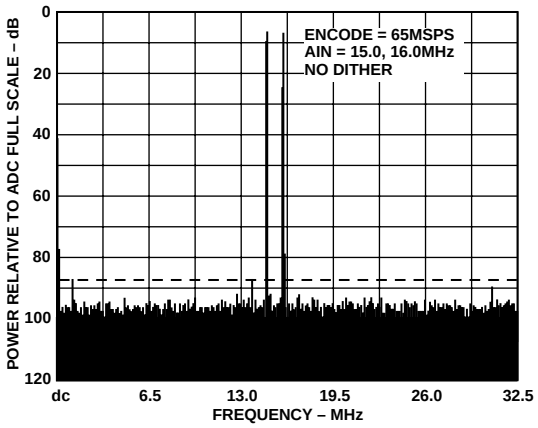


Figure 13. Two Tones at 15.0 MHz & 16.0 MHz

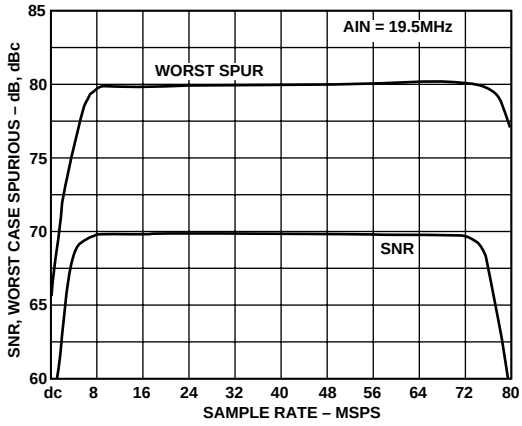


Figure 16. SNR, Worst Spurious vs. Encode

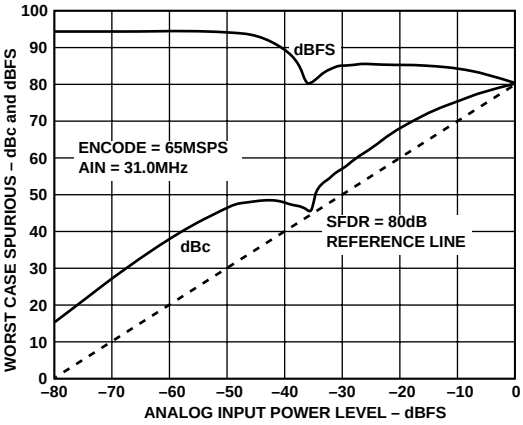


Figure 14. Single Tone SFDR

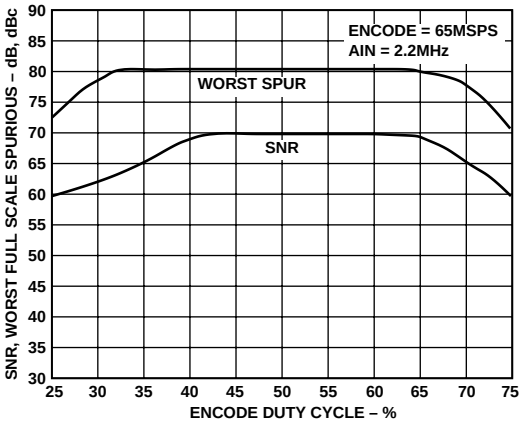


Figure 17. SNR, Worst Spurious vs. Duty Cycle

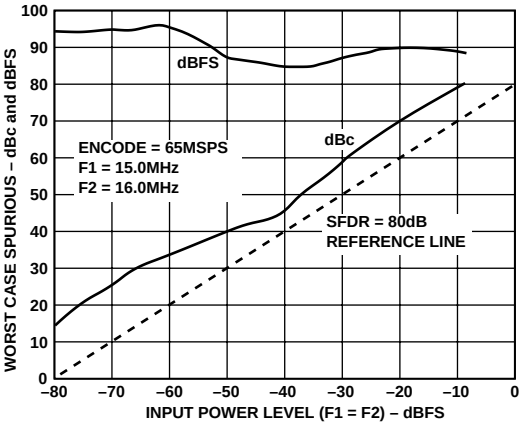


Figure 15. Two Tone SFDR

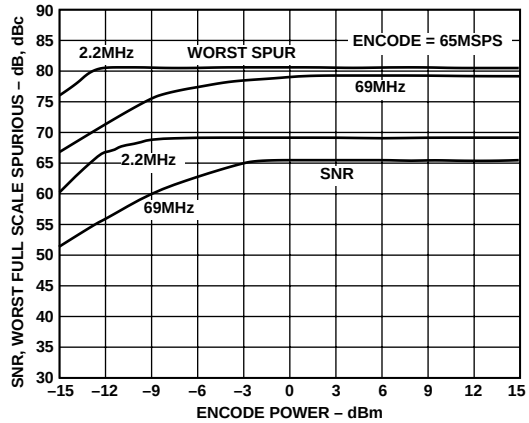


Figure 18. SNR, Worst Spurious vs. Encode Power

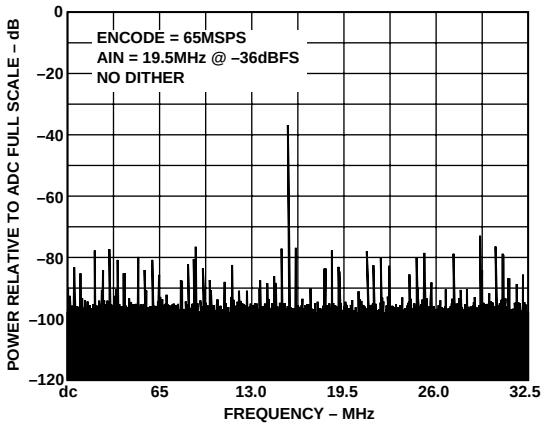


Figure 19. 16K FFT without Dither

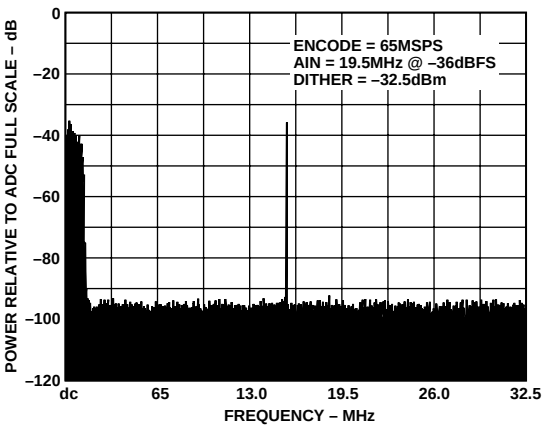


Figure 22. 16K FFT with Dither

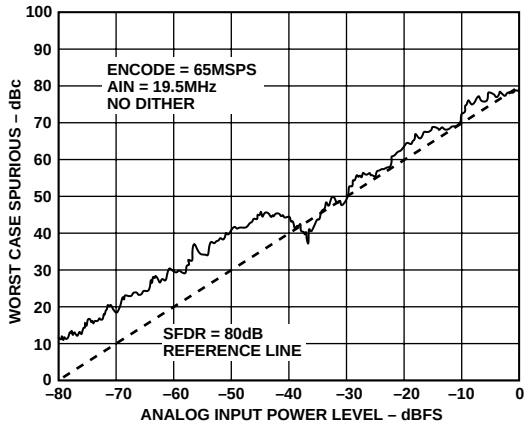


Figure 20. SFDR without Dither

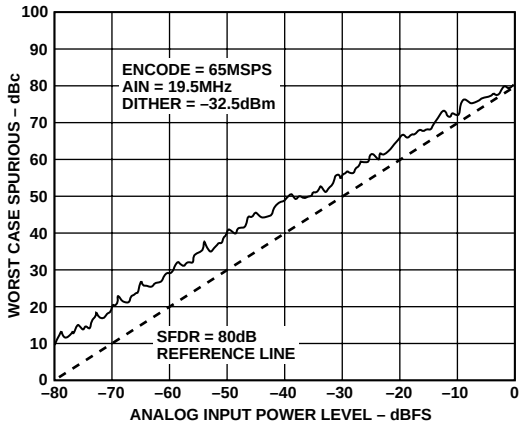


Figure 23. SFDR with Dither

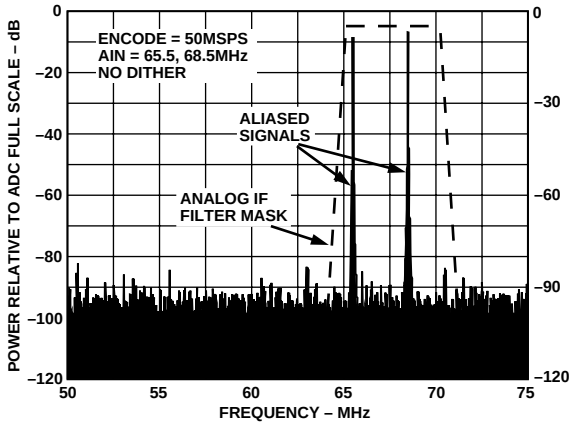


Figure 21. IF-Sampling at 70 MHz without Dither

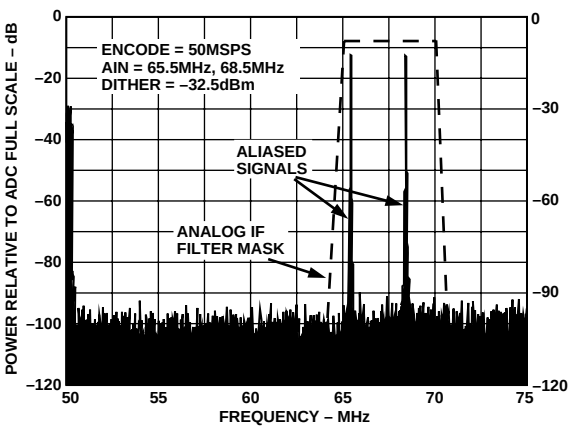


Figure 24. IF-Sampling at 70 MHz with Dither

THEORY OF OPERATION

The AD6640 analog-to-digital converter (ADC) employs a two-stage subrange architecture. This design approach ensures 12-bit accuracy, without the need for laser trim, at low power.

As shown in the functional block diagram, the AD6640 has complementary analog input pins, AIN and $\overline{\text{AIN}}$. Each analog input is centered at 2.4 volts and should swing ±0.5 volts around this reference (ref. Figure 2). Since AIN and $\overline{\text{AIN}}$ are 180 degrees out of phase, the differential analog input signal is 2 volts peak-to-peak.

Both analog inputs are buffered prior to the first track-and-hold, TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of a 6-bit coarse ADC. The digital output of the coarse ADC drives a 6-bit DAC; the DAC is 12 bits accurate. The output of the 6-bit DAC is subtracted from the delayed analog signal at the input of TH3 to generate a residue signal. TH2 is used as an analog pipeline to null out the digital delay of the coarse ADC.

The 6-bit coarse ADC word and 7-bit residue word are added together and corrected in the digital error correction logic to generate the output word. The result is a 12-bit parallel digital CMOS-compatible word, coded as twos complement.

APPLYING THE AD6640

Encoding the AD6640

Best performance is obtained by driving the encode pins differentially. However, the AD6640 is also designed to interface with TTL and CMOS logic families. The source used to drive the ENCODE pin(s) must be clean and free from jitter. Sources with excessive jitter will limit SNR (reference Equation 1 under "Noise Floor and SNR").

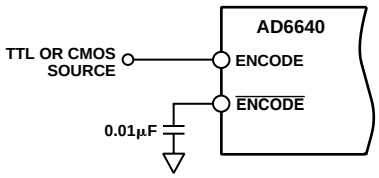


Figure 25. Single-Ended TTL/CMOS Encode

The AD6640 encode inputs are connected to a differential input stage (see Figure 3 under EQUIVALENT CIRCUITS). With no input signal connected to either ENCODE pin, the voltage dividers bias the inputs to 1.6 volts. For TTL or CMOS usage, the encode source should be connected to ENCODE, Pin 3. $\overline{\text{ENCODE}}$ should be decoupled using a low inductance or microwave chip capacitor to ground.

If a logic threshold other than the nominal 1.6 V is required, the following equations show how to use an external resistor, Rx, to raise or lower the trip point (see Figure 3; R1 = 17 kΩ, R2 = 8 kΩ).

$$V_l = \frac{5R2Rx}{R1R2 + R1Rx + R2Rx}$$ to lower logic threshold.

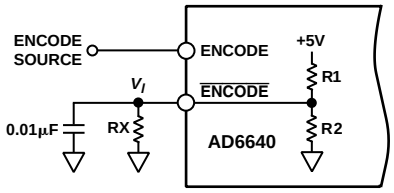


Figure 26. Lower Logic Threshold for Encode

$$V_l = \frac{5R2}{R2 + \frac{R1R_X}{R1 + R_X}}$$ to raise logic threshold.

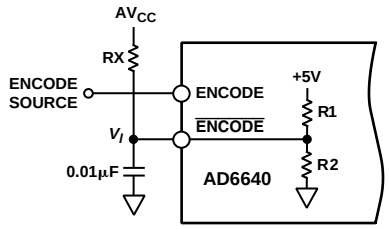


Figure 27. Raise Logic Threshold for Encode

While the single-ended encode will work well for many applications, driving the encode differentially will provide increased performance. Depending on circuit layout and system noise, a 1 dB to 3 dB improvement in SNR can be realized. It is not recommended that differential TTL logic be used however, because most TTL families that support complementary outputs are not delay or slew rate matched. Instead, it is recommended that the encode signal be ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins.

The simplest option is shown below. The low jitter TTL signal is coupled with a limiting resistor, typically 100 ohms, to the primary side of an RF transformer (these transformers are inexpensive and readily available; part number in Figure 28 is from Mini-Circuits). The secondary side is connected to the ENCODE and $\overline{\text{ENCODE}}$ pins of the converter. Since both encode inputs are self-biased, no additional components are required.

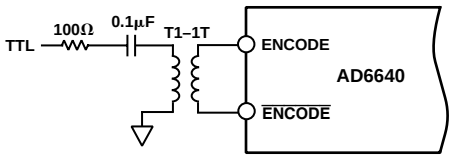


Figure 28. TTL Source – Differential Encode

A clean sine wave may be substituted for a TTL clock. In this case, the matching network is shown below. Select a transformer ratio to match source and load impedances. The input impedance of the AD6640 encode is approximately 11 kΩ differentially. Therefore "R," shown in the Figure 29, may be any value that is convenient for available drive power.

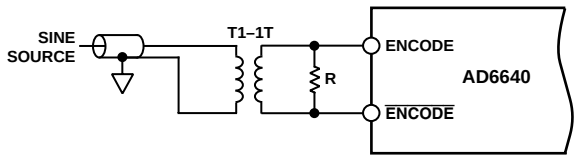


Figure 29. Sine Source – Differential Encode

If a low jitter ECL clock is available, another option is to ac-couple a differential ECL signal to the encode input pins as shown below. The capacitors shown here should be chip capacitors but do not need to be of the low inductance variety.

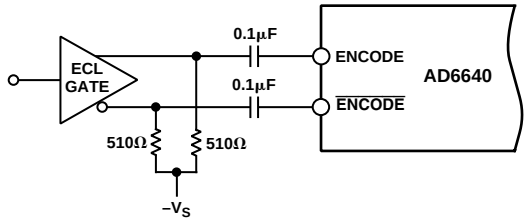


Figure 30. Differential ECL for Encode

As a final alternative, the ECL gate may be replaced by an ECL comparator. The input to the comparator could then be a logic signal or a sine signal.

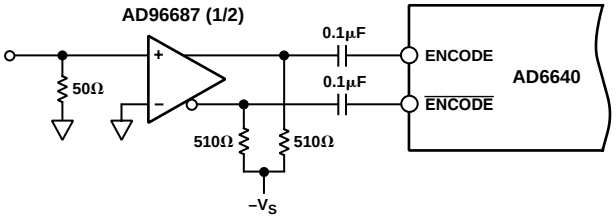


Figure 31. ECL Comparator for Encode

Driving the Analog Input

Because the AD6640 operates from a single +5 volt supply, the analog input voltage range is offset from ground by 2.4 volt. Each analog input connects through a 450 ohm resistor to the 2.4 volt bias voltage and to the input of a differential buffer (Figure 32). This resistor network on the input properly biases the followers for maximum linearity and range. Therefore, the analog source driving the AD6640 should be ac-coupled to the input pins. Since the differential input impedance of the AD6640 is 0.9 kΩ, the analog input power requirement is only –3 dBm, simplifying the drive amplifier in many cases.

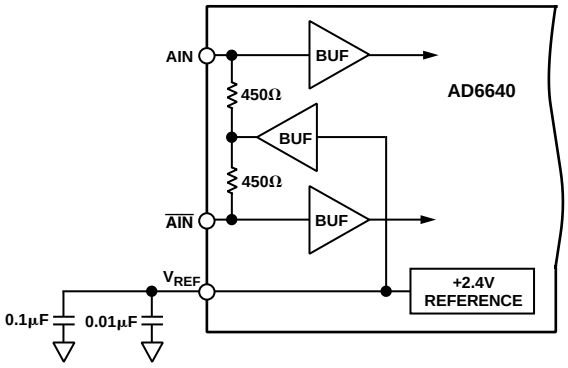


Figure 32. Differential Analog Inputs

To take full advantage of this high input impedance, a 20:1 transformer would be required. This is a large ratio and could result in unsatisfactory performance. In this case, a lower step-up ratio could be used. For example, if R_T were set to 260 ohms, along with a 4:1 transformer, the input would match to a 50 ohm source with a full-scale drive of +4 dBm (Figure 33). Note that the external load resistor, R_T, is in parallel with the AD6640 analog input resistance of 900 ohms. The external resistor value can be calculated from the following equation:

$$R_T = \frac{1}{\frac{1}{Z} - \frac{1}{900}}$$

where Z is the desired impedance (200 Ω for a 4:1 transformer with 50 Ω input source).

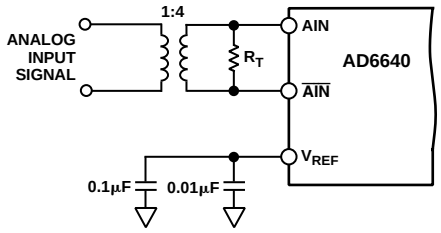


Figure 33. Transformer-Coupled Analog Input Signal

If the lower drive power is attractive, a combination transformer match and LC match could be employed that would use a 4:1 transformer with an LC as shown in Figure 34. This solution is useful when good performance in the third Nyquist zone is required. Such a requirement arises when digitizing high intermediate frequencies in communications receivers.

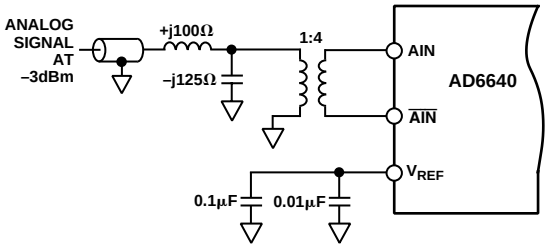


Figure 34. Low Power Drive Circuit

In applications where gain is needed but dc-coupling is not necessary, an extension of Figure 34 is recommended. A 50 ohm gain block may be placed in front of the LC matching network. Such gain blocks are readily available for commercial applications. These low cost modules can have excellent NF and intermodulation performance. This circuit is especially good for the "IF" receiver application previously mentioned.

In applications where dc-coupling is required the following circuit can be used (Figure 35). It should be noted that the addition of circuitry for dc-coupling may compromise performance in terms of noise, offset and dynamic performance. This circuit requires an inverting and noninverting signal path. Additionally, an offset must be generated so that the analog input to each pin is centered near 2.4 volts. Since the input is differential, small differences in the dc voltage at each input can translate into an offset for the circuit. The same holds true for gain mismatch. Therefore, some means of adjusting the gain and offset between

the sides should be implemented. The addition of small value resistors between the AD9631 and the AD6640 will prevent oscillation due to the capacitive input of the ADC.

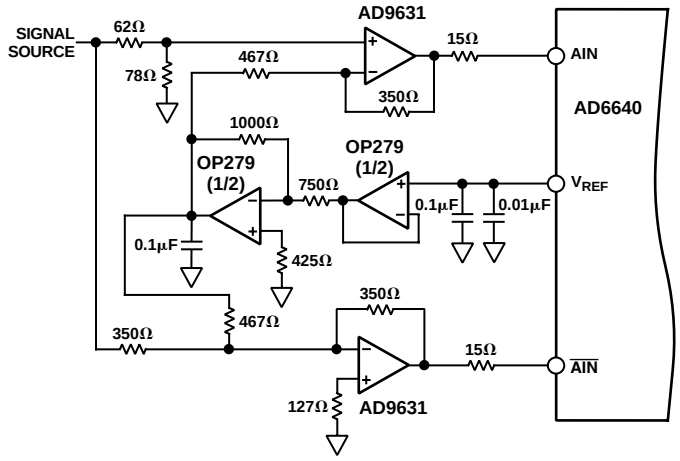


Figure 35. DC-Coupled Analog Input Circuit

Power Supplies

Care should be taken when selecting a power source. Linear supplies are strongly recommended as switching supplies tend to have radiated components that may be "received" by the AD6640. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 µF chip capacitors.

The AD6640 has separate digital and analog +5 V pins. The analog supplies are denoted AV_{CC} and the digital supply pins are denoted DV_{CC}. Although analog and digital supplies may be tied together, best performance is achieved when the supplies are separate. This is because the fast digital output swings can couple switching noise back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 volts; however the DV_{CC} supply may be varied according to output digital logic family (i.e., DV_{CC} should be connected to the same supply as the digital circuitry). The AD6640 is specified for DV_{CC} = 3.3 V as this is a common supply for digital ASICs.

Output Loading

Care must be taken when designing the data receivers for the AD6640. It is recommended that the digital outputs drive a series resistor (e.g. 348 ohms) followed by a gate like the 74LCX574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation board schematic shown in Figure 36. The digital outputs of the AD6640 have a constant rise time output stage. The output slew rate is about 1 V/ns when DV_{CC} = +5 V. A typical CMOS gate combined with PCB trace and through hole will have a load of approximately 10 pF. Therefore as each bit switches, 10 mA

$\left(10\,pF \times \frac{1V}{1\,ns}\right)$ of dynamic current per bit will flow in or out of the device. A full-scale transition can cause up to 120 mA (12 bits × 10 mA/bit) of current to flow through the digital output stages. The series resistor will minimize the output currents that can flow in the output stage. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD6640.

Layout Information

The schematic of the evaluation board (Figure 36) represents a typical implementation of the AD6640. The pinout of the AD6640 facilitates ease of use and the implementation of high frequency/high resolution design practices. All of the digital outputs are on one side while the other sides contain all of the inputs. It is highly recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. Depending on the configuration used for the encode and analog inputs, one or more capacitors are required on those input pins. The capacitors used on the $\overline{\text{ENCODE}}$ and V_{REF} pins must be a low inductance chip capacitor as referenced previously in the data sheet.

A multilayer board is recommended to achieve best results. Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate (broken only by the insertion of the series resistor). Digital data lines should be kept clear of analog and encode traces.

Evaluation Boards

The evaluation board for the AD6640 is very straightforward, consisting of power, signal inputs and digital outputs. The evaluation board includes the option for an onboard clock oscillator for the encode.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the crystal oscillator and the AV_{CC} pins of the AD6640.

The DV_{CC} power is supplied via J3, the digital interface. This digital supply connection also powers the digital gates on the PCB. By maintaining separate analog and digital power supplies, degradation in SNR and SFDR is kept to a minimum. Total power requirement is approximately 200 mA. This configuration allows for easy evaluation of different logic families (i.e., connection to a 3.3 volt logic board).

The analog input is connected via J2 and is transformer-coupled to the AD6640 (see Driving the Analog Input). The onboard termination resistor is 270 Ω. This resistor, in parallel with the AD6640's input resistance (900 Ω), provides a 50 Ω load to the analog source driving the 1:4 transformer. If a different input impedance is required, replace R16 by using the following equation

$$R16 = \frac{1}{\frac{1}{Z} - \frac{1}{900}}$$

where Z is desired input impedance (200 Ω for a 4:1 transformer with 50 Ω source).

The analog input range of the PCB is ±0.5 volts (i.e., signal ac-coupled to AD6640).

The encode signal may be generated using an onboard crystal oscillator, U1. The oscillator is socketed and may be replaced by an external encode source via J1. If an external source is used, it should be a high quality TTL source. A transformer converts the single-ended TTL signal to a differential clock (see Encoding the AD6640). Since the encode is coupled with a transformer, a sine wave could have been used; note, however, that U5 requires TTL levels to function properly.

AD6640 output data is latched using 74LCX574 (U3, U4) latches following 348 ohm series resistors. The resistors limit the current that would otherwise flow due to the digital output slew rate. The resistor value was chosen to represent a time constant of ~25% of the data rate at 65 MHz. This reduces slew rate while not appreciably distorting the data waveform. Data is latched in a pipeline configuration; a rising edge generates the new AD6640 data sample, latches the previous data at the converter output, and strobes the external data register over J3.

NOTE: Power and ground must be applied to J3 to power the digital logic section of the evaluation board.

Table I. AD6640ST/PCB Bill of Material

Item	Quantity	Reference	Description
1	2	+5 VA, GND	Banana Jack
2	11	C7–C9, C11–C17, C19	Ceramic Chip Capacitor 0805, 0.1 μF
3	2	C4, C6	Tantalum Chip Capacitor 10 μF
4	1	J3	40-Pin Double Row Male Header
5	3	J1, J2, J4	BNC Coaxial PCB Connector
6	1	R1	Surface Mount Resistor 1206, 348 Ω
7	25	R2–R14, R20–R25, R30–R35	Surface Mount Resistor 1206, 348 Ω
8	1	R15	Surface Mount Resistor 1206, 100 Ω
9	1	R16	Surface Mount Resistor 1206, 270 Ω
10	2	T1, T2	Surface Mount Transformer Mini-Circuits T4–1T, 1:4 Ratio
11	1	U1	Clock Oscillator (Optional)
12	1	DUT	AD6640AST 12-Bit–65 MSPS ADC Converter
13	2	U3, U4	74LCX574 Octal Latch
14	1	U5	74LVQ00 Quad Two Input NAND Gate
15	1	C1, C18	Ceramic Chip Capacitor 0508, 0.01 μF Low Inductance
16	2	C2, C3	Ceramic Chip Capacitor 0508, 0.1 μF Low Inductance
17	2	CR1, CR2	1N2810 Schottky Diode

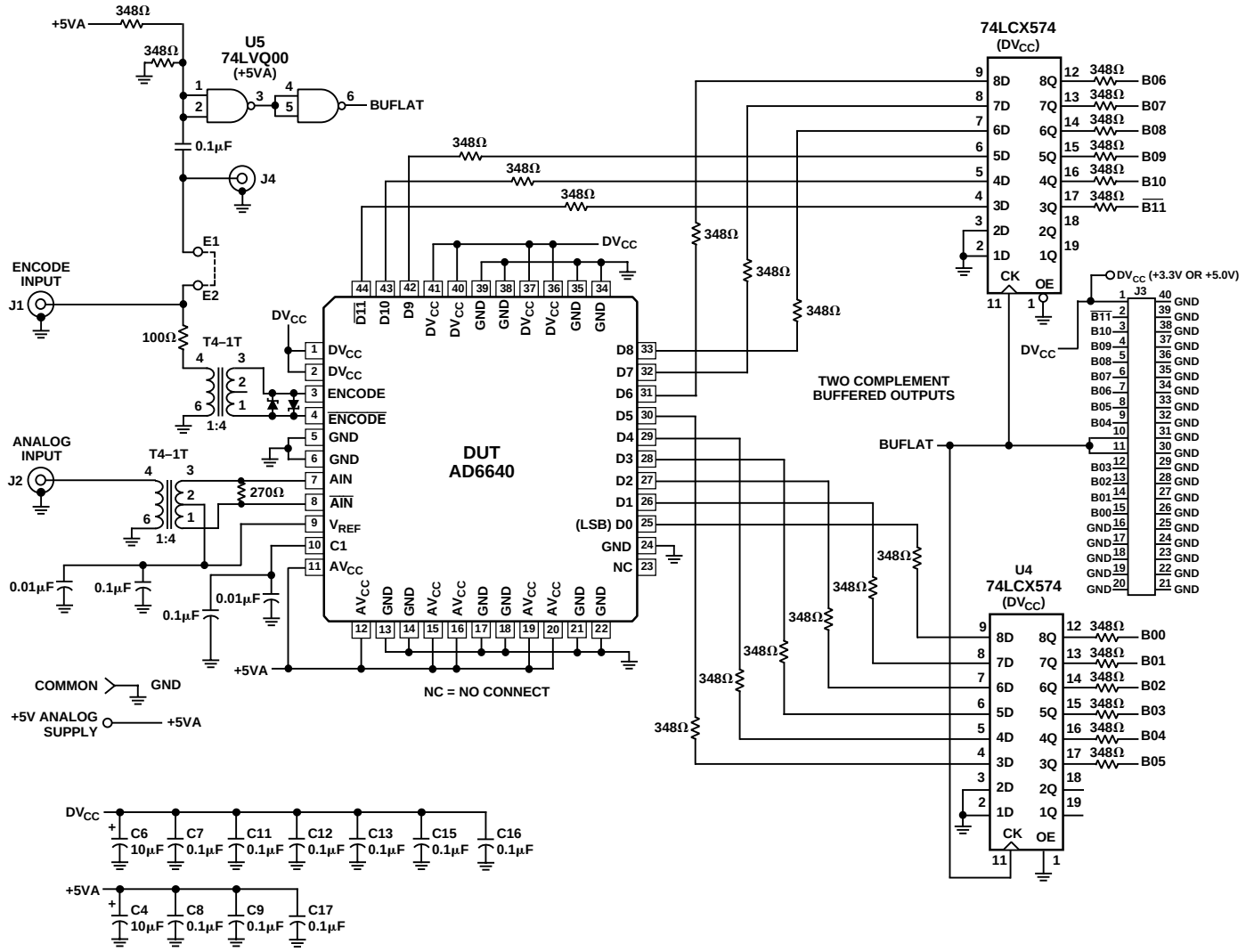


Figure 36. AD6640ST/PCB Schematic

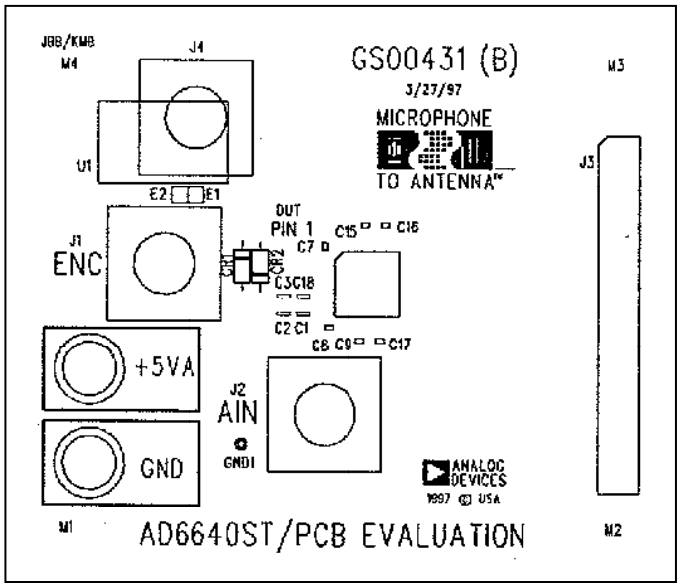


Figure 37. AD6640ST/PCB Top Side Silkscreen

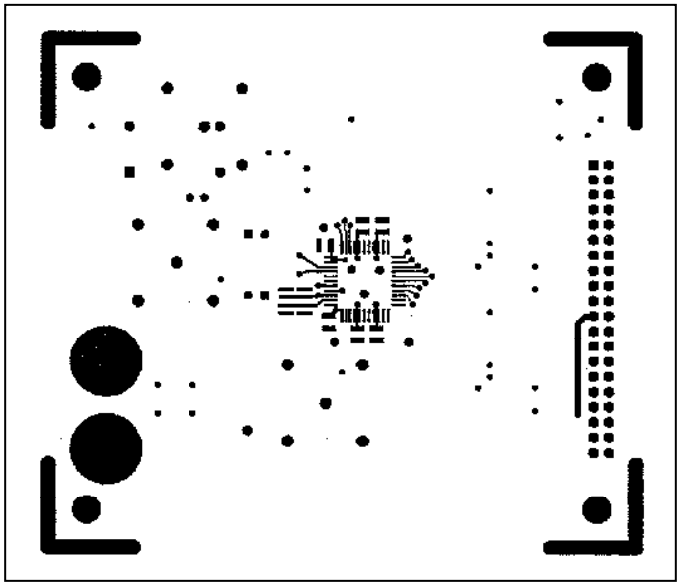


Figure 39. AD6640ST/PCB Top Side Copper

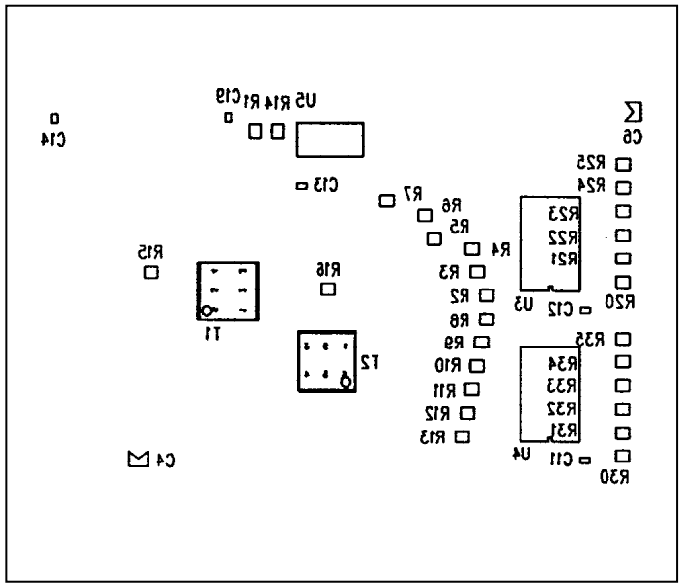


Figure 38. AD6640ST/PCB Bottom Side Silkscreen

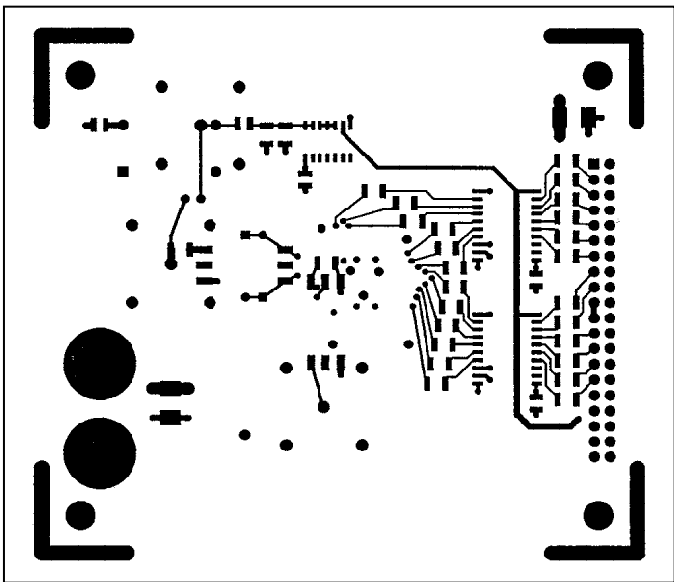


Figure 40. AD6640ST/PCB Bottom Side Copper (Positive)

NOTE: Evaluation boards are often updated, consult factory for latest version.

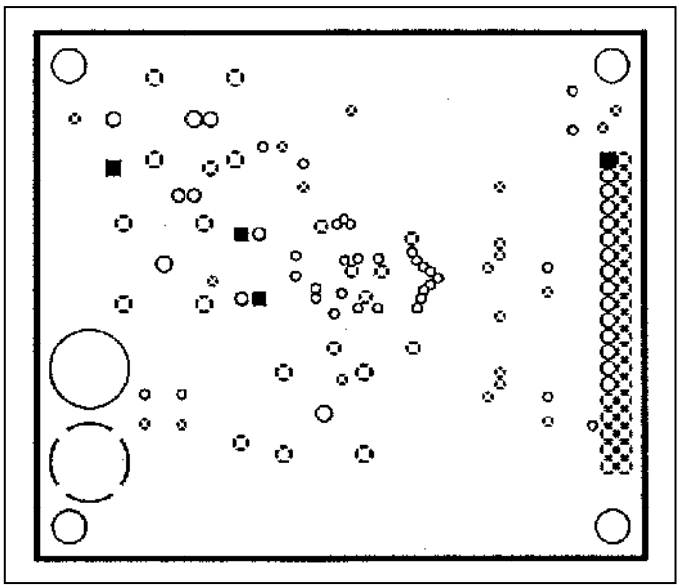


Figure 41. AD6640ST/PCB Ground Layer (Negative)

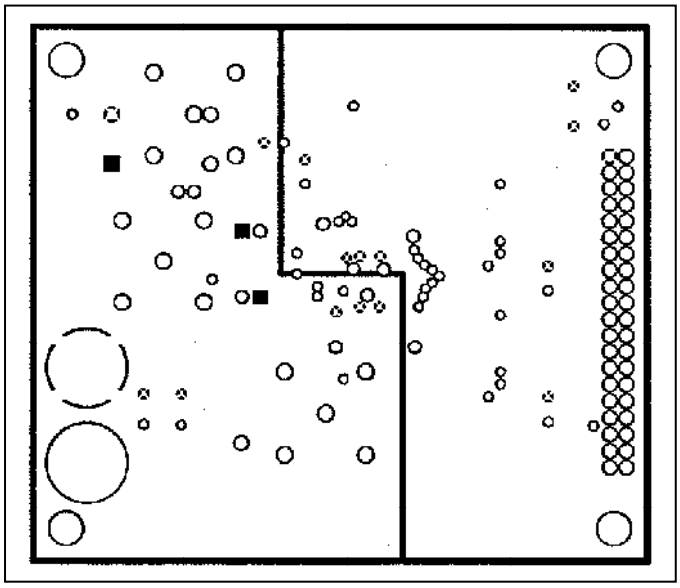


Figure 42. AD6640ST/PCB "Split" Power Layer (Negative)

DIGITAL WIDEBAND RECEIVERS

Introduction

Several key technologies are now being introduced that may forever alter the vision of radio. Figure 43 shows the typical dual conversion superheterodyne receiver. The signal picked up by the antenna is mixed down to an intermediate frequency (IF) using a mixer with a variable local oscillator (LO); the variable LO is used to "tune-in" the desired signal. This first IF is mixed down to a second IF using another mixer stage and a fixed LO. Demodulation takes place at the second or third IF using either analog or digital techniques.

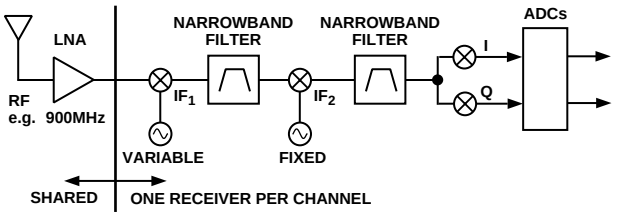


Figure 43. Narrowband Digital Receiver Architecture

If demodulation takes place in the analog domain then traditional discriminators, envelop detectors, phase locked loops or other synchronous detectors are generally employed to strip the modulation from the selected carrier.

However, as general purpose DSP chips such as the ADSP-2181 become more popular, they will be used in many baseband-sampled applications like the one shown in Figure 43. As shown in the figure, prior to ADC conversion, the signal must be mixed down, filtered, and the I and Q components separated. These functions are realizable through DSP techniques, however several key technology breakthroughs are required: high dynamic range ADCs such as the AD6640, new DSPs (highly programmable with onboard memory, fast), digital tuners and filters such as the AD6620, wide band mixers and amplifiers.

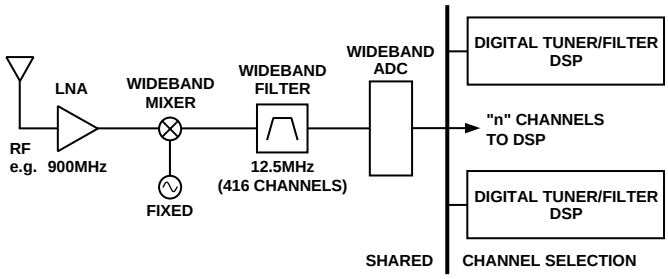


Figure 44. Wideband Digital Receiver Architecture

Figure 44 shows such a wideband system. This design shows that the front end variable local oscillator has been replaced with a fixed oscillator and the back end has been replaced with a wide dynamic range ADC, digital tuner and DSP. This technique offers many benefits.

First, many passive discrete components have been eliminated that formed the tuning and filtering functions. These passive components often require "tweaking" and special handling during assembly and final system alignment. Digital components require no such adjustments; tuner and filter characteristics are always exactly the same. Moreover, the tuning and filtering characteristics can be changed through software. Since software is used for demodulation, different routines may be used to demodulate different standards such as AM, FM, GMSK or any other desired standard. In addition, as new standards arise or new software revisions are generated, they may be field installed with standard software update channels. A radio that performs demodulation in software as opposed to hardware is often referred to as a soft radio because it may be changed or modified simply through code revision.

System Description

In the wideband digital radio (Figure 44), the first down conversion functions in much the same way as a block converter does. An entire band is shifted in frequency to the desired intermediate frequency. In the case of cellular base station receivers, 5 MHz to 30 MHz of bandwidth are down-converted simultaneously to an IF frequency suitable for digitizing with a wideband analog-to-digital converter. Once digitized the broadband digital data stream contains all of the in-band signals. The remainder of the radio is constructed digitally using special purpose and general purpose programmable DSP to perform filtering, demodulation and signal conditioning not unlike the analog counter parts.

In the narrowband receiver (Figure 43), the signal to be received must be tuned. This is accomplished by using a variable local oscillator at the first mix down stage. The first IF then uses a narrow band filter to reject out of band signals and condition the selected carrier for signal demodulation.

In the digital wideband receiver (Figure 44), the variable local oscillator has been replaced with a fixed oscillator, so tuning must be accomplished in another manner. Tuning is performed digitally using a digital down conversion and filter chip frequently called a channelizer. The term channelizer is used because the purpose of these chips is to select one channel out of many within the broadband spectrum present in the digital data stream of the ADC.

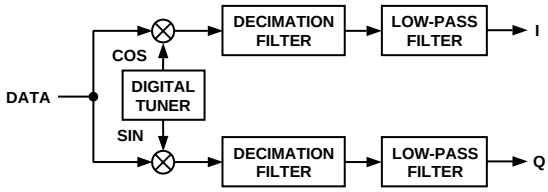


Figure 45. AD6620 Digital Channelizer

Figure 45 shows the block diagram of a typical channelizer, such as the AD6620. Channelizers consist of a complex NCO (Numerically Controlled Oscillator), dual multiplier (mixer), and matched digital filters. These are the same functions that would be required in an analog receiver, however implemented in digital form. The digital output from the channelizer is the desired carrier, frequently in I & Q format; all other signals have been filtered and removed based on the filtering characteristics desired. Since the channelizer output consists of one selected RF channel, one tuner chip is required for each frequency received, although only one wideband RF receiver is needed for the entire band. Data from the channelizer may then be processed using a digital signal processor such as the ADSP-2181 or the SHARC® processor, the ADSP-21062. This data may then be processed through software to demodulate the information from the carrier.

SHARC is a registered trademark of Analog Devices, Inc.

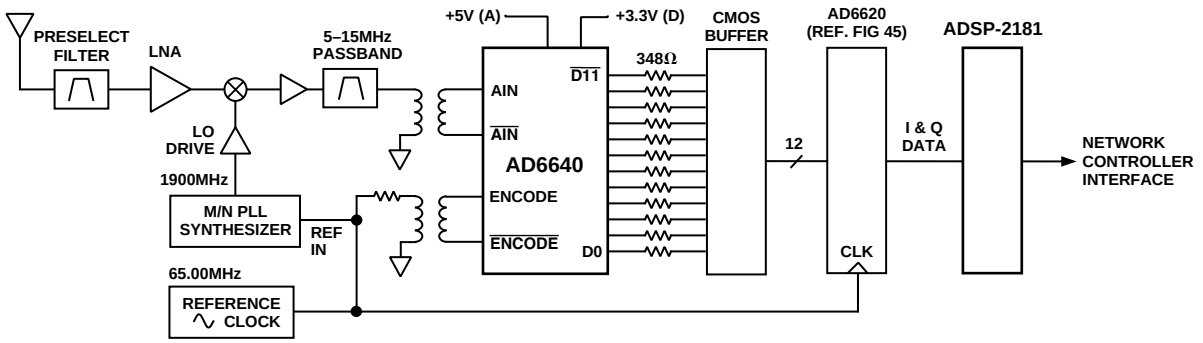


Figure 46. Simplified Wideband PCS Receiver

System Requirements

Figure 46 shows a typical wideband receiver subsystem based around the AD6640. This strip consists of a wideband IF filter, amplifier, ADC, latches, channelizer and interface to a digital signal processor. This design shows a typical clocking scheme used in many receiver designs. All timing within the system is referenced back to a single clock. While this is not necessary, it does facilitate PLL design, ease of manufacturing, system test, and calibration. Keeping in mind that the overall performance goal is to maintain the best possible dynamic range, many considerations must be made.

One of the biggest challenges is selecting the amplifier used to drive the AD6640. Since this is a communications application, it is common to directly sample an intermediate frequency (IF) signal. As such, IF gain blocks can be implemented instead of baseband op amps. For these gain block amplifiers, the critical specifications are third order intercept point and noise figure. A bandpass filter will remove harmonics generated within the amplifier, but intermods should be better than the performance of the A/D converter. In the case of the AD6640, amplifier intermods must be better than –80 dBFS when driving full-scale power. As mentioned earlier, there are several amplifiers to choose from and the specifications depend on the end application. Figure 47 shows a typical multitone test.

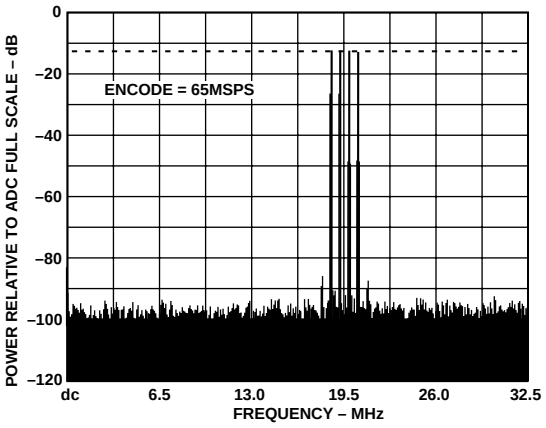


Figure 47. Multitone Performance

Two other key considerations for the digital wideband receiver are converter sample rate and IF frequency range. Since performance of the AD6640 converter is largely independent of both sample rate and analog input frequency (Figures 10, 11 and 16), the designer has greater flexibility in the selection of these parameters. Also, since the AD6640 is a bipolar device, power dissipation is not a function of sample rate. Thus there is no penalty paid in power by operating at faster sample rates. All of this is good because, by carefully selecting input frequency range and sample rate, some of the drive amplifier and ADC harmonics can actually be placed out-of-band.

For example, if the system has second and third harmonics that are unacceptably high, by carefully selecting the encode rate and signal bandwidth, these second and third harmonics can be placed out-of-band. For the case of an encode rate equal to 60 MSPS and a signal bandwidth of 7.5 MHz, placing the fundamental at 7.5 MHz places the second and third harmonics out of band as shown in the table below.

Table II.

Encode Rate	60 MSPS
Fundamental	7.5 MHz–15 MHz
Second Harmonic	15 MHz–30 MHz
Third Harmonic	22.5 MHz–30 MHz, 30 MHz–15 MHz

Another option can be found through bandpass sampling. If the analog input signal range is from dc to FS/2, then the amplifier and filter combination must perform to the specification required. However, if the signal is placed in the third Nyquist zone (FS to 3 FS/2), the amplifier is no longer required to meet the harmonic performance required by the system specifications since all harmonics would fall outside the passband filter. For example, the passband filter would range from FS to 3 FS/2. The second harmonic would span from 2 FS to 3 FS, well outside the passband filter's range. The burden then has been passed off to the filter design provided that the ADC meets the basic specifications at the frequency of interest. In many applications, this is a worthwhile tradeoff since many complex filters can easily be realized using SAW and LCR techniques alike at these relatively high IF frequencies. Although harmonic performance of the drive amplifier is relaxed by this technique, intermodulation performance cannot be sacrificed since intermods must be assumed to fall in-band for both amplifiers and converters.

Noise Floor and SNR

Oversampling is sampling at a rate that is greater than twice the bandwidth of the signal desired. Oversampling does not have anything to do with the actual frequency of the sampled signal, it is the bandwidth of the signal that is key. Bandpass or "IF" sampling refers to sampling a frequency that is higher than Nyquist and often provides additional benefits such as down conversion using the ADC and replacing a mixer with a track-and-hold. Oversampling leads to processing gains because the

faster the signal is digitized, the wider the distribution of noise. Since the integrated noise must remain constant, the actual noise floor is lowered by 3 dB each time the sample rate is doubled. The effective noise density for an ADC may be calculated by the equation:

$$V_{NOISE\ rms} / \sqrt{Hz} = \frac{10^{-SNR/20}}{\sqrt{4\ FS}}$$

For a typical SNR of 68 dB and a sample rate of 65 MSPS, this is equivalent to 25 nV/$\sqrt{\text{Hz}}$. This equation shows the relationship between SNR of the converter and the sample rate FS. This equation may be used for computational purposes to determine overall receiver noise.

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, the following equation accurately predicts the SNR based on three terms. These are jitter, average DNL error and thermal noise. Each of these terms contributes to the noise within the converter.

Equation 1:

$$SNR = -20 \log\left[\left(2\pi F_{ANALOG}\ \ t_{J\,rms}\right)^2 + \left(\frac{1+\varepsilon}{2^{12}}\right)^2 + \left(\frac{V_{NOISE\ rms}}{2^{12}}\right)^2\right]^{1/2}$$

F_{ANALOG} = analog input frequency

$t_{J\ rms}$ = rms jitter of the encode (rms sum of encode source and internal encode circuitry)

ε = average DNL of the ADC (typically 0.51 LSB)

$V_{NOISE\ rms}$ = V rms thermal noise referred to the analog input of the ADC (typically 0.707 LSB)

Processing Gain

Processing gain is the improvement in signal-to-noise ratio (SNR) gained through oversampling and digital filtering. Most of this processing gain is accomplished using the channelizer chips. These special purpose DSP chips not only provide channel selection and filtering but also provide a data rate reduction. The required rate reduction is accomplished through a process called decimation. The term decimation rate is used to indicate the ratio of input data rate to output data rate. For example, if the input data rate is 65 MSPS and the output data rate is 1.25 MSPS, then the decimation rate is 52.

Large processing gains may be achieved in the decimation and filtering process. The purpose of the channelizer, beyond tuning, is to provide the narrowband filtering and selectivity that traditionally has been provided by the ceramic or crystal filters of a narrowband receiver. This narrowband filtering is the source of the processing gain associated with a wideband receiver and is simply the ratio of the passband to whole band expressed in dB. For example, if a 30 kHz AMPS signal is being digitized with an AD6640 sampling at 65 MSPS, the ratio would be 0.015 *MHz*/32.5 *MHz*. Expressed in log form, the processing gain is –10 × log (0.015 *MHz*/32.5 *MHz*) or 33.4 dB.

Additional filtering and noise reduction techniques can be achieved through DSP techniques; many applications do use additional process gains through proprietary noise reduction algorithms.

Overcoming Static Nonlinearities with Dither

Typically, high resolution data converters use multistage techniques to achieve high bit resolution without large comparator arrays that would be required if traditional "flash" ADC techniques were employed. The multistage converter typically provides better wafer yields meaning lower cost and much lower power. However, since it is a multistage device, certain portions of the circuit are used repetitively as the analog input sweeps from one end of the converter range to the other. Although the worst DNL error may be less than an LSB, the repetitive nature of the transfer function can play havoc with low level dynamic signals. Spurious signals for a full-scale input may be –80 dBc. However at 36 dB below full scale, these repetitive DNL errors may cause spurious-free dynamic range (SFDR) to fall below 80 dBFS as shown in Figure 20.

A common technique for randomizing and reducing the effects of repetitive static linearity is through the use of dither. The purpose of dither is to force the repetitive nature of static linearity to appear as if it were random. Then, the average linearity over the range of dither will dominate SFDR performance. In the AD6640, the repetitive cycle is every 15.625 mV p-p.

To ensure adequate randomization, 5.3 mV rms is required; this equates to a total dither power of –32.5 dBm. This will randomize the DNL errors over the complete range of the residue converter. Although lower levels of dither such as that from previous analog stages will reduce some of the linearity errors, the full effect will only be gained with this larger dither. Increasing dither even more may be used to reduce some of the global INL errors. However, signals much larger than the mVs proposed here begin to reduce the usable dynamic range of the converter.

Even with the 5.3 mV rms of noise suggested, SNR would be limited to 36 dB if injected as broadband noise. To avoid this problem, noise may be injected as an out-of-band signal. Typically, this may be around dc but may just as well be at FS/2 or at some other frequency not used by the receiver. The bandwidth of the noise is several hundred kilohertz. By band-limiting and controlling its location in frequency, large levels of dither may be introduced into the receiver without seriously disrupting receiver performance. The result can be a marked improvement in the SFDR of the data converter.

Figure 23 shows the same converter shown earlier but with this injection of dither (reference Figure 20).

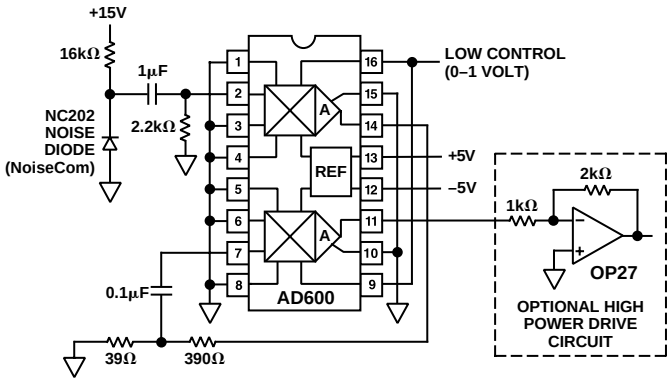


Figure 48. Noise Source (Dither Generator)

The simplest method for generating dither is through the use of a noise diode (Figure 48). In this circuit, the noise diode NC202 generates the reference noise that is gained up and driven by the AD600 and OP27 amplifier chain. The level of noise may be controlled by either presetting the control voltage when the system is set up, or by using a digital-to-analog converter (DAC) to adjust the noise level based on input signal conditions. Once generated, the signal must be introduced to the receiver strip. The easiest method is to inject the signal into the drive chain after the last down conversion as shown in Figure 49.

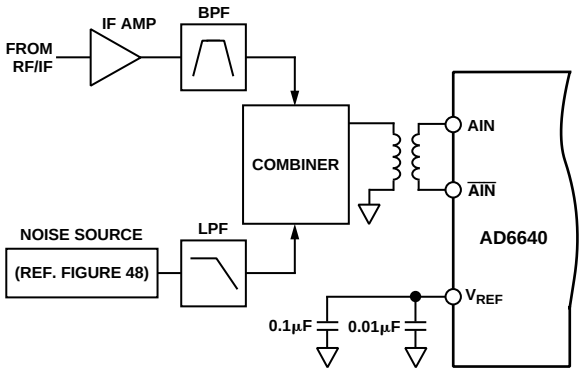


Figure 49. Using the AD6640 with Dither

Receiver Example

To determine how the ADC performance relates to overall receiver sensitivity, the simple receiver in Figure 50 will be examined. This example assumes that the overall down conversion process can be grouped into one set of specifications, instead of individually examining all components within the system and summing them together. Although a more detailed analysis should be employed in a real design, this model will provide a good approximation.

In examining a wideband digital receiver, several considerations must be applied. Although other specifications are important, receiver sensitivity determines the absolute limits of a radio excluding the effects of other outside influences. Assuming that receiver sensitivity is limited by noise and not adjacent signal strength, several sources of noise can be identified and their overall contribution to receiver sensitivity calculated.

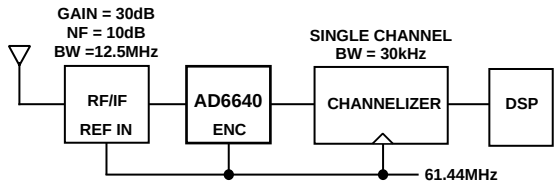


Figure 50. Receiver Analysis

The first noise calculation to make is based on the signal bandwidth at the antenna. In a typical broadband cellular receiver, the IF bandwidth is 12.5 MHz. Given that the power of noise in a given bandwidth is defined by $P_n = kTB$, where B is bandwidth, $k = 1.38 \times 10^{-23}$ is Boltzman's constant and $T = 300k$ is absolute temperature, this gives an input noise power of 5.18×10^{-14} watts or –102.86 dBm. If our receiver front end has a gain of 30 dB and a noise figure of 10 dB, then the total noise presented to the ADC input becomes –62.86 dBm (–102.86 + 30 + 10) or 0.16 mV rms. Comparing receiver noise to dither required for good SFDR, we see that in this example, our receiver supplies about 3% of the dither required for good SFDR.

Based on a typical ADC SNR specification of 68 dB, the equivalent internal converter noise is 0.140 mV rms. Therefore total broadband noise is 0.21 mV rms. Before processing gain, this is an equivalent SNR (with respect to full scale) of 64.5 dB. Assuming a 30 kHz AMPS signal and a sample rate of 61.44 MSPS, the SNR through processing gain is increased by approximately 33 dB to 97.5 dB. However, if eight strong and equal signals are present in the ADC bandwidth, then each must be placed 18 dB below full scale to prevent ADC overdrive. Therefore we give away 18 dB of range and reduce the carrier-to-noise ratio (C/N) to 79.5 dB.

Assuming that the C/N ratio must be 10 dB or better for accurate demodulation, one of the eight signals may be reduced by 66.5 dB before demodulation becomes unreliable. At this point, the input signal power would be –90.5 dBm. Referenced to the antenna, this is –120.5 dBm.

To improve sensitivity, several things can be done. First, the noise figure of the receiver can be reduced. Since front end noise dominates the 0.16 mV rms, each dB reduction in noise figure translates to an additional dB of sensitivity. Second, providing broadband AGC can improve sensitivity by the range of the AGC. However, the AGC would only provide useful improvements if all in-band signals are kept to an absolute minimal power level so that AGC can be kept near the maximum gain.

This noise limited example does not adequately demonstrate the true limitations in a wideband receiver. Other limitations such as SFDR are more restrictive than SNR and noise. Assume that the analog-to-digital converter has an SFDR specification of –80 dBFS or –76 dBm (Full scale = +4 dBm). Also assume that a tolerable carrier-to-interferer (C/I) (different from C/N) ratio is 18 dB. This means that the minimum signal level is –62 dBFS (–80 plus 18) or –58 dBm. At the antenna, this is –88 dBm. Therefore, as can be seen, SFDR (single or multitone) would limit receiver performance in this example. However, as shown previously, SFDR can be greatly improved through the use of dither (Figures 19, 22). In many cases, the addition of the out-of-band dither can improve receiver sensitivity nearly to that limited by thermal noise.

IF Sampling, Using the AD6640 as a Mix-Down Stage

Since performance of the AD6640 extends beyond the baseband region into the third Nyquist zone, the converter has many uses as a mix-down converter in both narrowband and wideband applications. This application is called bandpass sampling. Doing this has several positive implications in terms of the selection of the IF drive amplifier. Not only is filtering a bit easier, the selection of drive amplifiers is extended to classical IF gain blocks. In the third Nyquist zone and above, the second and third harmonics are easily filtered with a bandpass filter. Now only in-band spurs that result from third order products are important.

In narrowband applications, harmonics of the ADC can be placed out-of-band. One example is the digitization of a 201 MHz IF signal using a 17.333 MHz clock. As shown in Figure 51, the spurious performance has diminished due to internal slew rate limitations of the ADC. However, the SNR of the converter is still quite good. Subsequent digital filtering with a channelizer chip such as the AD6620 will yield even better SNR.

For multicarrier applications, third order intercept of the drive amplifier is important. If the input network is matched to the internal 900 ohm input impedance, the required full-scale drive level is –3 dBm. If spurious products delivered to the ADC are required to be below –90 dBFS, the typical performance of the ADC with dither applied, then the required third order intercept point for the drive amplifier can be calculated.

For multicarrier applications, the AD6640 is useful up to about 80 MHz analog in. For single channel applications, the AD6640 is useful to 200 MHz as shown from the bandwidth charts. In either case, many common IF frequencies exist in this range of frequencies. If the ADC is used to sample these signals, they will be aliased down to baseband during the sampling process in much the same manner that a mixer will down-convert a signal. For signals in various Nyquist zones, the following equations may be used to determine the final frequency after aliasing.

$$f_{1NYQUISTS} = f_{SAMPLE} - f_{SIGNAL}$$
$$f_{2NYQUISTS} = abs\,(f_{SAMPLE} - f_{SIGNAL})$$
$$f_{3NYQUISTS} = 2 \times f_{SAMPLE} - f_{SIGNAL}$$
$$f_{4NYQUISTS} = abs\,(2 \times f_{SAMPLE} - f_{SIGNAL})$$

Using the converter to alias down these narrowband or wideband signals has many potential benefits. First and foremost is the elimination of a complete mixer stage along with amplifiers, filters and other devices, reducing cost and power dissipation. In some cases, the elimination of two IF stages is possible.

Figures 21 and 24 in Typical Performance Characteristics illustrate a multicarrier, IF Sampling System. By using dither, all spurious components are forced below 90 dBFS (Figure 24). The dashed line illustrates how a 5 MHz bandpass filter could be centered at 67.5 MHz. As discussed earlier, this approach greatly reduces the size and complexity of the receiver's RF/IF section.

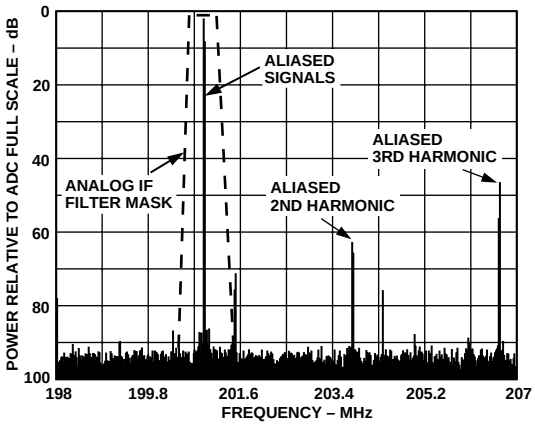


Figure 51. IF-Sampling a 201 MHz Input

RECEIVE CHAIN FOR A PHASED ARRAY CELLULAR BASE STATION

The AD6640 is an excellent digitizer for beam forming in phased array antenna systems. The price performance of the AD6640 followed by AD6620 channelizers allows for a very competitive solution. Phase array base stations allow better coverage by focusing the receivers' sensitivity in the direction needed. Phased array systems allow for the electronic beam to form on the receive antennas.

A typical phased array system may have eight antennas as shown in Figure 52. Since a typical base station will handle 32 calls, each antenna would have to be connected to 32 receivers. If done with analog or traditional radios, the system grows quite rapidly. With a multicarrier receiver, however, the design is quite compact. Each antenna will have a wideband down-converter with one AD6640 per receiver. The output of each AD6640 would drive 32 AD6620 channelizers, which are phase locked in groups of eight—one per antenna. This allows each group of eight AD6620's to tune and lock onto a different user. When the incoming signal direction is determined, the relative phase of each AD6620 in the group can be adjusted such the output signals sum together in a constructive manner, giving high gain and directivity in the direction of the caller. This application would not be possible with traditional receiver designs.

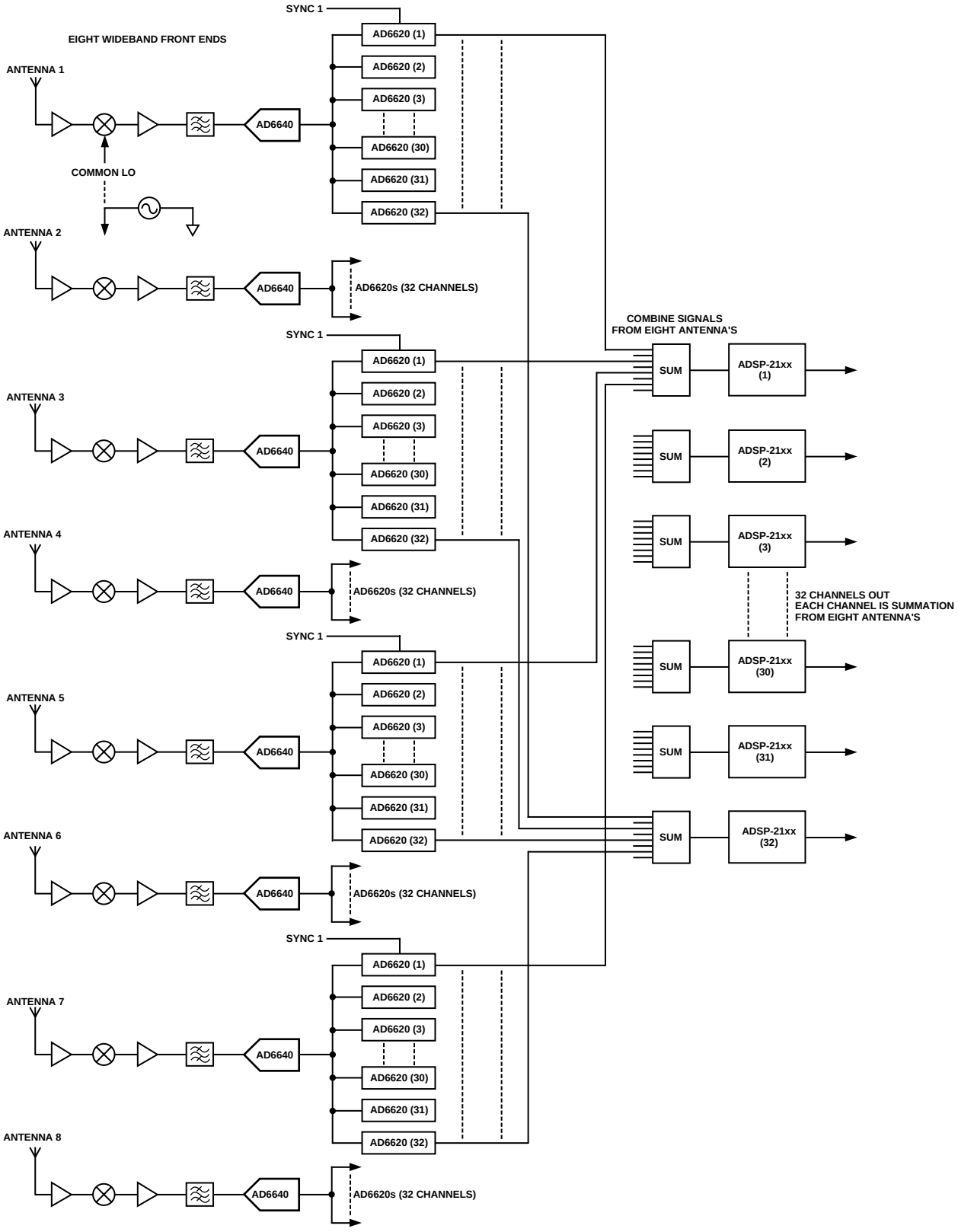
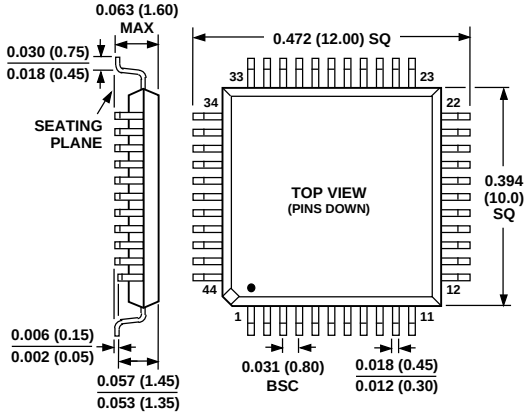


Figure 52. Receive Chain for a Phased Array Cellular Base Station with Eight Antennas and 32 Channels

AD6640AST OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

44-Terminal Plastic Thin Quad Flatpack (ST-44)



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Appendix C: Analog Devices AD603 – Variable Gain Amplifier

Included for your reference on the following pages is the data sheet for the AD603 Variable Gain Amplifier, provided by the courtesy of Analog Devices Inc., Norwood, MA.

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Low Noise, 90 MHz Variable-Gain Amplifier

AD603*

FEATURES
"Linear in dB" Gain Control
Pin Programmable Gain Ranges
–11 dB to +31 dB with 90 MHz Bandwidth
9 dB to 51 dB with 9 MHz Bandwidth
Any Intermediate Range, e.g., –1 dB to +41 dB with 30 MHz Bandwidth
Bandwidth Independent of Variable Gain
1.3 nV/√Hz Input Noise Spectral Density
±0.5 dB Typical Gain Accuracy
MIL-STD-883 Compliant and DESC Versions Available

APPLICATIONS
RF/IF AGC Amplifier
Video Gain Control
A/D Range Extension
Signal Measurement

PRODUCT DESCRIPTION

The AD603 is a low noise, voltage-controlled amplifier for use in RF and IF AGC systems. It provides accurate, pin selectable gains of –11 dB to +31 dB with a bandwidth of 90 MHz or 9 dB to 51 dB with a bandwidth of 9 MHz. Any intermediate gain range may be arranged using one external resistor. The input referred noise spectral density is only 1.3 nV/√Hz and power consumption is 125 mW at the recommended ±5 V supplies.

The decibel gain is "linear in dB," accurately calibrated, and stable over temperature and supply. The gain is controlled at a high impedance (50 MΩ), low bias (200 nA) differential input; the scaling is 25 mV/dB, requiring a gain-control voltage of only 1 V to span the central 40 dB of the gain range. An over- and underrange of 1 dB is provided whatever the selected range. The gain-control response time is less than 1 μs for a 40 dB change.

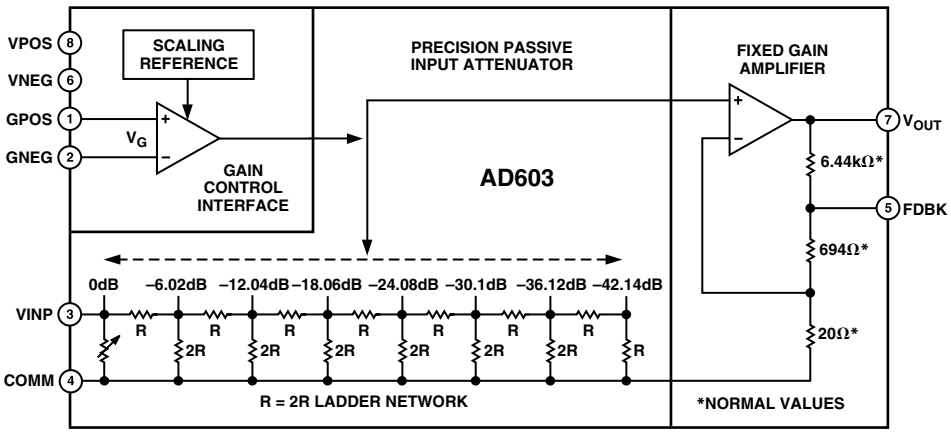
The differential gain-control interface allows the use of either differential or single-ended positive or negative control voltages. Several of these amplifiers may be cascaded and their gain-control gains offset to optimize the system S/N ratio.

The AD603 can drive a load impedance as low as 100 Ω with low distortion. For a 500 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically –60 dBc. The peak specified output is ±2.5 V minimum into a 500 Ω load, or ±1 V into a 100 Ω load.

The AD603 uses a proprietary circuit topology—the X-AMP™. The X-AMP comprises a variable attenuator of 0 dB to –42.14 dB followed by a fixed-gain amplifier. Because of the attenuator, the amplifier never has to cope with large inputs and can use negative feedback to define its (fixed) gain and dynamic performance. The attenuator has an input resistance of 100 Ω, laser trimmed to ±3%, and comprises a seven-stage R-2R ladder network, resulting in an attenuation between tap points of 6.021 dB. A proprietary interpolation technique provides a continuous gain-control function which is linear in dB.

The AD603A is specified for operation from –40°C to +85°C and is available in both 8-lead SOIC (R) and 8-lead ceramic DIP (Q). The AD603S is specified for operation from –55°C to +125°C and is available in an 8-lead ceramic DIP (Q). The AD603 is also available under DESC SMD 5962-94572.

FUNCTIONAL BLOCK DIAGRAM



*Patented.
X-AMP is a trademark of Analog Devices, Inc.

REV. D

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Fax: 781/326-8703
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AD603–SPECIFICATIONS (@ T_A = 25°C, V_S = ±5 V, –500 mV ≤ V_G ≤ +500 mV, GNEG = 0 V, –10 dB to +30 dB Gain Range, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted.)

Model / Parameter	Conditions	AD603 Min	AD603 Typ	AD603 Max	Unit
INPUT CHARACTERISTICS					
Input Resistance	Pins 3 to 4	97	100	**103**	Ω
Input Capacitance			2		pF
Input Noise Spectral Density[1]	Input Short Circuited		1.3		nV/√Hz
Noise Figure	f = 10 MHz, Gain = max, R_S = 10 Ω		8.8		dB
1 dB Compression Point	f = 10 MHz, Gain = max, R_S = 10 Ω		–11		dBm
Peak Input Voltage			±1.4	±2	V
OUTPUT CHARACTERISTICS					
–3 dB Bandwidth	V_{OUT} = 100 mV rms		90		MHz
Slew Rate	R_L ≥ 500 Ω		275		V/µs
Peak Output[2]	R_L ≥ 500 Ω	±2.5	±3.0		V
Output Impedance	f ≤ 10 MHz		2		Ω
Output Short-Circuit Current			50		mA
Group Delay Change vs. Gain	f = 3 MHz; Full Gain Range		±2		ns
Group Delay Change vs. Frequency	V_G = 0 V; f = 1 MHz to 10 MHz		±2		ns
Differential Gain			0.2		%
Differential Phase			0.2		Degree
Total Harmonic Distortion	f = 10 MHz, V_{OUT} = 1 V rms		–60		dBc
3rd Order Intercept	f = 40 MHz, Gain = max, R_S = 50 Ω		15		dBm
ACCURACY					
Gain Accuracy	–500 mV ≤ V_G ≤ +500 mV		±0.5	**±1**	dB
T_{MIN} to T_{MAX}				±1.5	dB
Output Offset Voltage[3]	V_G = 0 V			**20**	mV
T_{MIN} to T_{MAX}				30	mV
Output Offset Variation vs. V_G	–500 mV ≤ V_G ≤ +500 mV			**20**	mV
T_{MIN} to T_{MAX}				30	mV
GAIN CONTROL INTERFACE					
Gain Scaling Factor		**39.4**	40	**40.6**	dB/V
T_{MIN} to T_{MAX}		38		42	dB/V
GNEG, GPOS Voltage Range[4]		–1.2		**+2.0**	V
Input Bias Current			200		nA
Input Offset Current			10		nA
Differential Input Resistance	Pins 1 to 2		50		MΩ
Response Rate	Full 40 dB Gain Change		40		dB/µs
POWER SUPPLY					
Specified Operating Range		±4.75		±6.3	V
Quiescent Current			12.5	**17**	mA
T_{MIN} to T_{MAX}				20	mA

NOTES

[1]Typical open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited. This figure includes the effects of both voltage and current noise sources.

[2]Using resistive loads of 500 Ω or greater, or with the addition of a 1 kΩ pull-down resistor when driving lower loads.

[3]The dc gain of the main amplifier in the AD603 is ×35.7; thus, an input offset of 100 µV becomes a 3.57 mV output offset.

[4]GNEG and GPOS, gain control, voltage range is guaranteed to be within the range of $-V_S$ + 4.2 V to $+V_S$ – 3.4 V over the full temperature range of –40°C to +85°C.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

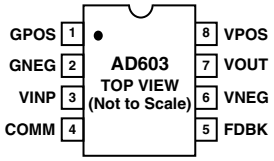
Supply Voltage $\pm V_S$ . . . . . ±7.5 V
Internal Voltage VINP (Pin 3) . . . . . ±2 V Continuous
. . . . . $\pm V_S$ for 10 ms
GPOS, GNEG (Pins 1, 2) . . . . . $\pm V_S$
Internal Power Dissipation[2] . . . . . 400 mW
Operating Temperature Range
AD603A . . . . . −40°C to +85°C
AD603S . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Lead SOIC Package: θ_{JA} = 155°C/W, θ_{JC} = 33°C/W
8-Lead Ceramic Package: θ_{JA} = 140°C/W, θ_{JC} = 15°C/W

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	GPOS	Gain-Control Input "HI" (Positive Voltage Increases Gain)
2	GNEG	Gain-Control Input "LO" (Negative Voltage Increases Gain)
3	VINP	Amplifier Input
4	COMM	Amplifier Ground
5	FDBK	Connection to Feedback Network
6	VNEG	Negative Supply Input
7	VOUT	Amplifier Output
8	VPOS	Positive Supply Input

CONNECTION DIAGRAMS
8-Lead Plastic SOIC (R) Package
8-Lead Ceramic DIP (Q) Package



ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
AD603AR	–40°C to +85°C	8-Lead SOIC	SO-8
AD603AQ	–40°C to +85°C	8-Lead Ceramic DIP	Q-8
AD603SQ/883B*	–55°C to +125°C	8-Lead Ceramic DIP	Q-8
AD603-EB		Evaluation Board	
AD603ACHIPS	–40°C to +85°C	Die	
AD603AR-REEL	–40°C to +85°C	13" Reel	SO-8
AD603AR-REEL7	–40°C to +85°C	7" Reel	SO-8

*Refer to AD603 Military data sheet. Also available as 5962-9457203MPA.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD603 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



THEORY OF OPERATION

The AD603 comprises a fixed-gain amplifier, preceded by a broadband passive attenuator of 0 dB to 42.14 dB, having a gain-control scaling factor of 40 dB per volt. The fixed gain is laser-trimmed in two ranges, to either 31.07 dB (×35.8) or 50 dB (×358), or may be set to any range in between using one external resistor between Pins 5 and 7. Somewhat higher gain can be obtained by connecting the resistor from Pin 5 to common, but the increase in output offset voltage limits the maximum gain to about 60 dB. For any given range, the bandwidth is independent of the voltage-controlled gain. This system provides an under- and overrange of 1.07 dB in all cases; for example, the overall gain is –11.07 dB to 31.07 dB in the maximum-bandwidth mode (Pin 5 and Pin 7 strapped).

This *X-AMP* structure has many advantages over former methods of gain-control based on nonlinear elements. Most importantly, the fixed-gain amplifier can use negative feedback to increase its accuracy. Since large inputs are first attenuated, the amplifier input is always small. For example, to deliver a ±1 V output in the –1 dB/+41 dB mode (that is, using a fixed amplifier gain of 41.07 dB) its input is only 8.84 mV; thus the distortion can be very low. Equally important, the small-signal gain and phase response, and thus the pulse response, are essentially independent of gain.

Figure 1 is a simplified schematic. The input attenuator is a seven-section R-2R ladder network, using untrimmed resistors of nominally R = 62.5 Ω, which results in a characteristic resistance of 125 Ω ± 20%. A shunt resistor is included at the input and laser trimmed to establish a more exact input resistance of 100 Ω ± 3%, which ensures accurate operation (gain and HP corner frequency) when used in conjunction with external resistors or capacitors.

The nominal maximum signal at input VINP is 1 V rms (±1.4 V peak) when using the recommended ±5 V supplies, although operation to ±2 V peak is permissible with some increase in HF distortion and feedthrough. *Pin 4 (SIGNAL COMMON) must be connected directly to the input ground; significant impedance in this connection will reduce the gain accuracy.*

The signal applied at the input of the ladder network is attenuated by 6.02 dB by each section; thus, the attenuation to each of the taps is progressively 0 dB, 6.02 dB, 12.04 dB, 18.06 dB, 24.08 dB, 30.1 dB, 36.12 dB and 42.14 dB. A unique circuit technique is employed to interpolate between these tap-points, indicated by the "slider" in Figure 1, thus providing continuous attenuation from 0 dB to 42.14 dB. It will help, in understanding the AD603, to think in terms of a mechanical means for moving this slider from left to right; in fact, its "position" is controlled by the voltage between Pins 1 and 2. The details of the gain-control interface are discussed later.

The gain is at all times very exactly determined, and a linear-in-dB relationship is automatically guaranteed by the exponential nature of the attenuation in the ladder network (the X-AMP principle). In practice, the gain deviates slightly from the ideal law, by about ±0.2 dB peak (see, for example, Figure 16).

Noise Performance

An important advantage of the X-AMP is its superior noise performance. The nominal resistance seen at inner tap points is 41.7 Ω (one third of 125 Ω), which exhibits a Johnson noise-spectral density (NSD) of 0.83 nV/$\sqrt{\text{Hz}}$ (that is, $\sqrt{4kTR}$) at 27°C, which is a large fraction of the total input noise. The first stage of the amplifier contributes a further 1 nV/$\sqrt{\text{Hz}}$, for a total input noise of 1.3 nV/$\sqrt{\text{Hz}}$. It will be apparent that it is essential to use a low resistance in the ladder network to achieve the very low specified noise level. The signal's source impedance forms a voltage divider with the AD603's 100 Ω input resistance. In some applications, the resulting attenuation may be unacceptable, requiring the use of an external buffer or preamplifier to match a high impedance source to the low impedance AD603.

The noise at maximum gain (that is, at the 0 dB tap) depends on whether the input is short-circuited or open-circuited: when shorted, the minimum NSD of slightly over 1 nV/$\sqrt{\text{Hz}}$ is achieved; when open, the resistance of 100 Ω looking into the first tap generates 1.29 nV/$\sqrt{\text{Hz}}$, so the noise increases to a total of 1.63 nV/$\sqrt{\text{Hz}}$. (This last calculation would be important if the AD603 were preceded by, for example, a 900 Ω resistor to allow operation from inputs up to 10 V rms.) As the selected tap moves away from the input, the dependence of the noise on source impedance quickly diminishes.

Apart from the small variations just discussed, the signal-to-noise (S/N) ratio at the output is essentially independent of the attenuator setting. For example, on the –11 dB/+31 dB range the fixed gain of ×35.8 raises the output NSD to 46.5 nV/$\sqrt{\text{Hz}}$. Thus, for the maximum undistorted output of 1 V rms and a 1 MHz bandwidth, the output S/N ratio would be 86.6 dB, that is, 20 log (1 V/46.5 μV).

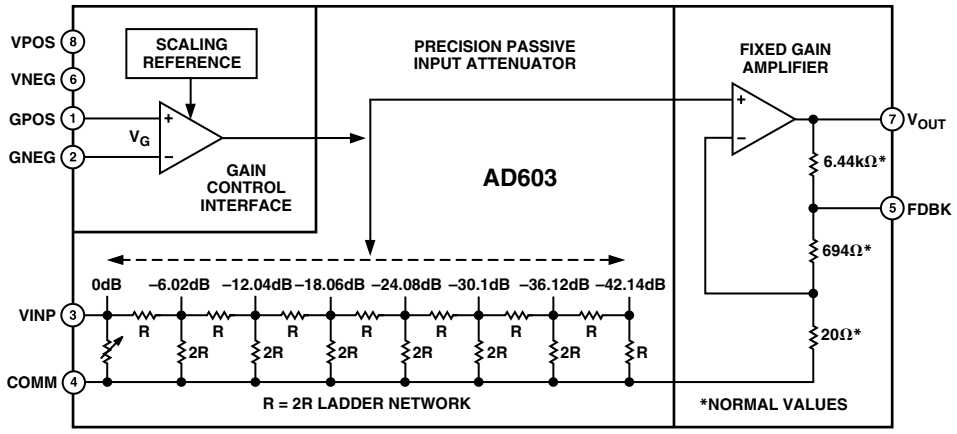


Figure 1. Simplified Block Diagram of the AD603

*Patented. X-AMP is a trademark of Analog Devices, Inc.

The Gain-Control Interface

The attenuation is controlled through a differential, high-impedance (50 MΩ) input, with a scaling factor which is laser-trimmed to 40 dB per volt, that is, 25 mV/dB. An internal bandgap reference ensures stability of the scaling with respect to supply and temperature variations.

When the differential input voltage V_G = 0 V, the attenuator "slider" is centered, providing an attenuation of 21.07 dB. For the maximum bandwidth range, this results in an overall gain of 10 dB (= –21.07 dB + 31.07 dB). When the control input is –500 mV, the gain is lowered by 20 dB (= 0.500 V × 40 dB/V), to –10 dB; when set to +500 mV, the gain is increased by 20 dB, to 30 dB. When this interface is overdriven in either direction, the gain approaches either –11.07 dB (= –42.14 dB + 31.07 dB) or 31.07 dB (= 0 + 31.07 dB), respectively. The only constraint on the gain-control voltage is that it be kept within the common-mode range (–1.2 V to +2.0 V assuming +5 V supplies) of the gain control interface.

The basic gain of the AD603 can thus be calculated using the following simple expression:

$$Gain\ (dB) = 40\ V_G + 10 \quad (1)$$

where V_G is in volts. When Pins 5 and 7 are strapped (see next section) the gain becomes

$$Gain\ (dB) = 40\ V_G + 20\ for\ 0\ to\ +40\ dB$$

and

$$Gain\ (dB) = 40\ V_G + 30\ for\ +10\ to\ +50\ dB \quad (2)$$

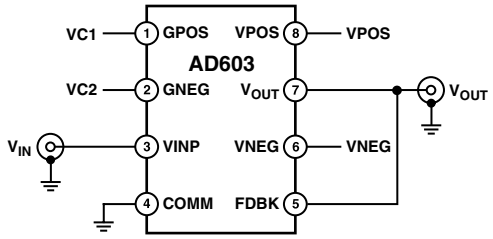
The high impedance gain-control input ensures minimal loading when driving many amplifiers in multiple channel or cascaded applications. The differential capability provides flexibility in choosing the appropriate signal levels and polarities for various control schemes.

For example, if the gain is to be controlled by a DAC providing a positive only ground-referenced output, the "Gain Control LO" (GNEG) pin should be biased to a fixed offset of 500 mV, to set the gain to –10 dB when "Gain Control HI" (GPOS) is at zero, and to 30 dB when at 1.00 V.

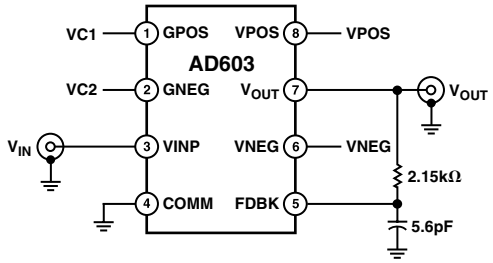
It is a simple matter to include a voltage divider to achieve other scaling factors. When using an 8-bit DAC having an FS output of 2.55 V (10 mV/bit), a divider ratio of 2 (generating 5 mV/bit) would result in a gain-setting resolution of 0.2 dB/bit. The use of such offsets is valuable when two AD603s are cascaded, when various options exist for optimizing the S/N profile, as will be shown later.

Programming the Fixed-Gain Amplifier Using Pin Strapping

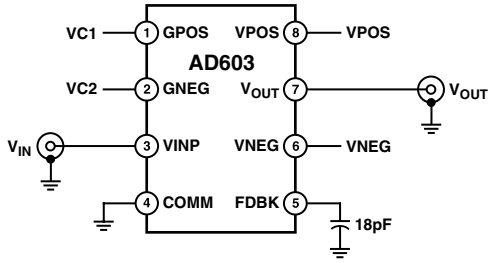
Access to the feedback network is provided at Pin 5 (FDBK). The user may program the gain of the AD603's output amplifier using this pin, as shown in Figure 2. There are three modes: in the default mode, FDBK is unconnected, providing the range +9 dB/+51 dB; when V_{OUT} and FDBK are shorted, the gain is lowered to –11 dB/+31 dB; when an external resistor is placed between V_{OUT} and FDBK any intermediate gain can be achieved, for example, –1 dB/+41 dB. Figure 3 shows the nominal maximum gain versus external resistor for this mode.



a. –10 dB to +30 dB; 90 MHz Bandwidth



b. 0 dB to +40 dB; 30 MHz Bandwidth



c. 10 dB to 50 dB; 9 MHz Bandwidth

Figure 2. Pin Strapping to Set Gain

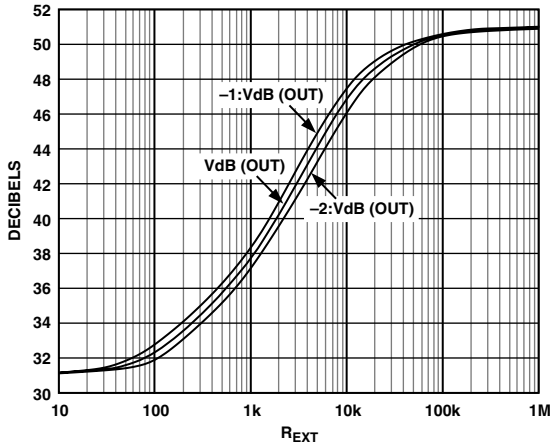


Figure 3. Gain vs. R_{EXT}, Showing Worst-Case Limits Assuming Internal Resistors Have a Maximum Tolerance of 20%

Optionally, when a resistor is placed from FDBK to COMM, higher gains can be achieved. This fourth mode is of limited value because of the low bandwidth and the elevated output offsets; it is thus not included in Figure 2.

The gain of this amplifier in the first two modes is set by the ratio of on-chip laser-trimmed resistors. While the ratio of these resistors is very accurate, the absolute value of these resistors can vary by as much as ±20%. Thus, when an external resistor is connected in parallel with the nominal 6.44 kΩ ± 20% internal resistor, the overall gain accuracy is somewhat poorer. The worst-case error occurs at about 2 kΩ (see Figure 4).

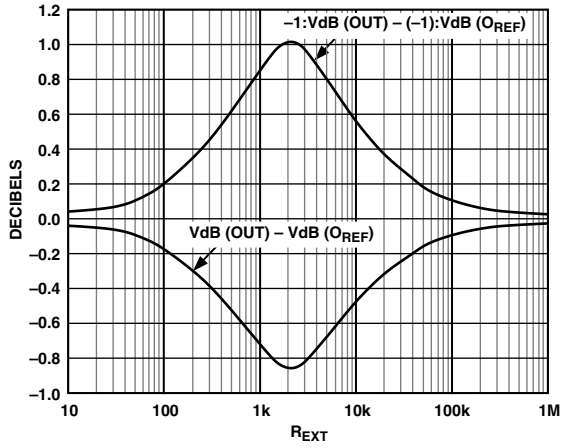


Figure 4. Worst-Case Gain Error, Assuming Internal Resistors Have a Maximum Tolerance of –20% (Top Curve) or +20% (Bottom Curve)

While the gain-bandwidth product of the fixed-gain amplifier is about 4 GHz, the actual bandwidth is not exactly related to the maximum gain. This is because there is a slight enhancing of the ac response magnitude on the maximum bandwidth range, due to higher order poles in the open-loop gain function; this mild peaking is not present on the higher gain ranges. Figure 2 shows how optional capacitors may be added to extend the frequency response in high gain modes.

CASCADING TWO AD603S

Two or more AD603s can be connected in series to achieve higher gain. Invariably, ac coupling must be used to prevent the dc offset voltage at the output of each amplifier from overloading the following amplifier at maximum gain. The required high pass coupling network will usually be just a capacitor, chosen to set the desired corner frequency in conjunction with the well-defined 100 Ω input resistance of the following amplifier.

For two AD603s, the total gain-control range becomes 84 dB (two times 42.14 dB); the overall –3 dB bandwidth of cascaded stages will be somewhat reduced. Depending on the pin-strapping, the gain and bandwidth for two cascaded amplifiers can range from –22 dB to +62 dB (with a bandwidth of about 70 MHz) to +22 dB to +102 dB (with a bandwidth of about 6 MHz).

There are several ways of connecting the gain-control inputs in cascaded operation. The choice depends on whether it is important to achieve the highest possible Instantaneous Signal-to-Noise Ratio (ISNR), or, alternatively, to minimize the ripple in the gain error. The following examples feature the AD603 programmed for maximum bandwidth; the explanations apply to other gain/bandwidth combinations with appropriate changes to the arrangements for setting the maximum gain.

Sequential Mode (Optimal S/N Ratio)

In the sequential mode of operation, the ISNR is maintained at its highest level for as much of the gain control range possible. Figure 5 shows the SNR over a gain range of –22 dB to +62 dB, assuming an output of 1 V rms and a 1 MHz bandwidth; Figure 6 shows the general connections to accomplish this. Here, both the positive gain-control inputs (GPOS) are driven in parallel by a positive-only, ground-referenced source with a range of 0 V to +2 V, while the negative gain-control inputs (GNEG) arc biased by stable voltages to provide the needed gain-offsets. These voltages may be provided by resistive dividers operating from a common voltage reference.

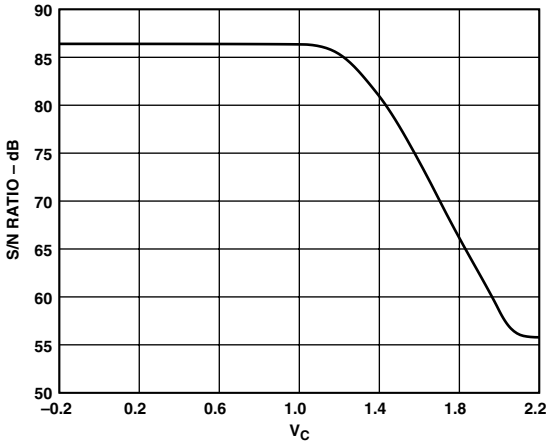


Figure 5. SNR vs. Control Voltage—Sequential Control (1 MHz Bandwidth)

The gains are offset (Figure 7) such that A2's gain is increased only after A1's gain has reached its maximum value. Note that for a differential input of –600 mV or less, the gain of a single amplifier (A1 or A2) will be at its minimum value of –11.07 dB; for a differential input of +600 mV or more, the gain will be at its maximum value of 31.07 dB. Control inputs beyond these limits will not affect the gain and can be tolerated without damage or foldover in the response. This is an important aspect of the AD603's gain-control response. (See the Specifications section of this data sheet for more details on the allowable voltage range) The gain is now

$$Gain\ (dB) = 40\ V_G + G_O \quad (3)$$

where V_G is the applied control voltage and G_O is determined by the gain range chosen. In the explanatory notes that follow, we assume the maximum-bandwidth connections are used, for which G_O is –20 dB.

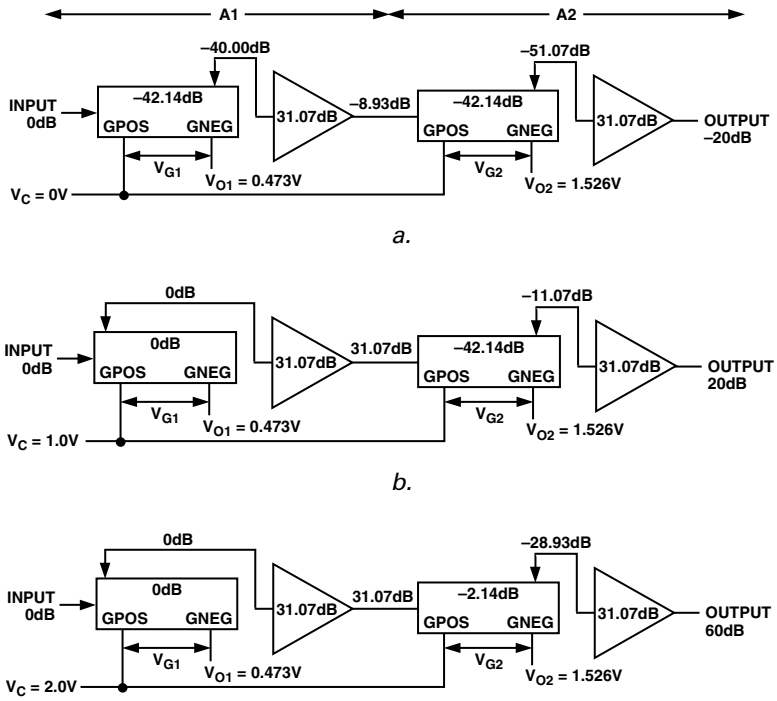


Figure 6. AD603 Gain Control Input Calculations for Sequential Control Operation

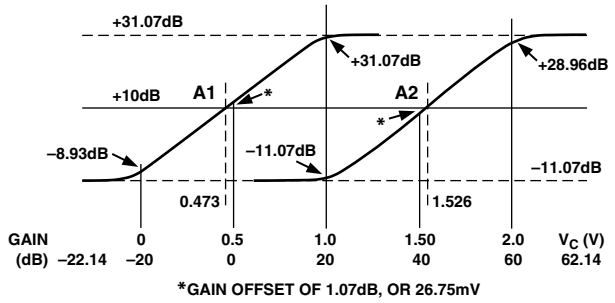


Figure 7. Explanation of Offset Calibration for Sequential Control

With reference to Figure 6, note that V_{G1} refers to the differential gain-control input to A1 and V_{G2} refers to the differential gain-control input to A2. When V_G is zero, V_{G1} = –473 mV and thus the gain of A1 is –8.93 dB (recall that the gain of each individual amplifier in the maximum-bandwidth mode is –10 dB for V_G = –500 mV and 10 dB for V_G = 0 V); meanwhile, V_{G2} = –1.908 V so the gain of A2 is "pinned" at –11.07 dB. The overall gain is thus –20 dB. This situation is shown in Figure 6a.

When V_G = +1.00 V, V_{G1} = 1.00 V – 0.473 V = +0.526 V, which sets the gain of A1 to at nearly its maximum value of 31.07 dB, while V_{G2} = 1.00 V – 1.526 V = 0.526 V, which sets A2's gain at nearly its minimum value –11.07 dB. Close analysis shows that the degree to which neither AD603 is completely pushed to its maximum or minimum gain exactly cancels in the overall gain, which is now +20 dB. This is depicted in Figure 6b.

When V_G = +2.0 V, the gain of A1 is pinned at 31.07 dB and that of A2 is near its maximum value of 28.93 dB, resulting in an overall gain of 60 dB (see Figure 6c). This mode of operation is further clarified by Figure 8, which is a plot of the separate gains of A1 and A2 and the overall gain versus the control voltage. Figure 9 is a plot of the gain error of the cascaded amplifiers versus the control voltage. Figure 10 is a plot of the gain error of the cascaded stages versus the control voltages.

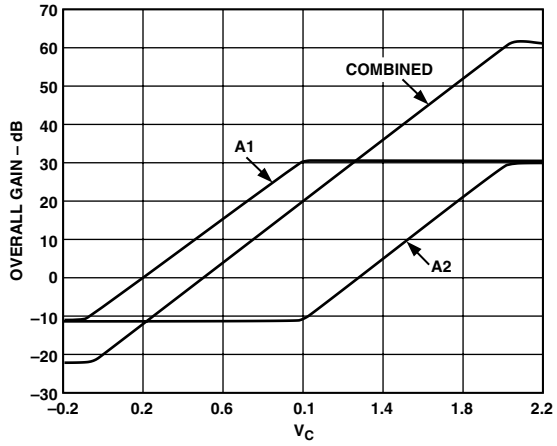


Figure 8. Plot of Separate and Overall Gains in Sequential Control

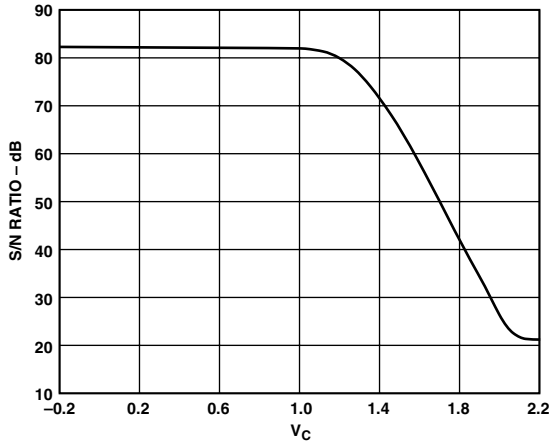


Figure 9. SNR for Cascaded Stages—Sequential Control

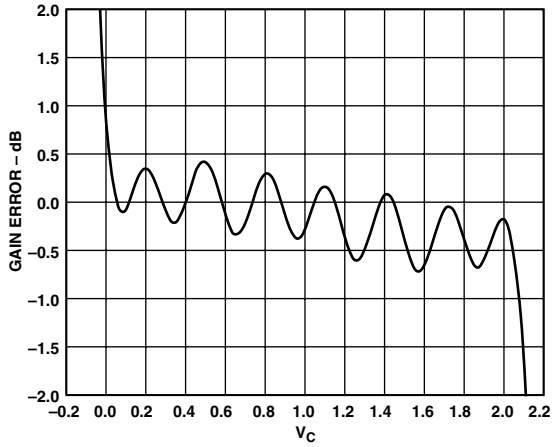


Figure 11. Gain Error for Cascaded Stages–Parallel Control

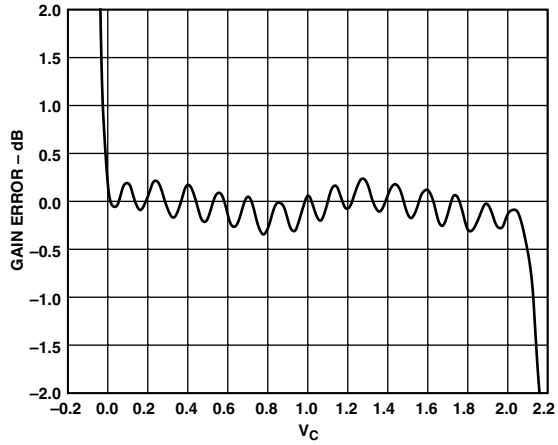


Figure 10. Gain Error for Cascaded Stages—Sequential Control

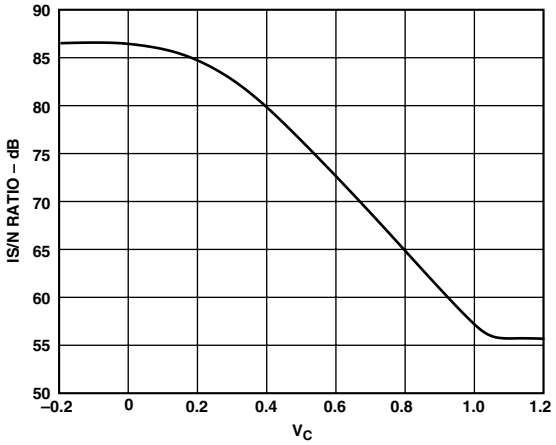


Figure 12. ISNR for Cascaded Stages–Parallel Control

Parallel Mode (Simplest Gain-Control Interface)

In this mode, the gain-control of voltage is applied to both inputs in parallel—the GPOS pins of both A1 and A2 are connected to the control voltage and the GNEW inputs are grounded. The gain scaling is then doubled to 80 dB/V, requiring only a 1.00 V change for an 80 dB change of gain:

$$Gain\ (dB) = 80\ V_G + G_O \qquad (4)$$

where, as before G_O depends on the range selected; for example, in the maximum-bandwidth mode, G_O is +20 dB. Alternatively, the GNEG pins may be connected to an offset voltage of 0.500 V, in which case, G_O is –20 dB.

The amplitude of the gain ripple in this case is also doubled, as shown in Figure 11, while the instantaneous signal-to-noise ratio at the output of A2 now decreases linearly as the gain increased (Figure 12).

Low Gain Ripple Mode (Minimum Gain Error)

As can be seen from Figures 9 and 10, the error in the gain is periodic, that is, it shows a small ripple. (Note that there is also a variation in the *output offset voltage*, which is due to the gain interpolation, but this is not exact in amplitude.) By offsetting the gains of A1 and A2 by half the period of the ripple, that is, by 3 dB, the residual gain errors of the two amplifiers can be made to cancel. Figure 13 shows that much lower gain ripple when configured in this manner. Figure 14 plots the ISNR as a function of gain; it is very similar to that in the "Parallel Mode."

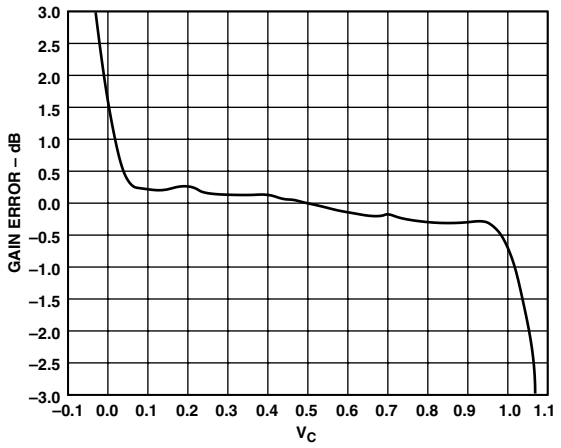


Figure 13. Gain Error for Cascaded Stages–Low Ripple Mode

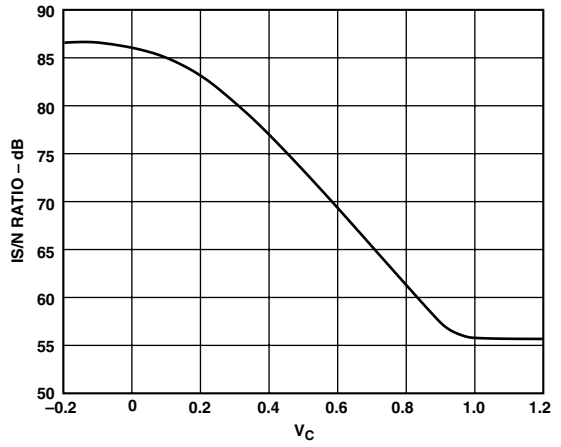


Figure 14. ISNR vs. Control Voltage–Low Ripple Mode

THEORY OF THE AD603

A Low Noise AGC Amplifier

Figure 15 shows the ease with which the AD603 can be connected as an AGC amplifier. The circuit illustrates many of the points previously discussed: It uses few parts, has linear-in-dB gain, operates from a single supply, uses two cascaded amplifiers in sequential gain mode for maximum S/N ratio, and an external resistor programs each amplifier's gain. It also uses a simple temperature-compensated detector.

The circuit operates from a single 10 V supply. Resistors R1, R2, R3, and R4 bias the common pins of A1 and A2 at 5 V. This pin is a low impedance point and must have a low impedance path to ground, here provided by the 100 μF tantalum capacitors and the 0.1 μF ceramic capacitors.

The cascaded amplifiers operate in sequential gain. Here, the offset voltage between the pins 2 (GNEG) of A1 and A2 is 1.05 V (42.14 dB × 25 mV/dB), provided by a voltage divider consisting of resistors R5, R6, and R7. Using standard values, the offset is not exact, but it is not critical for this application.

The gain of both A1 and A2 is programmed by resistors R13 and R14, respectively, to be about 42 dB; thus the maximum gain of the circuit is twice that, or 84 dB. The gain-control range can be shifted up by as much as 20 dB by appropriate choices of R13 and R14.

The circuit operates as follows. A1 and A2 are cascaded. Capacitor C1 and the 100 Ω of resistance at the input of A1 form a time-constant of 10 μs. C2 blocks the small dc offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 16 kHz, eliminating low frequency noise.

A half-wave detector is used, based on Q1 and R8. The current into capacitor C_{AV} is just the difference between the collector current of Q2 (biased to be 300 μA at 300 K, 27°C) and the collector current of Q1, which increases with the amplitude of the

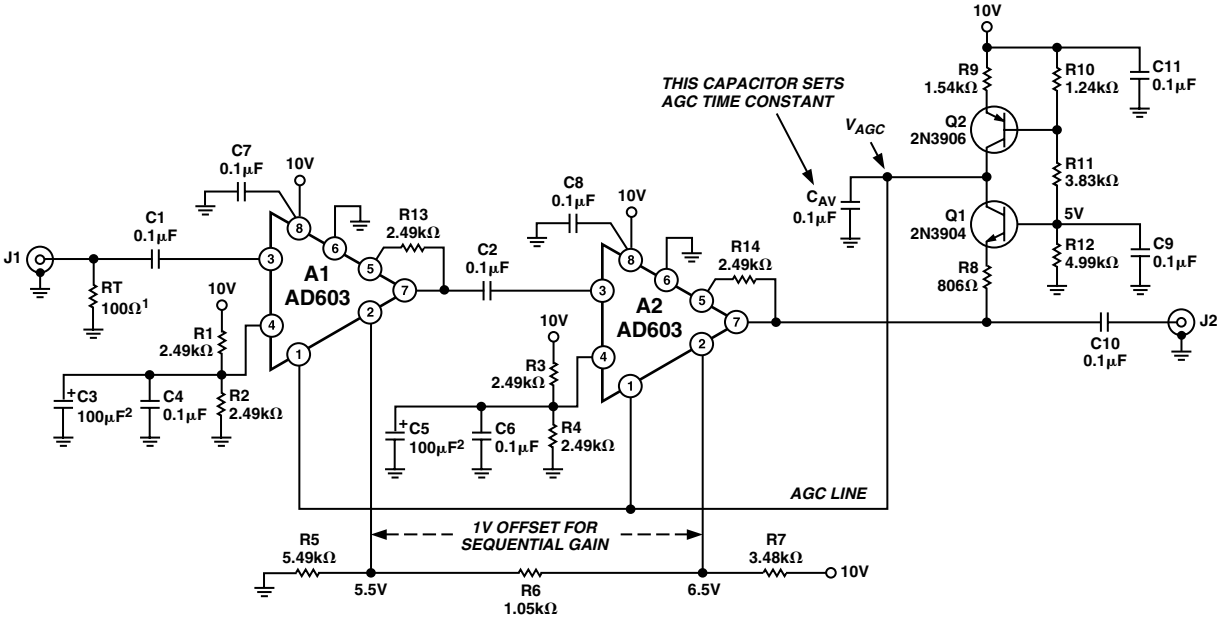


Figure 15. A Low Noise AGC Amplifier

output signal. The automatic gain control voltage, V_{AGC}, is the time-integral of this *error* current. In order for V_{AGC} (and thus the gain) to remain insensitive to short-term amplitude fluctuations in the output signal, the rectified current in Q1 must, on average, exactly balance the current in Q2. If the output of A2 is too small to do this, V_{AGC} will increase, causing the gain to increase, until Q1 conducts sufficiently.

Consider the case where R8 is zero and the output voltage V_{OUT} is a square wave at, say, 455 kHz, which is well above the corner frequency of the control loop.

During the time V_{OUT} is negative with respect to the base voltage of Q1, Q1 conducts; when V_{OUT} is positive, it is cut off. Since the average collector current of Q1 is forced to be 300 μA, and the square wave has a duty-cycle of 1:1, Q1's collector current when conducting must be 600 μA. With R8 omitted, the peak amplitude of V_{OUT} is forced to be just the V_{BE} of Q1 at 600 μA, typically about 700 mV, or 2 V_{BE} peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically –1.7 mV/°C. Although this may not be troublesome in some applications, the correct value of R8 will render the output stable with temperature.

To understand this, first note that the current in Q2 is made to be proportional to absolute temperature (PTAT). For the moment, continue to assume that the signal is a square wave.

When Q1 is conducting, V_{OUT} is now the sum of V_{BE} and a voltage that is PTAT and which can be chosen to have an equal but opposite TC to that of the V_{BE}. This is actually nothing more than an application of the "bandgap voltage reference" principle. When R8 is chosen such that the sum of the voltage across it and the V_{BE} of Q1 is close to the bandgap voltage of about 1.2 V, V_{OUT} will be stable over a wide range of temperatures, provided, of course, that Q1 and Q2 share the same thermal environment.

Since the average emitter current is 600 μA during each half-cycle of the square wave a resistor of 833 Ω would add a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value will depend on the type of transistor used and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the inexpensive 2N3904/2N3906 pair and sine wave signals, the recommended value is 806 Ω.

This resistor also serves to lower the peak current in Q1 when more typical signals (usually, sinusoidal) are involved, and the 1.8 kHz LP filter it forms with C_{AV} helps to minimize distortion due to ripple in V_{AGC}. Note that the output amplitude under sine wave conditions will be higher than for a square wave, since the average value of the current *for an ideal rectifier* would be 0.637 times as large, causing the output amplitude to be 1.88 (=1.2/0.637) V, or 1.33 V rms. In practice, the somewhat nonideal rectifier results in the sine wave output being regulated to about 1.4 V rms, or 3.6 V p-p.

The bandwidth of the circuit exceeds 40 MHz. At 10.7 MHz, the AGC threshold is 100 μV (–67 dBm) and its maximum gain is 83 dB (20 log 1.4 V/100 μV). The circuit holds its output at 1.4 V rms for inputs as low as –67 dBm to +15 dBm (82 dB), where the input signal exceeds the AD603's maximum input rating. For a 30 dBm input at 10.7 MHz, the second harmonic is 34 dB down from the fundamental and the third harmonic is 35 dB down.

CAUTION

Careful component selection, circuit layout, power-supply decoupling, and shielding are needed to minimize the AD603's susceptibility to interference from radio and TV stations, etc. In bench evaluation, we recommend placing all of the components in a shielded box and using feedthrough decoupling networks for the supply voltage. Circuit layout and construction are also critical, since stray capacitances and lead inductances can form resonant circuits and are a potential source of circuit peaking, oscillation, or both.

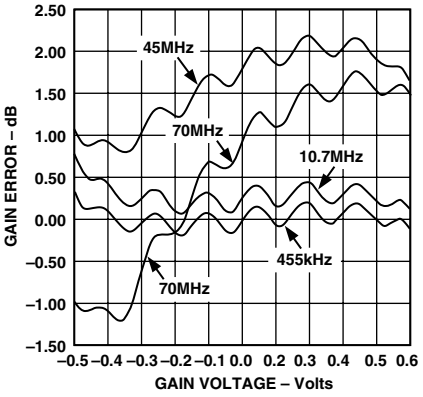


Figure 16. Gain Error vs. Gain Control Voltage at 455 kHz, 10.7 MHz, 45 MHz, 70 MHz

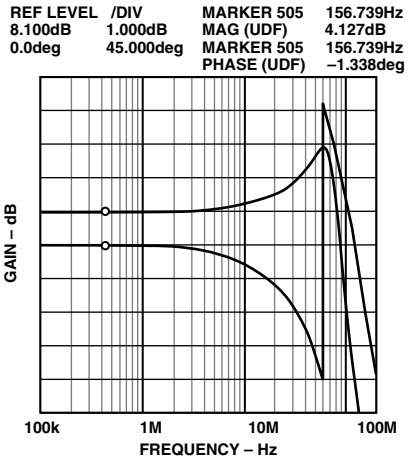


Figure 17. Frequency and Phase Response vs. Gain (Gain = –10 dB, P_{IN} = –30 dBm, Pin 5 Connected to Pin 7)

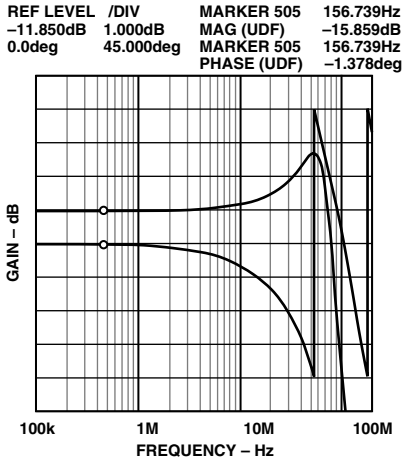


Figure 18. Frequency and Phase Response vs. Gain (Gain = +10 dB, P_{IN} = –30 dBm, Pin 5 Connected to Pin 7)

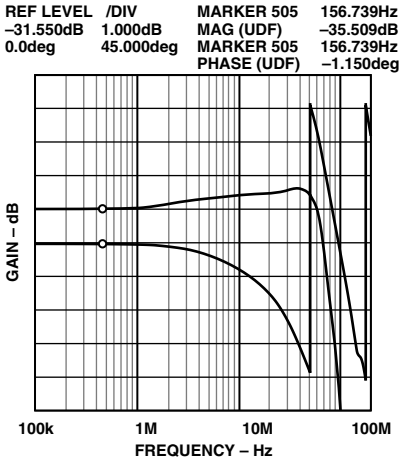


Figure 19. Frequency and Phase Response vs. Gain (Gain = +30 dB, P_{IN} = –30 dBm, Pin 5 Connected to Pin 7)

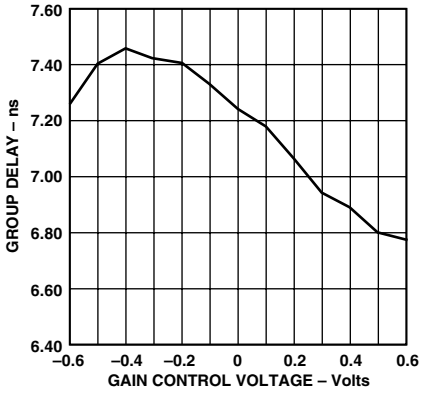


Figure 20. Group Delay vs. Gain Control Voltage

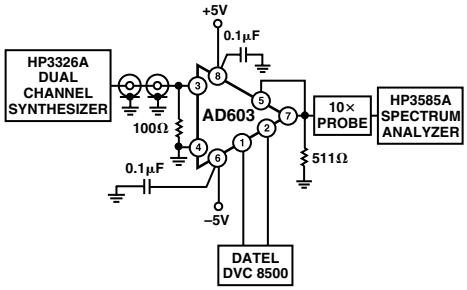


Figure 21. Third Order Intermodulation Distortion Test Setup

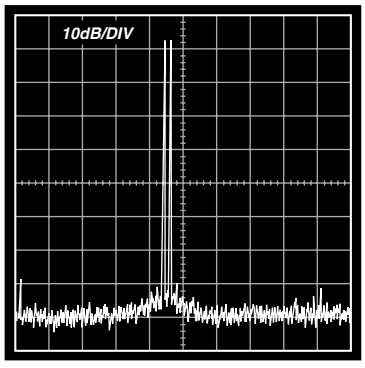


Figure 22. Third Order Intermodulation Distortion at 455 kHz (10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, P_{IN} = 0 dBm, Pin 5 Connected to Pin 7)

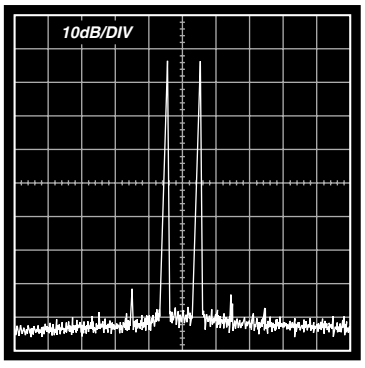


Figure 23. Third Order Intermodulation Distortion at 10.7 MHz (10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, P_{IN} = 0 dBm, Pin 5 Connected to Pin 7)

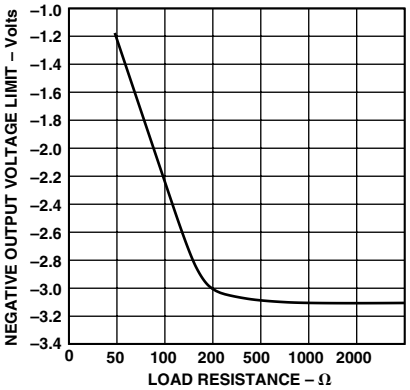


Figure 24. Typical Output Voltage Swing vs. Load Resistance (Negative Output Swing Limits First)

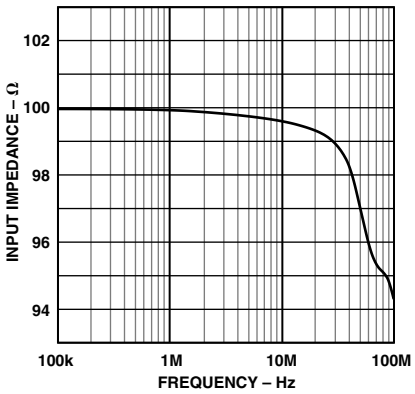


Figure 25. Input Impedance vs. Frequency (Gain = –10 dB)

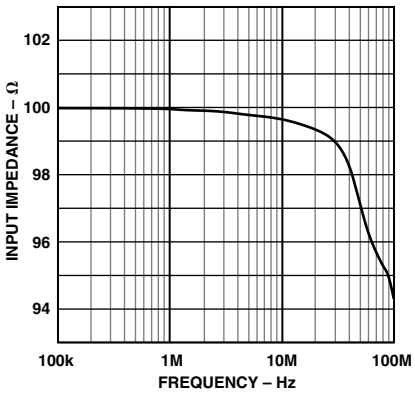


Figure 26. Input Impedance vs. Frequency (Gain = +10 dB)

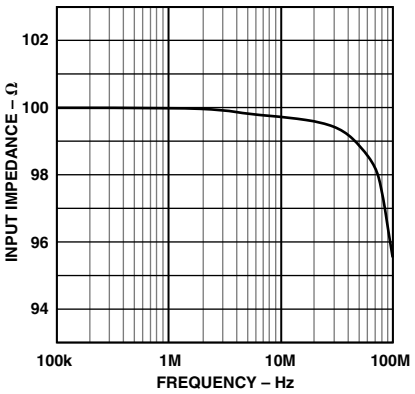


Figure 27. Input Impedance vs. Frequency (Gain = +30 dB)

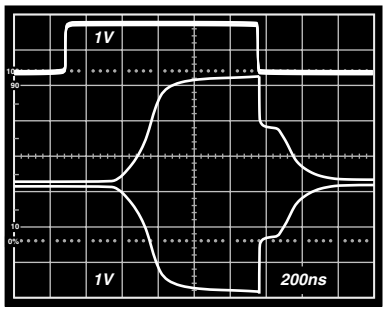


Figure 28. Gain-Control Channel Response Time

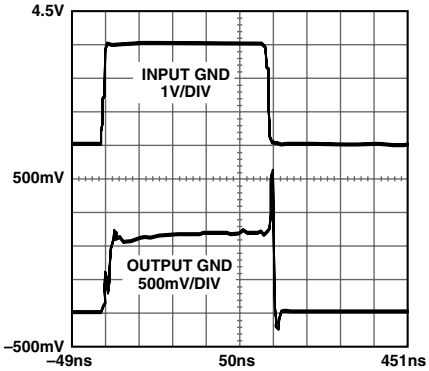


Figure 29. Input Stage Overload Recovery Time, Pin 5 Connected to Pin 7 (Input Is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

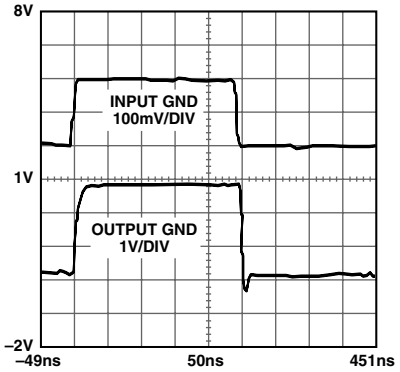


Figure 30. Output Stage Overload Recovery Time, Pin 5 Connected to Pin 7 (Input Is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

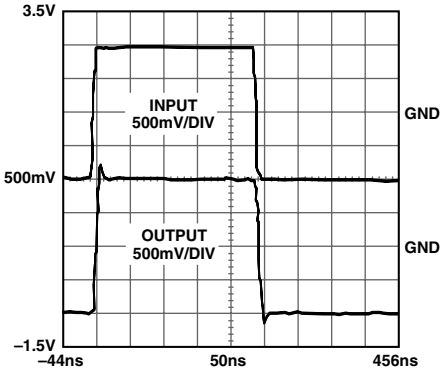


Figure 31. Transient Response, G = 0 dB, Pin 5 Connected to Pin 7 (Input is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

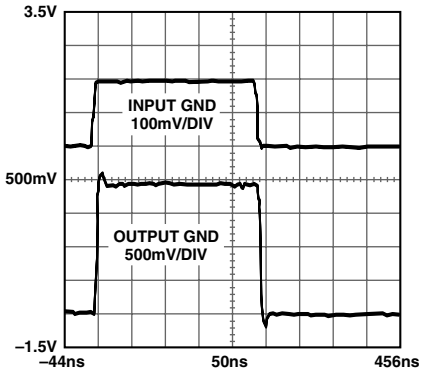


Figure 32. Transient Response, G = +20 dB, Pin 5 Connected to Pin 7 (Input is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

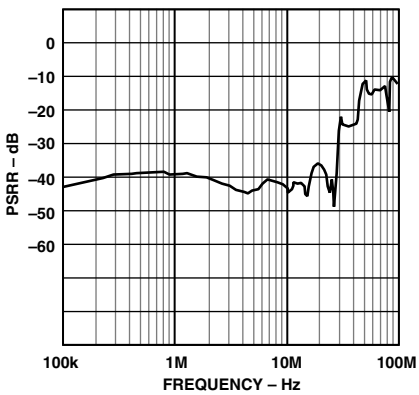


Figure 33. PSRR vs. Frequency (Worst Case Is Negative Supply PSRR, Shown Here)

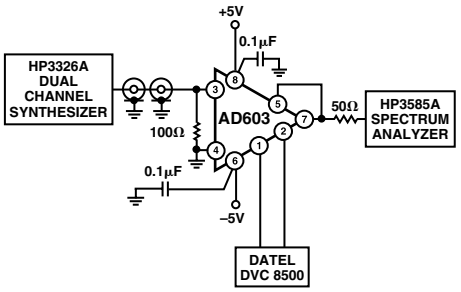


Figure 34. Test Setup Used for: Noise Figure, 3rd Order Intercept and 1 dB Compression Point Measurements

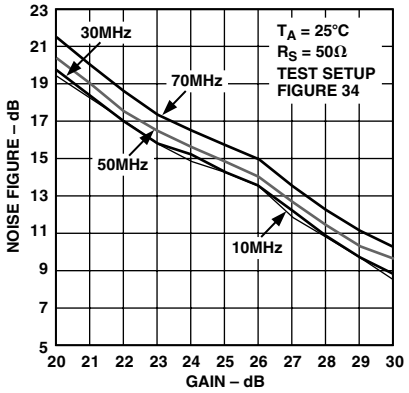


Figure 35. Noise Figure in –10 dB/ +30 dB Mode

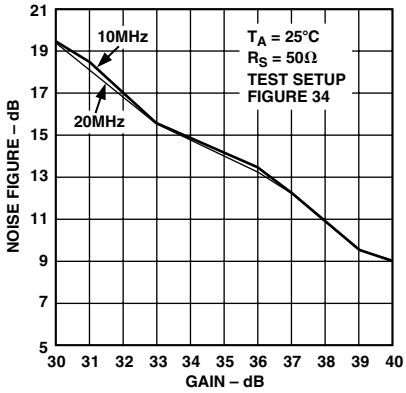


Figure 36. Noise Figure in 0 dB/40 dB Mode

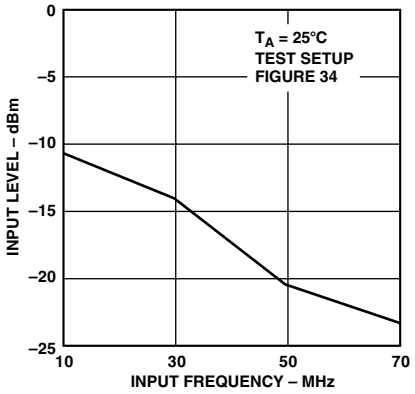


Figure 37. 1 dB Compression Point, –10 dB/+30 dB Mode, Gain = 30 dB

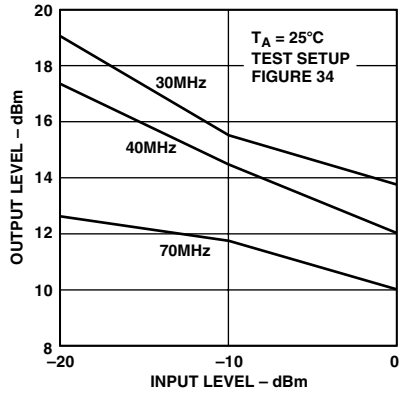


Figure 38. 3rd Order Intercept –10 dB/ +30 dB Mode, Gain = 10 dB

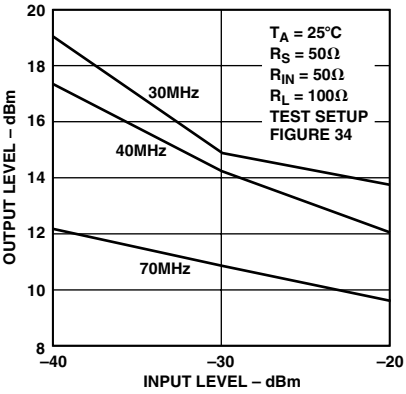
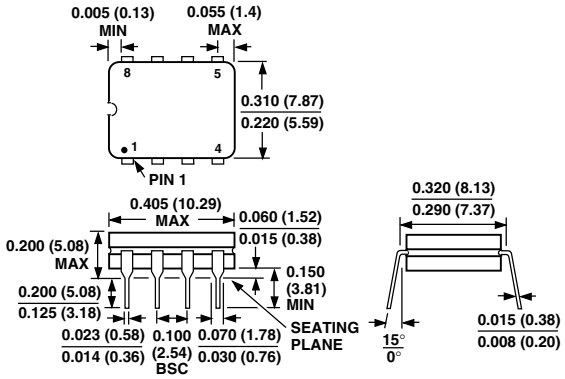


Figure 39. 3rd Order Intercept, –10 dB/ +30 dB Mode, Gain = 30 dB

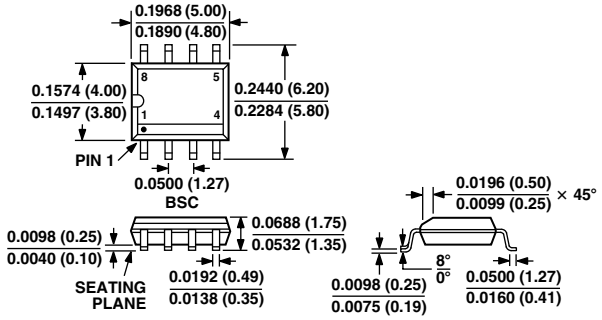
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Cerdip (Q-8)



8-Lead SOIC (SO-8)



C00539a–0–11/00 (rev. D)

PRINTED IN U.S.A.

Appendix D: Linear Technology LTC1451 – 12–bit Rail to Rail DAC

Included for your reference on the following pages is the data sheet for the LTC1451 12–bit Rail to Rail DAC, provided by the courtesy of Linear Technology Corp., Milpitas, CA.

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12-Bit Rail-to-Rail Micropower DACs in SO-8

FEATURES

- 12-Bit Resolution
- **Buffered True Rail-to-Rail Voltage Output**
- 3V Operation (LTC1453), I_{CC}: 250µA Typ
- 5V Operation (LTC1451), I_{CC}: 400µA Typ
- 3V to 5V Operation (LTC1452), I_{CC}: 225µA Typ
- Built-In Reference: 2.048V (LTC1451)
  1.220V (LTC1453)
- Multiplying Version (LTC1452)
- Power-On Reset
- **SO-8 Package**
- 3-Wire Cascadable Serial Interface
- **Maximum DNL Error: 0.5LSB**
- Low Cost

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

DESCRIPTION

The LTC®1451/LTC1452/LTC1453 are complete single supply, rail-to-rail voltage output 12-bit digital-to-analog converters (DACs) in an SO-8 package. They include an output buffer amplifier and an easy-to-use 3-wire cascadable serial interface.

The LTC1451 has an onboard reference of 2.048V and a full-scale output of 4.095V. It operates from a single 4.5V to 5.5V supply.

The LTC1452 is a multiplying DAC with a full-scale output of twice the reference input voltage. It operates from a single supply of 2.7V to 5.5V.

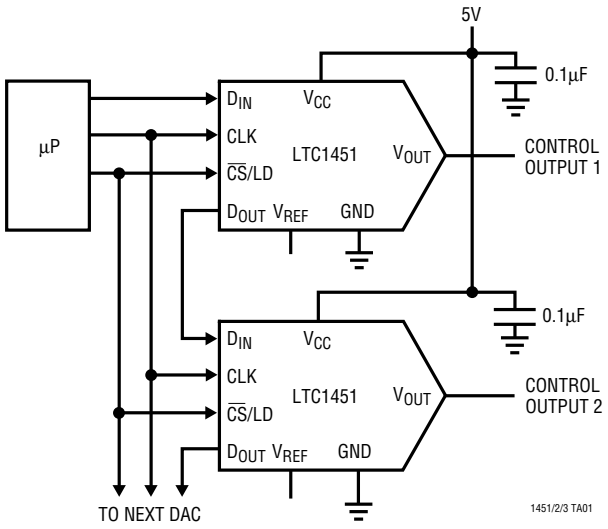
The LTC1453 has an onboard 1.22V reference and a full-scale output of 2.5V. It operates from a single supply of 2.7V to 5.5V.

The low power supply current makes the LTC1451 family ideal for battery-powered applications. The space saving 8-pin SO package and operation with no external components provide the smallest 12-bit DAC system available.

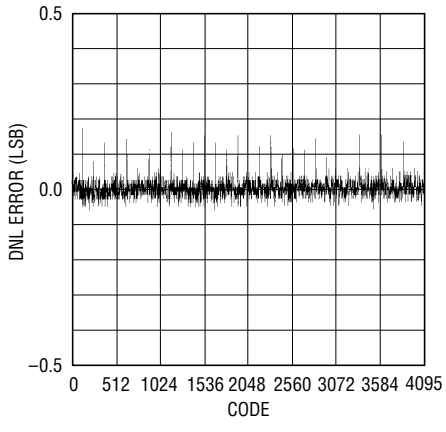
, LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

Daisy-Chained Control Outputs



Differential Nonlinearity vs Input Code

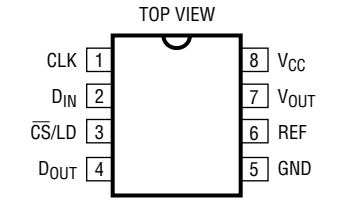


ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... –0.5V to 7.5V
TTL Input Voltage ..... –0.5V to 7.5V
V_{OUT} ..... –0.5V to V_{CC} + 0.5V
REF ..... –0.5V to V_{CC} + 0.5V
Maximum Junction Temperature ..... –65°C to 125°C

Operating Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER		S8 PART MARKING
LTC1451CN8	LTC1451CS8	1451C
LTC1452CN8	LTC1452CS8	1451I
LTC1453CN8	LTC1453CS8	1452C
LTC1451IN8	LTC1451IS8	1452I
LTC1452IN8	LTC1452IS8	1453C
LTC1453IN8	LTC1453IS8	1453I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1451), 2.7V to 5.5V (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), V_{OUT} and REF unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 1)	●			±0.5	LSB
INL	Integral Nonlinearity	T_A = 25°C				±3.5	LSB
		(Note 1)	●			±4	LSB
V_{OS}	Offset Error	T_A = 25°C				±12	mV
			●			±18	mV
$V_{OS}TC$	Offset Error Temperature Coefficient				±15		µV/°C
V_{FS}	Full-Scale Voltage	When Using Internal Reference, LTC1451, T_A = 25°C		4.065	4.095	4.125	V
		LTC1451	●	4.045	4.095	4.145	V
		External 2.048V Reference, V_{CC} = 5V, LTC1452	●	4.075	4.095	4.115	V
		When Using Internal Reference, LTC1453, T_A = 25°C		2.470	2.500	2.530	V
		LTC1453	●	2.460	2.500	2.540	V
$V_{FS}TC$	Full-Scale Voltage Temperature Coefficient	When Using Internal Reference, LTC1451			±0.10		LSB/°C
		When Using External 2.048V Reference, LTC1452			±0.02		LSB/°C
		When Using Internal Reference, LTC1453			±0.10		LSB/°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1451), 2.7V to 5.5V (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), V_{OUT} and REF unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference (LTC1451/LTC1453)							
	Reference Output Voltage	LTC1451 LTC1453	● ●	2.008 1.195	2.048 1.220	2.088 1.245	V V
	Reference Output Temperature Coefficient				±0.08		LSB/°C
	Reference Line Regulation		●		0.7	±2	LSB/V
	Reference Load Regulation	$0 \leq I_{OUT} \leq 100\mu A$, LTC1451 LTC1453	● ●		0.2 0.6	±1.5 ±3	LSB LSB
	Reference Input Range	$V_{REF} \leq V_{CC} - 1.5V$	●			$V_{CC}/2$	V
	Reference Input Resistance		●	8	14	30	kΩ
	Reference Input Capacitance				15		pF
	Short-Circuit Current	REF Shorted to GND	●			80	mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance, LTC1451 LTC1452 LTC1453	● ● ●	4.5 2.7 2.7		5.5 5.5 5.5	V V V
I_{CC}	Supply Current	$4.5V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1451 $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1452 $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1453	● ● ●	300 120 150	400 225 250	620 350 500	µA µA µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●			100	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●			120	mA
	Output Impedance to GND	Input Code = 0	●		40	120	Ω
AC Performance							
	Voltage Output Slew Rate	(Note 2)	●	0.5	1.0		V/µs
	Voltage Output Settling Time	(Notes 2, 3) to ±0.5LSB			14		µs
	Digital Feedthrough				0.3		nV•s
	AC Feedthrough	REF = 1kHz, $2V_{P-P}$, LTC1452			–95		dB
SINAD	Signal-to-Noise + Distortion	REF = 1kHz, $2V_{P-P}$, (Code: All 1s) LTC1452			85		dB

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V (LTC1451LTC1452), V_{CC} = 3V (LTC1453), $T_A = T_{MIN}$ to T_{MAX}

SYMBOL	PARAMETER	CONDITIONS		LTC1451/LTC1452 MIN	LTC1451/LTC1452 TYP	LTC1451/LTC1452 MAX	LTC1453 MIN	LTC1453 TYP	LTC1453 MAX	UNITS
Digital I/O										
V_{IH}	Digital Input High Voltage		●	2.4			2.0			V
V_{IL}	Digital Input Low Voltage		●			0.8			0.6	V
V_{OH}	Digital Output High Voltage	I_{OUT} = –1mA	●			V_{CC} – 1.0			V_{CC} – 0.7	V
V_{OL}	Digital Output Low Voltage	I_{OUT} = 1mA	●	0.4			0.4			V
I_{LEAK}	Digital Input Leakage	V = GND to V_{CC}	●			±10			±10	µA
C_{IN}	Digital Input Capacitance	Guaranteed by Design Not Subject to Test	●			10			10	pF
Switching										
t_1	D_{IN} Valid to CLK Setup		●			40			60	ns
t_2	D_{IN} Valid to CLK Hold		●			0			0	ns
t_3	CLK High Time		●			40			60	ns
t_4	CLK Low Time		●			40			60	ns
t_5	$\overline{CS}$/LD Pulse Width		●			50			80	ns
t_6	LSB CLK to $\overline{CS}$/LD		●			40			60	ns
t_7	$\overline{CS}$/LD Low to CLK		●			20			30	ns
t_8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●			150			220	ns
t_9	CLK Low to $\overline{CS}$/LD Low		●			20			30	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full scale).

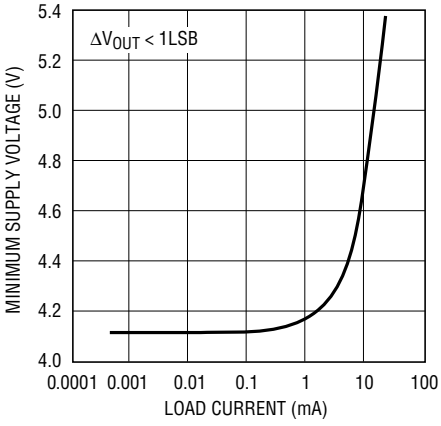
Note 2: Load is 5kΩ in parallel with 100pF.

Note 3: DAC switched between all 1s and the code corresponding to V_{OS} for the part, i.e., LTC1451: code 18; LTC1453: code 30.

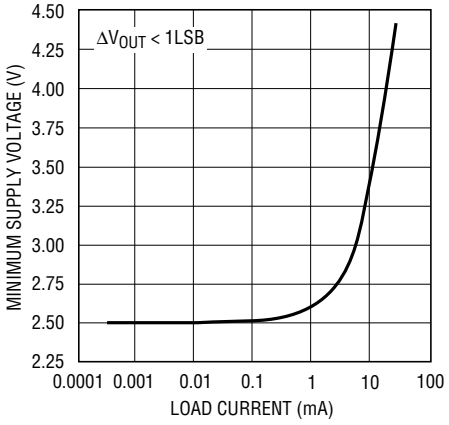
Note 4: Digital inputs at 0V or V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

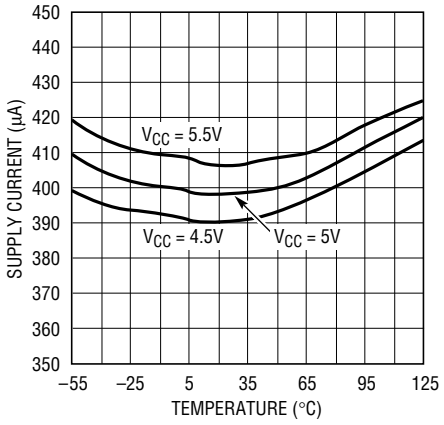
LTC1451 Minimum Supply Voltage vs Load Current



LTC1453 Minimum Supply Voltage vs Load Current

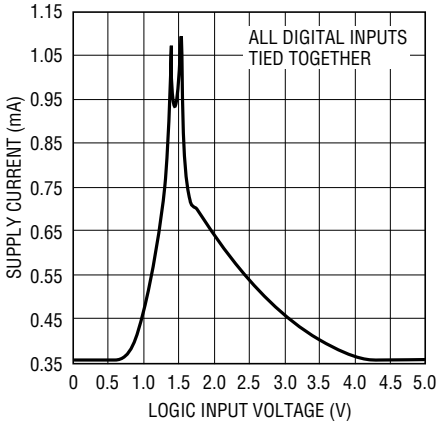


LTC1451 Supply Current vs Temperature

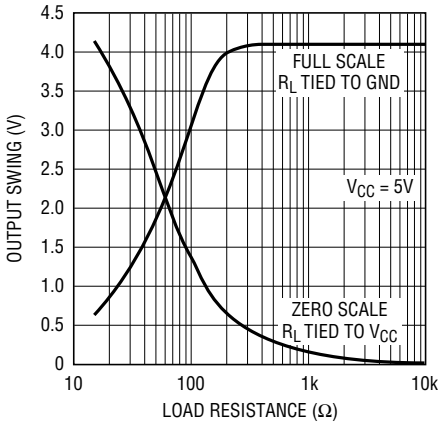


TYPICAL PERFORMANCE CHARACTERISTICS

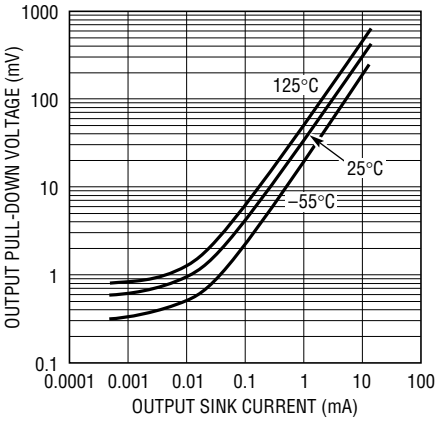
LTC1451
Supply Current vs Logic Input Voltage



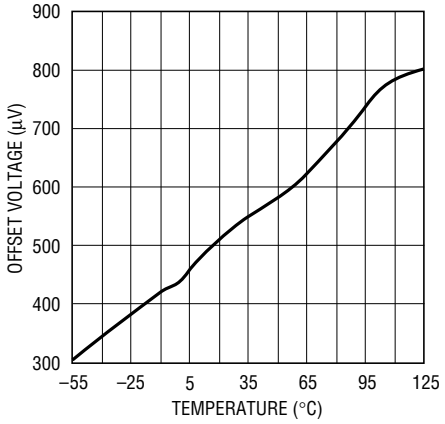
LTC1451
Output Swing vs Load Resistance



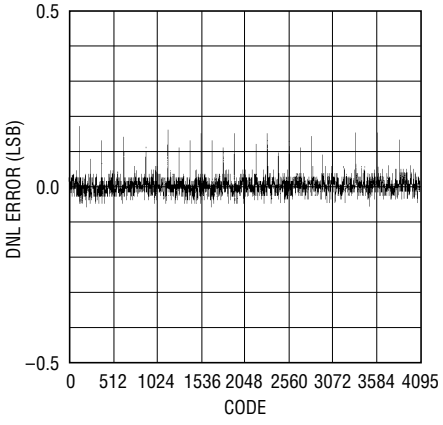
LTC1451
Pull-Down Voltage vs Output Sink Current Capability



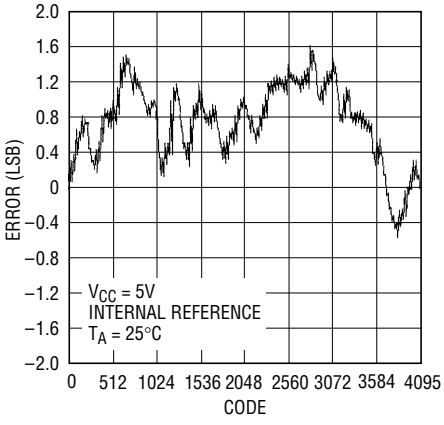
LTC1451
Offset Voltage vs Temperature



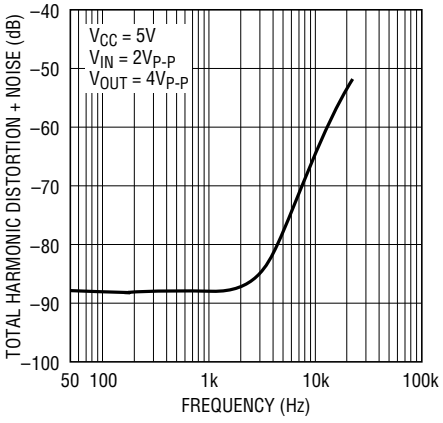
LTC1451
Differential Nonlinearity (DNL)



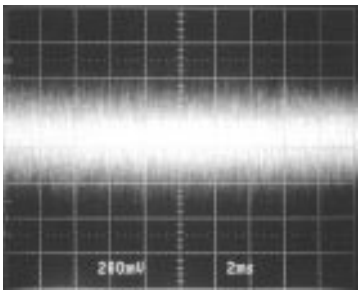
LTC1451
Integral Nonlinearity (INL)



LTC1452
Total Harmonic Distortion + Noise vs Frequency



LTC1451
Broadband Output Noise



PIN FUNCTIONS

CLK: The TTL Level Input for the Serial Interface Clock.

D_{IN}: The TTL Level Input for the Serial Interface Data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock.

$\overline{CS}$/LD: The TTL Level Input for the Serial Interface Enable and Load Control. When $\overline{CS}$/LD is low the CLK signal is enabled, so the data can be clocked in. When $\overline{CS}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

D_{OUT}: The Output of the Shift Register which Becomes Valid on the Rising Edge of the Serial Clock.

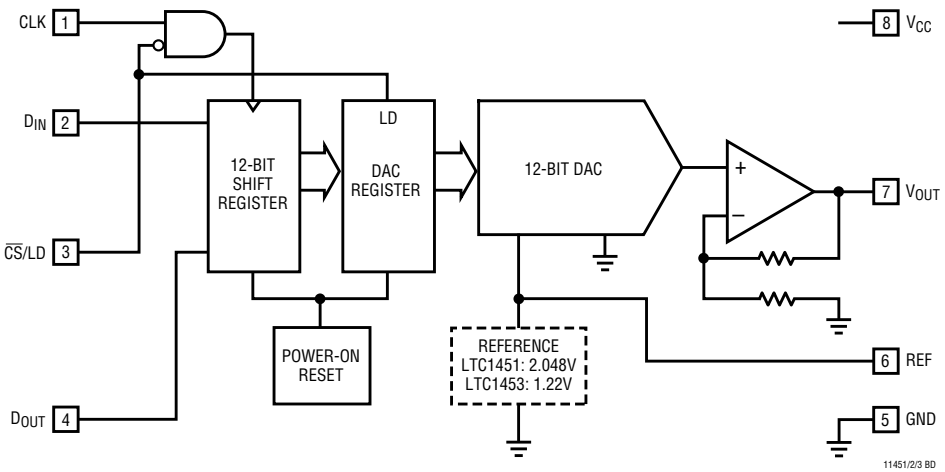
GND: Ground.

REF: The Output of the Internal Reference and the Input to the DAC Resistor Ladder. An external reference with voltage up to $V_{CC}/2$ may be used for the LTC1452.

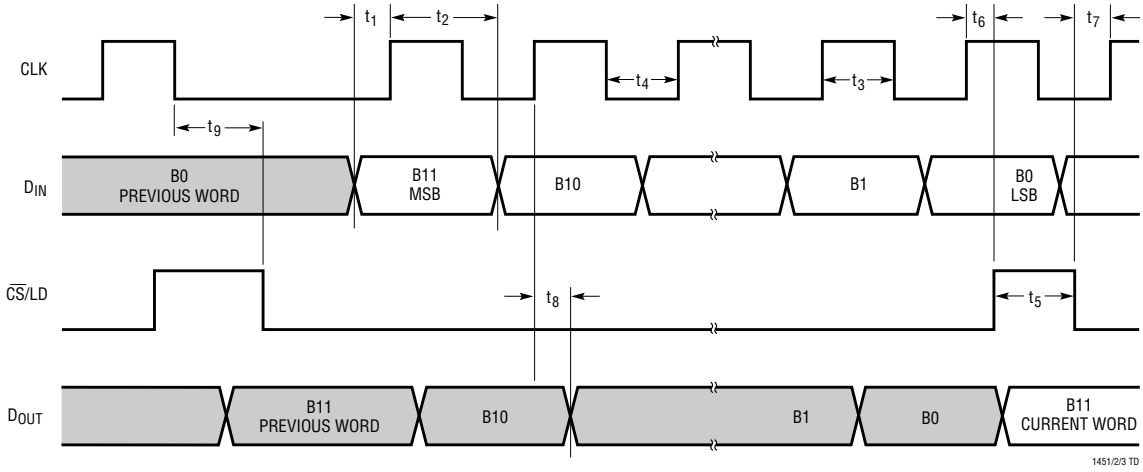
V_{OUT}: The Buffered DAC Output.

V_{CC}: The Positive Supply Input. $4.5V \leq V_{CC} \leq 5.5V$ (LTC1451), $2.7 \leq V_{CC} \leq 5.5V$ (LTC1452/LTC1453). Requires a bypass capacitor to ground.

BLOCK DIAGRAM



TIMING DIAGRAM



DEFINITIONS

Resolution (n): Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): This is the output of the DAC when all bits are set to 1.

Voltage Offset Error (V_{OS}): The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code \times V_{FS})/(2^n - 1)]$$

Least Significant Bit (LSB): One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/4095$$

Nominal LSBs:

LTC1451	LSB = 4.095V/4095 = 1mV
LTC1452	LSB = V(REF)/4095
LTC1453	LSB = 2.5V/4095 = 0.610mV

Integral Nonlinearity (INL): End-point INL is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)]/LSB$$

V_{OUT} = The output voltage of the DAC measured at the given input code

Differential Nonlinearity (DNL): DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in nV × sec.

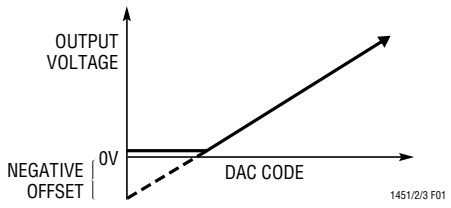


Figure 1. Effect of Negative Offset

OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first. The DAC register loads the data from the shift register when $\overline{CS}$/LD is pulled high. The CLK is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse.

The buffered output of the 12-bit shift register is available on the D_{OUT} pin which swings from GND to V_{CC}.

Multiple LTC1451/LTC1452/LTC1453s may be daisy-chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip, while the CLK and $\overline{CS}$/LD signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously.

Reference

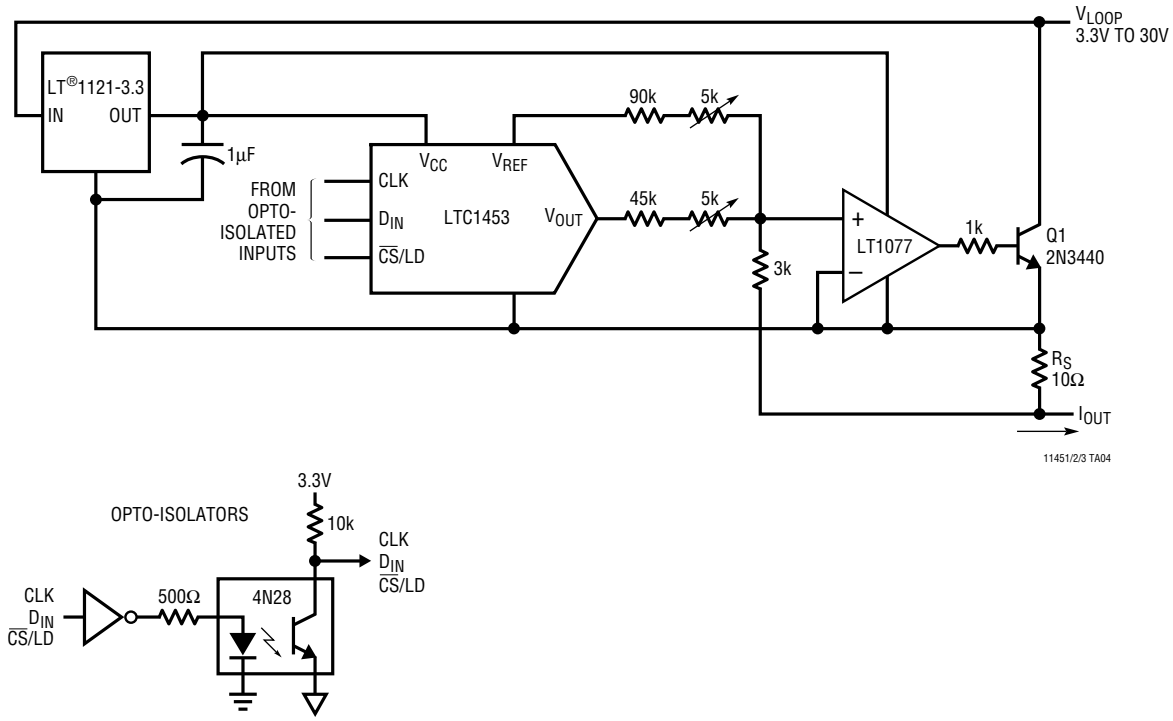
The LTC1451 includes an internal 2.048V reference, making 1LSB equal to 1mV (gain of 2). The LTC1453 has an internal reference of 1.22V with a full scale of 2.5V (gain of 2.05). The internal reference output is turned off when the pin is forced above the reference voltage, allowing an external reference to be connected to the reference pin. The LTC1452 has no internal reference and the REF pin must be driven externally. The buffer gain is 2, so the external reference must be less than $V_{CC}/2$ and be capable of driving the 8k minimum DAC resistor ladder.

Voltage Output

The LTC1451 family's rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

TYPICAL APPLICATIONS

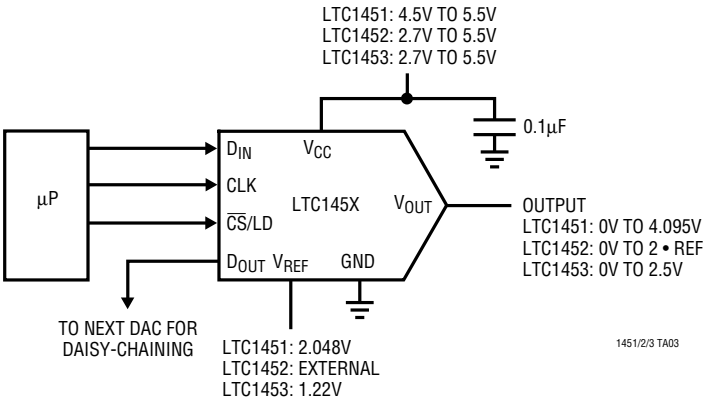
An Isolated 4mA to 20mA Process Controller Has 3.3V Minimum Loop Voltage



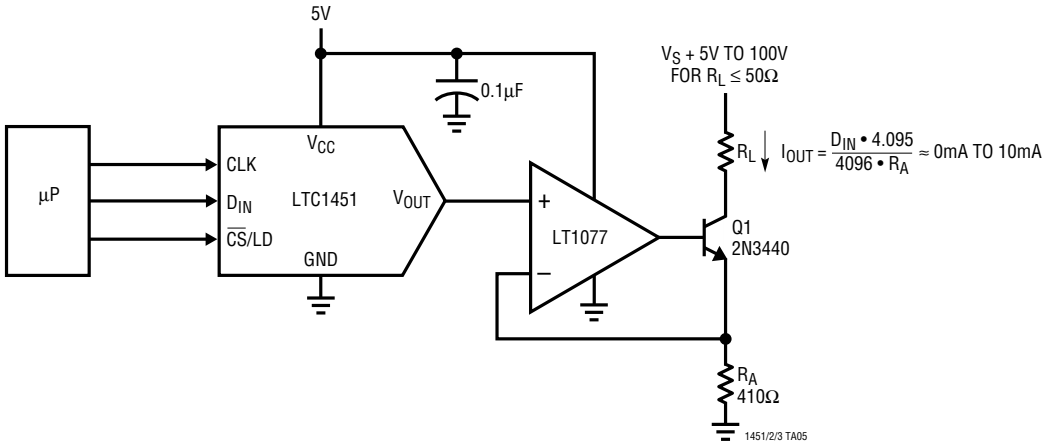
This circuit shows how to use an LTC1453 to make an opto-isolated digitally controlled 4mA to 20mA process controller. The controller circuitry, including the opto-isolation, is powered by the loop voltage that can have a wide range of 3.3V to 30V. The 1.22V reference output of the LTC1453 is used for the 4mA offset current and V_{OUT} is used for the digitally controlled 0mA to 16mA current. R_S is a sense resistor and the op amp modulates the transistor Q1 to provide the 4mA to 20mA current through this resistor. The potentiometers allow for offset and full-scale adjustment. The control circuitry dissipates well under the 4mA budget at zero-scale.

TYPICAL APPLICATIONS

12-Bit 3V to 5V Voltage Output DAC



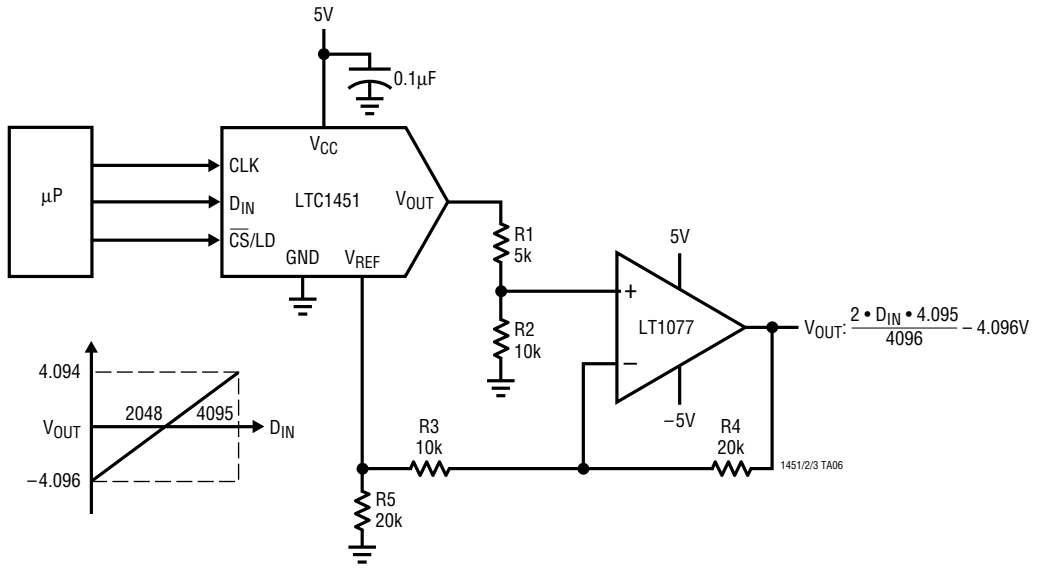
Digitally Programmable Current Source



This circuit shows a digitally programmable current source from an external voltage source using an external op amp, an LT1077 and an NPN transistor (2N3440). Any digital word from 0 to 4095 is loaded into the LTC1451 and its output correspondingly swings from 0V to 4.095V. In the configuration shown, this voltage will be forced across the resistor R_A. If R_A is chosen to be 410Ω the output current will range from 0mA at zero-scale to 10mA at full-scale. The minimum voltage for V_S is determined by the load resistor R_L and Q1's V_{CESAT} voltage. With a load resistor of 50Ω, the voltage source can be as low as 5V.

TYPICAL APPLICATIONS

A Wide Swing, Bipolar Output 12-Bit DAC



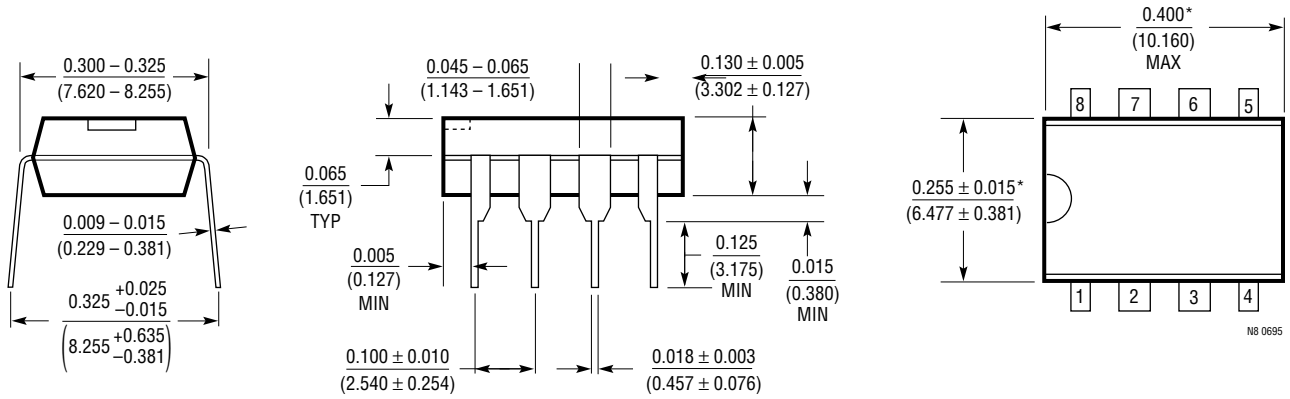
This circuit shows how to make a bipolar output 12-bit DAC with a wide output swing using an LTC1451 and an LT®1077. R1 and R2 resistively divide down the LTC1451 output and an offset is summed in using the LTC1451 onboard 2.048V reference and R3 and R4. R5 ensures that the onboard reference is always sourcing current and never has to sink any current even when V_{OUT} is at full-scale. The LT1077 output will have a wide bipolar output swing of –4.096V to 4.094V as shown in the figure above. With this output swing 1LSB = 2mV.

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

PACKAGE DESCRIPTION

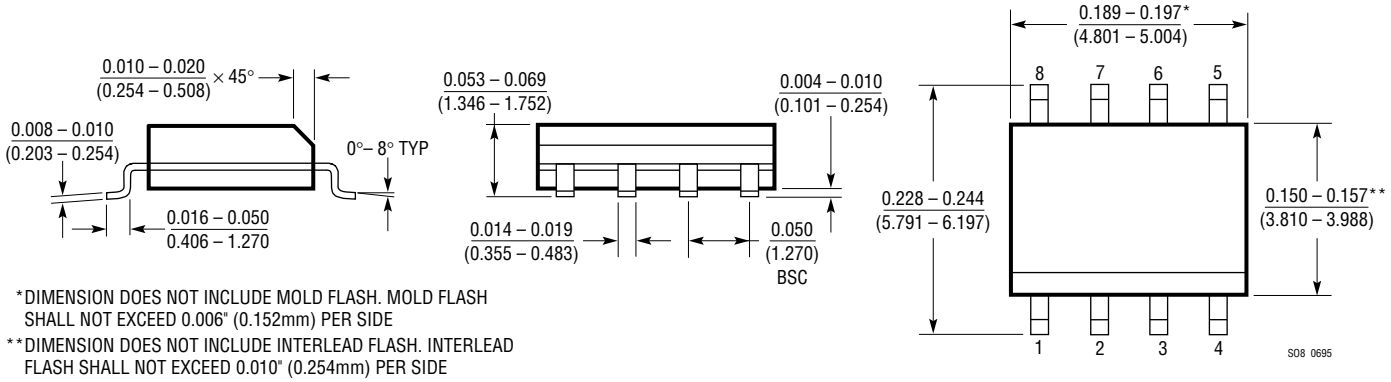
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic SOIC



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit V_{OUT} DAC, Full Scale: 2.048V, V_{CC}: 4.75V to 15.75V. Reference Can Be Overdriven Up to 12V, i.e., FS MAX = 12V	5V to 15V Single Supply, Complete V_{OUT} DAC in SO-8 Package
LTC7541	12-Bit Multiplying Parallel I_{OUT} DAC	5V to 16V Supply, 12-Bit Wide Interface
LTC7543/LTC8143	12-Bit Multiplying Serial I_{OUT} DAC	5V Supply, Clear Pin and Serial Data Output (LTC8143)
LTC8043	12-Bit Multiplying Serial I_{OUT} DAC	5V Supply, SO-8 Package

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Appendix E: Configuration EEPROM Format

E.1 Introduction

All VIM Modules are required to contain an Identification (ID) EEPROM with a checksum stored in the last location. When booted, the 'C6x processors check for the presence of VIM modules, through the presence bit on the VIM connector itself. If a module is present, the processor reads the module's ID EEPROM and generates a 16–bit checksum from the results of the readout. There are three conditions for the checksum; Valid Checksum (**0x00EE C0DE**), Bad Checksum (**0x000B ADC5**), and No VIM Module Installed (**0xFFFF FFFF**). All checksums are placed in Global SRAM at the following locations:

'C6x Processor	Global SRAM Location
Processor A	**0x0000 0900**
Processor B	**0x0000 1900**
Processor C	**0x0000 2900**
Processor D	**0x0000 3900**

If the generated checksum does not match the stored value, the processor lights its red LED, and places **BADC5** in Global SRAM. Even though the processor illuminates LED 0, the red LED, the processor is fully functional.

The bitwise layout of this register is defined in Table E–1, below.

Table E–1: VIM ID EEPROM Register – R/W @ VIM Address 0x0032 0000

Bit #	D31 – D4	D3	D2	D1	D0
Bit Name	Reserved	EEPROM_ Chip_Select	EEPROM_ Data_Out	Reserved	EEPROM_Clock
Access	Read/Write	Read/Write	Read Only	Read/Write	Read/Write
Function	Mask when reading	1 = Selected 0 = Not Selected	Stored Data	Mask when reading	Toggle to pluse Clock line

E.2 EEPROM Format Example

Shown on the next page is the contents of an EEPROM, the example shows the Pentek Model 6216, and an explanation of what each word is used for.

E.2 EEPROM Format Example (continued)

Table E–2: EEPROM Example (Model 6216 shown)			
Global SRAM Locations	**EEPROM Word Location**	**Contents**	**Comments**
0x0000 z900	00/01	0x00EE C0DE	Valid data flag
0x0000 z904	02/03	0x6216 0000	Model, Model Extension – Extension field is currently unused.
0x0000 z908	04/05	0x0354 2001	PCB number. This is taken from the VIM board.
0x0000 z90C	06/07	0x0001 FFFF	Assembly Rev, Option #1 – Rev A = 1, B=2, etc. space is allocated for up to 9 installed options.
0x0000 z910	08/09	0xFFFF FFFF	Option #2, Option #3 – When there are no options, **F** appears in the entire field.
0x0000 z914	10/11	0xFFFF FFFF	Option #4, Option #5
0x0000 z918	12/13	0xFFFF FFFF	Option #6, Option #7
0x0000 z91C	14/15	0xFFFF FFFF	Option #8, Option #9
0x0000 z920	16/17	0xFFFF FFFF	Module Specific Code goes in locations 16 through 61.
0x0000 z924	18/19	0xFFFF FFFF	
0x0000 z928	20/21	0xFFFF FFFF	
0x0000 z92C	22/23	0xFFFF FFFF	
0x0000 z930	24/25	0xFFFF FFFF	
0x0000 z934	26/27	0xFFFF FFFF	
0x0000 z938	28/29	0xFFFF FFFF	
0x0000 z93C	30/31	0xFFFF FFFF	
0x0000 z940	32/33	0xFFFF FFFF	
0x0000 z944	34/35	0xFFFF FFFF	
0x0000 z948	36/37	0xFFFF FFFF	
0x0000 z94C	38/39	0xFFFF FFFF	
0x0000 z950	40/41	0xFFFF FFFF	
0x0000 z954	42/43	0xFFFF FFFF	
0x0000 z958	44/45	0xFFFF FFFF	
0x0000 z95C	46/47	0xFFFF FFFF	
0x0000 z960	48/49	0xFFFF FFFF	
0x0000 z964	50/51	0xFFFF FFFF	
0x0000 z968	52/53	0xFFFF FFFF	
0x0000 z96C	54/55	0xFFFF FFFF	
0x0000 z970	56/57	0xFFFF FFFF	
0x0000 z974	58/59	0xFFFF FFFF	
0x0000 z978	60/61	0xFFFF FFFF	
0x0000 z97C	62/63	0x0000 xxxx	Word 62 should always be cleared (**0000**). Word 63 contains the byte summation of words 0 – 61.
NOTE: z = **0** for Processor A, **1** for Processor B, **2** for Processor C, and **3** for Processor D.			

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