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OPERATING MANUAL

MODEL 6229

Dual Digital Upconverter
and D/A Converter VIM-2 Module
for Pentek VIM Motherboards

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Model 6229 Operating Manual – Revision History

Date	Rev	Applicable Serial #'s	Comments
1/30/00	Preliminary	0004001 – Forward	Initial release.
5/19/00	Preliminary	0004001 – Forward	Sect. 1.7, Added additional information on 50 ohm option and updated previous information. Sect. 3.4.5, Added information on clearing the BIFO_Mode bit. Sect. 2.3.2, added information about using the Sync Bus connector with models 6210 & 6216. Changed Table 3–9, added Bit D–6; BIFO Data Read Mode. Added Sect. 3.8.1, BIFO Data Read Mode – D6. Sect. 3.8.2, added information that is dependent on the settings of the BIFO Data Read Mode bit. Added Chapter 4, The AD8320 Digitally Controlled Variable Gain Line Driver.
7/10/00	A	0004001 – Forward	Updated specifications
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12/29/03	B.3	0004001 – Forward	Sect. 1.1 and 1.2, added Pentek Model 4205. Chapter 3, added Pentek Model 4205 addressing.

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Chapter 1: Overview

1.1 General Description

Model 6229 is a VIM−2 module which attaches directly to a VIM−compatible processor baseboard, such as Pentek Models 4290, 4291, 4292, 4294, 4295, and 4205. The Model 6229 contains two complete channels of interpolation and frequency translation suitable for linking a DSP system to a radio transmitter.

Applications include generation of communication and radar test signals, electronic countermeasures, and implementation of transmit functions for advanced software radio communications systems.

1.2 Features

- ❑ VIM−2 module for VIM baseboards including Pentek's Models 4290, 4291, 4292, 4294, 4295, and 4205.
- ❑ Translates digital signals to HF or IF frequencies as high as 80 MHz
- ❑ Provides two identical, independent channels
- ❑ Interpolation filter, complex digital mixer, and programmable digital local oscillator
- ❑ 12−bit 200 MHz D/A covers DC to 80 MHz output range
- ❑ Lowpass output filters for baseband or IF analog outputs
- ❑ Synthesized signal generator mode
- ❑ Synchronization across multiple modules

1.3 Digital Upconverter

Both channels use the AD9856 Quadrature Digital Upconverter which includes halfband and CIC interpolation filters, a programmable local oscillator, a complex mixer, and a 12−bit D/A converter.

An on−chip multiplier accepts a reference clock from 5 to 50 MHz and multiplies it to create a 200 MHz internal sampling clock. The reference clock can be driven from a local 50 MHz crystal oscillator or from an external input reference. A front panel ribbon cable allows multiple slave 6229s to be driven from a single designated master 6229.

Three halfband interpolation filters upsample the baseband input by either 4x or 8x. Additional upsampling is performed by a CIC filter which interpolates by x2 to x63 in steps of 1, providing an overall interpolation range from x8 to x504.

1.3 Digital Upconverter (continued)

Complex local oscillator samples are generated by a direct digital frequency synthesizer, programmed with 32−bit resolution to cover an L.O. range from DC to 80 MHz.

The translated single sideband signal, now sampled at 200 MHz, is fed into an on−chip 12−bit D/A converter, capable of producing analog output signals anywhere within the DC to 80 MHz range. An optional inverse sinx/x filter can be inserted in the signal path prior to the D/A to compensate for its zero−order hold frequency response.

1.4 Oversampled D/A Converter

For applications requiring a non−translated baseband D/A output, samples from the VIM processor board can be upsampled with no frequency translation and then sent to the D/A converter. This minimizes the complexity of an output smoothing filter.

1.5 VIM Interface

Complex baseband samples generated by the baseboard processor are sent into the 6229 through the 32−bit parallel Bi−Directional FIFO (BIFO) path. Data may be packed with both I and Q components in a single 32−bit word for more efficient transfers.

1.6 Block Diagram

The block diagram of Pentek's Model 6229 Dual–Channel Quadrature Upconverter and D/A Converter is presented below.

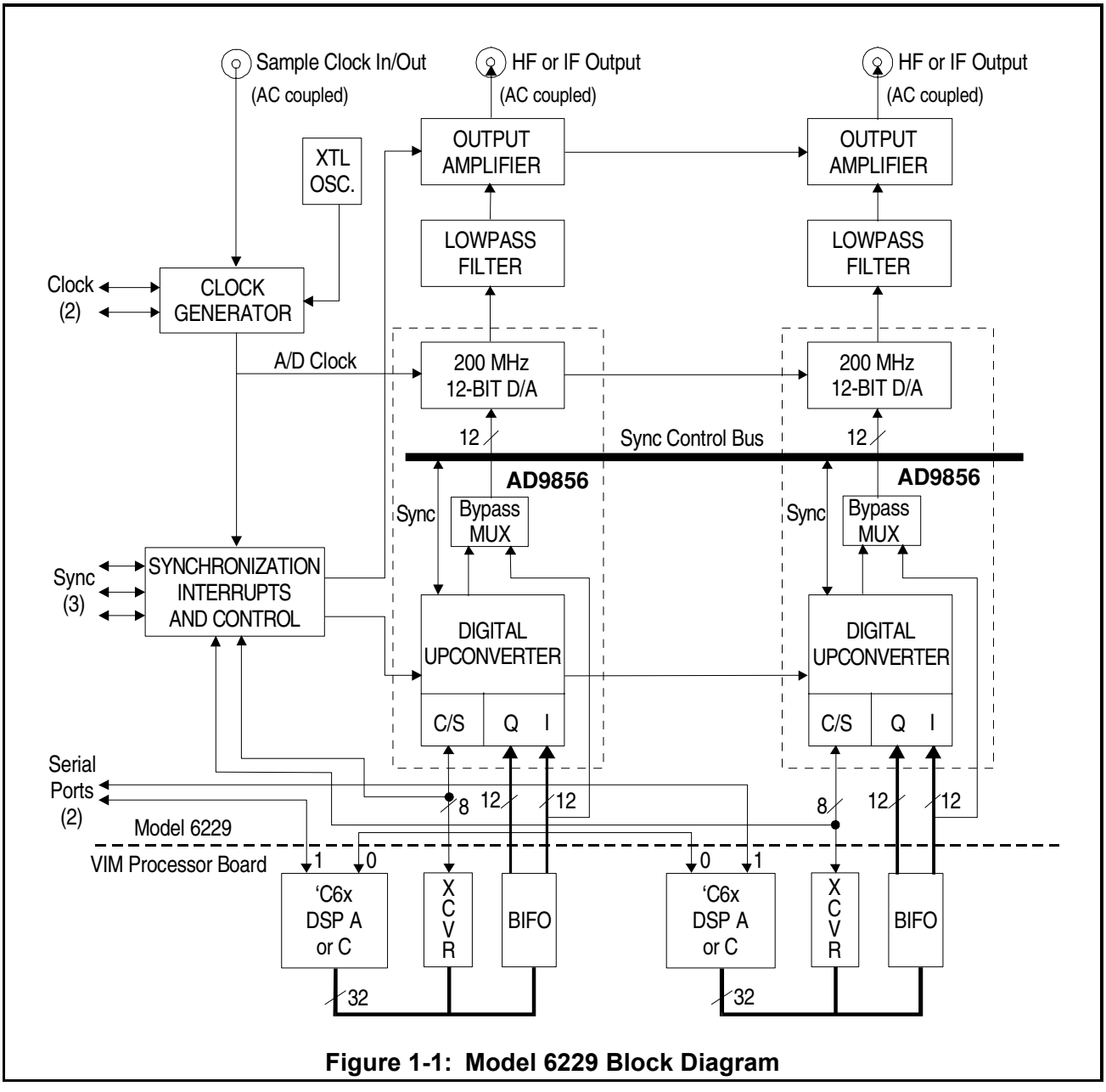


Figure 1-1: Model 6229 Block Diagram

1.7 Specifications

The specifications below are typical of the standard Model 6229 at 25°C ambient temperature, with +5 V_{DC} and +12 V_{DC} power supplies within ±1% of nominal and 50 Ω output loads, unless otherwise specified.

Input Channels

Quantity: 2

Input Logic Levels: TTL

Input Data Format: 32–bit parallel data stream from VIM baseboard. Each longword may contain one or two signed, 12–bit, 2's compliment Real only or I/Q samples.

Digital Upconverter: Analog Devices AD9856
(Data Sheet provided as Appendix A)

Reference Clock

Source: Selectable

Internal: 50 MHz crystal oscillator (100 ppm)

External: Front Panel Connector

Type: SMA

Input Impedance: 50 Ω

Coupling: AC

Maximum Amplitude: TTL or 1 – 3 V_{P-P} sine source
(Pentek recommends using a sine source as an external clock source. Small amounts of jitter associated with some TTL clock generators have been shown to cause locking problems with the AD9856 PLL circuit, which may results in CIC filter unrecoverable overflow errors. See Section 2.2.3.)

Frequency Range: 5 – 50 MHz

Duty Cycle: 45 – 55%, nominal 50%

Divider: Either of the above signals may be divided by 1, or by even integers up to 256; divider output must be ≥ 5 MHz

Maximum REFCLK Rate: 50 MHz

Multiplier disabled: 50 MHz

x4 Multiplier: 50 MHz

x20 Multiplier: 10 MHz

Minimum REFCLK Rate: 5 MHz

Maximum Input Word Rate: 50 MHz (see **Appendix A**)

1.7 Specifications (continued)

Analog Outputs

Quantity: 2

Connector Type: SMA

Output Impedance: 75 Ω (Standard)
50 Ω (Option 050)

Output Coupling:

Type: AC

Rolloff: 3 dB down @ 7 KHz

Maximum Output Amplitude (w/50Ω Load)**:**
(SIN X/X compensation bypassed, see Appendix A)

Single Tone Mode: 4.00 V_{p-p} (Standard)
1.70 V_{p-p} (Option 050)

Complex Quadrature Modulation Mode: 2.00 V_{p-p} (Standard)
0.85 V_{p-p} (Option 050)

Output Range:

Spur Free Dynamic Range: 55 dB

Harmonic Distortion @20 MHz: −60 dB

Delay Mismatch Between Channels: ±5 nsec maximum

Sample Clock: Multipin connector (programmable as input or output – differential LVDS compatible only) and one SMA connector (input only – TTL or Sine)

Sync: Multipin connector (programmable as input or output – differential LVDS compatible only) and one TTL input

Baseboard Functions: Provides access to VIM baseboard XDS connector and status LEDs

VIM Processor Reset: Front panel control and VIM reset signal (must be held for 4 x Front Panel clock speed)

1.7 Specifications (continued)

D/A Output Characteristics

Resolution:	12 bits
Error:	±10% FS
Differential Nonlinearity:	0.5 LSB
Integral Nonlinearity:	1 LSB

Output Anti−Aliasing Filter

Type:	Elliptical, Low−pass, 7−pole
Passband Ripple:	±3dB
Passband:	80 MHz
Stopband:	120 MHz
Stopband Attenuation:	60 dB minimum

Power Requirements

+5 V_{DC}

Minimum (idle):	152 mA
Maximum (loaded):	1230 mA

+12 V_{DC}

Minimum (idle):	50 mA
Maximum (loaded):	180 mA

Module Dimensions

Height:	114.3 mm (4.50 in.)
Depth:	82.5 mm (3.25 in.)
Width:	20.3 mm (0.80 in.)

Environmental

Operating Temperature:	0° to 50°C
Storage Temperature:	−20° to 90°C
Relative Humidity:	95% non−condensing
VME Rack Exhaust Temp:	0° to 50°C

Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If any damage is discovered, contact Pentek immediately at (201) 818–5900. Please save the original shipping container and packing material in case reshipment is required. The component and solder sides of the board are illustrated in Figure 2–2, on the next page.

2.2 Model 6229 Front Panel

The Model 6229's front panel is shown in the figure at the right. If only one VIM mezzanine board is installed, the other gap in the baseboard's front panel should be covered by a blank panel supplied with the baseboard.

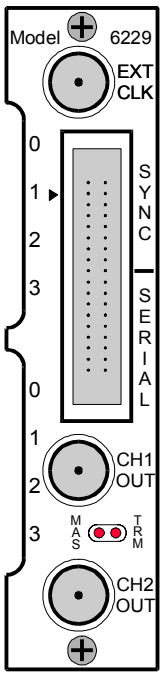


Figure 2-1: Model 6229 - Front Panel

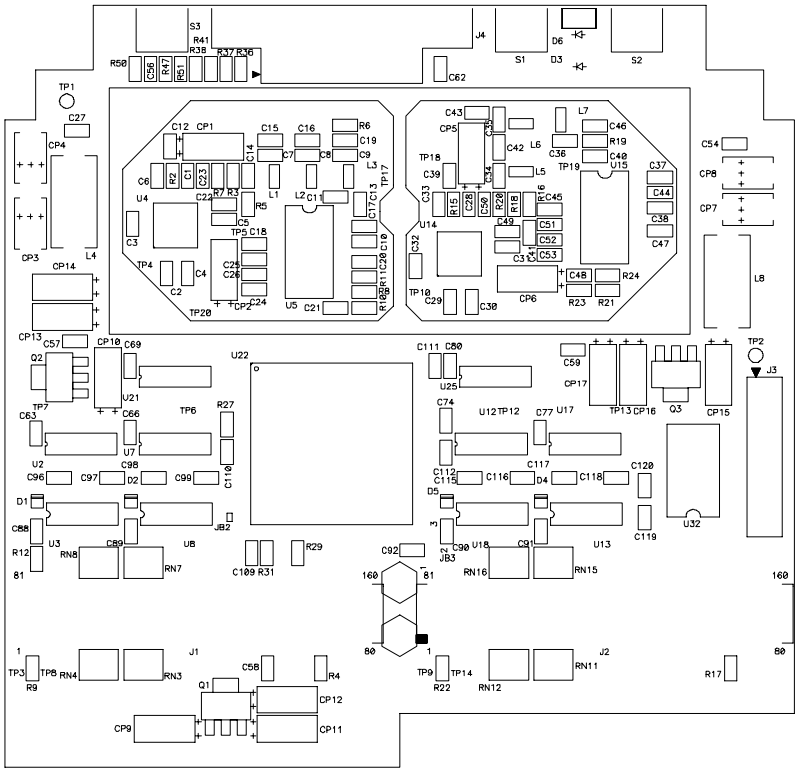
2.2.1 Front Panel LEDs

There are two red LEDs on the front panel of the Model 6229, labeled **MAS** and **TRM**. When the 6229 provides the master sync signals (this function is enabled by bit D0 in the Master Control Register, see Section 3.4.8) the MAS LED illuminates. When the 6229 is the last slave unit in a chain (or the only slave unit) sync termination must be activated using bit D1 in the Master Control Register (see Section 3.4.7). Enabling sync termination illuminates the TRM LED.

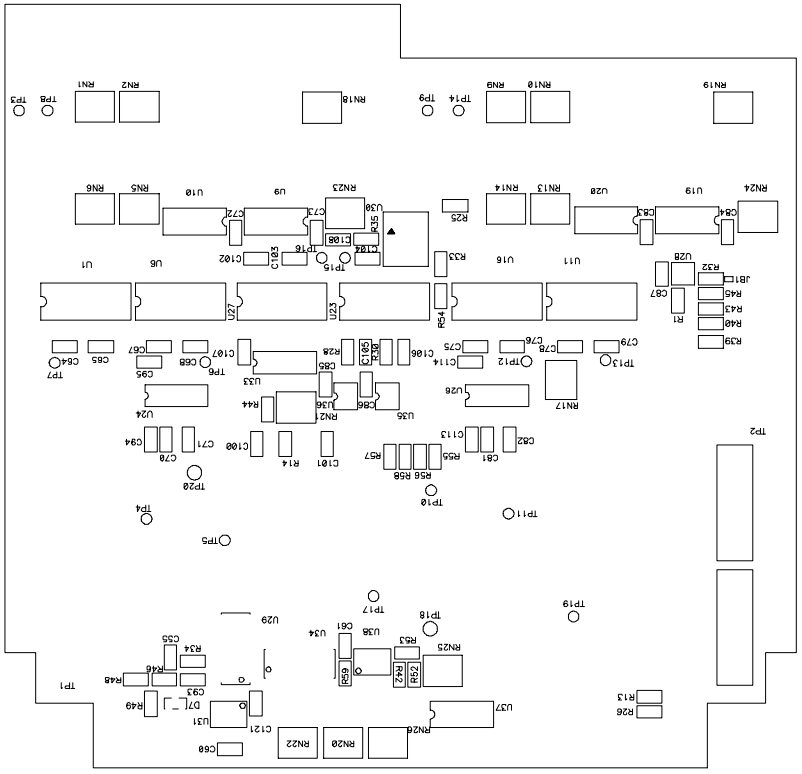
2.2.2 Analog Output Connectors

The front panel has two threaded, coaxial SMA connectors for analog signal outputs (labeled **CH1 OUT** and **CH2 OUT**), one for each D/A output channel. Each output is AC coupled, with 75 Ω output impedance. With Option 050, this output impedance is 50 Ω.

The maximum output amplitude (w/50Ω Load) in Single Tone Mode is 4.00 V_{p-p} (Standard) or 1.70 V_{p-p} (Option 050); in Complex Quadrature Modulation Mode the maximum amplitude is 2.00 V_{p-p} (Standard) or 0.85 V_{p-p} (Option 050). See Section 1.7 for further description of the analog output specifications.



(a) Component Side



(b) Solder Side

Figure 2-2: Model 6229 PC Board

2.2 Model 6229 Front Panel (continued)

2.2.3 External Clock Input Connector

An **EXT CLK** SMA connector is provided at the top of the Model 6229 front panel (see Figure 2–1, Section 2.2) for an external clock input. A TTL level with a 45% to 55% duty cycle or a 1 – 3 V_{P-P} sine signal may be used as an external clock source.

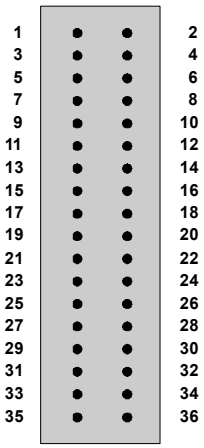
It is important that the clock source is stable and continuous, and that the external clock source is selected on the Model 6229 (see Section 3.4.6) prior to initializing the AD 9856 upconverters, or unrecoverable overflow errors may occur in the AD9856 CIC filters. This condition compromises the validity of the analog output signal, and is not recoverable without a reset and reinitialization of the AD9856. An external clock source with a duty cycle outside the 45 – 55% range, or changing the frequency of the external clock source once in operation, may also cause this condition to occur.

2.3 Sync Bus / Serial I/O Connector

Accessible through the Model 6229 front panel is a 36–pin serial connector (3M part #81036–500203, Pentek part # 354.03610). Included on this connector are signals used for synchronizing multiple units, four profile select pins, and VIM baseboard's serial port signals. The following table contains the pinouts and description of this connector.

Table 2-1: Model 6229 - Sync Bus / Serial I/O Pinouts

Pin	Signal		Pin	Signal
1	Ground		2	MCLKIN
3	$\overline{\text{MCLKIN}}$		4	Ground
5	GSYNC		6	$\overline{\text{GSYNC}}$
7	SSYNC		8	$\overline{\text{SSYNC}}$
9	ASYNC		10	$\overline{\text{ASYNC}}$
11	Ground		12	Reserved - N/C
13	Reserved - N/C		14	Ground
15	$\overline{\text{TTL-SYNC}}$		16	Ground
17	P0-CLKR1		18	Ground
19	P0-FSR1		20	P0-DR1
21	P0-CLKS1		22	Ch1-XPS0
23	P0-CLKX1		24	Ch1-XPS1
25	P0-FSX1		26	P0-DX1
27	P1-CLKR1		28	Ground
29	P1-FS1		30	P1-DR1
31	P1-CLKS1		32	Ch2-XPS0
33	P1-CLKX1		34	Ch2-XPS1
35	P1-FSX1		36	P1-DX1



2.3 Sync Bus / Serial I/O Connector (continued)

2.3.1 Signals for Synchronizing Multiple Boards

The following LVDS (Low−Voltage Differential Signaling) signals make up the Sync Bus, which can be used to synchronize the operation of multiple VIM modules: MCLKIN, GSYNC, SSYNC, and ASYNC. The subsections below describe each of these signals.

2.3.1.1 MCLKIN, $\overline{\text{MCLKIN}}$

This signal is the reference clock. When the Model 6229 is configured as a master, this is an LVDS output at the reference clock rate. If the board is configured for an external clock, then the original source for this signal is the EXT CLK SMA input connector (see Section 2.2.3). Otherwise, an on−board 50 MHz crystal oscillator is used as the fre−quency source. The frequency of MCLKIN is equal to the external or crystal frequency divided by the contents of the Reference Clock Divider register (see Section 3.5).

When configured as a slave, this signal is a differential LDVS input and will be used as the board's reference clock instead of the board's own external clock input or on−board oscillator. This is how several boards are able to sample synchronously from the same reference clock source.

2.3.1.2 GSYNC, $\overline{\text{GSYNC}}$

This LVDS signal is not used by slave Model 6229s on the Sync Bus. It can, however, be generated by a Model 6229 configured as a Sync Bus master, or it can be masked off. This signal would be used only by a Model 6216 configured as a Sync Bus slave, to synchronously change the gain setting of that device's GC1012A Digital Drop Receiver.

2.3.1.3 SSYNC, $\overline{\text{SSYNC}}$

This LVDS signal can be used to synchronize several functions across multiple VIM boards and channels. On the Model 6229, the SSYNC pulse can be enabled to synchronously reset the base−board BIFO (see Section 3.4.5), the BIFO Read Rate Divider (see Section 3.7.4), and the AD9856 (see Section 3.8.6). It can also be used to synchronize changes in upconverter profile selections (see Section 3.8.4).

If the Model 6229 is configured as a Sync Bus master, this is an LVDS output. If the Model 6229 is configured as a Sync Bus slave, this is an LVDS input.

2.3 Sync Bus / Serial I/O Connector (continued)

2.3.1 Signals for Synchronizing Multiple Boards (continued)

2.3.1.4 ASYNC, $\overline{\text{ASYNC}}$

This LVDS signal is not used by slave Model 6229s on the Sync Bus. It can, however, be generated by a Model 6229 configured as a Sync Bus master, or it can be masked off. This signal would be used only by a Model 6216 configured as a Sync Bus slave, to synchronously change the tuning frequency and/or clear the frequency accumulator of that device's GC1012A Digital Drop Receiver.

2.3.2 External Synchronization – $\overline{\text{TTL–SYNC}}$

This signal allows the user to apply an external signal to generate sync signals on all unmasked outputs (see Section 3.10). The signal is a single–ended TTL–compatible sync input. In Master units, on–card Sync signals will be created on the rising edge of this signal. If left unconnected, it is a logic high.

2.3.3 External Profile Selection – ChN–XPS0 and ChN–XPS1

The AD9856 DU has four groups of six internal profile registers, which allow users to store different sets of configuration settings for the device. Profiles are selected by means of two profile select pins on the device. On the Model 6229, these pins may be driven either by two bits in each channel's Channel Control Register #1 (see Section 3.7), or by the two pins assigned to that channel on the module's front panel Sync Bus connector. For further information, please refer to Sections 3.7.2 and 3.7.3.



The synchronizing functions of the Model 6229 are compatible with those of the Pentek's Model 6210 and 6216 digital receivers. However, the Sync Bus connectors on those units are not pin–to–pin compatible with the one on the 6229. Specifically, the 6210 and 6216 do not implement or support the External Profile Select functions of the Model 6229's Sync Bus connector, and that function will be disabled if a 6229's Sync Bus is connected to a 6210's or 6216's with a standard cable.

To synchronize 6229s with 6210s or 6216s without disabling the External Profile select, the Sync Bus cable must be constructed such that pins 22, 24, 32, and 34 of the 6229's connector are NOT CONNECTED to the 6210 or 6216 Sync Bus connectors.

2.3 Sync Bus / Serial I/O Connector (continued)

2.3.4 Serial Port Signals

The signals listed in the subsections below are part of the VIM baseboard's Serial Ports. If the Model 6229 is controlled by (i.e., installed over) Processors A & B, then Processor A's serial port is P0, and Processor B's serial port is P1. If the Model 6229 is under the control of Processors C & D, then Processor C's serial port is P0, and Processor D's is P1. All signals are point−to−point connections between the quickswitch and the expansion connector on the VIM baseboard.

2.3.4.1 P0−CLKR1, P1−CLKR1

This is the Serial Port Receive Clock Signal. This signal is a level translated version of the CLKR1 pin from one of the VIM baseboard's processors.

2.3.4.2 P0−FSR1, P1−FSR1

This is the Serial Port Receive Frame Sync signal. This signal is a level translated version of the FSR1 pin from one of the VIM baseboard's processors.

2.3.4.3 P0−CLKS1, P1−CLKS1

This is the Serial Port External Clock Source signal. This signal is a level translated version of the CLKS1 input to one of the VIM baseboard's processors.

2.3.4.4 P0−DR1, P1−DR1

This is the Serial Port Receive Data signal. This signal is a level translated version of the DR1 input to one of the VIM baseboard's processors.

2.3.4.5 P0−CLKX1, P1−CLKX1

This is the Serial Port Transmit Clock signal. It is a level translated version of the CLKR1 pin from one of the VIM baseboard's processors.

2.3.4.6 P0−FSX1, P1−FSX1

This is the Serial Port Transmit Frame Sync signal. It is a level translated version of the FSX1 pin from one of the VIM baseboard's processors.

2.3.4.7 P0−DX1, P1−DX1

This is the Serial Port Transmit Data signal. It is level translated version of the DX1 output from one of the VIM baseboard's processors.

2.4 Installing the Model 6229 on a VIM Baseboard

Pentek's VIM baseboards ship with two blank panels where optional VIM modules, such as the Model 6229, may be installed. This section provides directions for installing the Model 6229 VIM–2 module on a VIM–compatible baseboard

CAUTION **Perform all assembly steps at an antistatic workstation.**

Tools required for all procedures:

- ❑ #1 philips screwdriver
- ❑ flat–blade screwdriver (blade width 5/16–inch or less)

1) Remove the blank panel insert from the position on the baseboard in which your VIM module will be installed by removing the two countersunk philips screws from the top & bottom of the insert.

2) Remove the front panel from the VIM module by removing the two countersunk philips screws from the top & bottom of the panel.

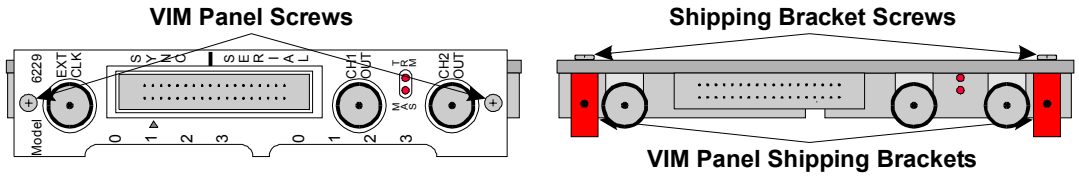


Figure 2-3: VIM Module Countersunk Screws

3) Remove the two (red) shipping brackets that were used to mount the front panel to the VIM module, by removing the two pan–head philips screws from the solder side of the VIM module (see figure above). Set these screws aside, as they are used to secure the VIM module to the VIM baseboard.

   (The panel shipping brackets may be discarded, or saved to store the panel back on the VIM module if it is removed from the VIM baseboard.)

2.4 Installing the Model 6229 on a VIM Baseboard (continued)

4) At the rear of the VIM module, on the component side, is a nylon spacer with a nylon screw threaded into it, as illustrated below. Remove the nylon screw threaded into the spacer from the component side. Set this screw aside, as it will be used when installing the VIM module on the baseboard.

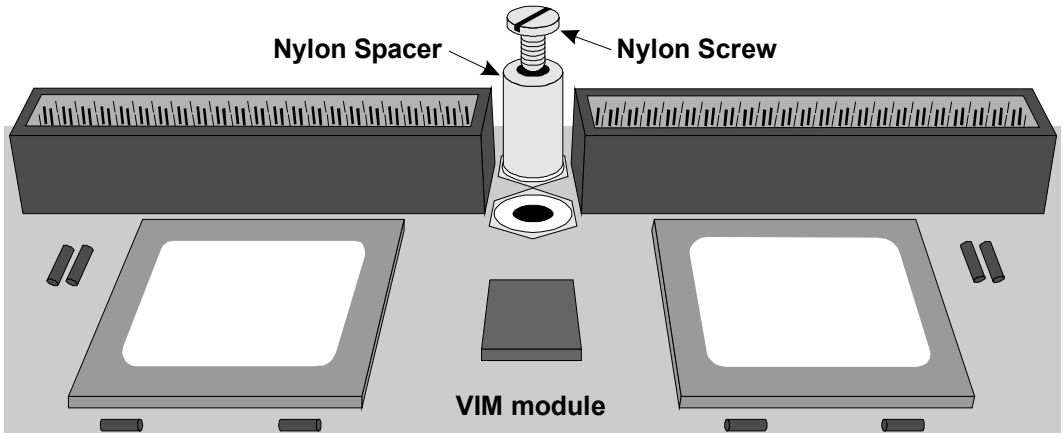


Figure 2-4: VIM Module Nylon Spacer



The spacer should be installed in the hole BEHIND the VIM connectors (i.e., farthest from the front panel's location). If the spacer is installed in the front hole, reposition it by removing the nylon screw on the SOLDER side of the VIM module, and threading it back into the spacer through the rear–most hole.

5) Remove one blank panel insert from your VIM baseboard, at the VIM position you wish to install the Model 6229 module, by removing the two countersunk Phillips screws from the panel insert (see figure below).

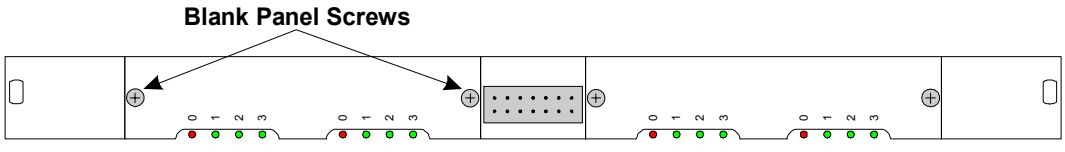


Figure 2–5: VIM Baseboard Blank Panel Screws

2.4 Installing the Model 6229 on a VIM Baseboard (continued)

6) With the VIM baseboard's component side (the one with the mezzanine connectors) up, and the connectors on the VIM module face down, align the P1 and P2 connectors on the VIM module with the pair of connectors corresponding to the desired location on the baseboard (e.g., P11 and P14 at the top of a Model 4290, or P8 and P4, at the bottom).

7) **GENTLY but firmly**, press down on the areas of the VIM module opposite both connectors, to fully seat the VIM module's connectors in the baseboard's. If you meet with significant resistance, check the connector alignment.

> **NOTE:** Misalignment can cause bent pins or break connector housings, so **NEVER APPLY EXCESSIVE FORCE**.

8) After seating the connectors, secure the front of the VIM module to the baseboard by threading two pan−head mounting screws through the holes in the front of the solder side of the VIM module into the threaded holes in baseboard's panel brackets.

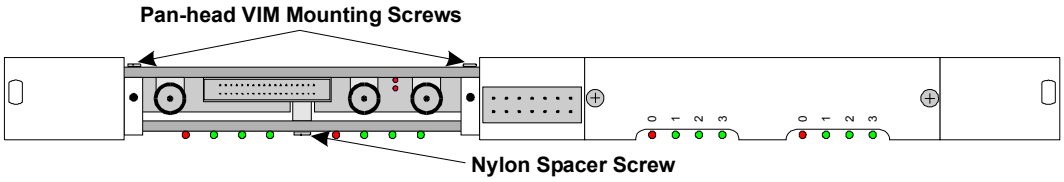


Figure 2–6: Model 6229 Mounted on VIM Baseboard
(Model 6229 illustrated in upper VIM position)

9) Turn the assembly over, such that the mezzanine board is on the work surface and the solder side of the VIM baseboard is face up.

10) Secure the rear of the VIM module to the baseboard, using the nylon screw you removed earlier, through the rear mounting hole on the baseboard, threaded into the nylon spacer on the VIM module.

11) Attach the VIM module's front panel to the baseboard using two countersunk philips screws, passed through the holes at the top and bottom of the VIM panel and threading them into the threaded holes in the baseboard's panel brackets.

12) If an additional VIM module is to be installed, repeat this procedure in the other module location on the baseboard.

2.4 Installing the Model 6229 on a VIM Baseboard (continued)

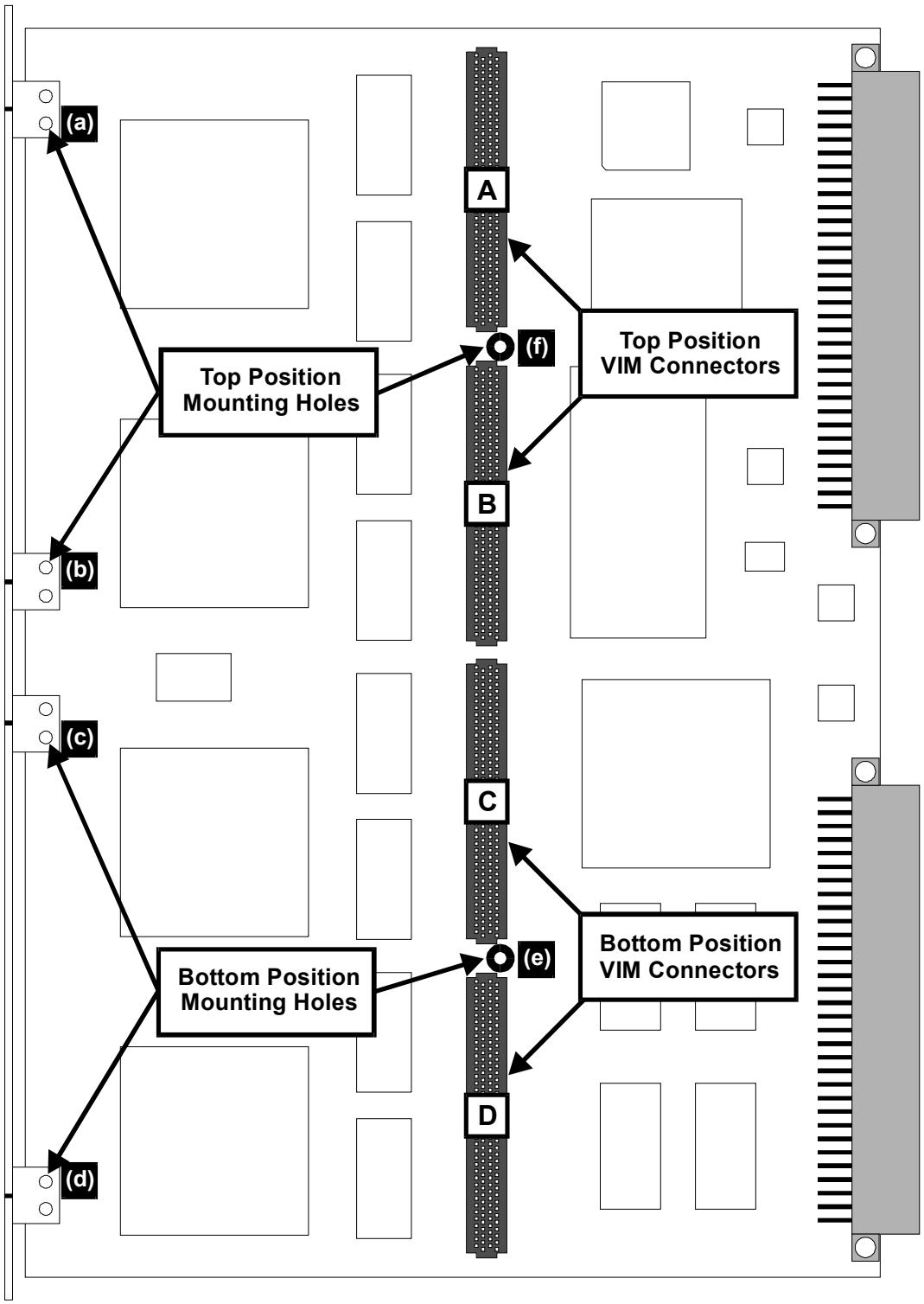


Figure 2-7: Typical VIM Baseboard - Connectors & Mounting Holes

Chapter 3: Memory Maps and Register Descriptions

3.1 Overview

This section covers access to the Model 6229 from the VIM baseboard. Memory maps to VIM module resources are given from the baseboard processor's viewpoint, and details are provided describing the use of each resource.

3.2 Model 6229 Memory Map

The two tables below provide base addresses of the Model 6229 control and status registers for each type of Pentek VIM Baseboard. Use the applicable address from these tables as the VIM registers base address ('VIMReg_base') in the following sections.

For a Pentek Model 4290 through 4295 VIM baseboard, use the VIM registers base addresses in Table 3–1, below. These baseboards have four processor nodes, one for each VIM Interface, and each node processor uses the same VIM base address to access the associated VIM module.

Table 3–1: VIM Base Addresses for Models 4290 to 4295 VIM Baseboards

VIM Baseboard	VIM Registers Base Address (VIMReg_base)
Model 4290 or 4291	0x0032 0000
Model 4292 or 4293	0x0202 0000
Model 4294 or 4295	0x1D02 0000

For a Pentek Model 4205 VIM baseboard, use the VIM registers base addresses in Table 3–2, below. The Model 4205 has a single baseboard processor, which uses a separate base address for each VIM Interface (emulating four processors). In addition, on this baseboard the VIM module registers can be accessed from the VMEbus.

Table 3–2: VIM Base Addresses for Model 4205 VIM Baseboards

VIM Site	VIM Registers Base Address (VIMReg_base)	
	Processor	VMEbus A32 Slave *
VIM A	0x4082 0000	A32VME_base + 0x00B2 0000
VIM B	0x4086 0000	A32VME_base + 0x00B6 0000
VIM C	0x408A 0000	A32VME_base + 0x00BA 0000
VIM D	0x408E 0000	A32VME_base + 0x00BE 0000

* Offsets relative to the base address 'A32VME_base' set on the Model 4205 baseboard (refer to the Model 4205 Operating Manual for these settings)

3.2 Model 6229 Memory Map (continued)

The following table provides a memory map for the Model 6229 32–bit control and status registers. All register addresses are expressed as offsets from the VIM registers base address for the applicable VIM baseboard—see Table 3–1 or Table 3–2 on the prior page for the VIM registers base address ('VIMReg_base') for your VIM baseboard. The sections following the table provide detailed information about each register.

Table 3-3: Model 6229 Memory Map

Address Offset *	Register Description	Access	Additional Information
VIMReg_base + 0x0000	ID EEPROM Readout	R. O.	Appendix C
VIMReg_base + 0x0004 to VIMReg_base + 0x001C	Reserved	N/A	N/A
VIMReg_base + 0x0020	Master Control Register **	R/W	Section 3.4
VIMReg_base + 0x0024	Reference Clock Divider **	R/W	Section 3.5
VIMReg_base + 0x0028	BIFO Read Rate Divider Low	R/W	Section 3.6
VIMReg_base + 0x002C	BIFO Read Rate Divider High	R/W	
VIMReg_base + 0x0030	Channel Control Register #1	R/W	Section 3.7
VIMReg_base + 0x0034	Channel Control Register #2	R/W	Section 3.8
VIMReg_base + 0x0038	Serial Port Enable Register	R/W	Section 3.9
VIMReg_base + 0x003C	Sync Generate Register **	R/W	Section 3.10
VIMReg_base + 0x0040	DUC Address Register	R/W	Section 3.11
VIMReg_base + 0x0044	DUC Data Register	R/W	Section 3.12
VIMReg_base + 0x0048 to VIMReg_base + 0x007C	Reserved	N/A	N/A

* VIMReg_base = see Table 3-1 or Table 3-2 on prior page.

** These registers are accessible ONLY to VIM baseboard Processors A or C, depending upon the location in which the module is installed. They do not appear in the memory maps for Processors B or D.

3.3 ID EEPROM Readout Register – R. O. @ VIMReg_base + 0x0000

The format for the code stored by Pentek in this EEPROM is listed in Appendix C of this manual. The format is provided for VIM module designers. Neither the format nor this register is intended for general use.

3.4 Master Control Register – R/W @ VIMReg_base + 0x0020

The Master Control Register allows you to configure the Model 6229 as a master or slave on the sync bus, toggle the on–board sync termination, and select the source of the clock as internal or external. Also, this register provides masks for the three Sync signals that can be generated by a 6229 configured as a Sync Bus master, and an Enable bit for the on–board oscillator. The Master Control Register is accessible only to Processor A or Processor C on the VIM baseboard, depending upon the position in which the module is installed. Neither Processor B nor Processor D on a VIM baseboard can access this register. Table 3–4, below, shows the contents of the Model 6229's Master Control Register. The subsections following the table give descriptions of the bits in this register.

Table 3-4: Model 6229 - Master Control Register
R/W @ VIMReg_base + 0x0020

Bit #	D31 - D8							
Bit Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Oscillator _Enable	GSYNC _Mask	ASYNC _Mask	SSYNC _Mask	BIFO_ Sync	Clk_Source _Select	Term_ Enable	Master/ $\overline{\text{Slave}}$
Bit Function	1 = Enable 0 = Disable	1 = Generate Signal 0 = Mask Signal			1 = Enable 0 = Disable	1 = Ext Clk 0 = Crystal	1 = Term 0 = No Term	1 = Master 0 = Slave
All bits default to the logic '0' state at power-up and reset								

3.4.1 Oscillator Enable Bit D7

This bit is used to enable the Model 6229's on–board, 50 MHz crystal oscillator if it is used as a stand–alone device (or as a Sync Bus master) without an external clock source. The oscillator is enabled by setting this bit to the logic '1' state. By default, this bit is initialized to the logic '0' state, which disables the on–card oscillator. This allows the Model 6229 to be used with an external clock source or as a Sync Bus slave, without an on–board RF source that could otherwise add interference to the output signal.

3.4.2 GSYNC Mask Bit D6

This bit is used to allow a Model 6229 that is configured as a Sync Bus master to generate a GSYNC signal. The GSYNC can be used to synchronously change the gain setting on a Model 6216 configured as a Sync Bus slave. Generation of GSYNC is enabled when this bit is set to the logic '1' state.

If there is no Model 6216 slave on a given 6229 master's Sync Bus (or if there is no need to change that device's gain setting), this bit should be cleared to the logic '0' state, which is its default condition. This signal is unused on the Model 6229, whether it is a master or a slave.

3.4 Master Control Register (continued)

3.4.3 ASYNC Mask Bit D5

This bit is used to allow a Model 6229 that is configured as a Sync Bus master to generate an ASYNC signal. The ASYNC can be used to synchronously change the tuning frequency and/or clear the frequency accumulator on a Model 6216 configured as a Sync Bus slave. Generation of ASYNC is enabled when this bit is set to the logic '1' state.

If there is no Model 6216 slave on a given 6229 master's Sync Bus (or if there is no need to change that device's frequency setting), this bit should be cleared to the logic '0' state, which is its default condition. This signal is unused on the Model 6229, whether it is a master or a slave.

3.4.4 SSYNC Mask Bit D4

This bit is used to allow a Model 6229 that is configured as a Sync Bus master to generate an SSYNC signal. The SSYNC is be used to synchronize the VIM baseboard's mezzanine interface BIFOs and the BIFO access rate dividers for multiple channels and boards. Generation of SSYNC is enabled when this bit is set to the logic '1' state.

If this board is not a Sync Bus master, this bit should be cleared to the logic '0' state, to disable the generation of SSYNC.



1) For a Model 6229 that is not connected to a Sync Bus, all three of the above bits (D4 : D6) should be cleared to logic '0'. Also note that none of these three bits can be used to actually fire any of the associated Sync signals. That function is performed by the Sync Generate Register (see Section 3.10).

2) When in Sync mode, write the data to the BIFO as fast as possible after the Outgoing Almost Empty condition is true and adjust the BIFO Outgoing Almost Empty condition to a larger threshold number.

3.4 Master Control Register (continued)

3.4.5 BIFO Sync Bit D3

This bit is used to synchronize the mezzanine BIFOs on VIM baseboards across multiple channels. This is accomplished by first clearing this bit to logic '0' on each channel to be synchronized, then resetting the baseboard's BIFO. When this bit is subsequently set to logic '1', no data is read from the BIFO until the next rising edge of an SSYNC signal (see Sections 3.4.4, above, and 2.3.1.3, on page 16). In this manner, data acquisition in all channels connected to the Sync Bus is started simultaneously.

When the BIFO_Mode bit (D6 in Channel Control Register #2, Section 3.8) is cleared to the logic '0' state (for synchronous BIFO read enables) this bit must be set to the logic '1' state. Note, this only has an effect if the BIFO mode bit is cleared to a '0' for synchronous BIFO read enables, and the BIFO_Enable bit (D5 in Channel Control Register #2, Section 3.8) must be set to a '1'. Also the BIFO read enable will not be activated by this method if the BIFO is empty. The read enable will also terminate if the BIFO goes empty at any point after acquisition begins and will have to be retriggered by another SSYNC signal to resume because synchronization is lost once the BIFO goes empty.

3.4.6 Clock Source Select Bit D2

This bit determines which signal will drive the Model 6229's Reference Clock Divider (see Section 3.5). When this bit is set to the logic '1' state, the signal applied to the front panel EXT CLK connector is selected. When this bit is cleared to the logic '0' state, the on−board, 50 MHz crystal oscillator is selected.

3.4.7 Termination Enable Bit D1

This bit is set to the logic '1' state to connect termination resistors to the Model 6229's Sync Bus. This should be done ONLY on the slave Model 6229 that is at the opposite end of the Sync Bus from the Sync Bus master, or on a stand−alone device that is not connected to the external Sync Bus. On all other devices, clear this bit to the logic '0' state, to disconnect the terminators.

3.4.8 Master / Slave Bit D0

Set this bit to the logic '1' state to configure a Model 6229 as a Sync Bus master. This bit must also be set to the logic '1' state on any Model 6229 that will not be connected to a Sync Bus. To configure a Model 6229 as a Sync Bus slave, clear this bit to the logic '0' state.

3.5 Reference Clock Divider – R/W @ VIMReg_base + 0x0024

The Reference Clock Divider Register divides the master clock signal (provided by the on–card, 50 MHz oscillator or the front panel EXT CLK connector, see Section 3.4.6) by the quantity written to the lower byte (D7 – D0) of this register, plus one. This register should ONLY be written with all zeros or odd numbers, such that the actual number that the master clock frequency is divided by is either 1 or an even number. The output of this divider is applied to the REFCLK input of the AD9856 DUC. The formulas used to determine the value for REFCLK are shown below.

Onboard Oscillator Selected:

$$REFCLK = \frac{50MHz}{DIV0 + 1}$$

External Clock Selected:

$$REFCLK = \frac{EXTERNAL\ CLOCK}{DIV0 + 1}$$

Where DIV0 is the value in the Reference Clock Divider Register, and is 0 or an odd number up to 9.

For example, when the low byte of this register contains all zeros (their default condi–tion), the master clock signal will be passed to the DUC's REFCLK input unaltered (i.e., divided by 1). However, if the internal oscillator is selected, and the low byte of this register contains the quantity 9, the DUC's REFCLK frequency will be 5 MHz (i.e., 50 MHz divided by (9+1)).

Like the Master Control Register, the Reference Clock Divider is only accessible from Processor A or Processor C on the VIM baseboard, depending upon the position in which the module is installed. Neither Processor B nor Processor D on a VIM base–board can ever access this register. Table 3–5, below, illustrates the contents of the Model 6229's Reference Clock Divider Register.

Table 3-5: Model 6229 - Reference Clock Divider
R/W @ VIMReg_base + 0x0024

Bit #	D31 - D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB---------------------------------------LSB							
Function	Master Clock is divided by the quantity in this field +1 to produce the Reference clock for the DUC. This field MUST be written with either an odd number, or zero.							
All bits default to the logic '0' state at power-up and reset								

3.6 BIFO Read Rate Dividers – R/W @ VIMReg_base + 0x0032 0028 (Low) & 0x0032 002C (High)

The Reference Clock, described in Section 3.5, on the previous page, may be further divided to create the Read Enable signal for the VIM baseboard's mezzanine BIFO. There are 12 bits provided for this frequency division, spread across these two registers. Each channel (i.e., each processor on the baseboard that can access this module) has its own unique version of this register pair, to allow the two channels to operate at different rates. The lower eight bits of the divider are bits D7 – D0 at VIMReg_base + 0x0028 (referred to in the Memory Map as BIFO Read Rate Divider Low), and the upper four bits are D3 – D0 at VIMReg_base + 0x002C (BIFO Read Rate Divider High). This divider works in a manner similar to the Reference Clock Divider. The BIFO Read Rate is equal to the Reference Clock rate divided by the 12–bit value in these registers plus one. Also, the valid data values for this 12–bit field are restricted to odd numbers (which will result in even divisors) and zero (which gives a divisor of one). Table 3–6, below, shows the locations of the 12 bits that comprise this divisor.

Table 3-6: Model 6229 - Baseboard BIFO Read Rate Dividers								
BIFO Read Rate Divider: High Bits - R/W @ VIMReg_base + 002C								
Bit #	**D31 - D8**							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	Not Used				MSB - - - - - - - - - - - - - - - - ->			
Function	Write with 0's, Mask when Reading				4 MSBs of 12-bit divisor			
BIFO Read Rate Divider: Low Bits - R/W @ VIMReg_base + 0028								
Bit #	**D31 - D8**							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	>- -LSB							
Function	8 LSBs of 12-bit divisor							
The Reference Clock is divided by the quantity in this 12-bit field +1 to produce the Read Enable for the Baseboard's BIFO. This 12-bit field MUST be written with either an odd number, or zero. All bits default to the logic '0' state at power-up and reset								

3.6 BIFO Read Rate Dividers (continued)

The formula used to determine the value for the BIFO Read Rate is shown below.

$$\text{BIFO READ RATE} = \frac{\text{REFCLOCK}}{\text{DIV1} + 1}$$

In addition, the following formulas show the relationship between the BIFO Read Rate and the upconverter parameters.

I/Q Unpacked Mode: $$\text{REFCLOCK} = \frac{2\text{HN(BIFOREADRATE)}}{\text{MI}}$$

I/Q Packed Mode: $$\text{REFCLOCK} = \frac{4\text{HN(BIFOREADRATE)}}{\text{MI}}$$

Real Unpacked Mode: $$\text{REFCLOCK} = \frac{4\text{HN(BIFOREADRATE)}}{\text{MI}}$$

Real Packed Mode: $$\text{REFCLOCK} = \frac{4\text{HN(BIFOREADRATE)}}{\text{MI}}$$

Where:
H is 1, if Halfband Filter #3 is bypassed,
H is 2, if Halfband Filter #3 is enabled,
M is 1, if the Refclk Multiplier is bypassed,
M is the set value if the Refclk Multiplier is enabled ($4 \le M \le 20$),
I is 1 (Full Word Input),
N is the CIC interpolation rate ($1 \le N \le 63$).

3.7 Channel Control Register #1 – R/W @ VIMReg_base + 0x0030

Each upconverter channel on the Model 6229 (i.e., each processor on the baseboard that can access this module) has its own unique version of this register. The register contains bits to select a channel's input data format, to control the selection of a group of profile registers within a given DUC chip, to enable synchronous reset of a channel's BIFO Read Rate divider, To enable a channel's output amplifier, and to determine the location of the 12–bit data samples in a given channel's 32–bit input longword. The contents of the Model 6229's Channel Control Register #1 is summarized in Table 3–7, below. The subsections that begin below the table provide further detail about the usage of this register's bits.

Table 3-7: Model 6229 - Channel Control Register #1
R/W @ VIMReg_base + 0x0030

Bit #	D31 - D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	Format_ Select_1	Format_ Select_0	Ext_Profile_ Select_Enable	Profile_ Select_1	Profile_ Select_0	BIFO_Divider_ Sync_Rst_En	O/P_Amp _Enable	Data_ Position
Function	1,1 = Unpack, I 1,0 = Pack, I	0,1 = Unpack, IQ 0,0 = Pack, IQ	1 = Enable 0 = Disable	1,1 = Profile 4 1,0 = Profile 3	0,1 = Profile 2 0,0 = Profile 1	1 = Enable 0 = Disable		1 = High Word 0 = Low Word
All bits default to the logic '0' state at power-up and reset								

3.7.1 Format Selection D7 & D6

These two bits select among the four input data formats that can be accepted by the Model 6229.

The state of D7 determines whether the model 6229 will accept Complex or Real–only data. When D7 is set to the logic '1' state, the Model 6229 is configured to accept Real (In–phase or I) data only. The Model 6229 is configured to accept Complex data (In–phase and Quadrature, or I and Q) data when D7 is cleared to the logic '0' state.

The state of D6 determines whether or not the Model 6229 accepts packed data (two 12–bit samples per 32–bit input longword). When D6 is set to the logic '1' state, the Model 6229 is configured to accept unpacked data (one 12–bit sample in each 32–bit input longword). The Model 6229 is configured to accept packed data when D6 is cleared to the logic '0' state. These data formats are illustrated in Table 3–8, on the next page.

3.7 Channel Control Register #1 (continued)

3.7.1 Format Selection (continued)

In the unpacked, complex data format, It is necessary to identify a given sample as real or imaginary. In these formats, the least significant bit is used as a Tag. Setting the Tag bit to the logic '1' state identifies a given sample as Real data. Quadrature or imaginary data is identified by the presence of a logic '0' in the LSB. Note that the Real data tag is only required on the first real sample, but it is good practice to tag all real samples in this format.

An additional variable to consider in the formatting of unpacked input samples is the location of the single sample in the longword. This is controlled by the D0 bit in this register, described in Section 3.7.6. The effect of this bit is also illustrated in Table 3–8, below.

Table 3-8: Model 6229 - Input Data Formats

Packed I/Q Format - D7 = 0, D6 = 0				
Samples	**D31 - D20**	**D19 - D16**	**D15 - D4**	**D3 - D0**
All	12-bit Q Sample	—	12-bit I Sample	—

Unpacked I/Q Format - D7 = 0, D6 = 1, D0 = 0 (Low Word)				
Samples	**D31 - D16**	**D15 - D4**	**D3 - D1**	**D0**
Odd	—	12-bit I Sample	—	1
Even	—	12-bit Q Sample	—	0

Unpacked I/Q Format - D7 = 0, D6 = 1, D0 = 1 (High Word)				
Samples	**D31 - D20**	**D19 - D16**	**D15 - D1**	**D0**
Odd	12-bit I Sample	—	—	1
Even	12-bit Q Sample	—	—	0

Packed, Real-Only Data - D7 = 1, D6 = 0				
Samples	**D31 - D20**	**D19 - D16**	**D15 - D4**	**D3 - D0**
All	12-bit I Sample (t)	—	12-bit I Sample (t-1)	—

Unpacked Real-Only Data - D7 = 1, D6 = 1, D0 = 0 (Low Word)			
Samples	**D31 - D16**	**D15 - D4**	**D3 - D0**
All	—	12-bit I Sample	—

Unpacked Real-Only Data - D7 = 1, D6 = 1, D0 = 1 (High Word)			
Samples	**D31 - D20**	**D19 - D16**	**D15 - D0**
All	12-bit I Sample	—	—

3.7 Channel Control Register #1 (continued)

3.7.1 Format Selection (continued)

3.7.1.1 Input Data Coding

Input data supplied to the Model 6229 must be encoded in true 2's complement format. The MSB (D15) is used as a sign bit and indicates a negative input voltage when set to the logic '1' state. The maximum negative output voltage (–1 VDC in uncompensated, single–tone mode) will be achieved when the input data code is `1000 0000 0000 0000` (`0x8000`), while an output exactly one step above half–scale (@ +490 µVDC) will be produced when all 16 input bits are cleared to the logic '0' state. A full–scale positive output voltage (+1 VDC) is produced in response to an input data code of `0111 1111 1111 0000` (`0x7FF0`). Table 3–9, below, illustrates the input data coding scheme used by the Model 6229.

Table 3-9: Model 6229 - Input Data Coding

Step (Decimal)	Output Voltage (DC, Nominal)	Binary Input Code (D15 - D0)	Hexadecimal Output Code
0	-1.00000 V	`1000 0000 0000 0000`	`0x8000`
1	-0.99951 V	`1000 0000 0001 0000`	`0x8010`
2	-0.99902 V	`1000 0000 0010 0000`	`0x8020`
⋮	⋮	⋮	⋮
2046	-0.00049 V	`1111 1111 1110 0000`	`0xFFE0`
2047	0.00000 V	`1111 1111 1111 0000`	`0xFFF0`
2048	+0.00049 V	`0000 0000 0000 0000`	`0x0000`
2049	+0.00098 V	`0000 0000 0001 0000`	`0x0010`
⋮	⋮	⋮	⋮
4093	+0.99902 V	`0111 1111 1101 0000`	`0x7FD0`
4094	+0.99951 V	`0111 1111 1110 0000`	`0x7FE0`
4095	+1.00000 V	`0111 1111 1111 0000`	`0x7FF0`



The discussion and table above do not take into account the tag bit, which is used only to identify Real samples in unpacked, I/Q format. For more details about the tag bit, please refer to Section 3.7.1, on the previous page.

3.7 Channel Control Register #1 (continued)

3.7.2 External Profile Select Enable D5

The AD9856 DUC chip contains four sets of internal profile registers, used to store different groups of settings that may be required for a given applica–tion. These profiles are selected among by means of two pins on the device, PS1 and PS0. There are two means by which these pins can be driven on the Model 6229.

When this bit is set to the logic '1' state, external profile selection is enabled. In this case, the profile select pins are driven by signals applied to pins on the Multi–pin connector at the center of the Model 6229's front panel (see Table 2–1 and Section 2.3.3).

When this bit is cleared to the logic '0' state, internal profile selection is enabled (i.e., external profile selection is disabled). In this case, a given channel's profile selection is determined by the Profile Select pins in this register (D4 : D3 in this register, see Section 3.7.3, below).

3.7.3 Profile Selection D4 & D3

These bits are only active when the External Profile Select Enable bit (D5 in this register, see Section 3.7.2, above) is cleared to the logic '0' state. In this case, the selected profile register set is equal to the binary value written to this bit field, plus 1. Table 3–10, below, provides details about the AD9856 registers selected by the 4 states this bit field may assume.

Table 3-10: Model 6229 - Profile Selection and AD9856 Profile Registers

D4 (or XPS1)	D3 (or XPS0)	Profile #	AD9856 Registers
0	0	1	02 - 06
0	1	2	07 - 0C
1	0	3	0D - 12
1	1	4	13 - 18

When bit D5 in this register is cleared to the logic '0' state, the states of these two bits is meaningless. When this is the case, the states of the front panel External Profile Select pins (XPS1 and XPS0, see Section 2.3.3) select the AD9856 profile registers.

3.7 Channel Control Register #1 (continued)

3.7.4 BIFO Read Rate Divider Synchronized Reset Enable D2

When this bit is set to the logic '1' state, the BIFO Read Rate Divider (see Section 3.6) will be reset by the SSYNC signal. This allows multiple channels and devices to be synchronized. When this bit is cleared to the logic '0' state, the SSYNC signal does not reset the BIFO Read Rate Divider, and the chan–nel will operate asynchronously with other channels in the system.

3.7.5 Output Amplifier Enable D1

This bit must be set to the logic '1' state to turn on the Model 6229's output amplifier. When this bit is cleared to the logic '0' state, the AD8320 is placed into its power–down mode and no output signal can be obtained from the channel in question.

3.7.6 Data Position in Input Longword D0

When the D6 bit in this register (see Section 3.7.1) is set to the logic '1' state (i.e., when the channel is configured to accept unpacked data) this bit determines whether the sample is expected in the upper or lower word if the input longword. Set this bit to the logic '1' state if the sample will reside in the high word (D31 – D16). Clear this bit to the logic '0' state if the low word (D15 – D0) will contain the sample. The effect of this bit is illustrated in Table 3–8, on page 32.

3.8 Channel Control Register #2 – R/W @ VIMReg_base + 0x0034

Channel Control Register #2 on the Model 6229 contains enable bits for the input BIFO, for the buffers that supply data to the AD9856, and for synchronization of the profile selects and the upconverters. It also contains bits to reset the upconverter and its serial control port. Each upconverter channel on the Model 6229 (i.e., each processor on the baseboard that can access this module) has its own unique version of this register. Table 3–11, below, summarizes the contents of this register. Detailed bit descriptions may be found in the subsections that begin at the top of the next page.

Table 3-11: Model 6229 - Channel Control Register #2
R/W @ VIMReg_base + 0x0034

Bit #	D31 - D7						
Name	Not Used						
Function	Write with 0's, Mask when Reading						
Bit #	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	BIFO Mode	BIFO Enable	Data Enable	Sync_PS _Enable	Reset_UC_ Ctl_Port	Sync_UC_ Reset_En	UC_ Reset
Function	1 = Enable 0 = Disable				1 = Reset 0 = Release	1 = Enable 0 = Disable	1 = Reset 0 = Release
All bits default to the logic '0' state at power-up and reset							

3.8 Channel Control Register #2 (continued)

3.8.1 BIFO Read Mode D6

This bit determines the read mode of the baseboard BIFO. When this bit is cleared to the logic '0' state, the BIFO read enables may be set to begin synchronously with other channels. When this bit set to the logic '1' state, the BIFO read is controlled by the BIFO Enable bit (D5 in this register) only. In this case, BIFO data will begin to stream when a '1' is written to D5 and will stop streaming when a '0' is written to D5.

Note that SSYNC will not start reads from the BIFO by this method if the BIFO is empty, and reads will terminate if the BIFO empties after reads have begun. When the BIFO Mode bit (D6) is set for asynchronous read mode, then the data will be read from the baseboard whenever this bit contains a '1', and is not affected by SSYNC or the BIFO sync bit in the Master Control Register. In this mode, reads will begin even if the BIFO is empty, and the user must ensure that enough data is in the BIFO before releasing reads so the BIFO does not empty, causing breaks in the data flow. If the user attempts to force a read of an empty BIFO the last data sample will be read indefinitely.

3.8.2 Baseboard BIFO Enable D5

This bit has two functions, determined by the BIFO Mode bit (bit D6 in this register). When the BIFO Mode bit is cleared to the logic '0' state for synchronous reads, then to read data from the baseboard, this bit must be set to the logic '1' state. (In addition, the BIFO sync bit in the Master Control Register (see Section 3.4.5) must be set, and an SSYNC pulse must be fired either externally (see Section 2.3.1.3) or internally (see Section 3.10). This bit was provided to disable the BIFO path in one channel and allow the other channel to acquire data. This bit can be cleared to the logic '0' state in the channel you wish to keep idle. When this bit contains a '0', the input data stream from the VIM baseboard is replaced by a stream of constant zero data. This forces the DUC output to a 0 V_{DC} level, instead of a raw carrier of unknown amplitude, when the enable is removed.

3.8.3 Data Enable D4

This bit must be set to the logic '1' state to allow input data samples to be applied to the AD9856. It must also be cleared to the logic '0' state when changing interpolation rates or multiplier settings on the AD9856. When this bit contains a '0', the input data stream from the VIM baseboard is replaced by a stream of constant zero data. This prevents an unrecoverable overflow condition that may result when changing AD9856 settings (see the AD9856 data sheet, in Appendix A, for more information).

3.8 Channel Control Register #2 (continued)

3.8.4 Synchronized Profile Selection Enable D3

When this bit is set to the logic '1' state, profile changes (either from the profile select bits (see Section 3.7.3), or the front panel profile select pins (see Sections 2.3.3 and 3.7.2) occur on the next rising edge of the SSYNC signal, allowing changes in settings to be synchronized with those on other channels or devices. When this bit is cleared to the logic '0' state, profile changes occur asynchronously.

3.8.5 Reset Upconverter Serial Control Port D2

Settings changes on the AD9856 are made via a serial control interface. Set this bit to the logic '1' state to reset this interface. This bit must be cleared to the logic '0' state for normal upconverter operation.

3.8.6 Synchronized Upconverter Reset Enable D1

When this bit is set to the logic '1' state, the rising edge of the SSYNC signal is used to reset the AD9856, for synchronized operation. When this bit is cleared to the logic '0' state, SSYNC does not reset the upconverter.

3.8.7 Up Converter Reset D0

Set this bit to the logic '1' state to reset the AD9856 upconverter. This reset is asynchronous, and overrides the Synchronized Reset Enable (Section 3.8.6, above). This bit must be cleared to the logic '0' state for normal upconverter operation.

3.9 Serial Port Enable Register – R/W @ VIMReg_base + 0x0038

A unique copy of this register exists in the memory space of each processor that can access a given 6229. The register contains only one active bit (D0), which is set to the logic '1' state to connect the serial port of the other processor to the processor that can access the bit. When this bit is cleared to the logic '0' state, the other processor's serial port is not connected to this processor's. Table 3–12, below, shows the register's contents.

Table 3-12: Model 6229 - Serial Port Enable
R/W @ VIMReg_base + 0x0038

Bit #	D31 - D1	D0
Name	Not Used	Ser_Port _Enable
Function	Write with 0's, Mask when Reading	1 = Connect 0 = Disconnect
All bits default to the logic '0' state at power-up and reset		

3.10 Sync Generate Register – R/W @ VIMReg_base + 0x003C

This register can only be accessed by Processor A or Processor C on the VIM baseboard, depending upon the position in which the module is installed. It does not exist in the memory maps for Processors B or D. This register would be used only on a 6229 that is configured as a Sync Bus master, or on a stand–alone unit that is not connected to an external Sync Bus. It contains only one active bit (D0), which used to generate sync signals on all unmasked sync outputs (see Table 3–4 and Sections 3.4.2, 3.4.3, and 3.4.4 for details about masking and enabling these outputs). When this bit is cleared to the logic '0' state, all sync outputs that are not masked will transition to a low logic level on the next rising edge of the reference clock signal. When this bit is set to the logic '1' state, all sync outputs that are not masked will transition to a high logic level on the next rising edge of the reference clock signal. Note that when reading this bit, it will not assume the last state written to it until the next rising edge of the reference clock signal. Table 3–13, below, summarizes this register's contents.

Table 3-13: Model 6229 - Sync Generate Register
R/W @ VIMReg_base + 0x003C

Bit #	D31 - D1	D0
Name	Not Used	Sync_ Generate
Function	Write with 0's, Mask when Reading	See Text Above
All bits default to the logic '0' state at power-up and reset		

When an external signal is connected to the $\overline{\text{TTL–SYNC}}$ input of the 6229 Sync Bus / Serial I/O Connector (see Section 2.3.2), the external signal is OR'ed with this bit to determine the sync transition.

The only signal among those that this bit is used to generate that actually has an effect on the Model 6229 is the SSYNC signal. On the Model 6229, SSYNC can be enabled to synchronously reset the baseboard BIFO (see Section 3.4.5), the BIFO Read Rate Divider (see Section 3.7.4) and the AD9856 (see Section 3.8.6). It can also be used to synchronize changes in DUC profile selections (see Section 3.8.4).

3.11 Upconverter Address Register – R/W @ VIMReg_base + 0x0040

The two AD9856 Digital Up Converter devices used on the Model 6229 each contain 26 internal control registers. These include the four groups of six profile registers, and two additional global control registers. The memory map for these registers is shown on page DS–11 of Appendix A (the AD9856 Data Sheet) in this manual. To access any of these registers, the internal address of the desired register in question must first be written to the 5 LSBs (D4 : D0) of this register. Another bit (D7) is provided in this register to determine whether the access to the AD9856 is a read or a write. Table 3–14, below, summarizes the content of this register.

Table 3-14: Model 6229 - Upconverter Address Register
R/W @ VIMReg_base + 0x0040

Bit #	D31 - D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	Access_Type	Not Used		DUC_A4	DUC_A3	DUC_A2	DUC_A1	DUC_A0
Function	1 = Read 0 = Write	Write with 0's, Mask when Reading		5-bit address of AD9856 register to be accessed				
All bits default to the logic '0' state at power-up and reset								

3.12 Upconverter Data Register – R/W @ VIMReg_base + 0x0044

After writing the address of register in the AD9856 that access is desired to, that access is completed by accessing this register. If the desired access type is a write, the data to be written to the AD9856's register is written here. That data will be written to the address pointed to by the Up Converter Address Register (see Section 3.11, above). To read the contents of a register in the upconverter, read this register. The data will be fetched from the AD9856 register pointed to by the Up Converter Address Register, and will be returned to this register. Table 3–15, below, shows this register's contents.

Table 3-15: Model 6229 - Upconverter Data Register
R/W @ VIMReg_base + 0x0044

Bit #	D31 - D8							
Name	Not Used							
Function	Write with 0's, Mask when Reading							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	DUC_D7	DUC_D6	DUC_D5	DUC_D4	DUC_D3	DUC_D2	DUC_D1	DUC_D0
Function	For Write operations - data to be written to AD9856 address pointed to by Address Register For Read operations - data returned from AD9856 address pointed to by Address Register							
All bits default to the logic '0' state at power-up and reset								

3.13 Mandatory Up Converter Register Settings

For proper operation of the Model 6229, certain control bits in the AD9856 **MUST** be set to specific states. These are summarized in Table 3–16, below. It is also very important that the register at address 0 in the AD9856 be accessed **BEFORE** changing the setting of **ANY** other register on the Up Converter.

Table 3-16: Model 6229 - Mandatory Up Converter Register Settings

AD9856 Register 0								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	SDO_ Active	LSB_ First	REFCLK_ Mult_4	REFCLK_ Mult_3	REFCLK_ Mult_2	REFCLK_ Mult_1	REFCLK_ Mult_0	Reserved*
Required State	1	0	—	—	—	—	—	1
AD9856 Register 1								
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	CIC_ Gain	Continuous _Mode	Full_Sleep _Mode	Single_Tone Mode	Bypass_Inv _Sinc_Filter	Bypass_ REFCLK_Mult	Input_Format _Select_1	Input_Format _Select_0
Required State	—	1	—	—	—	—	1	0
* This bit's state is mandated by the AD9856 Data Sheet, not the Model 6229's design								

The register settings described above establish the following operating conditions for the AD9856:

- The Serial Control port is configured to use dedicated input and output lines instead of a single I/O line.
- Serial Control Data is shifted into the DUC MSB first.
- The DUC must be operated in Continuous mode (NOT burst mode).
- The DUC is configured to accept 12–bit input data.

Chapter 4: The AD8320 Digitally Controlled Variable Gain Line Driver

4.1 The AD8320 Digitally Controlled Variable Gain Line Driver

The AD8320 is a digitally controlled variable gain amplifier. An 8−bit serial word determines the desired output gain over a 36 dB range (256 gain levels). The AD8320 provides linear gain response. The AD8320 is made up of a digitally controlled variable attenuator of 0 dB to –36 dB, which is preceded by a low−noise, fixed−gain buffer, and followed by a low−distortion, high−power amplifier. The AD8320 has a 220−ohm input impedance and accepts a single−ended input signal with a specified analog input level of up to 0.310 V_{p-p}. The output is specified for driving a 75−ohm load, although the AD8320 is capable of driving other loads. Distortion performance of –57 dBc is achieved with an output level up to 12 dBm (3.1 V_{p-p}) at 42 MHz, while –46 dBc distortion is achieved with an output level up to 18 dBm (6.2 V_{p-p}).

A key performance of the AD8320 results from the ability to maintain a constant 75 ohm output impedance during power−up and power−down conditions. This eliminates the need for external 75−ohm back−termination, resulting in twice the effective output voltage when compared to a standard operational amplifier. Additionally, the on−chip 7− ohm termination results in low glitch output during power−down and power−up transitions, eliminating the need for an external switch.

Additional information on the AD8320 variable gain amplifier is provided in Appendix B of this manual.

4.2 Programming the Variable Gain Line Driver

The AD8320 Digitally Controlled Variable Gain Line Driver is programmed via Registers 07, 0D, 13, and/or 19 (dependent on one of four selectable profiles) of the AD9856 Quadrature Digital Upconverter. Additional information on the AD9856 Quadrature Digital Upconverter can be found in Appendix A of this manual. Additional information on the AD8320 variable gain amplifier can be found in Appendix B of this manual.

The following formulas can be used to determine the output voltages of the 6229 VIM-2 module. These output voltages are dependent on the code settings programmed to the AD8320 Variable Gain Line Driver.

With a 50Ω Load:

CODE = AD8320's gain setting

Single Tone Mode $V_{p-p} = 0.2(0.316 + (0.077 * CODE))$
(SIN X/X compensation bypassed)

$V_{p-p} = 0.14(0.316 + (0.077 * CODE))$
(SIN X/X compensation on)

Modulation Mode: $V_{p-p} = 0.1(0.316 + (0.077 * CODE))$
(SIN X/X compensation bypassed)

$V_{p-p} = 0.07(0.316 + (0.077 * CODE))$
(SIN X/X compensation on)

With a 75Ω Load:

CODE = AD8320's gain setting

Single Tone Mode $V_{p-p} = 0.25(0.316 + (0.077 * CODE))$
(SIN X/X compensation bypassed)

$V_{p-p} = 0.175(0.316 + (0.077 * CODE))$
(SIN X/X compensation on)

Modulation Mode: $V_{p-p} = 0.125(0.316 + (0.077 * CODE))$
(SIN X/X compensation bypassed)

$V_{p-p} = 0.088(0.316 + (0.077 * CODE))$
(SIN X/X compensation on)

Appendix A: Analog Devices AD9856 – Quadrature Digital Upconverter

A.1 Digital Upconverter Data Sheet

Presented on the following pages is the Data Sheet for the Analog Devices AD9856 Quadrature Digital Upconverter.

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CMOS 200 MHz Quadrature Digital Upconverter

AD9856

FEATURES

Universal Low Cost Modulator Solution for Communications Applications
DC to 80 MHz Output Bandwidth
Integrated 12-Bit D/A Converter
Programmable Sample Rate Interpolation Filter
Programmable Reference Clock Multiplier
Internal SIN(x)/x Compensation Filter
>52 dB SFDR @ 40 MHz A_{OUT}
>48 dB SFDR @ 70 MHz A_{OUT}
>80 dB Narrowband SFDR @ 70 MHz A_{OUT}
+3 V Single Supply Operation
Space-Saving Surface-Mount Packaging
Bidirectional Control Bus Interface
Supports Burst and Continuous Tx Modes
Single Tone Mode for Frequency Synthesis Applications
Four Programmable, Pin-Selectable Modulator Profiles
Direct Interface to AD8320/AD8321 PGA Cable Driver

APPLICATIONS

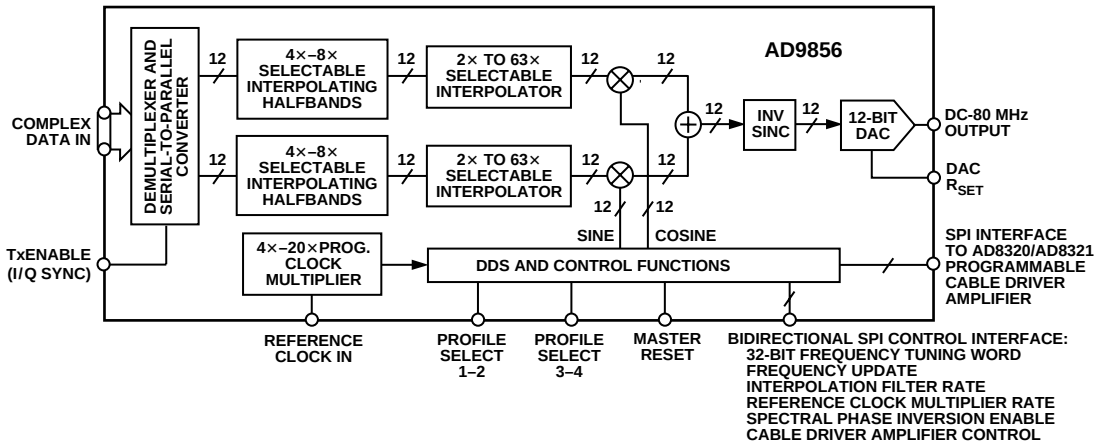
HFC Data, Telephony and Video Modems
Wireless and Satellite Communications
Cellular Basestations

GENERAL DESCRIPTION

The AD9856 integrates a high speed direct-digital synthesizer (DDS), a high performance, high speed 12-bit digital-to-analog converter (DAC), clock multiplier circuitry, digital filters and other DSP functions onto a single chip, to form a complete quadrature digital upconverter device. The AD9856 is intended to function as a universal I/Q modulator and agile upconverter for communications applications, where cost, size, power dissipation and dynamic performance are critical attributes.

The AD9856 is available in a space-saving surface mount package and specified to operate over the extended industrial temperature range of –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD9856–SPECIFICATIONS (V_S = +3 V ± 5%, R_{SET} = 3.9 kΩ, External reference clock frequency = 10 MHz with REFCLK Multiplier enabled at 20×).

Parameter	Temp	Test Level	AD9856 Min	AD9856 Typ	AD9856 Max	Units
REF CLOCK INPUT CHARACTERISTICS						
Frequency Range						
REFCLK Multiplier Disabled	Full	VI	5		200[1]	MHz
REFCLK Multiplier Enabled at 4×	Full	VI	5		50	MHz
REFCLK Multiplier Enabled at 20×	Full	VI	5		10	MHz
Duty Cycle	+25°C	V		50		%
Input Capacitance	+25°C	V		3		pF
Input Impedance	+25°C	V		100		MΩ
DAC OUTPUT CHARACTERISTICS						
Resolution				12		Bits
Full-Scale Output Current			5	10	20	mA
Gain Error	+25°C	I	–10		+10	%FS
Output Offset	+25°C	I			10	µA
Differential Nonlinearity	+25°C	V		0.5		LSB
Integral Nonlinearity	+25°C	V		1		LSB
Output Capacitance	+25°C	V		5		pF
Phase Noise @ 1 kHz Offset, 40 MHz A_{OUT}						
REFCLK Multiplier Enabled at 20×	+25°C	V		–85		dBc/Hz
REFCLK Multiplier at 4×	+25°C	V		–100		dBc/Hz
REFCLK Multiplier Disabled	+25°C	V		–110		dBc/Hz
Voltage Compliance Range	+25°C	I	–0.5		1.5	V
Wideband SFDR:						
1 MHz Analog Out	+25°C	IV		70		dBc
20 MHz Analog Out	+25°C	IV		65		dBc
42 MHz Analog Out	+25°C	IV		60		dBc
65 MHz Analog Out	+25°C	IV		55		dBc
80 MHz Analog Out	+25°C	IV		50		dBc
Narrowband SFDR: (±100 kHz Window)						
70 MHz Analog Out	+25°C	IV		80		dBc
MODULATOR CHARACTERISTICS						
Adjacent Channel Power (CH Power = –6.98 dBm)	+25°C	IV	50			dBm
Error Vector Magnitude	+25°C	IV		1	2	%
I/Q Offset	+25°C	IV	50	55		dB
Inband Spurious Emissions	+25°C	IV	45	50		dBc
Pass Band Amplitude Ripple (DC to 80 MHz)	+25°C	V		±0.3		dB
TIMING CHARACTERISTICS						
Serial Control Bus						
Maximum Frequency	Full	IV			10	MHz
Minimum Clock Pulsewidth High (t_{PWH})	Full	IV	30			ns
Minimum Clock Pulsewidth Low (t_{PWL})	Full	IV	30			ns
Maximum Clock Rise/Fall Time	Full	IV			1	ms
Minimum Data Setup Time (t_{DS})	Full	IV	25			ns
Minimum Data Hold Time (t_{DH})	Full	IV	0			ns
Maximum Data Valid Time (t_{DV})	Full	IV	30			ns
Wake-Up Time[2]	Full	IV			1	ms
Minimum RESET Pulsewidth High (t_{RH})	Full	IV	5			REFCLK Cycles
CMOS LOGIC INPUTS						
Logic "1" Voltage	+25°C	I	+2.6			V
Logic "0" Voltage	+25°C	I			+0.4	V
Logic "1" Current	+25°C	I			12	µA
Logic "0" Current	+25°C	I			12	µA
Input Capacitance	+25°C	V		3		pF

Parameter	Temp	Test Level	AD9856 Min	Typ	Max	Units
CMOS LOGIC OUTPUTS (1 mA LOAD)						
Logic "1" Voltage	+25°C	I	2.7			mA
Logic "0" Voltage	+25°C	I			0.4	mA
POWER SUPPLY						
$+V_S$ Current						
Full Operating Conditions[2]	+25°C	I			530	mA
Burst Operation (25%)	+25°C	I			450	mA
Single Tone Mode	+25°C	I			495	mA
160 MHz Clock	+25°C	I			445	mA
120 MHz Clock	+25°C	I			345	mA
Power-Down Mode	+25°C	I			2	mA

NOTES
[1]For 200 MHz operation in Modulation Mode at +85 °C operating temperature, V_S must be +3 V min.
[2]Assuming 1.3 kΩ and 0.01 µF loop filter components.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Maximum Junction Temperature . . . . . +165°C
Storage Temperature . . . . . –65°C to +150°C
V_S . . . . . +4 V
Operating Temperature . . . . . –40°C to +85°C
Digital Inputs . . . . . –0.7 V to $+V_S$
Lead Temperature (Soldering 10 sec) . . . . . +300°C
Digital Output Current . . . . . 5 mA
θ_{JA} Thermal Impedance . . . . . 38°C/W

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

EXPLANATION OF TEST LEVELS
Test Level

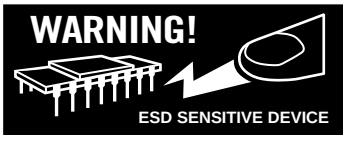
I – 100% Production Tested.
III – Sample Tested Only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – Devices are 100% production tested at +25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9856AST	–40°C to +85°C	Thin Quad Flatpack	ST-48
AD9856/PCB	+25°C	Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9856 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



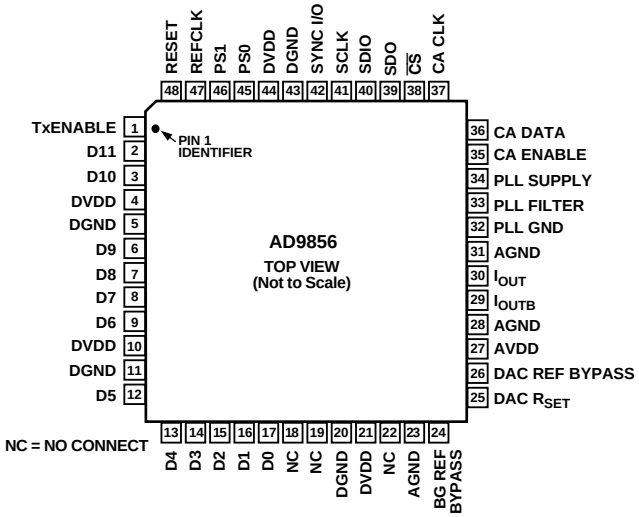
PIN FUNCTION DESCRIPTIONS

Pin #	Pin Name	Pin Function
1	TxENABLE	Input Pulse that Synchronizes the Data Stream
2	D11	Input Data (Most Significant Bit)
3	D10	Input Data
4, 10, 21, 44	DVDD	Digital Supply Voltage
5, 11, 20, 43	DGND	Digital Ground
6–9	D9–D6	Input Data
12–16	D5–D1	Input Data
17	D0	Input Data (Least Significant Bit)
18, 19, 22	NC	No Internal Connection
23, 28, 31	AGND	Analog Ground
24	BG REF BYPASS	No External Connection*
25	DAC R_{SET}	R_{SET} Resistor Connection
26	DAC REF BYPASS	No External Connection*
27	AVDD	Analog Supply Voltage

Pin #	Pin Name	Pin Function
29	I_{OUTB}	Complementary Analog Current Output of the DAC
30	I_{OUT}	True Analog Current Output of DAC
32	PLL GND	PLL Ground
33	PLL FILTER	PLL Loop Filter Connection
34	PLL SUPPLY	PLL Voltage Supply
35	CA ENABLE	Cable Driver Amp Enable
36	CA DATA	Cable Driver Amp Data
37	CA CLK	Cable Driver Amp Clock
38	$\overline{CS}$	Chip Select
39	SDO	Serial Data Output
40	SDIO	Serial Port I/O
41	SCLK	Serial Port Clock
42	SYNC I/O	Performs I/O Synchronization
45	PS0	Profile Select 0
46	PS1	Profile Select 1
47	REFCLK	Reference Clock Input
48	RESET	Master Reset

*In most cases optimal performance is achieved with no external connection. For extremely noisy environments BG REF BYPASS can be bypassed with up to a 0.1 µF capacitor to AGND (Pin 23). DAC REF BYPASS can be bypassed with up to a 0.1 µF capacitor to AVDD (Pin 27).

PIN CONFIGURATION



FUNCTIONAL BLOCK AND MODE DESCRIPTION

Operating Modes	1. Complex quadrature modulator mode. 2. Single tone output mode.
Input Data Format	Programmable: 12-bit, 6-bit, or 3-bit input formats. Data input to the AD9856 is 12-bit, twos complement. Complex I/Q symbol component data is required to be at least 2× oversampled, depending upon configuration.
Input Sample Rate	Up to 50 Msamples/s @ 200 MHz SYSCLK rate.
Input Reference Clock Frequency	For DC-80 MHz A_{OUT} operation (200 MHz SYSCLK rate): w/REFCLK Multiplier enabled: 10 MHz–50 MHz, programmable via control bus w/REFCLK Multiplier disabled: 200 MHz. Note: For optimum data synchronization, the AD9856 Reference Clock, and the input data clock, should be derived from the same clock source.
Internal Reference Clock Multiplier	Programmable in integer steps over the range of 4×–20×. Can be disabled (effective REFCLK Multiplier = 1) via control bus. Output of REFCLK Multiplier = SYSCLK rate, which is the internal clock rate applied to the DDS and DAC function.
Profile Select	Four pin-selectable, preprogrammed formats. Available for modulation and single tone operating modes.
Interpolating Range	Fixed 4×, selectable 2× and selectable 2×–63× range.
Half-Band Filters	Interpolating filters that provide upsampling and reduce the effects of the CIC passband roll-off characteristics.
TxENABLE Function–Burst Mode	When Burst Mode is enabled via the control bus, the rising edge of the applied TxENABLE pulse should be coincident with, and frame, the input data packet. This establishes data sampling synchronization.
TxENABLE Function–Continuous Mode	When continuous mode is enabled via the control bus, the TxENABLE pin becomes an I/Q control line. A Logic "1" on TxENABLE indicates I data is being presented to the AD9856. A Logic "0" on TxENABLE indicates Q data is being presented to the AD9856. Each rising edge of TxENABLE resynchronizes the AD9856 input sampling capability.
Inverse SINC Filter	Precompensates for SIN(x)/x roll-off of DAC; user bypassable.
I/Q Channel Invert	$[I \times Cos(\omega t) + Q \times Sin(\omega t)]$ or $[I \times Cos(\omega t) - Q \times Sin(\omega t)]$ (default), configurable via control bus, per profile.
Full Sleep Mode	Power dissipation reduced to less than 6 mW when Full Sleep Mode active, programmable via control bus.

Typical Modulated Output Spectral Plots

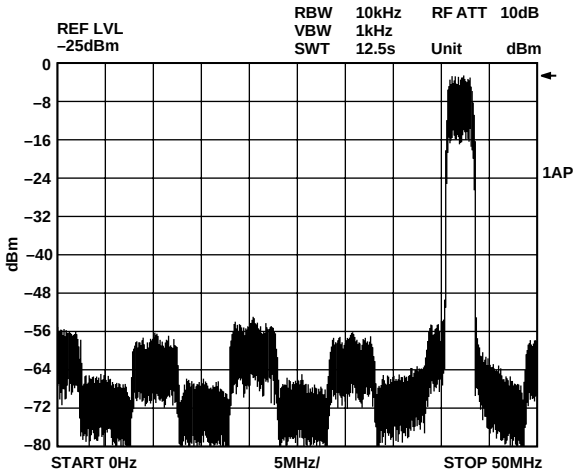


Figure 1. QPSK at 42 MHz and 2.56 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 12, CIC = 3, HB3 On, 2× Data

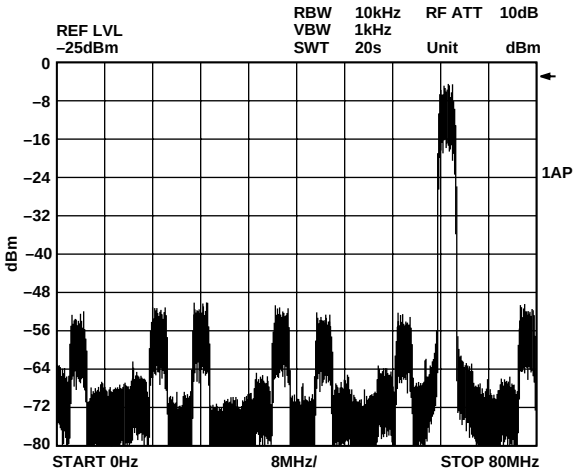


Figure 3. 16-QAM at 65 MHz and 2.56 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 18, CIC = 9, HB3 Off, 2× Data

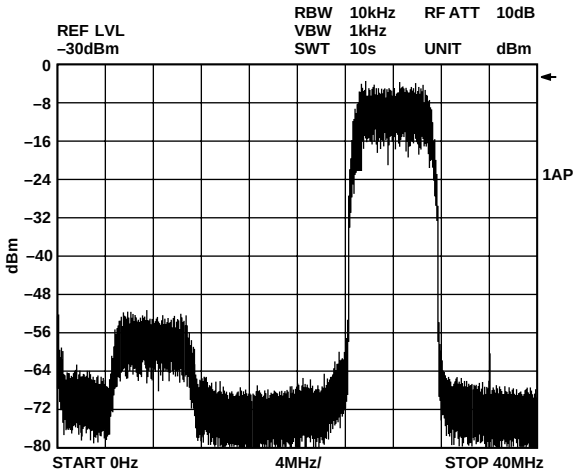


Figure 2. 64-QAM at 28 MHz and 6 MS/s; 36 MHz External Clock with REFCLK Multiplier = 4, CIC = 2, HB3 Off, 3× Data

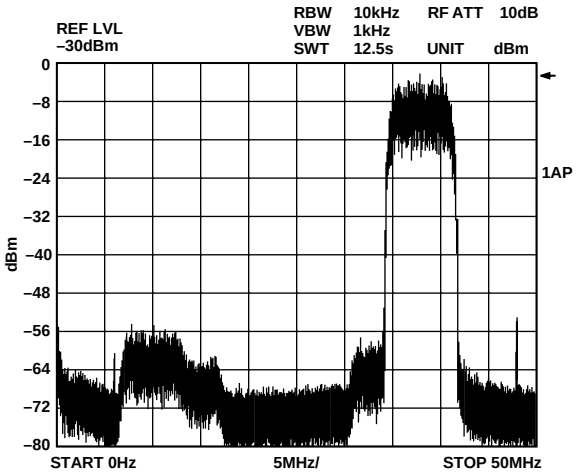


Figure 4. 256-QAM at 38 MHz and 6 MS/s; 48 MHz External Clock with REFCLK Multiplier = 4, CIC = 2, HB3 Off, 4× Data

Typical Single Tone Output Spectral Plots

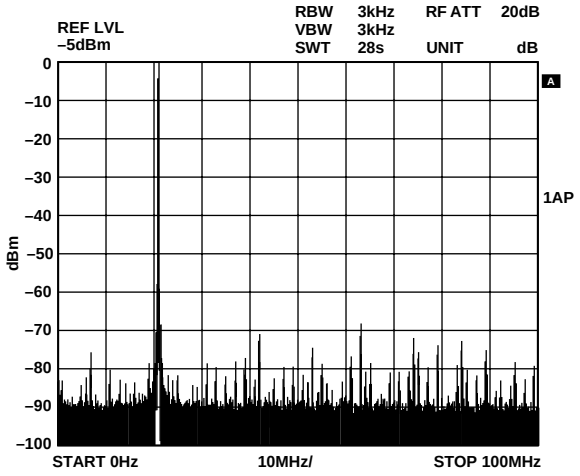


Figure 5. 21 MHz CW Output

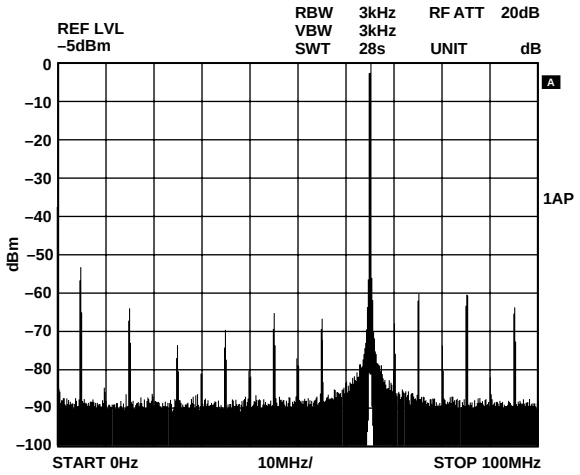


Figure 6. 65 MHz CW Output

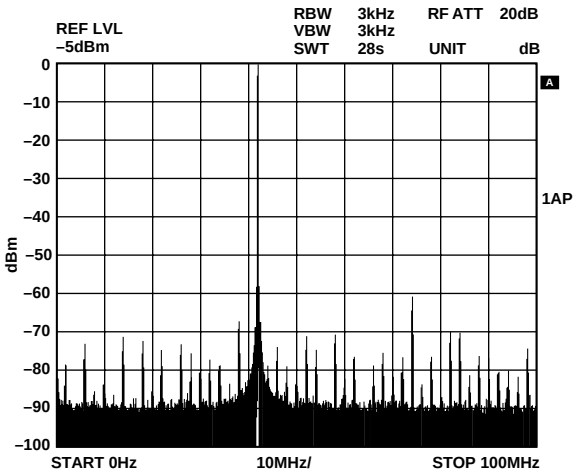


Figure 7. 42 MHz CW Output

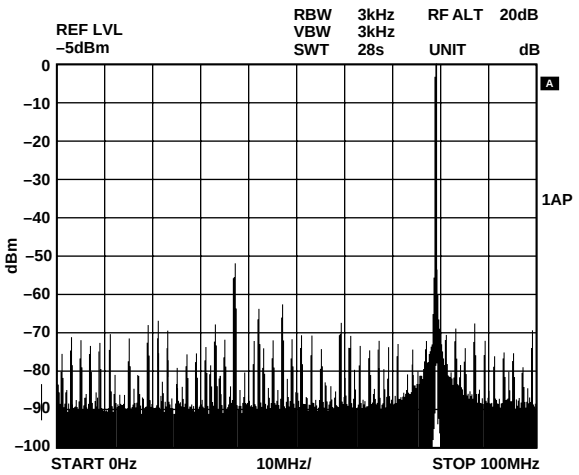


Figure 8. 79 MHz CW Output

Typical Narrowband SFDR Spectral Plots

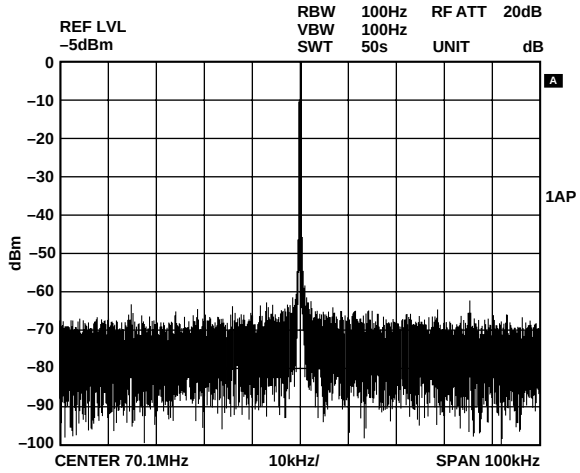


Figure 9. 70.1 MHz Narrowband SFDR, 10 MHz External Clock with REFCLK Multiplier = 20×

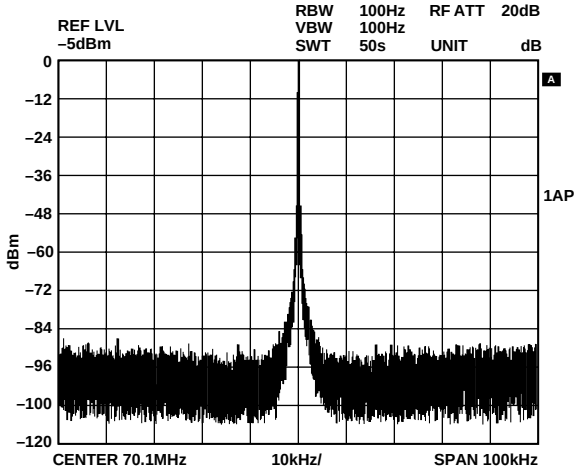


Figure 11. 70.1 MHz Narrowband SFDR, 200 MHz External Clock with REFCLK Multiplier Disabled

Typical Phase Noise Spectral Plots

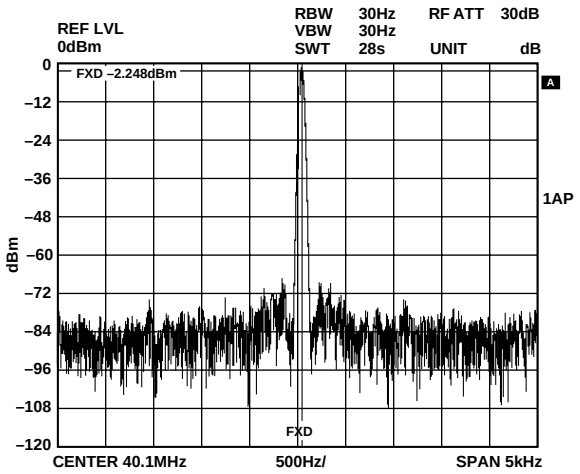


Figure 10. 40.1 MHz Output, 10 MHz External Clock with REFCLK Multiplier = 20×

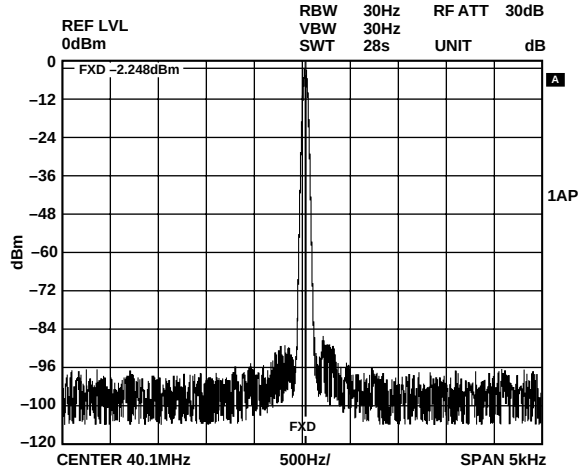


Figure 12. 40.1 MHz Output, 200 MHz External Clock with REFCLK Multiplier Disabled

Typical Plots of Output Constellations

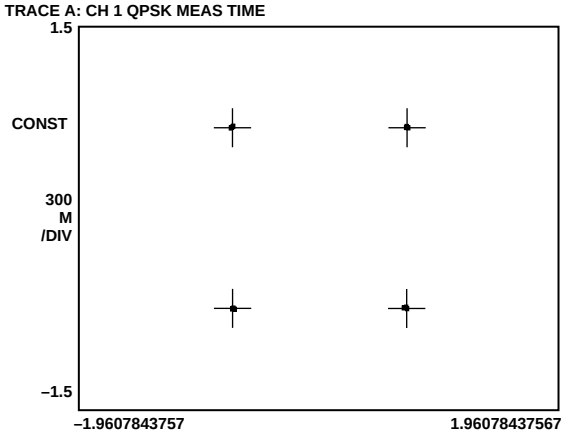


Figure 13. QPSK, 65 MHz, 2.56 MS/s

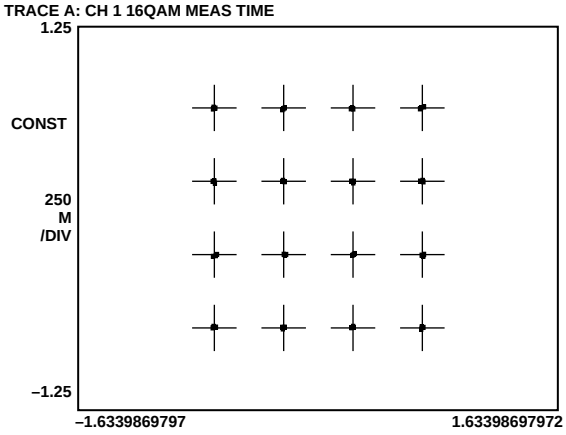


Figure 15. 16-QAM, 65 MHz, 2.56 MS/s

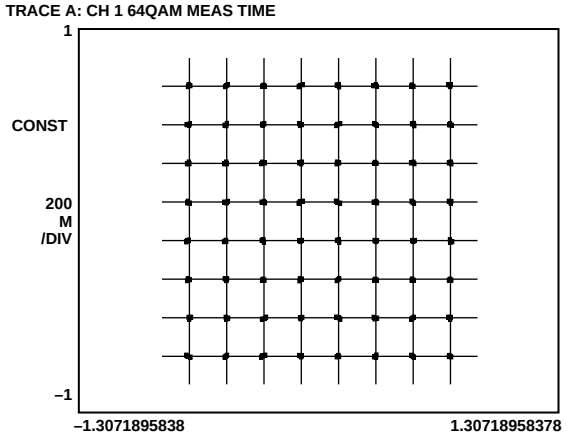


Figure 14. 64-QAM, 42 MHz, 6 MS/s

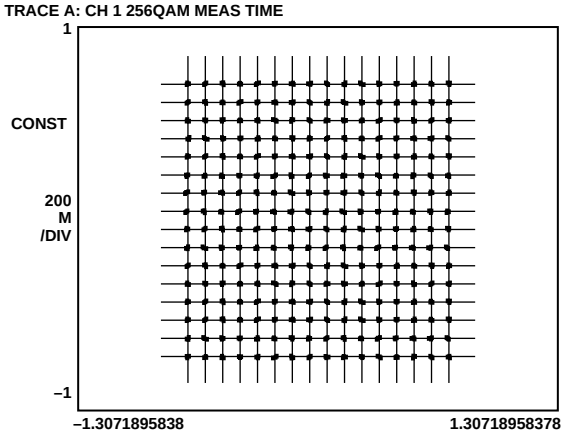


Figure 16. 256-QAM, 42 MHz, 6 MS/s

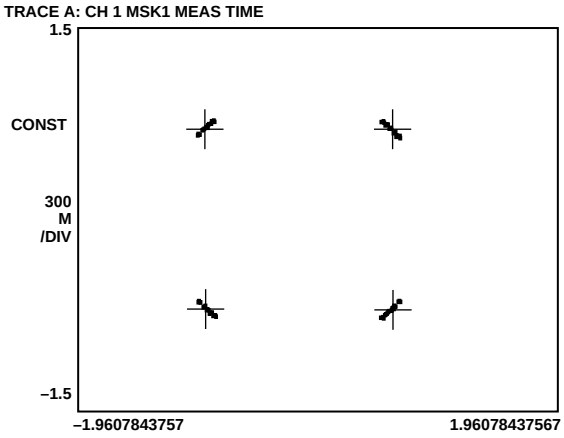


Figure 17. GMSK Modulation, 13 MS/s

Power Consumption

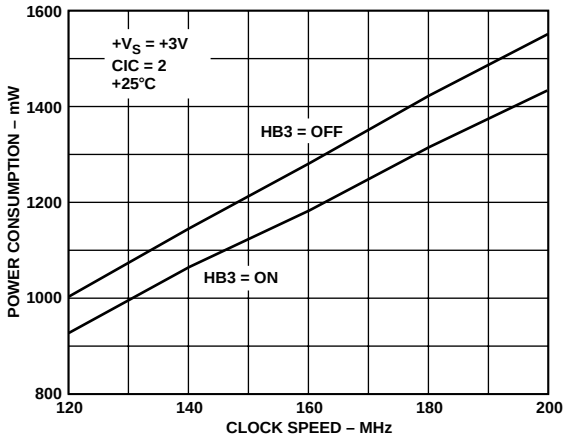


Figure 18. Power Consumption vs. Clock Speed; $+V_S$ = +3 V, CIC = 2, +25°C

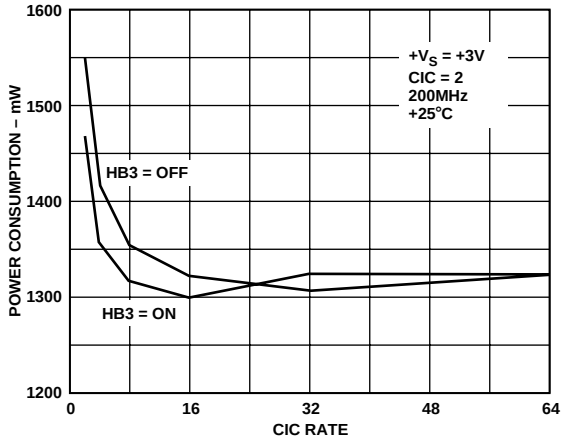


Figure 19. Power Consumption vs. CIC Rate; $+V_S$ = +3 V, 200 MHz, +25°C

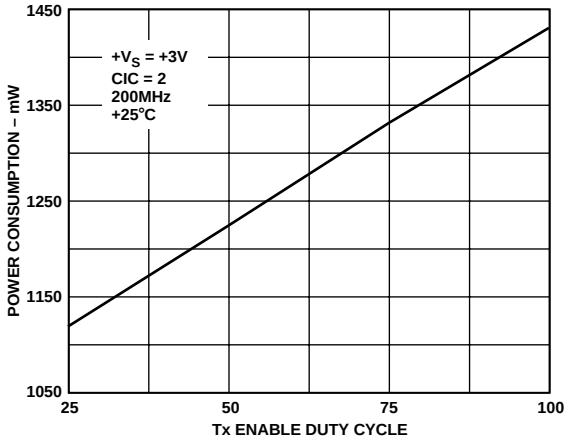


Figure 20. Power Consumption vs. Burst Duty Cycle; $+V_S$ = +3 V, CIC = 2, 200 MHz, +25°C

Table I. Serial Control Bus Register Layout

Register	AD9856 Register Layout									
Address (hex)	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default (hex)**	**Profile**
00	SDO Active	LSB First	REFCLK Mult.<4>	REFCLK Mult.<3>	REFCLK Mult.<2>	REFCLK Mult.<1>	REFCLK Mult.<0>	Reserved	15	N/A
01	CIC Gain	Continuous Mode	Full Sleep Mode	Single Tone Mode	Bypass Inverse Sinc Filter	Bypass REFCLK Mult.	Input Format Select <1>	Input Format Select <0>	06	N/A
02	Frequency Tuning Word <7:0>								04	1
03	Frequency Tuning Word <15:8>								00	1
04	Frequency Tuning Word <23:16>								00	1
05	Frequency Tuning Word <31:24>								00	1
06	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half Band Filter	FC	1
07	AD8320/AD8321 Gain Control Bits <7:0>								00	1
08	Frequency Tuning Word <7:0>								00	2
09	Frequency Tuning Word <15:8>								00	2
0A	Frequency Tuning Word <23:16>								00	2
0B	Frequency Tuning Word <31:24>								80	2
0C	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half Band Filter	1E	2
0D	AD8320/AD8321 Gain Control Bits <7:0>								00	2
0E	Frequency Tuning Word <7:0>								Unset	3
0F	Frequency Tuning Word <15:8>								Unset	3
10	Frequency Tuning Word <23:16>								Unset	3
11	Frequency Tuning Word <31:24>								Unset	3
12	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half Band Filter	Unset	3
13	AD8320/AD8321 Gain Control Bits <7:0>								00	3
14	Frequency Tuning Word <7:0>								Unset	4
15	Frequency Tuning Word <15:8>								Unset	4
16	Frequency Tuning Word <23:16>								Unset	4
17	Frequency Tuning Word <31:24>								Unset	4
18	Interpolator Rate <5>	Interpolator Rate <4>	Interpolator Rate <3>	Interpolator Rate <2>	Interpolator Rate <1>	Interpolator Rate <0>	Spectral Inversion	Bypass the Third Half Band Filter	Unset	4
19	AD8320/AD8321 Gain Control Bits <7:0>								00	4

REGISTER BIT DEFINITIONS

Control Bits—Register Address 00h and 01h

SDO Active—Register Address 00h, Bit 7. Active high indicates serial port uses dedicated in/out lines. Default low configures serial port as single line I/O.

LSB First—Register Address 00h, Bit 6. Active high indicates serial port access is LSB to MSB format. Default low indicates MSB to LSB format.

REFCLK Multiplier—Register Address 00h, Bits 5, 4, 3, 2, 1 form the reference clock multiplier. Valid entries range from 4–20 (decimal). Straight binary to decimal conversion is implemented. For example, to multiply the reference clock by 19 decimal, Program Register Address 00h, Bits 5–1, as 13h. Default value is 0A (hex).

RESERVED BIT—Register Address 00h, Bit 0. This bit is reserved. Always set this bit to Logic 1 when writing to this register.

CIC GAIN—Register Address 01h, Bit 7. The CIC GAIN bit multiplies the CIC filter output by 2. See the Cascaded Integrated Comb Filter section of this data sheet for more details. Default value is 0 (inactive).

CONTINUOUS MODE—Register Address 01h, Bit 6 is the continuous mode configuration bit. Active high, configures the AD9856 to accept continuous mode timing on the TxENABLE input. A low configures the device for burst mode timing. Default value is 0 (burst mode).

FULL SLEEP MODE—Register Address 01h, Bit 5. Active high full sleep mode bit. When activated, the AD9856 enters a full shutdown mode, consuming less than 2 mA, after completing a shutdown sequence. Default value is 0 (awake).

SINGLE TONE MODE—Register Address 01h, Bit 4. Active high configures the AD9856 for single tone applications. The AD9856 will supply a single frequency output as determined by the frequency tuning word (FTW) selected by the active profile. In this mode, the 12 input data pins are ignored but should be tied high or low. Default value is 0 (inactive).

BYPASS INVERSE SINC FILTER—Register Address 01h, Bit 3. Active high, configures the AD9856 to bypass the SIN(x)/x compensation filter. Defaults value is 0 (Inverse SINC Filter Enabled).

BYPASS REFCLK Multiplier—Register Address 01h, Bit 2. Active high, configures the AD9856 to bypass the REFCLK Multiplier function. When active, effectively causes the REFCLK Multiplier factor to be 1. Defaults value is 1 (REFCLK Multiplier bypassed).

INPUT FORMAT SELECT—Register Address 01h, Bits 1 and 0, form the Input Format Mode bits.

10b = 12-bit mode
01b = 6-bit mode
00b = 3-bit mode
Default value is 10b (12-bit mode).

Profile 1 Registers—Active when PROFILE Inputs Are 00b

FREQUENCY TUNING WORD (FTW)—The frequency tuning word for Profile 1 is formed via a concatenation of register addresses 05h, 04h, 03h and 02h. Bit 7 of register address 05h is the most significant bit of the Profile 1 frequency tuning word. Bit 0 of register address 02h is the least significant bit of the Profile 1 frequency tuning word. The output frequency equation is given as: $f_{OUT} = (FTW \times SYSCLK)/2^{32}$.

INTERPOLATION RATE—Register Address 06h, Bits 7 through 2 form the Profile 1 CIC filter interpolation rate value. Allowed values range from 2 to 63 (decimal).

SPECTRAL INVERSION—Register Address 06h, Bit 1. Active high, Profile 1 Spectral Inversion bit. When active, inverted modulation is performed [$I \times Cos(\omega t) + Q \times Sin(\omega t)$]. Default is inactive, logic zero, noninverted modulation [$I \times Cos(\omega t) - Q \times Sin(\omega t)$].

BYPASS HALF-BAND FILTER 3—Register Address 06h, Bit 0. Active high, causes the AD9856 to bypass the third half-band filter stage that precedes the CIC interpolation filter. Bypassing the third half-band filter negates the 2× upsample inherent with this filter and reduces the overall interpolation rate of the half-band filter chain from 8× to 4×. Default value is 0 (half-band 3 enabled).

AD8320/AD8321 GAIN CONTROL—Register Address 07h, Bits 7 through 0 form the Profile 1 AD8320/AD8321 gain bits. The AD9856 dedicates three output pins, which directly interface to the AD8320/AD8321 cable driver amp. This allows direct control of the cable driver via the AD9856. See the Programming/Writing the AD8320/AD8321 Cable Driver Gain Control section of this data sheet for more details. Bit 7 is the MSB, Bit 0 is the LSB. Default value is 00h.

Profile 2 Registers—Active when PROFILE Inputs Are 01b

Profile 2 Register functionality is identical to Profile 1, with the exception of the register addresses.

Profile 3 Registers—Active when PROFILE Inputs Are 10b

Profile 3 Register functionality is identical to Profile 1, with the exception of the register addresses.

Profile 4 Registers—Active when PROFILE Inputs Are 11b

Profile 4 Register functionality is identical to Profile 1, with the exception of the register addresses.

THEORY OF OPERATION

To gain a general understanding of the functionality of the AD9856 it is helpful to refer to Figure 21, which displays a block diagram of the device architecture. The following is a general description of the device functionality. Later sections will detail each of the data path building blocks.

Modulation Mode Operation

The AD9856 accepts 12-bit data words, which are strobed into the Data Assembler via an internal clock. The input, TxENABLE, serves as the "valve" which allows data to be accepted or ignored by the Data Assembler. The user has the option to feed the 12-bit data words to the AD9856 as single 12-bit words, dual 6-bit words, or quad 3-bit words. This provides the user with the flexibility to use fewer interface pins, if so desired. Furthermore, the incoming data is assumed to be complex, in that alternating 12-bit words are regarded as the inphase (I) and quadrature (Q) components of a symbol.

The rate at which the 12-bit words are presented to the AD9856 will be referred to as the Input Sample Rate (f_{IN}). It should be pointed out that f_{IN} is not the same as the baseband data rate provided by the user. As a matter of fact, it is required that the user's baseband data be upsampled by at least a factor of two (2) before being applied to the AD9856 in order to minimize the frequency-dependent attenuation associated with the CIC filter stage (detailed in a later section).

The Data Assembler splits the incoming data word pairs into separate I/Q data streams. The rate at which the I/Q data word pairs appear at the output of the Data Assembler will be referred to as the I/Q Sample Rate (f_{IQ}). Since two 12-bit input data words are used to construct the individual I and Q data paths, it should be apparent that the input sample rate is twice the I/Q sample rate (i.e., $f_{IN} = 2 \times f_{IQ}$).

Once through the Data Assembler, the I/Q data streams are fed through two half-band filters (half-band filters #1 and #2). The combination of these two filters results in a factor of four (4) increase of the sample rate. Thus, at the output of half-band filter #2, the sample rate is $4 \times f_{IQ}$. In addition to the sample rate increase, the half-band filters provide the low-pass filtering characteristic necessary to suppress the spectral images produced by the upsampling process. Further upsampling is available via an optional third half-band filter (half-band filter #3). When selected, this provides an overall upsampling factor of eight (8). Thus, if half-band filter #3 is selected, then the sample rate at its output is $8 \times f_{IQ}$.

After passing through the half-band filter stages, the I/Q data streams are fed to a Cascaded Integrator-Comb (CIC) filter. This filter is configured as an interpolating filter, which allows further upsampling rates of any integer value between 2 and 63, inclusive. The CIC filter, like the half-bands, has a built-in low-pass characteristic. Again, this provides for suppression of the spectral images produced by the upsampling process.

The digital quadrature modulator stage following the CIC filters is used to frequency shift the baseband spectrum of the incoming data stream up to the desired carrier frequency (this process is known as *upconversion*). The carrier frequency is controlled numerically by a Direct Digital Synthesizer (DDS). The DDS uses its internal reference clock (SYSCLK) to generate the desired carrier frequency with a high degree of precision. The carrier is applied to the I and Q multipliers in quadrature fashion (90° phase offset) and summed to yield a data stream that is the modulated carrier. It should be noted at this point that the incoming data has been converted from an input sample rate of f_{IN} to an output sample rate of SYSCLK (see the block diagram).

The sampled carrier is ultimately destined to serve as the input data to the digital-to-analog converter (DAC) integrated on the AD9856. The DAC output spectrum is distorted due to the intrinsic zero-order hold effect associated with DAC-generated signals. This distortion is deterministic, however, and follows the familiar SIN(x)/x (or SINC) envelope. Since the SINC distortion is predictable, it is also correctable. Hence, the presence of the optional Inverse SINC filter preceding the DAC. This is a FIR filter, which has a transfer function conforming to the inverse of the SINC response. Thus, when selected, it modifies the incoming data stream so that the SINC distortion, which would otherwise appear in the DAC output spectrum is virtually eliminated.

As mentioned earlier, the output data is sampled at the rate of SYSCLK. Since the AD9856 is designed to operate at SYSCLK frequencies up to 200 MHz, there is the potential difficulty of trying to provide a stable input clock (REFCLK). Although stable, high frequency oscillators are available commercially they tend to be cost prohibitive. To alleviate this problem, the AD9856 has a built-in programmable clock multiplier circuit. This allows the user to use a relatively low frequency (thus, less expensive) oscillator to generate the REFCLK signal. The low frequency REFCLK signal can then be multiplied in frequency by an integer factor of between 4 and 20, inclusive, to become the SYSCLK signal.

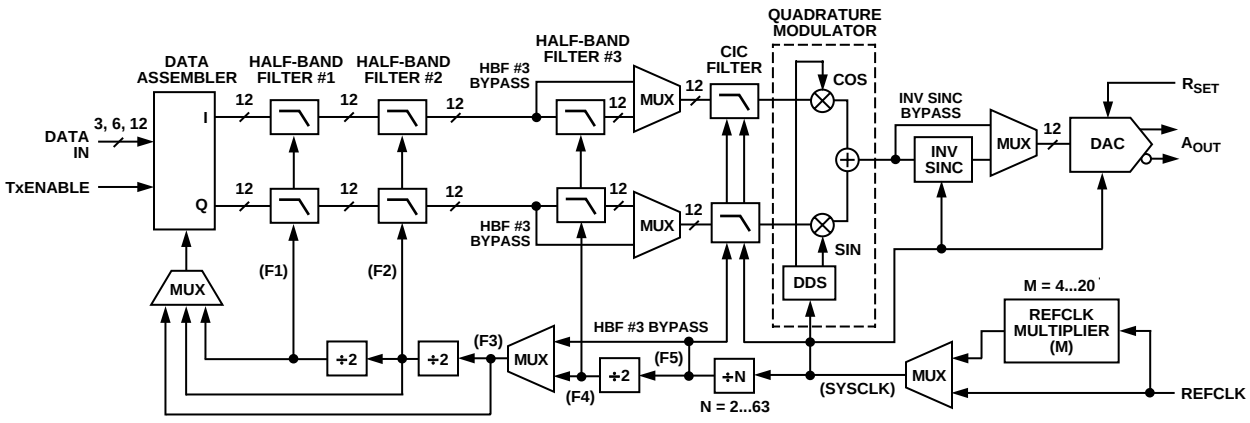


Figure 21. AD9856 Block Diagram

Single Tone Output Operation
The AD9856 can be configured for frequency synthesis applications by writing the single tone bit true. In single tone mode, the AD9856 disengages the modulator and preceding datapath logic to output a spectrally pure single frequency sine wave. The AD9856 provides for a 32-bit frequency tuning word, which results in a tuning resolution of 0.046 Hz at a SYSCLK rate of 200 MHz.

A good rule of thumb when using the AD9856 as a frequency synthesizer is to limit the fundamental output frequency to 40% of SYSCLK. This avoids generating aliases too close to the desired fundamental output frequency, thus minimizing the cost of filtering the aliases.

All applicable programming features of the AD9856 apply when configured in single tone mode. These features include:

1. Frequency hopping via the PROFILE inputs and associated tuning word, which allows Frequency Shift Keying (FSK) modulation.
2. Ability to bypass the REFCLK Multiplier, which results in lower phase noise and reduced output jitter.
3. Ability to bypass the SIN(x)/x compensation filter.
4. Full power-down mode.

INPUT WORD RATE (f_W) vs. REFCLK RELATIONSHIP
There is a fundamental relationship between the input word rate (f_W) and the frequency of the clock that serves as the timing source for the AD9856 (REFCLK). f_W is defined as the rate at which K-bit data words (K = 3, 6 or 12) are presented to the AD9856. There are, however, a number of factors that affect this relationship. They are:

- The interpolation rate of the CIC filter stage.
- Whether or not Half-Band Filter #3 is bypassed.
- The value of REFCLK Multiplier (if selected).
- Input Word Length.

This relationship can be summed up with the following equation:

$$REFCLK = (2\ HNf_W)/MI$$

Where *H*, *N*, *I* and *M* are integers and are determined as follows:

H = | 1: Half-Band Filter #3 Bypassed
| 2: Half-Band Filter #3 Enabled

M = | 1: REFCLK Multiplier Bypassed
| 4 ≤ M ≤ 20: REFCLK Multiplier Enabled

I = | 1: Full Word Input Format
| 2: Half Word Input Format
| 4: Quarter Word Input Format

N = CIC interpolation rate (2 ≤ N ≤ 63)

It should be obvious from these conditions that REFCLK and f_W have an integer ratio relationship. It is of utmost importance that the user chooses a value of REFCLK, which will ensure that this integer ratio relationship is maintained.

I/Q DATA SYNCHRONIZATION
As mentioned above, the AD9856 accepts I/Q data pairs, twos complement numbering system, in three different word length modes. The full word mode accepts 12-bit parallel I and Q data. The half word mode accepts dual 6-bit I and Q data inputs to form a 12-bit word. The quarter word mode accepts multiple 3-bit I and Q data inputs to form a 12-bit word. For all word length modes, the AD9856 assembles the data for signal processing into time aligned, parallel 12-bit I/Q pairs. In addition to the word length flexibility, the AD9856 operates in two "input timing" modes, burst or continuous, programmable via the serial port.

For burst mode input timing, no external data clock needs to be provided as the data is oversampled at the D<11:0> pins using the system clock (SYSCLK). The TxENABLE pin is required to frame the data burst as the rising edge of TxENABLE is used to synchronize the AD9856 to the input data rate. The AD9856 registers the input data at the approximate center of the data valid time. It should be obvious that for larger CIC interpolation rates, more SYSCLK cycles are available to oversample the input data, maximizing clock jitter tolerances.

For continuous mode input timing, the TxENABLE pin can be thought of as a data input clock running at 1/2 the input sample rate ($f_W/2$). In addition to synchronization, for continuous mode timing, the TxENABLE input indicates to the AD9856 whether an I or Q input is being presented to the D<11:0> pins. It is intended that data is presented in alternating fashion such that I data is followed by Q data. Stated another way, the TxENABLE pin should maintain approximately a 50/50 duty cycle. As in burst mode, the rising edge of TxENABLE synchronizes the AD9856 to the input data rate and the data is registered at the approximate center of the data valid time. The continuous operating mode can only be used in conjunction with the full word input format.

Burst Mode Input Timing
Figures 22–26 describe the input timing relationship between TxENABLE and the 12-bit input data word for all three input format modes when the AD9856 is configured for burst input timing. Also shown in these diagrams is the time-aligned, 12-bit parallel I/Q data as assembled by the AD9856.

Figure 22 describes the classic burst mode timing, for full word input mode, in which TxENABLE frames the input data stream. Note that sequential input of alternating I/Q data, starting with I data, is required.

The input sample rate for full word mode, when the third halfband filter is engaged, is given by:

$$f_{IN} = SYSCLK/4N$$

where *N* is the CIC interpolation rate.

The input sample rate for full word mode, when the third halfband filter is not engaged is given by:

$$f_{IN} = SYSCLK/2N$$

where *N* is the CIC interpolation rate

Figure 23 describes an alternate timing method for TxENABLE when the AD9856 is configured in full word, burst mode operation. The benefit of this timing is that the AD9856 will resynchronize the input sampling logic when the rising edge of TxENABLE is detected. The low time on TxENABLE is limited to one input sample period and must be low during the Q data period. The maximum high time on TxENABLE is unlimited. It should be clear that unlimited high time on TxENABLE results in the timing diagram of Figure 22. See Figure 26 for the ramifications of violating the TxENABLE low time constraint when operating in burst mode.

Figure 24 describes the input timing for half word mode, burst input timing operation.

In half word mode, data is input on the D<11:6> inputs. The D<5:0> inputs are unused in this mode and should be tied to DGND or DVDD. The AD9856 expects the data to be input in the following manner: I<11:6>,I<5:0>,Q<11:6>,Q<5:0>. Data is twos complement, the sign bit is D<11> in notation I<11:0>,Q<11:0>.

The input sample rate for half word mode, when the third half-band filter is engaged, is given by:

$$f_{IN} = SYSCLK/2N$$

where N is the CIC interpolation rate.

The input sample rate for half word mode, when the third half-band filter is not engaged is given by:

$$f_{IN} = SYSCLK/N$$

where N is the CIC interpolation rate.

Figure 25 describes the input timing for quarter word, burst input timing operation.

In quarter word mode, data is input on the D<11:9> inputs. The D<8:0> inputs are unused in this mode and should be tied to DGND or DVDD. The AD9856 expects the data to be input in the following manner: I<11:9>, I<8:6>, I<5:3>, I<2:0>, Q<11:9>, Q<8:6>, Q<5:3>, Q<2:0>. Data is twos complement, the sign bit is D<11> in notation I<11:0>, Q<11:0>.

The input sample rate for quarter word mode, when the third half-band filter is engaged, is given by:

$$f_{IN} = SYSCLK/N$$

where N is the CIC interpolation rate.

Please note that Half-Band Filter #3 must be engaged when operating in quarter word mode.

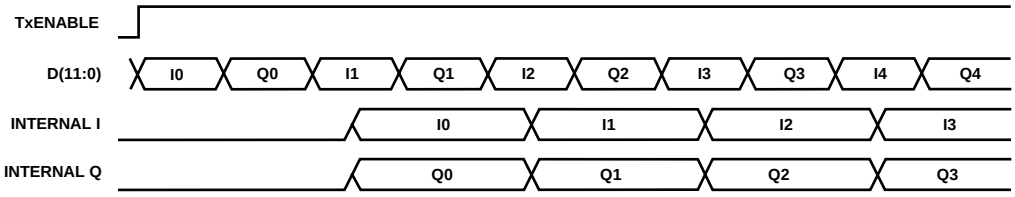


Figure 22. 12-Bit Input Mode, Classic Burst Timing

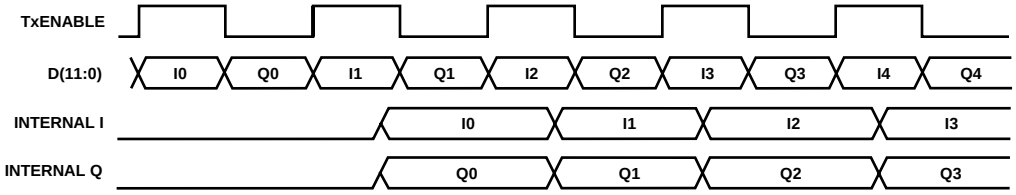


Figure 23. 12-Bit Input Mode, Alternate TxENABLE Timing

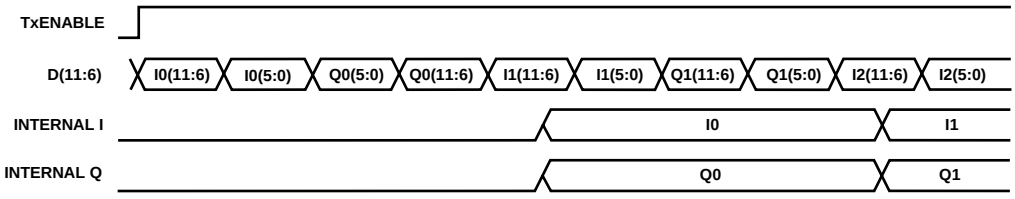


Figure 24. 6-Bit Input Mode, Burst Mode Timing

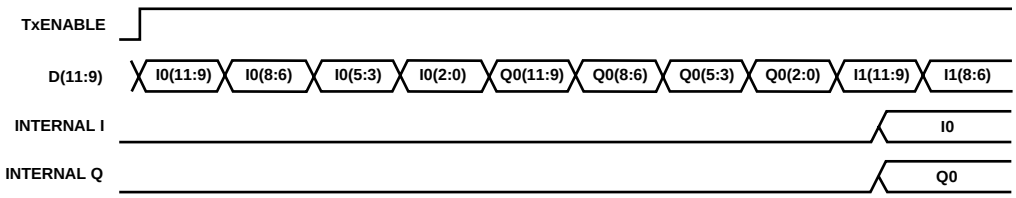


Figure 25. 3-Bit Input Mode, Burst Mode Timing

Figure 26 describes the end of burst timing and internal data assembly. It's important to note that in burst mode operation, if the TxENABLE input is low for more than one input sample period, numerical zeros are internally generated and passed to the data path logic for signal processing. This is not valid for continuous mode operation, as will be discussed later.

To ensure proper operation, the minimum time between falling and rising edges of TxENABLE is one input sample period.

Continuous Mode Input Timing

The AD9856 is configured for continuous mode input timing by writing the Continuous Mode bit true (Logic 1). The Continuous Mode bit is in register address 01h, Bit 6. The AD9856 must be configured for full word input format when operating in continuous mode input timing. The input data rate equations described above, for full word mode, apply for continuous mode. Figure 23, which is the alternate burst mode timing diagram, is also the continuous mode input timing. Figures 27 and 28 describe what the internal data assembler will present to the signal processing logic when the TxENABLE input is held static for greater than one input sample period. Please note that the timing diagram of Figures 27 and 28 detail INCORRECT timing relationships between TxENABLE and data. They are only presented to indicate that the AD9856 will resynchronize properly after detecting a rising edge of TxENABLE. It should also be noted that the significant difference between burst and continuous mode operation is that in addition to synchronizing the data, TxENABLE is used to indicate whether an I or Q input is being sampled.

Do not engage continuous mode simultaneously with the REFCLK multiplier function. This has been found to corrupt the CIC interpolating filter, forcing *unrecoverable* mathematical overflow that can only be resolved by issuing a RESET command. The problem is due to the PLL failing to be locked to the reference clock while nonzero data is being clocked into the interpolation stages from the data inputs. The recommended sequency is to first engage the REFCLK multiplier function (allowing at least 1 ms for loop stabilization) and then engage continuous mode via software.

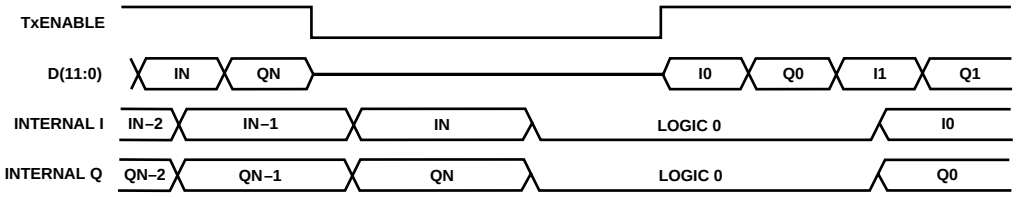


Figure 26. Burst Mode Input Timing—End of Burst

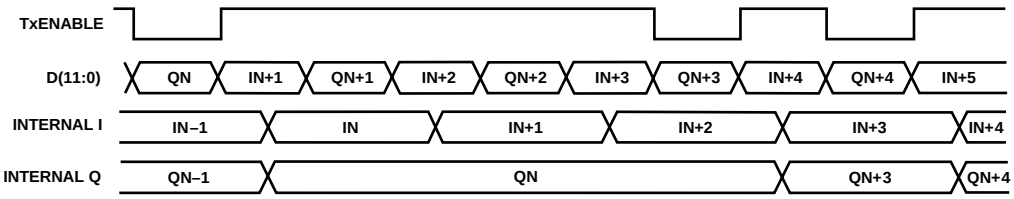


Figure 27. Continuous Mode Input Timing—TxENABLE Static High

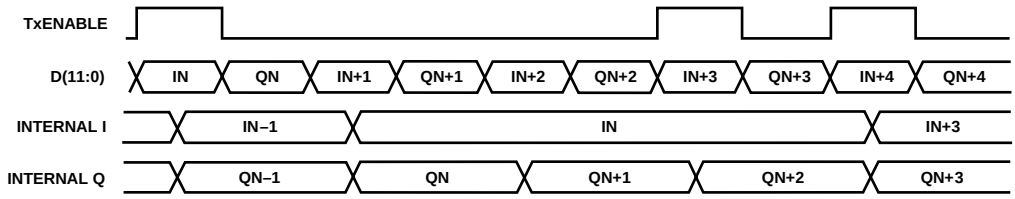


Figure 28. Continuous Mode Input Timing—TxENABLE Static Low

HALF-BAND FILTERS (HBFs)

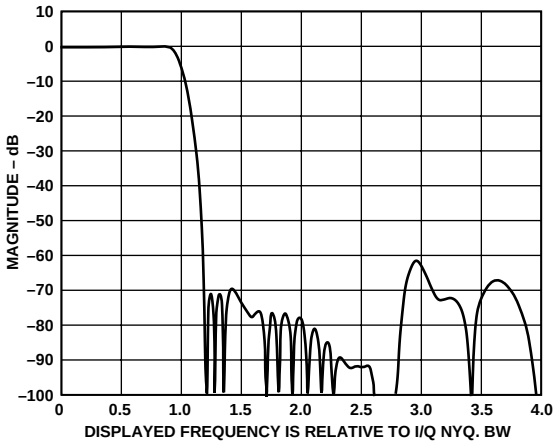
Before presenting a detailed description of the HBFs, recall that the input data stream is representative of complex data; i.e., two input samples are required to produce one I/Q data pair. The I/Q sample rate is one-half the input data rate. The I/Q sample rate (the rate at which I or Q samples are presented to the input of the first half-band filter) will be referred to as f_{IQ}. Since the AD9856 is a quadrature modulator, f_{IQ} represents the baseband of the internal I/Q sample pairs. It should be emphasized here that f_{IQ} is not the same as the baseband of the user's symbol rate data, which must be upsampled before presentation to the AD9856 (as will be explained later). The I/Q sample rate (f_{IQ}) puts a limit on the minimum bandwidth necessary to transmit the f_{IQ} spectrum. This is the familiar Nyquist limit and is equal to one-half f_{IQ}, which hereafter will be referred to as f_{NYQ}.

HBF 1 is a 47-tap filter that provides a factor-of-two increase in sampling rate. HBF 2 is a 15-tap filter offering an additional factor-of-two increase in sampling rate. Together, HBF 1 and 2 provide a factor-of-four increase in the sampling rate ($4 \times f_{IQ}$ or $8 \times f_{NYQ}$). Their combined insertion loss is a mere 0.01 dB, so virtually no loss of signal level occurs through the first two HBFs. HBF 3 is an 11-tap filter and, if selected, increases the sampling rate by an additional factor of two. Thus, the output sample rate of HBF 3 is $8 \times f_{IQ}$ or $16 \times f_{NYQ}$. HBF 3 exhibits 0.03 dB of signal level loss. As such, the loss in signal level through all three HBFs is only 0.04 dB and may be ignored for all practical purposes.

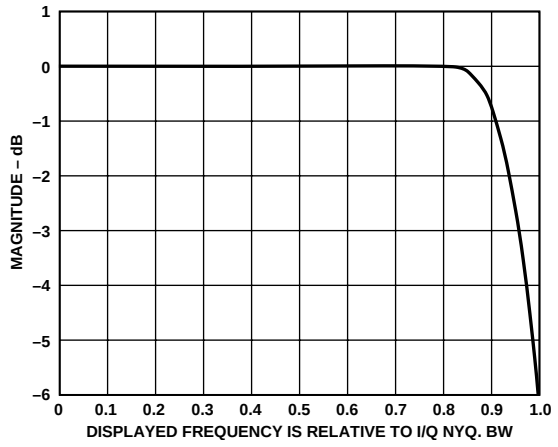
In relation to phase response, all three HBFs are linear phase filters. As such, virtually no phase distortion is introduced within the passband of the filters. This is an important feature as phase distortion is generally intolerable in a data transmission system.

In addition to knowledge of the insertion loss and phase response of the HBFs, some knowledge of the frequency response of the HBFs is useful as well. The combined frequency response of HBF 1 and 2 is shown in Figure 29.

The usable bandwidth of the filter chain puts a limit on the maximum data rate that can be propagated through the AD9856. A look at the passband detail of the HBF 1 and 2 response indicates that in order to maintain an amplitude error of no more than 1 dB, we are restricted to signals having a bandwidth of no more than about 90% of f_{NYQ}. Thus, in order to keep the bandwidth of the data in the flat portion of the filter passband, the user must oversample the baseband data by at least a factor of two prior to presenting it to the AD9856. Note that without oversampling, the Nyquist bandwidth of the baseband data corresponds to the f_{NYQ}. As such, the upper end of the data bandwidth will suffer 6 dB or more of attenuation due to the frequency response of HBF 1 and 2. Furthermore, if the baseband data applied to the AD9856 has been pulse shaped there is an additional concern. Typically, pulse shaping is applied to the baseband data via a filter having a raised cosine response. In such cases, an α value is used to modify the bandwidth of the data where the value of α is such that $0 \le \alpha \le 1$. A value of 0 causes the data bandwidth to correspond to the Nyquist bandwidth. A value of 1 causes the data bandwidth to be extended to twice the Nyquist bandwidth. Thus, with 2× oversampling of the baseband data and $\alpha = 1$, the Nyquist bandwidth of the data will correspond with the I/Q Nyquist bandwidth. As stated earlier, this results in problems near the upper edge of the data bandwidth due to the frequency response of HBF 1 and 2.



a. Half-Band 1 and 2 Frequency Response

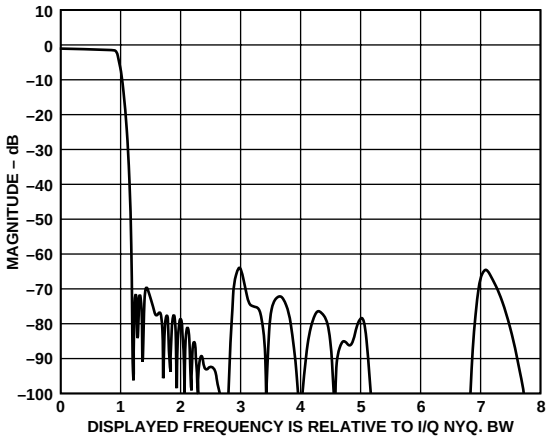


b. Passband Detail

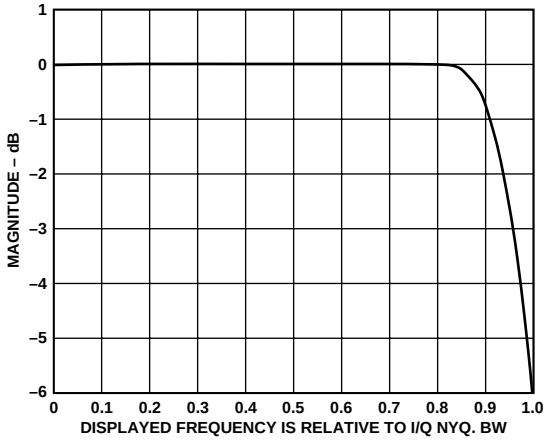
Figure 29. Combined Frequency Response of HBF 1 and 2

To reiterate, the user must *oversample* their baseband data by at least a *factor of two* (2). In addition, there is a further restriction on pulse shaping. That is, the maximum value of α that can be implemented is 0.8. This is because the data bandwidth becomes: $1/2(1 + \alpha)\ f_{NYQ} = 0.9\ f_{NYQ}$, which puts the data bandwidth at the extreme edge of the flat portion of the filter response. If a particular application requires an α value between 0.8 and 1, then the user must *oversample* the baseband data by at least a *factor of four* (4).

In applications requiring both a low data rate and a high output sample rate, a third HBF is available (HBF 3). Selection of HBF 3 offers an upsampling ratio of eight (8) instead of four (4). The combined frequency response of HBF 1, 2 and 3 is shown in Figure 30. Comparing the passband detail of HBF 1 and 2 with the passband detail of HBF 1, 2 and 3, it becomes evident that HBF 3 has virtually no impact on frequency response from 0 to 1 (where 1 corresponds to f_{NYQ}).



a. Half-Band 1, 2 and 3 Frequency Response



b. Passband Detail

Figure 30. Combined Frequency Response of HBF 1, 2 and 3

CASCADED INTEGRATOR-COMB (CIC) FILTER

A CIC filter is unlike a typical FIR filter in that it offers the flexibility to handle differing input and output sample rates (only in integer ratios, however). In the purest sense, a CIC filter can provide either an increase or a decrease in sample rate at the output relative to the input, depending on the architecture. If the integration stage precedes the comb stage, the CIC filter provides sample rate reduction (*decimation*). When the comb stage precedes the integrator stage the CIC filter provides an increase in sample rate (*interpolation*). In the AD9856, the CIC filter is configured as an interpolator. In fact, it is a programmable interpolator and provides a sample rate increase, R, such that $2 \le R \le 63$.

In addition to the ability to provide a change in sample rate between input and output, a CIC filter also has an intrinsic low-pass frequency response characteristic. The frequency response of a CIC filter is dependent on three factors:

1. The rate change ratio, R.
2. The order of the filter, N.
3. The number of unit delays per stage, M.

It can be shown that the system function, H(z), of a CIC filter is given by:

$$H(z)=\left(\frac{1-z^{-RM}}{1-z^{-1}}\right)^{N}=\left(\sum_{k=0}^{RM-1} z^{-k}\right)^{N}$$

The form on the far right has the advantage of providing a result for z = 1 (corresponding to zero frequency or dc). The alternate form yields an indeterminate form (0/0) for z = 1, but is otherwise identical. The only variable parameter for the AD9856's CIC filter is R. M and N are fixed at 1 and 4, respectively. Thus, the CIC system function for the AD9856 simplifies to:

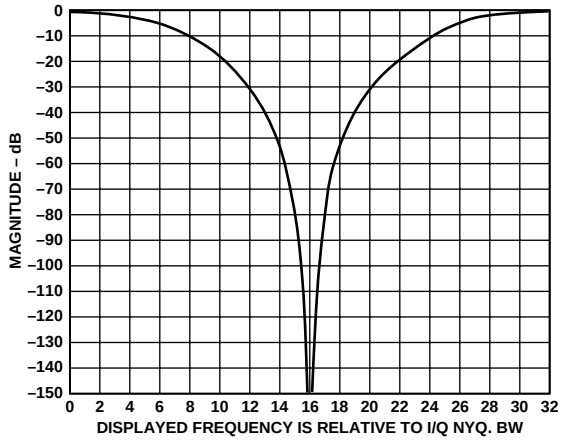
$$H(z)=\left(\frac{1-z^{-R}}{1-z^{-1}}\right)^{4}=\left(\sum_{k=0}^{R-1} z^{-k}\right)^{4}$$

The transfer function is given by:

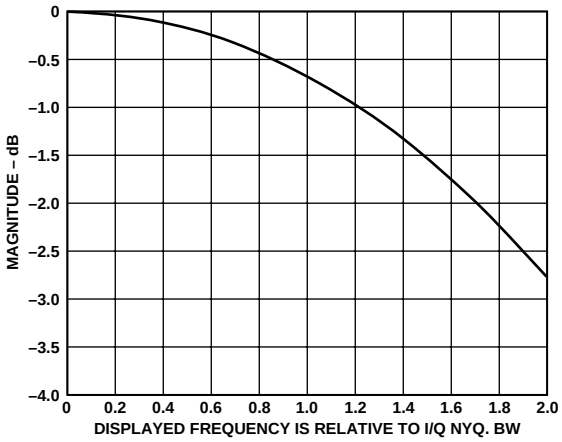
$$H(f)=\left(\frac{1-e^{-j(2\pi fR)}}{1-e^{-j(2\pi f)}}\right)^{4}=\left(\sum_{k=0}^{R-1} e^{-j(2\pi fk)}\right)^{4}$$

The frequency response in this form is such that f is scaled to the output sample rate of the CIC filter. That is, f = 1 corresponds to the frequency of the output sample rate of the CIC filter. H(f/R) will yield the frequency response with respect to the input sample of the CIC filter. Figure 31 reveals the CIC frequency response and passband detail for R = 2 and R = 63 and with HBF 3 bypassed. Figure 32 is similar but with HBF 3 selected. Note the flatter passband response when HBF 3 is employed.

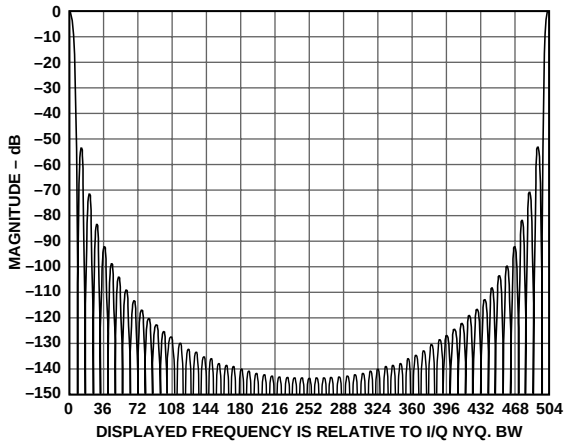
As with the case of the HBFs, consideration must be given to the frequency dependent attenuation that the CIC filter introduces over the frequency range of the data to be transmitted. Note that the CIC frequency response plots have f_{NYQ} as their reference frequency; i.e., unity (1) on the frequency scale corresponds to f_{NYQ}. If the incoming data that is applied to the AD9856 is oversampled by a factor of 2 (as required), then the Nyquist bandwidth of the applied data is one-half f_{NYQ} on the CIC frequency response plots. A look at the 0.5 point on the passband detail plots reveals a worst case attenuation of about 0.25 dB (HBF 3 bypassed, R = 63). This, of course, assumes pulse shaped data with $\alpha = 0$ (minimum bandwidth scenario). When a value of $\alpha = 1$ is used, the bandwidth of the data corresponds to f_{NYQ} (the point, 1.0 on the CIC frequency scale). Thus, the worst case attenuation for $\alpha = 1$ is about 0.9 dB.



a. CIC Frequency Response (R = 2, HBF 3 Bypass)



c. Passband Detail (R = 2, HBF 3 Bypass)



b. CIC Frequency Response (R = 63, HBF 3 Bypass)



d. Passband Detail (R = 63, HBF 3 Bypass)

Figure 31. CIC Filter Frequency Response (HB 3 Bypassed and R = 2, 63)

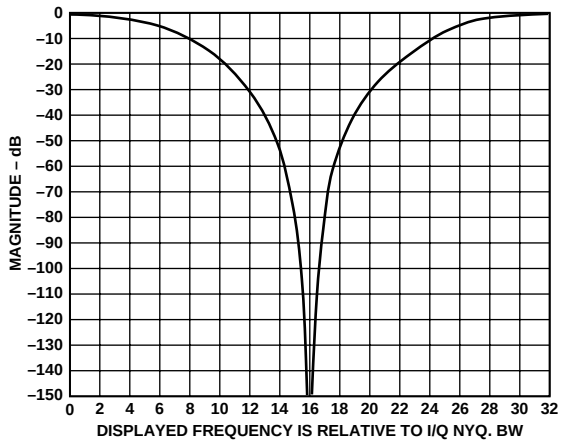
The degree of the impact of the attenuation introduced by the CIC filter over the Nyquist bandwidth of the data is application specific. The user must decide how much attenuation is acceptable. If less attenuation is desired, then additional oversampling of the baseband data must be employed. Alternatively, the user can precompensate the baseband data before presenting it to the AD9856. That is, if the data is precompensated through a filter that has a frequency response characteristic, which is the inverse of the CIC filter response, then the overall system response can be nearly perfectly flattened over the bandwidth of the data.

Another issue to consider with the CIC filters is insertion loss. Unfortunately, CIC insertion loss is not fixed but is a function of R, M and N. Since M and N are fixed for the AD9856, the CIC insertion loss is a function of R, only.

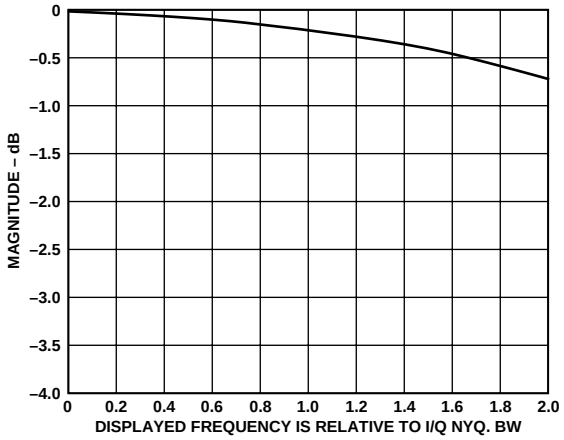
Interpolation rates that are an integer power-of-2 result in no insertion loss. However, all noninteger power-of-2 interpolation rates result in a specific amount of insertion loss.

To help overcome the insertion loss problem, the AD9856 provides the user a means to boost the gain through the CIC stage by a factor of 2 (via the CIC Gain bit—see the AD9856 control register description). The reason for this feature is to allow the user to take advantage of the full dynamic range of the DAC, thus maximizing the signal-to-noise ratio (SNR) at the output of the DAC stage. Obviously, it is desirable to operate the DAC over its full-scale range in order to minimize the inherent quantization effects associated with a DAC. Any significant loss through the CIC stage will be reflected at the DAC output as a reduction in SNR. The degradation in SNR can be overcome by boosting the CIC output level. Table II (The CIC Interpolation Filter Insertion Loss Table) tabulates insertion loss as a function of R. The values are provided in linear and decibel form, both with and without the factor-of-two gain employed.

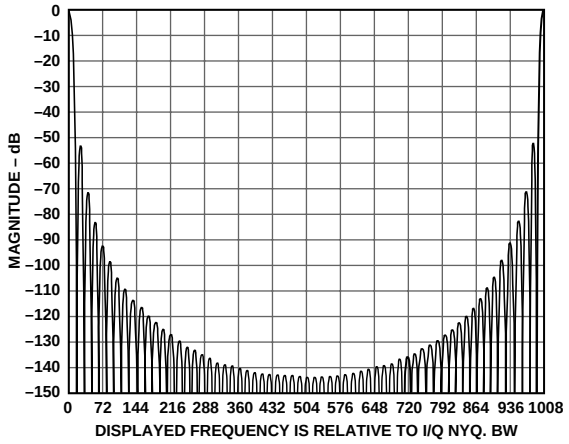
A word of caution: When the CIC Gain bit is active, the user must ensure that the data supplied to the AD9856 is scaled down to yield an overall gain of unity (1) through the CIC filter stage. Gains in excess of unity are likely to cause overflow errors in the data path, thereby compromising the validity of the analog output signal.



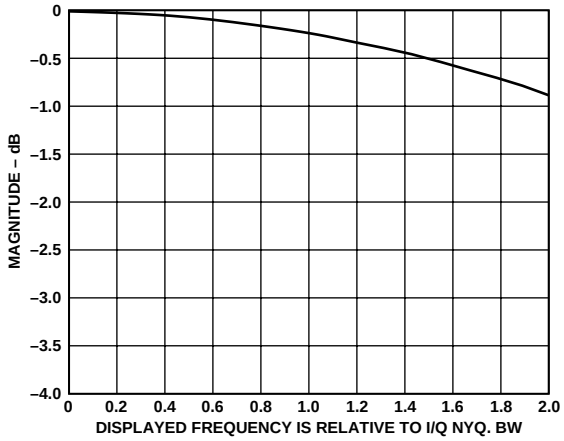
a. CIC Frequency Response (R = 2, HBF 3 Selected)



c. Passband Detail (R = 2, HBF 3 Selected)



b. CIC Frequency Response (R = 63, HBF 3 Active)



d. Passband Detail (R = 63, HBF 3 Active)

Figure 32. CIC Filter Frequency Response (HB 3 Selected and R = 2, 63)

DIGITAL QUADRATURE MODULATOR

Following the CIC filter stage the I and Q data (which have been processed independently up to this point) are mixed in the modulator stage to produce a digital modulated carrier. The carrier frequency is selected by programming the direct digital synthesizer (see the DDS section) with the appropriate 32-bit tuning word via the AD9856 control registers. The DDS simultaneously generates a digital (sampled) sine and cosine wave at the programmed carrier frequency. The digital sine and cosine data is multiplied by the Q and I data, respectively, to create the quadrature components of the original data upconverted to the carrier frequency. The quadrature components are digitally summed and passed on to the subsequent stages.

The key point is that the modulation is done digitally, which eliminates the phase and gain imbalance and crosstalk issues typically associated with analog modulators. Note that the modulated "signal" is actually a number stream sampled at the rate of SYSCLK, which is the same rate at which the DAC is clocked (see Figure 21, the AD9856 block diagram).

It should be pointed out that the architecture of the quadrature modulator results in a 3 dB loss of signal level. To visualize this, assume that both the I data and Q data are fixed at the maximum possible digital value, x. Then the output of the modulator, y, is:

$$y = x \times \cos(\omega) + x \times \sin(\omega) = x \times [\cos(\omega) + \sin(\omega)]$$

From this equation it can be shown that y assumes a maximum value of $x\sqrt{2}$ (a gain of 3 dB). However, if the same number of bits were used to represent the y values, as is used to represent the x values, an overflow would occur. To prevent this possibility, an effective "divide-by-two" is implemented on the y values, which reduces the maximum value of y by a factor of two. Since division by two results in a 6 dB loss, the modulator yields an overall loss of 3 dB (3 dB – 6 dB = –3 dB, or 3 dB of loss).

Table II. CIC Interpolation Filter Insertion Loss Table

Interpolation Rate	Default Gain		2× Gain	
	(Linear)	(dB)	(Linear)	(dB)
2	1.0000	0.000	2.0000	6.021
3	0.8438	–1.476	1.6875	4.545
4	1.0000	0.000	2.0000	6.021
5	0.9766	–0.206	1.9531	5.815
6	0.8438	–1.476	1.6875	4.545
7	0.6699	–3.480	1.3398	2.541
8	1.0000	0.000	2.0000	6.021
9	0.7119	–2.951	1.4238	3.069
10	0.9766	–0.206	1.9531	5.815
11	0.6499	–3.743	1.2998	2.278
12	0.8438	–1.476	1.6875	4.545
13	0.5364	–5.411	1.0728	0.610
14	0.6699	–3.480	1.3398	2.541
15	0.8240	–1.682	1.6479	4.339
16	1.0000	0.000	2.0000	6.021
17	0.5997	–4.441	1.1995	1.580
18	0.7119	–2.951	1.4238	3.069
19	0.8373	–1.543	1.6746	4.478
20	0.9766	–0.206	1.9531	5.815
21	0.5652	–4.955	1.1305	1.065
22	0.6499	–3.743	1.2998	2.278
23	0.7426	–2.585	1.4852	3.436
24	0.8438	–1.476	1.6875	4.545
25	0.9537	–0.412	1.9073	5.609
26	0.5364	–5.411	1.0728	0.610
27	0.6007	–4.427	1.2014	1.593
28	0.6699	–3.480	1.3398	2.541
29	0.7443	–2.565	1.4886	3.455
30	0.8240	–1.682	1.6479	4.339
31	0.9091	–0.827	1.8183	5.193
32	1.0000	0.000	2.0000	6.021
33	0.5484	–5.219	1.0967	0.802
34	0.5997	–4.441	1.1995	1.580
35	0.6542	–3.686	1.3084	2.335
36	0.7119	–2.951	1.4238	3.069
37	0.7729	–2.237	1.5458	3.783
38	0.8373	–1.543	1.6746	4.478
39	0.9051	–0.866	1.8103	5.155
40	0.9766	–0.206	1.9531	5.815
41	0.5258	–5.583	1.0517	0.437
42	0.5652	–4.955	1.1305	1.065
43	0.6066	–4.342	1.2132	1.679
44	0.6499	–3.743	1.2998	2.278
45	0.6952	–3.157	1.3905	2.863
46	0.7426	–2.585	1.4852	3.436
47	0.7921	–2.024	1.5842	3.996
48	0.8438	–1.476	1.6875	4.545
49	0.8976	–0.938	1.7952	5.082
50	0.9537	–0.412	1.9073	5.609
51	0.5060	–5.917	1.0120	0.104
52	0.5364	–5.411	1.0728	0.610
53	0.5679	–4.914	1.1358	1.106
54	0.6007	–4.427	1.2014	1.593
55	0.6347	–3.949	1.2693	2.072
56	0.6699	–3.480	1.3398	2.541
57	0.7065	–3.018	1.4129	3.002
58	0.7443	–2.565	1.4886	3.455
59	0.7835	–2.120	1.5669	3.901
60	0.8240	–1.682	1.6479	4.339
61	0.8659	–1.251	1.7317	4.770
62	0.9091	–0.827	1.8183	5.193
63	0.9539	–0.410	1.9077	5.610

INVERSE SINC FILTER (ISF)

The AD9856 is almost entirely a digital device. The input "signal" is made up of a time series of digital data words. These data words propagate through the device as numbers. Ultimately, this number stream must be converted to an analog signal. To this end, the AD9856 incorporates an integrated DAC. The output waveform of the DAC is the familiar "staircase" pattern typical of a signal that is sampled and quantized. The staircase pattern is a result of the finite time that the DAC holds a quantized level until the next sampling instant. This is known as a zero-order hold function. The spectrum of the zero-order hold function is the familiar SIN(x)/x, or SINC, envelope.

The series of digital data words presented at the input of the DAC represent an impulse stream. It is the spectrum of this impulse stream, which is the desired output signal. Due to the zero-order hold effect of the DAC, however, the output spectrum is the product of the zero-order hold spectrum (the SINC envelope) and the Fourier transform of the impulse stream. Thus, there is an intrinsic distortion in the output spectrum, which follows the SINC response.

The SINC response is deterministic and totally predictable. Thus, it is possible to pre-distort the input data stream in a manner, which compensates for the SINC envelope distortion. This can be accomplished by means of an ISF. The ISF incorporated on the AD9856 is a 17-tap, linear phase FIR filter. Its frequency response characteristic is the inverse of the SINC envelope. Data sent through the ISF is altered in such a way as to correct for the SINC envelope distortion.

It should be noted, however, that the ISF is sampled at the same rate as the DAC. Thus, the effective range of the SINC envelope compensation only extends to the Nyquist frequency (1/2 of the DAC sample rate).

Figure 33 is a plot that shows the effectiveness of the ISF in correcting for the SINC distortion. The plot includes a graph of the SINC envelope, the ISF response and the SYSTEM response (which is the product of the SINC and ISF responses). It should be mentioned at this point that the ISF exhibits an insertion loss of 3.1 dB. Thus, signal levels at the output of the AD9856 with the ISF bypassed are 3.1 dB higher than with the ISF engaged. However, for modulated output signals, which have a relatively wide bandwidth, the benefits of the SINC compensation usually outweigh the 3 dB loss in output level. The decision of whether or not to use the ISF is an application specific system design issue.

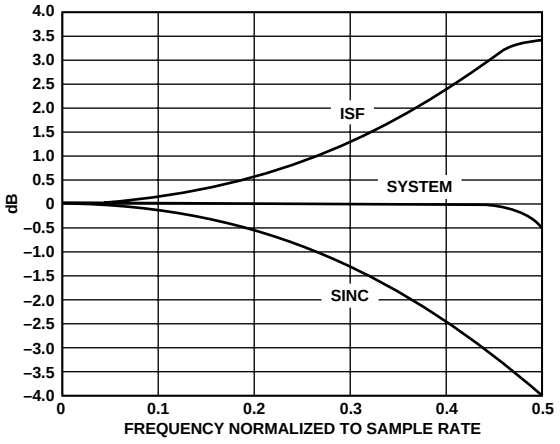


Figure 33. Inverse SINC Filter Response

DIRECT DIGITAL SYNTHESIZER FUNCTION

The direct digital synthesizer (DDS) block generates the sine/cosine carrier reference signals that are digitally modulated by the I/Q data paths. The DDS function is frequency tuned via the serial control port with a 32-bit tuning word. This allows the AD9856's output carrier frequency to be very precisely tuned while still providing output frequency agility.

The equation relating output frequency of the AD9856 digital modulator to the frequency tuning word (FTWORD) and the system clock (SYSCLK) is given as:

$$A_{OUT} = (FTWORD \times SYSCLK)/2^{32}$$

Where: A_{OUT} and *SYSCLK* frequencies are in Hz and *FTWORD* is a decimal number from 0 to 4,294,967,296 (2^{31})

Example: Find the FTWORD for A_{OUT} = 41 MHz and SYSCLK = 122.88 MHz

If A_{OUT} = 41 MHz and SYSCLK = 122.88 MHz, then:

$$FTWORD = 556AAAAB\ hex$$

Loading 556*AAAABh* into control bus registers 02h–05h (for Profile 1) programs the AD9856 for A_{OUT} = 41 MHz, given a SYSCLK frequency of 122.88 MHz.

D/A CONVERTER

A 12-bit digital-to-analog converter (DAC) is used to convert the digitally processed waveform into an analog signal. The worst case spurious signals due to the DAC are the harmonics of the fundamental signal and their aliases (please see the AD9851 Complete-DDS data sheet for a detailed explanation of aliased images). The wideband 12-bit DAC in the AD9856 maintains spurious-free dynamic range (SFDR) performance of –60 dBc up to A_{OUT} = 42 MHz and –55 dBc up to A_{OUT} = 65 MHz.

The conversion process will produce aliased components of the fundamental signal at n × SYSCLK ± $F_{CARRIER}$ (n = 1, 2, 3). These are typically filtered with an external RLC filter at the DAC output. It is important for this analog filter to have a sufficiently flat gain and linear phase response across the bandwidth of interest so as to avoid modulation impairments. A relatively inexpensive 7th order elliptical low-pass filter is sufficient to suppress the aliased components for HFC network applications.

The AD9856 provides true and complement current outputs on pins 30 and 29 respectively. The full-scale output current is set by the R_{SET} resistor at Pin 25. The value of R_{SET} for a particular I_{OUT} is determined using the following equation:

$$R_{SET} = 39.936/I_{OUT}$$

For example, if a full-scale output current of 20 mA is desired, then R_{SET} = (39.936/0.02), or approximately 2 kΩ. Every doubling of the R_{SET} value will halve the output current. Maximum output current is specified as 20 mA.

The full-scale output current range of the AD9856 is 5 mA–20 mA. Full-scale output currents outside of this range will degrade SFDR performance. SFDR is also slightly affected by output matching, that is, the two outputs should be terminated equally for best SFDR performance.

The output load should be located as close as possible to the AD9856 package to minimize stray capacitance and inductance. The load may be a simple resistor to ground, an op amp current-to-voltage converter, or a transformer-coupled circuit. It is best not to attempt to directly drive highly reactive loads (such as an LC filter). Driving an LC filter without a transformer requires that the filter be doubly terminated for best performance, that is, the filter input and output should both be resistively terminated with the appropriate values. The parallel combination of the two terminations will determine the load that the AD9856 will see for signals within the filter passband. For example, a 50 Ω terminated input/output low-pass filter will look like a 25 Ω load to the AD9856.

The output compliance voltage of the AD9856 is –0.5 V to +1.5 V. Any signal developed at the DAC output should not exceed +1.5 V, otherwise, signal distortion will result. Furthermore, the signal may extend below ground as much as 0.5 V without damage or signal distortion. The use of a transformer with a grounded center-tap for common-mode rejection results in signals at the AD9856 DAC output pins that are symmetrical about ground.

As previously mentioned, by differentially combining the two signals the user can provide some degree of common mode signal rejection. A differential combiner might consist of a transformer or an op amp. The object is to combine or amplify only the difference between two signals and to reject any common, usually undesirable, characteristic, such as 60 Hz hum or "clock feedthrough" that is equally present on both input signals. The AD9856 true and complement outputs can be differentially combined using a broadband 1:1 transformer with a grounded, center-tapped primary to perform differential combining of the two DAC outputs.

REFERENCE CLOCK MULTIPLIER

Due to the fact that the AD9856 is a DDS-based modulator, a relatively high frequency system clock is required. For DDS applications, the carrier is typically limited to about 40% of SYSCLK. For a 65 MHz carrier, the system clock required is above 160 MHz. To avoid the cost associated with these high frequency references, and the noise coupling issues associated with operating a high frequency clock on a PC board, the AD9856 provides an on-chip programmable clock multiplier (REFCLK Multiplier). The available clock multiplier range is from 4× to 20×, in integer steps. With the REFCLK Multiplier enabled, the input reference clock required for the AD9856 can be kept in the 10 MHz to 50 MHz range for 200 MHz system operation, which results in cost and system implementation savings. The REFCLK Multiplier function maintains clock integrity as evidenced by the AD9856's system phase noise characteristics of –105 dBc/Hz (A_{OUT} = 40 MHz, REFCLK Multiplier = 6, Offset = 1 kHz) and virtually no clock-related spurii in the output spectrum. External loop filter components consisting of a series resistor (1.3 kΩ) and capacitor (0.01 μF) provide the compensation zero for the REFCLK Multiplier PLL loop. The overall loop performance has been optimized for these component values.

THROUGHPUT AND LATENCY

Data latency through the AD9856 is easiest to describe in terms of SYSCLK clock cycles. Latency is a function of the AD9856 configuration; primarily affected by the CIC interpolation rate and whether the third half-band filter is engaged.

When the third half-band filter is engaged the AD9856 latency is given by:

$$126\ N + 37\ \textit{SYSCLK clock cycles}$$

where N is the CIC interpolation rate.

If the AD9856 is configured to bypass the third half-band filter, the latency is given by:

$$63\ N + 37\ \textit{SYSCLK clock cycles}.$$

These equations should be considered estimates as observed latency may be data dependent. The latency was calculated using the linear delay model for the FIR filters.

In single tone mode, frequency hopping is accomplished via changing the PROFILE input pins. The time required to switch from one frequency to another is less than 50 SYSCLK cycles with the Inverse SINC Filter engaged. With the Inverse SINC Filter bypassed, the latency drops to less than 35 SYSCLK cycles.

CONTROL INTERFACE

The AD9856 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols.

The interface allows read/write access to all registers that configure the AD9856. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats. The AD9856's serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO).

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a communication cycle with the AD9856. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9856, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9856 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer (1–4), and the starting register address for the first byte of the data transfer.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9856. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9856 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Normally, using one communication cycle in a multibyte transfer is the preferred method. However, single byte communication cycles are useful to reduce CPU overhead when register access requires one byte only. Examples of this may be to write the AD9856 SLEEP bit, or an AD8320/AD8321 gain control byte.

At the completion of any communication cycle, the AD9856 serial port controller expects the next 8 rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9856 is registered on the rising edge of SCLK. All data is driven out of the AD9856 on the falling edge of SCLK.

Figures 34–37 are useful in understanding the general operation of the AD9856 Serial Port.

INSTRUCTION BYTE

The instruction byte contains the following information as shown below (see Table III):

Table III. Instruction Byte Information

MSB	D6	D5	D4	D3	D2	D1	LSB
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

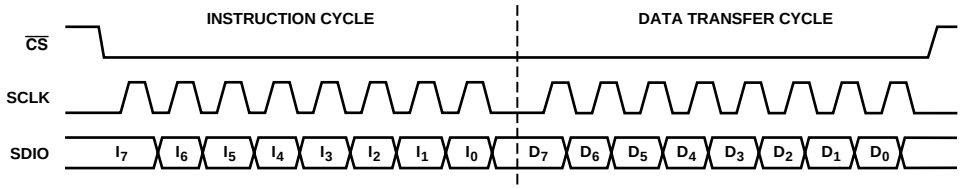


Figure 34. Serial Port Writing Timing—Clock Stall Low

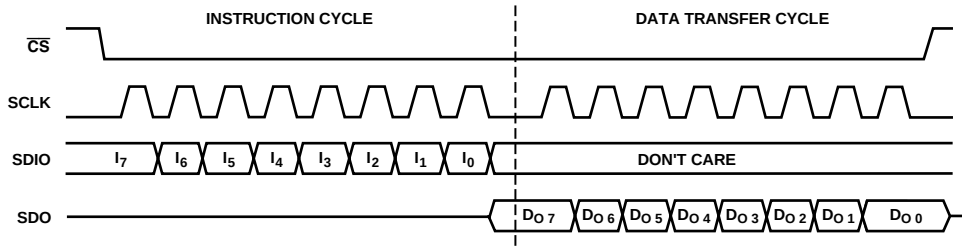


Figure 35. Three-Wire Serial Port Read Timing—Clock Stall Low

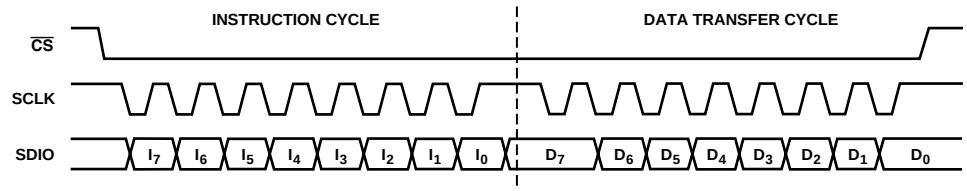


Figure 36. Serial Port Write Timing—Clock Stall High

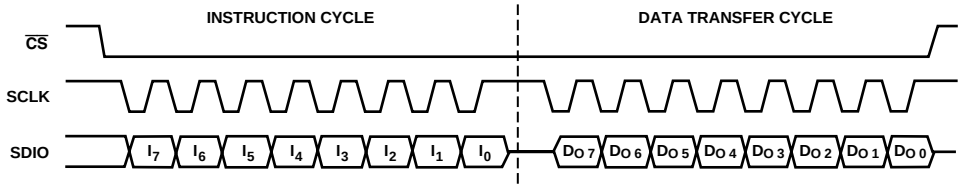


Figure 37. Two-Wire Serial Port Read Timing—Clock Stall High

R/$\overline{W}$–Bit 7 of the instruction byte determines whether a read or write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic zero indicates a write operation.

N1, N0—Bits 6 and 5 of the instruction byte determine the number of bytes to be transferred during the data transfer cycle of the communications cycle. The bit decodes are shown in Table IV.

Table IV. N1, N2 Decode Bits

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

A4, A3, A2, A1, A0—Bits 4, 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9856.

SERIAL INTERFACE PORT PIN DESCRIPTION

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD9856 and to run the internal state machines. SCLK maximum frequency is 10 MHz.

$\overline{CS}$—Chip Select. Active low input that allows more than one device on the same serial communications lines. The SDO and SDIO pins will go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until $\overline{CS}$ is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

SDIO—Serial Data I/O. Data is always written into the AD9856 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 7 of register address 0h. The default is logic zero, which configures the SDIO pin as bidirectional.

SDO—Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9856 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

SYNC I/O—Synchronizes the I/O port state machines without affecting the addressable registers contents. An active high input on the SYNC I/O pin causes the current communication cycle to abort. After SYNC I/O returns low (Logic 0) another communication cycle may begin, starting with the instruction byte write.

CA CLK—Output clock pin to the AD8320/AD8321. If using the AD9856 to control the AD8320/AD8321 Programmable Cable Driver Amplifier, connect this pin to the CLK input of the AD8320/AD8321.

CA DATA—Output data pin to the AD8320/AD8321. If using the AD9856 to control the AD8320/AD8321 Programmable Cable Driver Amplifier, connect this pin to the SDATA input of the AD8320/AD8321.

CA ENABLE—Output Enable pin to the AD8320/AD8321. If using the AD9856 to control the AD8320/AD8321 Programmable Cable Driver Amplifier, connect this pin to the DATAEN input of the AD8320/AD8321.

MSB/LSB TRANSFERS

The AD9856 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the REG0<6> bit. The default value of REG0<6> is low (MSB first). When REG0<6> is set active high, the AD9856 serial port is in LSB first format. The instruction byte must be written in the format indicated by REG0<6>. That is, if the AD9856 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the most significant byte. In MSB first mode, the serial port internal byte address generator decrements for each byte required of the multibyte communication cycle. Multibyte data transfers in LSB first format can be completed by writing an instruction byte that includes the register address of the least significant byte. In LSB first mode, the serial port internal byte address generator increments for each byte required of the multibyte communication cycle.

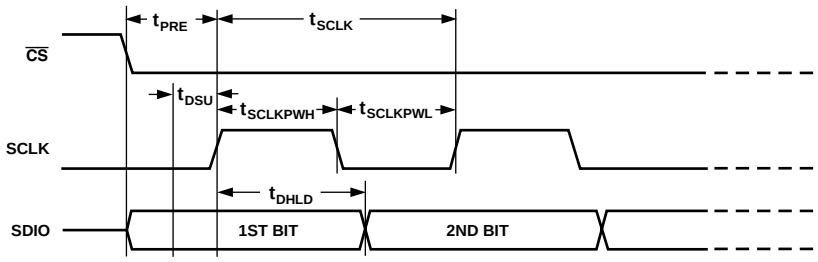
NOTES ON SERIAL PORT OPERATION

The AD9856 serial port configuration bits reside in Bits 6 and 7 of register address 0h. It is important to note that the configuration changes *immediately* upon writing to this register. For multibyte transfers, writing to this register may occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remainder of the current communication cycle.

The AD9856 serial port controller address can roll from 19h to 0h for multibyte I/O operations if the MSB first mode is active. The serial port controller address can roll from 0h to 19h for multibyte I/O operations if the LSB first mode is active.

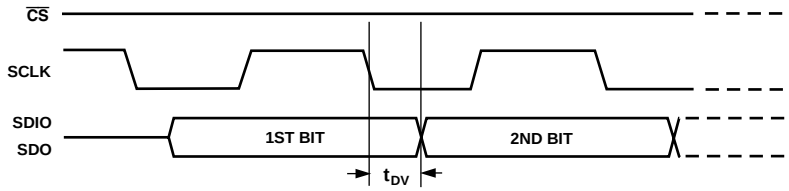
The system must maintain synchronization with the AD9856 or the internal control logic will not be able to recognize further instructions. For example, if the system sends an instruction byte for a 2-byte write, then pulses the SCLK pin for a 3-byte write (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle will properly write the first two data bytes into the AD9856, but the next eight rising SCLK edges are interpreted as the next instruction byte, *not* the final byte of the previous communication cycle.

In the case where synchronization is lost between the system and the AD9856, the SYNC I/O pin provides a means to re-establish synchronization without re-initializing the entire chip. The SYNC I/O pin enables the user to reset the AD9856 state machine to accept the next eight SCLK rising edges to be coincident with the instruction phase of a new communication cycle. By applying and removing a “high” signal to the SYNC I/O pin, the AD9856 is set to once again begin performing the communication cycle in synchronization with the system. Any information that had been written to the AD9856 registers during a valid communication cycle prior to loss of synchronization will remain intact.



SYMBOL	DEFINITION	MIN
t_{PRE}	$\overline{CS}$ SETUP TIME	30ns
t_{SCLK}	PERIOD OF SERIAL DATA CLOCK	100ns
t_{DSU}	SERIAL DATA SETUP TIME	30ns
$t_{SCLKPWH}$	SERIAL DATA CLOCK PULSEWIDTH HIGH	40ns
$t_{SCLKPWL}$	SERIAL DATA CLOCK PULSEWIDTH LOW	40ns
t_{DHLD}	SERIAL DATA HOLD TIME	0ns

Figure 38. Timing Diagram for Data Write to AD9856



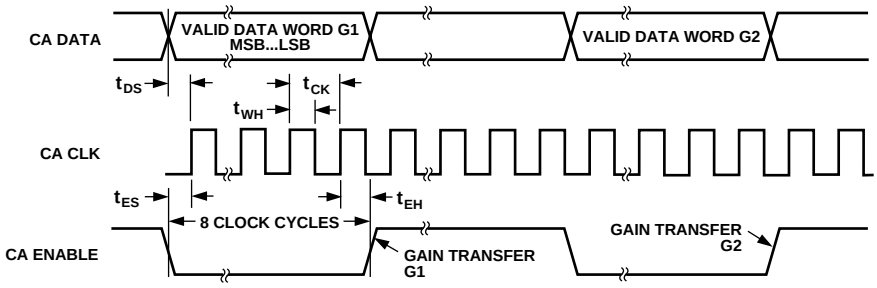
SYMBOL	DEFINITION	MAX
t_{DV}	DATA VALID TIME	30ns

Figure 39. Timing Diagram for Read from AD9856

PROGRAMMING/WRITING THE AD8320/AD8321 CABLE DRIVER AMPLIFIER GAIN CONTROL

Programming the Gain Control register of the AD8320/AD8321 programmable cable driver amplifier can be accomplished via the AD9856 serial port. Four 8-bit registers (one per profile) within the AD9856 store the gain value to be written to the AD8320/AD8321. The AD8320/AD8321 is written via three dedicated AD9856 output pins that are directly connected to the AD8320/AD8321's serial input port. The transfer of data from the AD9856 to the AD8320/AD8321 requires 136 SYSCLK clock cycles and occurs upon detection of three conditions. Each is described below:

1. Power-up Reset—Upon initial power up, the AD9856 clears (Logic 0) the contents of control registers 07h, 0Dh, 13h, and 19h, which defines the lowest gain setting of the AD8320/AD8321. Thus, the AD9856 writes all 0s out of the AD8320/AD8321 serial interface.
2. Change in profile selection bits (PS1, PS0)—The AD9856 samples the PS1, PS0 input pins and writes to the AD8320/AD8321 gain control register when a change in profile is determined. The data written to the AD8320/AD8321 comes from the AD9856 gain control register associated with the current profile.
3. Serial Port Write of AD9856 Registers that Contain AD8320/AD8321 Data—The AD9856 will write to the AD8320/AD8321 with data from the gain control register associated with the current profile whenever ANY AD9856 gain control register is updated. The user does not have to write the AD9856 in any particular order or be concerned with time between writes. If the AD9856 is currently writing to the AD8320/AD8321 while one of the four AD9856 gain control registers is being addressed, the AD9856 will immediately terminate the AD8320/AD8321 write sequence (without updating the AD8320/AD8321) and begin a new AD8320/AD8321 write sequence.



SYMBOL	DEFINITION	MIN
t_{DS}	CA DATA SETUP TIME	6.5ns
t_{DH}	CA DATA HOLD TIME	2ns
t_{WH}	CA CLOCK PULSE HIGH	9ns
t_{CK}	CA CLOCK PERIOD	25ns
t_{ES}	CA ENABLE SETUP TIME	17ns
t_{EH}	CA ENABLE HOLD TIME	2.0ns

Figure 40. Programmable Cable Driver Amplifier Output Control Interface Timing

UNDERSTANDING AND USING PIN SELECTABLE MODULATOR PROFILES

The AD9856 Quadrature Digital Upconverter is capable of storing four preconfigured modulation modes called "profiles" that define the following:

- Output Frequency—32 Bits
- Interpolation Rate—6 Bits
- Spectral Inversion Status—1 Bit
- Bypass 3rd Half-Band Filter—1 Bit
- Gain Control of AD8320/AD8321—8 Bits

Output Frequency: This attribute consists of four 8-bit words loaded into four register addresses to form a 32-bit frequency tuning word (FTW) for each profile. The lowest register address corresponds to the least significant 8-bit word. Ascending addresses correspond to increasingly significant 8-bit words. The output frequency equation is given as: $f_{OUT} = (FTW \times SYSCLK)/2^{32}$.

Interpolation Rate: Consists of a 6-bit word representing the allowed interpolation values from 2 to 63. Interpolation is the mechanism used to "up-sample" or multiply the input data rate such that it exactly matches that of the DDS sample rate (SYSCLK). This implies that the system clock must be an exact multiple of the symbol rate. This 6-bit word represents the 6 MSBs of the eight bits allocated for that address. The remaining two bits contain the spectral inversion status bit and half-band bypass bit.

Spectral Inversion: Single bit that when at Logic 0 the default or "noninverted" output from the adder is sent to the following stages. A Logic 1 will cause the inverted output to be sent to the following stages. The noninverted output is described as $I \times Cos(\omega t) - Q \times Sin(\omega t)$. The inverted output is described as $I \times Cos(\omega t) + Q \times Sin(\omega t)$. This bit is located adjacent to the LSB at the same address as the interpolation rate (see above).

Bypass Third Half-Band Filter: A single bit located in the LSB position of the same address as the interpolation rate. When this bit is Logic 0, the third half-band filter is engaged and its inherent 2× interpolation rate is applied. When this bit is Logic 1, the third half-band filter is bypassed and the 2× interpolation rate is negated. This allows users to input higher data rates—rates that may be too high for the minimum interpolation rate if all three half-band filters with their inherent 2× interpolation rate are engaged. The overall effect is to reduce minimum interpolation rate from 8× to 4×.

AD8320/AD8321 Gain Control: An 8-bit word that controls the gain of an AD8320/AD8321 Programmable Gain Amplifier connected to the AD9856 with the 3-bit SPI interface bus. Gain range is from –10 dB (00 hex) to +26 dB (FFhex). The gain is linear in V/V/LSB and follows the equation: $A_V = 0.316 + 0.077 \times Code$. Where "Code" is the decimal equivalent of the 8-bit gain word.

Profile Selection: After profiles have been loaded into the appropriate registers, the user may select which profile to use with two input pins: PS0 and PS1, Pins 45 and 46. Profiles are selected according to the table below.

Table V. Profile Select Matrix

PS1	PS0	PROFILE
0	0	1
0	1	2
1	0	3
1	1	4

Except while in single tone mode, it is recommended that users suspend the TxENABLE function by bringing that pin to Logic 0 prior to changing from one profile to another and then reasserting TxENABLE afterwards. This assures that any dis-continuities resulting from register data transfer are not transmitted up or downstream. Furthermore, changing interpolation rates during a burst may create an unrecoverable digital overflow condition that would interrupt transmission of the current burst until a RESET and reloading procedure would be completed.

POWER DISSIPATION CONSIDERATIONS

The majority of the AD9856 power dissipation comes from digital switching currents. As such, power dissipation is highly dependent upon chip configuration.

Obviously, the major contributor to switching current is the maximum clock rate at which the device is operated, but other factors can play a significant role. Factors such as the CIC interpolation rate, and whether the third half-band filter and inverse SINC filters are active, can affect the power dissipation of the device.

It is important for the user to consider all of these factors when optimizing performance for power dissipation. For example, there are two ways to achieve a 6 MS/s transmission rate with the AD9856. The first method uses an f_{MAX} of 192 MHz; the other method uses an f_{MAX} of 144 MHz, which reduces power dissipation by nearly 25%.

For the first method, the input data must be externally 4× upsampled. The AD9856 must be configured for a CIC interpolation rate of three while bypassing the 3rd half-band filter. This results in an I/Q input sample rate of 24 MHz which is further upsampled by a factor of 8 to 192 MHz.

The second method requires an f_{MAX} of 144 MHz with externally 2× upsampled input data. The AD9856 is configured for a CIC interpolation rate of 3 while bypassing the 3rd half-band filter. The input I/Q sample rate is 12 MHz, which is further upsampled by a factor of 12 MHz to 144 MHz.

For burst applications with relatively long nonbursting periods, the sleep bit is useful for saving power. When in sleep mode, power is reduced to below 6 mW. Consideration must be given to wake-up time, which will generally be in the 400 µs to 750 µs range. For those applications that cannot use the sleep bit due to this wake-up time, there is an alternate method of reducing power dissipation when not transmitting. By writing the "Bypass REFCLK Multiplier" bit active, the power is reduced by nearly the REFCLK Multiplier factor. For example, if the external reference clock is 16 MHz and REFCLK Multiplier is set to 10×, all clocks will divide down by a factor of 10 when the REFCLK Multiplier is bypassed. This effectively scales down the power dissipation by nearly a factor of 10. In this case, both the REFCLK Multiplier function and the DAC, which use relatively little power, remain fully powered. The REFCLK Multiplier circuit is locked to the 16 MHz external reference clock but its output is driving a very small load, hence very little power dissipation. When the REFCLK Multiplier is reactivated, the acquisition time is small. In this power-reduction technique, the larger the REFCLK Multiplier factor, the larger the power savings.

The AD9856 is specified for operation at +3.0 V ± 5% and the thermal impedance of the AD9856 in the 48-LQFP plastic package is 38°C/W. At 200 MHz operation, power dissipation is 1.5 W. This permits operation over the industrial temperature range without exceeding the maximum junction temperature of 150°C. To realize this quoted thermal impedance, all power and ground pins must be soldered down to a multilayer PCB with power and ground copper planes directly available at the package pins.

Under worst case conditions, that is, with power supplies at +2.85 V and ambient temperatures of +85°C, device operation at 200 MHz is guaranteed for single tone mode only. For modulation mode at 200 MHz, +85°C operation, the minimum power supply voltage is +3.0 V.

AD9856 EVALUATION BOARD

An evaluation board is available for the AD9856 quadrature digital upconverter that facilitates bench and system analysis of the device. The AD9856/PCB contains the AD9856 device and Windows software that allows control of the device via the printer port of a PC. The DAC output is provided on a jack for spectral analysis. The AD9856/PCB circuit board provides a single-ended 65 MHz, 50 Ω, elliptical low-pass filter on the output of the DAC.

There is also a provision for the user to implement the AD8320/AD8321 programmable cable driver amplifier on the AD9856/PCB evaluation board. The AD8320/AD8321 gain is programmed through the AD9856 via the menu driven control software.

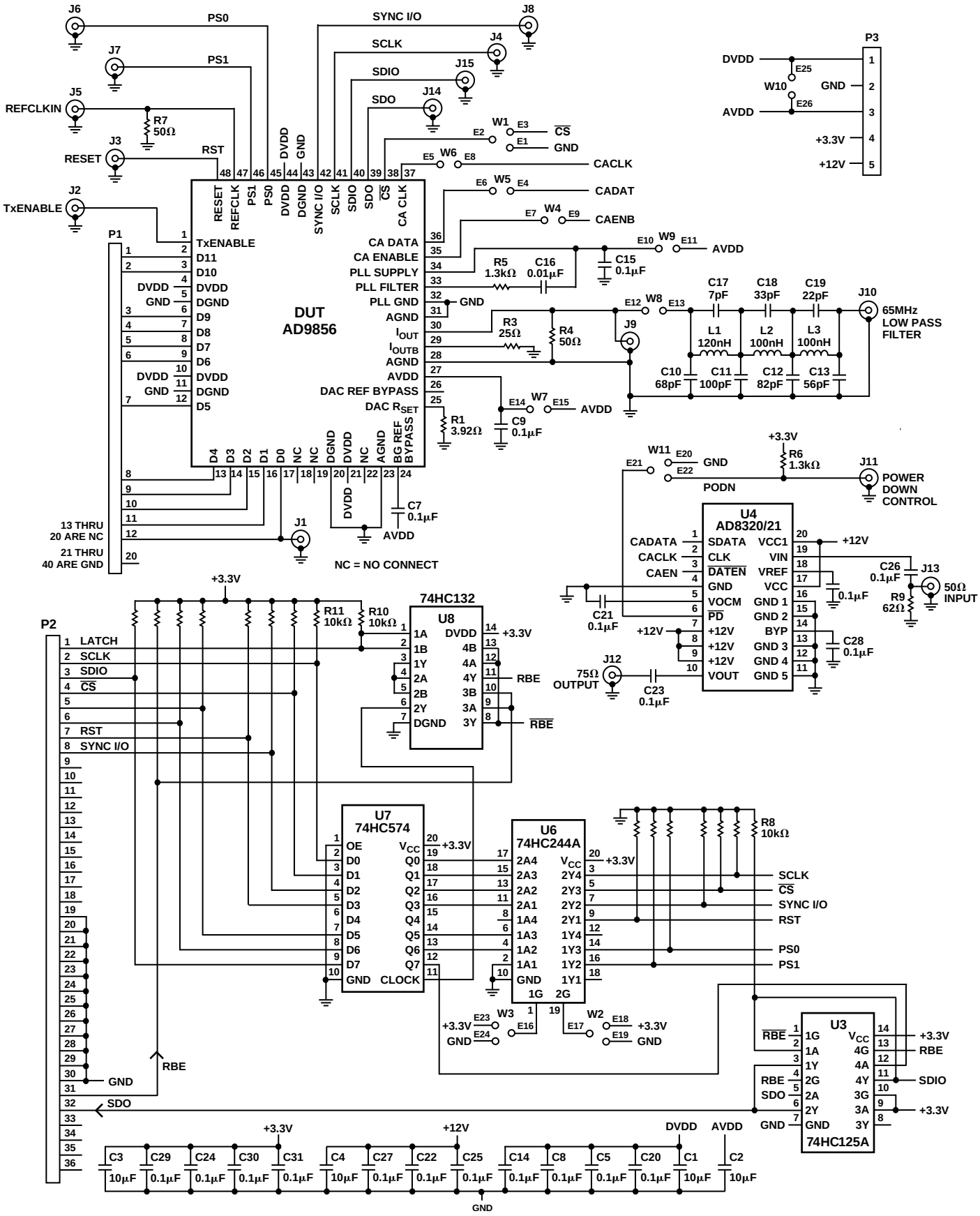
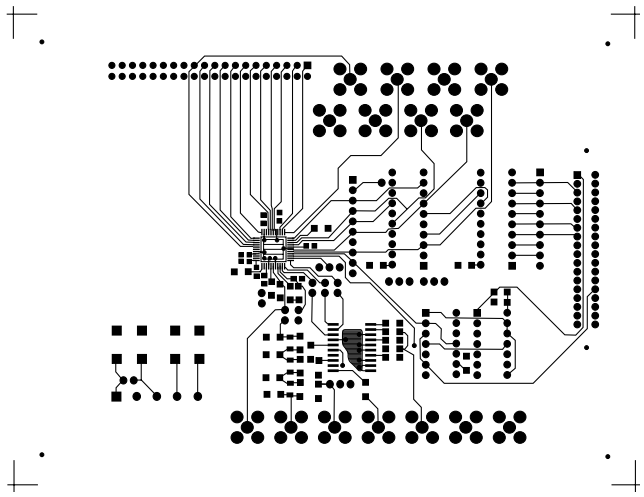
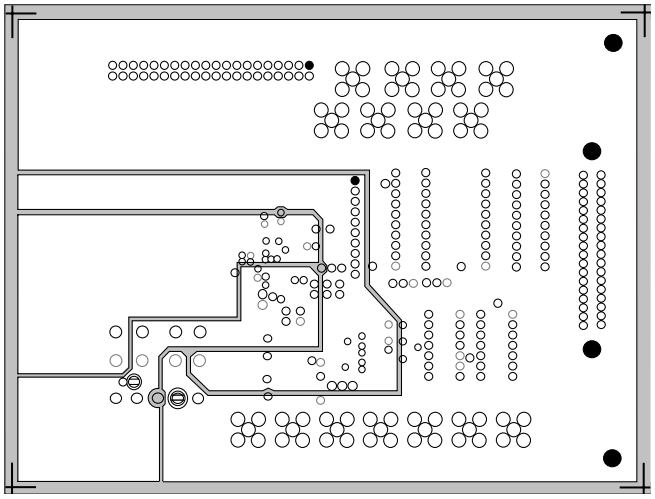


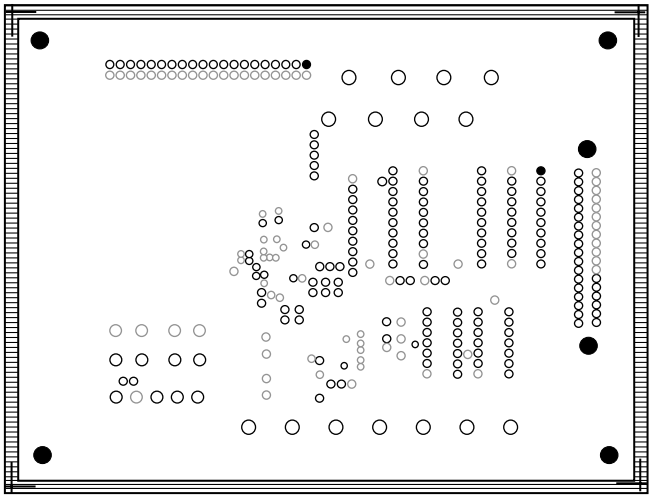
Figure 41. AD9856/PCB Evaluation Board Electrical Schematic



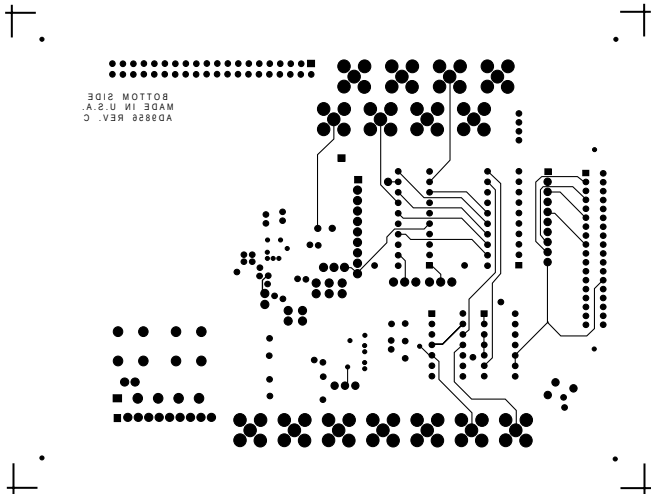
a. Layer 1 (Top)—Signal Routing and Ground Plane



c. Layer 3—DUT +V, +5 V and +12 V Power Plane



b. Layer 2—Ground Plane



d. Layer 4 (Bottom)—Signal Routing

Figure 42. PCB Layout Patterns for Four-Layer AD9856-PCB Evaluation Board

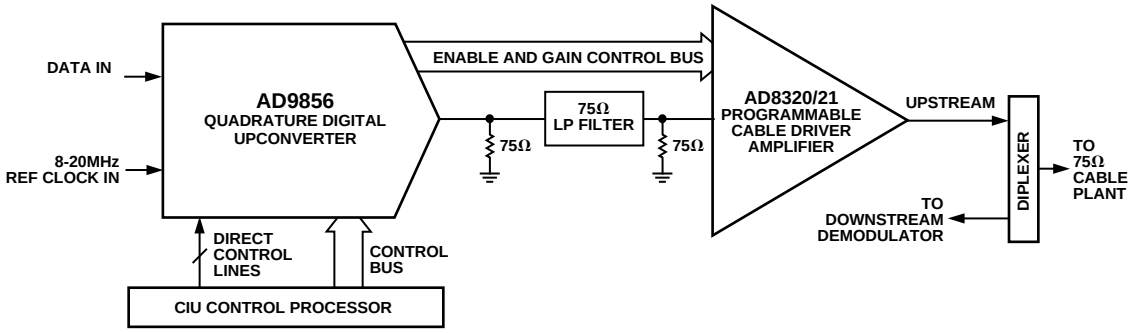


Figure 43. Basic Implementation of AD9856 Digital Modulator and AD8320/AD8321 Programmable Cable Driver Amplifier in 5 MHz–65 MHz HFC Return-Path Application

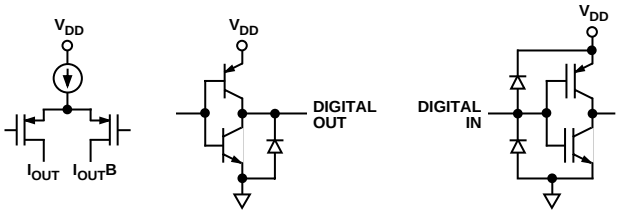
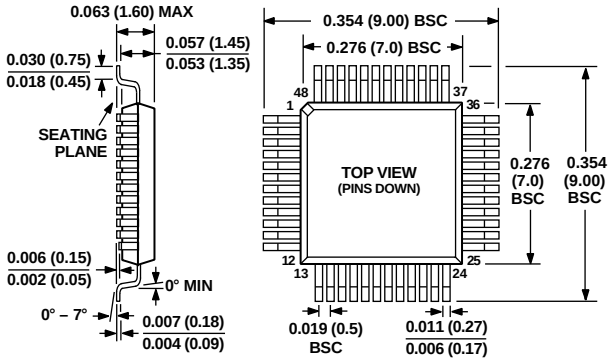


Figure 44. Equivalent I/O Circuits

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Quad Flatpack IC Package (LQFP)
(ST-48)



C3476a–0–9/99

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Appendix B: Analog Devices AD8320 – Serial Digital Controlled Variable Gain Line Driver

B.1 Output Amplifier Data Sheet

Presented on the following pages is the data sheet for the Analog Devices AD8230 Serial Digital Controlled Variable Gain Line Driver.

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Serial Digital Controlled Variable Gain Line Driver

AD8320

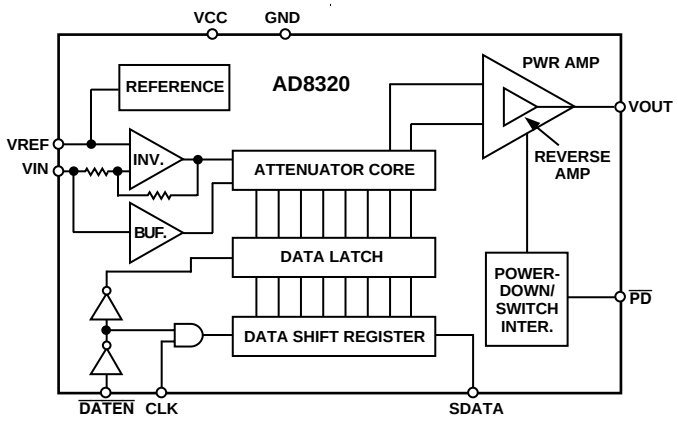
FEATURES

8-Bit Serial Gain Control
V/V/LSB Linear Gain Response
36 dB Gain Range
±0.20 dB Gain Accuracy
Upper Bandwidth: 150 MHz
22 dBm 1 dB Compression Point (75 Ω)
Drives Low Distortion Signals into 75 Ω Load:
–57 dBc SFDR at 42 MHz and 12 dBm Out
–46 dBc SFDR at 42 MHz and 18 dBm Out
Single Supply Operation from 5 V to 12 V
Maintains 75 Ω Output Impedance
Power-Up and Power-Down Condition
Supports SPI Input Control Standard

APPLICATIONS

Coaxial Cable Driver
HFC Cable Telephony Systems
HFC High Speed Data Modems
Interactive Set-Top Boxes
PC Plug-In Modems
Interfaces with AD9853 I^2C Controlled Digital Modulator
High Performance Digitally Controlled Variable Gain Block

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The AD8320 is a digitally controlled variable gain amplifier optimized for coaxial line driving applications. An 8-bit serial word determines the desired output gain over a 36 dB range (256 gain levels). The AD8320 provides linear gain response.

The AD8320 is made up of a digitally controlled variable attenuator of 0 dB to –36 dB, which is preceded by a low noise, fixed gain buffer and followed by a low distortion high power amplifier. The AD8320 has a 220 Ω input impedance and accepts a single-ended input signal with a specified analog input level of up to 0.310 V p-p. The output is specified for driving a 75 Ω load, such as coaxial cable, although the AD8320 is capable of driving other loads. Distortion performance of –57 dBc is achieved with an output level up to 12 dBm (3.1 V p-p) at 42 MHz, while –46 dBc distortion is achieved with an output level up to 18 dBm (6.2 V p-p).

A key performance and cost advantage of the AD8320 results from the ability to maintain a constant 75 Ω output impedance during power-up and power-down conditions. This eliminates the need for external 75 Ω back-termination, resulting in twice the effective output voltage when compared to a standard operational amplifier. Additionally, the on-chip 75 Ω termination results in low glitch output during power-down and power-up transitions, eliminating the need for an external switch.

The AD8320 is packaged in a 20-lead SOIC and operates from a single +5 V through +12 V supply and has an operational temperature range of –40°C to +85°C.

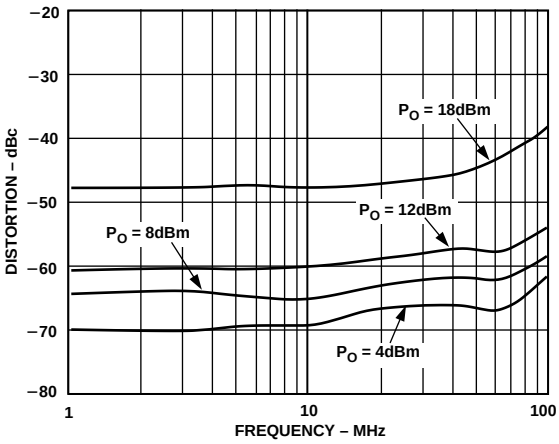


Figure 1. Worst Harmonic Distortion vs. Frequency for Various Output Levels at V_{CC} = 12 V

REV. 0

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AD8320–SPECIFICATIONS (@ V_{CC} = 12 V, T_A = +25°C, V_{IN} = 0.310 V p-p, R_L = 75 Ω, R_S = 75 Ω unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS					
Full-Scale Input Voltage	Max Gain, P_{OUT} = 18 dBm, V_{CC} = 12 V		0.310		V p-p
	Max Gain, P_{OUT} = 12 dBm, V_{CC} = 5 V		0.155		V p-p
Input Resistance			220		Ω
Input Capacitance			2.0		pF
GAIN CONTROL INTERFACE					
Gain Range			36		dB
Full Scale (Max) Gain			26 (20)		dB (V/V)
Gain Offset (Min) Gain			–10.0 (0.316)		dB (V/V)
Gain Scaling Factor			0.077		V/V/LSB
OUTPUT CHARACTERISTICS					
Bandwidth (–3 dB)	All Gain Codes		150		MHz
Bandwidth Roll-Off	F = 65 MHz		0.7		dB
Bandwidth Peaking	F = 65 MHz		0		dB
Output Offset Voltage	All Gain Codes		±40		mV
Output Offset Drift	Full Temperature Range		±0.25		mV/°C
Output Noise Spectral Density	Max. Gain, Frequency = 10 MHz		73		nV/√Hz
	Min. Gain, Frequency = 10 MHz		53		nV/√Hz
	$\overline{PD}$ = 0, Frequency = 10 MHz		4.5		nV/√Hz
1 dB Compression Point	V_{CC} = 12 V		22.5		dBm
	V_{CC} = 5 V		16		dBm
Output Impedance	Power Up and Power Down	65	75	85	Ω
Overload Recovery	Max Gain, V_{IN} = 500 mV p-p		40		ns
OVERALL PERFORMANCE					
Worst Harmonic Distortion	F = 42 MHz, P_{OUT} = 12 dBm, V_{CC} = 12 V		–57.0	–52.0	dBc
	F = 42 MHz, P_{OUT} = 12 dBm, V_{CC} = 5 V		–43.0	–39.0	dBc
	F = 42 MHz, P_{OUT} = 18 dBm, V_{CC} = 12 V		–46.0	–42.0	dBc
	F = 65 MHz, P_{OUT} = 12 dBm, V_{CC} = 12 V		–57.0	–52.0	dBc
	F = 65 MHz, P_{OUT} = 12 dBm, V_{CC} = 5 V		–42.5	–39.0	dBc
	F = 65 MHz, P_{OUT} = 18 dBm, V_{CC} = 12 V		–43.0	–40.0	dBc
3rd Order Intercept	F = 42 MHz, P_{OUT} = 18 dBm, V_{CC} = 12 V		34		dBm
	F = 42 MHz, P_{OUT} = 12 dBm, V_{CC} = 5 V		32		dBm
	F = 65 MHz, P_{OUT} = 18 dBm, V_{CC} = 12 V		32.5		dBm
	F = 65 MHz, P_{OUT} = 12 dBm, V_{CC} = 5 V		28.5		dBm
Full-Scale (Max Gain) Accuracy	F = 10 MHz		±0.1		dB
Gain Offset (Min Gain) Accuracy	F = 10 MHz		±0.2		dB
Gain Accuracy	F = 10 MHz, All Gain Codes	–0.75	±0.2	0.75	dB
Gain Drift	Full Temperature Range		±0.5		mdB/°C
Gain Variation w/Supply	V_{CC} = +5 V to 12 V		35		mdB/V
Output Settling to 1 mV					
Gain Change @ $T_{\overline{DATEN}}$ = 1	Min to Max Gain, V_{IN} = 0.31 V p-p		30		ns
Input Change	Max Gain, V_{IN} = 0 V to 0.31 V p-p		25		ns
POWER CONTROL					
Power-Down Settling Time to 1 mV	Max Gain, V_{IN} = 0		45		ns
Power-Up Settling Time to 1 mV	Max Gain, V_{IN} = 0		65		ns
Power-Down Pedestal Offset	Max Gain, V_{IN} = 0		±30		mV
Spectral Output Leakage	F ($\overline{PD}$) = 400 Hz @ 15% Duty Cycle		–70		dBm
	5 MHz ≤ F ≤ 65 MHz				
Maximum Reverse Power	$\overline{PD}$ = 0		5		dBm
POWER SUPPLY					
Specified Operating Range		+5		+12	V
Quiescent Current	$\overline{PD}$ = 1, V_{CC} = +5 V		80	85	mA
Power Down	$\overline{PD}$ = 0, V_{CC} = +5 V		25	30	mA
Power Up, V_{CC} = +12 V	$\overline{PD}$ = 1, V_{CC} = +12 V		97	105	mA
Power Down, V_{CC} =+12 V	$\overline{PD}$ = 0, V_{CC} = +12 V		32	37	mA

LOGIC INPUTS (TTL/CMOS Logic) ($\overline{\text{DATEN}}$, CLK, SDATA, 5 V ≤ V_{CC} ≤ 12 V; Full Temperature Range)

Parameter	Min	Typ	Max	Units
Logic "1" Voltage	2.1		5.0	V
Logic "0" Voltage	0		0.8	V
Logic "1" Current (V_{INH} = 5 V) CLK, SDATA, $\overline{\text{DATEN}}$	0		20	nA
Logic "0" Current (V_{INL} = 0 V) CLK, SDATA, $\overline{\text{DATEN}}$	–450		–75	nA
Logic "1" Current (V_{INH} = 5 V) $\overline{\text{PD}}$	0		190	μA
Logic "0" Current (V_{INL} = 0 V) $\overline{\text{PD}}$	–320		–70	μA

TIMING REQUIREMENTS (Full Temperature Range, V_{CC} Supply Range, T_R = T_F = 4 ns, F_{CLK} = 8 MHz unless otherwise noted.)

Parameter	Min	Typ	Max	Units
Clock Pulse Width (T_{WH})	12.0			ns
Clock Period (T_C)	32.0			ns
Setup Time SDATA vs. Clock (T_{DS})	6.5			ns
Setup Time $\overline{\text{DATEN}}$ vs. Clock (T_{ES})	17.0			ns
Hold Time SDATA vs. Clock (T_{DH})	5.0			ns
Hold Time $\overline{\text{DATEN}}$ vs. Clock (T_{EH})	3.0			ns
Input Rise and Fall Times, SDATA, $\overline{\text{DATEN}}$, Clock (T_R, T_F)			10	ns

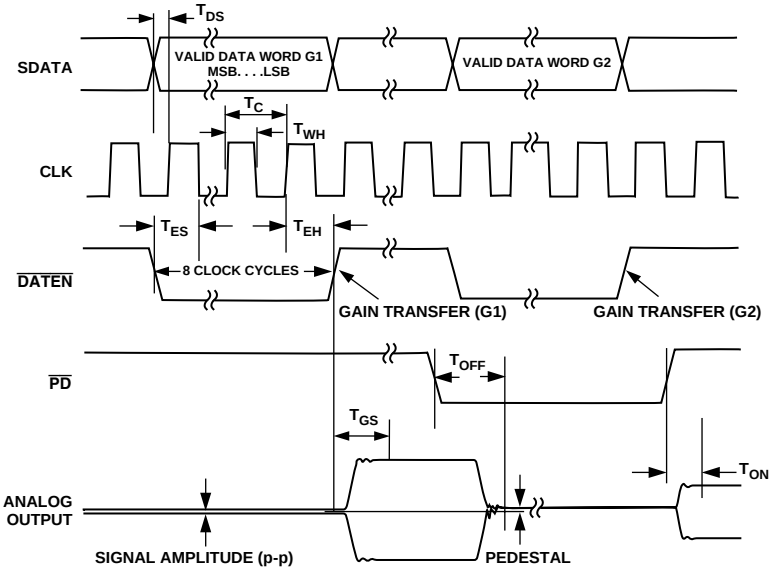


Figure 2. Serial Interface Timing

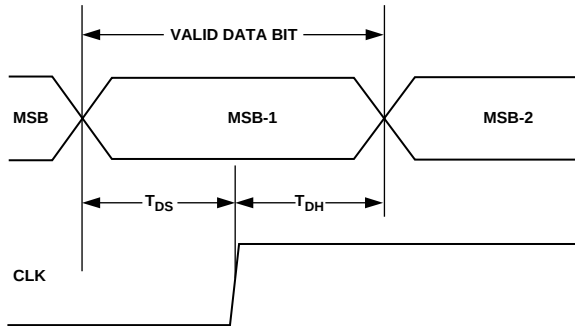


Figure 3.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $+V_S$
- Pins 7, 8, 9, 17, 20 . . . . . –0.8 V to +13 V

Input Voltages
- Pins 19 . . . . . ±3 V
- Pins 1, 2, 3, 6 . . . . . –0.8 V to +5 V

Internal Power Dissipation
- Small Outline (RP) . . . . . 1.3 W

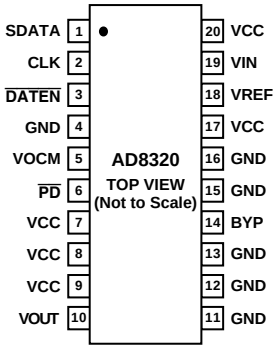
Operating Temperature Range . . . . . –40°C to +85°C

Storage Temperature Range . . . . . –65°C to +150°C

Lead Temperature, Soldering 60 seconds . . . . . +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	θ_{JA}	Package Option
AD8320ARP	–40°C to +85°C	20-Lead Thermally Enhanced Power SOIC*	53°C/W	RP-20
AD8320-EB		Evaluation Board		

*Shipped in tubes (38 pieces/tube) and dry packed per J-STD-020.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8320 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin	Function	Description
1	SDATA	Serial Data Input. This digital input allows for an 8-bit serial (gain) word to be loaded into the internal register with the MSB (most significant bit) first.
2	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave register. A Logic 0 to 1 transition latches the data bit and a 1 to 0 transfers the data bit to the slave. This requires the input serial data word to be valid at or before this clock transition.
3	$\overline{\text{DATEN}}$	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0 to 1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A 1 to 0 transition inhibits the data latch (holds the previous gain state) and simultaneously enables the register for serial data load.
4, 11, 12, 13, 15, 16	GND	Common External Ground Reference.
5	VOCM	VCC/2 Reference Pin. A dc output reference level that is equal to 1/2 of the supply voltage (VCC). This port should be externally ac decoupled (0.1 µF cap).
6	$\overline{\text{PD}}$	Power-Down Low Logic Input. A Logic 0 powers down (shuts off) the power amplifier disabling the output signal and enabling the reverse amplifier. A Logic 1 enables the output power amplifier and disables the reverse amplifier.
7, 8, 9, 17, 20	VCC	Common Positive External Supply Voltage.
10	VOUT	Output Signal Port. DC biased to approximately VCC/2.
14	BYP	Internal Bypass. This pin must be externally ac decoupled (0.1 µF cap).
18	VREF	Input Reference Voltage (typically 1.9 V at 27°C). This port should be externally ac decoupled (0.1 µF cap).
19	VIN	Analog Voltage Input Signal Port. DC biased to VREF voltage.

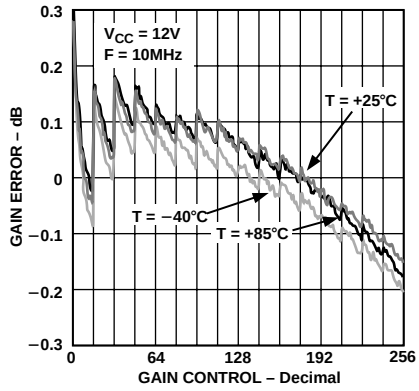


Figure 4. Gain Error vs. Gain Control at Various Temperatures

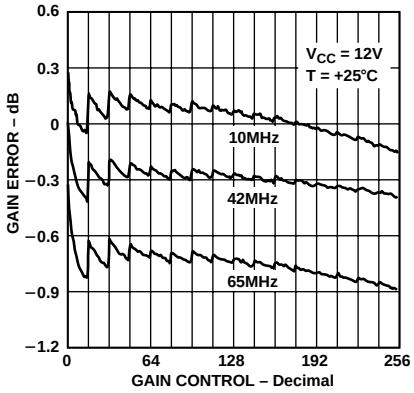


Figure 5. Gain Error vs. Gain Control at Various Frequencies

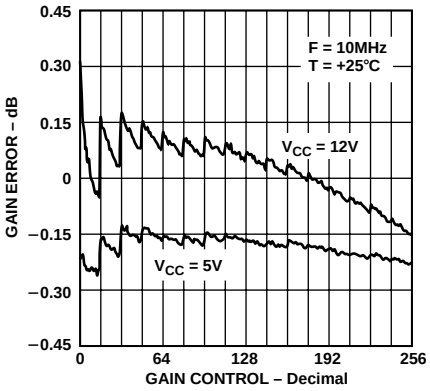


Figure 6. Gain Error vs. Gain Control at Different Supply Voltages

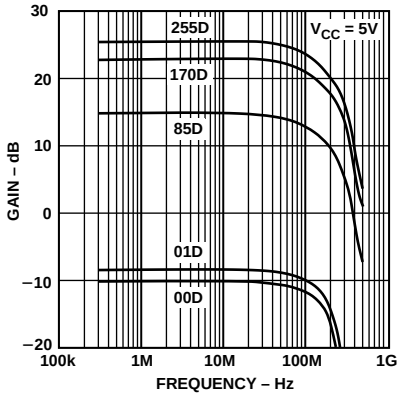


Figure 7. AC Response

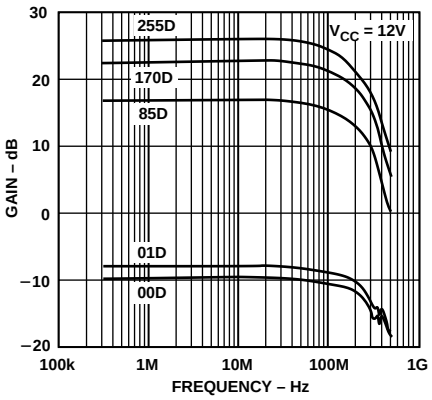


Figure 8. AC Response

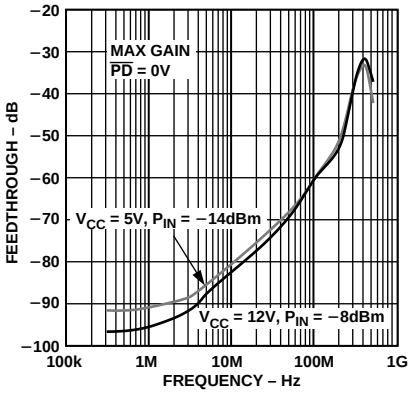


Figure 9. Input Signal Feedthrough vs. Frequency

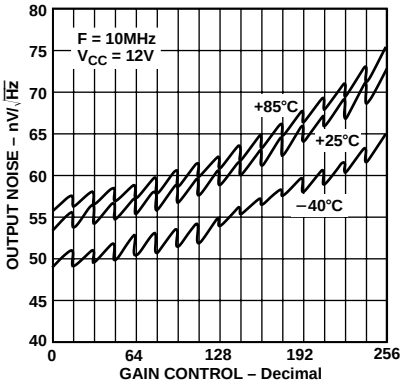


Figure 10. Output Referred Noise vs. Gain Control at Various Temperatures

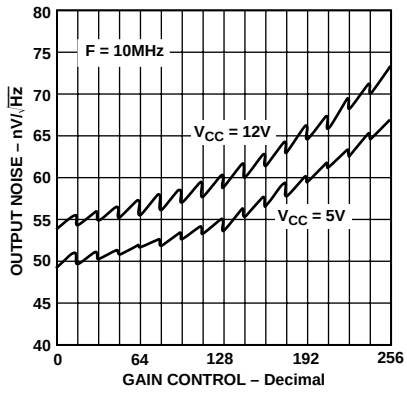


Figure 11. Output Referred Noise vs. Gain Control at Different Supply Voltages

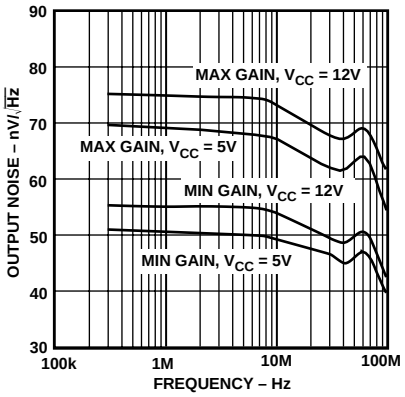


Figure 12. Output Referred Noise vs. Frequency

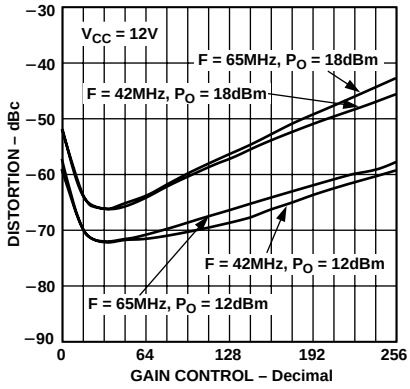


Figure 13. Worst Harmonic Distortion vs. Gain Control

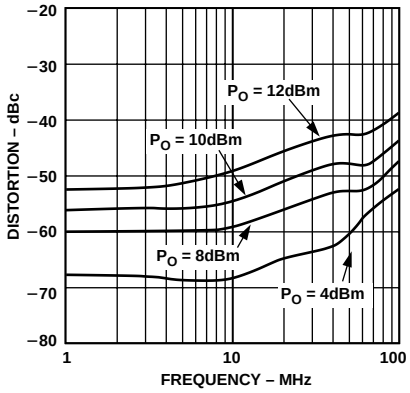


Figure 14. Worst Harmonic Distortion vs. Frequency for Various Output Levels at V_{CC} = 5 V

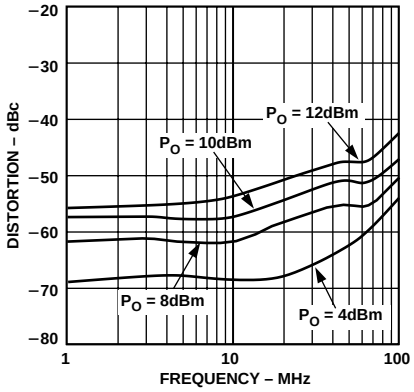


Figure 15. Worst Harmonic Distortion vs. Frequency for Various Output Levels at V_{CC} = 6 V

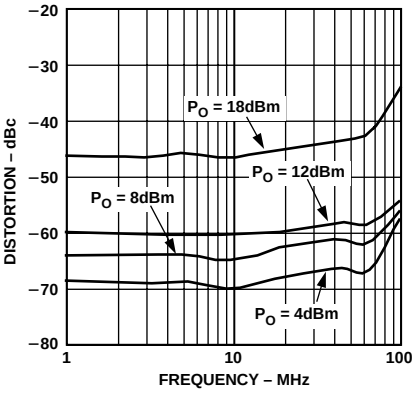


Figure 16. Worst Harmonic Distortion vs. Frequency for Various Output Levels at V_{CC} = 10 V

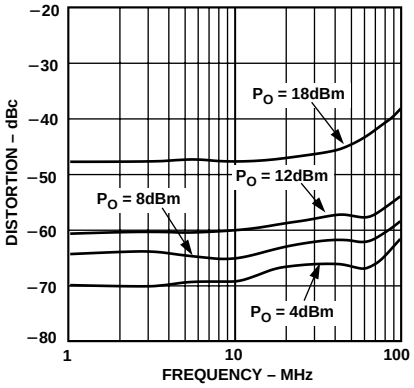


Figure 17. Worst Harmonic Distortion vs. Frequency for Various Output Levels at V_{CC} = 12 V

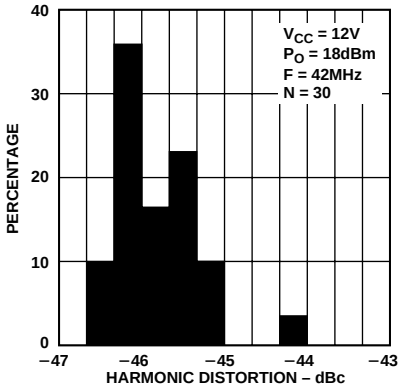


Figure 18. Distribution of Worst Harmonic Distortion

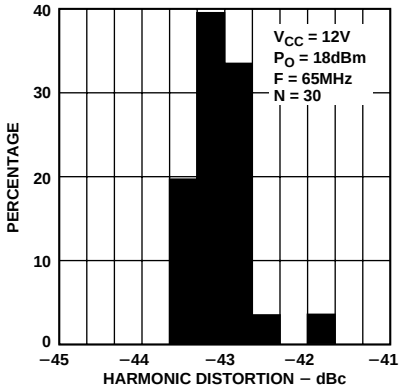


Figure 19. Distribution of Worst Harmonic Distortion

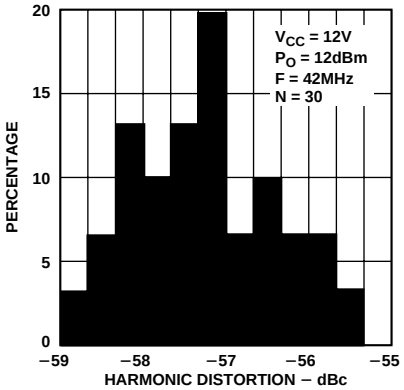


Figure 20. Distribution of Worst Harmonic Distortion

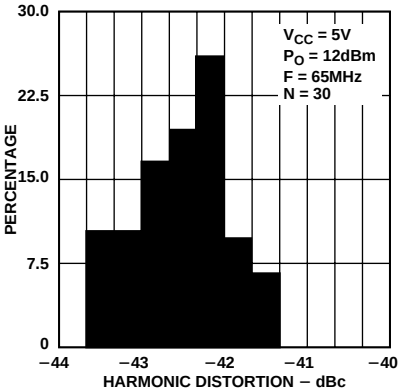


Figure 21. Distribution of Worst Harmonic Distortion

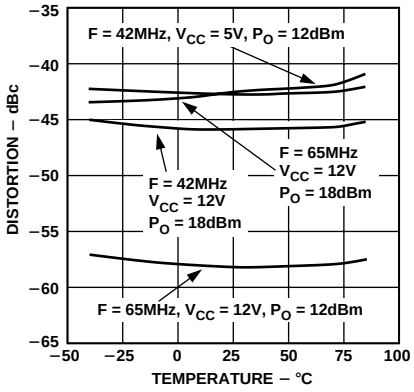


Figure 22. Harmonic Distortion vs. Temperature

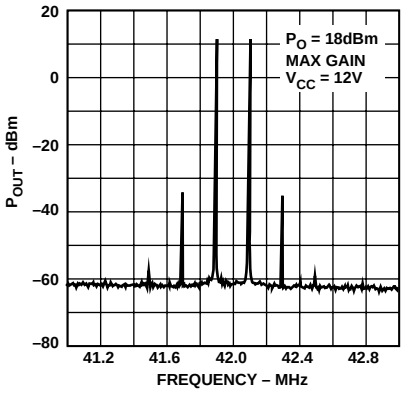


Figure 23. Two-Tone Intermodulation Distortion

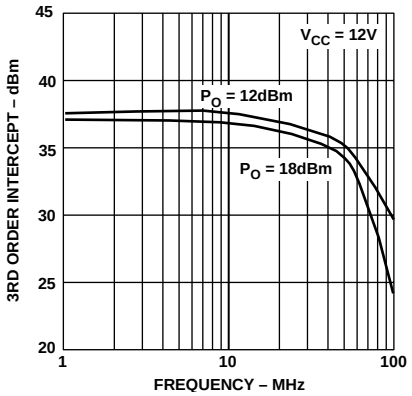


Figure 24. Third Order Intercept vs. Frequency

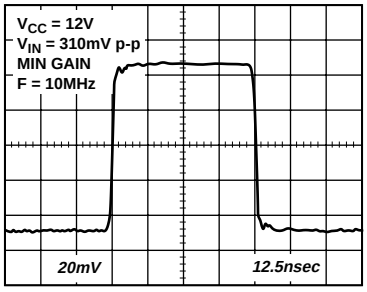


Figure 25. Transient Response

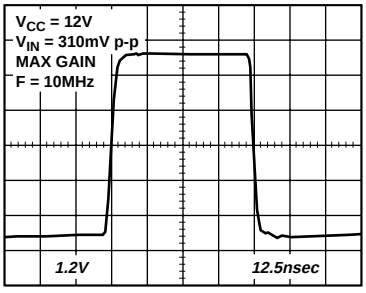


Figure 26. Transient Response

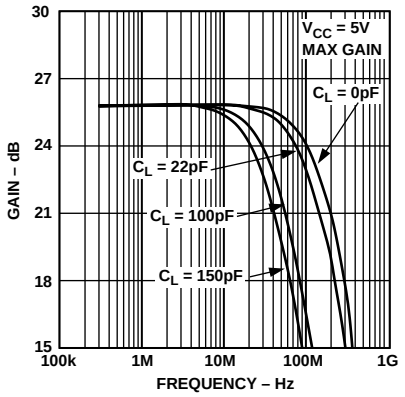


Figure 27. AC Response for Various Capacitive Loads

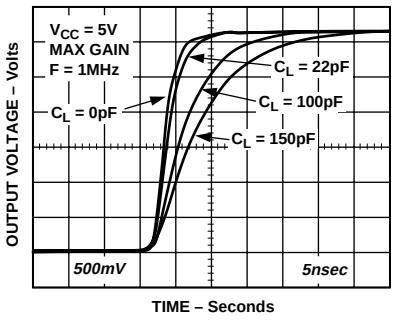


Figure 28. Transient Response for Various Capacitive Loads

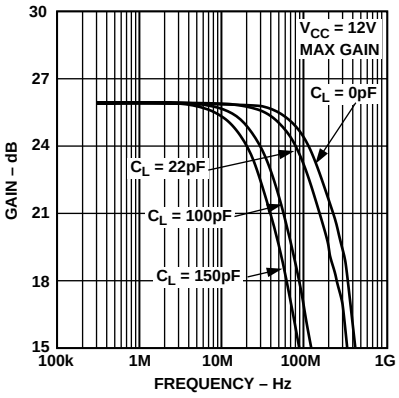


Figure 29. AC Response for Various Capacitive Loads

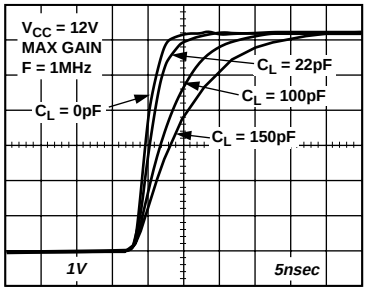


Figure 30. Transient Response for Various Capacitive Loads

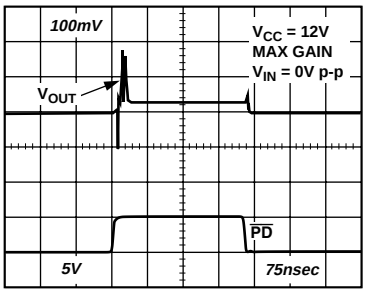


Figure 31. Power-Up/Power-Down Glitch

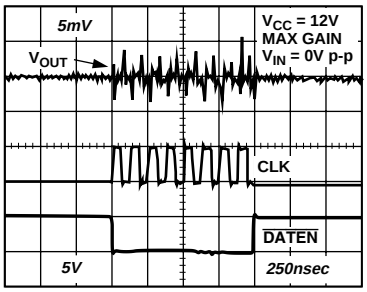


Figure 32. Clock Feedthrough

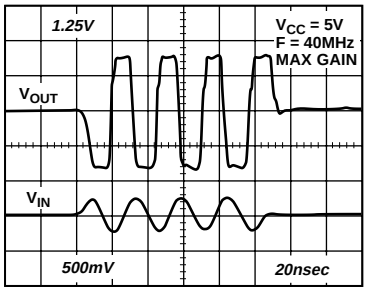


Figure 33. Overload Recovery

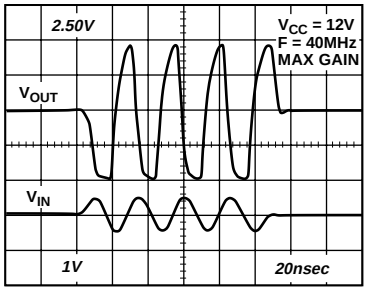


Figure 34. Overload Recovery

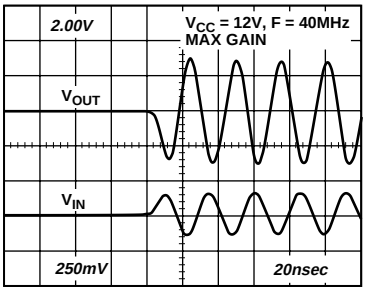


Figure 35. Output Settling Time Due to Input Change

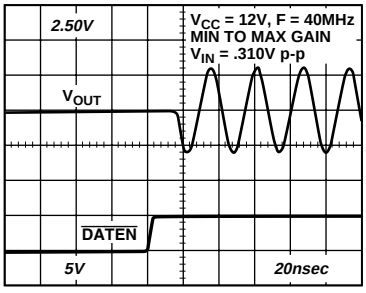


Figure 36. Output Settling Time Due to Gain Change

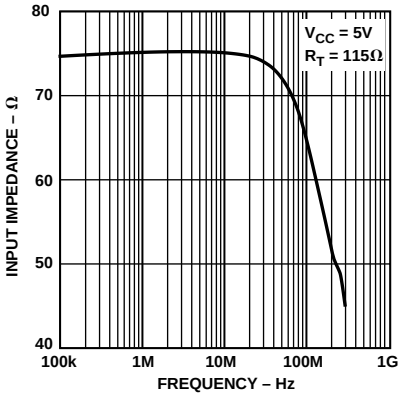


Figure 37. Input Impedance vs. Frequency

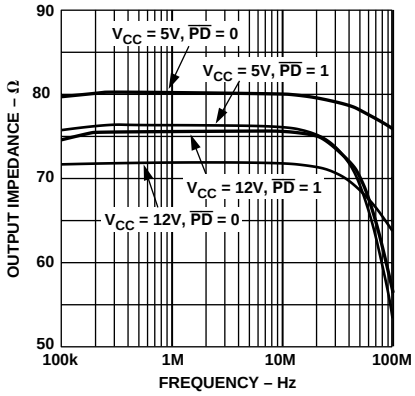


Figure 38. Output Impedance vs. Frequency

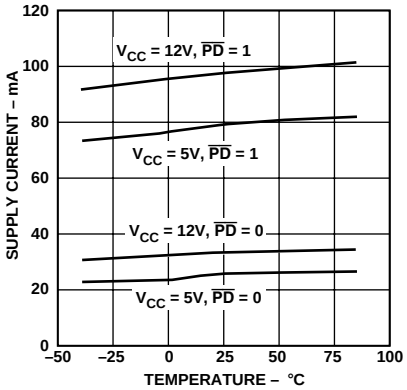


Figure 39. Supply Current vs. Temperature

OPERATIONAL DESCRIPTION

The AD8320 is a digitally controlled variable gain power amplifier that is optimized for driving 75 Ω cable. A multifunctional bipolar device on single silicon, it incorporates all the analog features necessary to accommodate reverse path (upstream) high speed (5 MHz to 65 MHz) cable data modem and cable telephony requirements. The AD8320 has an overall gain range of 36 dB (–10 dB to 26 dB) and is capable of greater than 100 MHz of operation at output signal levels exceeding 18 dBm. Overall, when considering the device's wide gain range, low distortion, wide bandwidth and variable load drive, the device can be used in many variable gain block applications.

The digitally programmable gain is controlled by the three wire "SPI" compatible inputs. These inputs are called SDATA (serial data input port), $\overline{\text{DATEN}}$ (data enable low input port) and CLK (clock input port). See Pin Function Descriptions and Functional Block diagram. The AD8320 is programmed by an 8-bit "attenuator" word. These eight bits determine the 256 programmable gain settings. See attenuator core description below. The gain is linear in V/V/LSB and can be described by the following equation:

$$A_V = 0.316 + 0.077 \times Code \ (R_L = 75\ \Omega)$$

where *code* is the decimal equivalent of the 8-bit word. For example, if all 8 bits are at a logic "1," the decimal equivalent is 255 and A_V equals 19.95 V/V or 26 dB. The gain scaling factor is 0.077 V/V/LSB, with an offset of 0.316 V/V (–10.0 dB). Figure 40 shows the linear gain versus decimal code and Figure 41 shows the gain in dB versus decimal code. Note the nonlinearity that results when viewed in dB versus code. The dB step size increases as the attenuation increases (i.e., gain decreases) and reaches a maximum step size of approximately 1.9 dB (gain change between 01 and 00 decimal).

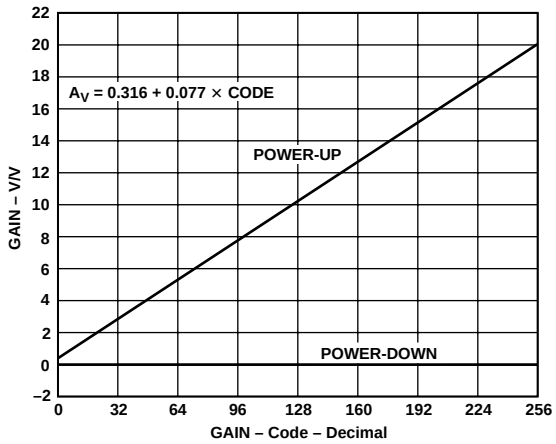


Figure 40. Linear Gain vs. Gain Control

The AD8320 is composed of three analog functions in the power-up or forward mode (Figure 42). The input inverter/buffer amplifier provides single-ended to differential output conversion. The output signals are nominally 180 degrees out of phase and equal in amplitude with a differential voltage gain of 2 (6 dB). Maintaining close to 180 degrees and equal amplitude is required for proper gain accuracy of the attenuator core over the specified operating frequency. The input buffer/inverter also provides equal dc voltages to the core inputs via the internal reference. This is required to ensure proper core linearity over the full specified power supply range (5 V to 12 V).

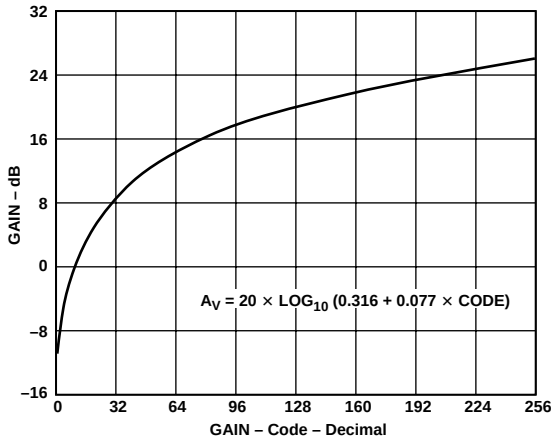


Figure 41. Log Gain vs. Gain Control

The attenuator core can be viewed as eight binarily weighted (differential in–differential out) transconductance (gm) stages with the "in phase" current outputs of all eight stages connected in parallel to their respective differential load resistors (not shown). The core *differential* output signals are also 180 degrees out of phase and equal in amplitude. The input stages are likewise parallel, connected to the inverting input amplifier and buffer outputs as shown. Nine bits plus of accuracy is achieved for all gain settings over the specified frequency, supply voltage and temperature range. The actual total core GM × RL attenuation is determined by which combination of binarily weighted gm stages are selected by the data latch. With 8 bits, 256 levels of attenuation can be programmed. This results in a 36 dB attenuation range (0 dB to –36 dB). See gain equation above.

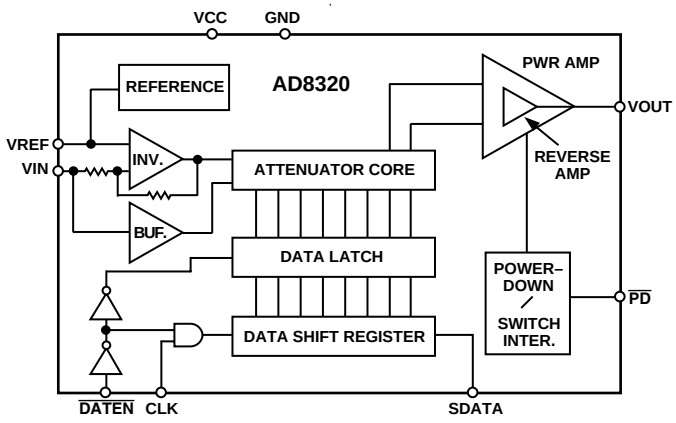


Figure 42. Functional Block Diagram

To update the AD8320 gain, the following digital load sequence is required. The attenuation setting is determined by the 8-bit word in the data latch. This 8-bit word is serially loaded (MSB first) into the shift register at each rising edge of the clock. See Figure 43. During this data load time (T), $\overline{\text{DATEN}}$ is low and the data latch is latched holding the previous (T – 1) data word keeping the attenuation level unchanged. After eight clock cycles the new data word is fully loaded and $\overline{\text{DATEN}}$ is switched high. This enables the data latch (becomes transparent) and the loaded register data is passed to the attenuator with the updated gain value. Also at this $\overline{\text{DATEN}}$ transition, the internal clock is disabled, thus inhibiting new serial input data.

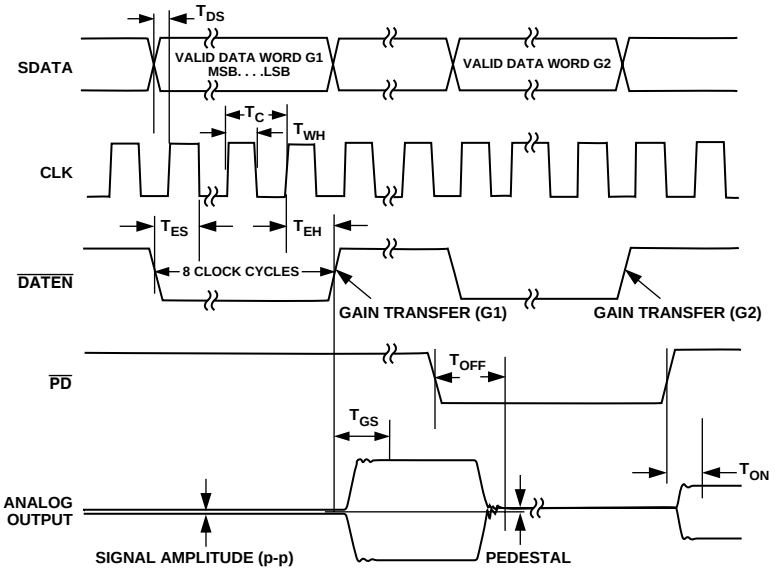


Figure 43. Serial Interface Timing

The power amplifier has two basic modes of operation; forward or power-up mode and reverse or power-down mode. In the power-up mode ($\overline{PD}$ = 1), the power amplifier stage is enabled and the differential output core signal is amplified by 20 dB. With a core attenuation range of 0 dB to –36 dB and 6 dB of input gain, the overall AD8320 gain range is 26 dB to –10 dB. In this mode, the single-ended output signal maintains a dc level of VCC/2. This dc output level provides for optimum large signal linearity and allows for dc coupling the output if necessary. The output stage is unique in that it maintains a dynamic output impedance of 75 Ω. This allows for a direct 75 Ω cable connection and results in 6 dB of added load power versus using a series 75 Ω back-termination resistor as required with traditional low output impedance amplifiers. The power amplifier will also drive lower or higher output loads, although the device's gain (not gain range) will change accordingly (see Applications section).

In the power-down mode ($\overline{PD}$ = 0), the power amplifier is turned off and a "reverse" amplifier (the inner triangle in Figure 42) is enabled. During this 1 to 0 transition, the output power amplifier's input stage is also disabled, resulting in no forward output signal (S21 is 0), although the attenuator core and input amplifier/buffer signals are not affected (S11 ≈ 0). The function of the reverse amplifier is to maintain 75 Ω and VCC/2 at the output port (VOUT) during power-down. This is required to minimize line reflections (S22 ≈ 0) and ensures proper filter operation for any forward mode device sharing the same bus (i.e., in a multiplexed configuration). (See Applications section.) In the time domain, as $\overline{PD}$ switches states, a transitional glitch and pedestal offset results. (See Figures 31 and 43.) The powered down supply current drops to 32 mA versus 97 mA (V_{CC} = 12 V) in power-up mode.

Generally, using the power-down low input ($\overline{PD}$) for switching allows for multiple devices to be multiplexed via splitters (N-1 off, 1 on) and reduces overall total power consumption as required for cable data applications. For cable telephony, the power-down current generally needs to be much lower during what is referred to as sleep and standby modes, and VCC supply switching via PFETS or equivalent, as described in the applications section, would be required.

APPLICATIONS

The AD8320 is primarily intended to be used as the return path (also called upstream path) line driver in cable modem and cable telephony applications. Data to be transmitted is modulated in either QPSK or QAM format. This is done either in DSP or by a dedicated QPSK/QAM modulator such as the AD9853.

The amplifier receives its input signal either from the dedicated QPSK/QAM modulator or from a DAC. In both cases, the signal must be low-pass filtered before being applied to the line driving amplifier.

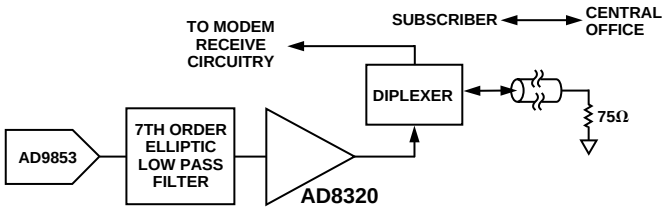


Figure 44. Block Diagram of Cable Modem's Upstream Driver Section

The amplifier drives the line through a diplexer. The insertion loss of a diplexer is typically –3 dB. As a result, the line driver must deliver a power level roughly 3 dB greater than required by the applicable cable modem standard so that diplexer losses are canceled out.

Because the distance to the central office varies from subscriber to subscriber, signals from different subscribers will be attenuated by differing amounts. As a result, the line driver is required to vary its gain so that all signals arriving at the central office have the same amplitude.

Basic Connection

Figure 45 shows the basic schematic for operating the AD8320. Because the amplifier operates from a single supply, the input signal must be ac-coupled using a 0.1 µF capacitor. The input pin has a bias level of about 1.9 V. This bias level is available on the VREF pin (Pin 18) and can be used to externally bias signals if dc-coupling is desired. Under all conditions, a 0.1 µF decoupling capacitor must be connected to the VREF pin. If the VREF voltage is to be used externally, it should be buffered first.

The VIN pin of the AD8320 (Pin 19) has an input impedance of 220 Ω. Typically, in video applications, 75 Ω termination is favored. As a result, an external shunt resistance (R1) to ground of 115 Ω is required to create an overall input impedance of 75 Ω. If 50 Ω termination is required, a 64.9 Ω shunt resistor should be used. Note, to avoid dc loading of the VIN pin, the ac-coupling capacitor should be placed between the input pin and the shunt resistor as shown in Figure 45.

On the output side, the VOUT pin also has a dc bias level. In this case the bias level is midway between the supply voltage and ground. The output signal must therefore be ac-coupled before being applied to the load. The dc bias voltage is available on the VOCM pin (Pin 5) and can be used in dc-coupled applications. This node must be decoupled to ground using a 0.1 µF capacitor. If the VOCM voltage is to be used externally, it should be buffered.

Since the AD8320 has a dynamic output impedance of 75 Ω, no external back termination resistor is required. If the output signal is being evaluated on 50 Ω test equipment such as a spectrum analyzer, a 75 Ω to 50 Ω adapter (commonly called a pad) should be used to maintain a properly matched circuit.

Varying the Gain

The gain of the AD8320 can be varied over a range of 36 dB, from –10 dB to +26 dB, by varying the 8-bit gain setting word.

The timing diagram for AD8320's serial interface is shown in Figure 43.

The write cycle to the device is initiated by the falling edge of $\overline{\text{DATEN}}$. This is followed by eight clock pulses that clock in the control word. Because the clock signal is level triggered, data is effectively clocked on the falling edge of CLK.

After the control word has been clocked in, the $\overline{\text{DATEN}}$ line goes back high, allowing the gain to be updated (this takes about 30 ns).

The relationship between gain and control word is given by the equation:

$$Gain\ (V/V) = 0.077 \times Code + 0.316$$

where *code* is the decimal equivalent of the gain control word (0 to 255).

The gain in dB is given by the equation:

$$Gain\ (dB) = 20 \log_{10} (0.077 \times Code + 0.316)$$

The digital interface also contains an asynchronous power-down mode. The normally high $\overline{\text{PD}}$ line can be pulled low at any time. This turns off the output signal after 45 ns, and reduces the quiescent current to between 25 mA and 32 mA (depending upon the power supply voltage). In this mode, the programmed gain is maintained.

Clock Line Feedthrough

Clock feedthrough results in a 5 mV p-p signal appearing superimposed on the output signal (see Figure 32). If this impinges upon the dynamic range of the application, the clock signal should be noncontinuous, i.e., should only be turned on for eight cycles during programming.

Power Supply and Decoupling

The AD8320 should be powered with a good quality (i.e., low noise) single supply of between +5 V and +12 V. In order to achieve an output power level of +18 dBm (6.2 V p-p) into

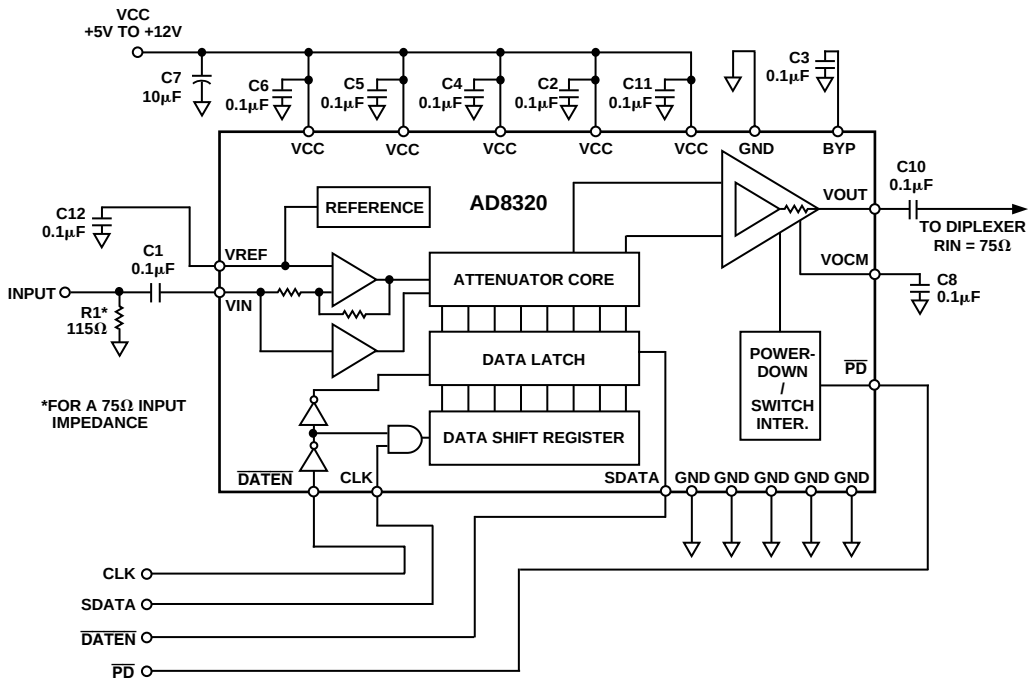


Figure 45. Basic Connection

75 Ω, a supply voltage of at least +10 V is required. To achieve a signal level of +12 dBm (about 3.1 V p-p) into 75 Ω, a minimum supply level of +5 V is required. However, for the lowest possible distortion, the power supply voltage should be raised as high as possible. In varying the power supply from +5 V to +12 V, the quiescent current increases from 80 mA to 97 mA.

Careful attention must be paid to decoupling the power supply pins. A 10 µF capacitor, located fairly close to the device, is required to provide good decoupling for lower frequency signals. In addition, five 0.1 µF decoupling capacitors should be located close to each of the five power supply pins (7, 8, 9, 17 and 20). A 0.1 µF capacitor must also be connected to the pin labeled BYP (Pin 14), to provide decoupling to an internal node of the device. All six ground pins should be connected to a low impedance ground plane.

Alternative Power-Down Mode

As previously mentioned, the AD8320 can be put into a low power sleep mode by pulling the $\overline{PD}$ pin low. If lower power consumption is required during power-down mode, an alternative scheme can be used as shown in Figure 46.

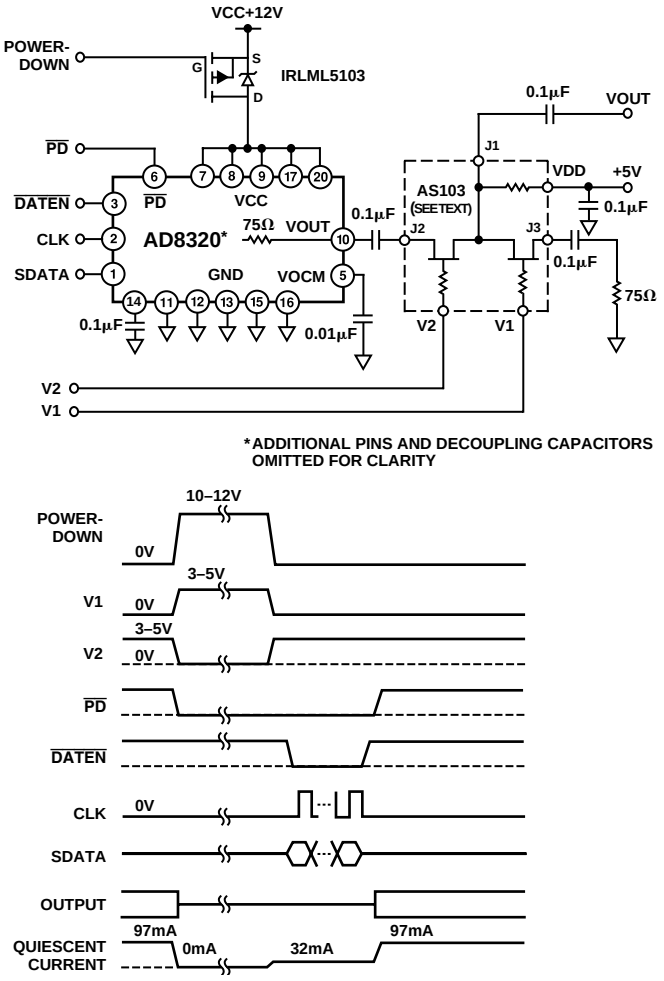


Figure 46. Alternative Power-Down Mode with Timing

A HEXFET power MOSFET (International Rectifier part number IRLML5103) is used to turn on and off the current to the supply pins of the AD8320. Under normal operating conditions, the gate (labeled POWER-DOWN) should be grounded. Pulling the gate to within 2 V of the supply will open the switch and reduce the current to the amplifier to zero.

In cable modem and cable telephony applications the modem must always present an output impedance of 75 Ω to the line. This forces the line driver to always present a 75 Ω impedance to the diplexer. In this application, a single pole double throw RF switch (AS103, Alpha Semiconductor) is used to switch in an external 75 Ω impedance when the AD8320 is turned off. This resistor then mimics the dynamic output impedance of the AD8320. TTL or CMOS logic can be used to drive the two voltages driving the RF switch (V1 and V2).

Before the AD8320 is turned back on again, the gain needs to be set to a known level. This can be done by holding the $\overline{PD}$ pin of the AD8320 low after POWER-DOWN has gone high. While $\overline{PD}$ is held low, the 8-bit serial data stream can be clocked into the AD8320. During this time the quiescent current will increase to 32 mA. However, this time period can be as small as about 1 µs. In this mode the output settles about 45 ns after the rising edge of $\overline{PD}$.

Alternatively, if $\overline{DATEN}$ is held low as the AD8320 is powered on, the device will power up in minimum gain. In this mode, the output settles after about 200 µs. Note that for both cases, the capacitor on VOCM has been reduced from 0.1 µF to 0.01 µF to facilitate a faster turn-on time. All other capacitors in the circuit should be connected as shown in Figure 45.

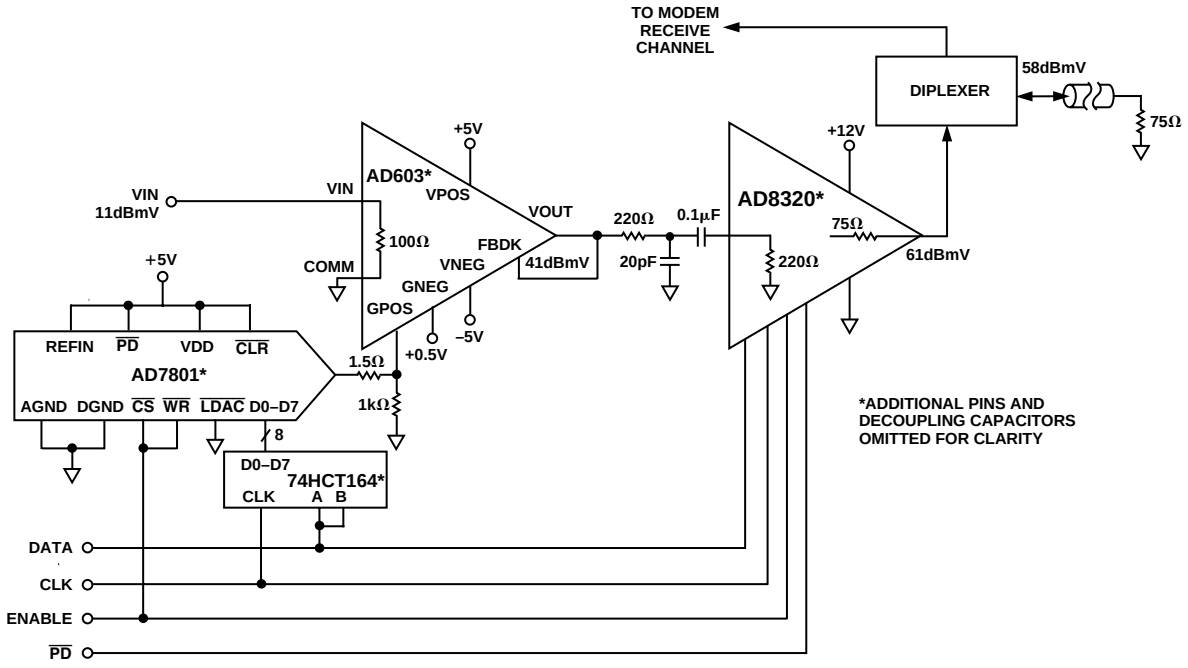


Figure 47. Enhanced Dynamic Range Circuit

Enhanced Dynamic Range Application

The AD8320 can be combined with the AD603 to give additional dynamic range as shown in Figure 47. The AD603 is a voltage controlled variable gain amplifier. The gain of the AD603 is determined by the difference in voltage between the GPOS and GNEG pins. This differential voltage has a range of ±0.5 V. In this example, the voltage on GNEG is tied to +0.5 V. As the voltage on GPOS is varied from 0 V to 1 V, the gain of the AD603 changes from –10 dB to +30 dB with a slope of 25 mV/dB (i.e., linear in dB). The gain control voltage is supplied by the AD7801 DAC. The output voltage of the DAC (0 V to +2.5 V) is divided down to fit the 0 V to 1 V range of the AD603 using a resistor attenuator network.

In order that the same gain control word can be used for both the AD603 and the AD8320, the serial data stream is converted to the parallel format of the AD7801 DAC using a serial-to-parallel shift register. The rising edge of the enable pulse simultaneously updates both amplifiers.

As the control word is varied from 00Dec to 255Dec, the gain of the signal chain varies from –26 dB to +50 dB (there is 6 dB of attenuation between AD603 and AD8320). In practice, this circuit is not usable at the lower end of the gain range due to the small input signal (11 dBmV or about 10 mV p-p). Figure 48 shows the spectrum of the output signal at a frequency of 42 MHz and an output level of 61 dBmV (3.1 V p-p, max gain).

The gain vs. code transfer function of the two amplifiers along with the overall gain is shown in Figure 49. The overall gain transfer function combines a linear in dB transfer function with a linear in Volts/Volt transfer function. It is clear from Figure 49 that the overall gain transfer function can be considered to be approximately linear in dB over the top 50 dB of its range.



Figure 48. Output Spectrum of Enhanced Dynamic Range Circuit (Output Level = 61 dBmV, Frequency = 42 MHz)

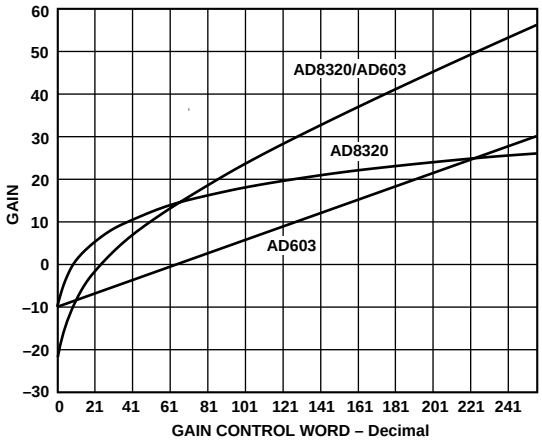


Figure 49. Gain Transfer Function of Enhanced Dynamic Range Circuit

Varying Gain by Varying Load Impedance

As already mentioned, the AD8320 has a dynamic output impedance of 75 Ω. The specified gain range assumes that the output is terminated with a 75 Ω load impedance. Varying the load impedance allows the gain to be varied, up to a maximum of twice the specified gain (for $R_L = \infty$). The variation in gain with load resistance is shown in Figure 50 for the case of a gain control word of 255Dec (i.e., max gain).

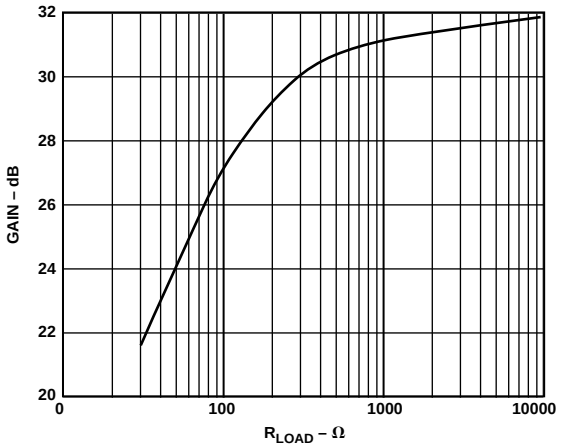


Figure 50. Gain vs. R_{LOAD} (Gain Control Word = 255Dec)

The gain can be described by the following equation:

$$A_V = 20 \log_{10} \left[\left(\frac{2 R_{LOAD}}{R_{LOAD} + 75} \right) \left(0.316 + 0.077 \times Code \right) \right]$$

where *Code* is the decimal equivalent of the 8-bit word.

Evaluation Board

A two layer evaluation board for the AD8320 is available (part number AD8320-EB). This board has been carefully laid out and tested to demonstrate the specified high speed performance of the device. Figure 51 shows the schematic of the evaluation board. The silkscreen for the component side layer is shown in Figure 52. The layout of the board is shown in Figure 53 and Figure 54.

The evaluation board package includes a fully populated board with BNC-type connectors along with Windows®-based software for controlling the board from a PC's printer port via a standard printer cable.

A prototyping area is provided to allow for additional circuitry on the board. The single supply and ground to the board are brought over to this area and are available on two strips. There are also two extra strips available on the prototyping area which can be used for additional power supplies.

The board should be powered with a good quality (i.e., low noise) single supply of between +5 V and +12 V. Extensive decoupling is provided on the board. A 10 µF capacitor, located fairly close to the device, provides good decoupling for lower frequency signals. In addition, and more importantly, five 0.1 µF decoupling capacitors are located close to each of the five power supply pins (7, 8, 9, 17 and 20).

Controlling the Evaluation Board from a PC

The evaluation board ships with Windows-based control software. A standard printer cable can be used to connect the evaluation board to a PC's printer port (also called parallel port). The cable length should be kept to less than about 5 feet. The wiring of a standard printer cable, with respect to the signal lines that are used in this application, is shown in Figure 55. Although the software controls the evaluation board via the PC's parallel port, the AD8320 digital interface is serial. Three of the parallel port's eight bits (and one digital ground line) are used to implement this serial interface. A fourth bit is used to control the $\overline{PD}$ pin.

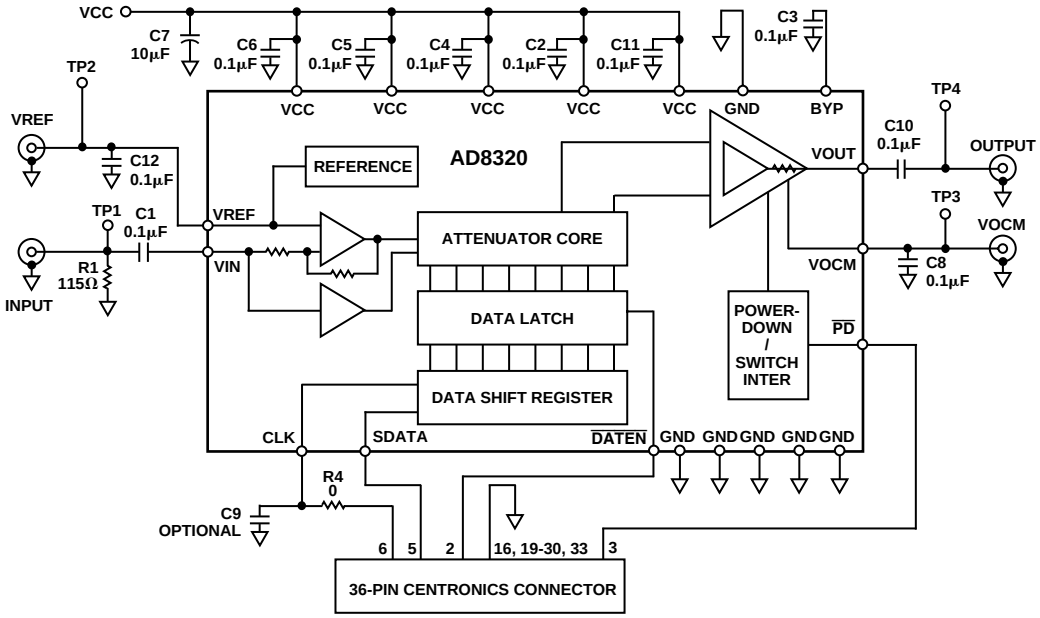


Figure 51. Evaluation Board Schematic

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The control software requires Windows 3.1 or later to operate. To install the software, insert the disk labeled "Disk # 1 of 2" in the PC and run the file called SETUP.EXE. Additional installation instructions will be given on-screen. Before beginning installation, it is important to close any other Windows applications that are running.

When you launch the installed control software from Windows, you will be asked to select the printer port you are using. Most modern PCs have only one printer port, usually called LPT1. However, some laptop computers use the PRN port.

Figure 56 shows the main screen of the control software. Using the slider, you can set any gain in the AD8320's 36 dB range. The gain is displayed on-screen in dB and V/V. The 8-bit gain setting byte is also displayed, in binary, hexadecimal and decimal.

Each time the slider is moved, the software automatically sends and latches the required 8-bit data stream to the AD8320. You can power down or reset the device simply by clicking the appropriate buttons. The software also offers one volatile storage location that can be used to store a particular gain. This functions in the same way as the memory on a pocket calculator.

Overshoot on PC Printer Ports' Data Lines

The data lines on some printer ports have excessive overshoot. Overshoot on the pin used as the serial clock (Pin 6 on the D-Sub-25 connector) can cause communication problems. This overshoot can be eliminated by applying mild filtering to the CLK line on the evaluation board. This can be done by putting a small series resistor on the CLK line, combined with a capacitor to ground. Pads are provided (C9, R4) on the component side of the evaluation board to allow easy insertion of these devices. Determining the size of these values will take some experimentation. Depending upon the overshoot from the printer port, this capacitor may need to be as large as 0.01 μF, while the resistor is typically in the 50 Ω to 100 Ω range.

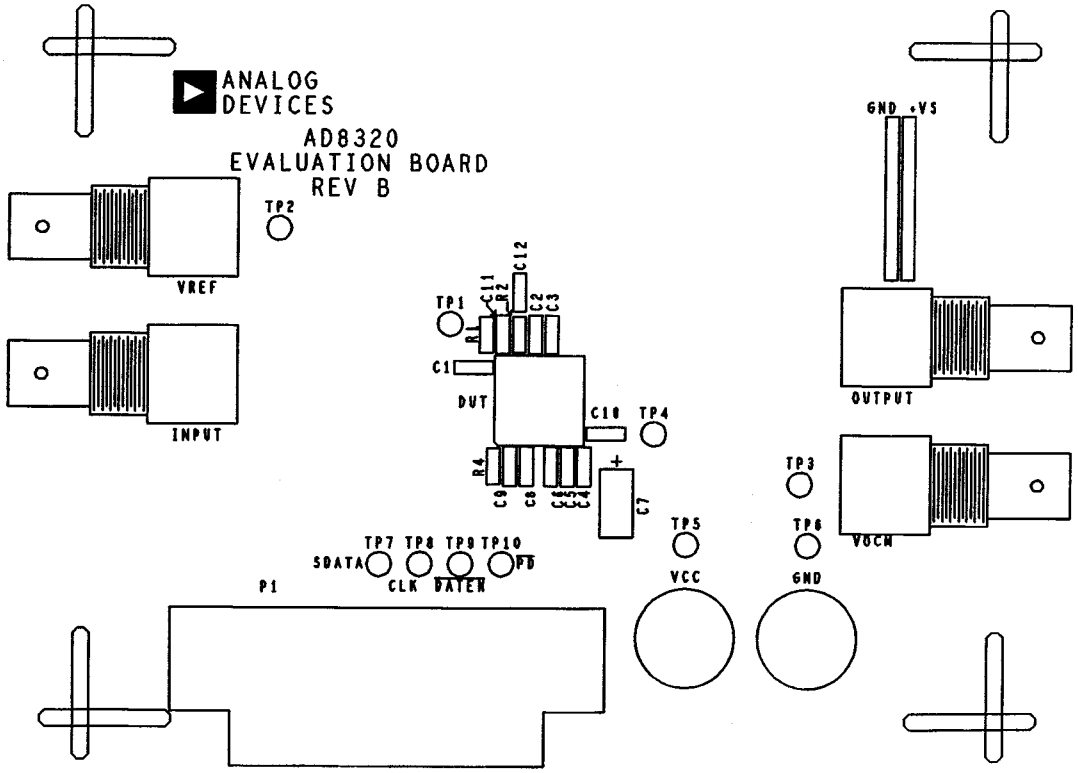


Figure 52. Evaluation Board Silkscreen (Component Side)

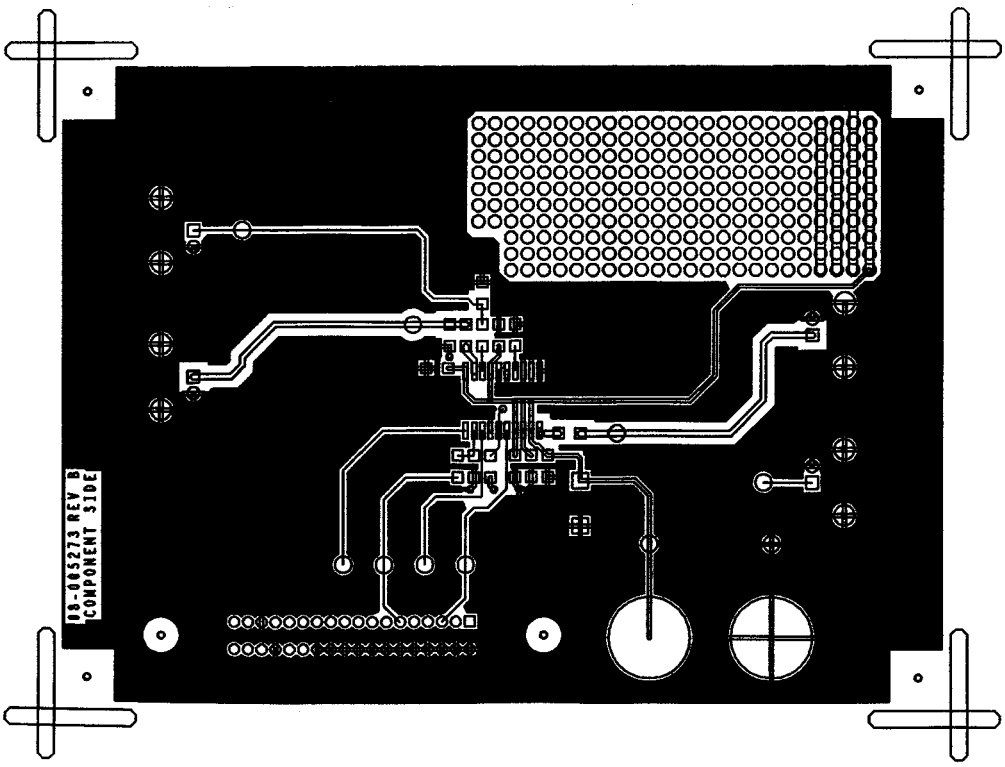


Figure 53. Evaluation Board Layout (Component Side)

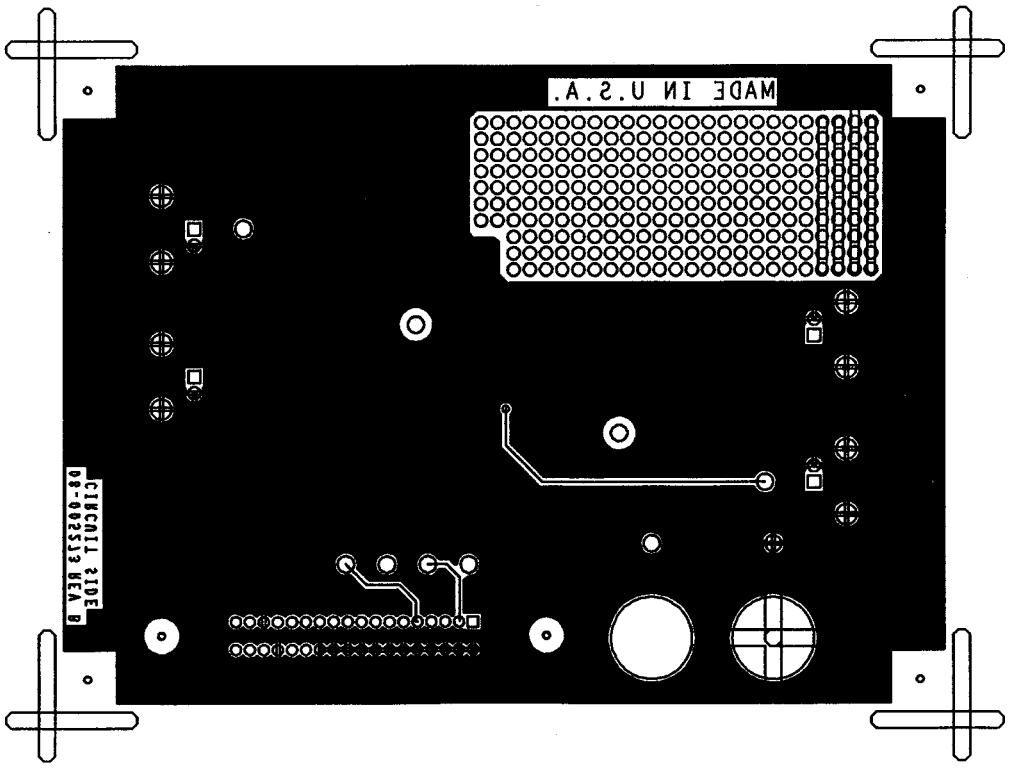
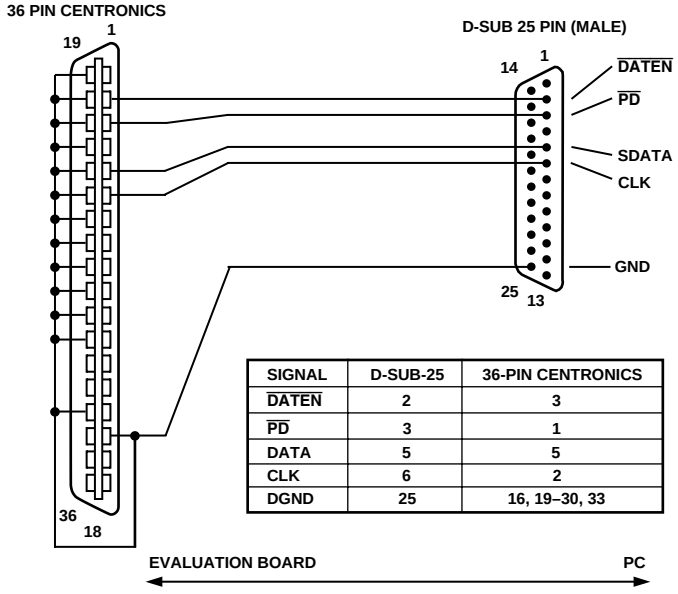


Figure 54. Evaluation Board Layout (Solder Side)



SIGNAL	D-SUB-25	36-PIN CENTRONICS
$\overline{\text{DATEN}}$	2	3
$\overline{\text{PD}}$	3	1
DATA	5	5
CLK	6	2
DGND	25	16, 19–30, 33

Figure 55. Interconnection Between AD8320EB and PC Printer Port

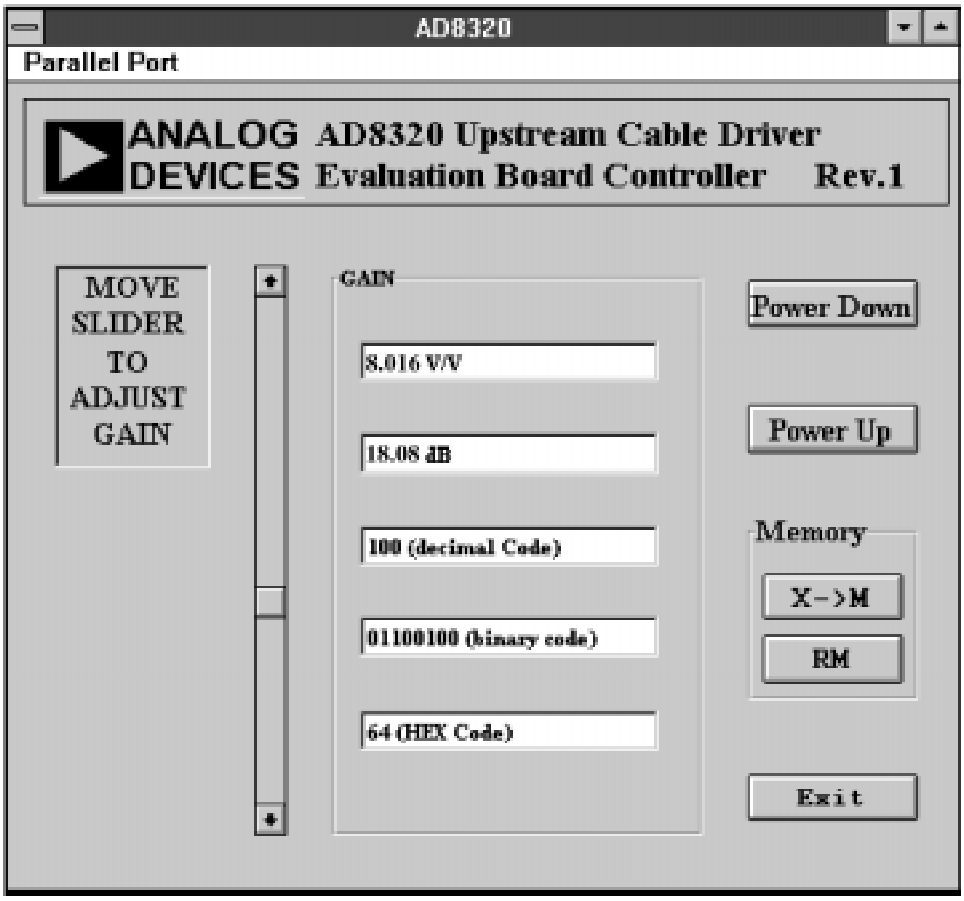
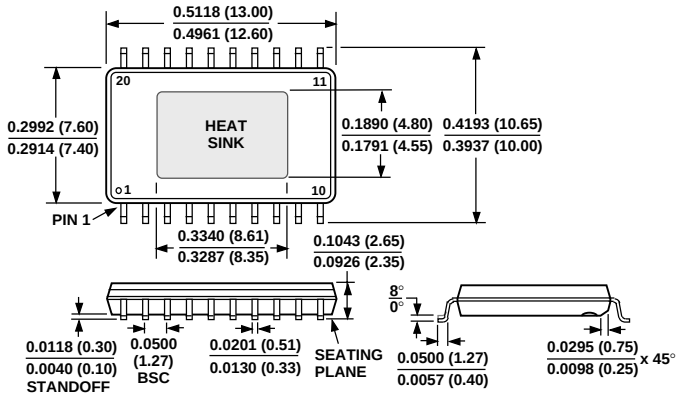


Figure 56. Screen Display of Windows-Based Control Software

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Thermally Enhanced Power Small Outline Package (RP-20)



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Appendix C: Configuration EEPROM Format

C.1 Introduction

All VIM Modules contain an Identification (ID) EEPROM with a checksum stored in the last location. When booted, the VIM baseboard processors check for the presence of VIM modules, through the presence bit on the VIM connector itself. If a module is present, the processor reads the module's ID EEPROM and generates a 16–bit checksum from the results of the readout.

The contents of the ID EEPROM, plus the calculated checksum, are stored in Global SDRAM on the VIM baseboard. Refer to the respective VIM baseboard Operating Manual for the location of the Global SDRAM.

There are three conditions for the checksum: valid checksum (**`0x00EE C0DE`**); bad checksum (**`0x00B ADC5`**); and no VIM module installed (**`0xFFFF FFFF`**). If the generated checksum does not match the stored value, the processor lights its red LED, and places **`BADC5`** in Global SRAM. Even though the processor illuminates LED 0, the red LED, the processor is fully functional.

The ID EEPROM is accessed using a Model 6229 register at memory address VIMReg_base+0x0000, as offset from the VIM base address defined for the applicable VIM baseboard. The bit layout of this register is defined in Table C–1, below.

Table C-1: VIM ID EEPROM Register
R/W @ VIM Address 0x0032 0000

Bit #	D31 - D4	D3	D2	D1	D0
Bit Name	Reserved	Chip Select	Serial Data Out	Reserved	Serial Clock
Access	Read/Write	Read/Write	Read Only	Read/Write	Read/Write
Function	Mask when reading	1 = Selected 0 = Not Selected	Stored Data	Mask when reading	Toggle to pluse Clock line

C.2 EEPROM Format Example

Table C–2 on the next page shows the contents of the EEPROM for the Pentek Model 6229, and an explanation of what each pair of 16–bit words is used for. The SDRAM location is the address where each pair of words is stored relative to the start address of the Global SDRAM on the VIM baseboard.

C.2 EEPROM Format Example (continued)

Table C-2: EEPROM Example (Model 6229 shown)

EEPROM Word Location	SDRAM Location	Contents	Comments
00/01	+0x00	0x00EE C0DE	Valid data flag
02/03	+0x04	0x6229 0000	Model, Model Extension (Extension is currently unused)
04/05	+0x08	0x0354 2001	PCB number. This is taken from the VIM board.
06/07	+0x0C	0x0001 FFFF	Assembly Rev, Option #1: Rev A = 1, B=2, etc. space is allocated for up to 9 installed options.
08/09	+0x10	0xFFFF FFFF	Option #2, Option #3: When there are no options, F's appears in the entire field.
10/11	+0x14	0xFFFF FFFF	Option #4, Option #5
12/13	+0x18	0xFFFF FFFF	Option #6, Option #7
14/15	+0x1C	0xFFFF FFFF	Option #8, Option #9
16/17	+0x20	0xFFFF FFFF	Module Specific Code goes in locations 16 through 61.
18/19	+0x24	0xFFFF FFFF	
20/21	+0x28	0xFFFF FFFF	
22/23	+0x2C	0xFFFF FFFF	
24/25	+0x30	0xFFFF FFFF	
26/27	+0x34	0xFFFF FFFF	
28/29	+0x38	0xFFFF FFFF	
30/31	+0x3C	0xFFFF FFFF	
32/33	+0x40	0xFFFF FFFF	
34/35	+0x44	0xFFFF FFFF	
36/37	+0x48	0xFFFF FFFF	
38/39	+0x4C	0xFFFF FFFF	
40/41	+0x50	0xFFFF FFFF	
42/43	+0x54	0xFFFF FFFF	
44/45	+0x58	0xFFFF FFFF	
46/47	+0x5C	0xFFFF FFFF	
48/49	+0x60	0xFFFF FFFF	
50/51	+0x64	0xFFFF FFFF	
52/53	+0x68	0xFFFF FFFF	
54/55	+0x6C	0xFFFF FFFF	
56/57	+0x70	0xFFFF FFFF	
58/59	+0x74	0xFFFF FFFF	
60/61	+0x78	0xFFFF FFFF	
62/63	+0x7C	0x0000 xxxx	Word 62 should always be cleared (0000). Word 63 contains the byte summation of words 0 - 61.

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