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Model 6235

Dual Wideband Receiver with A/D and FPGA - VIM-2



GateFlow ReadyFlow Board Support Libraries

Features

- Two identical receiver channels include A/D, digital downconverter and a shared FPGA
- Two low distortion 105 MHz 12-bit A/D converters
- Wideband digital downconverters with decimation range from 2 to 64
- Output bandwidths to 40 MHz for 100 MHz sampling clock
- Advanced Virtex-II FPGA for signal preprocessing
- Factory-installed cores available

Ordering Information

Model	Description
6235	Dual Wideband Receiver with A/D and FPGA VIM-2
Options:	
-102	Front panel FPGA I/O (additional slot)
-300	Xilinx XC2V3000 FPGA

General Information

Model 6235 is a dual wideband digital receiver VIM-2 module. It attaches directly to VIM-compatible processor boards and includes a Virtex-II FPGA (Field Programmable Gate Array) and two 12-bit A/Ds.

Front End

The Model 6235 accepts two analog RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors.

Each of the two inputs is transformer coupled, and digitized by an AD9432 12-bit A/D converter. The AD9432 is capable of operating at sample rates to 105 MHz. The A/D converter clock can be driven from an internal crystal oscillator or from an external sample clock supplied through a front panel SMA connector or front panel sync bus.

Digital Downconverter

The digitized output of each A/D feeds the Graychip GC1012B wideband digital downconverter, capable of 40 MHz bandwidth at 100 MHz sampling clock. It offers a programmable decimation range from 2 to 64 and delivers complex 16-bit I and Q samples to the FPGA.

Synchronization

The front panel clock and sync bus allow one 6235 to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling. Multiple slaves can then be clocked synchronously with the master.

Additional sync lines allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and FIFO data collection on multiple 6235's.

FPGA

The downcomverter outputs are delivered to a Xilinx Virtex-II FPGA, Model XC2V1000 (standard) or XC2V3000 (Option -300), which is factory-configured to perform various modes of data packing, formatting and channel selection. The A/D outputs are also connected directly to the FPGA, so that wideband A/D data can be delivered directly to the processor board bypassing the downconverters.

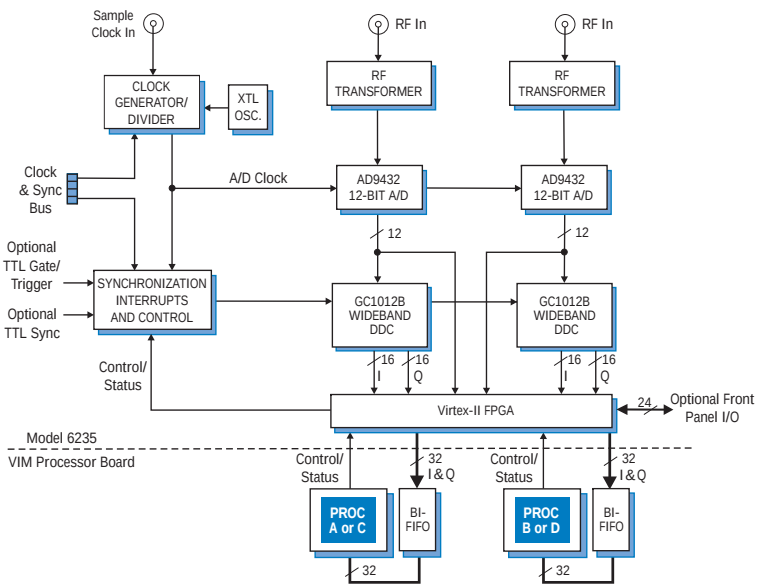
Optionally available GateFlow Design Kits allow the FPGA to be configured by the user for implementation of custom preprocessing functions such as convolution, framing, pattern recognition and decompression.

Front Panel I/O

An optional front panel connector provides digital input and output for the FPGA. These lines are available for triggering, synchronizing, or framing signals. They are also useful during FPGA algorithm development for timing and signal probing.

VIM Processor Interface

The FPGA outputs are connected through the VIM mezzanine interface to the 32-bit synchronous FIFO on the VIM processor board where it is buffered for efficient transfers into the processor. The processor can control the programmable registers on its associated GC1012B, as well as control and initiate sync bus functions.



PENTEK

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458

Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

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