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OPERATING MANUAL

MODEL 6235

Two−Channel Digital Receiver VIM−2 Module
for Pentek VIM Baseboards

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3/14/03	A	Replaced GC1012A Data sheet in Appedix with GC1012B. Added Option 401/404, Ch 6. Corrected Sync/Gate and FPGA connector part numbers, Sect 2.4.3 & 2.4.5, per KBcase 1155. Added VIM base addresses for Pentek baseboards, Sect 3.2.
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Chapter 1: Introduction

1.1 General Description

The Pentek Model 6235 is a general purpose, wideband digital receiver VIM® (Velocity Interface Mezzanine) module. This receiver features two on−board 12−bit, 105−MHz A/D converters, and has two wideband receivers to perform frequency down conversion, low−pass filtering, and decimation of the digitized input signal.

The Model 6235 VIM−2 module attaches directly to VIM−compatible baseboards, including the Pentek Models 4205, and 4290 through 4295 Quad DSP (Digital Signal Processing) boards.

1.2 Features

- Two 105−MHz, 12−bit A/D converters
- Two wideband digital receivers
- Each receiver can select either of the inputs
- 300 kHz to 150 MHz input range (to 500 MHz with Option 050)
- 1.25 MHz to 40 MHz output bandwidth
- Internal or external A/D sample clock to 105 MHz
- Front panel timing and sync bus can synchronize multiple modules
- Advanced Xilinx® Virtex®−II FPGA for signal processing
- Direct connection to two VIM baseboard BIFOs, with no shared bus bottlenecks
- Compliant with VIM−2 module specification



When the Model 6235 is mounted on a standard Model 4290 baseboard, data collection at the maximum sample clock rate (105 MHz) is not recommended. However, on a Model 4290 baseboard with Option 320 or 330, the 6235 will operate at the maximum sample clock rate.

1.3 Analog/Digital Conversion

The Model 6235 accepts two analog RF inputs on front panel SMA connectors in the range of 300 kHz to 500 MHz (with Option 050). Each input is transformer coupled, and then digitized by an AD9432 12−bit, 105−MHz A/D converter. The A/D converter clock can be driven from an internal 100−MHz crystal oscillator, an external sample clock supplied through a front panel SMA connector, or the front panel sync bus.

1.4 Digital Receivers

The Model 6235 includes two Graychip GC1012B wideband digital receiver (DDR) chips, which are individually bypassable. Each GC1012B accepts one 12−bit parallel input from its associated A/D converter. For an input sampling clock of 100 MHz, each receiver is capable of tuning throughout the DC to 50 MHz range, with output bandwidths ranging from 2 MHz to 40 MHz.

1.5 Field Programmable Gate Array

Each GC1012B delivers real or complex parallel data streams into an FPGA (field programmable gate array), where data is formatted for delivery across the VIM interface into the 32−bit parallel Bi−FIFOs (BIFOs) on the VIM baseboard. These Bi−FIFO buffers allow the processors on the VIM baseboard to unload blocks of data efficiently. The AD9432 digital outputs are also connected directly to each FPGA, bypassing the GC1012s, so that A/D data can be delivered directly to the baseboard.

The Model 6235 contains one Xilinx Virtex−II XC2V1000 FPGA. (The Xilinx Model XC2V3000 is optionally available.) The FPGA is factory programmed to implement the standard data formatting, clocking, and control functions specified in this document.

The FPGA can be re−programmed from a processor on the VIM baseboard. Pentek has an available FPGA Design Kit that provides information for the user to modify the programmable logic functions for the Virtex−II FPGA. This allows the user to implement his own algorithms for special timing requirements and for pre−processing of AD9432 or GC1012B output data before sending it to the baseboard BIFOs. Pentek offers this capability as a separate development package, Model 4953 − Option 235. Contact Pentek at (201) 818−5900 for details about this package.

Refer to Section 1.10, FPGA Configuration, for additional information about the gate array configurations.

Options 401 and 404 for the Model 6235 provides a Fast Fourier Transform (FFT) capability programmed into the FPGA using Xilinx Model XC2V3000. See Chapter 6 for description of these options.

1.6 VIM Interface

The digital outputs of the FPGA are connected directly through the VIM interface to the 32−bit synchronous Bi−FIFOs on the VIM baseboard. These Bi−FIFO buffers allow the processors on the VIM baseboard to unload blocks of data efficiently.

Through the VIM interface, baseboard processors can control all programmable regis−ters on the associated GC1012Bs, access FPGA capabilities, control and initiate sync bus functions, and control the board's interrupt functions.

1.7 Timing and Synchronization

The front panel LVDS (low−voltage differential signal) Sync Bus includes sample clock, sync, and gate signals. It allows one Model 6235 to act as a bus master, driving the sample clock out to a front panel flat cable using LVDS differential signaling. The sync line on the bus allows synchronization of the local oscillator phase, frequency switch−ing, decimating filter phase, and BIFO data collection on multiple 6235s. Up to seven slave 6235s can then be driven from the master, supporting synchronous sampling and sync functions across all connected modules. The sync source is connected to the LVDS bus through the FPGA, so that it can be routed to the GC1012B's S−sync (system sync), A−sync (accumulator sync), and G−sync (gain sync) lines under software control. Gates are used to enable writes to the VIM baseboard BIFOs.

A VIM baseboard processor can access all control and status registers to control syn−chronization, gating, triggering, and clocking modes. Baseboard processors can gener−ate sync, gate, and trigger signals for distribution across the LVDS Sync Bus.

In addition to the LVDS Sync Bus signals, the Model 6235 accepts an external sample clock supplied through a front panel SMA connector, and two optional TTL input tim−ing signals, one for external sync and the other external gating or triggering.

Refer to Chapter 5, Timing and Synchronization, for additional information about the use and programming of gate and sync signals.

1.8 Interrupts

The Model 6235 has several maskable interrupt sources. Interrupts may be generated by the A/D converter overload outputs, DDR overflow, transitions on the gate or sync signals, clock loss, or a programmable over−temperature on one of three sensors or a faulty power supply voltage.

The board's programmable Voltage/Temperature Monitor, an ADM1024, provides constant monitoring of critical voltages and temperatures on the PCB. If the voltage or temperature fall outside of the set limits, an interrupt can be generated.

1.9 Block Diagram

The following is a simplified block diagram of the Model 6235 digital receiver, connected to a VIM baseboard.

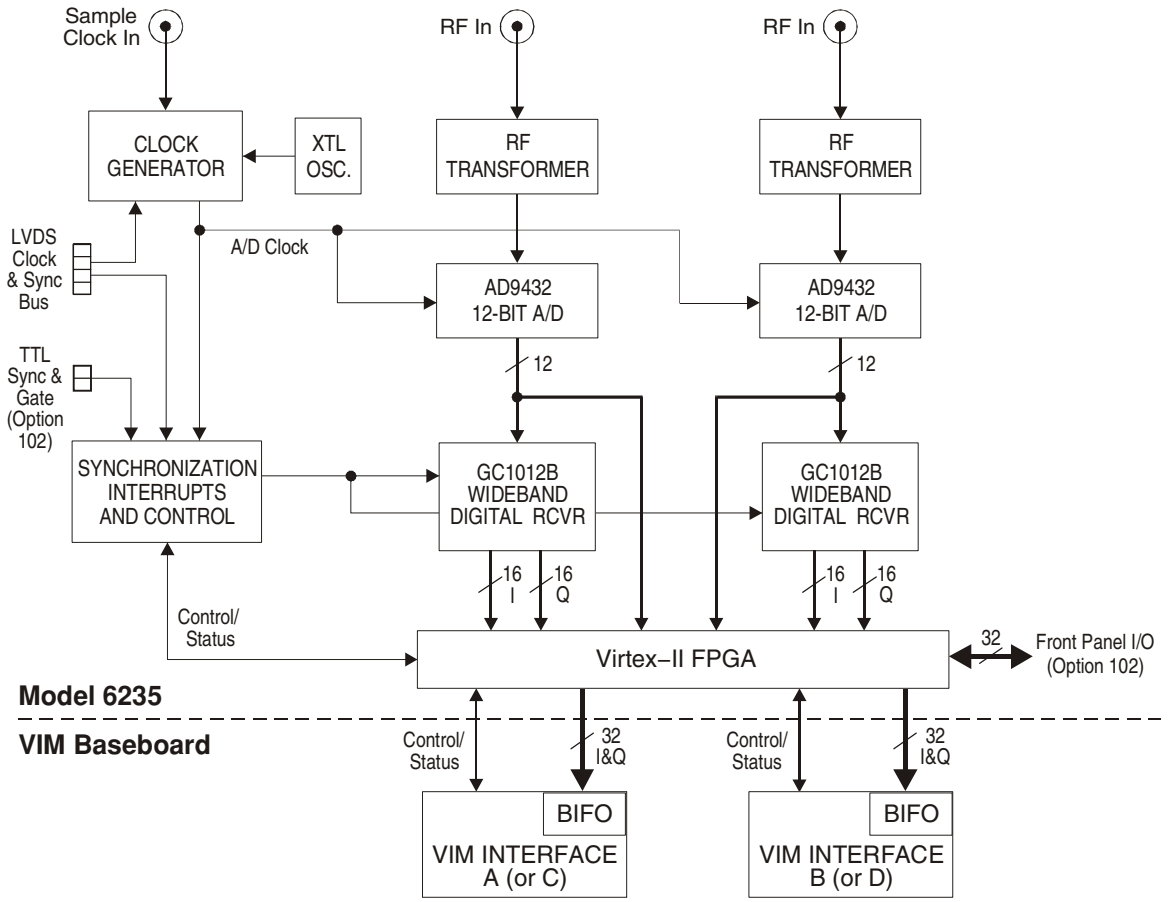


Figure 1–1: Model 6235 Block Diagram

There are two processor channels on the Model 6235, one for each baseboard VIM interface. These are identified as **A** and **B** if your VIM module is installed on the upper VIM position of the baseboard, or **C** and **D** if your VIM module is installed on the lower VIM position of the baseboard. Each processor channel is associated with (and controls) one RF analog input, one GC1012B, and one VIM baseboard BIFO.

1.10 FPGA Configuration

The standard FPGA on the Model 6235 is the Xilinx Virtex−II XC2V1000; the Xilinx Virtex−II XC2V3000 is available as Option 300. The baseline functionality of the Model 6235 consumes approximately 18% of the XC2V1000 or 6% of the XC2V3000.

The Model 6235 is shipped with a default set of logic functions for this FPGA, on a JTAG−programmable serial EEPROM. Upon power−up, this set of default functions is loaded into the FPGA. The FPGA can be configured in several different ways:

- The default method is serial configuration load from the configuration EEPROM. This is the power up mode of the board. Configuration reload may also be forced at any time by a baseboard processor (see Section 3.3).

- The second method, to facilitate development and debugging, is by serial download to the FPGA using a Xilinx Parallel III or MultiLINX™ cable. This method will replace the factory−programmed configuration that loads at power up from the EEPROM, but is volatile and will exist only until the power is turned off.

- The third method is JTAG programming the FPGA using a Xilinx Parallel III or MultiLINX™ cable. This method will replace the factory−programmed configuration that loads at power up from the EEPROM, but does not overwrite the EEPROM. This method is volatile and will exist only until the power is turned off.

- The fourth method is byte−wide upload to the FPGA from a baseboard processor. This is done by the processor writing the configuration data to the FPGA configuration data register (see Section 3.4). For the XC2V1000, about 468 kBytes of FLASH memory on the baseboard is required to hold the FPGA configuration; for the XC2V3000, about 1.2 MBytes is required. This method is also volatile, that is, the new configuration will exist only until the power is turned off.

- The last method is to reconfigure the EEPROM via the JTAG interface with a Xilinx cable, then power−up the board with the new configuration. This overwrites the default configuration by reprogramming the EEPROM. This method, however, is nonvolatile, and will permanently overwrite the factory−programmed configuration in the EEPROM. After turning power off, the FPGA will power up with this new configuration instead of the default configuration the Model 6235 was shipped with.

Pentek has an available FPGA Design Kit for the Model 6235 that provides information for the user to modify the programmable logic functions for the Virtex−II FPGA. This allows the user to implement his own algorithms for special timing requirements and for pre−processing of AD9432 or GC1012B output data. Pentek offers this capability as a separate development package, Model 4953 − Option 235. Contact Pentek at (201) 818−5900 for details about this package.

1.10 FPGA Configuration (continued)

When the Model 6235 is attached to a Pentek VIM baseboard, the standard XC2V1000 FPGA, or the optional XC2V3000 FPGA, provides serial port connectivity as shown in the following illustration.

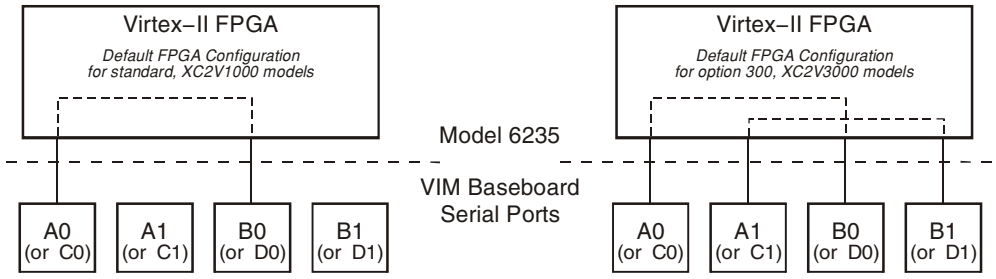


Figure 1–2: Model 6235 FPGA Interconnectivity

Option 102 for the Model 6235 provides an FPGA I/O connector on an additional front panel located in the adjacent VMEbus slot (see Section 2.4). The FPGA I/O pins are split into two groups of 16 pins each, with one group going to each of the two base–board VIM interfaces. The user can configure these FPGA I/O pins as either inputs or outputs (see Section 3.19), on either the XC2V1000 or the XC2V3000 models. The quickswitches and 25–ohm series resistors provide some over–voltage and short pro–tection to the FPGA I/O pins. For convenience, Option 102 also provides a 4–pin TTL Sync/Gate header.

Options 401 and 404 for the Model 6235 provides an XC2V3000 FPGA with a Fast Fou–rier Transform (FFT) capability programmed into the FPGA. Option 401 is a 1024–point FFT, while Option 404 is a 4096–point FFT. Refer to Chapter 6 for description of these options.

1.11 Board Support Software

Pentek's Model 4999 ReadyFlow® Board Support Libraries allow high–level program–ming to speed development tasks. Refer to the ReadyFlow software documentation for the Model 6235 (Pentek part #801.62350) for further description of these capabilities.

An available Pentek Model 4996 VxWorks® Driver allows high–level programming for various workstation platforms. In addition to the feature set provided by the driver, source code is included, allowing users to modify software functionality. Refer to the VxWorks Driver documentation for the Model 6235 (Pentek part #803.62350) for further description of these capabilities.

1.12 Specifications

Front Panel Connectors

Analog Inputs:	Two female SMA connectors (one per A/D converter)
Sample Clock Input:	One female SMA connector
Sync/Gate Bus:	One 26−pin connector, with four gates, one sync, and one clock input/output LVDS signals, plus one sync and one gate input TTL signals

Option 102 Panel Connectors:

TTL Sync/Gate:	One 4−pin header, with one sync and one gate TTL inputs
FPGA Inputs/Outputs:	One 50−pin connector
FPGA Input/Output:	32 pins (16 pins for each baseboard VIM interface)
Max. Load per I/O pin:	20 mA (These pins are connected through IDT Quick Switch P/N QS32245)

Analog Signal Inputs

Quantity:	Two, via front panel SMA connectors
Input Type:	Single−ended, non−inverting
Coupling:	AC
Input Impedance:	50Ω
Full Scale Input:	+4 dBm
Input Bandwidth:	Standard: 150 MHz
	Option 050: 500 MHz (reduces SNR by −10 dB)

Analog Input Transformers

Quantity:	Two (enclosed in a shielded cover)
Type:	ADT4−5WT (Mini−Circuits)
3 dB Passband:	300 kHz to 500 MHz
Input Return Loss:	8.72 dB min., 31.13 dB max.
Bypass:	None

Analog/Digital Converters

Quantity:	Two (enclosed in a shielded cover)
Device:	Analog Devices AD9432 (see Appendix C)
Sampling Rate:	3 MHz to 105 MHz (Lower sampling rates, to 1 MHz, possible with modulated duty cycle)
Resolution:	12 bits
Coupling:	Transformer coupled
Clock Source:	Onboard crystal oscillator, external clock, or LVDS clock

Internal Clock

Frequency:	100−MHz crystal oscillator, better than 100 ppm accuracy

External Clock Input

Type:	Sine Wave
Voltage Range:	0 to 10 dBm
Frequency:	1 MHz to 105 MHz
Impedance:	50Ω, AC coupled

1.12 Specifications (continued)

Gates

Quantity:	Two, one per VIM baseboard BIFO; each baseboard VIM interface can create its own gate
Gate Sources:	Front panel LVDS Sync Bus (four) gate inputs, TTL Gate/Trigger input, or (two) programmable registers
Polarity:	External gate input has programmable polarity
Gate Disable:	Each gate can be disabled by the baseboard processor; when disabled, VIM BIFO writes default to enabled
Triggering:	Each gate can be programmed as a trigger, programmable trigger length up to 16,383 VIM BIFO writes

Digital Receivers

Quantity:	Two receiver chips
Device:	Graychip GC1012B (see Appendix D)
Decimation:	2 to 64
Data Source:	Associated A/D 12−bit parallel output
Clock Source:	A/D clock
Sync:	Maskable inside each GC1012B chip (All receiver channels directed to the same VIM BIFO must be synced at the GC1012B output)
Output:	32 bits parallel complex, 16−bit I, 16−bit Q; Parallel real also available, 16−bit I, 16−bit I
Bypass Mode:	Data from A/D converters can be written directly into the FPGA (bypassing GC1012Bs) at a sample rate equal to the A/D clock decimated by any value from 1 to 4096

Field−Programmable Gate Array

Device:	Standard: Xilinx Virtex−II XC2V1000 Option 300: Xilinx Virtex−II XC2V3000
Programming:	Factory programmed by Pentek (see Section 1.10)

Power Dissipation

For XC2V1000 FPGA w/base circuitry:	8.5 W
For XC2V1000 FPGA w/heavy use:	11.5 W
For XC2V3000 FPGA w/heavy use:	13.5 W

(Note: Estimated at 100MHz; FPGA power consumption varies based on usage)

Physical:

Dimensions	VIM−2 Module
Height:	114.3 mm (4.5 in.)
Depth:	82.5 mm (3.25 in.)
Width:	20.3 mm (0.80 in.)
Weight:	130.4 grams (4.6 oz.)

Environmental:

Operating Temperature:	0° to 50°C
Storage Temperature:	−20° to 90°C
Relative Humidity:	95% non−condensing
VME Rack Exhaust Temp:	0° to 50°C

Chapter 2: Installation and Connections

2.1 Inspection

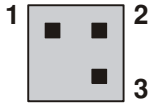
After unpacking, inspect the unit carefully for possible damage to connectors or components. If any damage is discovered, contact Pentek immediately at (201) 818–5900. Please save the original shipping container and packing material in case reshipment is required. The component side of the PCB is illustrated in Figure 2–1 on the next page.

2.2 Jumper Settings

There is only one jumper block on the Model 6235 module that can be set by the user. Do not change jumpers that are not identified in this section—all other jumpers are reserved for factory test and setup purposes only.

Jumper **JB1** selects the source of the Virtex FPGA configuration data download, either from an on–board Serial EEPROM or from a serial download (using a Xilinx cable). Refer to Virtex Config Register, Section 3.3, for further information on configuring the Virtex FPGA. The following table shows the jumper settings for this FPGA configuration data source jumper. This jumper block has three pins. Note the location of pin 1 of the jumper block, which is identified on the PCB (see Figure 2–1 on the next page).

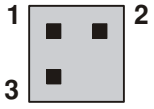
Table 2–1: FPGA Configuration Data Source Jumper



Jumper JB1 Position	FPGA Data Source
1 – 2	Serial Download (Xilinx cable)
Removed, or 2 – 3 *	On–board Serial EEPROM
* Factory Default Setting	

NOTE: On Model 6235 PCBs identified as Revision A, the pin arrangement of the jumper block is different from subsequent revision PCBs. The following table shows the **JB1** pin orientation and settings for the Rev A PCB.

Table 2–2: FPGA Configuration Data Source Jumper – Rev A PCBs



Jumper JB1 Position	FPGA Data Source
1 – 2	Serial Download (Xilinx cable)
Removed, or 1 – 3 *	On–board Serial EEPROM
* Factory Default Setting	

2.2 Jumper Settings (continued)

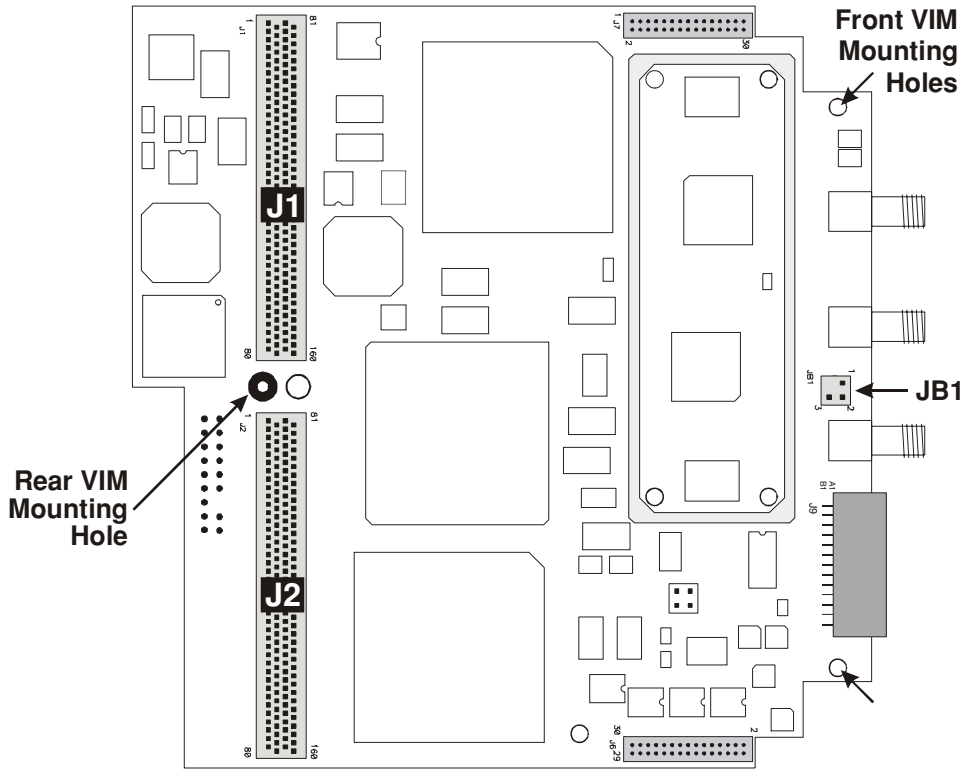


Figure 2–1: Model 6235 Module Assembly Drawing, Component Side

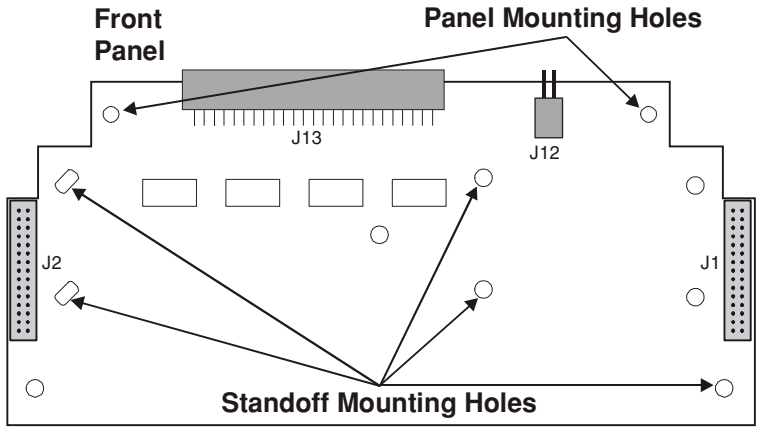


Figure 2–2: Model 6235 Option 102 PCB Assembly, Component Side

2.3 Installing the Model 6235 on a VIM Baseboard

This section provides instructions for installing the Model 6235 VIM–2 module on a VIM–compatible baseboard. Pentek's VIM baseboards ship with two blank panel inserts and four VIM interface connectors where you can install VIM modules such as the Model 6235. See Figure 2–3, on the next page, for illustration of a typical Pentek VIM baseboard.

CAUTION

Perform all assembly steps at an antistatic workstation.

Tools required for all procedures:

- #1 Phillips screwdriver
- Flat–blade screwdriver (blade width 5/16–inch or less)

The Model 6235 is shipped in different configurations. The installation instructions vary according to the configuration you receive from Pentek, as follows:

❑ If you have ordered a Model 6235 **without** Option 102, you have received a single VIM module that you must mount on your existing VIM baseboard.

Refer to Section 2.3.1 for the instructions for this configuration.

❑ If you have ordered a Model 6235 **with** Option 102, you have received an assembly of a Model 6235 PCB and an Option 102 PCB, plus a front panel assembly. You must disassemble these components to mount them onto your existing VIM baseboard.

Refer to Section 2.3.2 for the instructions for this configuration.

NOTE: Be sure to follow all instructions in the order presented.

All required mounting hardware and front panels are included in your shipment.

2.3 Installing the Model 6235 on a VIM Baseboard (continued)

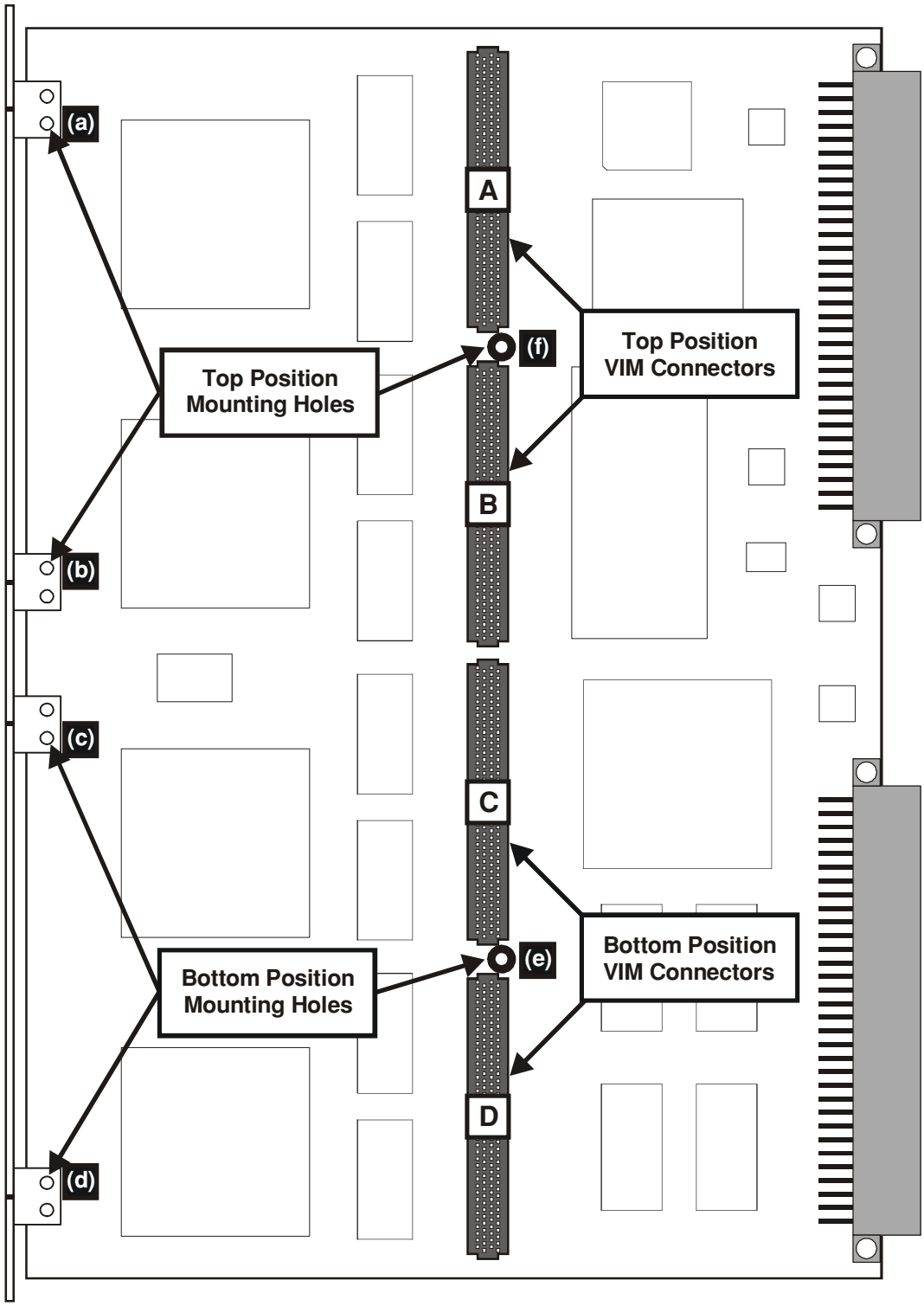


Figure 2–3: Typical VIM Baseboard – Connectors & Mounting Holes

2.3 Installing the Model 6235 on a VIM Baseboard (continued)

2.3.1 Installing Model 6235 without Option 102

This section provides instructions for installing the Model 6235 VIM–2 (without Option 102) on your existing VIM baseboard.

The Model 6235 module is shipped as an assembled unit and must be disas–sembled for installation on your VIM baseboard.

1) Remove the front panel from the Model 6235 VIM–2 module by removing the two countersunk Phillips screws from the panel (see figure below).

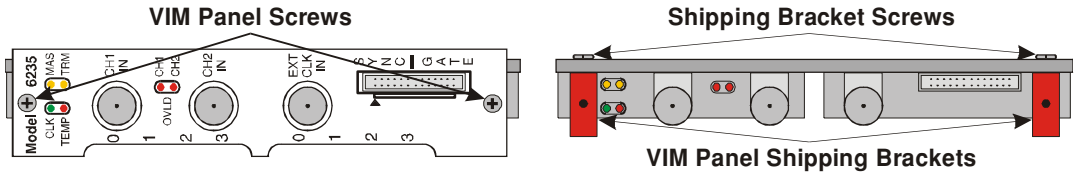


Figure 2–4: Model 6235 Panel Mounting and Shipping Screws
(Shown with panel removed, at right)

2) Remove the (red) shipping brackets that hold the front panel to the VIM–2 module by removing the pan–head Phillips shipping bracket screws from the solder side of the Model 6235 PCB (see figure above). Set these screws aside, as they are used to secure the VIM module to the VIM baseboard.

   (The shipping brackets may be discarded, or saved to store the panel back on the VIM module if it is removed from the VIM baseboard.)

3) A nylon spacer is installed on the component side of the Model 6235 PCB, between the VIM connectors (see Figure 2–5 on the following page). Remove the nylon screw that is threaded into the top of the spacer from the component side. Set this screw aside, as it is used to secure the VIM module to the VIM baseboard.

2.3 Installing the Model 6235 on a VIM Baseboard (continued)

2.3.1 Installing Model 6235 without Option 102 (continued)

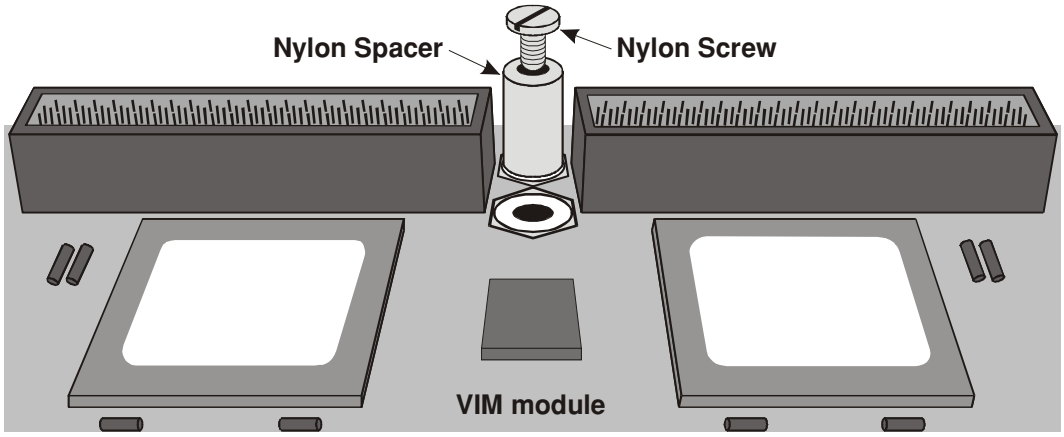


Figure 2–5: VIM Module Nylon Spacer



The nylon spacer must be installed in the hole at the REAR of the VIM connectors, farthest from the front panel (as illustrated above and indicated at position (a) in Figure 2–1 on page 18).

If the spacer is installed in the front hole, reposition it by removing the nylon screw on the solder side of the module and threading it back into the spacer through the rear hole.

4) Remove one blank panel insert from your VIM baseboard, at the VIM position you wish to install the Model 6235 module, by removing the two countersunk Phillips screws from the panel insert (see figure below).

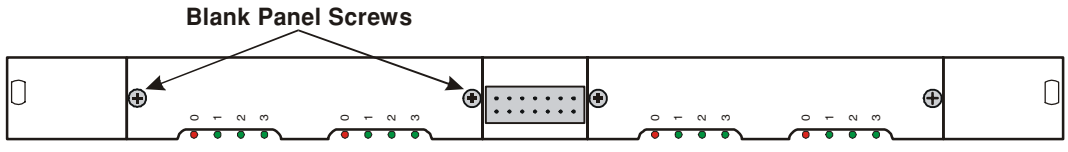


Figure 2–6: VIM Baseboard Blank Panel Screws

2.3 Installing the Model 6235 on a VIM Baseboard (continued)

2.3.1 Installing Model 6235 without Option 102 (continued)

5) With the VIM baseboard's component side (the side with the VIM connectors) facing up, align the two VIM connectors on the Model 6235 VIM−2 module (**J1** and **J2**) with two VIM connectors on the baseboard. The Model 6235 VIM−2 module may be installed in either the top or bottom mezzanine position on the VIM baseboard. See Figure 2−1 for location of the Model 6235 VIM connectors; see Figure 2−3 for location of the VIM connectors on a typical VIM baseboard.

6) **GENTLY but firmly**, press down on the VIM module opposite the connectors to fully seat the module's connectors into the baseboard. If you meet with significant resistance, check the connector alignment.

> **NOTE:** Misalignment can cause bent pins or break connector housings, so **NEVER APPLY EXCESSIVE FORCE**.

7) After seating the connectors, secure the front of the VIM module to the VIM baseboard by screwing two short pan−head Phillips screws through the mounting holes in the front of the VIM module (see figure below and Figure 2−1), into the threaded holes in baseboard's panel brackets (indicated at positions (a) and (b), or (c) and (d) on Figure 2−3).

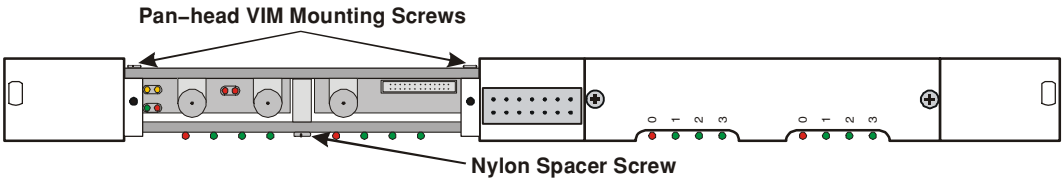


Figure 2−7: Model 6235 Mounted on VIM Baseboard
(Model 6235 illustrated in upper VIM position)

8) Turn the assembly over, such that the VIM module is on the work surface and the solder side of the VIM baseboard is facing up. Secure the baseboard to the nylon spacer on the VIM module, using the nylon screw removed earlier (see figure above), through the rear mounting hole on the baseboard (indicated at position (e) or (f) on Figure 2−3).

9) Attach the Model 6235 VIM module's front panel to the baseboard, by screwing the countersunk Phillips screws through the holes of the VIM panel, into the threaded holes in the baseboard's front panel brackets.

The Model 6235 installation is complete.

2.3 Installing the Model 6235 on a VIM Baseboard (continued)

2.3.2 Installing Model 6235 with Option 102

The Model 6235 with Option 102 is shipped as an assembled unit and must be disassembled for installation. A separate Option 102 front panel assembly is also provided.

1) Remove both front panels from the Model 6235 VIM–2 module and the Option 102 module by removing the two countersunk Phillips screws from each panel (see figure below).

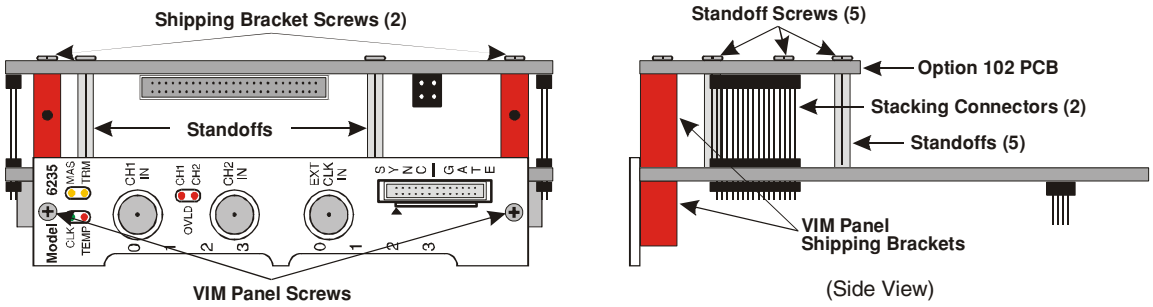


Figure 2–8: Model 6235 with Option 102 Shipping Assembly
(Shown with Option 102 panel removed)

2) Remove the (red) shipping brackets that hold the front panels to both modules by removing the pan–head Phillips shipping bracket screws from the solder side of the Option 102 PCB (see figure above).

   (The shipping brackets may be discarded, or saved to store the panels if they are removed from the VIM baseboard.)

3) Remove and set aside the five pan–head Phillips standoff screws from the top of the Option 102 board (see figure above).

4) **CAREFULLY**, remove the Option 102 board from the stacking connectors (see figure above), taking care to not bend the pins.

5) **GENTLY**, remove and set aside both stacking connectors from the Model 6235 PCB. Do not remove the five (black) metal standoffs from this PCB.

CAUTION

Be careful when removing the stacking connectors, as they are fragile and can easily be damaged.

2.3 Installing the Model 6235 on a VIM Baseboard (continued)

2.3.2 Installing Model 6235 with Option 102 (continued)

6) A nylon spacer is installed on the component side of the Model 6235 PCB, between the VIM connectors. Remove and set aside the nylon screw that is threaded into the top of the spacer (see figure below).

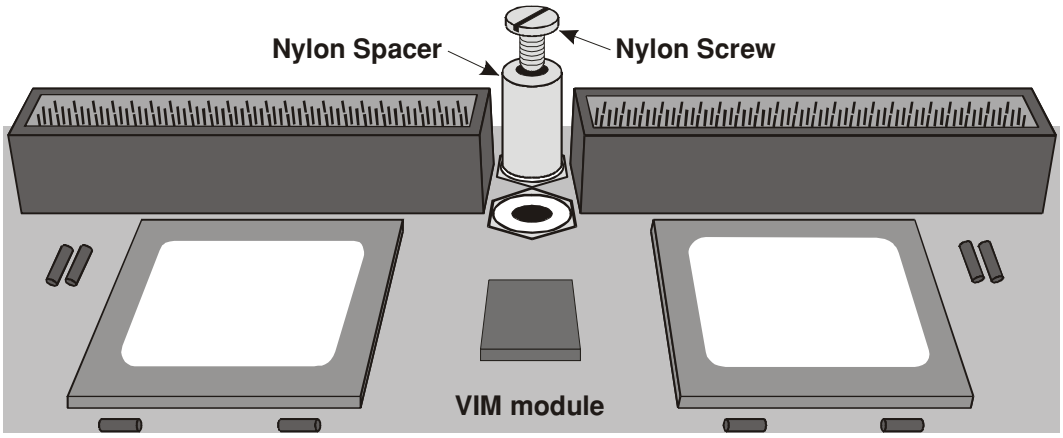


Figure 2–9: VIM Module Nylon Spacer



The nylon spacer must be installed in the hole at the REAR of the VIM connectors, farthest from the front panel (as shown in the figure above).

If the spacer is installed in the front hole, reposition it using the nylon screw on the solder side of the module.

7) Remove one blank panel insert from your VIM baseboard, at the VIM position you wish to install the Model 6235 module, by removing the two countersunk Phillips screws from that panel insert (see figure below).

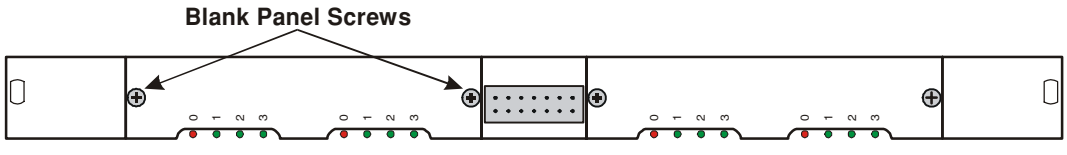


Figure 2–10: VIM Baseboard Blank Panel Screws

2.3 Installing the Model 6235 on a VIM Baseboard (continued)

2.3.2 Installing Model 6235 with Option 102 (continued)

8) With the VIM baseboard's component side (the side with the VIM connectors) facing up, align the two VIM connectors on the Model 6235 VIM–2 module (**J1** and **J2**) with two VIM connectors on the baseboard. The Model 6235 VIM–2 module may be installed in either the top or bottom mezzanine position on the VIM baseboard. See Figure 2–1 for location of the Model 6235 VIM connectors; see Figure 2–3 for location of the VIM connectors on a typical VIM baseboard.

9) **GENTLY but firmly**, press down on the VIM module opposite the connectors to fully seat the VIM module's connectors into the baseboard. If you meet with significant resistance, check the connector alignment.

> **NOTE:** Misalignment can cause bent pins or break connector housings, so **NEVER APPLY EXCESSIVE FORCE**.

10) After seating the connectors, secure the front of the VIM module to the VIM baseboard by screwing two short pan–head Phillips screws through the holes at the front of the VIM module into the threaded holes in the baseboard's panel brackets (indicated at positions (a) and (b), or (c) and (d) on Figure 2–3).

11) Turn the assembly over, such that the VIM module is on the work surface and the solder side of the VIM baseboard is facing up. Secure the baseboard to the nylon spacer on the VIM module, using the nylon screw removed earlier, through the rear mounting hole on the baseboard (indicated at position (e) or (f) on Figure 2–3).

12) Remove one top or bottom blank panel insert from the Option 102 front panel assembly provided (see figure below), depending on the VIM position in which the Model 6235 module was installed in the above steps. The remaining fixed plates and blank panel will be installed onto the baseboard front panel in the following steps.

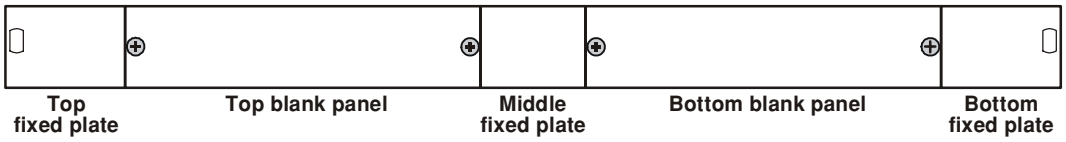


Figure 2–11: Option 102 Front Panel Assembly

2.3 Installing the Model 6235 on a VIM Baseboard (continued)

2.3.2 Installing Model 6235 with Option 102 (continued)

13) Install the Option 102 front panel assembly (which is in two pieces depending on which blank panel you removed earlier) onto the VIM baseboard front panel using the four long pan–head Phillips screws supplied (see figure below).

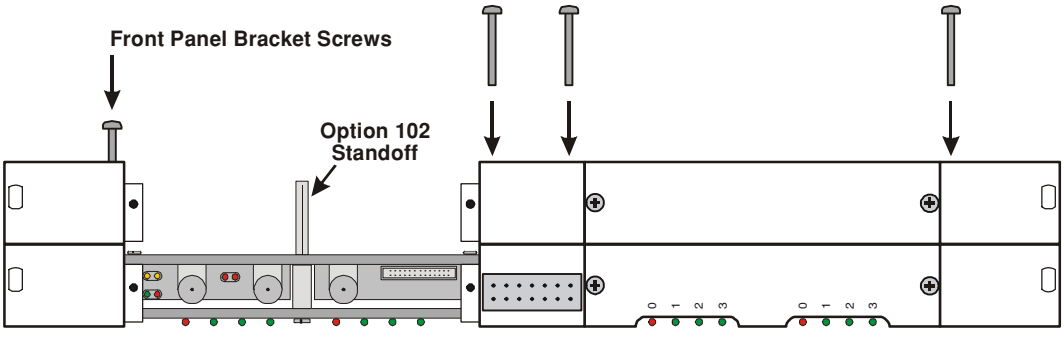


Figure 2–12: VIM Baseboard with Option 102 Front Panel Assembly
(Model 6235 illustrated in upper VIM position)

14) **CAREFULLY**, insert the two stacking connectors into the solder side of the Model 6235 PCB. Note that the stacking connector's longer leads must be inserted through holes on the solder side of the PCB (see figure below).

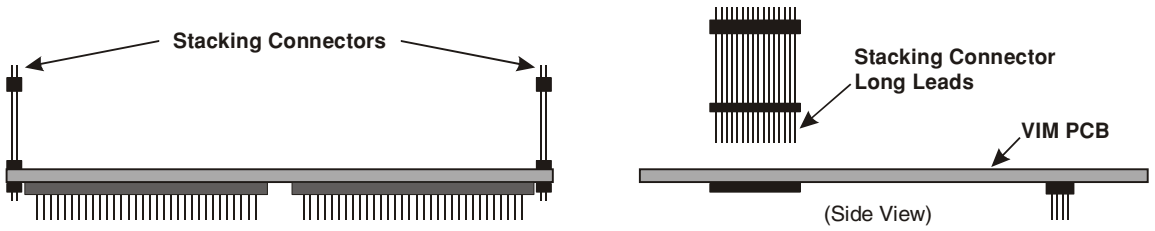


Figure 2–13: Option 102 Stacking Connectors on VIM Module

CAUTION

Be careful when installing the stacking connectors, as they are fragile and can easily be damaged.

2.3 Installing the Model 6235 on a VIM Baseboard (continued)

2.3.2 Installing Model 6235 with Option 102 (continued)

15) Align the Option 102 PCB connectors **J1** and **J2** with the two stacking connectors on the VIM module. **GENTLY but firmly**, press down on the areas of the board opposite the connectors to fully seat the board's connectors into the VIM module.

> **NOTE:** Misalignment can cause bent pins or break connector housings, so **NEVER APPLY EXCESSIVE FORCE**.

16) After seating the connectors, secure the front of the Option 102 PCB to the baseboard by screwing two short pan−head Phillips screws through the holes near the front of the PCB into the threaded holes in the Option 102 front panel assembly's panel brackets (see figure below).

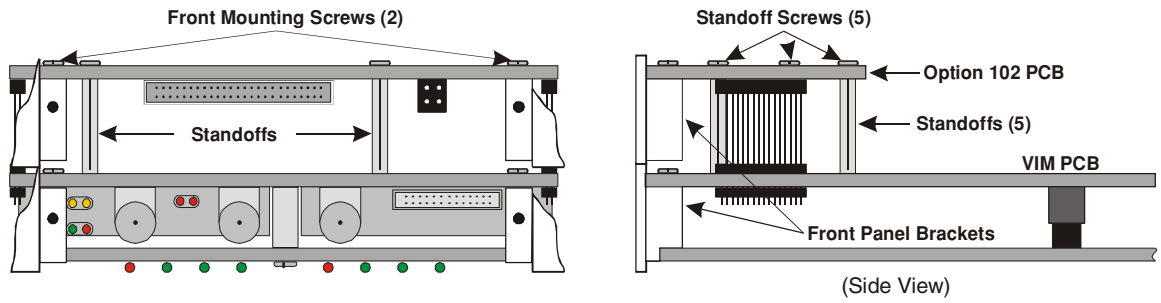


Figure 2−14: Option 102 PCB Mounted on VIM Module

17) Screw the five pan−head Phillips standoff screws removed from the PCB earlier through the solder side of the Option 102 PCB into the VIM module standoffs (see figure above).

18) Attach the Model 6235 and Option 102 front panels to the VIM baseboard, by screwing the countersunk Phillips panel screws through the holes in each VIM panel into the threaded holes in the baseboard's front panel brackets.

The Model 6235 installation is complete.

2.4 Front Panel Connections

The Model 6235 standard configuration provides a single front panel—a second front panel is provided with Option 102, mounted on an adjacent VMEbus board. Both of these front panels are illustrated in the figure at the right.

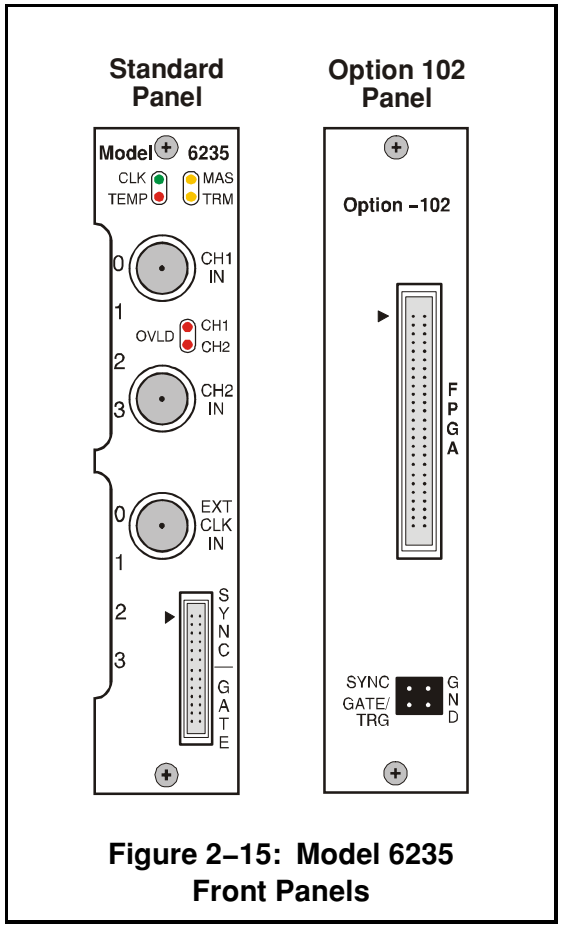


Figure 2–15: Model 6235 Front Panels

The standard panel includes three coaxial SMA input connectors labeled **CH1**, **CH2**, and **EXT CLK IN**, and a 26–pin Sync bus connector labeled **SYNC/GATE**. The optional second panel provides a 4–pin **SYNC/GATE/TRG** input connector, and a 50–pin **FPGA** I/O connector. These connectors are described in the following subsections.

2.4.1 Analog Input Connectors

The Model 6235's standard front panel has two threaded, coaxial SMA connectors for analog signal inputs (labeled **CH1 IN** and **CH2 IN**), one for each A/D input channel.

The analog input signal must be within the range of 1 V_{p-p} (4 dBm). Each input drives an RF transformer with approximately 50 Ω input impedance. This device amplifies the amplitude of the input signal by a factor of one.

2.4.2 External Clock Input Connector

The Model 6235's standard panel has a threaded, coaxial SMA connector, labeled **EXT CLK IN**, for input of an external clock. The external clock signal must be a sine signal of 01 to 10 dBm.

This input clock can be used as the reference signal to derive the sample clock signal for the A/D converters and DDRs. This input is enabled using bit D2, EXT CLK, in the Master Control Register (see Section 3.7.7).

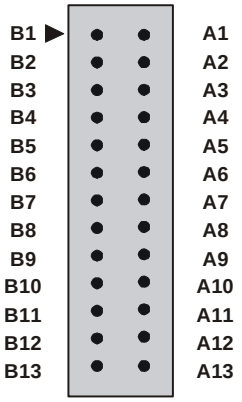
2.4 Front Panel Connections (continued)

2.4.3 Sync/Gate Connector

The 26−pin **SYNC/GATE** connector provides input/output for six low−voltage differential signal (LVDS) pairs: four gates, one sync, and one clock. When the Model 6235 is a sync bus Master, these pins output the sync bus signals to other 6235 slave units. When the 6235 is a sync bus Slave, these pins input the signals from a bus Master. Two TTL Gate/Sync inputs are also provided. The mating 26−pin connector is Pentek part # 353.02607 (ERNI # 214346). The following table the connector pin configuration.

Table 2−3: SYNC/GATE Connector Pins

Signal	Pin	Pin	Signal
TTL GATE	B1	A1	GND
TTL SYNC	B2	A2	GND
GATE D−	B3	A3	GATE D+
GND	B4	A4	GND
GATE C−	B5	A5	GATE C+
GND	B6	A6	GND
GATE B−	B7	A7	GATE B+
GND	B8	A8	GND
GATE A−	B9	A9	GATE A+
GND	B10	A10	GND
SYNC−	B11	A11	SYNC+
GND	B12	A12	GND
CLK−	B13	A13	CLK+

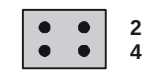


2.4.4 Sync/Gate Header (Option 102 only)

The optional 4−pin **SYNC/GATE/TRG** connector provides a second set of connections for TTL Sync/Gate inputs. These are wired to the same TTL SYNC and TTL GATE signals as pins B1 and B2 of the **SYNC/GATE** connec−tor, above. The mating 2−pin connector housing (use two for both signals) is Pentek part # 353.00201 (Berg # 65039−035) or equivalent. This connector housing uses discrete 0.025" square socket pins, Pentek part # 354.00104 (Berg # 48254−000). The following table the connector pin configuration.

Table 2−4: SYNC/GATE/TRG Header Pins

Signal	Pin	Pin	Signal
TTL SYNC	1	2	GND
TTL GATE/TRG	3	4	GND



2.4 Front Panel Connections (continued)

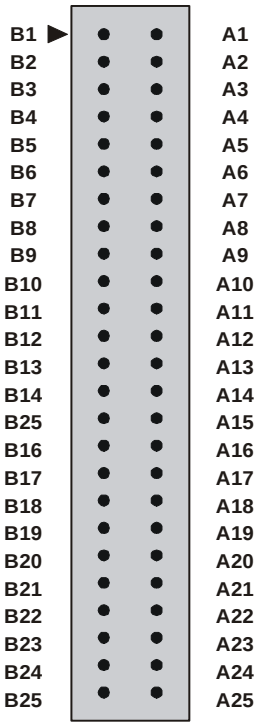
2.4.5 FPGA Connector (Option 102 only)

The optional 50−pin **FPGA** connector provides a 32−pin FPGA input/output data path. These pins correspond to bits D0 through D15 of the I/O Data Register (see Section 3.21). The mating connector is Pentek part # 353.05006 (ERNI part # 214347).

The following table shows the pinouts of this connector, and illustrates the connector pin configuration.

Table 2−5: FPGA Connector Pins

Description	Pin	Pin	Signal
GND	B1	A1	GND
FPGA I/O 31	B2	A2	FPGA I/O 30
FPGA I/O 29	B3	A3	FPGA I/O 28
GND	B4	A4	GND
FPGA I/O 27	B5	A5	FPGA I/O 26
FPGA I/O 25	B6	A6	FPGA I/O 24
GND	B7	A7	GND
FPGA I/O 23	B8	A8	FPGA I/O 22
FPGA I/O 21	B9	A9	FPGA I/O 20
GND	B10	A10	GND
FPGA I/O 19	B11	A11	FPGA I/O 18
FPGA I/O 17	B12	A12	FPGA I/O 16
N/C (Spare)	B13	A13	N/C (Spare)
GND	B14	A14	GND
FPGA I/O 15	B15	A15	FPGA I/O 14
FPGA I/O 13	B16	A16	FPGA I/O 12
GND	B17	A17	GND
FPGA I/O 11	B18	A18	FPGA I/O 10
FPGA I/O 9	B19	A19	FPGA I/O 8
GND	B20	A20	GND
FPGA I/O 7	B21	A21	FPGA I/O 6
FPGA I/O 5	B22	A22	FPGA I/O 4
GND	B23	A23	GND
FPGA I/O 3	B24	A24	FPGA I/O 2
FPGA I/O 1	B25	A25	FPGA I/O 0



2.5 Front Panel LEDs

The Model 6235 front panel has six LED indicators, as shown in Figure 2–15, page 29.

2.5.1 Clock LED

The green **CLK** LED is illuminated when a clock signal is detected. If this LED is not illuminated, then no clock signal has been detected and no data from this stream can be processed.

2.5.2 Over Temperature LED

There are several temperature/voltage sensors on the Model 6235 PCB. The sensor thresholds are set by a VIM baseboard processor (see Hardware Monitor Port Register, Section 3.6). When an over–temperature or over–voltage condition is indicated, the red **TEMP** LED is illuminated on the front panel. In addition, an over–temperature/voltage interrupt is available to any baseboard processor (see Table 3–18, page 55).

NOTE: You must set up the sensors' Hardware Monitor Port following power on of a Model 4290/4291 VIM baseboard (see Hardware Monitor Port Register, Section 3.6). ReadyFlow board support software for the Model 6235 is provided for this purpose.

2.5.3 Master LED

The yellow **MAS** LED is illuminated when this Model 6235 is the sync bus Master (MASTR bit D00 = 1, Master Control Register, Section 3.7.9). The bus Master generates all sync/gate/clock signals on the sync bus.

2.5.4 Terminate LED

When this Model 6235 is the last (or only) Slave unit on the sync bus, you must enable bus termination (TERM bit D01, Master Control Register, see Section 3.7.8). Enabling bus termination illuminates the yellow TRM LED.

2.5.5 Overload LEDs

There are two red overload LEDs, labeled **OVLD CH1** and **OVLD CH2**. Each LED is an indicator for the A/D overload detection function in each of the AD9432 A/D converters. When an overload indication is set by the AD9432, the associated OVLD LED is illuminated. In addition, an OVLD interrupt may be generated from each A/D overload indication to the VIM baseboard processors (see Section 3.15).

Chapter 3: Memory Maps and Register Descriptions

3.1 Overview

This chapter describes processor access to the Model 6235 from the VIM baseboard. Memory maps to VIM module resources are given from the baseboard processor's viewpoint, and details are provided describing the use of each resource.

3.2 Model 6235 Memory Map

The two tables below provide base addresses of the Model 6235 control and status registers for each type of Pentek VIM Baseboard. Use the applicable address from these tables as the VIM registers base address ('VIMReg_base') in the following sections.

For a Pentek Model 4290 through 4295 VIM baseboard, use the VIM registers base addresses in Table 3–1, below. These baseboards have four processor nodes, one for each VIM Interface, and each node processor uses the same VIM base address to access the associated VIM module.

Table 3–1: Base Addresses for Pentek VIM Baseboards

Pentek VIM Baseboard	VIM Registers Base Address (VIMReg_base)
Model 4290 or 4291	0x0032 0000
Model 4292 or 4293	0x0202 0000
Model 4294 or 4295	0x1D02 0000

For a Pentek Model 4205 VIM baseboard, use the VIM registers base addresses in Table 3–2, below. The Model 4205 has a single baseboard processor, which uses a separate base address for each VIM Interface (emulating four processors). In addition, on this baseboard the VIM module registers can be accessed from the VMEbus.

Table 3–2: Base Addresses for Model 4205 VIM Baseboards

VIM Site	VIM Registers Base Address (VIMReg_base)	
	MPC7455	VMEbus A32 Slave *
VIM A	0x4082 0000	A32VME_base + 0x00B2 0000
VIM B	0x4086 0000	A32VME_base + 0x00B6 0000
VIM C	0x408A 0000	A32VME_base + 0x00BA 0000
VIM D	0x408E 0000	A32VME_base + 0x00BE 0000

* Offsets relative to the base address 'A32VME_base' set on the Model 4205 baseboard (refer to the Model 4205 Operating Manual for these settings)

3.2 Model 6235 Memory Map (continued)

The following table provides a memory map for the Model 6235 32–bit control and status registers. All register addresses are expressed as offsets from the VIM base address for the applicable VIM baseboard—see Table 3–1 or Table 3–2 on the prior page for the VIM registers base address ('VIMReg_base') for your VIM baseboard. The sections following the table provide information about each register.

Table 3–3: Model 6235 Memory Map

Address Offset*	Register Description	Access	Information
VIMReg_base+0x0000	ID EEPROM Readout	R.O.	Appendix A
VIMReg_base+0x0004	Virtex Config (Proc. A or C only)	R/W	Section 3.3
VIMReg_base+0x0008	Virtex Config Data (Proc. A or C only)	W	Section 3.4
VIMReg_base+0x000C	Wait States (Proc. A or C only)	R/W	Section 3.5
VIMReg_base+0x0010	Hardware Monitor Port (Proc. A or C only)	R/W	Section 3.6
VIMReg_base+0x0014 – 0x001C	Not Used	–	–
VIMReg_base+0x0020	Master Control (Proc. A or C only)	R/W	Section 3.7
VIMReg_base+0x0024	Bypass Rate Divide	R/W	Section 3.8
VIMReg_base+0x0028	Sync Mask	R/W	Section 3.9
VIMReg_base+0x002C	DCM Control (Proc. A or C only)	R/W	Section 3.10
VIMReg_base+0x0030	Gate Control	R/W	Section 3.11
VIMReg_base+0x0034	Trigger Length	R/W	Section 3.12
VIMReg_base+0x0038	Channel Control	R/W	Section 3.13
VIMReg_base+0x003C	Sync/Gate Generator	R/W	Section 3.14
VIMReg_base+0x0040	Not Used	–	–
VIMReg_base+0x0044	Interrupt Mask	R/W	Section 3.15
VIMReg_base+0x0048	Interrupt Flag	R/Clr	Section 3.16
VIMReg_base+0x004C	Interrupt Status	R.O.	Section 3.17
VIMReg_base+0x0050	Semaphore	R/W	Section 3.18
VIMReg_base+0x0054 – 0x005C	Not Used	–	–
VIMReg_base+0x0060	I/O Direction (Option 102 only)	R/W	Section 3.19
VIMReg_base+0x0064	I/O Enable (Option 102 only)	R/W	Section 3.20
VIMReg_base+0x0068	I/O Data (Option 102 only)	R/W	Section 3.21
VIMReg_base+0x006C – 0x00FC	Not Used	–	–
VIMReg_base+0x0100 – 0x013F	Graychip Registers	R/W	Section 3.22

* VIMReg_base = see Table 3–1 or Table 3–2 on prior page

3.3 Virtex Config Register

The Virtex Config Register can be used to reconfigure/reprogram the Virtex FPGA. The bits in this register allow you to read and set the status of the FPGA configuration cycle, and to control uploading the configuration from a baseboard processor. This register is accessible only to Processor A on the VIM baseboard (or Processor C for a Model 6235 installed in the bottom VIM position on the baseboard).

Refer to Section 1.10, FPGA Configuration, for additional information about configuring the Virtex FPGA.

The following table shows the contents of the Virtex Config Register. The subsections following the table provide descriptions of the bits in this register.

Table 3–4: Virtex Config Register
R/W @ VIMReg_base+0x0004 (Proc A or C only)

	D31 – D06	D05	D04	D03*	D02*	D01	D00
Bit Name	Not used	WRITE	Not used	$\overline{\text{INIT}}$	DONE	PRGM	LD SRC
Function	Write zeros, Mask read	0 = NA 1 = Write	Write zeros, Mask read	0 = Configuring 1 = Completed	0 = Configuring 1 = Completed	0 = Disable 1 = Reprogram	0 = Onboard 1 = Upload

* These bits are Read Only
All bits default to the logic '0' state at power on and reset

3.3.1 WRITE Bit D05

This bit sets the write access of the Virtex Config Data Register, described in Section 3.4. When you set this bit to logic '1', you can write configuration data to the FPGA. To write data with the Virtex Config Data Register, you must also enable configuration upload (LD SRC bit D00 = 1, Section 3.3.5). Clear the bit to logic '0' (its default state) to disable configuration data from being accepted by the FPGA.

3.3.2 $\overline{\text{INIT}}$ Bit D03

This read–only bit indicates the status of the FPGA's '$\overline{\text{INIT}}$' pin. At initialization of a configuration cycle this bit goes to logic '0', then logic '1'. It will remain at logic '0' if an error in configuration data is detected. When read as logic '1', initialization is done.

3.3.3 DONE Bit D02

This read–only bit indicates the status of the FPGA's 'DONE' pin. When read as logic '0', the FPGA is in the configuration cycle. When read as logic '1', the FPGA has completed configuration.

3.3 Virtex Config Register (continued)

3.3.4 PRGM Bit D01

The FPGA begins a configuration reprogramming cycle after you transition this bit from logic '0', to logic '1', to logic '0', when in the Serial EEPROM or processor upload modes (see LD SRC, below). It has no effect in the serial download mode, as the Xilinx cable has control in that mode.

3.3.5 LD SRC Bit D00

This bit selects the source of the FPGA configuration data. When you clear this bit to logic '0' (its default state), the Virtex selects its configuration data from the on−board Serial EEPROM or from a serial download (depending on the setting of the configuration data source jumper on the 6235 module PCB, see Section 2.2). When you set this bit to logic '1', the FPGA is in processor upload mode, and you can upload the configuration using the Virtex Config Data Register, as described in Section 3.4.

3.4 Virtex Config Data Register

The Virtex Config Data Register writes configuration data to the Virtex FPGA. The write access is set by the WRITE bit in the Virtex Config Register (Section 3.3.1). When the LD SRC bit in the Virtex Config Register (Section 3.3.5) is set to '1', the FPGA configuration data can be uploaded, one byte at a time, using the Virtex Config Data Register. The Virtex Config Data Register is accessible only to Processor A (or Processor C for a Model 6235 installed in the bottom VIM position on the baseboard).

The following table shows the contents of this register.

Table 3−5: Virtex Config Data Register
W.O. @ VIMReg_base+0x0008 (Proc A or C only)

	D31 – D08	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	Not used	D7	D6	D5	D4	D3	D2	D1	D0
Function	Write zeros	Eight bits (one byte) of configuration data							
When reset or power−up, the state of this register is unknown.									

Refer to Section 1.10, FPGA Configuration, for additional information about configuring the Virtex FPGA.

3.5 Wait State Register

With the possibility of DBCLKs above 50 MHz, programmable wait states are provided to guarantee adequate access time. These wait states are user−programmable, using the Wait States Register. The Wait States Register is accessible only to Processor A on the VIM baseboard (or Processor C for a Model 6235 installed in the bottom VIM position on the baseboard).

The following table shows the contents of the Wait State Register. The paragraphs following the table provide descriptions of the fields in this register.

Table 3−6: Wait States Register
R/W @ VIMReg_base+0x000C (Proc A or C only)

	D31 – D08	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	Not used	GC DDR W3	GC DDR W2	GC DDR W1	GC DDR W0	CTL REG W3	CTL REG W2	CTL REG W1	CTL REG W0
Function	Write zeros, Mask read	Number of wait states for DDRs				Number of wait states for FPGA			
All bits default to the logic '1' state at power on and reset									

NOTE: At power up or reset, the wait states default to a maximum.

3.5.1 GC DDR Wn

Bits D07 to D04

The binary value in the four GC DDR bits determines the number of wait states for both GC1012B DDRs (wait state = [GC DDR] + 2 DBCLK cycles).

3.5.2 CTL REG Wn

Bits D03 to D00

The binary value in the four CTL REG bits sets the number of wait states for the FPGA (wait state = [CTL REG] + 2 DBCLK cycles). If configuring the FPGA using the Virtex Config Data Register (Section 3.4), the CTL REG wait state should be set to 0x1 or greater.

The wait states are equal to the greater of the VIM interface minimum write cycle time or the wait state selection in this register. For modules with a DBCLK of 50 MHz or less, a setting of GC DDR = 0 and CTL REG = 0 is adequate.

3.6 Hardware Monitor Port Register

The board's Voltage/Temperature Monitor, an Analog Devices ADM1024, provides constant monitoring of critical voltages and temperatures on the PCB. When an over–temperature or over–voltage condition is indicated, the red **TEMP** LED is illuminated on the front panel. In addition, an over–temperature/voltage interrupt is available to all VIM baseboard processors (see Table 3–18, Section 3.15).

There are several programmable temperature and voltage sensors for the ADM1024. The Hardware Monitor Port Register allows you to program these sensor thresholds. Only Processor A on the VIM baseboard can access this register (or Processor C for a Model 6235 installed in the bottom VIM position on the baseboard). The following table shows the contents of this register: one bit sets the read/write direction of the serial data and the other two provide the serial clock and data to set the thresholds.

Table 3–7: Hardware Monitor Port Register
R/W @ VIMReg_base+0x0010 (Proc A or C only)

	D31 – D03	D02	D01	D00
Bit Name	Not used	SER DIR	SER CLK	SER DAT
Function	Write with zeros, Mask when reading	0 = Read 1 = Write	Serial Clock	Serial Clock
All bits default to the logic '0' state at power on and reset				

NOTE: You must set up the port devices following power on of the VIM baseboard.

Routines for programming the sensor thresholds are provided in the ReadyFlow board support software for the Model 6235 (see Section 1.11). Alternately, you can program the thresholds directly from the Hardware Monitor Port Register, using internal ADM1024 registers (refer to the ADM1024 data sheet, Appendix B, for description of these registers). Each ADM1024 register has a separate bus read and write address, sent as serial data. The bus write address is **58** hex; the bus read address is **59** hex.

There are seven conditions monitored on the PCB, as listed in the following table:

Table 3–8: ADM1024 Registers

Monitored Condition	ADM1024 Register	Limits
Internal temperature	Internal Temp Value	0 to 85 degrees C
External temperature sensor 1 (under shield)	Ext. Temp1 Value	0 to 85 degrees C
External temperature sensor 2 (on PCB)	+2.5V Measured Value/Ext. Temp2	0 to 85 degrees C
+1.5 Volt supply	+Vccp1 Measured Value	+1.5 Volts, ±10%
+3.3 Volt supply	Vcc Measured Value	+3.3 Volts, ±10%
+5 Volt supply	+5V Value	+5 Volts, ±10%
+12 Volts Supply	+12V Measured Value	+12 Volts, ±10%

3.7 Master Control Register

The Master Control Register allows you to configure the Model 6235 as a Master or Slave on the Sync Bus, toggle the on−board sync bus termination, select the source of the clock, select the source and polarity of the sync, and enable the on−board oscillator. The Master Control Register is accessible only to Processor A on the VIM baseboard (or Processor C for a Model 6235 installed in the bottom VIM position on the baseboard).

The following table shows the contents of the Master Control Register. The subsections following the table provide descriptions of the bits.

Table 3−9: Master Control Register
R/W @ VIMReg_base+0x0020 (Proc A or C only)

	D31 – D16	D15	D14 – D10	D09	D08
Bit Name	Not used	RESET	Not used	SYNC SRC	SYNC POL
Function	Write with zeros, Mask when reading	0 = Run 1 = Reset	Write with zeros, Mask when reading	0 = Bypass Sync bus 1 = Sync bus	0 = Negative 1 = Positive

	D07	D06 – D05	D04	D03	D02	D01	D00
Bit Name	EXT SYNC	Not used	CLK SRC	OSC DSBL	EXT CLK	TERM	MASTR
Function	0 = Onboard 1 = Ext Sync	Write with zeros, Mask when reading	0 = Bypass Sync bus 1 = Sync bus	0 = Enable 1 = Disable	0 = Onboard 1 = Ext Clock	0 = Non-term 1 = Terminat'd	0 = Slave 1 = Master

All bits default to the logic '0' state at power on and reset

3.7.1 RESET Bit D15

This bit issues a reset to the entire Model 6235 module. When the bit is set to logic '1', the module is in reset. When the bit is cleared to logic '0' (its default state), the module is in a normal run state.



This RESET signal should be held for at least four times the front panel clock speed (4 x Front Panel Clock).

3.7.2 SYNC SRC Bit D09

This bit selects the source of the sync signal for the GC1012B's S−sync, A−sync, and G−sync inputs. When this bit is cleared to logic '0' (its default state), the sync bus is bypassed and the sync is selected by EXT SYNC bit D07, Section 3.7.4. When the bit is set to logic '1', the LVDS sync bus (SYNC/GATE connector, Section 2.4.3) is the source of the sync.

3.7 Master Control Register (continued)

3.7.3 SYNC POL Bit D08

This bit selects the polarity of the external sync input for resetting the GC1012B DDRs. When the bit is cleared to logic '0' (its default state), a negative sync input resets the GC1012Bs. When this bit is set to logic '1', a positive sync input resets the GC1012Bs.

3.7.4 EXT SYNC Bit D07

When this Model 6235 is the sync bus Master (MASTR bit D00 = 1) or when the LVDS sync input is bypassed (SYNC SRC bit D09 = 0), this bit selects the sync signal for the GC1012B DDRs. When this bit is cleared to logic '0' (its default state), the Sync/Gate Generator Register, Section 3.14, is the source of the sync. When the bit is set to logic '1', the external TTL sync input (SYNC/GATE connectors, Section 2.4.3 or 2.4.4) is the source.

3.7.5 CLK SRC Bit D04

This bit selects the source of the module's clock. When the bit is cleared to logic '0' (its default state), the sync bus is bypassed and the clock is selected by EXT CLK, Section 3.7.7. When this bit is set to logic '1', the LVDS sync bus (SYNC/GATE connector, Section 2.4.3) is the source of the clock.

3.7.6 OSC DSBL Bit D03

This bit enables or disables the output from the on–board 100–MHz oscillator. When the bit is cleared to logic '0' (its default state), the 100–MHz oscillator is enabled. When bit is set to logic '1', the oscillator is disabled.

3.7.7 EXT CLK Bit D02

When the module is a sync bus Master (MASTR bit D00 = 1) or when the LVDS sync bus clock is bypassed (CLK SRC bit D04 = 0), this bit selects the module's clock signal. When this bit is cleared to logic '0' (its default state), the on–board oscillator is selected (OSC DSBL bit D03 above, must be cleared to logic '0' to enable the oscillator). When the bit is set to logic '1', the external clock input is used (EXT CLK IN connector, Section 2.4.2).

3.7.8 TERM Bit D01

This bit enables termination of the sync bus by a Slave unit, or a Master unit if it is the only unit on the bus. When the bit is cleared to logic '0' (its default state), the sync bus is not terminated. When the bit is set to logic '1', the bus is terminated. The sync bus must be terminated when this unit is the last (or only) Slave on the sync bus, or if it is a Master and the only unit on the bus.

3.7 Master Control Register (continued)

3.7.9 MASTR Bit D00

This bit selects between Master or Slave on the sync bus for this Model 6235. Wh1en the bit is cleared to logic '0' (its default state), the module is a Slave. When bit is set to logic '1', the sync bus on this module is Master. When set as a sync bus Master, this Model 6235 is the source of the sync, clock, and gate signals output to the LVDS sync bus. You must select these sources using control bits EXT SYNC (bit D07), EXT CLK (bit D02), and EXT GATE (Section 3.11.9), and if needed, generate the sync and/or gate signals using the Sync/Gate Generator Register (Section 3.14).

3.8 Bypass Rate Divide Register

This register sets the decimation rate of data samples written to the processor BIFO when the associated channel is in DDR Bypass mode (selected by DAT MODE, Channel Control Register, Section 3.13.14). Each processor on the baseboard has its own copy of this register, associated with that processor channel.

The following table shows the contents of this register. The paragraph following the table provides description of these bits.

Table 3–10: Bypass Rate Divide Register
R/W @ VIMReg_base+0x0024

	D31 – D12				D11	D10	D09	D08
Bit Name	Not used				B11	B10	B09	B08
Function	Write with zeros, Mask when reading				4 MSBs of 12–bit rate divider 'N–1'			
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	B7	B6	B5	B4	B3	B2	B1	B0
Function	8 LSBs of 12–bit rate divider 'N–1'							
All bits default to the logic '0' state at power on and reset								

The rate divider is a 12–bit binary value, with bit D11 the MSB. To take every Nth sample, where N is any integer value between 1 and 4096, set this register to N–1. The default value is '0x000', which is dividing by 1.



If you select 'Channel Packing' DDR Bypass mode (Section 4.2.3), the bypass rate dividers of both processor channels (A and B, or C and D) MUST be set at the same rate and synchronized for proper operation.

3.9 Sync Mask Register

The Sync Mask Register enables the output from the module's sync signal (selected by SYNC SRC, Master Control Register, Section 3.7.2) to any of the GC1012B's three sync inputs, S–Sync, A–Sync, or G–Sync. Each processor on the VIM baseboard has its own version of this register for the GC1012B associated with that processor.

The following table shows the contents of this register. The paragraph following the table provides description of these bits.

Table 3–11: Sync Mask Register
R/W @ VIMReg_base+0x0028

	D31 – D03	D02	D01	D00
Bit Name	Not used	G–Sync	A–Sync	S–Sync
Function	Write with zeros, Mask when reading	0 = Disable sync 1 = Enable sync		
All bits default to the logic '0' state at power on and reset				

Each bit of the register corresponds to one of the three GC1012B sync inputs. When one of the bits is set to logic '1', the sync signal is enabled to that GC1012B input. When a bit is cleared to logic '0', the sync is not enabled for that GC1012B input.

3.10 DCM Control Register

The DCM Control Register controls the Digital Clock Manager (DCM) on the FPGA. The DCM Control Register is accessible only to Processor A on the VIM baseboard (or Processor C for a Model 6235 installed in the bottom VIM position on the baseboard).

The following table shows the contents of this register. Two of these bits are read−only status bits. The subsections following the table provide descriptions of the bits.

Table 3–12: DCM Control Register
R/W @ VIMReg_base+0x002C (Proc A or C only)

	D31 – D04	D03*	D02*	D01	D00
Bit Name	Not used	DCM CLK LOSS	LOCKD	DCM RST	CLK SEL
Function	Write with zeros, Mask when reading	0 = Valid clock 1 = No clock	0 = Not locked 1 = Locked	0 = Run 1 = Reset	0 = Input clock 1 = DCM

* These bits are Read Only
All bits default to the logic '0' state at power on and reset

This register is for future use only. Operation up to 105 MHz is possible without the use of the DCM. Bit 0 (CLK SEL) should remain at the default of logic '0'.

3.10.1 DCM CLK LOSS Bit D03

This read−only bit indicates the status of the DCM clock source. When read as logic '0', the DCM has a valid input clock source. When read as logic '1', the DCM has lost its input clock source.

3.10.2 LOCKD Bit D02

This read−only bit indicates the locked status of the DCM. When read as logic '0', the DCM is not locked. When read as logic '1', the DCM is locked.

3.10.3 DCM RST Bit D01

This bit issues a reset to the DCM. When the bit is set to logic '1', the DCM is in reset. When the bit is cleared to logic '0' (its default state), the DCM is in a normal run state. The DCM must be reset before operation or if lock is lost.

3.10.4 CLK SEL Bit D00

This bit selects the clock source for the FPGA. When the bit is cleared to logic '0' (its default state), the input clock is the clock source and the DCM is bypassed. When this bit is set to logic '1', the DCM is the clock source (use only above 24 MHz).

3.11 Gate Control Register

The Gate Control Register contains several fields to select the characteristics and source of the VIM BIFO write gates for the controlling processor. Each processor on the VIM baseboard has its own version of this register. However, only Processor A (or Processor C for a Model 6235 installed in the bottom VIM position on the baseboard) can set the gate polarity (GATE POL, bite D08). Each processor may use any one of the gates available (Gate A, B, C, or D) for enabling BIFO writes associated with that processor.

When the Model 6235 is the sync bus Master (MASTR = 1, Master Control Register, Section 3.7.9), the module generates four gates for the LVDS sync bus: Gates A and C from Processor A (or Processor C for a Model 6235 installed in the bottom VIM position on the baseboard), and Gates B and D from Processor B (or Processor D). When the sync bus is bypassed (GATE SRC bit D04 = 0), the Model 6235 generates only two gates, Gate A and B (or C and D), for use on the module. Refer to Chapter 5, Timing and Synchronization, for additional information about these gate and sync signals.

The following table shows the contents of the Gate Control Register. The subsections following the table provide descriptions of the bits in this register.

Table 3–13: Gate Control Register
R/W @ VIMReg_base+0x0030

	D31 – D13	D12	D11	D10	D09	D08
Bit Name	Not used	INT EDGE D	INT EDGE C	INT EDGE B	INT EDGE A	GATE POL *
Function	Write with zeros, Mask when reading	0 = Start 1 = End	0 = Start 1 = End	0 = Start 1 = End	0 = Start 1 = End	0 = Negative 1 = Positive

	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	GATE SEL1	GATE SEL0	GATE DISBL	GATE SRC	TRIG CLEAR	HOLD MODE	GATE/TRIG	EXT GATE
Function	00 = Gate A 01 = Gate B 10 = Gate C 11 = Gate D		0 = Enable 1 = Disable	0 = Bypass Sync bus 1 = Sync bus	0 = None 1 = Force Gate inactive	0 = None 1 = Hold	0 = Gate 1 = Trigger	0 = Register 1 = TTL Input

* Proc A or C only
All bits default to the logic '0' state at power on and reset

3.11.1 INT EDGE x

Bits D12 to D09

Each of these four bits selects whether the start or the end of the respective gate (Gate A for INT EDGE A, etc.) creates an interrupt to the controlling processor (each gate interrupt may be independently enabled for this processor using the Interrupt Mask Register, Section 3.15). When the bit is cleared to logic '0' (its default state), the start of the gate creates an interrupt. When the bit is set to logic '1', the end of the gate creates the interrupt.

3.11 Gate Control Register (continued)

3.11.2 GATE POL Bit D08

This bit selects the polarity of the external TTL gate/trigger input. This bit is only available to Processors A or C (Processor A bit controls polarity for both A and B; Processor C bit controls polarity for both C and D). When the bit is cleared to logic '0' (its default state), BIFO writes are enabled by a negative input in Gate mode, or triggered on a negative−going edge in Trigger mode. When the bit is set to logic '1', BIFO writes are enabled by a positive input in Gate mode, or triggered on a positive−going edge in Trigger mode.

3.11.3 GATE SELn Bits D07 to D06

These two bits select the gate for the BIFO writes associated with this processor on the VIM baseboard. The settings for these two bits are:

```
00 (default) - Gate A
01           - Gate B
10           - Gate C
11           - Gate D
```

3.11.4 GATE DISBL Bit D05

This bit enables or disables the selected gate (GATE SEL, Section 3.11.3) from controlling BIFO writes for this processor. When this bit is cleared to logic '0' (its default state), the gate is enabled to control BIFO writes. When this bit is set to logic '1', the gate is disabled. When the gate is disabled, BIFO writes are defaulted to enabled; however, it does not disable the generation of interrupts from the gate signal.

3.11.5 GATE SRC Bit D04

This bit selects the source of the BIFO gate (GATE SEL, Section 3.11.3). When this bit is cleared to logic '0' (its default state), the LVDS sync bus is bypassed and the source of the BIFO gate is selected using EXT GATE, Section 3.11.9. When the bit is set to logic '1', the LVDS sync bus (SYNC/GATE connector, Section 2.4.3) is the source of the gate.

3.11.6 TRIG CLEAR Bit D03

This bit forces the selected gate to the inactive state in Trigger mode (GATE/TRIG bit D01 = 1, Section 3.11.8). When this bit is cleared to logic '0' (its default state), there is no effect on the gate. When the bit is set to logic '1', the gate is forced to inactive (BIFO writes disabled), regardless of the trigger length specified (Trigger Length Register, Section 3.12).

3.11 Gate Control Register (continued)

3.11.7 HOLD MODE Bit D02

This bit enables a gate Hold after the trigger is received in Trigger mode (GATE/TRIG bit D01 = 1, Section 3.11.8). When the bit is cleared to logic '0' (its default state), the selected gate is active (BIFO writes enabled) for the specified trigger length after the trigger (specified using the Trigger Length Register, Section 3.12), and then goes inactive (BIFO writes disabled). When the bit is set to logic '1', Hold is enabled and the gate remains active (BIFO writes enabled) after the trigger is received, until this bit is cleared.

3.11.8 GATE/TRIG Bit D01

When the source of the selected BIFO gate is either an on−board register or the external TTL gate input (EXT GATE, Section 3.11.9), this bit selects between Gate or Trigger mode for enabling BIFO writes. When the bit is cleared to logic '0' (its default state), Gate mode is selected. When the bit is set to logic '1', Trigger mode is selected, and you must set the trigger length using the Trigger Length Register, Section 3.12, or enable trigger Hold (HOLD MODE, Section 3.11.7).

3.11.9 EXT GATE Bit D00

When the Model 6235 is the sync bus Master (MASTR bit D00 = 1, Master Control Register, Section 3.7.9), or when the LVDS sync bus is bypassed for gate signals (GATE SRC bit D04 = 0, Section 3.11.5), this bit selects the source of the designated BIFO gate. When this bit is cleared to logic '0' (its default state), the Sync/Gate Generator Register, Section 3.14, is the source of the BIFO gate. When the bit is set to logic '1', the external TTL gate input (SYNC/GATE connectors, Section 2.4.3 or 2.4.4) is the source of the gate.

See Chapter 5, Timing and Synchronization, for additional information about the use and programming of gate and sync signals.

3.12 Trigger Length Register

When the Model 6235 is set for Trigger mode (GATE/TRIG = 1, Gate Control Register, Section 3.11.8), this register sets the length that the gate is active (BIFO writes enabled) after receipt of the trigger. Each processor on the VIM baseboard has its own version of this register, for the gate selected by that processor.

The following table shows the contents of the Trigger Length Register. The paragraph following the table provides a description of the bits in this register.

Table 3–14: Trigger Length Register
R/W @ VIMReg_base+0x0034

	D31 – D14		D13	D12	D11	D10	D09	D08
Bit Name	Not used		D13	D12	D11	D10	D9	D8
Function	Write with zeros, Mask when reading		6 MSBs of 14–bit Trigger Length					
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Function	8 LSBs of 14–bit Trigger Length							
All bits default to the logic '0' state at power on and reset								

The trigger length is a 14–bit binary value, with bit D13 the MSB. This value specifies the length of the gate after the trigger as the number of BIFO writes of the processor that generates the selected gate, up to 16,383.



If you set the Trigger Length Register and select this gate source for multiple processor channels (GATE SEL, Gate Control Register, Section 3.11.3), you must set the same data routing modes for those channels (DAT MODE, Channel Control Register, Section 3.13.14)

3.13 Channel Control Register

The Channel Control Register selects the Data Routing mode of each processor channel, enables the sync signal to reset the DDR Bypass mode rate dividers, and resets the processor channel. Control bits for the FFT processor are available in this register only with Option 401 or 404 (see Chapter 6 for description of this option). This register is accessible to each processor on the VIM baseboard; however, certain bits are available to Processor A only (or Processor C for a Model 6235 installed in the bottom VIM position on the baseboard). The following table shows the contents of the register, and the subsections following the table provide descriptions of the bits in the register.

Table 3–15: Channel Control Register
R/W @ VIMReg_base+0x0038

	D31 – D16							
Bit Name	Not used							
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D09**	**D08**
Bit Name	RESET	FFT MARK EN [1, 2]	FFT ENBL [1, 2]	AVG [1, 2]	PWR [1, 2]	SCALE [1, 2]	HANN [1, 2]	CONT [1, 2]
Function	0 = Run 1 = Reset	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = One-Shot 1 = Contin.
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	FFT CE SRC [1, 2]	FFT DAT SRC [1, 2]	FFT RST [1]	DIV RST EN	CHAN SRC [1]	DAT MODE2	DAT MODE1	DAT MODE0
Function	0 = VIM A 1 = VIM B	0 = A/D 1 = DDR	0 = Run 1 = Reset	0 = Disable 1 = Enable	0 = Normal 1 = Other	Data Routing mode – see Section 3.13.14		

1 – Option 401/404 only
2 – Proc A or C only
All bits default to the logic '0' state at power on and reset

3.13.1 RESET Bit D15

This bit issues a reset to the associated processor channel (including resets to the A/D, DDR, and FPGA. (This does not reset the Master Control Register, Section 3.7). When the bit is set to logic '1', the channel is in reset. When the bit is cleared to logic '0' (its default state), the channel is in normal run state.

3.13.2 FFT MARK EN (Option 401/404, Processor A or C only) Bit D14

This bit enables the FFT processor to provide a marker word at the start of the FFT data, replacing the first FFT data result from both channels. When the bit is set to logic '1', a marker word (**0xA5A5A5A5**) is placed in the first word of the FFT result. When the bit is cleared to logic '0' (its default state), the first word of the FFT result is the first result from the FFT processor.

This feature is not available if AVG (bit D12, Section 3.13.4) is Enabled.

3.13 Channel Control Register (continued)

3.13.3 FFT ENBL (Option 401/404, Processor A or C only) Bit D13

This bit enables the FFT processor to run for both channels. This bit must be set to logic '1' before starting FFT calculations. When not utilizing the FFT processor, this bit should be cleared to logic '0' to avoid wasted power consumption, since the FFT processor consumes a significant amount of power. After enabling the FFT processor with this bit, it should be reset with the FFT RST bit D05, Section 3.13.11, before beginning FFT calculation.

3.13.4 AVG (Option 401/404, Processor A or C only) Bit D12

This bit enables the FFT processor to average two 50% overlapping FFT results. This results in a 3dB gain in dynamic range and is the only way to take advantage of the two overlapping outputs of the FFT processor, since the VIM interface cannot accept both of them simultaneously. The averaging function is only available in conjunction with the power conversion function. This bit affects both channel inputs.

When cleared to logic '0' (its default state), the data stream from the FFT processor to the VIM interface will be one FFT data point out per input data cycle period.

When set to logic '1,' the data stream from the FFT processor to the VIM interface will be one FFT data point out per input data cycle period, however, each point will be the average of two 50% overlapping FFTs. For example, the 4096−point FFT processor will calculate the FFT for data sample t0 through t4095, while also calculating the FFT for data samples t2048 through t6143. The results of the two FFTs are delayed in time to line up and are then summed together.

3.13.5 PWR (Option 401/404, Processor A or C only) Bit D11

This bit enables a sum−of−squares power calculation of the FFT data. When cleared to logic '0' (its default state), the output data format is complex data. When set to logic '1,' the output data format is the result of a sum−of−squares power calculation of the complex data (see Section 4.2.6 for description of these formats). This bit affects both channels.

3.13.6 SCALE (Option 401/404, Processor A or C only) Bit D10

This bit enables an option divide by two in the first butterfly stage of the FFT. Because of the fixed−point nature of the FFT processor, it is possible in some conditions when the Hanning window is disabled to overflow the 16 bits. If this occurs, an indication of it can create an interrupt and can be monitored in the Interrupt Flag Register (Section 3.16). Under most conditions, this bit should be cleared to logic '0' (its default state). If the FFT processor is overflowing, set this bit to a logic '1.' This bit affects both channels.

3.13 **Channel Control Register** (continued)

3.13.7 **HANN** (Option 401/404, Processor A or C only) Bit D09

This bit enables the Hanning Window Function on both channels. When the bit is cleared to logic '0,' the Hanning Window function is disabled and data is routed directly to the FFT processor. When set to logic '1,' data is multiplied by a Hanning window function before being fed to the FFT processor.

3.13.8 **CONT** (Option 401/404, Processor A or C only) Bit D08

This bit selects either continuous or one−shot mode of FFT operation on both channels. When the bit is cleared to logic '0' (its default state), one−shot mode is selected. The FFT processor will start at the start of the GATE (falling edge) and calculate one complete FFT result and then stop and wait for another gate start. This mode is useful when you want to trigger an FFT calculation by an external event. In this case you would select the triggered gate mode (see Gate Control Register section). When using the triggered gate with the FFT, set the Trigger Length Register to 4 less than the length of the FFT (`0xFFC` for the 4096−point FFT).

When this bit is set to logic '1,' continuous mode is selected. The FFT processor will begin calculating FFTs at the start of the GATE (falling edge) and continue to output FFTs one after another continuously and indefinitely until the GATE signal ends. Note that when the GATE signal ends, data flow to the VIM interface immediately stops, and therefore it is likely that a portion of the last FFT will be lost. Before the start of a new GATE, the FFT processor should be reset with FFT RST bit 05, Section 3.13.11.

3.13.9 **FFT CE SRC** (Option 401/404, Processor A or C only) Bit D07

This bit selects the clock enable and gate source for the FFT processor. When cleared to logic '0' (its default state), the FFT processor uses channel #1's (VIM A or C interface) clock enable and gate. When set to logic '1,' the FFT processor uses channel #2's (VIM B or D interface) clock enable and gate. The clock enable for the FFT processor will be the DDR WS pulse for DDR data, or the Bypass Rate Divider pulse for A/D data.

Since there is only one FFT processor to be time−shared by the two data channels, the clock enable and gate that governs it must come from one or the other VIM interface. For this reason, when FFT data is desired from both channels, they must follow several rules:

- Both channels must be either A/D data or DDR data.
- For A/D data, the Bypass Rate Divider must be the same for both channels.
- For DDR data, the outputs of the two DDRs must be synchronized and at the same decimation rate.

3.13 Channel Control Register (continued)

3.13.9 FFT CE SRC (continued)

- Both VIM interfaces must be using the same gate.

However, if for example FFT data is required for only the second VIM interface, then the FFT processor would be set to be controlled by the second VIM interface's clock enable (DDR WS pulse for DDR data, Bypass Rate Divider for A/D data) and gate, while the first VIM interface could operate independently on non–FFT data.

3.13.10 FFT DAT SRC (Option 401/404, Processor A or C only) Bit D06

This bit selects the data source for both channels of the FFT processor. When the bit is cleared to logic '0' (its default state), the data source is A/D data. When set to logic '1,' the data source is DDR data.

3.13.11 FFT RST (Option 401/404 only) Bit D05

This bit resets the FFT processor. This should be done once after enabling the FFT the first time and every time before the beginning of a GATE signal when in continuous mode. When set to logic '1,' the FFT is held in reset. When cleared to logic '0' (its default state), the FFT is in normal run state. This bit is available in this register for both VIM interface processors (A and B, or C and D). They are OR'ed together to the FFT processor.

3.13.12 DIV RST EN Bit D04

This bit enables the module's Sync signal to reset the DDR Bypass mode rate dividers, to allow synchronization of all dividers. When this bit is cleared to logic '0' (its default state), this reset is not enabled. When bit is set to logic '1', the Sync is enabled to reset the bypass mode decimate dividers.

3.13.13 CHAN SRC (Option 401/404 only) Bit D03

This bit selects which input channel's data is routed to this VIM interface, depending on the processor that makes the selection. Note that this selection also determines the format of the data output in DDR Bypass, Channel Packing mode, see Section 3.13.14.

VIM Interface	CHAN SRC	Data Routed to VIM Interface
VIM A (or C) (Processor A or C)	0 (default)	Channel #1 A/D, DDR, or FFT data
	1	Channel #2 A/D, DDR, or FFT data
VIM B (or D) (Processor B or D)	0 (default)	Channel #2 A/D, DDR, or FFT data
	1	Channel #1 A/D, DDR, or FFT data

3.13 Channel Control Register (continued)

3.13.14 DAT MODEn

Bits D02 to D00

These three bits select the Data Routing mode to the FPGA. There are several different modes of data formatting (these are described in Section 4.2). The settings for these three bits are:

```
000 (default)- Disabled
001          - DDR Bypass, 12-bit data, Unpacked
010          - DDR Bypass, 12-bit data, Time Packed
011          - DDR Bypass, 12-bit data, Channel Packed
100 or 101   - DDR Mode, 16-bit data, Unpacked I/Q
110          - DDR Mode, 16-bit data, Packed I/Q
111          - FFT Mode (Option 401/404 only, see Chapter 6)
```

NOTE: For the DDR Bypass, Channel Packed mode (011), with Option 401 or 404 the format for data output depends on the setting of CHAN SRC, Bit D03, Section 3.13.13.

VIM Interface	CHAN SRC	Data Output Format (for mode 011)
VIM A (or C) (Processor A or C)	0 (default)	D31:16 = A/D 1 D15:0 = A/D 2
	1	D31:16 = A/D 2 D15:0 = A/D 1
VIM B (or D) (Processor B or D)	0 (default)	D31:16 = A/D 2 D15:0 = A/D 1
	1	D31:16 = A/D 1 D15:0 = A/D 2



When you select any DDR routing mode, ensure that the GC1012Bs are configured accordingly using the GC1012B registers (see Section 3.22, Graychip Registers).

The Channel Control Registers do not set up the GC1012B registers.

3.14 Sync/Gate Generator Register

The Sync/Gate Generator Register is used on a Model 6235 that is configured as a sync bus Master (MASTR = 1, Master Control Register, Section 3.7.9), or on a 6235 that is not connected to an external LVDS sync bus. Each processor on the baseboard has its own copy of this register, associated with that processor channel.

The following table shows the contents of the Sync/Gate Generator Register. The sub–sections following the table provide descriptions of the two bits that are used to gener–ate gate and sync signals for the associated processor channel.

Table 3–16: Sync/Gate Generator Register
R/W @ VIMReg_base+0x003C

	D31 – D02	D01	D00
Bit Name	Not used	$\overline{\text{FIFO GATE}}$	$\overline{\text{SYNC}}$
Function	Write with zeros, Mask when reading	0 = Enable 1 = Disable	0 = Reset 1 = Release
All bits default to the logic '1' state at power on and reset			

3.14.1 $\overline{\text{FIFO GATE}}$ Bit D01

If the gate source is set to the on–board register (EXT GATE = 0, Gate Con–trol Register, Section 3.11.9), this bit creates the gate signal for the associated processor BIFO, and for output to the sync bus for a sync bus Master.

For a BIFO gate, when the bit is cleared to logic '0', BIFO writes are enabled. When the bit is set to logic '1' (its default state), BIFO writes are disabled.

When the board is a sync bus Master, the gate created by Processor A (or C) is output to both GATE A and GATE C pins of the SYNC/GATE connector, Section 2.4.3, and the gate created by Processor B (or D) is output to both GATE B and GATE D pins of the SYNC/GATE connector.

3.14.2 $\overline{\text{SYNC}}$ Bit D00

If the sync source is set to the on–board register (EXT SYNC = 0, Master Control Register, Section 3.7.4), this bit creates the sync signal (SYNC) for all GC1012B DDRs on the board, and for output to the sync bus (SYNC/GATE connector, Section 2.4.3) for a sync bus Master. The $\overline{\text{SYNC}}$ bits for both pro–cessors are OR'ed together to create the SYNC signal for the board. When the bit is cleared to logic '0', the GC1012B is in reset. When the bit is set to logic '1' (its default state), the GC1012B is released for normal operation.

Refer to Chapter 5, Timing and Synchronization, for additional information about the use and programming of gate and sync signals.

3.15 Interrupt Mask Register

The Interrupt Mask Register contains one enable bit for each interrupt condition defined for the controlling processor. Each processor on the VIM baseboard has its own version of this register.

The following table shows which bit in this register is associated with each interrupt condition. Table 3–18, on the next page, provides description of the interrupt condition associated with each of these bits.

Table 3–17: Interrupt Mask Register
R/W @ VIMReg_base+0x0044

	D31 – D13	D12	D11	D10	D09	D08
Bit Name	Not used	FFT OVFLW *	TEMP	VALID CLK	CLK LOSS	GATE D
Function	Write with zeros, Mask when reading	0 = Disable Interrupt 1 = Enable Interrupt				

	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	GATE C	GATE B	GATE A	SYNC	Not used	DDR OVFLW	OVLD CH2	OVLD CH1
Function	0 = Disable Interrupt 1 = Enable Interrupt							

* Option 401/404 only
All bits default to the logic '0' state at power on and reset

Each bit of the Interrupt Mask Register enables or disables the generation of the interrupt to that processor. Setting the bit associated with a given interrupt to the logic '1' state enables the generation of an interrupt to the processor when that interrupt condition occurs. When a bit is cleared to logic '0', the processor will not be interrupted by the associated interrupt condition.

The following two sections, Interrupt Flag Register, Section 3.16, and Status Register, Section 3.17, contain associated functions for using these processor interrupts.

3.15 Interrupt Mask Register (continued)

Table 3–18: Interrupt Register Bits

Bit Name	Bit Position	Interrupt Function
FFT OVFLW	D12	This bit is associated with an overflow interrupt from the FFT processor. This bit is available only with Option 401 or 404.
TEMP	D11	This bit is associated with a temperature/voltage limit interrupt from the ADM1024. (To determine the sensor causing the interrupt, use the Hardware Monitor Port Register, Section 3.6.)
VALID CLK	D10	This bit is associated with a Valid Clock indication interrupt. The interrupt status will go to logic '1' 16 clock cycles after detection of a clock. It will also indicate that 16 clock cycles have occurred since the beginning of a BIFO reset. This can be used as an indication that the BIFO reset is complete, since a BIFO reset requires several clock cycles to complete. The bit will remain high during normal operation, thus it should be masked (disabled) after it is no longer useful to prevent undesired interrupts.
CLK LOSS	D09	This bit is associated with a Clock Loss interrupt.
GATE D GATE C GATE B GATE A	D08 D07 D06 D05	Each of these bits is associated with a Gate interrupt. The interrupt occurs at the start or end of the respective gate signal, depending on the setting of INT EDGE x in the Gate Control Register, Section 3.11.
SYNC	D04	This bit is associated with a Sync interrupt. The interrupt occurs at the start of the sync pulse.
DDR OVFLW	D02	This bit is associated with an overflow interrupt from any of the GC1012B DDRs.
OVLD CH2 OVLD CH1	D01 D00	Each of these bits is associated with an analog input overload interrupt from one of the A/D converters (A/D2 or A/D1).

Note: These bit assignments and definitions apply to Interrupt Mask Register, Section 3.15, Interrupt Flag Register, Section 3.16, and Interrupt Status Register, Section 3.17

3.16 Interrupt Flag Register

The Interrupt Flag Register has one read/clear bit associated with each interrupt condition for the VIM processor (the same bit associations as the Interrupt Mask Register, Section 3.15). Each processor on the VIM baseboard has its own version of this register.

The following table shows which bit in this register is associated with each interrupt condition. Table 3–18, on the prior page, provides description of the interrupt condition associated with each of these bits.

Table 3–19: Interrupt Flag Register
R/Clr @ VIMReg_base+0x0048

	D31 – D13	D12	D11	D10	D09	D08
Bit Name	Not used	FFT OVFLW *	TEMP	VALID CLK	CLK LOSS	GATE D
Function	Write with zeros, Mask when reading	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 0 = Enabled to latch 1 = Clear latch				

	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	GATE C	GATE B	GATE A	SYNC	Not Used	DDR OVFLW	OVLD CH2	OVLD CH1
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 0 = Enabled to latch 1 = Clear latch							

* Option 401/404 only

IMPORTANT! When reset, including power–up, the state of this register is unknown. You should clear this register before using it, by writing '1's into all bits.

Each bit of this register latches an interrupt occurrence. A logic '1' in any bit in this register indicates that an interrupt has occurred. Note that when any bit in the Interrupt Status Register (Section 3.17) changes to logic '1', the corresponding bit in this register will also be set to logic '1'. However, when a bit in the Interrupt Status Register changes from logic '1' to logic '0', the corresponding latched bit in this register does not clear, but remains at the logic '1' state.

Since these bits latch in response to an interrupt, to detect subsequent interrupts, you must clear the bits in this register. To clear any bit in this register that is set to the logic '1' state, you must write to that bit twice, first with a '1' to clear the bit, then with a '0' to re–enable the bit for latching.

3.17 Interrupt Status Register

The Interrupt Status Register has one read–only bit associated with each interrupt condition for the VIM processor (the same bit associations as the Interrupt Mask Register, Section 3.15). Each baseboard processor has its own version of this register.

The following table shows which bit in this register is associated with each interrupt condition, and Table 3–18, on page 55, provides description of the interrupt condition associated with each of these bits.

Table 3–20: Interrupt Status Register
R.O. @ VIMReg_base+0x004C

	D31 – D13	D12	D11	D10	D09	D08
Bit Name	Not used	FFT OVFLW *	TEMP	VALID CLK	CLK LOSS	GATE D
Function	Mask when reading	0 = None 1 = Overflow	0 = None 1 = Overtemp	0 = None 1 = Clock OK	0 = None 1 = No Clock	0 = None 1 = Gate

	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	GATE C	GATE B	GATE A	SYNC	Not Used	DDR OVFLW	OVLD CH2	OVLD CH1
Function	0 = None 1 = Gate	0 = None 1 = Gate	0 = None 1 = Gate	0 = None 1 = Sync	Mask read	0 = None 1 = Overflow	0 = None 1 = Overload	0 = None 1 = Overload

* Option 401/404 only
When reset or power–up, the state of this register is unknown.

Each bit in this register changes whenever the associated interrupt indication changes. A bit changes to the logic '1' state whenever that interrupt occurs, and clears to logic '0' state when that interrupt clears (whereas the associated bit in the Interrupt Flag Register, Section 3.16, remains latched at logic '1' until it is cleared by that register's clear action).

If the corresponding bit in the Interrupt Mask Register (Section 3.15) has been set to the logic '1' state, then an Interrupt Status Register bit transition from logic '0' to logic '1' will also generate an interrupt to the processor on the VIM baseboard. If you do not want an interrupt to occur and have set the corresponding interrupt mask bit to '0', you may poll this Status Register bit to determine if such an event has occurred.

3.18 Semaphore Register

The Semaphore Register contains communications bits that may be written by one processor on the VIM baseboard and read by both processors. Each processor may write only four of the bits in this register, but either processor may read all bits. These bits allow coordination between programs running in the baseboard processors.

The following table shows which bits are associated with each processor for writing.

Table 3–21: Semaphore Register
R/W @ VIMReg_base+0x0050

	D31 – D08							
Bit Name	Not used							
Function	Write with zeros, Mask when reading							
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	B3	B2	B1	B0	A3	A2	A1	A0
Function	Bits written by Processor B (or D)				Bits written by Processor A (or C)			
All bits default to the logic '0' state at power on and reset								

3.19 I/O Direction Register (Option 102 only)

The I/O Direction Register determines the input/output direction of each corresponding bit of the FPGA I/O Data Register described in Section 3.21. Each data bit can be individually programmed for input or output by this register. This register is accessible to either processor on the VIM baseboard.

NOTE: This register is available only with Option 102.

The following table shows which bit of this register is associated with each FPGA I/O data bit, and the paragraphs following the table provide descriptions of these bits.

Table 3–22: I/O Direction Register
R/W @ VIMReg_base+0x0060

	D31 – D16							
Bit Name	Not used							
Function	Write with zeros, Mask when reading							
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D09**	**D08**
Bit Name	DIR15/ DIR31	DIR14/ DIR30	DIR13/ DIR29	DIR12/ DIR28	DIR11/ DIR27	DIR10/ DIR26	DIR9/ DIR25	DIR8/ DIR24
Function	0 = Input bit 1 = Output bit							
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	DIR7/ DIR23	DIR6/ DIR22	DIR5/ DIR21	DIR4/ DIR20	DIR3/ DIR19	DIR2/ DIR18	DIR1/ DIR17	DIR0/ DIR16
Function	0 = Input bit 1 = Output bit							
DIR[15:0] for Processor A or C DIR[31:16] for Processor B or D All bits default to the logic '0' state at power on and reset								

These bits are assigned to the front panel FPGA connector pins as follows, depending on whether the Model 6235 is installed in the top or bottom VIM position on the baseboard:

- DIR15:0 for Processor A (Processor C if installed in the lower VIM position)
- DIR31:16 for Processor B (Processor D if installed in the lower VIM position)

Refer to the connector diagram in Table 2–5, Section 2.4.5, for the pin assignments of each bit.

When a bit is cleared to logic '0' (its default state), the corresponding data bit can be input at the Model 6235 front panel FPGA connector (Section 2.4.5). When the bit is set to logic '1', the corresponding data bit is set for output.

3.20 I/O Enable Register (Option 102 only)

The I/O Enable Register enables connection of the I/O bits of the I/O Data Register (Section 3.21) to the Model 6235 front panel FPGA connector (see Section 2.4.5). This register is accessible to either processor on the VIM baseboard.

NOTE: This register is available only with Option 102.

The following table shows the contents of the register. The I/O EN bit enables connection of I/O bits 15:0 for processor A/C, or I/O bits 31:16 for processor B/D.

Table 3–23: I/O Enable Register
R/W @ VIMReg_base+0x0064

	D31 – D01	D00
Bit Name	Not used	I/O EN
Function	Write with zeros, Mask when reading	0 = Disable 1 = Enable
All bits default to the logic '0' state at power on and reset		

3.21 I/O Data Register (Option 102 only)

The I/O Data register allows you to read or write data from the Virtex FPGA to the Model 6235 front panel FPGA connector (see Section 2.4.5). The direction (read or write) for each bit is controlled by the corresponding bit of the I/O Direction Register, Section 3.19. The data bits are enabled or disabled for connection to the front panel by the I/O Enable Register, Section 3.20. This register is accessible to either processor on the VIM baseboard.

NOTE: This register is available only with Option 102.

The following table shows which bit in this register is associated with each FPGA data bit, and the paragraphs following the table provide descriptions of these bits.

Table 3–24: I/O Data Register
R/W @ VIMReg_base+0x0068

	D31 – D16							
Bit Name	Not used							
Function	Write with zeros, Mask when reading							
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D09**	**D08**
Bit Name	FPGA I/O 15/31	FPGA I/O 14/30	FPGA I/O 13/29	FPGA I/O 12/28	FPGA I/O 11/27	FPGA I/O 10/26	FPGA I/O 9/25	FPGA I/O 8/24
Function	Each bit can be used as data Input or Output, depending on corresponding bit of I/O Direction Register, Section 3.19							
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	FPGA I/O 7/23	FPGA I/O 6/22	FPGA I/O 5/21	FPGA I/O 4/20	FPGA I/O 3/19	FPGA I/O 2/18	FPGA I/O 1/17	FPGA I/O 0/16
Function	Each bit can be used as data Input or Output, depending on corresponding bit of I/O Direction Register, Section 3.19							
FPGA[15:0] for Processor A or C FPGA[31:16] for Processor B or D When reset or power–up, the state of this register is unknown.								

These bits are assigned to the front panel FPGA connector pins as follows, depending on whether the Model 6235 is installed in the top or bottom VIM position on the base–board:

- FPGA I/O 15:0 for Processor A (Processor C if installed in the lower VIM position)
- FPGA I/O 31:16 for Processor B (Processor D if installed in the lower VIM position)

Refer to the connector diagram in Table 2–5, Section 2.4.5, for the pin assignments of each bit.

3.22 Graychip Registers

The Graychip Registers allow you to read or write data from/to each Graychip GC1012B on the Model 6235. Each baseboard processor has its own version of these registers, for the GC1012B chip associated with that processor.

There are 16 registers in the GC1012B. The address of each register is listed below.

Frequency Byte 0 Register – VIMReg_base+0x0100
Frequency Byte 1 Register – VIMReg_base+0x0104
Frequency Byte 2 Register – VIMReg_base+0x0108
Frequency Byte 3 Register – VIMReg_base+0x010C
Sync Mode Register – VIMReg_base+0x0110
Filter Mode Register – VIMReg_base+0x0114
Gain Control Register – VIMReg_base+0x0118
Gain Exponent Register – VIMReg_base+0x011C
Output Mode Register – VIMReg_base+0x0120
Output Status Register – VIMReg_base+0x0124
One Shot Address – VIMReg_base+0x0128
Checksum Register – VIMReg_base+0x012C
I–Output Byte 0 Register – VIMReg_base+0x0130
I–Output Byte 1 Register – VIMReg_base+0x0134
Q–Output Byte 0 Register – VIMReg_base+0x0138
Q–Output Byte 1 Register – VIMReg_base+0x013C

The following table shows the bit layout of each register. You can read or write one byte at a time to each register.

Table 3–25: Graychip Registers
R/W @ Address VIMReg_base+0x0100 – 013F

	D31 – D08	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	Not used	D7	D6	D5	D4	D3	D2	D1	D0
Function	Write zeros, Mask read	Eight bits of data to/from GC1012B							
When reset or power–up, the state of these registers is unknown.									

GC1012B library functions are provided in the ReadyFlow board support software package for the Model 6235 (Pentek part #801.62350). Refer also to the Graychip GC1012B data sheet, Appendix D, for more information on this device.

Chapter 4: Data Formatting

4.1 Overview

This chapter provides descriptions of the data routing and formatting of the Model 6235's A/D conversion.

4.2 Data Routing and Formats

The Model 6235 has two RF analog input channels. Each input channel includes an AD6645 A/D converter that provides data to one of the board's two Graychip GC1012B DDRs. Data from both the A/Ds and the DDRs is provided to the FPGA for formatting before being sent to the VIM baseboard BIFOs.

Use the Channel Control Register (Section 3.13) to set the FPGA's Data Routing mode, and to reset the FPGA's data formatter state machine. Five modes of output data formatting are provided on the standard Model 6235, plus one for the FFT output with Option 401 or 404. These are described in Sections 4.2.1 to 4.2.6.

DDR Bypass Routing Modes — The FPGA takes the A/D data directly, bypassing the GC1012B DDRs. This raw output data (real data) is written to the baseboard VIM BIFOs at a programmed decimation rate, and may be unpacked, packed by time of arrival, or packed by channel.

DDR Routing Modes — Each GC1012B accepts one 12-bit parallel input from its associated A/D converter. The FPGA is configured to accept two channels of parallel inputs from the two GC1012B DDRs. The DDR data is written to the VIM BIFO when the BIFO gate is enabled. The data formatter state machine is reset when the gate is disabled, but will complete writing the current DDR data to the VIM BIFO before stopping.



1) When you select a DDR Data Routing mode, ensure that the GC1012Bs are configured accordingly using the GC1012B registers (see Section 3.22, Graychip Registers, and the Graychip GC1012B Data Sheet, Appendix D). The Channel Control Registers do not set up the GC1012B registers.

2) The DDR mode descriptions assume that the GC1012B is set up for COMPLEX output (the default output), providing both I and Q values. If the GC1012B is configured for REAL output, only one sample is output.

FFT Mode (Option 401 or 404 only) — The FPGA's FFT processor computes FFT outputs and writes them to the VIM BIFOs. See Chapter 6 for description of the FFT Operation.

4.2 Data Routing and Formats (continued)

4.2.1 DDR Bypass Mode, Unpacked (DAT MODE=001)

This mode takes the raw 12−bit A/D data (real data) directly from the two A/Ds, bypassing the GC1012Bs. The output is written to the baseboard VIM BIFO at a programmed decimation rate f_s/N, where N is 1 to 4096, only when the gate is enabled.

Data is left justified in the 12 most significant bits out of 16 in each of the 16−bit halves of the 32−bit BIFO data word. Each baseboard BIFO receives data from its associated input channel; that is, VIM A (or C) BIFO from A/D 1, VIM B (or D) BIFO from A/D 2. Identical data is placed in both halves of the 32−bit word. Data is in the following format:

Table 4−1: Output Data Format − DDR Bypass Mode, Unpacked

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Value	d	d	d	d	d	d	d	d	d	d	d	d	0	0	0	0
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Value	d	d	d	d	d	d	d	d	d	d	d	d	0	0	0	0

d = raw A/D data bit (same value in both halves of word)

4.2.2 DDR Bypass Mode, Time Packed (DAT MODE=010)

This mode takes the 12−bit A/D data directly from the two A/Ds, bypassing the GC1012Bs. The output is written to the VIM BIFO at a programmed decimation rate $f_s/2N$, where N is 1 to 4096, only when the gate is enabled.

Data is packed with data word data(t) in the upper half of the 32 bits, and word data(t−1) in the lower half of the 32 bits. Each baseboard BIFO receives data from its associated input channel; that is, VIM A (or C) BIFO from A/D 1, VIM B (or D) BIFO from A/D 2. Each sample is left justified in the 12 most significant bits out of 16 in each of the 16−bit halves of the 32−bit BIFO data word. Data is in the following format:

Table 4−2: Output Data Format − DDR Bypass Mode, Time Packed

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Value	d_t	d_t	d_t	d_t	d_t	d_t	d_t	d_t	d_t	d_t	d_t	d_t	0	0	0	0
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Value	d_{t-1}	d_{t-1}	d_{t-1}	d_{t-1}	d_{t-1}	d_{t-1}	d_{t-1}	d_{t-1}	d_{t-1}	d_{t-1}	d_{t-1}	d_{t-1}	0	0	0	0

d_t = raw data from A/D at time (t), d_{t-1} = raw data from A/D at time (t−1)

4.2 Data Routing and Formats (continued)

4.2.3 DDR Bypass Mode, Channel Packed (DAT MODE=011)

This mode takes the raw 12–bit A/D data (real data) directly from the two A/Ds, bypassing the GC1012Bs. The output is written to the VIM BIFO at a decimation rate f_s/N, where N is 1 to 4096, only when the gate is enabled.



You MUST set the bypass decimation rate dividers (Section 3.8) of both processor channels (A and B, or C and D) at the same rate and synchronized for this mode to function properly!

Data is packed with data from A/D 1 in the upper half of the 32 bits, and data from A/D 2 in the lower half of the 32 bits. Baseboard VIM A and B BIFOs (or C and D BIFOs) receive the same data from the two A/Ds (see **NOTE** above). Each sample is left justified in the 12 most significant bits out of 16 in each of the 16–bit halves of the 32–bit BIFO data word.

Data is in the following format:

Table 4–3: Output Data Format – DDR Bypass Mode, Channel Packed

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Value	d_1	d_1	d_1	d_1	d_1	d_1	d_1	d_1	d_1	d_1	d_1	d_1	0	0	0	0
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Value	d_2	d_2	d_2	d_2	d_2	d_2	d_2	d_2	d_2	d_2	d_2	d_2	0	0	0	0

d_1 = raw data from A/D 1, d_2 = raw data from A/D 2 (see **NOTE** below)

NOTE: With Option 401 or 404, the output data format depends on the setting of CHAN SRC, Bit D03, Section 3.13.13.

VIM Interface	CHAN SRC	Output Data Format
VIM A (or C)	0	D31:16 = A/D 1 D15:0 = A/D 2
	1	D31:16 = A/D 2 D15:0 = A/D 1
VIM B (or D)	0	D31:16 = A/D 2 D15:0 = A/D 1
	1	D31:16 = A/D 1 D15:0 = A/D 2

4.2 Data Routing and Formats (continued)

4.2.4 DDR Mode, Unpacked I/Q (DAT MODE=100 or 101)

This mode expects data from each GC1012B to be 32−bit I/Q pairs. VIM BIFO writes are controlled by the gate. The data is output in two consecutive 32−bit words written per I/Q pair. Data is in the following format:

Table 4−4: Output Data Format − DDR Mode, Unpacked I/Q

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Value	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Value	0	0	0	0	0	0	0	0	0	0	T	0	0	0	0	0
D = Data bit; T = I/Q tag (I = 0, Q = 1)																

NOTE: On the standard Model 6235, the Q value is the first 32−bit word of each I/Q pair, followed by the I value. With Option 401 or 404, the I value is the first word of each I/Q pair, followed by the Q value.

NOTE: This description assumes that the GC1012B is set up for COMPLEX output (the default output), providing both I and Q values. If the GC1012B is configured for REAL output, only one sample is output and the FPGA marks the data as an I sample.

4.2.5 DDR Mode, Packed I/Q (DAT MODE=110)

This mode expects data from each GC1012B to be 32−bit I/Q pairs. BIFO writes are controlled by the gate. The data format is a 16−bit I and a 16−bit Q data value packed into a 32−bit word. Data is in the following format:

Table 4−5: Output Data Format − DDR Mode, Packed I/Q

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Value	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Value	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q
I = I sample data bit; Q = Q sample data bit																

NOTE: This description assumes that the GC1012B is set up for COMPLEX output (the default output), providing both I and Q values. If the GC1012B is configured for REAL output, only one sample is output and the lower half of the 32−bit output word is cleared.

4.2 Data Routing and Formats (continued)

4.2.6 FFT Mode (DAT MODE=111) (Option 401/404 only)

The FFT processor allows a sum−of−squares power calculation of the FFT result. The FFT output is controlled using Bit D11, PWR, in the Channel Control Register (Section 3.13.5). The two settings of this bit are Power mode and Complex mode (default), and each provides a different output format to the VIM interface.

Complex Output Mode

When in Complex output mode, the data format is the 16−bit real component in bits 31:16, followed by the imaginary component in bits 15:0.

Table 4−6: Output Data Format − FFT Complex Mode

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Value	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Value	Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0

Power Output Mode

When in Power output mode, the data format is a 32−bit unsigned value that is the result of a sum−of−squares power calculation of the 16−bit complex value.

Table 4−7: Output Data Format − FFT Power Mode

Bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Value	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Value	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

See Chapter 6 for description of the FFT Operation.

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Chapter 5: Timing and Synchronization

5.1 Overview

This chapter provides descriptions of the timing and synchronization of the module processing. The Model 6235 uses two gates, one sync, and one clock (see Figure 5–1 on the next page for a logic diagram of these signals). Both gates, the clock, and the sync signals can go out or in on the front panel LVDS Sync Bus.

5.2 Gates

Gates are used to enable writes to the VIM baseboard BIFOs. Any processor channel may use any one of four gate sources as its gate (Gate Control Register, Section 3.11). Gates may also be disabled on a channel–by–channel basis, in which case BIFO writes are always enabled. All gate features are programmable on a (processor) channel–by–channel basis, except external gate polarity, which is selectable from Processor A (or Processor C) only and is global. Gate transitions from high to low or low to high can create interrupts on any processor.

Each gate can be driven directly from the front panel LVDS Sync Bus GATE A/B signal (Section 2.4.3) if the Model 6235 is a sync bus Slave, or from a gate signal generated on the board. When the Model 6235 is a sync bus Master, the generated gates are output to the LVDS Sync Bus. Note that four gates are output to the LVDS Sync/Gate connector from a Master 6236, GATE A from Processor A (or C) is output to both GATE A and C pins and GATE B from Processor B (or D) is output to both GATE B and D pins.

Each on–board generated gate may be created from a register write by each processor (Section 3.14) or selected from an external TTL gate source (Sections 2.4.3 and 2.4.4). The polarity of the external gate source is programmable. The external gate and the register write may be programmed to act as a trigger. In this case, the gate is generated after a transition on the external gate source or register write, and the resulting gate continues either indefinitely or for a programmed number of BIFO writes up to 16,383. At any time the triggered gate may be asynchronously disabled by a register write.

5.3 Sync

Register bits allow routing of the sync source to the GC1012B's S–sync, A–sync, and G–sync inputs (Sync Mask Register, Section 3.9). This sync signal can be driven directly from the front panel LVDS Sync Bus SYNC signal (Section 2.4.3) if the Model 6235 is a sync bus Slave, or from a sync signal generated on the board.

The on–board sync can be selected from the external TTL SYNC input (Section 2.4.3) or created by a register write (Section 3.14). When the Model 6235 is a sync bus Master, the on–board sync is output to the LVDS Sync Bus.

5.4 Clock

The clock for all board functions can be driven either from the front panel LVDS Sync Bus CLK signal (Section 2.4.3), if the Model 6235 is a sync bus Slave, or from a clock signal generated on the board.

The on−board clock can be generated using the 100−MHz oscillator (Master Control Register, Section 3.7) or can be selected from the external clock input (Section 2.4.2). When the Model 6235 is a sync bus Master, the on−board clock is output to the LVDS Sync Bus.

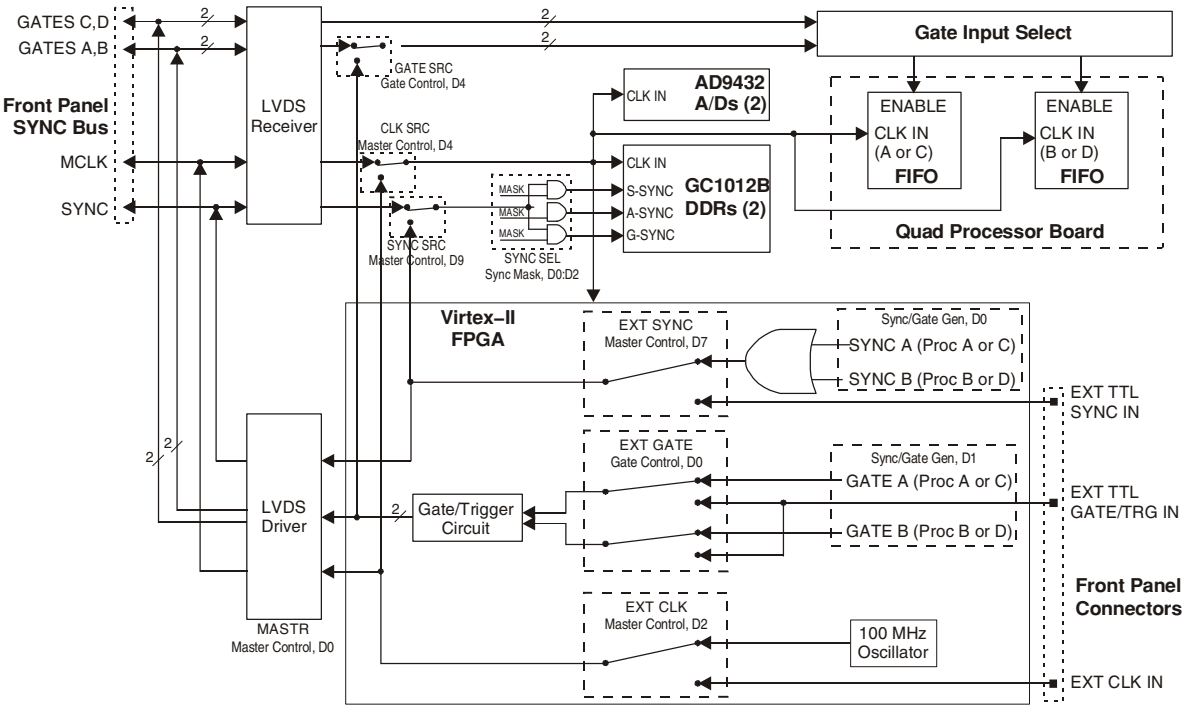
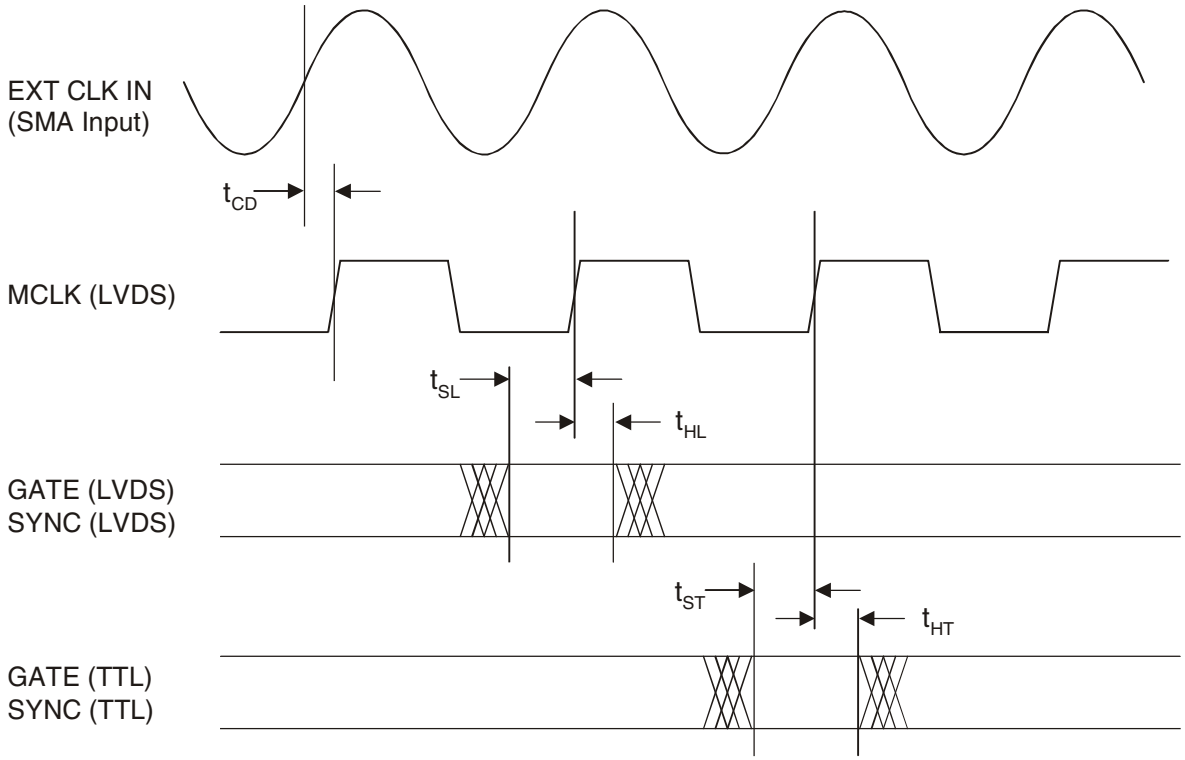


Figure 5−1: Model 6235 − Gate/Sync/Clock Logic

5.5 Timing Diagram

The following figure shows the timing signal relationships for the Model 6235.



		MIN	MAX	
t_{CD}	EXT CLK IN to MCLK Delay	2.0	4.0	nsec
t_{SL}	LVDS GATE/TRIG Setup Time	3.2	–	nsec
t_{HL}	LVDS GATE/TRIG Hold Time	–	5.8	nsec
t_{ST}	TTL GATE/TRIG Setup Time	2.3	–	nsec
t_{HT}	TTL GATE/TRIG Hold Time	–	5.8	nsec

Figure 5–2: Model 6236 – Timing Signal Relationships

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Chapter 6: Option 401 or 404 FFT Operation

6.1 Overview

Options 401 and 404 incorporate an extremely powerful FFT (Fast Fourier Transform) processor into the FPGA in the Model 6235. Option 401 is a 1024−point FFT, while Option 404 is a 4096−point FFT.

Utilizing a unique pipelined and highly distributed radix−4 FFT algorithm, which fully leverages the abundance of dedicated multiplier elements in the Xilinx Virtex™ II XC2V3000 FPGA, this FFT processor can calculate either a 1024−point or 4096−point FFT at a rate of four points per clock cycle, or a calculation speed that exceeds real time (of the applicable data rate) by a factor of four. In addition to this, it also can also apply the Hanning Window Function to the data input stream, calculate a sum−of−squares power calculation on the data output stream, and also average overlapping FFT results.

The FFT processor is capable of 126 MHz clock rates in the fastest FPGA speed grade, however, the maximum clock rate of the A/D converters, limitations on the maximum VIM interface clock rate, and power consumption issues, limit the maximum clock rate for the FFT to 100 MHz. Due to the four times real time calculation rate of the FFT pro−cessor, the FFT processor may be time−shared by the two data channels of the Model 6235 and still allow for FFT calculations at two times real time each. In this manner, the FFT processor produces two output data streams per channel. The two FFT output data streams have a 50% overlap. Since passing this much data to the VIM data inter−face would require a VIM interface data rate that is twice its limit, the two overlapping FFTs are delayed to line up in time, and then averaged.

The following figure shows the Option 401 or 404 signal flow logic diagram.

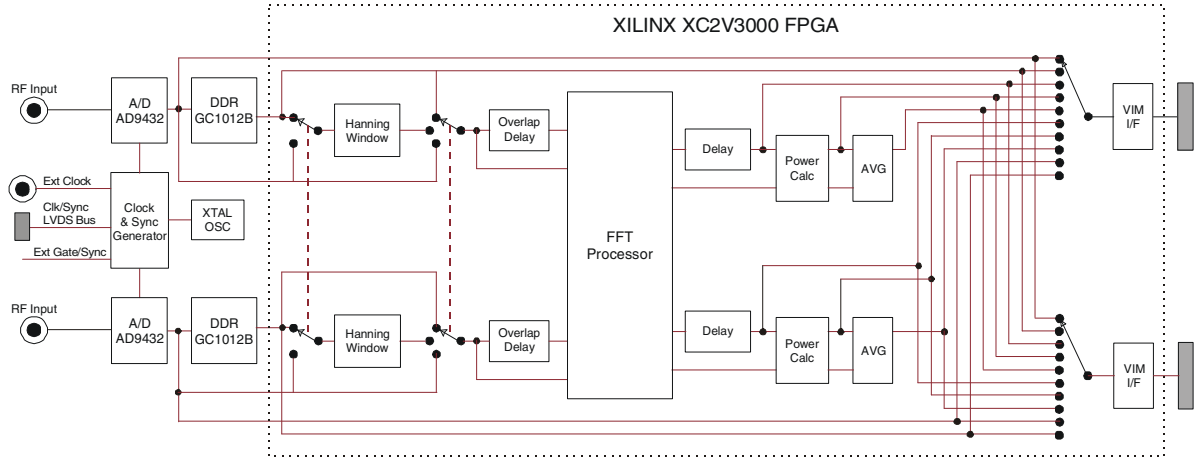


Figure 6−1: Model 6235 Option 401/404 Block Diagram

6.2 FFT Processor Performance (@ 100 MHz clock rate)

Data Input: Four simultaneous complex data inputs (16–bit I and 16–bit Q).

Input Data Sources: Two of four input streams are connected to either Channel #1 A/D data or Channel #1 DDR data. One is time delayed to create 50% overlap.

Two of four input streams are connected to either Channel #2 A/D data or Channel #2 DDR data. One is time delayed to create 50% overlap.

Data Input Rate: 100 MHz sample rate on each of four inputs.

Calculation Time Per FFT:

4096 points:	10.24 µsec
1024 points:	2.56 µsec

FFT Data Output: Four simultaneous complex data outputs (16–bit I and 16–bit Q) or 32–bit unsigned power.

Output Configuration: Two output data streams for each of the two data input sources with a 50% overlap. When averaging mode is disabled, one of these data streams is routed to the VIM interface and the overlapping data is not utilized. When averaging mode is enabled, a delay and summation is employed to average the two overlapping FFT results.

Output Data Rate: Two simultaneous VIM interface output data streams at the input data sample rate (40.96 µsec for a 4096–point FFT at 100 MHz input sample rate).

6.3 FFT Calculation Accuracy

The FFT algorithm utilized is 16–bit signed fixed point. Therefore, the largest number that can be represented is 32,767. This allows for a dynamic range of 90 dB. An additional 3 dB of dynamic range can be realized when averaging the power calculations of overlapping FFTs is enabled. Due to the nature of the Hanning Window function, when it is enabled there is a loss of 6 dB in dynamic range. Likewise, when calculating the FFT of the A/D input instead of the DDR output, since the data is not complex, there is a loss of 6 dB of dynamic range. This is because the FFT processor input is complex and for raw A/D data, the 'Q' term is zero.

A table of the achievable dynamic range is shown below.

Table 6–1: Dynamic Range

Data Source	Hanning	Power Calculation	Averaging	Output Dynamic Range
DDR Data	Disabled	Disabled	N/A	90dB
DDR Data	Disabled	Enabled	Disabled	90dB
DDR Data	Disabled	Enabled	Enabled	93dB
DDR Data	Enabled	Disabled	N/A	84dB
DDR Data	Enabled	Enabled	Disabled	84dB
DDR Data	Enabled	Enabled	Enabled	87dB
A/D Data	Disabled	Disabled	N/A	84dB
A/D Data	Disabled	Enabled	Disabled	84dB
A/D Data	Disabled	Enabled	Enabled	87dB
A/D Data	Enabled	Disabled	N/A	78dB
A/D Data	Enabled	Enabled	Disabled	78dB
A/D Data	Enabled	Enabled	Enabled	81dB

6.4 FFT Operation

Use the Channel Control Register (Section 3.13) to set the FFT processor operating modes and to reset the FFT processor before beginning FFT calculations.

The FFT processor may be configured to operate in either one−shot mode, or continuous mode. This is controlled using bit D08, CONT, in the Channel Control Register (Section 3.13.8). In either case, the FFT will begin processing at the beginning (falling edge) of the GATE signal.

- In the one−shot mode, one complete FFT will be computed and passed to the VIM interface, then the processor stops and waits for the beginning of the next gate. This is ideal for use with the Model 6235's triggered gate mode, which allows the triggering of the FFT calculation with an external event.

- In the continuous mode, FFTs are calculated for data starting at the beginning at the GATE signal, and will continue calculating consecutive FFTs indefinitely as long as the GATE signal is low. The FFT processing will keep up with input data up to the full maximum clock rate without loss of data.

Since the FFT processor is time−shared by the two data channels, when FFT data is desired from both data channels, the following rules must be observed:

1) Both channels must be either A/D data or DDR data.

2) If the data source is A/D data, the rate divider is common.

3) If the data source is DDR data, the outputs of the two DDRs must be synchronized and at the same decimation rate.

4) Both VIM interfaces must be using the same gate.

When one VIM interface has selected a data source other than the FFT, they may work completely independent as with a standard Model 6235. The output choices for each VIM interface has however been enhanced over the standard 6235. It is possible to direct data from either A/D channel or DDR channel to either, or both VIM interfaces. This allows, for instance, the possibility of routing FFT data for channel #1 A/D or DDR data stream to one VIM interface, while simultaneously routing the raw channel #1 A/D or DDR data stream to the other VIM interface.

See Section 4.2.6 for the FFT output data formats.

Appendix A: Configuration EEPROM Format

A.1 Introduction

All VIM Modules contain an Identification (ID) EEPROM with a checksum stored in the last location. When booted, each VIM baseboard processor checks for the presence of a VIM module, through the presence bit on the VIM connector. If a module is present, the processor reads the module's ID EEPROM and generates a 16–bit checksum from the data read. If the generated checksum does not match the stored value, the processor illuminates its red LED. Even though the processor illuminates LED 0, the red LED, the processor is fully functional.

The contents of the ID EEPROM, plus the calculated checksum, are stored in Global SDRAM on the VIM baseboard. Refer to the respective VIM baseboard Operating Manual for the location of the Global SDRAM. The first word stored is a valid data flag, based on the checksum: valid checksum (**0x00EE CODE**), bad checksum (**0x000B ADC5**), or no VIM module installed (**0xFFFF FFFE**).

The ID EEPROM is accessed using a Model 6235 register at memory address VIM_base+0x0000, as offset from the VIM base address defined for the applicable VIM baseboard. The bit layout of this register is defined in Table A–1, below.

Table A–1: VIM ID EEPROM Register
R/W @ VIM_base+0x0000

Bit #	D31 – D4	D3	D2	D1	D0
Bit Name	Not Used	Chip Select	Serial Data Out	Reserved	Serial Clock
Access	Read/Write	Read/Write	Read Only	Read Only	Read/Write
Function	Not Applicable	1 = Selected 0 = Not Selected	Stored Data	Mask when reading	Toggle to pulse Clock line

A.2 EEPROM Format Example

Table A–2 on the next page shows the contents of the EEPROM for the Pentek Model 6235, and an explanation of what each pair of 16–bit words is used for. The SDRAM location is the address where each pair of words is stored relative to the start address of the Global SDRAM on the VIM baseboard.

A.2 EEPROM Format Example (continued)

Table A–2: EEPROM Example (Model 6235 shown)

EEPROM Word Location	SDRAM Location	Contents	Comments
00/01	+0x00	0x00EE C0DE	Valid data flag
02/03	+0x04	0x6235 0000	Model, Model Extension (Extension currently unused)
04/05	+0x08	0x0354 2001	PCB number – this is taken from the VIM board
06/07	+0x0C	0x0001 FFFF	Assembly Rev, Option #1 Rev A = 0001, Rev B = 0002, etc.; Option #1 – up to 9 installed options may be specified, if there are no options, field = '**FFFF**'
08/09	+0x10	0xFFFF FFFF	Option #2, Option #3
10/11	+0x14	0xFFFF FFFF	Option #4, Option #5
12/13	+0x18	0xFFFF FFFF	Option #6, Option #7
14/15	+0x1C	0xFFFF FFFF	Option #8, Option #9
16/17	+0x20	0xFFFF FFFF	
18/19	+0x24	0xFFFF FFFF	
20/21	+0x28	0xFFFF FFFF	
22/23	+0x2C	0xFFFF FFFF	
24/25	+0x30	0xFFFF FFFF	
26/27	+0x34	0xFFFF FFFF	
28/29	+0x38	0xFFFF FFFF	
30/31	+0x3C	0xFFFF FFFF	
32/33	+0x40	0xFFFF FFFF	
34/35	+0x44	0xFFFF FFFF	
36/37	+0x48	0xFFFF FFFF	
38/39	+0x4C	0xFFFF FFFF	Module Specific Code goes in locations 16 through 61
40/41	+0x50	0xFFFF FFFF	
42/43	+0x54	0xFFFF FFFF	
44/45	+0x58	0xFFFF FFFF	
46/47	+0x5C	0xFFFF FFFF	
48/49	+0x60	0xFFFF FFFF	
50/51	+0x64	0xFFFF FFFF	
52/53	+0x68	0xFFFF FFFF	
54/55	+0x6C	0xFFFF FFFF	
56/57	+0x70	0xFFFF FFFF	
58/59	+0x74	0xFFFF FFFF	
60/61	+0x78	0xFFFF FFFF	
62/63	+0x7C	0x0000 xxxx	Word 62 should always be cleared (**0000**). Word 63 contains the checksum of words 0 – 61.

Appendix B: Analog Devices ADM1024 System Hardware Monitor

B.1 Introduction

The following pages are a reprint of the Analog Devices ADM1024 System Hardware Monitor Data Sheet.

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System Hardware Monitor with Remote Diode Thermal Sensing

ADM1024

FEATURES

Up to Nine Measurement Channels
Inputs Programmable-to-Measure Analog Voltage, Fan Speed or External Temperature
External Temperature Measurement with Remote Diode (Two Channels)
On-Chip Temperature Sensor
Five Digital Inputs for VID Bits
LDCM Support
System Management Bus (SMBus)
Chassis Intrusion Detect
Interrupt and Over Temperature Outputs
Programmable $\overline{\text{RESET}}$ Input Pin
Shutdown Mode to Minimize Power Consumption
Limit Comparison of all Monitored Values

APPLICATIONS

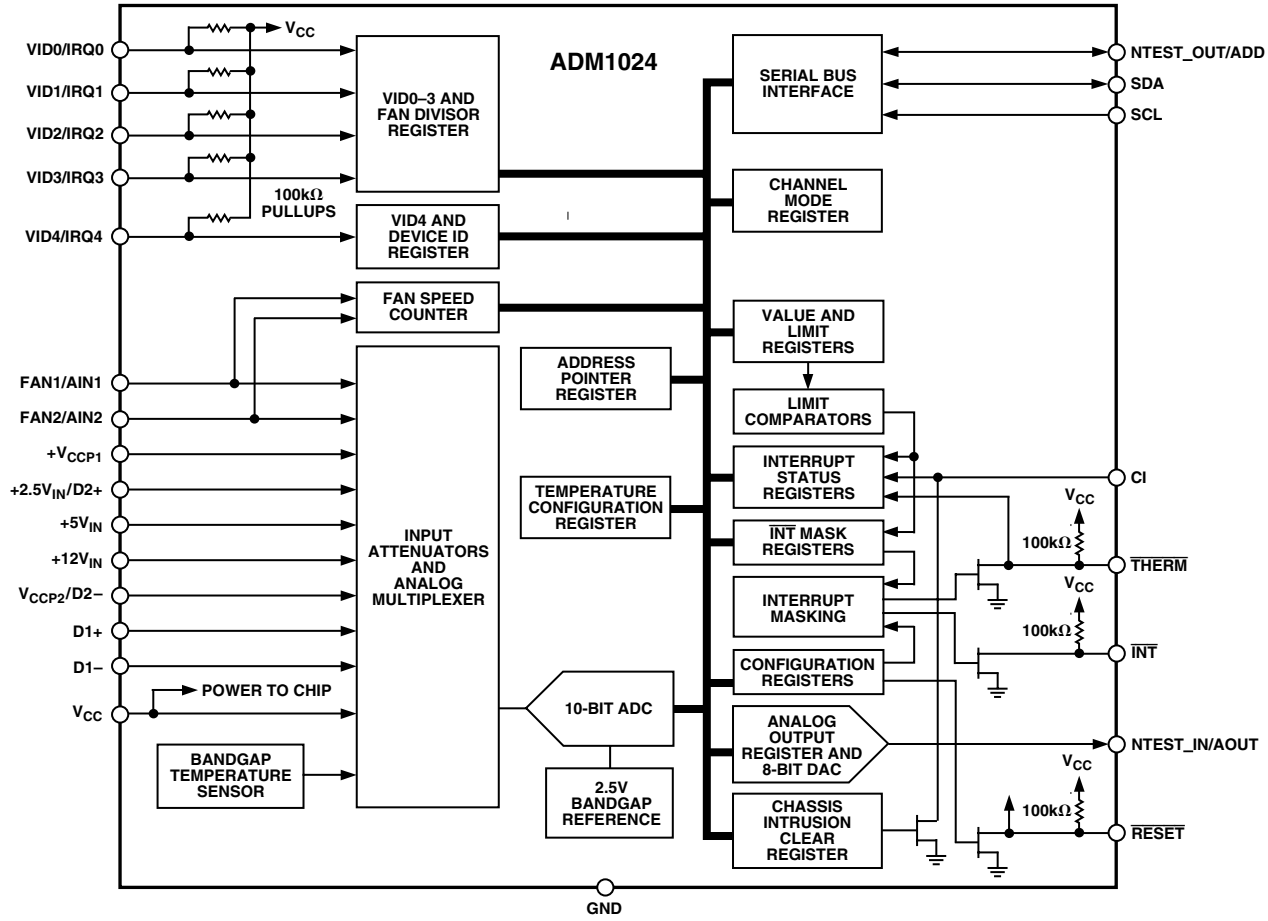
Network Servers and Personal Computers
Microprocessor-Based Office Equipment
Test Equipment and Measuring Instruments

PRODUCT DESCRIPTION

The ADM1024 is a complete system hardware monitor for microprocessor-based systems, providing measurement and limit comparison of various system parameters. Eight measurement inputs are provided, of which three are dedicated to monitoring 5 V and 12 V power supplies and the processor core voltage. The ADM1024 can monitor a fourth power-supply voltage by measuring its own V_{CC}. One input (two pins) is dedicated to a remote temperature-sensing diode. Two further pins can be

(*continued on page 7*)

FUNCTIONAL BLOCK DIAGRAM



REV. A

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ADM1024—SPECIFICATIONS[1, 2] ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage, V_{CC}	2.8	3.30	5.5	V	
Supply Current, I_{CC}		1.4	3.5	mA	Interface Inactive, ADC Active
		1.0		mA	ADC Inactive, DAC Active
		45	145	µA	Shutdown Mode
TEMPERATURE-TO-DIGITAL CONVERTER					
Internal Sensor Accuracy			±3	°C	$0°C \le T_A \le 100°C$
			±2	°C	$T_A = 25°C$
Resolution		±1		°C	
External Diode Sensor Accuracy			±5	°C	$0°C \le T_A \le 100°C$
		±3		°C	25°C
Resolution		±1		°C	
Remote Sensor Source Current	80	110	150	µA	High Level
	4	6.5	9	µA	Low Level
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error, TUE (12 V_{IN})			±4	%	(See Note 3)
TUE (AIN, V_{CCP}, 2.5 V_{IN}, 5 V_{IN})			±3	%	
Differential Nonlinearity, DNL			±1	LSB	
Power Supply Sensitivity		±1		%/V	
Conversion Time (Analog Input or Int. Temp)		754.8	856.8	µs	$0°C \le T_A \le 100°C$[4]
Conversion Time (External Temperature)		9.6		ms	(See Note 4)
Input Resistance (2.5 V, 5 V, 12 V, V_{CCP1}, V_{CCP2})	80	140	200	kΩ	
Input Resistance (AIN1, AIN2)		5		MΩ	
ANALOG OUTPUT					
Output Voltage Range	0		2.5	V	
Total Unadjusted Error, TUE			±3	%	I_L = 2 mA
Full-Scale Error		±1	±5	%	
Zero-Scale Error		2		LSB	No Load
Differential Nonlinearity, DNL			±1	LSB	Monotonic by Design
Integral Nonlinearity		±1		LSB	
Output Source Current		2		mA	
Output Sink Current		1		mA	
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy			±12	%	$0°C \le T_A \le 100°C$
Full-Scale Count			255		
FAN1 and FAN2 Nominal Input RPM[5]		8800		rpm	Divisor = 1, Fan Count = 153
		4400		rpm	Divisor = 2, Fan Count = 153
		2200		rpm	Divisor = 3, Fan Count = 153
		1100		rpm	Divisor = 4, Fan Count = 153
Internal Clock Frequency	19.8	22.5	25.2	kHz	$0°C \le T_A \le 100°C$
DIGITAL OUTPUTS NTEST_OUT					
Output High Voltage, V_{OH}	2.4			V	I_{OUT} = +3.0 mA, V_{CC} = 2.85 V – 3.60 V
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –3.0 mA, V_{CC} = 2.85 V – 3.60 V
OPEN-DRAIN DIGITAL OUTPUTS (INT, $\overline{\text{THERM}}$, $\overline{\text{RESET}}$)					(See Note 6)
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –3.0 mA, V_{CC} = 3.60 V
High Level Output Current, I_{OH}		0.1	100	µA	$V_{OUT} = V_{CC}$
$\overline{\text{RESET}}$ and CI Pulsewidth	20	45		ms	
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –3.0 mA, V_{CC} = 2.85 V – 3.60 V
High Level Output Current, I_{OH}		0.1	100	µA	$V_{OUT} = V_{CC}$

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	2.2			V	
Input Low Voltage, V_{IL}			0.8	V	
Hysteresis		500		mV	
Glitch Immunity		100		ns	
DIGITAL INPUT LOGIC LEVELS (ADD, CI, $\overline{\text{RESET}}$, VID0–VID4, FAN1, FAN2)					(See Note 7)
Input High Voltage, V_{IH}	2.2			V	V_{CC} = 2.85 V – 5.5 V
Input Low Voltage, V_{IL}			0.8	V	V_{CC} = 2.85 V – 5.5 V
NTEST_IN					
Input High Voltage, V_{IH}	2.2			V	V_{CC} = 2.85 V – 5.5 V
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	–1			µA	$V_{IN} = V_{CC}$
Input Low Current, I_{IL}			1	µA	V_{IN} = 0
Input Capacitance, C_{IN}		20		pF	
SERIAL BUS TIMING[8]					
Clock Frequency, f_{SCLK}			400	kHz	See Figure 1
Glitch Immunity, t_{SW}			50	ns	See Figure 1
Bus Free Time, t_{BUF}	1.3			µs	See Figure 1
Start Setup Time, $t_{SU;STA}$	600			ns	See Figure 1
Start Hold Time, $t_{HD;STA}$	600			ns	See Figure 1
SCL Low Time, t_{LOW}	1.3			µs	See Figure 1
SCL High Time, t_{HIGH}	0.6			µs	See Figure 1
SCL, SDA Rise Time, t_r			300	ns	See Figure 1
SCL, SDA Fall Time, t_f			300	µs	See Figure 1
Data Setup Time, $t_{SU;DAT}$	100			ns	See Figure 1
Data Hold Time, $t_{HD;DAT}$			900	ns	See Figure 1

NOTES

[1]All voltages are measured with respect to GND, unless otherwise specified.

[2]Typicals are at T_A = 25°C and represent most likely parametric norm. Shutdown current typ is measured with V_{CC} = 3.3 V.

[3]TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC, multiplexer and on-chip input attenuators, including an external series input protection resistor value between zero and 1 kΩ.

[4]Total monitoring cycle time is nominally $m \times 755$ µs + $n \times 33244$ µs, where m is the number of channels configured as analog inputs, plus two for the internal V_{CC} measurement and internal temperature sensor, and n is the number of channels configured as external temperature channels (D1 and D2).

[5]The total fan count is based on two pulses per revolution of the fan tachometer output.

[6]Open-drain digital outputs may have an external pull-up resistor connected to a voltage lower or higher than V_{CC} (up to 6.5 V absolute maximum).

[7]All logic inputs except ADD are tolerant of 5 V logic levels, even if V_{CC} is less than 5 V. ADD is a three-state input that may connected to V_{CC}, GND, or left open-circuit.

[8]Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.2 V for a rising edge.

Specifications subject to change without notice.

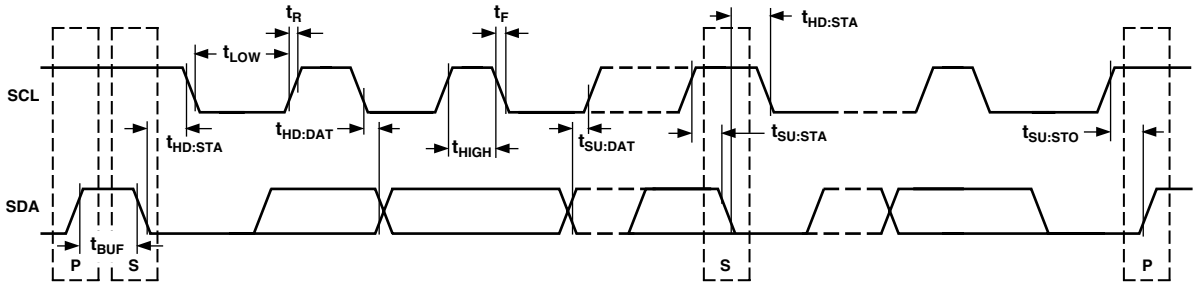


Figure 1. Diagram for Serial Bus Timing

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (V_{CC}) . . . . . 6.5 V
Voltage on 12 V V_{IN} Pin . . . . . 20 V
Voltage on AOUT, N TEST_OUT ADD, 2.5 V_{IN}/D2+ . . . . . –0.3 V to (V_{CC} + 0.3 V)
Voltage on Any Other Input or Output Pin . . –0.3 V to +6.5 V
Input Current at Any Pin . . . . . ±5 mA
Package Input Current . . . . . ±20 mA
Maximum Junction Temperature (T_J max) . . . . . 150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering
Vapor Phase 60 sec . . . . . 215°C
Infrared 15 sec . . . . . 200°C
ESD Rating All Pins . . . . . 2000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

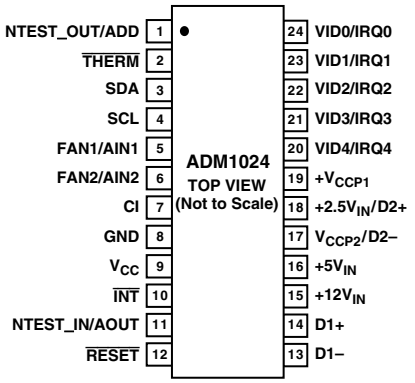
THERMAL CHARACTERISTICS

24-Lead Small Outline Package: θ_{JA} = 50°C/W, θ_{JC} = 10°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1024ARU	0°C to 100°C	24-Lead TSSOP	RU-24

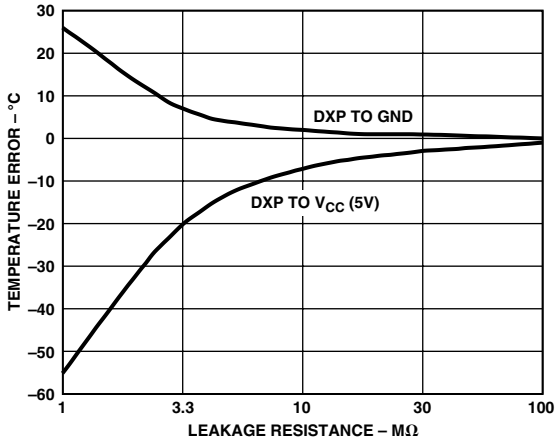
PIN CONFIGURATION



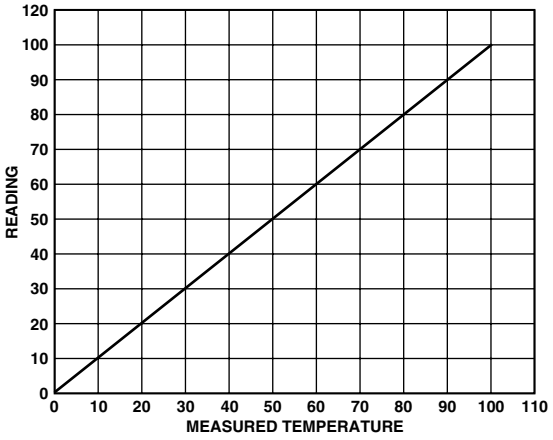
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	NTEST_OUT/ADD	Digital I/O. Dual Function pin. This is a three-state input that controls the 2 LSBs of the Serial Bus Address. This pin functions as an output when doing a NAND test.
2	$\overline{\text{THERM}}$	Digital I/O. Dual Function pin. This pin functions as an interrupt output for temperature interrupts only, or as an interrupt input for fan control. It has an on-chip 100 kΩ pull-up resistor.
3	SDA	Digital I/O. Serial Bus bidirectional Data. Open-drain output.
4	SCL	Digital Input. Serial Bus Clock.
5	FAN1/AIN1	Programmable Analog/Digital Input. 0 V to 2.5 V analog input or digital (0 to V_{CC}) amplitude fan tachometer input.
6	FAN2/AIN2	Programmable Analog/Digital Input. 0 V to 2.5 V analog input or digital (0 to V_{CC}) amplitude fan tachometer input.
7	CI	Digital I/O. An active high input from an external latch which captures a Chassis Intrusion event. This line can go high without any clamping action, regardless of the powered state of the ADM1024. The ADM1024 provides an internal open drain on this line, controlled by Bit 6 of Register 40h or Bit 7 of Register 46h, to provide a minimum 20 ms pulse on this line, to reset the external Chassis Intrusion Latch.
8	GND	System Ground.
9	V_{CC}	POWER (2.8 V to 5.5 V). Typically powered from 3.3 V power rail. Bypass with the parallel combination of 10 μF (electrolytic or tantalum) and 0.1 μF (ceramic) bypass capacitors.
10	$\overline{\text{INT}}$	Digital Output. Interrupt Request (open-drain). The output is enabled when Bit 1 of Register 40h is set to 1. The default state is disabled. It has an on-chip 100 kΩ pull-up resistor.
11	NTEST_IN/AOUT	Digital Input/Analog Output. An active-high input that enables NAND Test mode board-level connectivity testing. Refer to section on NAND testing. Also functions as a programmable analog output when NAND Test is not selected.
12	$\overline{\text{RESET}}$	Digital I/O. Master Reset, 5 mA driver (open drain), active low output with a 45 ms minimum pulsewidth. Set using Bit 4 in Register 40h. Also acts as reset input when pulled low (e.g., power-on reset). It has an on-chip 100 kΩ pull-up resistor.
13	D1–	Analog Input. Connected to cathode of first external temperature sensing diode.
14	D1+	Analog Input. Connected to anode of first external temperature sensing diode.
15	+12 V_{IN}	Programmable Analog Input. Monitors 12 V supply.
16	+5 V_{IN}	Analog Input. Monitors 5 V supply.
17	V_{CCP2}/D2–	Programmable Analog Input. Monitors second processor core voltage or cathode of second external temperature sensing diode.
18	+2.5 V_{IN}/D2+	Programmable Analog Input. Monitors 2.5 V supply or anode of second external temperature sensing diode.
19	+V_{CCP1}	Analog Input. Monitors 1st processor core voltage (0 V to 3.6 V).
20	VID4/IRQ4	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID4 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.
21	VID3/IRQ3	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID0–VID3 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.
22	VID2/IRQ2	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID0-VID3 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.
23	VID1/IRQ1	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID0–VID3 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.
24	VID0/IRQ0	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID0–VID3 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.

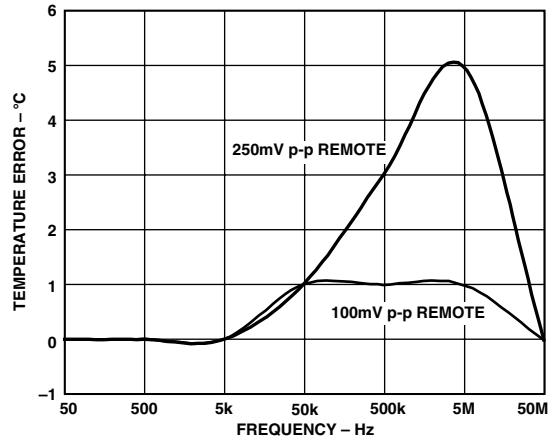
ADM1024–Typical Performance Characteristics



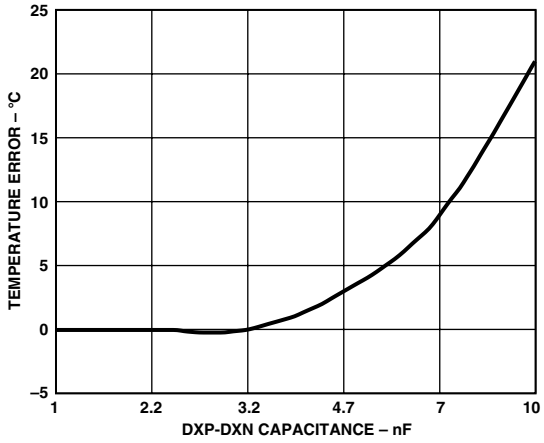
TPC 1. Temperature Error vs. PC Board Track Resistance



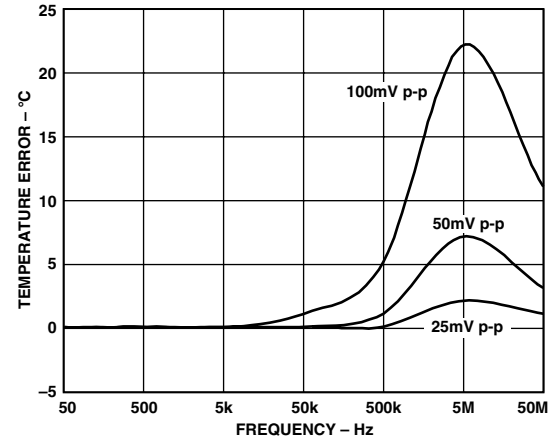
TPC 4. Pentium® III Temperature Measurement vs. ADM1024 Reading



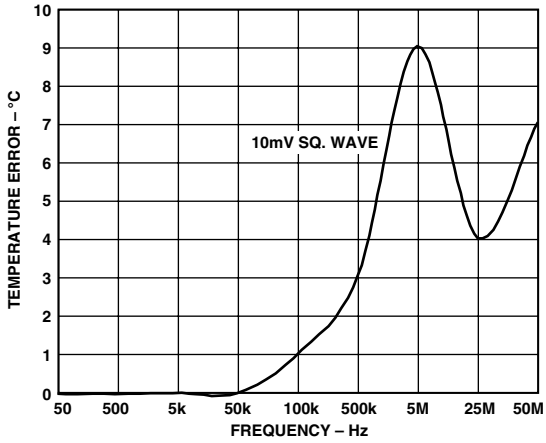
TPC 2. Temperature Error vs. Power Supply Noise Frequency



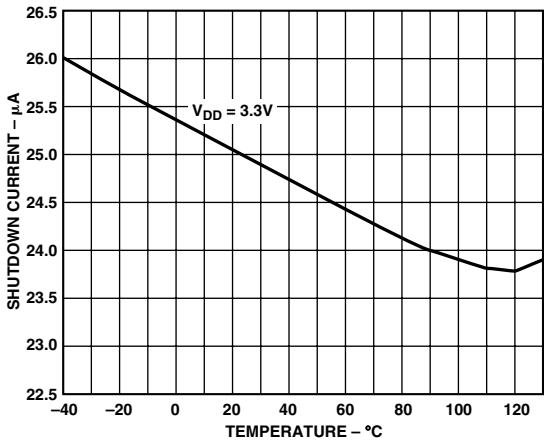
TPC 5. Temperature Error vs. Capacitance Between D+ and D–



TPC 3. Temperature Error vs. Common-Mode Noise Frequency



TPC 6. Temperature Error vs. Differential-Mode Noise Frequency



TPC 7. Standby Current vs. Temperature

(continued from page 1)

configured as inputs to monitor a 2.5 V supply and a second processor core voltage, or as a second temperature sensing input. The remaining two inputs can be programmed as general-purpose analog inputs or as digital fan-speed measuring inputs.

Measured values can be read out via an SMBus serial System Management Bus, and values for limit comparisons can be programmed in over the same serial bus. The high-speed successive-approximation ADC allows frequent sampling of all analog channels to ensure a fast interrupt response to any out-of-limit measurement.

The ADM1024's 2.8 V to 5.5 V supply voltage range, low supply current, and SMBus interface make it ideal for a wide range of applications. These include hardware monitoring and protection applications in personal computers, electronic test equipment, and office electronics.

GENERAL DESCRIPTION

The ADM1024 is a complete system hardware monitor for microprocessor-based systems. The device communicates with the system via a serial System Management Bus. The serial bus controller has a hardwired address line for device selection (Pin 1), a serial data line for reading and writing addresses and data (Pin 3), and an input line for the serial clock (Pin 4). All control and programming functions of the ADM1024 are performed over the serial bus.

MEASUREMENT INPUTS

Programmability of the measurement inputs makes the ADM1024 extremely flexible and versatile. The device has a 10-bit A-to-D converter, and nine measurement input pins that can be configured in different ways.

Pins 5 and 6 can be programmed as general-purpose analog inputs with a range of 0 V to 2.5 V, or as digital inputs to monitor the speed of fans with digital tachometer outputs. The fan inputs can be programmed to accommodate fans with different speeds and different numbers of pulses per revolution from their tach outputs.

Pins 13 and 14 are dedicated temperature inputs and may be connected to the cathode and anode of an external temperature-sensing diode.

Pins 15, 16, and 19 are dedicated analog inputs with on-chip attenuators, configured to monitor 12 V, 5 V and the processor core voltage, respectively.

Pins 17 and 18 may be configured as analog inputs with on-chip attenuators to monitor a second processor core voltage and a 2.5 V supply, or they may be configured as a temperature input and connected to a second temperature-sensing diode.

The ADC also accepts input from an on-chip bandgap temperature sensor that monitors system-ambient temperature.

Finally, the ADM1024 monitors the supply from which it is powered, so there is no need for a separate 3.3 V analog input, if the chip V_{CC} is 3.3 V. The range of this V_{CC} measurement can be configured for either a 3.3 V or 5 V V_{CC} by Bit 3 of the Channel Mode Register.

SEQUENTIAL MEASUREMENT

When the ADM1024 monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensor, while at the same time the fan speed inputs are independently monitored. Measured values from these inputs are stored in Value Registers. These can be read out over the serial bus, or can be compared with programmed limits stored in the Limit Registers. The results of out-of-limit comparisons are stored in the Interrupt Status Registers, and will generate an interrupt on the $\overline{INT}$ line (Pin 10).

Any or all of the Interrupt Status Bits can be masked by appropriate programming of the Interrupt Mask Register.

PROCESSOR VOLTAGE ID

Five digital inputs (VID4 to VID0—Pins 20 to 24) read the processor voltage ID code. These inputs can also be reconfigured as interrupt inputs.

The VID pins have internal 100 kΩ pull-up resistors.

CHASSIS INTRUSION

A chassis intrusion input (Pin 7) is provided to detect unauthorized tampering with the equipment.

$\overline{RESET}$

A $\overline{RESET}$ input/output (Pin 12) is provided. Pulling this pin low will reset all ADM1024 internal registers to default values. The ADM1024 can also be programmed to give a low-going 45 ms reset pulse at this pin.

The $\overline{RESET}$ pin has an internal, 100 kΩ pull-up resistor.

ANALOG OUTPUT

The ADM1024 contains an on-chip, 8-bit digital-to-analog converter with an output range of zero to 2.5 V (Pin 11). This is typically used to implement a temperature-controlled fan by controlling the speed of a fan dependent upon the temperature measured by the on-chip temperature sensor.

Testing of board level connectivity is simplified by providing a NAND tree test function. The AOUT (Pin 11) also doubles as a NAND test input, while Pin 1 doubles as a NAND tree output.

INTERNAL REGISTERS OF THE ADM1024

A brief description of the ADM1024's principal internal registers is given below. More detailed information on the function of each register is given in Tables VI to XIX.

Configuration Registers: Provide control and configuration.

Channel Mode Register: Stores the data for the operating modes of the input channels.

Address Pointer Register: This register contains the address that selects one of the other internal registers. When writing to the ADM1024, the first byte of data is always a register address, which is written to the Address Pointer Register.

Interrupt ($\overline{INT}$) Status Registers: Two registers to provide status of each Interrupt event. These registers are also mirrored at addresses 4Ch and 4Dh.

Interrupt ($\overline{INT}$) Mask Registers: Allow masking of individual interrupt sources.

Temperature Configuration Register: The configuration of the temperature interrupt is controlled by the lower three bits of this register.

VID/Fan Divisor Register: The status of the VID0 to VID4 pins of the processor can be written to and read from these registers. Divisor values for fan-speed measurement are also stored in this register.

Value and Limit Registers: The results of analog voltage inputs, temperature and fan speed measurements are stored in these registers, along with their limit values.

Analog Output Register: The code controlling the analog output DAC is stored in this register.

Chassis Intrusion Clear Register: A signal latched on the chassis intrusion pin can be cleared by writing to this register.

SERIAL BUS INTERFACE

Control of the ADM1024 is carried out via the serial bus. The ADM1024 is connected to this bus as a slave device, under the control of a master device, e.g., ICH.

The ADM1024 has a 7-bit serial bus address. When the device is powered up, it will do so with a default serial bus address. The five MSBs of the address are set to 01011, the two LSBs are determined by the logical states of Pin 1 (NTESTOUT/ADD). This is a three-state input that can be grounded, connected to V_{CC} or left open-circuit to give three different addresses.

Table I. ADD Pin Truth Table

ADD Pin	A1	A0
GND	1	0
No Connect	0	0
V_{CC}	0	1

If ADD is left open-circuit the default address will be 0101100. ADD is sampled only at power-up, so any changes made while power is on will have no immediate effect.

The facility to make hardwired changes to A1 and A0 allows the user to avoid conflicts with other devices sharing the same serial bus, for example if more than one ADM1024 is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line, SCL, remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master will write to the slave device. If the R/$\overline{W}$ bit is a 1, the master will read from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low-to-high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADM1024, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions.

To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register. This is illustrated in Figure 2a. The device address is sent over the bus followed by R/$\overline{W}$ set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

When reading data from a register there are two possibilities:

1. If the ADM1024's Address Pointer Register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADM1024 as before, but only the data byte containing the register address is sent, as data is not to be written to the register. This is shown in Figure 2b.

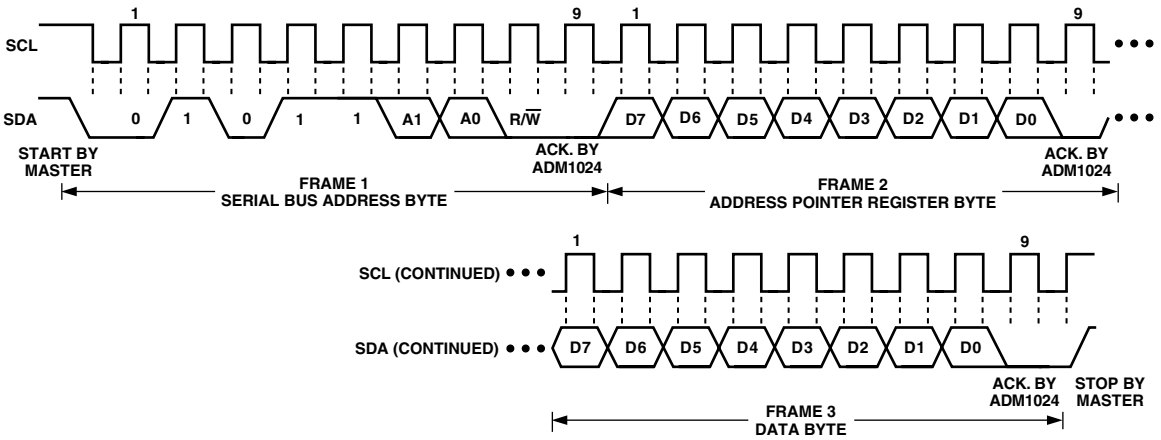


Figure 2a. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

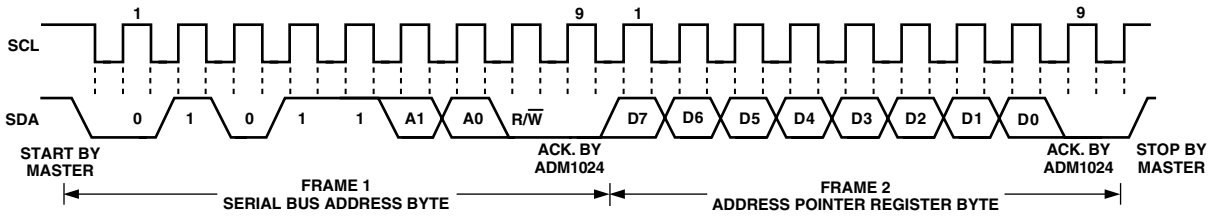


Figure 2b. Writing to the Address Pointer Register Only

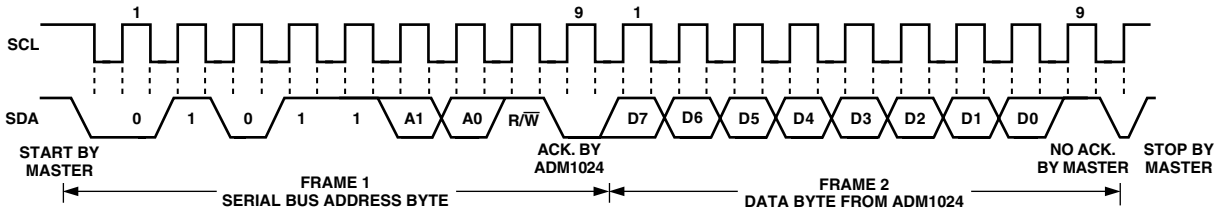


Figure 2c. Reading Data from a Previously Selected Register

A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 2c.

2. If the Address Pointer Register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the Address Pointer Register, so Figure 2b can be omitted.

NOTES

1. Although it is possible to read a data byte from a data register without first writing to the Address Pointer Register, if the Address Pointer Register is already at the correct value, it is not possible to write data to a register without writing to the Address Pointer Register because the first data byte of a write is always written to the Address Pointer Register.
2. In Figures 2a to 2c, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the three-state ADD pin.

MEASUREMENT INPUTS

The ADM1024 has nine external measurement pins that can be configured to perform various functions by programming the Channel Mode Register.

Pins 13 and 14 are dedicated to temperature measurement, while Pins 15, 16, and 19 are dedicated analog input channels. Their function is unaffected by the Channel Mode Register.

Pins 5 and 6 can be individually programmed as analog inputs, or as digital fan speed measurement inputs, by programming Bits 0 and 1 of the Channel Mode Register.

Pins 17 and 18 can be configured as analog inputs or as inputs for external temperature-sensing diodes by programming Bit 2 of the Channel Mode Register.

Bit 3 of the Channel Mode Register configures the internal V_{CC} measurement range for either 3.3 V or 5 V.

Bits 4 to 6 of the Channel Mode Register enable or disable Pins 22 to 24, when they are configured as interrupt inputs by setting Bit 7 of the Channel Mode Register. This function is controlled for Pins 20 and 21 by Bits 6 and 7 of Configuration Register 2.

Bit 7 of the Channel Mode Register allows the processor core voltage ID bits (VID0 to VID4, Pins 24 to 20) to be reconfigured as interrupt inputs.

A truth table for the Channel Mode Register is given in Table II.

Table II. Channel Mode Register

Channel Mode Register Bit	Controls Pin(s)	Function
0	5	0 = FAN1, 1 = AIN1
1	6	0 = FAN2, 1 = AIN2
2	17, 18	0 = 2.5 V, V_{CCP2}, 1 = D2–, D2+
3	Int. V_{CC} Meas.	0 = 3.3 V, 1 = 5 V
4	24	0 = VID0, 1 = IRQ0
5	23	0 = VID1, 1 = IRQ1
6	22	0 = VID2, 1 = IRQ2
7	20–24	0 = VID0 to VID4, 1 = Interrupt Inputs

Power-on Default = 0000 0000

Table III. A/D Output Code vs. V_{IN}

Input Voltage							A/D Output	
+12 V_{IN}	+5 V_{IN}	V_{CC} (3.3 V)	V_{CC} (5 V)	+2.5 V_{IN}	+$V_{CCP1/2}$	AIN(1/2)	Decimal	Binary
<0.062	<0.026	<0.0172	<0.026	<0.013	<0.014	<0.010	0	00000000
0.062–0.125	0.026–0.052	0.017–0.034	0.026–0.052	0.013–0.026	0.014–0.028	0.010–0.019	1	00000001
0.125–0.188	0.052–0.078	0.034–0.052	0.052–0.078	0.026–0.039	0.028–0.042	0.019–0.029	2	00000010
0.188–0.250	0.078–0.104	0.052–0.069	0.078–0.104	0.039–0.052	0.042–0.056	0.029–0.039	3	00000011
0.250–0.313	0.104–0.130	0.069–0.086	0.104–0.130	0.052–0.065	0.056–0.070	0.039–0.049	4	00000100
0.313–0.375	0.130–0.156	0.086–0.103	0.130–0.156	0.065–0.078	0.070–0.084	0.049–0.058	5	00000101
0.375–0.438	0.156–0.182	0.103–0.120	0.156–0.182	0.078–0.091	0.084–0.098	0.058–0.068	6	00000110
0.438–0.500	0.182–0.208	0.120–0.138	0.182–0.208	0.091–0.104	0.098–0.112	0.068–0.078	7	00000111
0.500–0.563	0.208–0.234	0.138–0.155	0.208–0.234	0.104–0.117	0.112–0.126	0.078–0.087	8	00001000
4.000–4.063	1.666–1.692	1.100–1.117	1.666–1.692	• • • 0.833–0.846	0.900–0.914	0.625–0.635	64 (1/4-Scale)	01000000
8.000–8.063	3.330–3.560	2.200–2.217	3.330–3.560	• • • 1.667–1.680	1.800–1.814	1.250–1.260	128 (1/2-Scale)	10000000
12.000–12.063	5.000–5.026	3.300–3.317	5.000–5.026	• • • 2.500–2.513	2.700–2.714	1.875–1.885	192 (3/4-Scale)	11000000
15.312–15.375	6.380–6.406	4.210–4.230	6.380–6.406	• • • 3.190–3.203	3.445–3.459	2.392–2.402	245	11110101
15.375–15.437	6.406–6.432	4.230–4.245	6.406–6.432	3.203–3.216	3.459–3.473	2.402–2.412	246	11110110
15.437–15.500	6.432–6.458	4.245–4.263	6.432–6.458	3.216–3.229	3.473–3.487	2.412–2.422	247	11110111
15.500–15.563	6.458–6.484	4.263–4.280	6.458–6.484	3.229–3.242	3.487–3.501	2.422–2.431	248	11111000
15.563–15.625	6.484–6.510	4.280–4.300	6.484–6.510	3.242–3.255	3.501–3.515	2.431–2.441	249	11111001
15.625–15.688	6.510–6.536	4.300–4.314	6.510–6.536	3.255–3.268	3.515–3.529	2.441–2.451	250	11111010
15.688–15.750	6.536–6.562	4.314–4.331	6.536–6.562	3.268–3.281	3.529–3.543	2.451–2.460	251	11111011
15.750–15.812	6.562–6.588	4.331–4.348	6.562–6.588	3.281–3.294	3.543–3.558	2.460–2.470	252	11111100
15.812–15.875	6.588–6.615	4.348–4.366	6.588–6.615	3.294–3.307	3.558–3.572	2.470–2.480	253	11111101
15.875–15.938	6.615–6.640	4.366–4.383	6.615–6.640	3.307–3.320	3.572–3.586	2.480–2.490	254	11111110
>15.938	>6.640	>4.383	>6.640	>3.320	>3.586	>2.490	255	11111111

A-TO-D CONVERTER

These inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of eight bits. The basic input range is zero to 2.5 V, which is the input range of AIN1 and AIN2, but five of the inputs have built-in attenuators to allow measurement of 2.5 V, 5 V, 12 V and the processor core voltages V_{CCP1} and V_{CCP2}, without any external components. To allow for the tolerance of these supply voltages, the A-to-D converter produces an output of 3/4 full-scale (decimal 192) for the nominal input voltage, and so has adequate headroom to cope with overvoltages. Table III shows the input ranges of the analog inputs and output codes of the A-to-D converter.

When the ADC is running, it samples and converts an input every 748 µs, except for the external temperature (D1 and D2) inputs. These have special input signal conditioning and are averaged over 16 conversions to reduce noise, and a measurement on one of these inputs takes nominally 9.6 ms.

INPUT CIRCUITS

The internal structure for the analog inputs are shown in Figure 3. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter which gives the input immunity to high frequency noise.

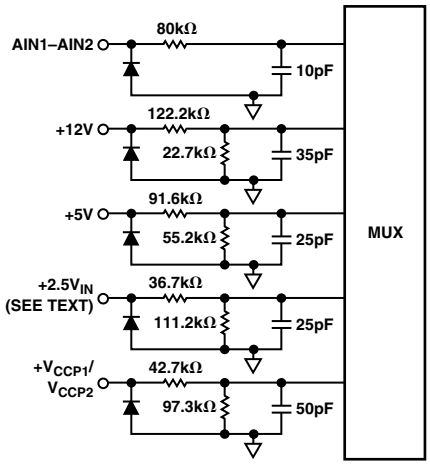


Figure 3. Structure of Analog Inputs

2.5 V INPUT PRECAUTIONS

When using the 2.5 V input, the following precautions should be noted. There is a parasitic diode between Pin 18 and V_{CC} due to the presence of a PMOS current source (which is used when Pin 18 is configured as a temperature input). This will become forward-biased if Pin 18 is more than 0.3 V above V_{CC}. Therefore, V_{CC} should never be powered off with a 2.5 V input connected.

SETTING OTHER INPUT RANGES

AIN1 and AIN2 can easily be scaled to voltages other than 2.5 V. If the input voltage range is zero to some positive voltage, all that is required is an input attenuator, as shown in Figure 4.

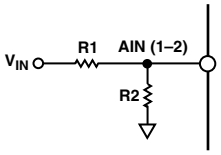


Figure 4. Scaling AIN(1–2)

$$\frac{R1}{R2} = \frac{(V_{FS} - 2.5)}{2.5}$$

Negative and bipolar input ranges can be accommodated by using a positive reference voltage to offset the input voltage range so it is always positive.

To measure a negative input voltage, an attenuator can be used as shown in Figure 5.

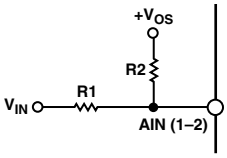


Figure 5. Scaling and Offsetting AIN(1–2) for Negative Inputs

$$\frac{R1}{R2} = \frac{|V_{FS-}|}{V_{OS}}$$

This is a simple and cheap solution, but the following point should be noted. Since the input signal is offset but not inverted, the input range is transposed. An increase in the magnitude of the –12 V supply (going more negative), will cause the input voltage to fall and give a lower output code from the ADC. Conversely, a decrease in the magnitude of the –12 V supply will cause the ADC code to increase. The maximum negative voltage corresponds to zero output from the ADC. This means that the upper and lower limits will be transposed.

Bipolar input ranges can easily be accommodated. By making R1 equal to R2 and V_{OS} = 2.5 V, the input range is ±2.5 V. Other input ranges can be accommodated by adding a third resistor to set the positive full-scale input voltage.

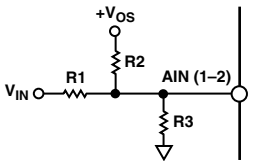


Figure 6. Scaling and Offsetting AIN(1–2) for Bipolar Inputs

$$\frac{R1}{R2} = \frac{|V_{FS-}|}{R2}$$

(R3 has no effect as the input voltage at the device Pin is zero when V_{IN} = minus full-scale.)

$$\frac{R1}{R3} = \frac{(V_{FS+} - 2.5)}{2.5}$$

(R2 has no effect as the input voltage at the device pin is 2.5 V when V_{IN} = plus full-scale).

Offset voltages other than 2.5 V can be used, but the calculation becomes more complicated.

TEMPERATURE MEASUREMENT SYSTEM

Internal Temperature Measurement

The ADM1024 contains an on-chip bandgap temperature sensor, whose output is digitized by the on-chip ADC. The temperature data is stored in the Temperature Value Register (address 27h) and the LSB from Bits 6 and 7 of the Temperature Configuration

Register (address 4Bh). As both positive and negative temperatures can be measured, the temperature data is stored in two's complement format, as shown in Table IV. Theoretically, the temperature sensor and ADC can measure temperatures from –128°C to +127°C with a resolution of 1°C, although temperatures below –40°C and above +125°C are outside the operating temperature range of the device.

External Temperature Measurement

The ADM1024 can measure the temperature of two external diode sensors or diode-connected transistors, connected to Pins 13 and 14 or 17 and 18.

Pins 13 and 14 are a dedicated temperature input channel. Pins 17 and 18 can be configured to measure a diode sensor by setting Bit 2 of the Channel Mode Register to 1.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{BE}, varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass-production.

The technique used in the ADM1024 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by:

$$\Delta V_{BE} = KT/q \times ln(N)$$

where:

K is Boltzmann's constant
q is charge on the carrier
T is absolute temperature in Kelvins
N is ratio of the two currents.

Figure 7 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

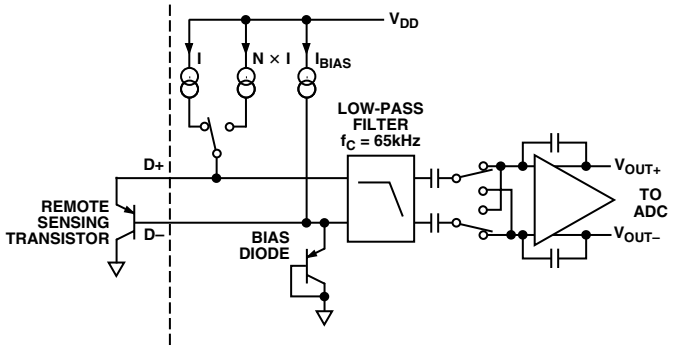


Figure 7. Signal Conditioning for External Diode Temperature Sensors

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input.

To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the section on layout considerations for more information on C1.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise, thence to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 8-bit two's complement format. To further reduce the effects of noise. Digital filtering is performed by averaging the results of 16 measurement cycles. An external temperature measurement takes nominally 9.6 ms.

The results of external temperature measurements are stored in 8-bit, two's-complement format, as illustrated in Table IV.

Table IV. Temperature Data Format

Temperature	Digital Output
–128°C	1000 0000
–125°C	1000 0011
–100°C	1001 1100
–75°C	1011 0101
–50°C	1100 1110
–25°C	1110 0111
0°C	0000 0000
+0.5°C	0000 0000
+10°C	0000 1010
+25°C	0001 1001
+50°C	0011 0010
+75°C	0100 1011
+100°C	0110 0100
+125°C	0111 1101
+127°C	0111 1111

LAYOUT CONSIDERATIONS

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADM1024 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. Ten mil track minimum width and spacing is recommended.



Figure 8. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and at the same temperature.

   Thermocouple effects should not be a major problem as 1°C corresponds to about 240 µV, and thermocouple voltages are about 3 µV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.

5. Place 0.1 µF bypass and 2200 pF input filter capacitors close to the ADM1024.

6. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This will work up to about 6 feet to 12 feet.

7. For really long distances (up to 100 feet) use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D– and the shield to GND close to the ADM1024. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. One Ω series resistance introduces about 0.5°C error.

LIMIT VALUES

Limit values for analog measurements are stored in the appropriate limit registers. In the case of voltage measurements, high and low limits can be stored so that an interrupt request will be generated if the measured value goes above or below acceptable values. In the case of temperature, a Hot Temperature or High Limit can be programmed, and a Hot Temperature Hysteresis or Low Limit, which will usually be some degrees lower. This can be useful as it allows the system to be shut down when the hot limit is exceeded, and restarted automatically when it has cooled down to a safe temperature.

MONITORING CYCLE TIME

The monitoring cycle begins when a one is written to the Start Bit (Bit 0), and a zero to the $\overline{\text{INT}}$_Clear Bit (Bit 3) of the Configuration Register. $\overline{\text{INT}}$_Enable (Bit 1) should be set to one to enable the $\overline{\text{INT}}$ output. The ADC measures each analog input in turn, as each measurement is completed the result is automatically stored in the appropriate value register. This "round-robin" monitoring cycle continues until it is disabled by writing a 0 to Bit 0 of the Configuration Register.

As the ADC will normally be left to free-run in this manner, the time taken to monitor all the analog inputs will normally not be of interest, as the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can be calculated as follows:

$$m \times t_1 \times n \times t_2$$

where:

m is the number of inputs configured as analog inputs, plus the internal V_{CC} measurement and internal temperature sensor.

t_1 is the time taken for an analog input conversion, nominally 755 µs.

n is the number of inputs configured as external temperature inputs.

t_2 is the time taken for a temperature conversion, nominally 33.24 ms.

This rapid sampling of the analog inputs ensures a quick response in the event of any input going out of limits, unlike other monitoring chips that employ slower ADCs.

FAN MONITORING CYCLE TIME

When a monitoring cycle is started, monitoring of the fan speed inputs begins at the same time as monitoring of the analog inputs. However, the two monitoring cycles are not synchronized in any way. The monitoring cycle time for the fan inputs is dependent on fan speed and is much slower than for the analog inputs. For more details see Fan Speed Measurement section.

INPUT SAFETY

Scaling of the analog inputs is performed on chip, so external attenuators are normally not required. However, since the power supply voltages will appear directly at the pins, its is advisable to add small external resistors in series with the supply traces to the chip to prevent damaging the traces or power supplies should a accidental short such as a probe connect two power supplies together.

As the resistors will form part of the input attenuators, they will affect the accuracy of the analog measurement if their value is too high. The analog input channels are calibrated assuming an external series resistor of 500 Ω, and the accuracy will remain within specification for any value from zero to 1 kΩ, so a standard 510 Ω resistor is suitable.

The worst such accident would be connecting –12 V to +12 V—a total of 24 V difference, with the series resistors this would draw a maximum current of approximately 24 mA.

ANALOG OUTPUT

The ADM1024 has a single analog output from a unsigned 8-bit DAC which produces 0 V–2.5 V. The analog output register defaults to FF during power-on reset, which produces maximum fan speed. The analog output may be amplified and buffered with external circuitry such as an op amp and transistor to provide fan speed control.

Suitable fan drive circuits are given in Figures 9a to 9f. When using any of these circuits, the following points should be noted:

1. All of these circuits will provide an output range from zero to almost 12 V, apart from Figure 10a which loses the base-emitter voltage drop of Q1 due to the emitter-follower configuration.
2. To amplify the 2.5 V range of the analog output up to 12 V, the gain of these circuits needs to be around 4.8.
3. Care must be taken when choosing the op amp to ensure that its input common-mode range and output voltage swing are suitable.
4. The op amp may be powered from the 12 V rail alone or from ±12 V. If it is powered from 12 V then the input common-mode range should include ground to accommodate the minimum output voltage of the DAC, and the output voltage should swing below 0.6 V to ensure that the transistor can be turned fully off.
5. If the op amp is powered from –12 V, precautions such as a clamp diode to ground may be needed to prevent the base-emitter junction of the output transistor being reverse-biased in the unlikely event that the output of the op amp should swing negative for any reason.

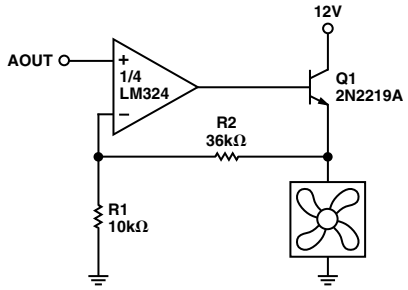


Figure 9a. Fan Drive Circuit with Op Amp and Emitter—Follower

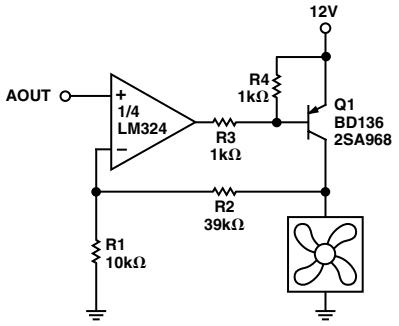


Figure 9b. Fan Drive Circuit with Op Amp and PNP Transistor

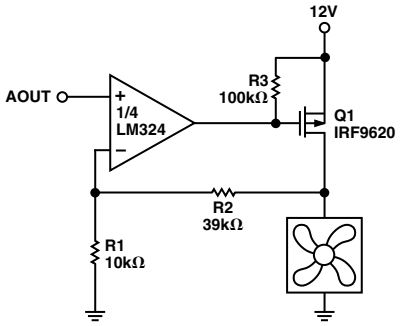


Figure 9c. Fan Driver Circuit with Op Amp and P-Channel MOSFET

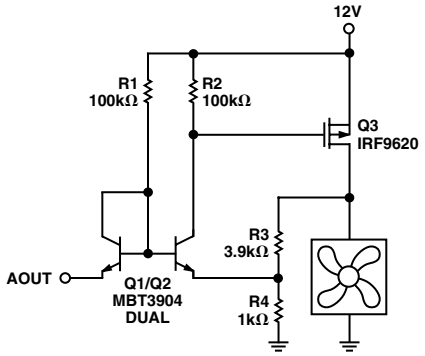


Figure 9d. Discrete Fan Drive Circuit with P-Channel MOSFET, Single Supply

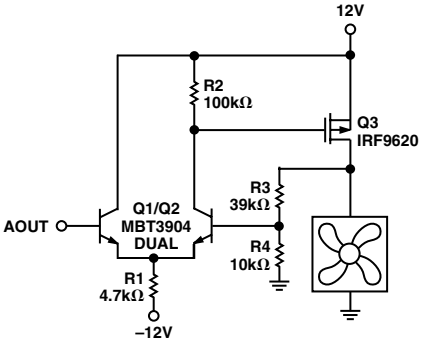


Figure 9e. Discrete Fan Drive Circuit with P-Channel MOSFET, Dual Supply

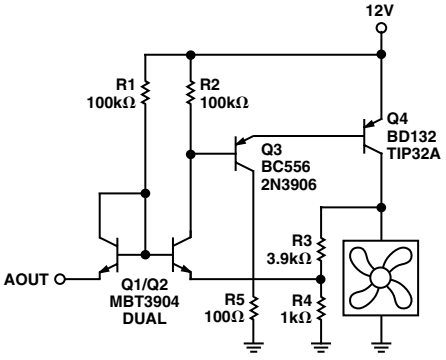


Figure 9f. Discrete Fan Drive Circuit with Bipolar Output Dual Supply

6. In all these circuits, the output transistor must have an I_{CMAX} greater than the maximum fan current, and be capable of dissipating power due to the voltage dropped across it when the fan is not operating at full speed.
7. If the fan motor produces a large back e.m.f when switched off, it may be necessary to add clamp diodes to protect the output transistors in the event that the output goes very quickly from full scale to zero.

FAULT-TOLERANT FAN CONTROL

The ADM1024 incorporates a fault-tolerant fan control capability that can override the setting of the analog output and force it to maximum to give full fan speed in the event of a critical over-temperature problem even if, for some reason, this has not been handled by the system software.

There are four temperature set points that will force the analog output to FFh if any one of them is exceeded for three or more consecutive measurements. Two of these limits are programmable by the user and two are hardware limits intended as *must not exceed* limits that cannot be changed.

The analog output will be forced to FFh if:

The temperature measured by the on-chip sensor exceeds the limit programmed into register address 13h.

or

The temperature measured by either of the remote sensors exceeds the limit programmed into address 14h.

or

The temperature measured by the on-chip sensor exceeds 70°C, which is hardware programmed into a read-only register at address 17h.

or

The temperature measured by either of the remote sensors exceeds 85°C, which is hardware programmed into a read-only register at address 18h.

Once the hardware override of the analog output is triggered, it will only return to normal operation after three consecutive measurements that are 5 degrees lower than each of the above limits.

The analog output can also be forced to FFh by pulling the $\overline{\text{THERM}}$ pin (Pin 2) low.

The limits in registers 13h and 14h can be programmed by the user. Obviously these limits should not exceed the hardware values in registers 17h and 18h, as they would have no effect. The power-on default values of these registers are the same as the two hardware registers, 70°C and 85°C respectively, so there is no need to program them if these limits are acceptable.

Once these registers have been programmed, or if the defaults are acceptable, the values in these registers can be locked by writing a 1 to Bits 1 and 2 of Configuration Register 2 (address 4Ah). This prevents any unauthorized tampering with the limits. These lock bits can only be written to 1 and can only be cleared by power-on reset or by taking the $\overline{\text{RESET}}$ pin low, so registers 13h and 14h cannot be written to again unless the device is powered off, then on.

LAYOUT AND GROUNDING

Analog inputs will provide best accuracy when referred to a clean ground. A separate, low-impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance but is not mandatory.

The power supply bypass, the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors connected between Pin 9 and ground, should also be located as close as possible to the ADM1024.

FAN INPUTS

Pins 5 and 6 may be configured as analog inputs or fan speed inputs by programming Bits 0 and 1 of the Channel Mode Register. The power-on default for these bits is all zeroes, which makes Pins 5 and 6 fan inputs.

Signal conditioning in the ADM1024 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to V_{CC}. In the event that these inputs are supplied from fan outputs that exceed 0 V to 6.5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 10a to 10d show circuits for most common fan tach outputs.

If the fan tach output has a resistive pull-up to V_{CC} it can be directly connected to the fan input, as shown in Figure 10a.

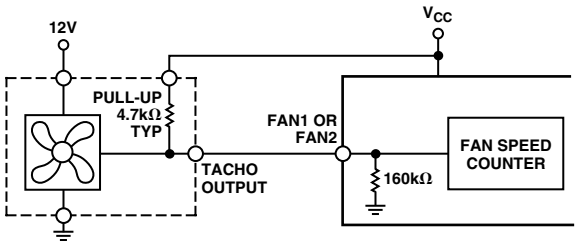


Figure 10a. Fan with Tach. Pull-Up to +V_{CC}

If the fan output has a resistive pull-up to 12 V (or other voltage greater than 6.5 V), the fan output can be clamped with a Zener diode, as shown in Figure 10b. The Zener voltage should be chosen so it is greater than V_{IH} but less than 6.5 V, allowing for the voltage tolerance of the Zener. A value of between 3 V and 5 V is suitable.

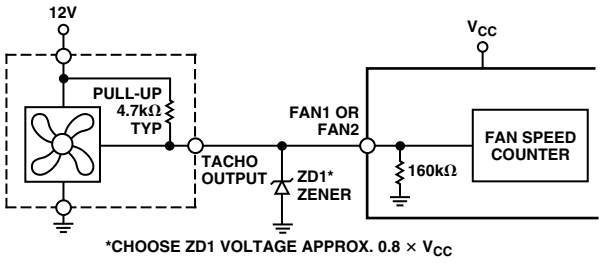


Figure 10b. Fan with Tach. Pull-Up to Voltage >6.5 V (e.g., 12 V) Clamped with Zener Diode

If the fan has a strong pull-up (less than 1 kΩ) to 12 V, or a totem-pole output, then a series resistor can be added to limit the Zener current, as shown in Figure 10c. Alternatively, a resistive attenuator may be used, as shown in Figure 10d.

R1 and R2 should be chosen such that:

$$2\ V < V_{PULL\text{-}UP} \times R2/(R_{PULL\text{-}UP} + R1 + R2) < 5\ V$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, so this should be taken into account when calculating resistor values.

With a pull-up voltage of 12 V and pull-up resistor less than 1 kΩ, suitable values for R1 and R2 would be 100 kΩ and 47 kΩ. This will give a high-input voltage of 3.83 V.

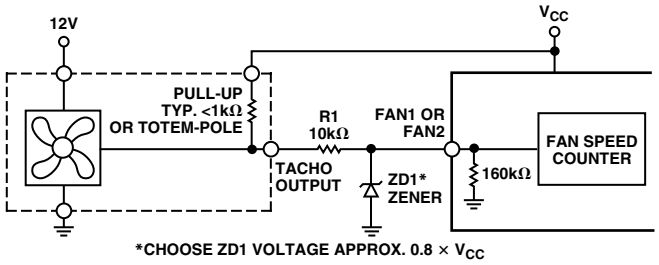


Figure 10c. Fan with Strong Tach. Pull-Up to >V_{CC} or Totem-Pole Output, Clamped with Zener and Resistor

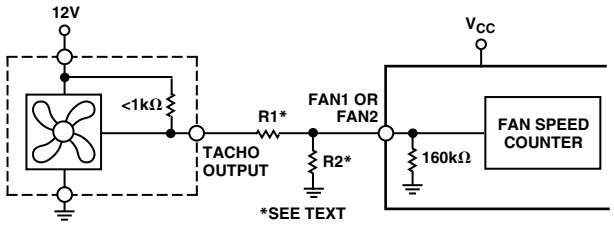


Figure 10d. Fan with Strong Tach. Pull-Up to >V_{CC} or Totem-Pole Output, Attenuated with R1/R2

FAN SPEED MEASUREMENT

The fan counter does not count the fan tach output pulses directly, because the fan speed may be less than 1000 rpm and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 22.5 kHz oscillator into the input of an 8-bit counter for two periods of the fan tach output, as shown in Figure 11; the accumulated count is actually proportional to the fan tach period and inversely proportional to the fan speed.

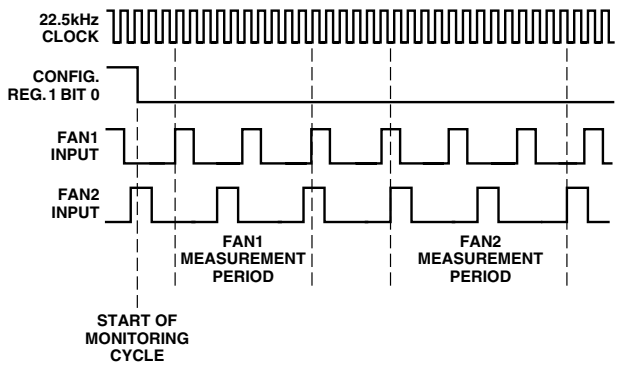


Figure 11. Fan Speed Measurement

The monitoring cycle begins when a one is written to the Start Bit (Bit 0), and a zero to the $\overline{\text{INT}}$_Clear Bit (Bit 3) of the Configuration Register. $\overline{\text{INT}}$_Enable (Bit 1) should be set to one to enable the $\overline{\text{INT}}$ output. The measurement begins on the rising edge of a fan tach pulse, and ends on the next-but-one rising edge. The fans are monitored sequentially, so if only one fan is monitored the monitoring time is the time taken after the Start Bit for it to produce two complete tach cycles or for the counter to reach full scale, whichever occurs sooner. If more than one fan is monitored, the monitoring time depends on the speed of the fans and the timing relationship of their tach pulses. This is illustrated in Figure 12. Once the fan speeds have been measured, they will be stored in the Fan Speed Value Registers and the most recent value can be read at any time. The measurements will be updated as long as the monitoring cycle continues.

To accommodate fans of different speed and/or different numbers of output pulses per revolution, a prescaler (divisor) of 1, 2, 4, or 8 may be added before the counter. The default value is 2, which gives a count of 153 for a fan running at 4400 rpm producing two output pulses per revolution.

The count is calculated by the equation:

$$Count = (22.5 \times 10^3 \times 60)\ /(rpm \times Divisor)$$

For constant speed fans, fan failure is normally considered to have occurred when the speed drops below 70% of nominal, which would correspond to a count of 219. Full scale (255) would be reached if the fan speed fell to 60% of its nominal value. For temperature-controlled variable speed fans the situation will be different.

Table V shows the relationship between fan speed and time per revolution at 60%, 70%, and 100% of nominal rpm for fan speeds of 1100, 2200, 4400, and 8800 rpm, and the divisor that would be used for each of these fans, based on two tach pulses per revolution.

Table V. Fan Speeds and Divisors

Divisor	Nominal rpm	Time per Rev (ms)	70% rpm	Time per Rev (70%) (ms)	60% rpm	Time per Rev (60%) (ms)
÷1	8800	6.82	6160	9.74	5280	11.36
÷2	4400	13.64	3080	19.48	2640	22.73
÷4	2200	27.27	1540	38.96	1320	45.44
÷8	1100	54.54	770	77.92	660	90.90

FAN1 and FAN2 Divisors are programmed into Bits 4 to 7 of the VID 0–3/Fan Divisor Register.

LIMIT VALUES

Fans in general will not overspeed if run from the correct voltage, so the failure condition of interest is underspeed due to electrical or mechanical failure. For this reason only, low-speed limits are programmed into the limit registers for the fans. It should be noted that, since fan period rather than speed is being measured, a fan failure interrupt will occur when the measurement *exceeds* the limit value.

MONITORING CYCLE TIME

The monitoring cycle time depends on the fan speed and number of tach output pulses per revolution. Two complete periods of the fan tach output (three rising edges) are required for each fan

measurement. Therefore, if the start of a fan measurement just misses a rising edge, the measurement can take almost three tach periods. In order to read a valid result from the fan value registers, the total monitoring time allowed after starting the monitoring cycle should, therefore, be three tach periods of FAN1 plus three tach periods of FAN2 at the lowest normal fan speed.

Although the fan monitoring cycle and the analog input monitoring cycle are started together, they are not synchronized in any other way.

FAN MANUFACTURERS

Manufacturers of cooling fans with tachometer outputs are listed below:

NMB Tech
9730 Independence Ave.
Chatsworth, California 91311
Phone: 818-341-3355; Fax: 818-341-8207

Model	Frame Size	Airflow CFM
2408NL	2.36 in sq. × 0.79 in (60 mm sq. × 20 mm)	9–16
2410ML	2.36 in sq. × 0.98 in (60 mm sq. × 25 mm)	14–25
3108NL	3.15 in sq. × 0.79 in (80 mm sq. × 20 mm)	25–42
3110KL	3.15 in sq. × 0.98 in (80 mm sq. × 25 mm)	25–40

Mechatronics Inc.
P.O. Box 613
Preston, WA 98050
800-453-4569
Models—Various sizes available with tach output option.

Sanyo Denki, America, Inc.
468 Amapola Avenue
Torrance, CA 90501
310-783-5400
Models—109P Series

CHASSIS INTRUSION INPUT

The Chassis Intrusion input is an active high input/open-drain output intended for detection and signalling of unauthorized tampering with the system. An external circuit powered from the system's CMOS backup battery is used to detect and latch a chassis intrusion event, whether or not the system is powered up. Once a chassis intrusion has been detected and latched, the CI input will generate an interrupt when the system is powered up.

The actual detection of chassis intrusion is performed by an external circuit that will, for example, detect when the cover has been removed. A wide variety of techniques may be used for the detection, for example:

- Microswitch that opens or closes when the cover is removed.
- Reed switch operated by magnet fixed to the cover.
- Hall-effect switch operated by magnet fixed to the cover.
- Phototransistor that detects light when cover is removed.

The chassis intrusion interrupt will remain asserted until the external detection circuit is reset. This can be achieved by setting Bit 7 of the Chassis Intrusion Clear Register to one, which will cause the CI pin to be pulled low for at least 20 ms. This register bit is self-clearing.

The chassis intrusion circuit should be designed so that it can be reset by pulling its output low. A suitable chassis intrusion circuit using a phototransistor is shown in Figure 12. Light falling on the phototransistor when the PC cover is removed will cause it to turn on and pull up the input of N1, thus setting the latch N3/N4. After the cover is replaced, a low reset on the CI output will pull down the input of N4, resetting the latch.

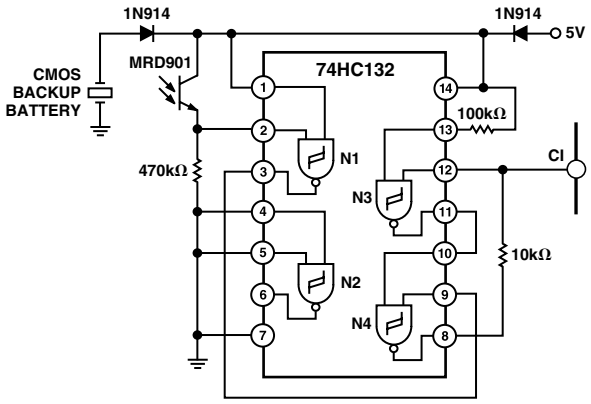


Figure 12. Chassis Intrusion Detector and Latch

The Chassis Intrusion input can also be used for other types of alarm input. Figure 13 shows a temperature alarm circuit using an AD22105 temperature switch sensor. This produces a low-going output when the preset temperature is exceeded, so the output is inverted by Q1 to make it compatible with the CI input. Q1 can by almost any small-signal NPN transistor, or a TTL or CMOS inverter gate may be used if one is available. See the AD22105 data sheet for information on selecting R_{SET}.

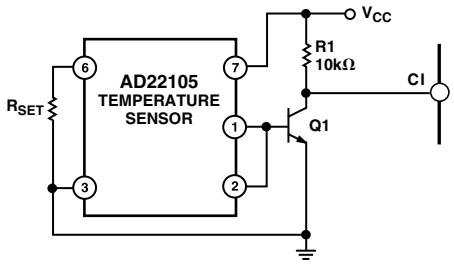


Figure 13. Using the CI Input with a Temperature Sensor

Note: The chassis intrusion input does not have a protective clamp diode to V_{CC}, as this could pull down the chassis intrusion latch and reset it when the ADM1024 was powered down.

THE ADM1024 INTERRUPT STRUCTURE

The Interrupt Structure of the ADM1024 is shown in Figure 14. As each measurement value is obtained and stored in the appropriate value register, the value and the limits from the corresponding limit registers are fed to the high and low limit comparators. The result of each comparison (1 = out of limit, 0 = in limit) is routed to the corresponding bit input of the Interrupt Status Registers via a data demultiplexer, and used to set that bit high or low as appropriate.

The Interrupt Mask Registers have bits corresponding to each of the Interrupt Status Register Bits. Setting an Interrupt Mask Bit high forces the corresponding Status Bit output low, while setting an Interrupt Mask Bit low allows the corresponding Status Bit

to be asserted. After masking, the status bits are all OR'd together to produce the $\overline{INT}$ output, which will pull low if any unmasked status bit goes high, i.e., when any measured value goes out of limit. The ADM1024 also has a dedicated output for temperature interrupts only, the $\overline{THERM}$ input/output Pin 2. The function of this is described later.

The $\overline{INT}$ output is enabled when Bit 1 of Configuration Register 1 ($\overline{INT}$_Enable) is high, and Bit 3 ($\overline{INT}$_Clear) is low.

The $\overline{INT}$ pin has an internal, 100 kΩ pull-up resistor.

VID/IRQ INPUTS

The processor voltage ID inputs VID0 to VID4 can be reconfigured as interrupt inputs by setting Bit 7 of the Channel Mode Register (address 16h). In this mode they operate as level-triggered interrupt inputs, with VID0/IRQ0 to VID2/IRQ2 being active low and VID2/IRQ2 and VID4/IRQ4 being active high. The individual interrupt inputs can be enabled or masked by setting or clearing Bits 4 to 6 of the Channel Mode Register and Bits 6 and 7 of Configuration Register 2 (address 4Ah). These interrupt inputs are not latched in the ADM1024, so they do not require clearing as do bits in the Status Registers. However, the external interrupt source should be cleared once the interrupt has been serviced, or the interrupt request will be reasserted.

INTERRUPT CLEARING

Reading an Interrupt Status Register will output the contents of the Register, then clear it. It will remain cleared until the monitoring cycle updates it, so the next read operation should not be performed on the register until this has happened, or the result will be invalid. The time taken for a complete monitoring cycle is mainly dependent on the time taken to measure the fan speeds, as described earlier.

The $\overline{INT}$ output is cleared with the $\overline{INT}$_Clear bit, which is Bit 3 of the Configuration Register, without affecting the contents of the Interrupt ($\overline{INT}$) Status Registers.

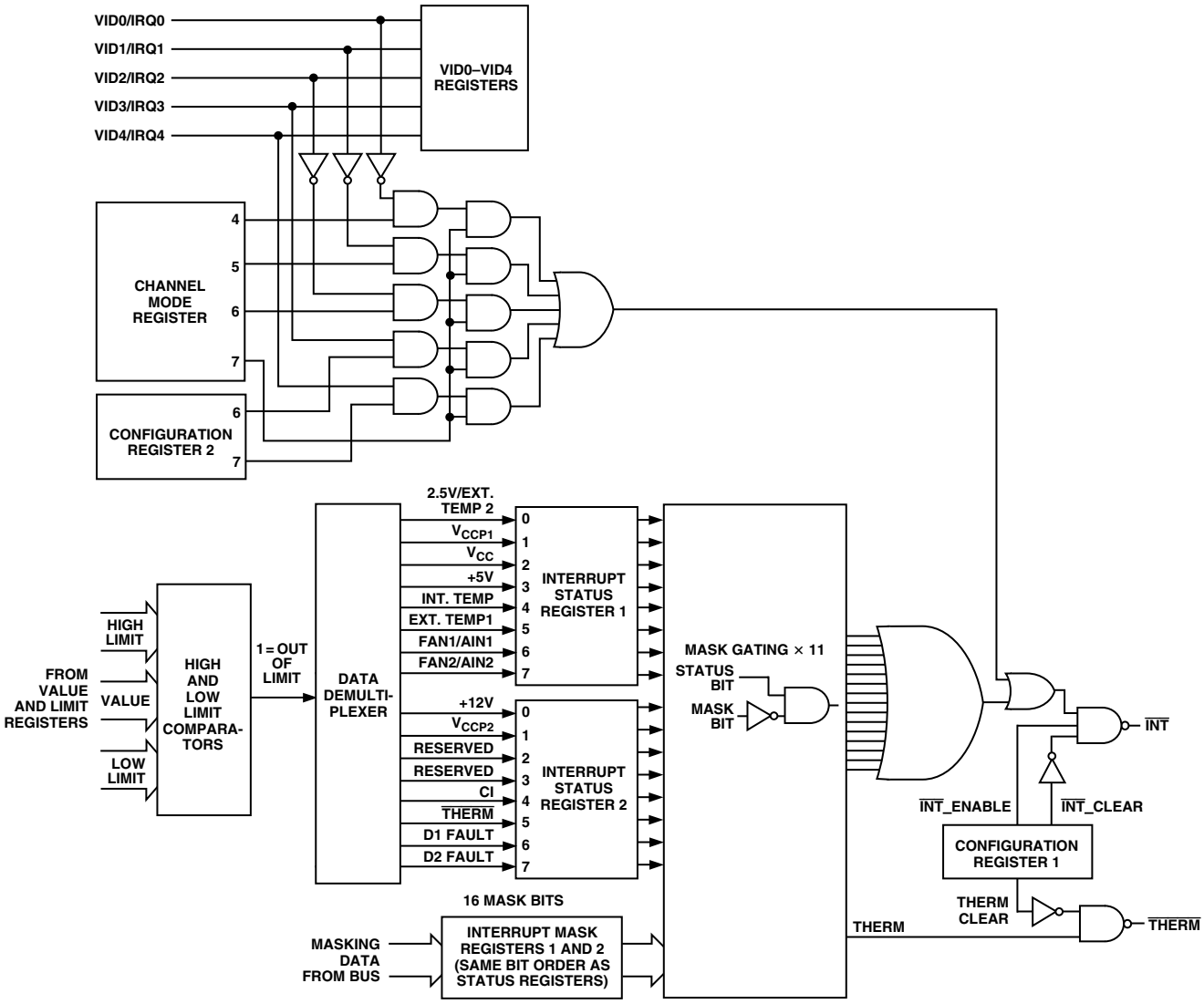


Figure 14. Interrupt Register Structure

INTERRUPT STATUS MIRROR REGISTERS

Whenever a bit in one of the Interrupt Status Registers is updated, the same bit is written to duplicate registers at addresses 4Ch and 42h. These registers allow a second management system to access the status data without worrying about clearing the data. The data in these registers is for reading only and has no effect on the interrupt output.

TEMPERATURE INTERRUPT MODES

The ADM1024 has two distinct methods of producing interrupts for out-of-limit temperature measurements from the internal or external sensors. Temperature errors can generate an interrupt on the $\overline{INT}$ pin along with other interrupts, but there is also a separate $\overline{THERM}$ pin that generates an interrupt only for temperature errors.

Operation of the $\overline{INT}$ output for temperature interrupts is illustrated in Figure 15. Assuming that the temperature starts off within the programmed limits and that temperature interrupt sources are not masked, $\overline{INT}$ will go low if the temperature measured by any of the internal or external sensors exceeds the programmed high temperature limit for that sensor, or the hardware limits in register 13h, 14h, 17h, or 18h.

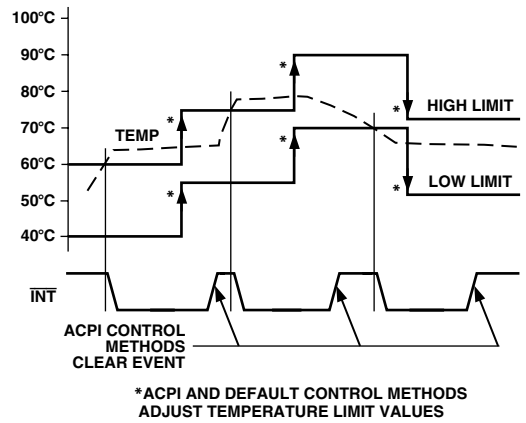


Figure 15. Operation of $\overline{INT}$ for Temperature Interrupts

Once the interrupt has been cleared, it will not be reasserted even if the temperature remains above the high limit(s). However, $\overline{INT}$ will be reasserted if:

a. the temperature falls below the low limit for the sensor

or

b. the high limit is/are reprogrammed to a new value, and the temperature then rises above the new high limit on the next monitoring cycle

or

c. the $\overline{THERM}$ pin is pulled low externally, which sets Bit 5 of Interrupt Status Register 2

or

d. An interrupt is generated by another source.

Similarly, should the temperature measured by a sensor start off within limits then fall below the low limit, $\overline{INT}$ will be asserted. Once cleared, it will not be reasserted unless:

a. the temperature rises above the high limit

or

b. the low limit is/are reprogrammed, and the temperature then falls below the new low limit

or

c. the $\overline{THERM}$ pin is pulled low externally, which sets Bit 5 of Interrupt Status Register 2

or

d. an interrupt is generated by another source.

$\overline{THERM}$ INPUT/OUTPUT

The Thermal Management Input/Output ($\overline{THERM}$) is a logic input/output with an internal, 100 kΩ pull-up resistor, that provides a separate output for temperature interrupts only. It is enabled by setting Bit 2 of Configuration Register 1. The $\overline{THERM}$ output has two operating modes that can be programmed by Bit 3 of Configuration Register 2 (address 4Ah). With this bit set to the default value of 0, the $\overline{THERM}$ output operates in "Default" interrupt mode. With this bit set to 1, the $\overline{THERM}$ output operates in "ACPI" mode.

Thermal interrupts can still be generated at the $\overline{INT}$ output while $\overline{THERM}$ is enabled, but if these are not required they can be masked by writing a 1 to bit 0 of Configuration Register 2 (address 4Ah). The $\overline{THERM}$ pin can also function as a logic input for an external sensor, for example a temperature sensor such as the ADM22105 used in Figure 16b. If $\overline{THERM}$ is taken low by an external source, the analog output will be forced to FFh to switch a controlled fan to maximum speed. This also generates an $\overline{INT}$ output as previously described.

DEFAULT MODE

In Default mode, the $\overline{THERM}$ output operates like a thermostat with hysteresis. $\overline{THERM}$ will go low and Bit 5 of Interrupt Status Register 2 will be set, if the temperature measured by any of the sensors exceeds the high limit programmed for that sensor. It will remain asserted until reset by reading Interrupt Status Register 2, by setting Bit 6 of Configuration Register 1, or when the temperature falls below the low limit programmed for that sensor.

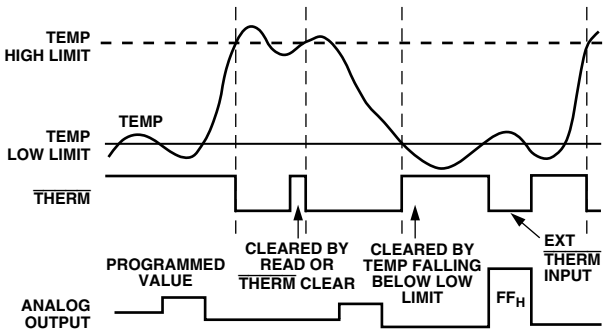


Figure 16a. $\overline{INT}$ or $\overline{THERM}$ Output in Default Mode

If $\overline{\text{THERM}}$ is cleared by reading the status register, it will be reasserted after the next temperature reading and comparison if it remains above the high limit.

If $\overline{\text{THERM}}$ is cleared by setting Bit 6 of Configuration Register 1, it cannot be reasserted until this bit is cleared.

$\overline{\text{THERM}}$ will also be asserted if one of the hardware temperature limits at addresses 13h, 14h, 17h, or 18h is exceeded for three consecutive measurements. When this happens, the analog output will be forced to FFh to boost a controlled cooling fan to full speed.

Reading Status Register 1 will not clear $\overline{\text{THERM}}$ in this case, because errors caused by exceeding the hardware temperature limits are stored in a separate register that is not cleared by reading the status register. In this case, $\overline{\text{THERM}}$ can only be cleared by setting Bit 0 of Configuration Register 2.

$\overline{\text{THERM}}$ will be cleared automatically if the temperature falls at least 5 degrees below the limit for three consecutive measurements.

ACPI MODE

In ACPI mode, $\overline{\text{THERM}}$ responds only to the hardware temperature limits at addresses 13h, 14h, 17h and 18h, not to the software programmed limits.

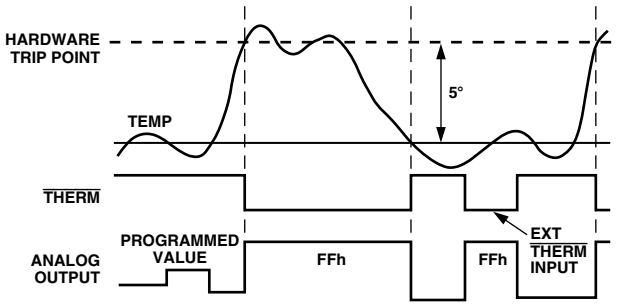


Figure 16b. $\overline{\text{THERM}}$ Output in ACPI Mode

$\overline{\text{THERM}}$ will go low if either the internal or external hardware temperature limit is exceeded for three consecutive measurements. It will remain low until the temperature falls at least 5 degrees below the limit for three consecutive measurements. While $\overline{\text{THERM}}$ is low, the analog output will go to FFh to boost a controlled fan to full speed.

$\overline{\text{RESET}}$ INPUT/OUTPUT

$\overline{\text{RESET}}$ (Pin 12) is an I/O pin that can function as an open-drain output, providing a low-going 20 ms output pulse when Bit 4 of the Configuration Register is set to 1, provided the reset function has first been enabled by setting Bit 7 of Interrupt Mask Registers #2 to 1. The bit is automatically cleared when the reset pulse is output. Pin 11 can also function as a $\overline{\text{RESET}}$ input by pulling this pin low to reset the internal registers of the ADM1024 to default values. Only those registers that have power on default values as listed in Table VI are affected by this function. The DAC register, Value and Limit Registers are not affected.

NAND TESTS

A NAND gate is provided in the ADM1024 for Automated Test Equipment (ATE) board level connectivity testing. The device is placed into NAND Test Mode by powering up with Pin 11 held high. This pin is automatically sampled after power-up and if it is connected high, then the NAND test mode is invoked.

In NAND test mode, all digital inputs may be tested as illustrated below. NTEST_OUT/ADD will become the NAND test output pin. To perform a NAND tree test all pins included in the NAND tree should first be driven high. Each pin can then be toggled and a resulting toggle can be observed on NTEST_OUT/ADD.

Allow for a typical propagation delay of 500 ns. The structure of the NAND tree is shown in Figure 17.

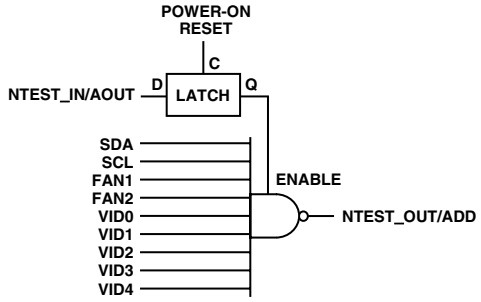


Figure 17. NAND Tree

Note that NTEST_OUT/ADD is a dual function line and if both functions are required, then this line should not be hard-wired directly to V_{CC}/GND. Instead it should be connected via a 5 kΩ resistor.

Note: If any of the inputs shown in Figure 17 are unused, they should not be connected directly to ground, but via a resistor such as 10 kΩ. This will allow the ATE (Automatic Test Equipment) to drive every input high so that the NAND tree test can be carried out properly.

USING THE ADM1024

POWER-ON RESET

When power is first applied, the ADM1024 performs a "power-on reset" on several of its registers. Registers whose power-on values are not shown have power-on conditions that are indeterminate (this includes the Value and Limit Registers). The ADC is inactive. In most applications, usually the first action after power-on would be to write limits into the Limit Registers.

Power-on reset clears or initializes the following registers (the initialized values are shown in Table VIII):

- Configuration Registers #1 and #2
- Channel Mode Register
- Interrupt ($\overline{\text{INT}}$) Status Registers #1 and #2
- Interrupt ($\overline{\text{INT}}$) Status Mirror Registers #1 and #2
- Interrupt ($\overline{\text{INT}}$) Mask Registers #1 and #2
- VID/Fan Divisor Register
- VID4 Register
- Chassis Intrusion Clear Register
- Test Register
- Analog Output Register
- Hardware Trip Registers

INITIALIZATION

Configuration Register INITIALIZATION performs a similar, but not identical, function to power-on reset. The Test Register and Analog Output Register are not initialized.

Configuration Register INITIALIZATION is accomplished by setting Bit 7 of the Configuration Register high. This bit automatically clears after being set.

USING THE CONFIGURATION REGISTERS

Control of the ADM1024 is provided through two configuration registers. The ADC is stopped upon power-up, and the $\overline{\text{INT}}$_Clear signal is asserted, clearing the $\overline{\text{INT}}$ output. The Configuration Registers are used to start and stop the ADM1024; enable or disable interrupt outputs and modes, and provide the initialization function described above.

Bit 0 of Configuration Register 1 controls the monitoring loop of the ADM1024. Setting Bit 0 low stops the monitoring loop and puts the ADM1024 into a low power mode thereby reducing power consumption. Serial bus communication is still possible with any register in the ADM1024 while in low-power mode. Setting Bit 0 high starts the monitoring loop.

Bit 1 of Configuration Register 1 enables or disables the $\overline{\text{INT}}$ Interrupt output. Setting Bit 1 high enables the $\overline{\text{INT}}$ output, setting Bit 1 low disables the output.

Bit 2 of Configuration Register 1 enables or disables the $\overline{\text{THERM}}$ output. Setting Bit 1 high enables the $\overline{\text{INT}}$ output, setting Bit 1 low disables the output.

Bit 3 of Configuration Register 1 is used to clear the $\overline{\text{INT}}$ interrupt output when set high. The ADM1024 monitoring function will stop until Bit 3 is set low. Interrupt Status register contents will not be affected.

Bit 4 of Configuration Register 1 causes a low-going 45 ms (typ) pulse at the $\overline{\text{RESET}}$ pin (Pin 12).

Bit 6 of Configuration Register 1 is used to clear an interrupt at the $\overline{\text{THERM}}$ output when it is set to 1.

Bit 7 of Configuration Register 1 is used to start a Configuration Register Initialization when it is set to 1.

Bit 0 of Configuration Register 2 is used to mask temperature interrupts at the $\overline{\text{INT}}$ output when it is set to 1. The $\overline{\text{THERM}}$ output is unaffected by this bit.

Bits 1 and 2 of Configuration Register 2 lock the values stored in the Local and Remote Fan Control Registers at addresses 13h and 14h. The values in these registers cannot be changed until a power-on reset is performed.

Bit 3 of Configuration Register 2 selects the $\overline{\text{THERM}}$ interrupt mode. The default value of 0 selects one-time mode. Setting this bit to 1 selects ACPI mode.

STARTING CONVERSION

The monitoring function (analog inputs, temperature, and fan speeds) in the ADM1024 is started by writing to Configuration Register 1 and setting Start (Bit 0), high. The $\overline{\text{INT}}$_Enable (Bit 1) should be set to 1, and $\overline{\text{INT}}$ Clear (Bit 3) set to 0 to enable interrupts. The $\overline{\text{THERM}}$ enable bit (Bit 2) should be set to 1 and the $\overline{\text{THERM}}$ Clear bit (Bit 6) should be set to 0 to enable temperature interrupts at the $\overline{\text{THERM}}$ pin. Apart from initially starting together, the analog measurements and fan speed measurements proceed independently, and are not synchronized in any way.

The time taken to complete the analog measurements depends on how they are configured, as described elsewhere. The time taken to complete the fan speed measurements depends on the fan speed and the number of tach output pulses per revolution.

Once the measurements have been completed, the results can be read from the Value Registers at any time.

REDUCED POWER AND SHUTDOWN MODE

The ADM1024 can be placed in a low-power mode by setting Bit 0 of the Configuration Register to 0. This disables the internal ADC. Full shutdown mode may then be achieved by setting Bit 0 of the Test Register to 1. This turns off the analog output and stops the monitoring cycle, if running, but it does not affect the condition of any of the registers. The device will return to its previous state when this bit is reset to zero.

APPLICATION CIRCUIT

Figure 18 shows a generic application circuit using the ADM1024. The analog monitoring inputs are connected to the power supplies including two processor core voltage inputs. The VID inputs are connected to the processor voltage ID pins. There are two tach inputs from fans, and the analog output is used to control the speed of a third fan. An opto-sensor for chassis intrusion detection is connected to the CI input. Of course, in an actual application, every input and output may not be used, in which case unused analog and digital inputs should be tied to analog or digital ground as appropriate.

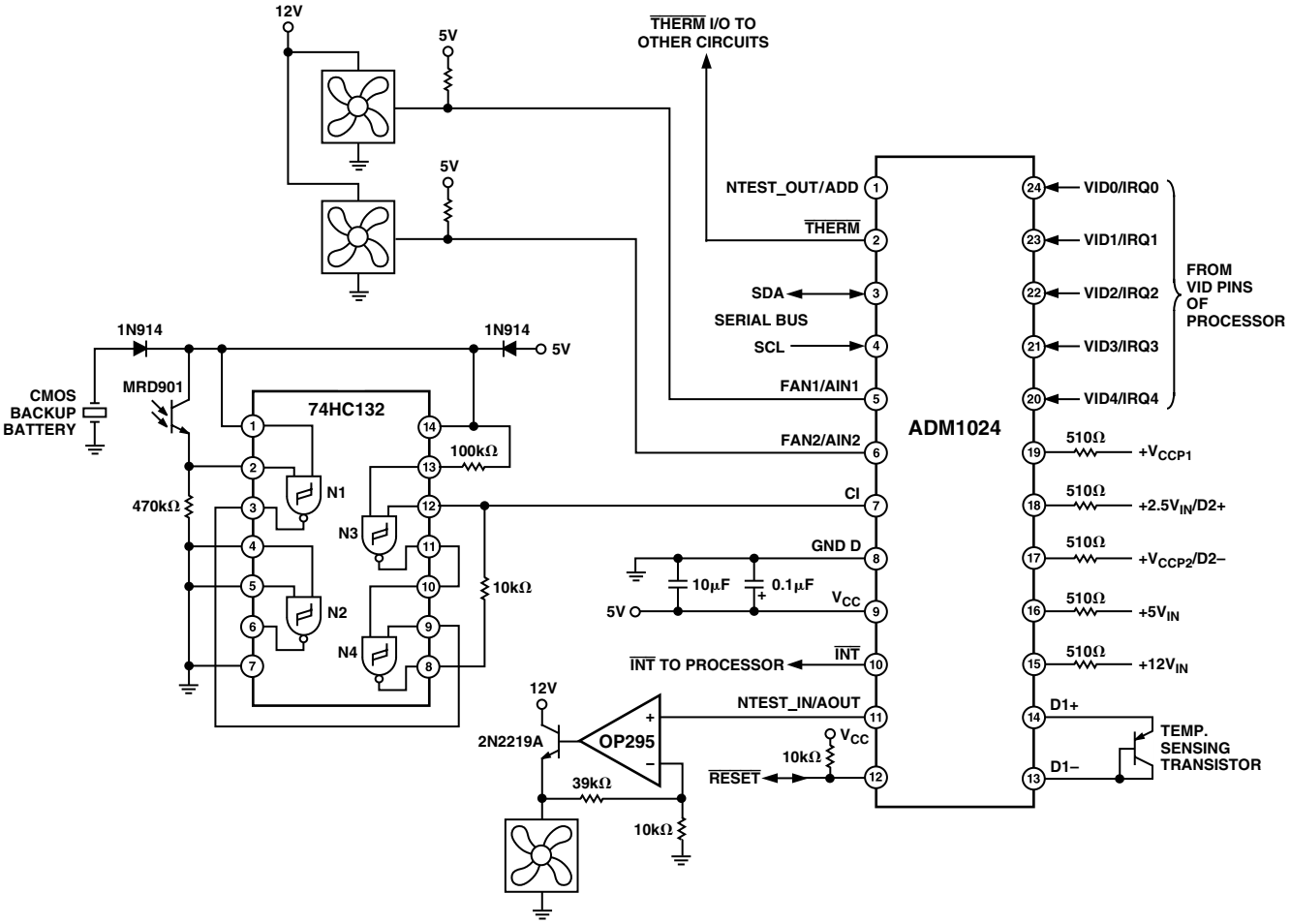


Figure 18. Application Circuit

ADM REGISTERS

Table VI. Address Pointer Register

Bit	Name	R/$\overline{W}$	Description
7–0	Address Pointer	Write	Address of ADM1024 Registers. See the tables below for detail.

Table VII. List of Registers

Hex Address	Description	Power-On Value (Binary Bit 7–0)	Notes
13h	Internal Temperature Hardware Trip Point	= 70°C	Can be written only if the write once bit in Configuration Register 2 has not been set. Values higher than 70°C will have no affect as the fixed trip point in register 16h will be reached first.
14h	External Temp Hardware Trip Point	= 85°C	Can be written only if the write once bit in Configuration Register 2 has not been set. Values higher than 85°C will have no affect as the fixed trip point in register 17h will be reached first.
15h	Test Register	0000 00X0	Setting Bit 0 of this register to 1 selects shutdown mode. Caution: Do not write to any other bits in this register.
16h	Channel Mode Register	0000 0000	This register configures the input channels and configures VID0 to VID as processor voltage ID or interrupt inputs.
17h	Internal Temperature Fixed Hardware Trip Point	= 70°C	Read Only. Cannot be changed.
18h	External Temperature Fixed Hardware Trip Point	= 85°C	Read Only. Cannot be changed.
19h	Programmed Value of Analog Output	1111 1111	
1Ah	AIN1 Low Limit	Indeterminate	
1Bh	AIN2 Low Limit	Indeterminate	
20h	2.5 V Measured Value/EXT Temp2	Indeterminate	Read Only.
21h	V_{CCP1} Measured Value	Indeterminate	Read Only.
22h	V_{CC} Measured Value	Indeterminate	Read Only.
23h	5 V Value	Indeterminate	Read Only.
24h	12 V Measured Value	Indeterminate	Read Only.
25h	V_{CCP2} Measured Value	Indeterminate	Read Only
26h	Ext. Temp1 Value	Indeterminate	Read Only. Stores the measurement from a diode sensor connected to Pins 13 and 14.
27h	Internal Temperature Value	Indeterminate	Read Only. This register is used to store eight bits of the internal temperature reading.
28h	FAN1/AIN1 Value	Indeterminate	Read Only. Stores FAN1 or AIN1 reading depending on the configuration of Pin 5.
29h	FAN2/AIN1 Value	Indeterminate	Read Only. Stores FAN2 or AIN2 reading depending on the configuration of Pin 6.
2Ah	Reserved	Indeterminate	
2Bh	2.5 V/Ext. Temp2 High Limit	Indeterminate	Stores high limit for 2.5 V input or, in temperature mode, this register stores the high limit for a diode sensor connected to Pins 17 and 18.
2Ch	2.5 V/Ext. Temp2 Low Limit	Indeterminate	Stores low limit for 2.5 V input or, in temperature mode, this register stores the low limit for a diode sensor connected to Pins 17 and 18.
2Dh	V_{CCP1} High Limit	Indeterminate	
2Eh	V_{CCP1} Low Limit	Indeterminate	
2Fh	V_{CC} High Limit	Indeterminate	
30h	V_{CC} Low Limit	Indeterminate	
31h	5 V High Limit	Indeterminate	
32h	5 V Low Limit	Indeterminate	
33h	12 V High Limit	Indeterminate	
34h	12 V Low Limit	Indeterminate	

Table VII (continued)

Hex Address	Description	Power-On Value (Binary Bit 7–0)	Notes
35h	V_{CCP2} High Limit	Indeterminate	
36h	V_{CCP2} Low Limit	Indeterminate	
37h	Ext Temp1. High Limit	Indeterminate	Stores high limit for a diode sensor connected to Pins 13 and 14.
38h	Ext Temp1. Low Limit	Indeterminate	Stores low limit for a diode sensor connected to Pins 13 and 14.
39h	Internal Temp. High Limit	Indeterminate	Stores the high limit for the internal temperature reading.
3Ah	Internal Temp. Low Limit	Indeterminate	Stores the low limit for the internal temperature reading.
3Bh	AIN1/FAN1 High Limit	Indeterminate	Stores high limit for AIN1 or FAN1, depending on the configuration of Pin 5.
3Ch	AIN2/FAN2 High Limit	Indeterminate	Stores high limit for AIN2 or FAN2, depending on the configuration of Pin 6.
3Dh	Reserved	Indeterminate	
3Eh	Company ID Number	0100 0001	This location will contain the company identification number (Read Only).
3Fh	Revision Number	0001 nnnn	Last four bits of this location will contain the revision number of the part. (Read Only)
40h	Configuration Register 1	0000 1000	See Table IX.
41h	Interrupt INT Status Register 1	0000 0000	See Table X.
42h	Interrupt INT Status Register 2	0000 0000	See Table XI.
43h	INT Mask Register 1	0000 0000	See Table XII.
44h	INT Mask Register 2	0000 0000	See Table XIII.
46h	Chassis Intrusion Clear Register	0000 0000	See Table XIV.
47h	VID 0–3/Fan Divisor Register	0101 (VID3–VID0)	See Table XV.
49h	VID4 Register	1000 000 (VID4)	See Table XVI.
4Ah	Configuration Register 2	0000 0000	See Table XVII.
4Ch	Interrupt Status Register Mirror No. 1	0000 0000	See Table XVIII.
4Dh	Interrupt Status Register Mirror No. 2	0000 0000	See Table XIX.

Table VIII. Register 16h, Channel Mode Register (Power-On Default = 00h)

Bit	Name	R/$\overline{W}$	Description
0	FAN1/AIN1	R/$\overline{W}$	Clearing this bit to 0 configures Pin 5 as FAN1 input. Setting this bit to 1 configures Pin 5 as AIN1. Power-on default = 0.
1	FAN2/AIN2	R/$\overline{W}$	Clearing this bit to 0 configures Pin 6 as FAN2 input. Setting this bit to 1 configures Pin 6 as AIN2. Power-on default = 0.
2	2.5 V, V_{CCP}/D2	R/$\overline{W}$	Clearing this bit to 0 configures Pins 17 and 18 to measure 2.5 V and V_{CCP2}. Setting this bit to 1 configures Pins 18 and 19 as an input for a second remote temperature-sensing diode. Power-on default = 0.
3	Int V_{CC}	R/$\overline{W}$	Clearing this bit to 0 sets the measurement range for the internal V_{CC} measurement to 3.3 V. Setting this bit to 1 sets the internal V_{CC} measurement range to 5 V. Power-on default = 0.
4	IRQ0 EN	R/$\overline{W}$	Setting this bit to 1 enables Pin 24 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.
5	IRQ1 EN	R/$\overline{W}$	Setting this bit to 1 enables Pin 23 as an active high interrupt input, provided have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.
6	IRQ2 EN	R/$\overline{W}$	Setting this bit to 1 enables Pin 22 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.
7	VID/IRQ	R/$\overline{W}$	Clearing this bit to 0 configures Pins 20 to 24 as processor voltage ID inputs. Setting this bit to 1 configures Pins 20 to 24 as interrupt inputs. Power-on default = 0.

Table IX. Register 40h, Configuration Register 1 (Power-On Default = 08h)

Bit	Name	R/$\overline{W}$	Description
0	START	R/$\overline{W}$	Logic 1 enables start-up of ADM1024, logic 0 places it in standby mode. Caution: The outputs of the interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred (see "$\overline{INT}$ Clear" bit). At start-up, limit checking functions and scanning begins. Note, all high and low limits should be set into the ADM1024 prior to turning on this bit. (Power-Up Default = 0)
1	$\overline{INT}$_Enable	R/$\overline{W}$	Logic 1 enables the $\overline{INT}$_output. 1 = Enabled 0 = Disabled (Power-Up Default = 0).
2	$\overline{THERM}$ Enable	R/$\overline{W}$	0 = $\overline{THERM}$ disabled. 1 = $\overline{THERM}$ enabled.
3	$\overline{INT}$_Clear	R/$\overline{W}$	During Interrupt Service Routine (ISR) this bit is asserted Logic 1 to clear INT output without affecting the contents of the Interrupt Status Register. The device will stop monitoring. It will resume upon clearing of this bit. (Power-Up Default = 0)
4	$\overline{RESET}$	R/$\overline{W}$	Setting this bit generates a low-going 45 ms reset pulse at Pin 12. This bit is self-clearing and power-up default is 0.
5	Reserved	R/$\overline{W}$	Default = 0.
6	$\overline{THERM}$ CLR	R/$\overline{W}$	A one clears the $\overline{THERM}$ output without changing the Status Register contents.
7	Initialization	R/$\overline{W}$	Logic 1 restores Power-Up default values to the Configuration register, Interrupt status registers, Interrupt Mask Registers, Fan Divisor Register, and the Temperature Configuration Register. This bit automatically clears itself since the power-on default is zero.

Table X. Register 41h, Interrupt Status Register 1 (Power-On Default = 00h)

Bit	Name	R/$\overline{W}$	Description
0	2.5 V/External Temp2 Error	Read Only	A one indicates that a High or Low limit has been exceeded.
1	V_{CCP1} Error	Read Only	A one indicates that a High or Low limit has been exceeded.
2	V_{CC} Error	Read Only	A one indicates that a High or Low limit has been exceeded.
3	5 V Error	Read Only	A one indicates that a High or Low limit has been exceeded.
4	Internal Temp Error	Read Only	A one indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
5	External Temp1 Error	Read Only	A one indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
6	FAN1/AIN1 Error	Read Only	A one indicates that a High or Low limit has been exceeded.
7	FAN2/AIN2 Error	Read Only	A one indicates that a High or Low limit has been exceeded.

Table XI. Register 42h, Interrupt Status Register 2 (Power-On Default = 00h)

Bit	Name	R/$\overline{W}$	Description
0	12 V Error	Read Only	A one indicates a High or Low limit has been exceeded.
1	V_{CCP2} Error	Read Only	A one indicates a High or Low limit has been exceeded.
2	Reserved	Read Only	Undefined.
3	Reserved	Read Only	Undefined.
4	Chassis Error	Read Only	A one indicates Chassis Intrusion has gone high.
5	$\overline{THERM}$ Interrupt	Read Only	Indicates that $\overline{THERM}$ pin has been pulled low by an external source.
6	D1 Fault	Read Only	Short or open-circuit sensor diode D1.
7	D2 Fault	Read Only	Short or open-circuit sensor diode D2.

NOTES
1. Any time the STATUS Register is read out, the conditions (i.e., Register) that are read are automatically reset. In the case of the channel priority indication, if two or more channels were out of limits, then another indication would automatically be generated if it was not handled during the ISR.
2. In the Mask Register, the errant voltage interrupt may be disabled, until the operator has time to clear the errant condition or set the limit higher/lower.

Table XII. Register 43h, $\overline{\text{INT}}$ Interrupt Mask Register 1 (Power-On Default = 00h)

Bit	Name	R/$\overline{\text{W}}$	Description
0	2.5 V/Ext. Temp2	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
1	V_{CCP1}	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
2	V_{CC}	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
3	5 V	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
4	Int. Temp	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
5	Ext. Temp1	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
6	FAN1/AIN1	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
7	FAN2/AIN2	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.

Table XIII. Register 44h, $\overline{\text{INT}}$ Mask Register 2 (Power-On Default = 00h)

Bit	Name	R/$\overline{\text{W}}$	Description
0	12 V	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
1	V_{CCP2}	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
2	Reserved	Read/$\overline{\text{Write}}$	Power-up default set to Low.
3	Reserved	Read/$\overline{\text{Write}}$	Power-up default set to Low.
4	CI	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
5	$\overline{\text{THERM}}$ (Input)	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
6	D1 Fault	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
7	D2 Fault	Read/$\overline{\text{Write}}$	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.

Table XIV. Register 46h, Chassis Intrusion Clear (Power-On Default = 00h)

Bit	Name	R/$\overline{\text{W}}$	Description
0–6	Reserved	Read Only	Undefined, always reads as 00h.
7	Chassis Int. Clear	Read/$\overline{\text{Write}}$	A one outputs a minimum 20 ms active low pulse on the Chassis Intrusion pin. The register bit clears itself after the pulse has been output.

Table XV. Register 47h, VID0–3/FAN Divisor Register (Power-On Default 0101(VID3–0))

Bit	Name	R/$\overline{\text{W}}$	Description
0–3	VID	Read	The VID[3:0] inputs from processor core power supplies to indicate the operating voltage (e.g., 1.3 V to 3.5 V)
4–5	FAN1 Divisor	Read/$\overline{\text{Write}}$	Sets counter prescaler for FAN1 speed measurement <5:4> = 00 – divide by 1 <5:4> = 01 – divide by 2 <5:4> = 10 – divide by 4 <5:4> = 11 – divide by 8.
6–7	FAN2 Divisor	Read/$\overline{\text{Write}}$	Sets counter prescaler for FAN2 speed measurement <7:6> = 00 – divide by 1 <7:6> = 01 – divide by 2 <7:6> = 10 – divide by 4 <7:6> = 11 – divide by 8.

Table XVI. Register 49h, VID4/Device ID Register (Power-On Default 1000000(VID4))

Bit	Name	R/$\overline{\text{W}}$	Description
0	VID4	Read Only	VID4 Input from Pentium.
1–7	Reserved	Read Only	Undefined, always reads as 1000 000(VID4).

Table XVII. Register 4AH, Configuration Register 2 (Power-On Default [7:0] = 0x00h)

Bit	Name	R/$\overline{W}$	Description
0	Thermal $\overline{INT}$ Mask	Read/$\overline{Write}$	Setting this bit masks the thermal interrupts for the $\overline{INT}$ output ONLY. The $\overline{THERM}$ output will still be generated, regardless of the setting of this bit.
1	Ambient Temp Fan Control Register Write Once Bit	Read/$\overline{Write}$ Once	Writing a one to this bit will lock in the values set into the ambient temperature automatic fan control register 13h. This register will not be able to be written again until a reset is performed (either POR, Hard or Soft Reset).
2	Remote Temp Fan Control Register Write Once Bit	Read/$\overline{Write}$ Once	Writing a one to this bit will lock in the values set into the remote temperature automatic fan control register 14h. This register will not be able to be written again until a reset is performed (either POR, Hard or Soft Reset).
3	$\overline{THERM}$ Interrupt Mode	Read/$\overline{Write}$	If this bit is 0 the $\overline{THERM}$ output operates in default mode. If this bit is 1, the $\overline{THERM}$ output operates in ACPI mode.
4, 5	Reserved	Read Only	Reserved.
6	IRQ3 EN	Read/$\overline{Write}$	Setting this bit to 1 enables Pin 21 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.
7	IRQ4 EN	Read/$\overline{Write}$	Setting this bit to 1 enables Pin 20 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.

Table XVIII. Register 4Ch, Interrupt Status Register 1 Mirror (Power-On Default <7:0> = 00h)

Bit	Name	R/$\overline{W}$	Description
0	2.5 V/Ext. Temp2 Error	Read Only	A one indicates that a High or Low limit has been exceeded.
1	V_{CCP1} Error	Read Only	A one indicates that a High or Low limit has been exceeded.
2	V_{CC} Error	Read Only	A one indicates that a High or Low limit has been exceeded.
3	5 V Error	Read Only	A one indicates that a High or Low limit has been exceeded.
4	Internal Temp Error	Read Only	A one indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
5	External Temp1 Error	Read Only	A one indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
6	FAN1/AIN1 Error	Read Only	A one indicates that a High or Low limit has been exceeded.
7	FAN2/AIN2 Error	Read Only	A one indicates that a High or Low limit has been exceeded.

Table XIX. Register 4DH, Interrupt Status Register 2 Mirror (Power-On Default <7:0> = 00h)

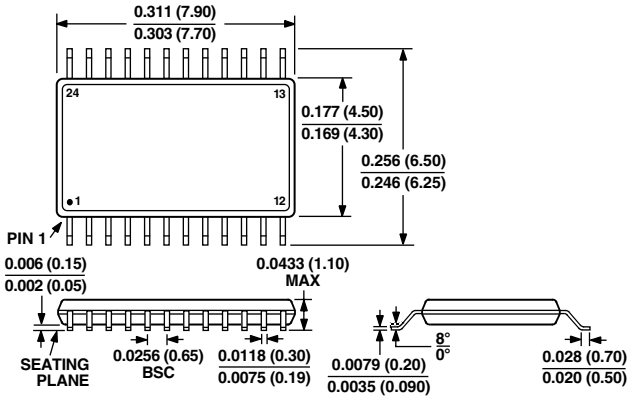
Bit	Name	R/$\overline{W}$	Description
0	12 V Error	Read Only	A one indicates a High or Low limit has been exceeded.
1	V_{CCP2} Error	Read Only	A one indicates a High or Low limit has been exceeded.
2	Reserved	Read Only	Undefined.
3	Reserved	Read Only	Undefined.
4	Chassis Error	Read Only	A one indicates Chassis Intrusion has gone high.
5	$\overline{THERM}$ Interrupt	Read Only	Indicates that $\overline{THERM}$ pin has been pulled low by an external source.
6	D1 Fault	Read Only	Short or open-circuit sensor diode D1.
7	D2 Fault	Read Only	Short or open-circuit sensor diode D2.

NOTE
An error that causes continuous interrupts to be generated may be masked in its respective mask register, until the error can be alleviated.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead TSSOP Package
(RU-24)



C00059–0–2/01 (rev. A)

ADM1024–Revision History

Location	Page
Data sheet changed from REV. 0 to REV A.	
Changes to Power Supply and Analog-to-Digital Converter sections of SPECIFICATIONS	2

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Appendix C: Analog Devices AD9432

C.1 Introduction

The following pages are a reprint of the Analog Devices AD9432 12–Bit, 100 MHz A/D Converter data sheet.

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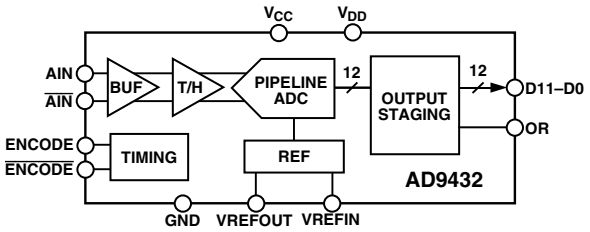
12-Bit, 80 MSPS/105 MSPS A/D Converter

AD9432

FEATURES
On-Chip Reference and Track/Hold
On-Chip Input Buffer
850 mW Typical Power Dissipation at 105 MSPS
500 MHz Analog Bandwidth
SNR = 67 dB @ 49 MHz AIN at 105 MSPS
SFDR = 80 dB @ 49 MHz AIN at 105 MSPS
2.0 V p-p Differential Analog Input Range
Single 5.0 V Supply Operation
3.3 V CMOS/TTL Outputs
Two's Complement Output Format

APPLICATIONS
Communications
Basestations and 'Zero-IF' Subsystems
Wireless Local Loop (WLL)
Local Multipoint Distribution Service (LMDS)
HDTV Broadcast Cameras and Film Scanners

FUNCTIONAL BLOCK DIAGRAM



GENERAL INTRODUCTION

The AD9432 is a 12-bit monolithic sampling analog-to-digital converter with an on-chip track-and-hold circuit and is optimized for high-speed conversion and ease of use. The product operates at a 105 MSPS conversion rate with outstanding dynamic performance over its full operating range.

The ADC requires only a single 5.0 V power supply and a 105 MHz encode clock for full-performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3 V logic. The encode input supports either differential or single-ended and is TTL/CMOS-compatible.

Fabricated on an advanced BiCMOS process, the AD9432 is available in a 52-lead plastic quad flatpack package (LQFP) specified over the industrial temperature range (–40°C to +85°C).

REV. E

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AD9432–SPECIFICATIONS

(V_{DD} = 3.3 V, V_{CC} = 5.0 V; external reference; differential encode input, unless otherwise noted.)

Parameter	Temp	Test Level	AD9432BST/BSQ-80 Min	Typ	Max	AD9432BST/BSQ-105 Min	Typ	Max	Unit
RESOLUTION				12			12		Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I	–0.75	±0.25	+0.75	–0.75	±0.25	+0.75	LSB
	Full	VI	–1.0	±0.5	+1.0	–1.0	±0.5	+1.0	LSB
Integral Nonlinearity	25°C	I	–1.0	±0.5	+1.0	–1.0	±0.5	+1.0	LSB
	Full	VI	–1.5	±1.0	+1.5	–1.5	±1.0	+1.5	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Gain Error[1]	25°C	I	–5	+2	+7	–5	+2	+7	% FS
Gain Tempco[1]	Full	V		150			150		ppm/°C
ANALOG INPUT									
Input Voltage Range (AIN–$\overline{AIN}$)	Full	V		±1.0			±1.0		V
Common-Mode Voltage	Full	V		3.0			3.0		V
Input Offset Voltage	Full	VI	–5	±0	+5	–5	±0	+5	mV
Input Resistance	Full	VI	2	3	4	2	3	4	kΩ
Input Capacitance	25°C	V		4			4		pF
Analog Bandwidth, Full Power	25°C	V		500			500		MHz
ANALOG REFERENCE									
Output Voltage	Full	VI	2.4	2.5	2.6	2.4	2.5	2.6	V
Tempco	Full	V		50			50		ppm/°C
Input Bias Current	Full	VI		15	50		15	50	µA
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	80			105			MSPS
Minimum Conversion Rate	Full	IV			1			1	MSPS
Encode Pulsewidth High (t_{EH})	25°C	IV	4.0	6.2		4.0	4.8		ns
Encode Pulsewidth Low (t_{EL})	25°C	IV	4.0	6.2		4.0	4.8		ns
Aperture Delay (t_A)	25°C	V		2.0			2.0		ns
Aperture Uncertainty (Jitter)	25°C	V		0.25			0.25		ps rms
Output Valid Time (t_V)[2]	Full	VI	3.0	5.3		3.0	5.3		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		5.5	8.0		5.5	8.0	ns
Output Rise Time (t_R)[2]	Full	V		2.1			2.1		ns
Output Fall Time (t_F)	Full	V		1.9			1.9		ns
Out-of-Range Recovery Time	25°C	V		2			2		ns
Transient Response Time	25°C	V		2			2		ns
Latency	Full	IV		10			10		Cycles
DIGITAL INPUTS									
Encode Input Common Mode	Full	V		1.6			1.6		V
Differential Input (ENC–$\overline{ENC}$)	Full	V		750			750		mV
Single-Ended									
Logic "1" Voltage	Full	IV	2.0			2.0			V
Logic "0" Voltage	Full	IV			0.8			0.8	V
Input Resistance	Full	VI	3	5	8	3	5	8	kΩ
Input Capacitance	25°C	V		4.5			4.5		pF
DIGITAL OUTPUTS									
Logic "1" Voltage (V_{DD} = 3.3 V)	Full	VI	V_{DD} – 0.05			V_{DD} – 0.05			V
Logic "0" Voltage (V_{DD} = 3.3 V)	Full	VI			0.05			0.05	V
Output Coding				Two's Complement			Two's Complement		
POWER SUPPLY									
Power Dissipation[3]	Full	VI		790	1000		850	1100	mW
Power Supply Rejection Ratio (PSRR)	25°C	I	–5	+0.5	+5	–5	+0.5	+5	mV/V
I_{VCC}	Full	VI		158	200		170	220	mA
I_{VDD}	Full	VI		9.5	12.2		12.5	16	mA

Parameter	Temp	Test Level	AD9432BST/BSQ-80 Min	AD9432BST/BSQ-80 Typ	AD9432BST/BSQ-80 Max	AD9432BST/BSQ-105 Min	AD9432BST/BSQ-105 Typ	AD9432BST/BSQ-105 Max	Unit
DYNAMIC PERFORMANCE[4]									
Signal-to-Noise Ratio (SNR)									
(Without Harmonics)									
f_{IN} = 10.3 MHz	25°C	I	65.5	67.5		65.5	67.5		dB
f_{IN} = 40 MHz	25°C	I	65	67.2			67.2		dB
f_{IN} = 49 MHz	25°C	I		67.0		64	67.0		dB
f_{IN} = 70 MHz	25°C	V		66.1			66.1		dB
Signal-to-Noise Ratio (SINAD)									
(With Harmonics)									
f_{IN} = 10.3 MHz	25°C	I	65	67.2		65	67.2		dB
f_{IN} = 40 MHz	25°C	I	64.5	66.9			66.9		dB
f_{IN} = 49 MHz	25°C	I		66.7		63	66.7		dB
f_{IN} = 70 MHz	25°C	V		65.8			65.8		dB
Effective Number of Bits									
f_{IN} = 10 MHz	25°C	V		11.0			11.0		Bits
f_{IN} = 40 MHz	25°C	V		10.9			10.9		Bits
f_{IN} = 49 MHz	25°C	V		10.9			10.9		Bits
f_{IN} = 70 MHz	25°C	V		10.7			10.7		Bits
Second and Third Harmonic Distortion									
f_{IN} = 10 MHz	25°C	I	–75	–85		–75	–85		dBc
f_{IN} = 40 MHz	25°C	I	–73	–85			–83		dBc
f_{IN} = 49 MHz	25°C	I		–83		–72	–80		dBc
f_{IN} = 70 MHz	25°C	V		–80			–78		dBc
Worst Harmonic or Spur									
(Excluding Second and Third)									
f_{IN} = 10 MHz	25°C	I	–80	–90		–80	–90		dBc
f_{IN} = 40 MHz	25°C	I	–80	–90			–90		dBc
f_{IN} = 49 MHz	25°C	I		–90		–80	–90		dBc
f_{IN} = 70 MHz	25°C	V		–90			–90		dBc
Two-Tone Intermod Distortion (IMD)									
f_{IN1} = 29.3 MHz; f_{IN2} = 30.3 MHz	25°C	V		–75			–75		dBc
f_{IN1} = 70.3 MHz; f_{IN2} = 71.3 MHz	25°C	V		–66			–66		dBc

NOTES

[1]Gain error and gain temperature coefficients are based on the ADC only (with a fixed 2.5 V external reference and a 2 V p-p differential analog input).

[2]t_V and t_{PD} are measured from the transition points of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 µA. Rise and fall times measured from 10% to 90%.

[3]Power dissipation measured with encode at rated speed and a dc analog input. (Outputs Static, I_{VDD} = 0.)

[4]SNR/harmonics based on an analog input voltage of –0.5 dBFS referenced to a 2 V full-scale input range.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} . . . . . 6 V
V_{CC} . . . . . 6 V
Analog Inputs . . . . . –0.5 V to V_{CC} + 0.5 V
Digital Inputs . . . . . –0.5 V to V_{DD} + 0.5 V
VREFIN . . . . . –0.5 V to V_{CC} + 0.5 V
Digital Output Current . . . . . 20 mA
Operating Temperature . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Case Temperature . . . . . 150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.

THERMAL CHARACTERISTICS

52-Lead Plastic LQFP (ST-52)
θ_{JA} = 50°C/W, No Airflow

52-lead PowerQuad® 4 LQFP (SQ-52)
θ_{JA} = 25°C/W, Soldered Exposed Heat Sink, No Airflow
θ_{JA} = 33°C/W, Unsoldered Exposed Heat Sink, No Airflow
θ_{JC} = 2°C/W, Bottom of package (Exposed Heat Sink)

Simulated Typical performance for 4-layer JEDEC board, horizontal orientation.

ORDERING GUIDE

Model	Temperature Ranges	Package Descriptions	Package Option
AD9432BSQ -80, -105	–40°C to +85°C	52-Lead Thermally Enhanced Plastic Quad Flatpack	SQ-52
AD9432BST -80, -105	–40°C to +85°C	52-Lead Plastic Quad Flatpack (LQFP)	ST-52
AD9432/PCB	25°C	Evaluation Board	

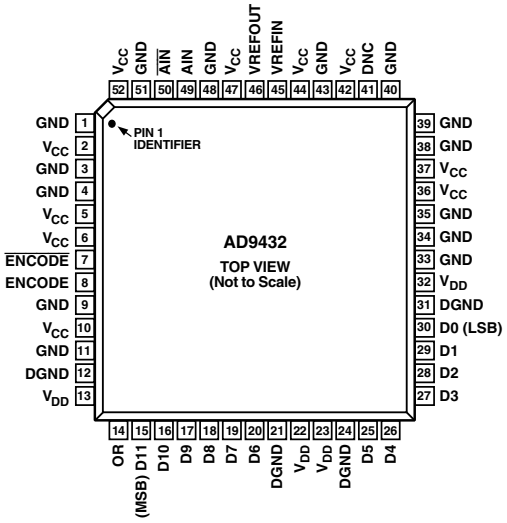
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9432 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PowerQuad is a registered trademark of AMkor Technology, Inc.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Number (AD9432BST)	Mnemonic	Function
1, 3, 4, 9, 11, 33, 34, 35, 38, 39, 40, 43, 48, 51	GND	Analog Ground
2, 5, 6, 10, 36, 37, 42, 44, 47, 52	V_{CC}	Analog Supply (5 V)
7	$\overline{\text{ENCODE}}$	Encode Clock for ADC–Complementary
8	ENCODE	Encode Clock for ADC–True (ADC samples on rising edge of ENCODE)
14	OR	Out of Range Output
15–20, 25–30	D11–D6, D5–D0	Digital Output
12, 21, 24, 31	DGND	Digital Output Ground
13, 22, 23, 32	V_{DD}	Digital Output Power Supply (2.7 V to 3.6 V)
41	DNC	Do Not Connect
45	VREFIN	Reference Input for ADC (2.5 V Typical); Bypass with 0.1 μF to Ground.
46	VREFOUT	Internal Reference Output (2.5 V Typical)
49	AIN	Analog Input–True
50	$\overline{\text{AIN}}$	Analog Input–Complementary

DEFINITION OF SPECIFICATIONS

Analog Bandwidth (Small Signal)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic "1" state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable Encode duty cycle.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise Plus Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Harmonic
The ratio of the rms signal amplitude to the rms value of the worst harmonic component, reported in dBc.

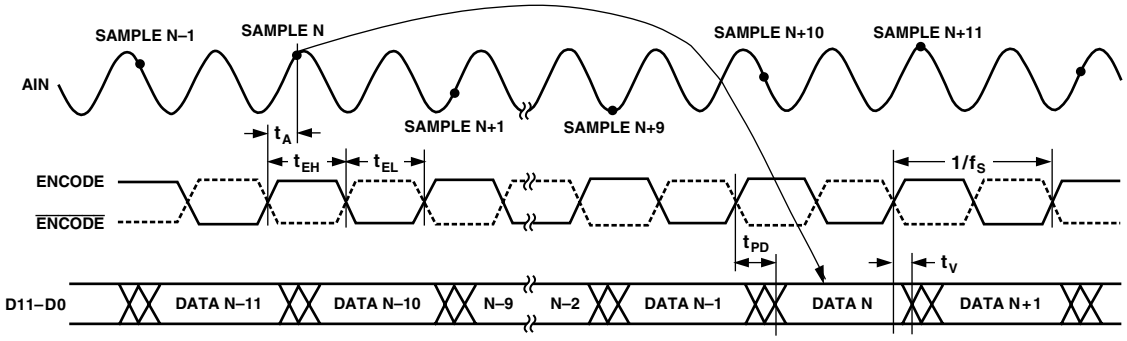


Figure 1. Timing Diagram

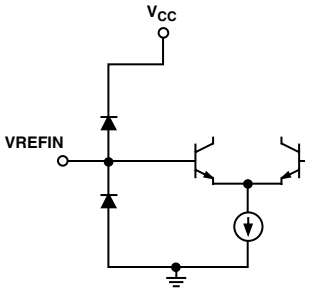


Figure 2. Equivalent Voltage Reference Input Circuit

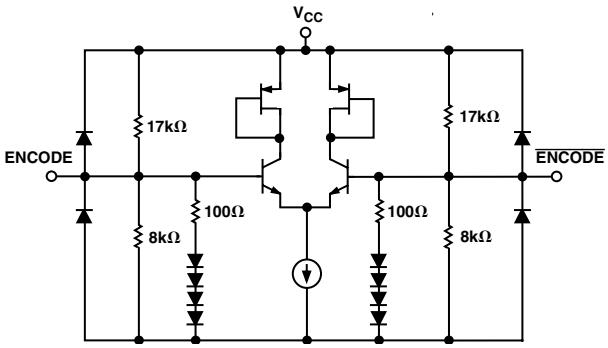


Figure 4. Equivalent Encode Input Circuit

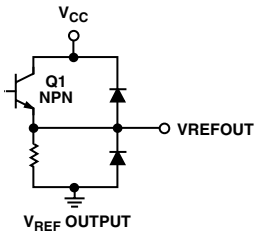


Figure 3. Equivalent Voltage Reference Output Circuit

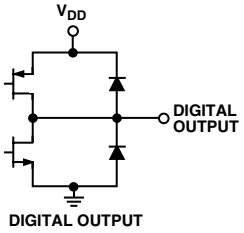


Figure 5. Equivalent Digital Output Circuit

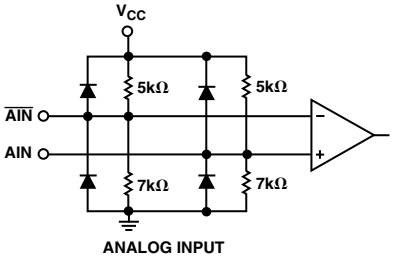
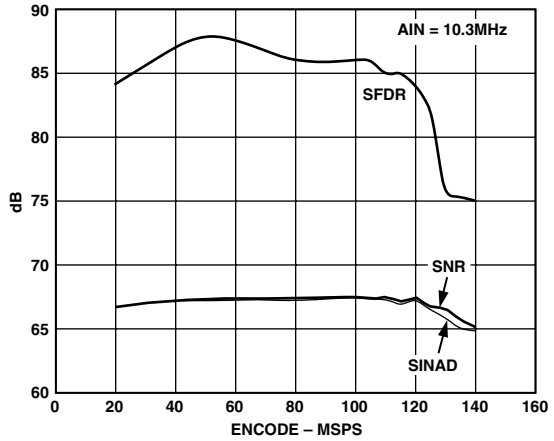
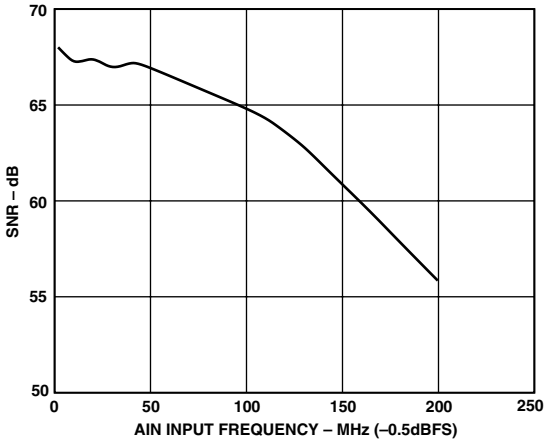


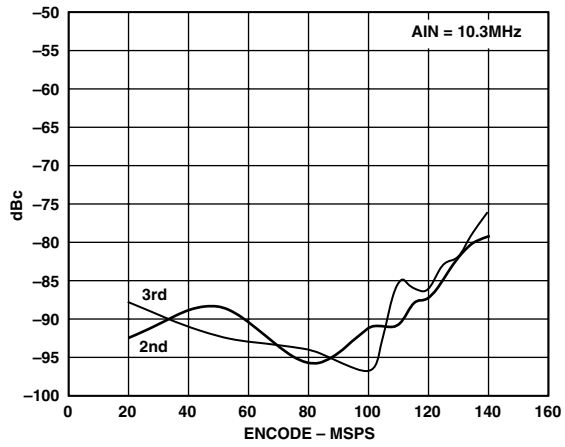
Figure 6. Equivalent Analog Input Circuit



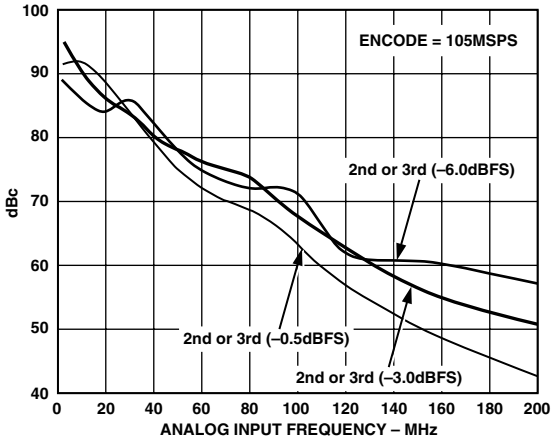
TPC 1. SNR/SINAD/SFDR vs. f_S: f_{IN} = 10.3 MHz



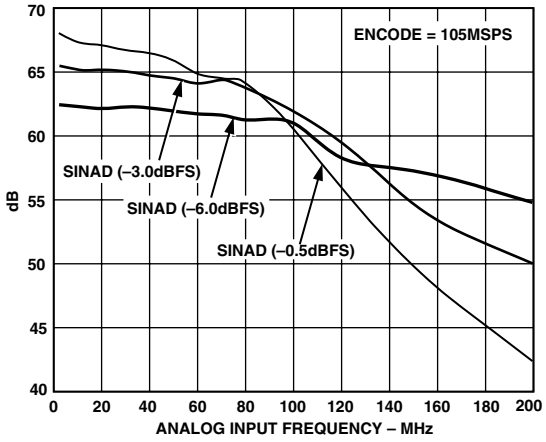
TPC 4. SNR vs. AIN Input Frequency, Encode = 105 MSPS



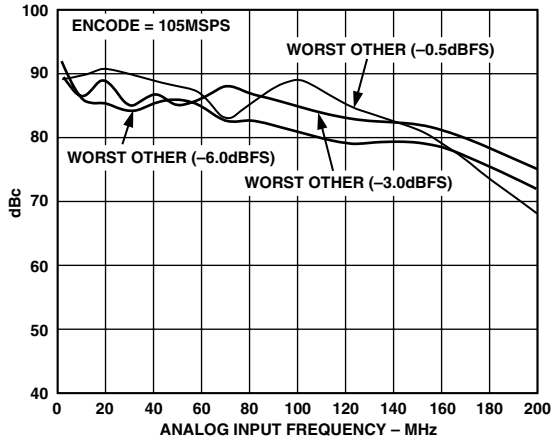
TPC 2. Harmonics vs. f_S: f_{IN} = 10.3 MHz



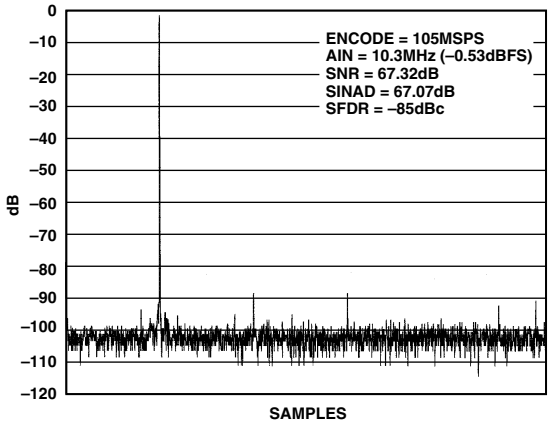
TPC 5. Harmonics vs. f_{IN}: f_S = 105 MSPS



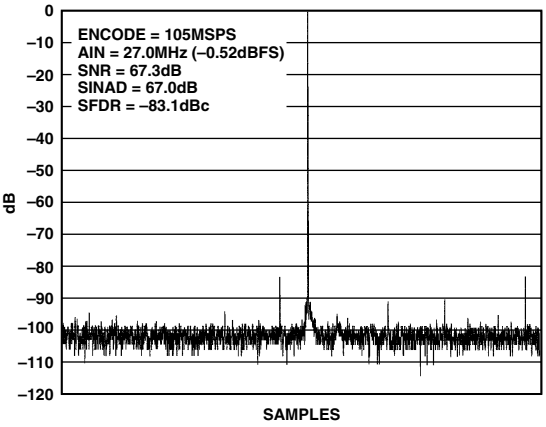
TPC 3. SINAD vs. f_{IN}: f_S = 105 MSPS



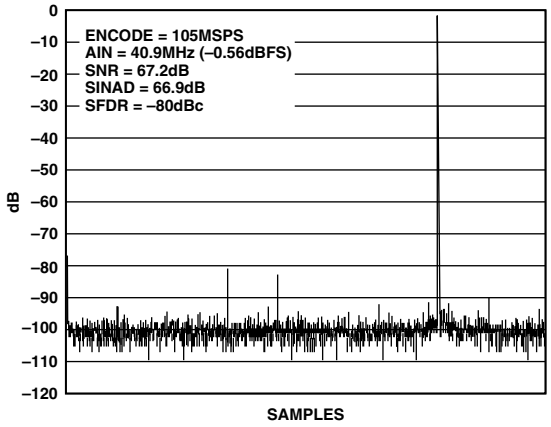
TPC 6. Worst-Case Spur (Other than Second and Third) vs. f_{IN}: f_S = 105 MSPS



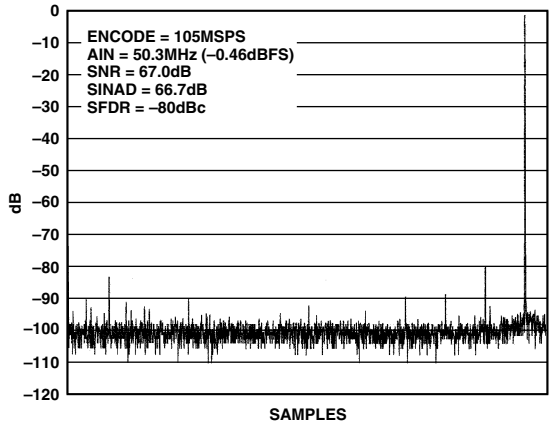
TPC 7. Spectrum: f_S = 105 MSPS, f_{IN} = 10.3 MHz



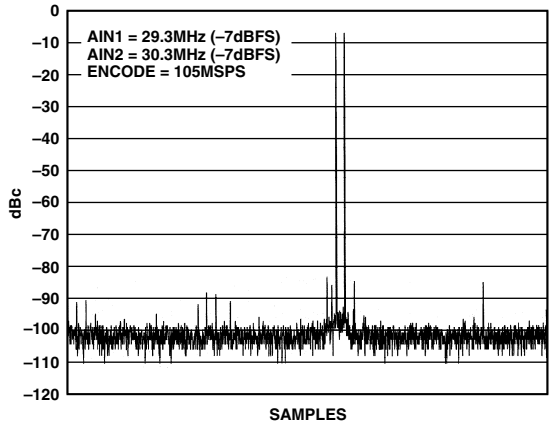
TPC 8. Spectrum: f_S = 105 MSPS, f_{IN} = 27 MHz



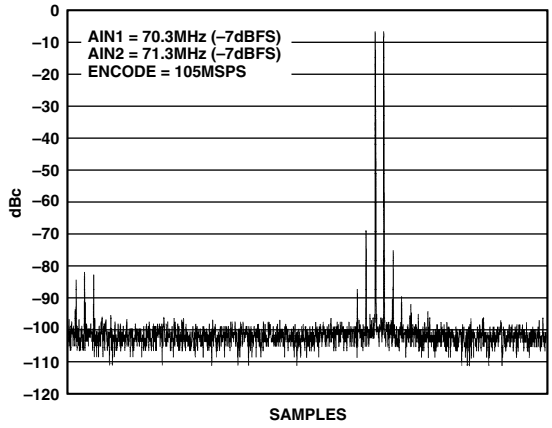
TPC 9. Spectrum: f_S = 105 MSPS, f_{IN} = 40.9 MHz



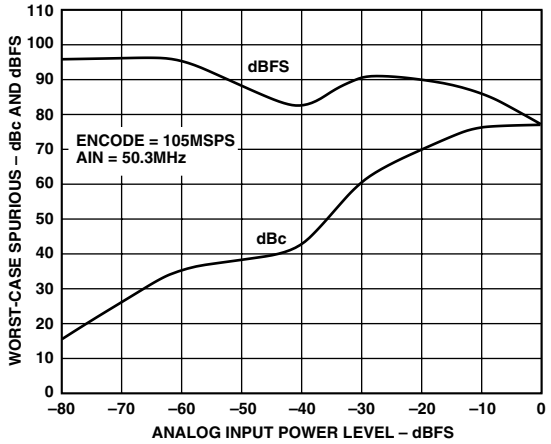
TPC 10. Spectrum: f_S = 105 MSPS, f_{IN} = 50.3 MHz



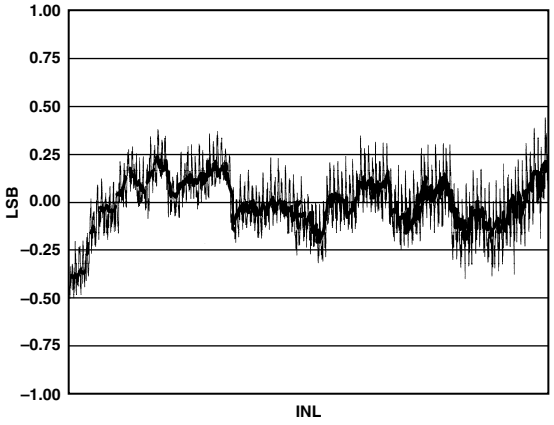
TPC 11. Two-Tone Spectrum, Wideband: f_S = 105 MSPS, AIN1 = 29.3 MHz, AIN2 = 30.3 MHz



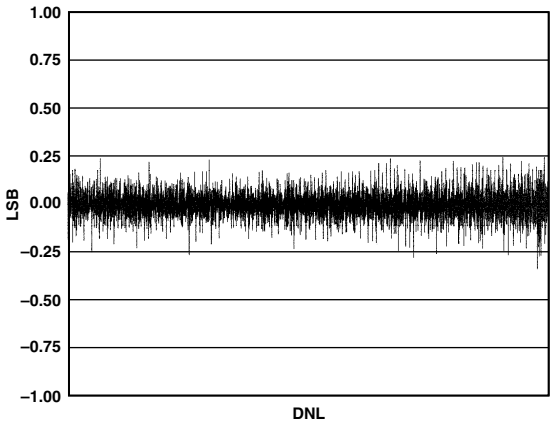
TPC 12. Two-Tone Spectrum, Wideband: f_S = 105 MSPS, AIN1 = 70.3 MHz, AIN2 = 71.3 MHz



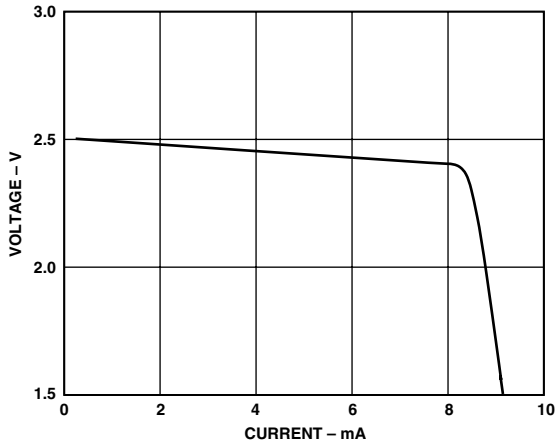
TPC 13. Single Tone SFDR



TPC 15. Integral Nonlinearity: f_S = 105 MSPS



TPC 14. Differential Nonlinearity: f_S = 105 MSPS



TPC 16. Voltage Reference Output vs. Current Load

APPLICATION NOTES

Theory of Operation

The AD9432 is a multibit pipeline converter that uses a switched capacitor architecture. Optimized for high speed, this converter provides flat dynamic performance up to frequencies near Nyquist. DNL transitional errors are calibrated at final test to a typical accuracy of 0.25 LSB or less.

USING THE AD9432

Analog Input

The analog input to the AD9432 is a differential buffer. The input buffer is self-biased by an on-chip resistor divider that sets the dc common-mode voltage to a nominal 3 V (see Equivalent Circuits section). Rated performance is achieved by driving the input differentially. Minimum input offset voltage is obtained when driving from a source with a low differential source impedance such as a transformer in ac applications. Capacitive coupling at the inputs will increase the input offset voltage by as much as ±25 mV. Driving the ADC single-endedly will degrade performance. For best dynamic performance, impedances at AIN and $\overline{\text{AIN}}$ should match.

Special care was taken in the design of the analog input section of the AD9432 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 2 V p-p. Each analog input will be 1 V p-p when driven differentially.

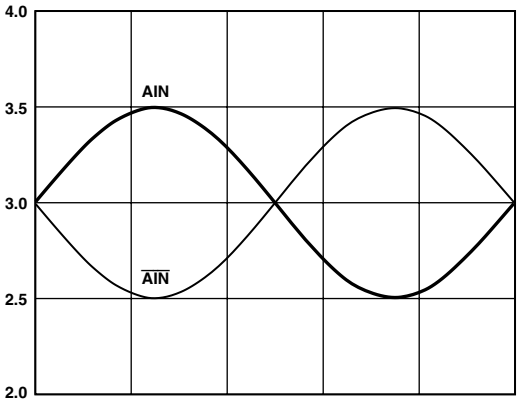


Figure 7. Full-Scale Analog Input Range

ENCODE Input

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track/hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9432, and the user is advised to give commensurate thought to the clock source. The ENCODE input supports either differential or single-ended and is fully TTL/CMOS compatible.

Note that the ENCODE inputs cannot be driven directly from PECL level signals (V_{IHD} is 3.5 V max). PECL level signals can easily be accommodated by ac coupling as shown in Figure 8. Good performance is obtained using an MC10EL16 in the circuit to drive the encode inputs.

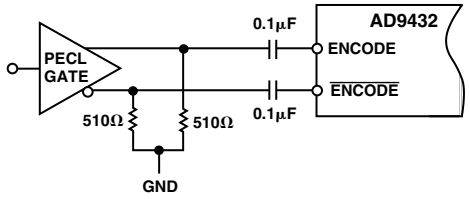


Figure 8. AC Coupling to ENCODE Inputs

ENCODE Voltage Level Definition

The voltage level definitions for driving ENCODE and $\overline{\text{ENCODE}}$ in single-ended and differential mode are shown in Figure 9.

ENCODE Inputs

Differential Signal Amplitude (V_{ID}) . . . . . 500 mV min
. . . . . 750 mV nom
High Differential Input Voltage (V_{IHD}) . . . . . 3.5 V max
Low Differential Input Voltage (V_{ILD}) . . . . . 0 V min
Common-Mode Input (V_{ICM}) . . . . . 1.25 V min, 1.6 V nom
High Single-Ended Voltage (V_{IHS}) . . . . . 2 V min to 3.5 V max
Low Single-Ended Voltage (V_{ILS}) . . . . . 0 V min to 0.8 V max

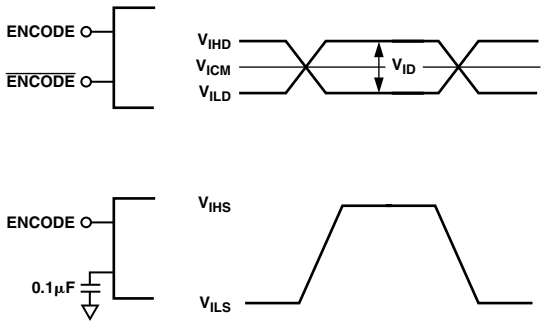


Figure 9. Differential and Single-Ended Input Levels

Often, the cleanest clock source is a crystal oscillator producing a pure sine wave. In this configuration, or with any roughly symmetrical clock input, the input can be ac-coupled and biased to a reference voltage that also provides the ENCODE. This ensures that the reference voltage is centered on the encode signal.

Digital Outputs

The digital outputs are 3.3 V (2.7 V to 3.6 V) TTL/CMOS-compatible for lower power consumption. The output data format is Two's Complement, illustrated in Table I. The out of range (OR) output (logic LOW for normal operation) will be HIGH during any clock cycle when the ADC output data (Dx) reach positive or negative full scale (–2048 or +2047). The OR is internally generated each clock cycle, has the same pipeline latency and propagation delay as the ADC output data, and will remain HIGH until the output data reflect an in-range condition. The ADC output bits (Dx) will not roll over, and will therefore remain at positive or negative full scale (+2048 or –2047) while the OR output is HIGH.

Table I. Output Coding (VREF = 2.5 V) (Two's Complement)

Code	AIN–$\overline{\text{AIN}}$ (V)	Digital Output
+2047	1.000	0111 1111 1111
•	•	•
•	•	•
0	0	0000 0000 0000
–1	–0.00049	1111 1111 1111
•	•	•
•	•	•
–2048	–1.000	1000 0000 0000

Voltage Reference

A stable and accurate 2.5 V voltage reference is built into the AD9432 (VREFOUT). In normal operation the internal reference is used by strapping Pin 45 to Pin 46 and placing a 0.1 μF decoupling capacitor at VREFIN.

The input range can be adjusted by varying the reference voltage applied to the AD9432. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage changes linearly.

Timing

The AD9432 provides latched data outputs, with 10 pipeline delays. Data outputs are included or available one propagation delay (t_{PD}) after the rising edge of the encode command (see Figure 1). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9432; these transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9432 is 1 MSPS. At internal clock rates below 1 MSPS, dynamic performance may degrade. Therefore, input clock rates below 1 MHz should be avoided.

During initial power-up, or whenever the clock to the AD9432 is interrupted, the output data will not be accurate data for 200 ns or 10 clock cycles, whichever is longer.

Using the AD8138 to Drive the AD9432

A new differential output op amp from Analog Devices, Inc., the AD8138, can be used to drive the AD9432 in dc-coupled applications. The AD8138 was specifically designed for ADC driver applications. Superior SNR performance is maintained up to analog frequencies of 30 MHz. The AD8138 op amp provides single-ended-to-differential conversion, providing for a low-cost option to transformer coupling for ac applications as well.

The circuit in Figure 10 was breadboarded and the measured performance is shown in Figures 11 and 12. The figures shown are for ±5 V supplies at the AD8138—performance dropped by about 1 dB–2 dB with a single 5 V supply at the AD8138.

Figure 11 shows SNR and SINAD for a –1 dBFS analog input frequency varied from 2 MHz to 40 MHz with an encode rate of 105 MSPS. The measurements are for nominal conditions at room temperature. Figure 12 shows the second and third harmonic distortion performance under the same conditions.

The dc common-mode voltage for the AD8138 outputs can be adjusted via input V_{OCM} to provide the 3 V common-mode voltage the AD9432 inputs require.

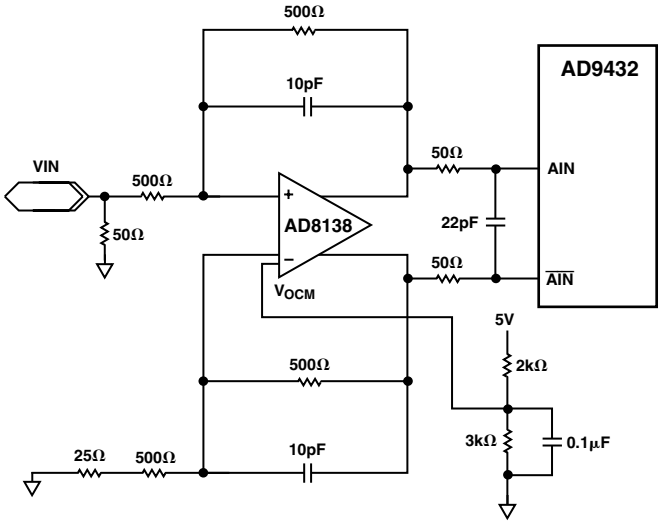


Figure 10. AD8138/AD9432 Schematic

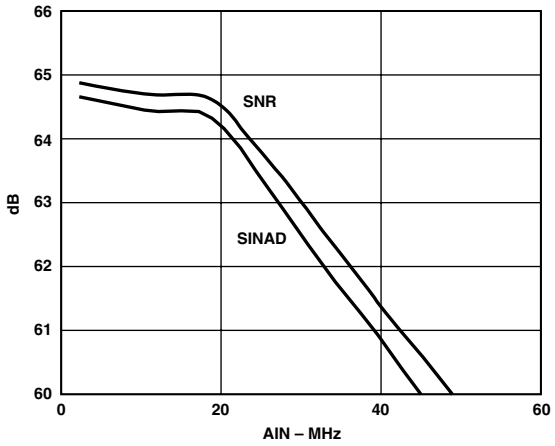


Figure 11. Measured SNR and SINAD (Encode = 105 MSPS)

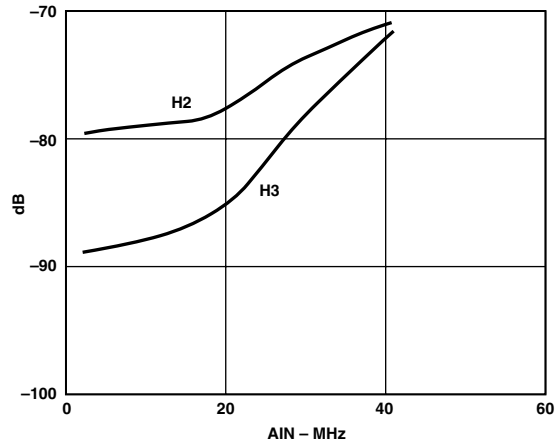


Figure 12. Measured Second and Third Order Harmonic Distortion (Encode = 105 MSPS)

EVALUATION BOARD

The AD9432 evaluation board offers an easy way to test the AD9432. It requires an analog signal, encode clock, and power supplies as inputs. The clock is buffered on the board to provide the clocks for an on-board DAC and latches. The digital outputs and output clock are available at a standard 37-pin connector P7.

Power Connector

Power is supplied to the board via two detachable 4-pin power strips P30, P40.

P40

P1	VCC2	5 V/165 mA	DAC Supply
P2	GND		
P3	VCC	5 V/200 mA	ADC Analog Supply
P4	GND		

P30

P5			No Connect
P6			No Connect
P7	VD	3.3 V /105 mA	Latch, ADC Digital Output Supply
P8	GND		

Analog Inputs

The evaluation board accepts a 2 V p-p analog input signal at SMB connector P2. This single-ended signal is ac-coupled by capacitor C11 and drives a wideband RF transformer T1 (Mini-Circuits ADT1-1WT) that converts the single-ended signal to a differential signal. (*The AD9432 should be driven differentially to provide optimum performance.*) The evaluation board is shipped with termination resistors R4, R5, which provide the effective 50 Ω termination impedance; input termination resistor R10 is optional. Note: The second harmonic distortion that some RF transformers tend to introduce at high frequencies can be reduced by coupling two transformers in series as shown in Figure 13. (Improvements on the order of 3 dB–4 dB can be realized.)

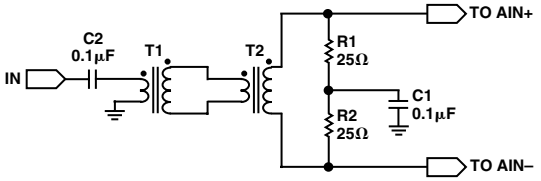


Figure 13. Improving Second Harmonic Distortion Performance

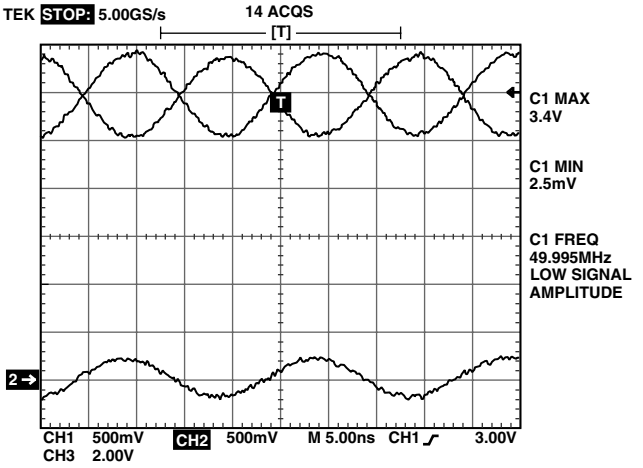


Figure 14. Analog Input Levels

The full-scale analog inputs to the ADC should be two 1 V p-p signals 180 degrees out of phase with each other, as shown in Figure 14. The analog inputs are dc biased by two on-chip resistor dividers that set the common-mode voltage to approximately 0.6 × VCC (0.6 × 5 = 3 V). AIN+ and AIN– each vary between 2.5 V and 3.5 V as shown in the two upper traces in Figure 14. The lower trace is the input at SMB P2 (*on a 2 V/div scale*).

Encode

The encode input to the board is at SMB connector P3. The (>1 V p-p) input is ac-coupled and drives two high-speed differential line receivers (MC10EL16). These receivers provide subnanosecond rise times at their outputs—a requirement for the ADC clock inputs for optimum performance. The EL16 outputs are PECL levels and must be ac-coupled to meet the common-mode dc levels required at the AD9432 encode inputs. A PECL/TTL translator (MC100ELT23), provides the clocks required at the output latches, DAC, and 37-pin connector.

Note: Jitter performance on the clock source is critical at this performance level; a stable, crystal-controlled signal generator is used to generate all of the ADC performance plots. Figure 15 shows the Encode+ clock at the ADC. The 3 V latch clock generated on the card is also shown in the plot.

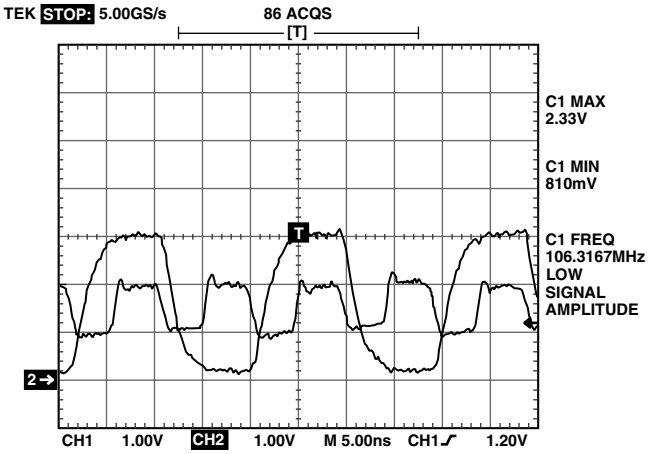


Figure 15. Encode+ Clock and Latch Clock

DATA OUTPUTS

The ADC digital outputs are latched on the board by two 574s; the latch outputs are available at the 37-pin connector at Pins 25–36. A latch output clock (data ready) is available at Pin 21, with the complement at Pin 2. There are series termination resistors on the data and clock outputs. These can be changed if required to accommodate different loading situations. Figure 16 shows a data bit switching and output clock (DR) at the connector.

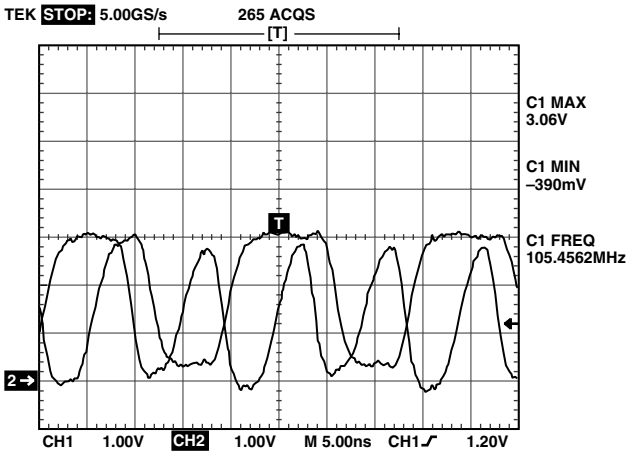


Figure 16. Data Bit and Clock at 37-Pin Connector

REFERENCE

The AD9432 has an on-chip reference of 2.5 V available at VREFOUT (Pin 46). Most applications will simply tie this output to the VREFIN input (Pin 45). This is accomplished jumping E4 to E6 on the board. An external voltage reference can drive the VREFIN pin if desired by strapping E4 to E3 and placing an AD780 voltage reference on the board (not supplied).

DAC

The evaluation board has an on-board reconstruction DAC (AD9752). This is placed only to facilitate testing and debug of the board. It should not be used to measure the performance of the ADC, as it will not accurately indicate the ADC performance. The DAC output is available at SMB P1. It will drive a 50 Ω load. Provision to power down the DAC is at Pin 15 at the DAC.

PCB LAYOUT

The PCB is designed on a four-layer (1 oz. Cu) board. Components and routing are on the top layer with a ground flood for additional isolation. Test and ground points were judiciously placed to facilitate high-speed probing. A common ground plane exists on the second layer. The third layer has three split power planes, two for the ADC and one for support logic. The DAC, components, and routing are located on the bottom layer.

TROUBLESHOOTING

If the board does not seem to be working correctly, try the following:

- Verify power at IC pins.
- Check that all jumpers are in the correct position for the desired mode of operation.
- Verify VREF is at 2.5 V.
- Try running encode clock and analog inputs at low speeds (*10 MSPS/1 MHz*) and monitor 574 outputs, DAC output, and ADC outputs for toggling.

The AD9432 Evaluation Board is provided as a design example for customers of Analog Devices, Inc. ADI makes no warranties, express, statutory, or implied, regarding merchantability or fitness for a particular purpose.

PCB Bill of Materials

#	Quantity	REFDES	Device	Package	Value
1	30	C1–C8, C10–C13, C17, C19–C22, C27–C29, C41, C42, C47, C48, C53, C56, C58, C60, C61, C70	Capacitor	603	0.1 µF
2	1	C9	Capacitor	603	0.01 µF
3	4	C14, C18, C31, C34	Capacitor	CAPTAJD	10 µF
4	1	C15	Capacitor	CAPTAJD	1 µF
5	18	E1–E13, E30, E32, E40, E42, E43	E-HOLE	Test Point	
6	3	P1, P2, P3	Connector	SMB	
7	1	P7	37-Pin Connector	Female	AMP 747462-2
8	2	P30, P40	Power Connector		
9	6	R1, R2, R7, R8, R10, R18 (R1, R2, R10 Optional)	Resistor	1206	50 Ω
10	2	R3, R35	Resistor	1206	100 Ω
11	4	R25, R26, R31, R32	Resistor	1206	500 Ω
12	2	R6, R24	Resistor	1206	2 kΩ
13	4	RP1–RP4	RES PAK		100 Ω
14	1	T1	Transformer		Mini-Circuits ADT1-1WT
15	1	U1	DAC	SOIC	AD9752
16	1	U2	Reference (Not Supplied)	SOIC	AD780N
17	2	U3, U4	Inverter (U4 Not Supplied)	SC70	NC7SZ04P5
18	1	U9	ADC	52QFP	AD9432
19	2	U12–U13	Latch	SOIC	74AC574M
20	1	Z1	PECL/TTL Translator	SOIC	MC100ELT23
21	2	Z2, Z3	Differential Receiver	SOIC	MC10EL16
22	3	R4, R5, R15	Resistor	1206	24.9 Ω

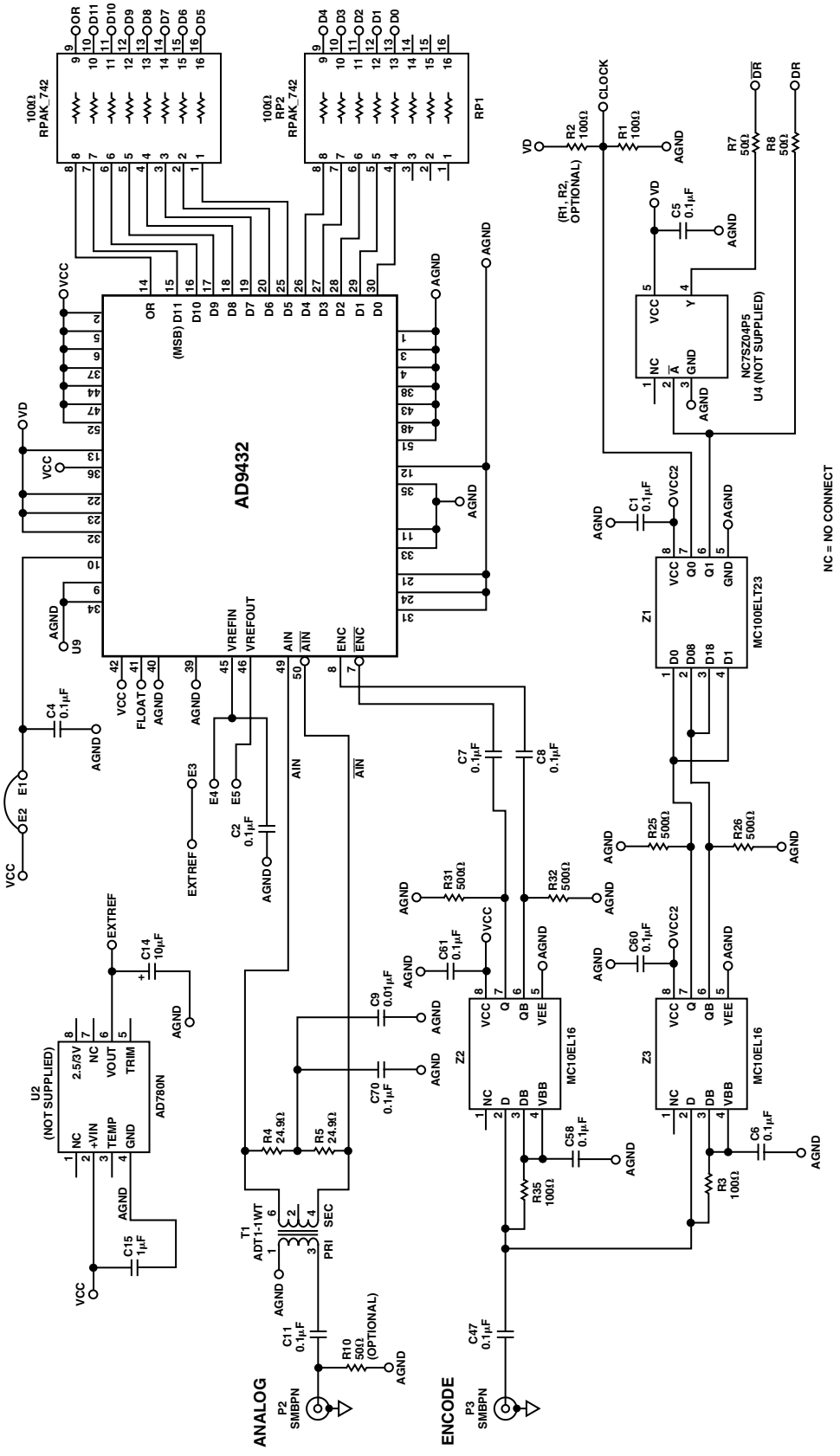


Figure 17a. PCB Schematic

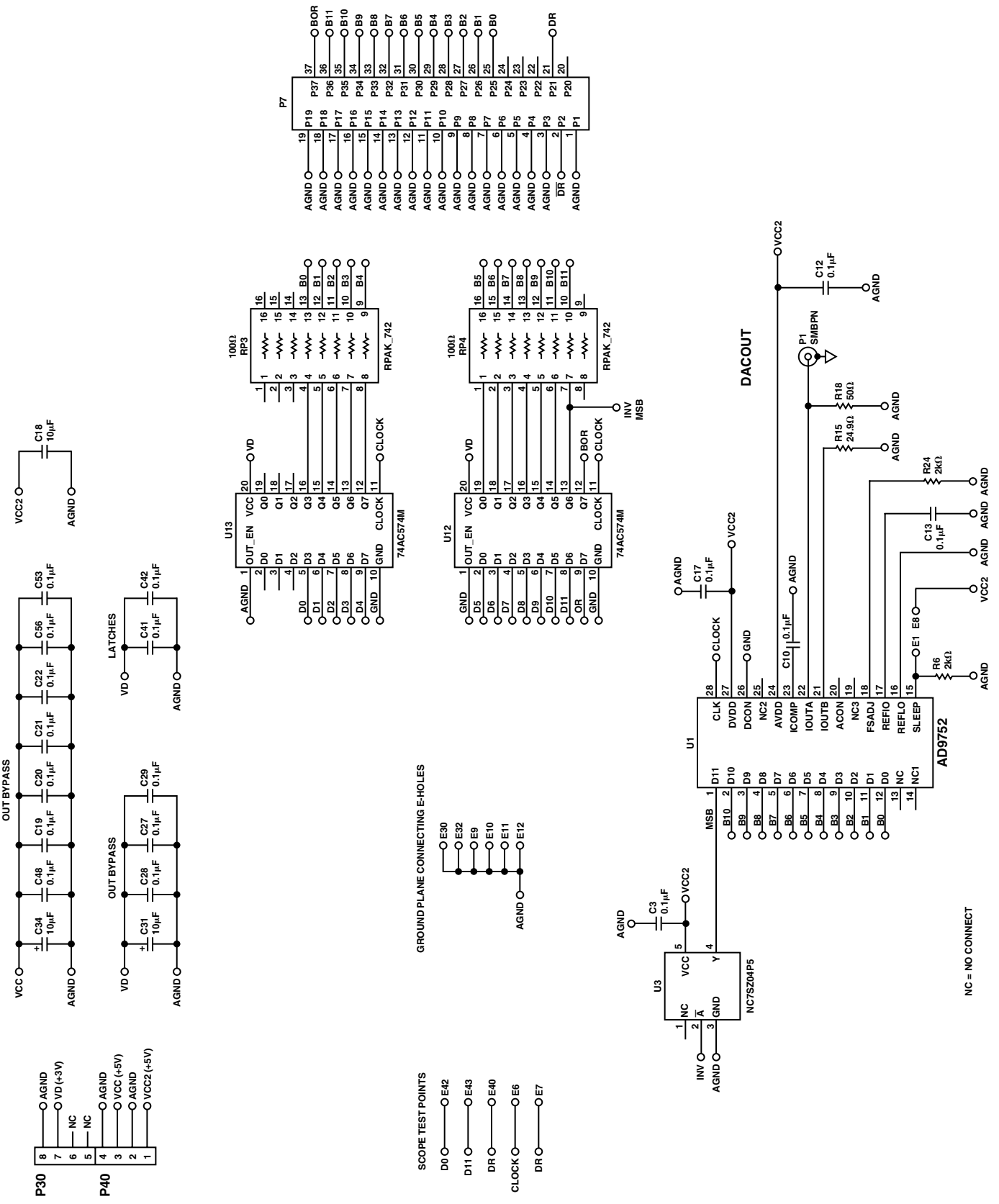


Figure 17b. PCB Schematic (Continued)

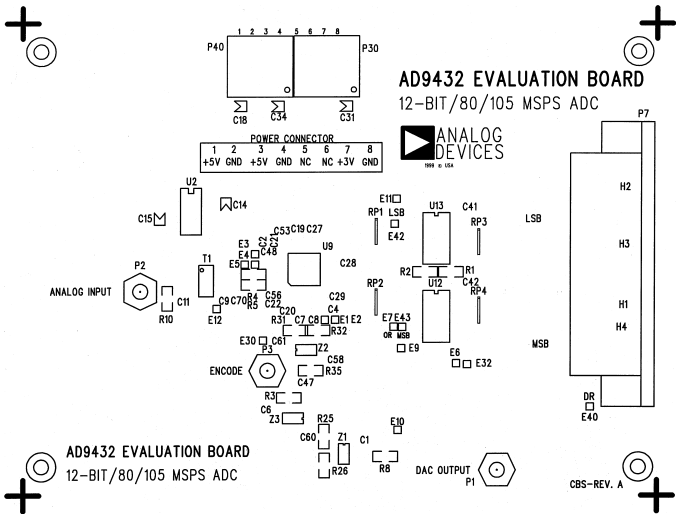


Figure 18. Top Silkscreen

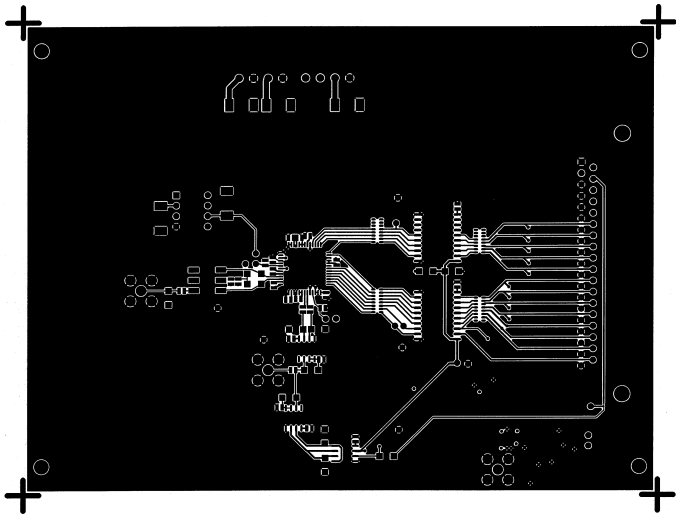


Figure 19. Top Level Routing

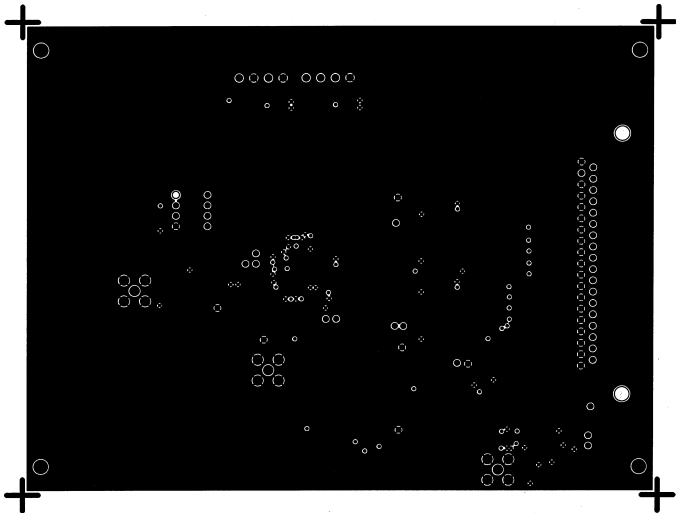


Figure 20. Ground Plane

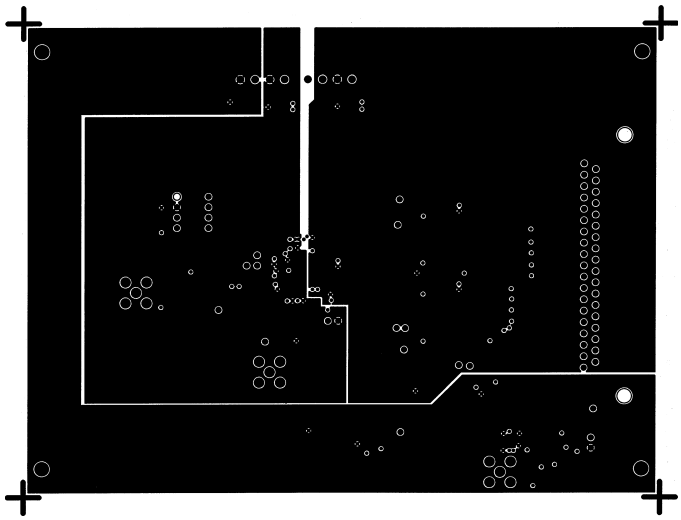


Figure 21. Split Power Plane

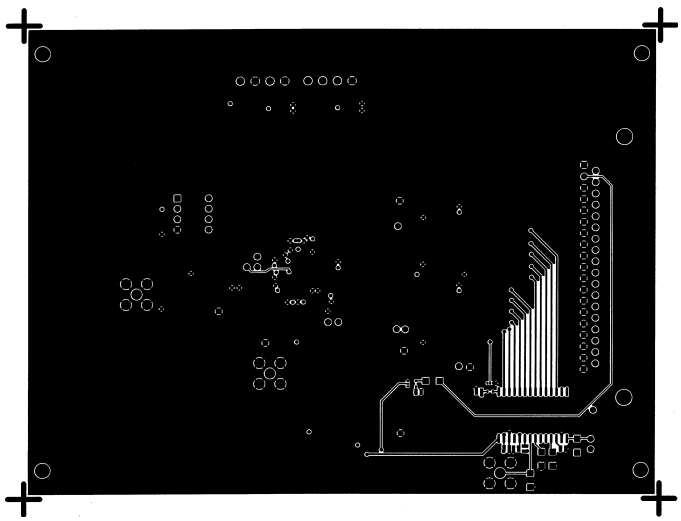


Figure 22. Bottom Layer Route

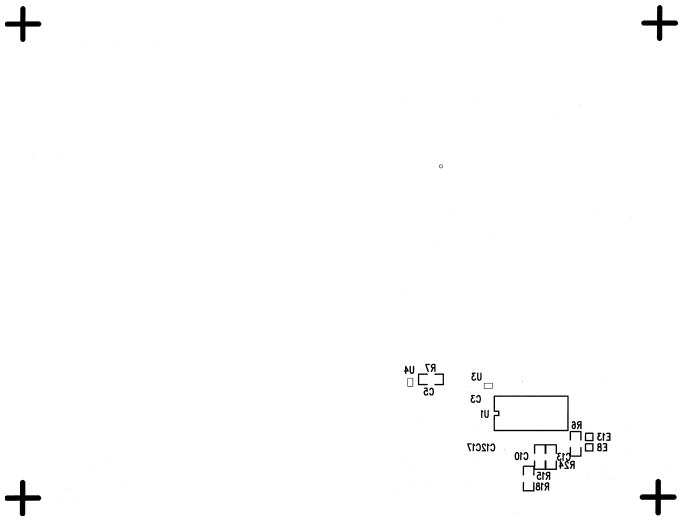
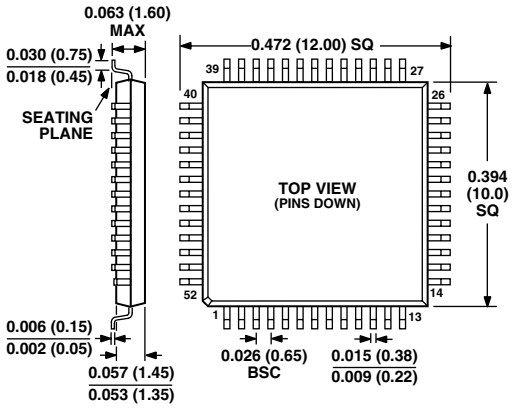


Figure 23. Bottom Silkscreen

OUTLINE DIMENSIONS

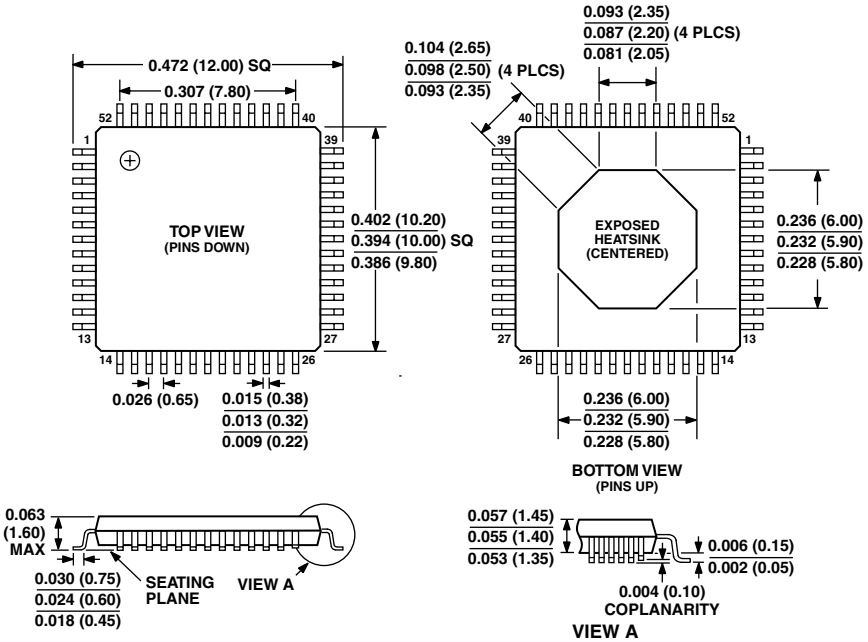
Dimensions shown in inches and (mm).

52-Lead Plastic Quad Flatpack (LQFP)
(ST-52)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

THERMALLY ENHANCED
52-Lead Power Thin Plastic Quad Flatpack (LQFP_ED)
(SQ-52)



NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
2. ALTHOUGH NOT REQUIRED IN ALL APPLICATIONS, THE AD9432 HAS AN EXPOSED METALLIC PAD ON THE PACKAGE BOTTOM WHICH IS INTENDED TO ENHANCE THE HEAT REMOVAL PATH. TO MAXIMIZE THE REMOVAL OF HEAT, A LAND PATTERN WITH CLOSELY SPACED THERMAL VIAS TO THE GROUND PLANE(S) SHOULD BE INCORPORATED ON THE PCB WITHIN THE FOOTPRINT OF THE PACKAGE CORRESPONDING TO THE EXPOSED METAL PAD DIMENSIONS OF THE PACKAGE. THE SOLDERABLE LAND AREA SHOULD BE SOLDER MASK DEFINED AND BE AT LEAST THE SAME SIZE AND SHAPE AS THE EXPOSED PAD AREA ON THE PACKAGE. AT LEAST 0.25 MM CLEARANCE BETWEEN THE OUTER EDGES OF THE LAND PATTERN AND THE INNER EDGES OF THE PAD PATTERN SHOULD BE MAINTAINED TO AVOID ANY SHORTS.

Revision History

Location	Page
Data Sheet changed from REV. D to REV. E.	
Edits to SPECIFICATIONS	3
Edits to ABSOLUTE MAXIMUM RATINGS	3
Edits to ORDERING GUIDE	3
Addition of text to USING THE AD9432 section	9
Edits to Figure 17a	13
Edits to Figure 17b	14
Addition of SQ-52 Package Outline	16

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Appendix D: Graychip GC1012

D.1 Introduction

The following pages are a reprint of the Graychip GC1012 Wideband Digital Receiver Data Sheet.

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GC1012B

3.3V DIGITAL TUNER CHIP

DATASHEET

October 2002

This datasheet contains information which may be changed at any time without notice.

REVISION HISTORY

This datasheet is revised from the GC1012A datasheet to reflect the changes in the GC1012B replacement.

Revision	Date	Description
1.0	3 May 2002	First GC1012A datasheet. Major changes in specifications to reflect 3.3volt operation.
1.1	9 October 2002	Corrected checksum table, page 7

0.1 GC1012B TO GC1012A COMPARISON

The GC1012B is designed to be a functional and footprint compatible replacement for the GC1012A chip. The timing specifications for the GC1012B meet and exceed the timing specifications for the GC1012A. Electrically the GC1012B is a 3.3 volt only part, making it incompatible with the GC1012A's 5 volt mode. The GC1012B is fully compatible with the GC1012A's 3.3 volt mode, but at a lower power consumption. See Section 4 for timing and electrical specifications. NOTE: The GC1012B inputs are NOT 5 volt tolerant; chip damage may occur if the input voltages exceed Vcc + 0.5V (3.8 volts). Designs using the GC1012A at 5 volts will need to add a 3.3 volt supply and voltage level translators to use the GC1012B.

The function of the GC1012B has been slightly enhanced, but any enhancements are "backward" compatible with the GC1012A so that a GC1012A user will not need to change any software or processing algorithms to use the GC1012B chip. The checksums for the diagnostics have changed and are shown on page 7. Highlights of the enhancements follow.

0.1.1 Clock Loss Detect and Power Down Modes

The GC1012A chip used a slow internal clock to power down the chip or to put it into a low power mode if the clock is stopped. The slow clock has been removed in the GC1012B and replaced with a mode that will put the chip in a fully static mode if the clock has stopped. The fully static mode powers down the chip and reduces the power consumption down to a few microwatts until the clock resumes. The user can also force the power down state if desired. Two control bits (address 7 bit 5 and address 9 bit 7) are used to control the clock loss detect and power down modes. One control bit turns off the clock loss detect circuit, the other forces the power down mode. Both bits are cleared at power up to keep GC1012A compatibility.

See Section 1.9 for details.

0.1.2 Control Interface

The control interface has been enhanced to use either the R/$\overline{W}$ and $\overline{CS}$ strobes of the original GC1012A, or to use the $\overline{RE}$, $\overline{WE}$ and $\overline{CE}$ strobes used by most memory interfaces. If the $\overline{RE}$ pin is grounded, then the interface behaves in the R/$\overline{W}$ and $\overline{CS}$ mode, where the $\overline{WE}$ pin becomes the R/$\overline{W}$ pin and the $\overline{CE}$ pin becomes the $\overline{CS}$ pin. The $\overline{RE}$ pin on the GC1012B chip is a ground pin (pin 103) on the GC1012A chip, so that a GC1012B chip soldered into a GC1012A socket will automatically operate in the GC1012A R/$\overline{W}$ and $\overline{CS}$ mode.

See Section 1.3 for details.

This document contains information which may be changed at any time without notice

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GC1012B DATASHEET

1.0 FUNCTIONAL DESCRIPTION

Fabricated in high speed CMOS technology, the GC1012B chip is an all digital tuner which can downconvert and band limit signals from wide band digitized sources. At full rate operation (100 MHz input rate), the input bandwidth can be up to 50 MHz wide. Any signal within the input bandwidth can be down-converted to zero frequency, low pass filtered, and output at a reduced sample rate. The chip's output can be formatted as either a complex data stream, or as a real data stream. The complex samples are output at rates equal to $F_O=F_{CK}/D$, where F_O is the output rate, D is 1, 2, 4, 8, 16, 32 or 64 and F_{CK} is the input sample (clock) rate. The real output rates are $F_O=2F_{CK}/D$ for D equal to 2, 4, 8, 16, 32, or 64.

The signal is low pass filtered to remove out of band energy before the sample rate is decreased. The filter's out of band rejection is over 75 dB and its passband ripple is less than 0.2 dB peak to peak. The passband of the output filter covers 80% of the output bandwidth.

The 28 bit accumulator in the chip's digital oscillator circuit provides a tuning accuracy equal to the input clock rate divided by 2^{28}. The tuning resolution at a clock rate of 50 MHz is less than 0.2 Hz giving a tuning accuracy of +/- 0.1 Hz. The phase noise in the oscillator is low enough to provide a spur free dynamic range of over 75 dB.

The chip's output circuit allows the user to select a real or complex data output format, to select spectral inversion, or to offset the output spectrum by half of the output sample rate. The output's signal gain can be adjusted in 0.03 dB steps. The word size of the output samples are either 10, 12, 14, or 16 bits.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of an 8 bit data I/O port, a 4 bit address port, read and write strobes, and a control select strobe.

I and Q output registers can be read from the control port to allow an external processor to monitor or process the chip's output samples. These registers are valuable for monitoring the chip's output power in order to set and adjust gain levels.

1.1 KEY FEATURES

- 100 million samples per second input rate
- 0.1 Hz tuning resolution
- >75 dB dynamic range
- Programmable output bandwidth
- 12 bit inputs, 10, 12, 14, or 16 bit outputs
- Real or complex output formats
- Built in strobe/sync generator
- Symmetric rounding used throughout
- Gain adjust in 0.03 dB steps
- Microprocessor interface for control, output, and diagnostics
- Power down mode
- Auto power down with clock loss detection
- Built in diagnostics
- 850 mW at 60 MHz, 3.3 volts
- 120 pin quad flat pack package

This document contains information which may be changed at any time without notice

1.2 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1

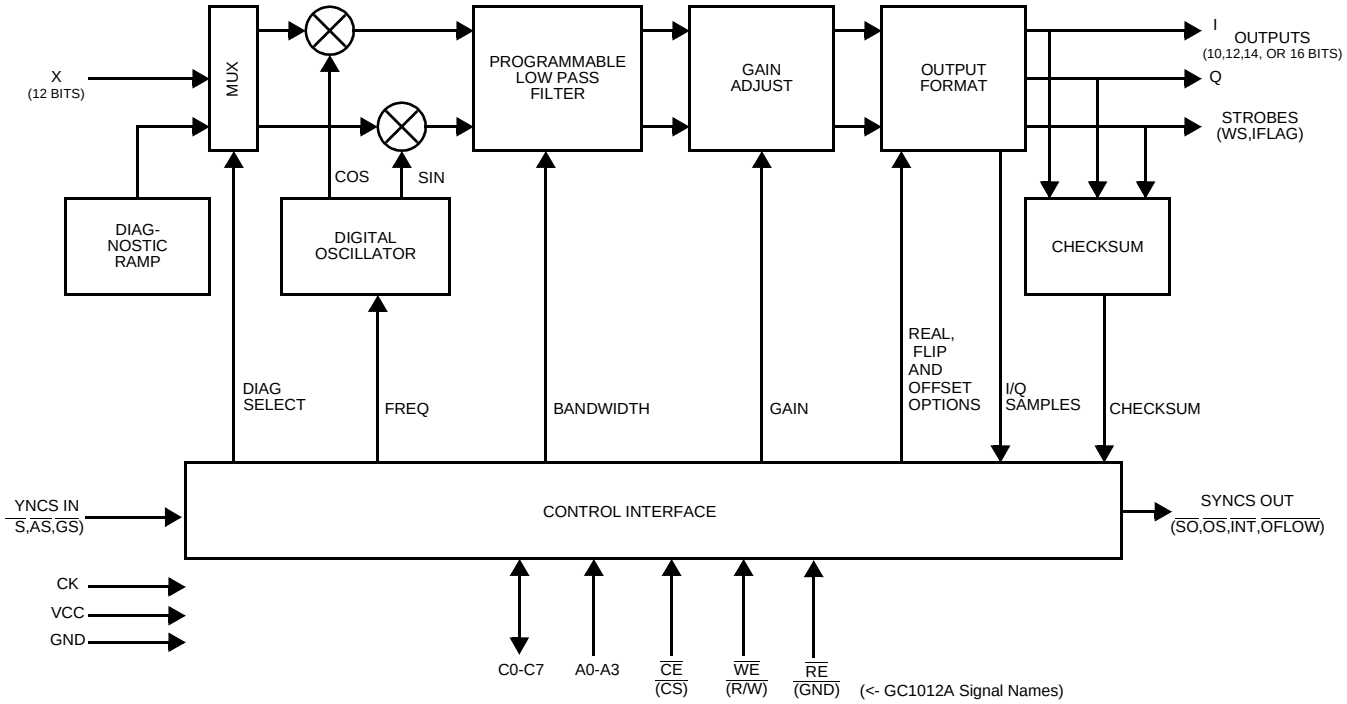


Figure 1. GC1012B Block Diagram

Each of these functions are described below.

1.3 CONTROL INTERFACE

The control interface performs four major functions: It allows an external processor to configure the chip, it allows an external processor to capture and read output samples from the chip, it allows an external processor to perform diagnostics, and it generates internal synchronization strobes.

The chip is configured by writing control information into 8 bit control registers within the chip. The contents of these control registers and how to use them are described in Section 3. The registers are written to or read from using the **C[0:7]**, **A[0:3]**, **$\overline{\text{WE}}$, $\overline{\text{RE}}$**, and **$\overline{\text{CE}}$** pins. Each control register has been assigned a unique address within the chip. An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:3]** to the desired register address, setting the **$\overline{\text{CE}}$** pin low, setting **C[0:7]** to the desired value and then pulsing **$\overline{\text{WE}}$** low. **$\overline{\text{RE}}$** must remain high

To read from a control register the processor must set **A[0:3]** to the desired address, set **$\overline{\text{CE}}$** low, and then set **$\overline{\text{RE}}$** low. The chip will then drive **C[0:7]** with the contents of the selected register. After the processor has read the value from **C[0:7]** it should set **$\overline{\text{RE}}$** and **$\overline{\text{CE}}$** high. The **C[0:7]** pins are turned off (high impedance) whenever **$\overline{\text{CE}}$** is high or **$\overline{\text{WE}}$** is low.

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The chip will only drive these pins when **$\overline{\text{CE}}$** is low and **$\overline{\text{RE}}$** is high. If RE is held low, then the interface will behave in the GC1012A mode, where **$\overline{\text{CE}}$** is **$\overline{\text{CS}}$**, and **$\overline{\text{WE}}$** is **R/$\overline{\text{W}}$**.

Control register addresses 12, 13, 14, and 15 are reserved to allow an external processor to read output samples from the chip. Addresses 12 and 13 are the I-registers which store the16 bit in-phase part of the output sample. Addresses 14 and 15 are the Q-registers which store the quadrature part. In the real mode the I registers store the even-time output samples and the Q registers store the odd-time output samples. Output ready and missed flags are provided in control register 9 in order to synchronize the storing and reading of the output samples. An interrupt output pin is also provided on the chip which can be used to interrupt the external processor when a new sample is ready. See the description of control register 9 in Section 3.6 for more details. The setup, hold and pulse width requirements for control read or write operations are given in Section 4.4.

Checksums are read from the chip during diagnostics using address 11. More details on the diagnostic modes is given in Section 1.11.

Address 10 is used to generate a one-shot pulse on the **$\overline{\text{OS}}$** output pin. This pulse can be used to synchronize the output timing and/or frequency oscillators of multiple GC1012B chips.

The control interface also generates the chip's internal sync strobes. The user may select to synchronize the chip using an external sync strobe (**$\overline{\text{SS}}$**), or use the chip's internal sync counter. The internal sync counter can be synchronized to **$\overline{\text{SS}}$**, or left to free run (See **SS_OFF** in Section 3.2). The period of the internal sync counter can be either 256 clocks or 2^{20} clocks. The 256 clock period is intended to be used for chip test purposes only. The internal sync counter is used during diagnostics to clear the data paths and strobe the checksum generator. The internal sync counter can also be used to periodically re-synchronize all of the counters in the chip during normal operating modes.

1.4 DIGITAL OSCILLATOR

The digital oscillator generates sine and cosine sequences which are used to mix the desired signal down to zero frequency. The digital oscillator contains a 28 bit frequency register, a 28 bit frequency accumulator, and a sine-cosine generator. The tuning frequency of the oscillator is set by loading a 28 bit frequency word from the control registers into the frequency register. If the frequency register is set to the word **FREQ**, then the tuning frequency will be: $\text{Frequency} = \frac{\text{Sample Rate}}{2^{28}}\textbf{FREQ}$. The tuning frequency should be set to the middle of the desired output bandwidth.

The frequency word **FREQ** is stored into the control registers at control addresses 0,1,2 and 3. The 28 bit word is then transferred into the frequency register using one of the following methods:

(1) The frequency register is always loading (the frequency changes immediately as the frequency word is loaded into the control registers).

(2) The frequency register is loaded when the user sets a control register bit.

(3) The frequency register is synchronously loaded when the accumulator sync strobe (**$\overline{\text{AS}}$**) goes low.

(4) The frequency register is synchronously loaded when the system sync strobe (**$\overline{\text{SS}}$**) goes low.

See Section 3.2 for more details on the frequency load modes.

The 28 bit frequency word is accumulated in the 28 bit frequency accumulator. The frequency accumulator will normally free run, but can be synchronously cleared by either the system sync (**$\overline{\text{SS}}$**) or the accumulator sync (**$\overline{\text{AS}}$**). The accumulator clear modes are controlled by bits in control register 4. See Section 3.2 for details.

The upper 13 frequency accumulator bits are used to generate the oscillator's sine and cosine outputs. These sines and cosines are generated to 12 bit accuracy. The oscillator's peak spur levels are below -75 dB.

1.5 MIXER

The mixer multiplies the 12 bit input samples by the 12 bit sine and cosine values coming from the digital oscillator. An input signal at the oscillator's tuning frequency will be centered at zero frequency after passing through the mixer. The mixer outputs are rounded to 13 bits using the "round-to-even" rounding algorithm. The "round-to-even" algorithm prevents a DC rounding bias by detecting fractions which are exactly equal to 0.5 and rounding them up half of the time and rounding them down half of the time. The choice to round up or down is made so as to always give an even result.

1.6 PROGRAMMABLE LOW PASS FILTER

The mixer's output is filtered using a programmable bandwidth low pass filter. The filter allows the output sample rate to be reduced by a factor of **D** = 2, 4, 8, 16, 32, or 64. The value of **D** is set using control register 5. The filter can be bypassed by setting **D** equal to 1. This allows the chip to be used as a mixer without any output filtering.

The low pass filter is a finite impulse response (FIR) filter with linear phase, 0.13 dB peak to peak ripple and over 75 dB of out of band rejection. The 2 dB output bandwidth is +/- $0.4F_S$ (80% usable bandwidth) where F_S is the complex output rate. The 0.1 dB bandwidth is +/- 0.36 F_S (72% usable bandwidth). The number of taps is equal to 20**D**.

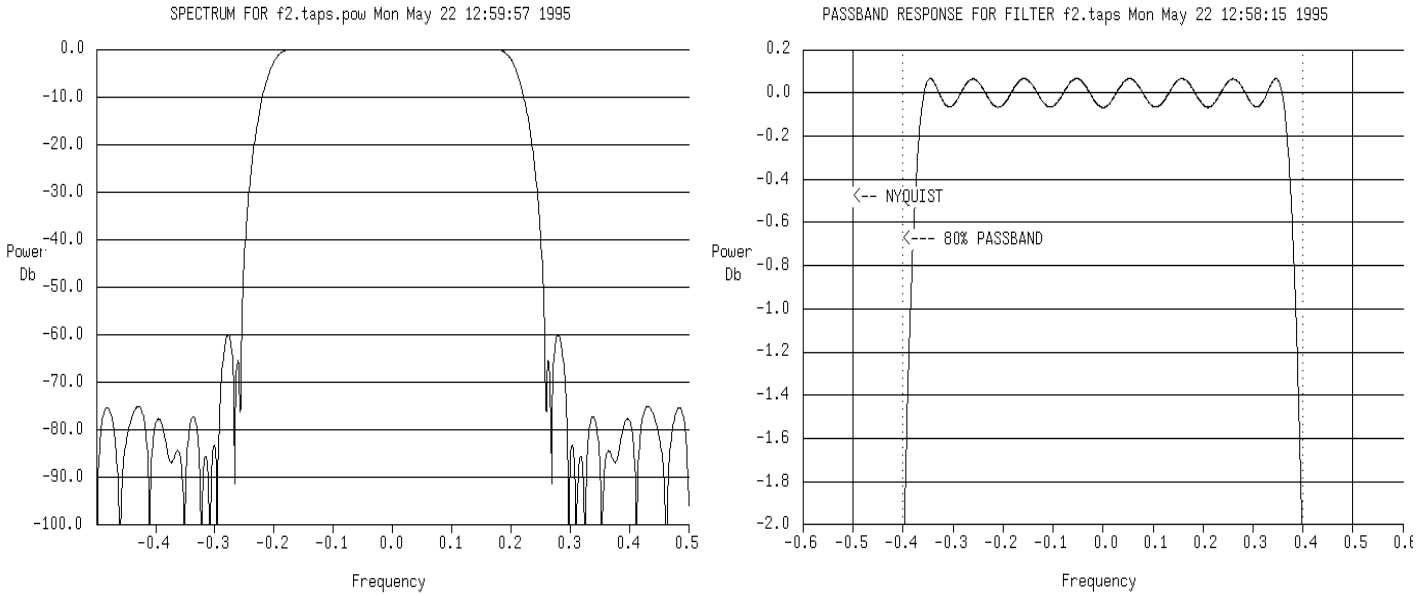
The coefficients for the 40 tap decimate by 2 filter are:

```
-12     -42     -52     7       85      46      -110    -145    82      276
39      -396    -293    434     714     -273    -1400   -409    3115    6462
6462    3115    -409    -1400   -273    714     434     -293    -396    39
276     82      -145    -110    46      85      7       -52     -42     -12
```

The coefficients for the other filters are available from GRAYCHIP.

Figure 2 shows the spectral response of the decimate by 2 low pass filter. The decimate by 4, 8, 16, 32 and 64 filters are similar. Figure 2(a) shows the overall frequency response prior to decimation.Note that the filter rolls off quickly to 60 dB and is down below 75 dB in the region which aliases back into the passband. Figure 2(b) shows the 0.13 dB ripple in the passband.

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(a) Overall (b) Passband

Figure 2. Filter Response

1.7 GAIN

The programmable bandwidth filter is followed by a gain circuit which adjusts the output level in 0.03 dB steps. The gain is controlled by the power of two gain value **S** and the fractional gain value **F**. The input to output gain of the chip is equal to $\mathbf{G} = 2^{(\mathbf{S}-B)}(1+\mathbf{F}/256)$, where **S** ranges from 0 to 15, **F** ranges from 0 to 255, and **B** is the base gain setting for each value of **D**. The base gain setting **B** gives a unity input to output gain for the chip, i.e., a 12 bit constant going into the chip will come out in the 12 MSBs of the 16 bit output word. The values of **B** are:

D	**B**
1	6
2	5
4	4
8	3
16	2
32	1
64	0

The **S** and **F** gain settings are double buffered so that they can be applied synchronously. A new gain setting takes effect either when **S** is loaded, or, if the GS_MODE control bit is used, when the $\overline{\mathbf{GS}}$ strobe is received.

The gain settings and GS_MODE bit are stored in control registers 6 and 7.

Overflow detection circuitry detects overflow conditions in the gain output words and saturates the samples to plus or minus full scale. Overflows are reported in the STATUS register and on the $\overline{\mathbf{OFLOW}}$ output pin. The overflow status can be used to detect if the gain settings are too high.

1.8 OUTPUT FORMATTING

The output format circuit allows the user to flip the output spectrum, to offset the spectrum by one-fourth the Nyquist rate, to convert the complex output stream to a real one at twice the rate, to round the samples to 10, 12, 14 or16 bits, and to multiplexes the I and Q samples together. These options are set using control register 8.

A word strobe (**WS**) is generated as an output clock signal. The **WS** strobe is either one clock cycle wide or is a 50% duty cycle clock. The polarity of **WS** is programmable.

The I and Q samples can be multiplexed together onto the I output pins by using the IQMUX mode. The **IFLAG** output pin is used in this mode to identify when the I words are being output. The **WS** strobe rate is doubled in this mode. The Q output pins are cleared in this mode.

Only the I output pins are used in the real mode. The Q pins are cleared. The output spectrum is centered from 0 to $F_O/2$ in the real mode. The spectrum is centered from $-F_O/2$ to $+F_O/2$ in the complex mode. The OFFSET control allows the spectrum to be centered from 0 to F_O.

The output format circuitry is synchronized by the $\overline{\textbf{SS}}$ input sync. This allows one to synchronize the output timing of multiple GC1012B chips.

1.9 POWER DOWN AND KEEPALIVE MODES

Unused chips in a system can be powered down by setting the POWER_DOWN control bit in register 9 (See Section 3.6). This reduces the internal clock rate down to 1 KHz to minimize the power consumed by the chip while still refreshing the internal dynamic nodes at a suitable rate.

The chip includes a “keepalive” circuit which detects when the clock has stopped for more than 2 milliseconds. The chip will automatically go into the power down mode if clock loss is detected. The keepalive detection circuit can be disabled by setting bit 5 in register 7 (See Section 3.4). NOTE: The chip will draw up to an Amp of current if the clock is stopped and the keepalive circuit is disabled.

1.10 THE ONE SHOT PULSE GENERATOR

The chip can generate a one-shot pulse which is output on the $\overline{\textbf{OS}}$ pin by writing to address 10. The pulse can be connected to the $\overline{\textbf{SS}}$, $\overline{\textbf{AS}}$, or $\overline{\textbf{GS}}$ sync input pins of GC1012B chips (including itself) to synchronize the output timing, frequency oscillators, or gain settings of multiple chips.

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1.11 DIAGNOSTICS

An input ramp generator, a sync period generator, and a checksum generator are provided on the chip in order to run diagnostic tests. Diagnostics are performed by turning on the ramp generator, enabling the diagnostic syncs, letting the chip operate for at least 4 sync periods, reading the checksum and comparing it to its predicted value. A new checksum is generated every sync period. The input ramp sequence is the same for every sync period and the chip is re-initialized at the beginning of each sync period so that each checksum should be the same once the chip's data path has been flushed. The chip requires at least 3 sync periods to flush, so the fourth and following checksums should be valid. The test is then repeated for several different tuning frequencies, decimation settings, and output modes.

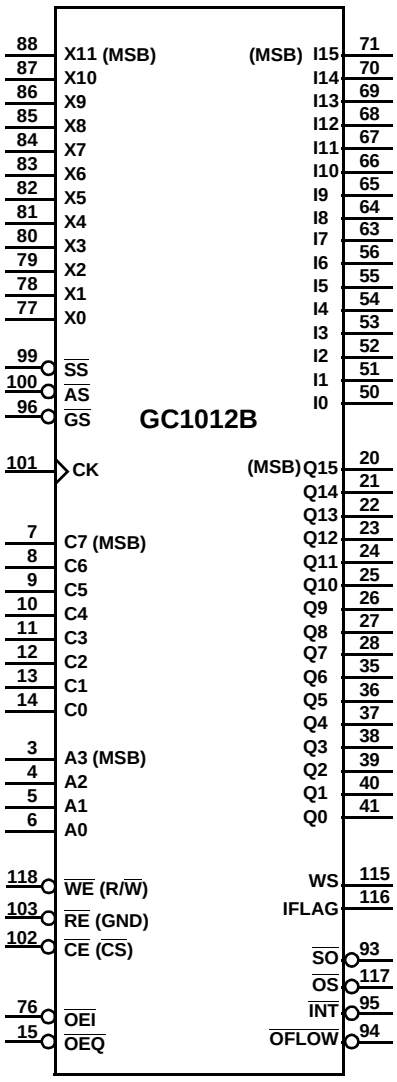
The sync period is 2^{20} clocks, or approximately 1 million clock cycles, so four sync periods will be about 4 million clocks. This represents a delay of less than 67 milliseconds for a clock rate of 60 MHz.

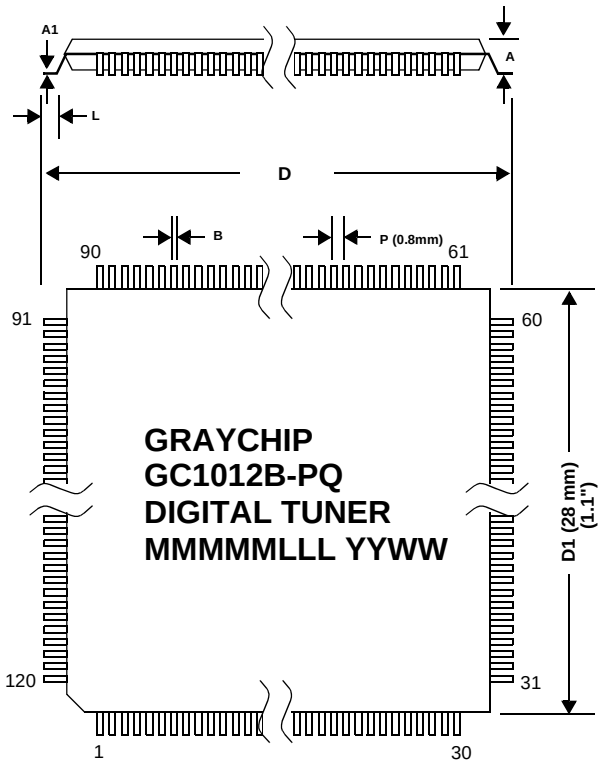
The following table lists the expected checksums for four test configurations. All values are in HEX.

CONTROL REGISTER	**TEST 1**	**TEST 2**	**TEST 3**	**TEST 4**
FREQ (REG 0,1,2,3)	0000101	0F0F0F0	55AA55A	AA55AA5
SYNC MODE (REG 4)	A9	A9	A9	A9
FILTER MODE (REG 5)	82	93	E4	D7
GAIN FRACTION (REG 6)	AA	55	00	FF
GAIN EXPONENT (REG 7)	5	4	3	0
OUTPUT (REG 8)	16	46	21	80
EXPECTED CHECKSUMS (REG 11)	C5	05	12	C9

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2.0 PIN DESCRIPTIONS





120 PIN QUAD FLAT PACK PACKAGE

GC1012B-PQ = Enhanced Thermal Plastic Package

Package Markings: MMMMM = Mask Code
LLL = Lot Number
YYWW = Date Code

DIMENSION		PLASTIC	CERAMIC
D	(width pin to pin)	31.2 mm (1.228")	32.0 mm (1.260")
D1	(width body)	28.0 mm (1.102")	28.0 mm (1.102")
P	(pin pitch)	0.8 mm (0.031")	0.8 mm (0.031")
B	(pin width)	0.35 mm (0.014")	0.35 mm (0.014")
L	(leg length)	0.88 mm (0.035")	0.70 mm (0.028")
A	(height)	4.07 mm (0.160")	3.25 mm (0.128")
A1	(pin thickness)	0.17 mm (0.007")	0.2 mm (0.008")

VCC PINS: 2,16,17,29,32,33,43,44,47,48,58,59,62,74,75,89,91,97, 104,105,106,109,110,114,119

GND PINS: 1,18,19,30,31,34,42,45,46,49,57,60,61,72,73,90,92,98, 107,108,111,112,113,120

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

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SIGNAL	DESCRIPTION
X[0:11]	**INPUT DATA.** *Active high* The 12 bit two's complement input samples. New samples are clocked into the chip on the rising edge of the clock. The input data rate is assumed to be equal to the clock rate.
CK	**CLOCK INPUT.** *Active high* The clock input to the chip. The **X**, **$\overline{SS}$**, **$\overline{GS}$** and **$\overline{AS}$** signals are clocked into the chip on the rising edge of this clock. The **I**, **Q**, **WS**, **IFLAG**, **$\overline{OS}$**, **$\overline{OFLOW}$** and **$\overline{SO}$** signals are clocked out on the rising edge of this clock.
$\overline{SS}$	**SYSTEM SYNC**. *Active low* The sync input to the chip. All timers, accumulators, and control counters are, or can be, synchronized to **$\overline{SS}$**. Bits in control register 4 (see Section 3.2) determine the operation of **$\overline{SS}$**. This sync is clocked into the chip on the rising edge of the clock.
$\overline{AS}$	**ACCUMULATOR SYNC**. *Active low* The accumulator sync is provided to synchronously change tuning frequencies. This sync can be used to load a new tuning frequency into the frequency register and/or to clear the frequency accumulator. This signal is clocked into the chip on the rising edge of the clock.
$\overline{GS}$	**GAIN SYNC**. *Active low* The gain sync is provided to synchronously change gain settings. This signal is clocked into the chip on the rising edge of the clock.
I[0:15]	**IN-PHASE OUTPUT DATA**. *Active high* The I part of each complex output sample is output as a 16 bit word on this pin. The bits are clocked out on the rising edge of the clock.
$\overline{OEI}$	**IN-PHASE OUTPUT ENABLE**. *Active low* The **I[0:15]** output pins are put into a high impedance state when this pin is high.
Q[0:15]	**QUADRATURE OUTPUT DATA**. *Active high* The Q part of each complex output sample is output as a 16 bit word on this pin. The bits are clocked out on the rising edge of the clock.
$\overline{OEQ}$	**QUADRATURE OUTPUT ENABLE**. *Active low* The **Q[0:15]** output pins are put into a high impedance state when this pin is high.
WS	**WORD STROBE**. *Programmable active high or low level* This strobe is output synchronous with the **I** and **Q** data words. The strobe occurs once per bit and is either one clock wide or has a 50% duty cycle. The high/low polarity of the strobe is programmable. See Section 3.5 for details.
IFLAG	**IN-PHASE STROBE**. *Active high* This strobe identifies the in-phase half of a complex pair when the outputs are in the IQ_MUX mode. See Section 3.5 for details. This signal is high when the I-half is output and is low when the Q-half is output.
$\overline{SO}$	**SYNC OUT**. *Active low* This signal is either a delayed version of the input system sync **$\overline{SS}$**, or, if SS_MUX in control register 4 is set, is the internally generated sync which has a period of 2^{20} clocks.
$\overline{INT}$	**INTERRUPT OUT**. *Active low* This signal is the READY flag from control register 9. This interrupt goes active when a new output sample is ready in control registers 12, 13, 14, and 15.
$\overline{OS}$	**ONE SHOT STROBE**. *Active low* This output is a one-shot sync strobe generated by writing to control address 10. The strobe is one clock cycle wide.
$\overline{OFLOW}$	**OVERFLOW FLAG**. *Active low* This signal goes low when an overflow is detected in the gain circuit. The signal will either pulse low for one clock cycle or will stay low depending upon the state of the OFLOW_MODE bit in control register 9.
C[0:7]	**CONTROL DATA I/O BUS**. *Active high* This is the 8 bit control data I/O bus. Control register data is loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{CS}$** is low and **R/$\overline{W}$** is high.
A[0:3]	**CONTROL ADDRESS BUS**. *Active high* These pins are used to address the 16 control registers within the chip. Each of the 16 control registers within the chip are assigned a unique address. A control register can be written to or read from by setting **A[0:3]** to the register's address.
$\overline{RE}$	**READ STROBE**. *Active low* The **$\overline{RE}$** strobe is used to read the control registers. Control register data is output when both **$\overline{RE}$** and **$\overline{CE}$** are low.
$\overline{WE}$	**WRITE STROBE.** *Active low* The **$\overline{WE}$** strobe is used to write the control registers. Control register data is written when both **$\overline{WE}$** and **$\overline{CE}$** are low.
$\overline{CE}$	**CHIP ENABLE**. *Active low* This control enables the read or write operation. The contents of the register selected by **A[0:3]** will be output on **C[0:7]** when **$\overline{RE}$** is low and **$\overline{CE}$** is low. If **$\overline{WE}$** is low when **$\overline{CE}$** goes low, then the selected register will be loaded with the contents of **C[0:7].**

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3.0 CONTROL REGISTERS

The chip is configured and controlled through the use of 16 eight bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{\text{CS}}$**, **$\overline{\text{WE}}$**, **$\overline{\text{RE}}$**, **A[0:3]**, and **C[0:7]**) described in the previous section. The register names and their addresses are:

ADDRESS	NAME	ADDRESS	NAME
0	FREQ byte 0	8	Output Mode
1	FREQ byte 1	9	Status
2	FREQ byte 2	10	One Shot
3	FREQ byte 3	11	Checksum
4	Sync mode	12	I-output byte 0
5	Filter mode	13	I-output byte 1
6	Gain Fraction	14	Q-output byte 0
7	Gain Exponent	15	Q-output byte 1

The following sections describe each of these registers. The type of each register bit is either R or R/W indicating whether the bit is read only or read/write. All bits are active high.

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3.1 FREQUENCY WORD REGISTERS

Registers 0, 1, 2, and 3 contain the 28 bit frequency tuning word. Bit 0 is the LSB, bit 27 is the MSB.

ADDRESS 0: FREQUENCY BYTE 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[0:7]	Byte 0 (least significant) of frequency word

ADDRESS 1: FREQUENCY BYTE 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[8:15]	Byte 1 of frequency word

ADDRESS 2: FREQUENCY BYTE 2

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**FREQ**[16:23]	Byte 2 of frequency word

ADDRESS 3: FREQUENCY BYTE 3

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**FREQ**[24:27]	4 most significant bits of the frequency word
4-7	R/W	-	unused

If the desired tuning frequency is **F**, then the frequency word should be set to:

$$\mathbf{FREQ} = 2^{28}\mathbf{F}/(\text{clock rate})$$

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3.2 SYNC MODE REGISTER

The sync mode register controls the action of the **$\overline{\text{SS}}$** and **$\overline{\text{AS}}$** sync strobes and how they affect the chip's internal timers, counters, and accumulators.

ADDRESS 4: Sync Mode Register

BIT	TYPE	NAME	DESCRIPTION
0 (LSB)	R/W	SS_OFF	This bit disables the **$\overline{\text{SS}}$** input.
1	R/W	AS_ON	Enables the accumulator sync **$\overline{\text{AS}}$**. Normally the frequency accumulator will free run. This bit causes the frequency accumulator to be initialized to the contents of the frequency register when **$\overline{\text{AS}}$** goes low. **$\overline{\text{SS}}$**, instead of **$\overline{\text{AS}}$**, will reset the accumulator if AS_MUX is set and **$\overline{\text{SS}}$** is not disabled by SS_OFF.
2	R/W	AS_MUX	Use **$\overline{\text{SS}}$** for the accumulator sync. The **$\overline{\text{AS}}$** input is ignored and the **$\overline{\text{SS}}$** strobe is used in its place when this bit is set and **$\overline{\text{SS}}$** is not disabled by SS_OFF. (See AS_ON and AS_FREQ).
3	R/W	LD_FREQ	Load the frequency register in the digital oscillator with the contents of the frequency word registers. If left on, this bit will cause the frequency register to load whenever a frequency word register is changed.
4	R/W	AS_FREQ	Enables the synchronous frequency load mode. When this bit is set and **$\overline{\text{AS}}$** goes low, the frequency register will be synchronously loaded with the contents of the frequency control registers. **$\overline{\text{SS}}$**, instead of **$\overline{\text{AS}}$**, will load the frequency register if AS_MUX is set and **$\overline{\text{SS}}$** is not disabled by SS_OFF.
5	R/W	SS_DIAG	Enables diagnostic syncs. This bit routes the internal sync to the checksum generator and to all accumulators and control counters within the chip. This forces the chip to re-initialize at the start of every sync period. The internal sync period will be 2^{20} clocks if SS_MUX is set, otherwise it will be determined by the period of an externally provided **$\overline{\text{SS}}$** strobe.
6	R/W	TEST	Shortens the internal sync counter period from 2^{20} clocks to 2^{8} clocks. This mode is used to test chips at the factory.
7 (MSB)	R/W	SS_MUX	Use the sync counter's terminal count strobe for the internal sync instead of the sync input **$\overline{\text{SS}}$**. The internal sync is output on the **$\overline{\text{SO}}$** pin.

The operation of these control bits are illustrated in Figure 3.

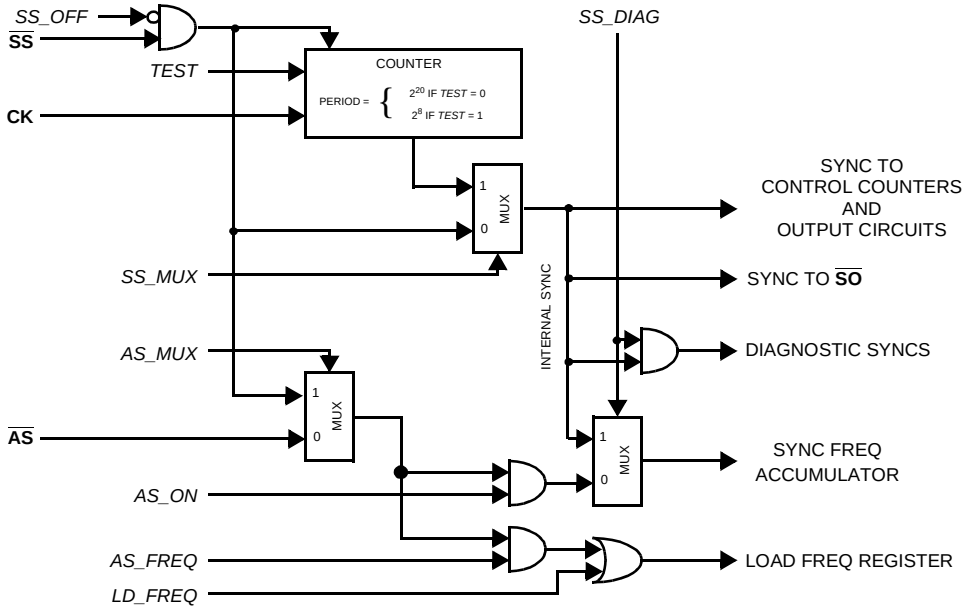


Figure 3. Sync Controls

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3.3 FILTER MODE REGISTER

This register controls filtering, output formatting and the diagnostic input mode.

ADDRESS 5: Filter Mode Register

BIT	TYPE	NAME	DESCRIPTION
0-2	R/W	**DEC[0:2]**	The decimation mode. The output sample rate is set using **DEC** according to the following table:

	F_O **DECCOMPLEX** (REAL = 0)	F_O **REAL** (REAL = 1)
0 or 1	F_{CK}	?
2	$F_{CK}/2$	F_{CK}
3	$F_{CK}/4$	$F_{CK}/2$
4	$F_{CK}/8$	$F_{CK}/4$
5	$F_{CK}/16$	$F_{CK}/8$
6	$F_{CK}/32$	$F_{CK}/16$
7	$F_{CK}/64$	$F_{CK}/32$

Where F_{CK} is the input rate and F_O is the output rate.

3	R/W	-	Unused.
4	R/W	REAL	Output real samples instead of complex samples. The output spectrum is centered from 0 to $F_O/2$ where F_O is the output rate (see **DEC** above for the REAL mode). NOTE: The FLIP bit described below is active low in the real mode.
5	R/W	OFFSET	Offset the complex output spectrum. Used in the complex output mode (REAL=0) to force the output spectrum to be centered at $F_O/2$, where F_O is the output sample rate (see **DEC** above for the COMPLEX mode). This mode is useful for single-sideband AM signals because it moves the lower band edge up to zero frequency where it belongs. The upper half of the spectrum will appear as negative frequencies.
6	R/W	FLIP	Flip the output spectrum. This bit inverts the output spectrum. In the complex mode the spectrum is flipped about zero. In the real mode the spectrum is flipped about $F_O/4$, where F_O is the real mode's output sample rate. In the complex mode FLIP=1 flips the spectrum. In the real mode FLIP=0 flips the spectrum.
7	R/W	DIAG	Use the diagnostic ramp for the input to the chip instead of the **X** input. The ramp counts from -2048 to +2047 and then starts over again.

The effect on the output spectrum of the REAL, OFFSET and FLIP bits is illustrated in the following diagram. (F_O is the output sample rate)

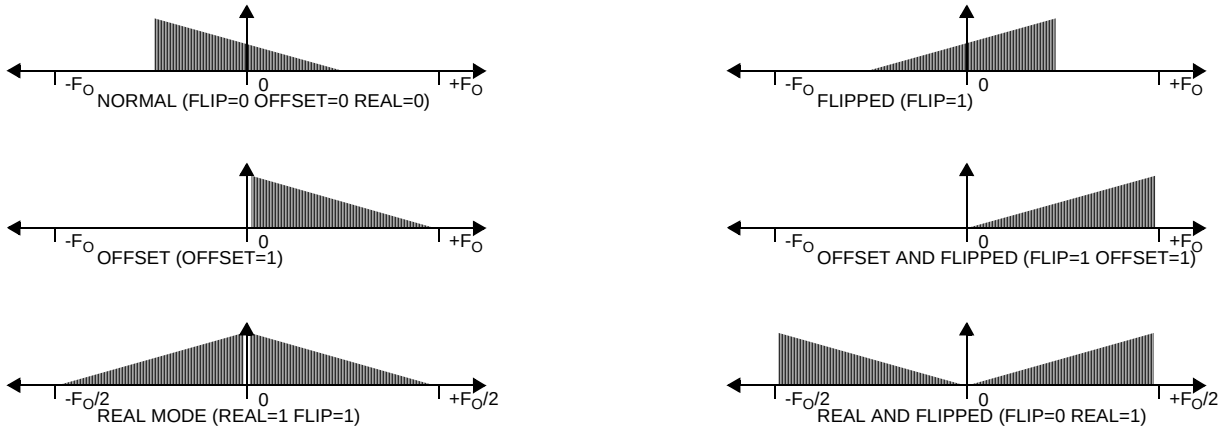


Figure 4. Output Spectral Formats

3.4 GAIN CONTROL REGISTERS

These registers set the output gain.

ADDRESS 6: Gain Control Register

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**F[0:7]**	The 8 bit gain fraction.

ADDRESS 7: Gain Exponent Register

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	**S[0:3]**	The 4 bit gain exponent.
4	R/W	GS_MODE	Turns on the synchronous gain mode. See below.
5	R/W	CKDET_DISABLE	Provided for testability. Turns off the clock loss detect function in the powerdown circuit. This bit powers up low and should be kept low.
6	R	-	unused
7	R	-	unused.

The chip's input to output gain is set using **F** and **S** according to the formula:

$$GAIN = 2^{(\mathbf{S}-\mathbf{B})}(1+\mathbf{F}/256)$$

where **B** is the base gain setting which is a function of the decimation mode of the chip. The unity gain setting (**S**=**B** and **F**=0) means that a 12 bit DC input will show up in the upper 12 bits of the 16 bit output.

The values of **B** are:

DEC	B
0 or 1	6
2	5
3	4
4	3
5	2
6	1
7	0

The GS_MODE control bit determines when new gain settings are applied to the output. New gain settings are double buffered so that they can be synchronized with the output words. If GS_MODE is low, then the gain settings are applied to the output samples immediately after **S** has been loaded. If GS_MODE is high, then the new gain settings are not used until $\overline{\mathbf{GS}}$ goes low.

NOTE: The gain settings must be loaded in the correct order- **F** first and then **S**. The circuit detects new gain settings by sensing when **S** is loaded. this means that **S** must be loaded even if one only wishes to change **F**.

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3.5 OUTPUT MODE REGISTER

The output mode register controls the output formatting.

ADDRESS 8: Output mode register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	IQ_MUX	The IQ_MUX control is used in the complex mode to multiplex the I and Q output words onto the **I[0:15]** output pins. Normally the I and Q halves are output on separate ports. When this bit is high, the halves are multiplexed together so that the I half is output first, followed by the Q half. The word strobe (**WS**) rate is doubled in this mode. The **IFLAG** output signal is used in this mode to identify the I half of each complex pair. The **Q[0:15]** output pins are forced low in this mode.
1	R/W	WS_POL	Changes the polarity of **WS**.
2	R/W	WS_MODE	Changes the mode of **WS**. Normally **WS** pulses high during the clock cycle before an **I** or **Q** output transition. This bit changes **WS** so that it is a 50% duty cycle clock with its rising edge in the middle of each output period
3	R/W	-	Unused
4	R/W	R10	Round the output samples to the 10 bits MSBs of the output word.
5	R/W	R12	Round the output samples to the 12 bits MSBs of the output word.
6	R/W	R14	Round the output samples to the 14 bits MSBs of the output word.
7	R/W	R16	Round the output samples to the 16 bits MSBs of the output word.

One and only one of the rounding options should be selected. Unused LSBs are cleared.

The IQ_MUX and WS_MODE controls are illustrated in the timing diagrams shown in Figure 5. Note that the polarity shown for **WS** can be changed using the WS_POL control.

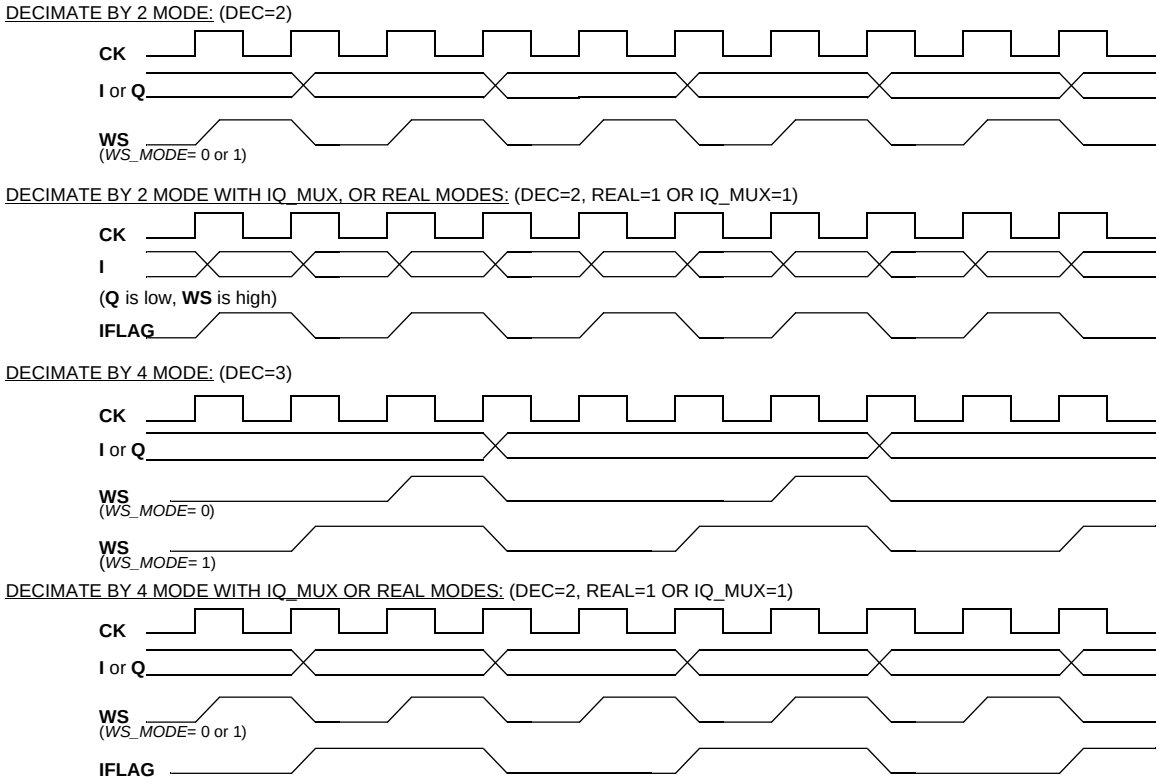


Figure 5. Timing For Output Modes

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3.6 OUTPUT STATUS REGISTER

This register contains flags and status information for the output samples.

ADDRESS 9: Output Status Register

BIT	TYPE	NAME	DESCRIPTION
0	R/W	READY	Tells the chip that the user is ready to capture an output sample. The chip clears this bit when it has captured the sample. See Notes below.
1	R/Clear	MISSED	The chip sets this bit high if a new output sample was ready but the user had not set READY high. This lets the user know if a sample has been missed. This bit is cleared by writing a 0 to the bit. Attempting to write a 1 to this bit does nothing.
2	R/W	INT_ENABLE	This bit is used to turn on the interrupt output. If this bit is off the **$\overline{\text{INT}}$** output pin is forced high. When this bit is high the **$\overline{\text{INT}}$** output pin is equal to READY. When READY goes low, meaning that a new sample has been captured, the **$\overline{\text{INT}}$** pin will go low. If **$\overline{\text{INT}}$** is tied to a processor's interrupt input, then the processor will be interrupted whenever a new sample is ready.
3	R/W	-	Unused
4	R/W	OFLOW_MODE	This bit sets the mode of the **$\overline{\text{OFLOW}}$** output. When OFLOW_MODE is low the **$\overline{\text{OFLOW}}$** output is an inverted version of OVERFLOW (see bit 6 below). If OFLOW_MODE and OFLOW_ENABLE are high, then the **$\overline{\text{OFLOW}}$** output pulses low for one clock cycle each time there is an overflow.
5	R/W	OFLOW_ENABLE	This bit enables the overflow modes. If this bit is low, then OVERFLOW (see bit 6 below) will not be set and the **$\overline{\text{OFLOW}}$** output will not go low. This bit does not affect the overflow detection and saturation logic in the gain circuit.
6	R/Clear	OVERFLOW	The chip sets this bit when an overflow occurs and OFLOW_ENABLE is turned on. This bit can be used to indicate if the gain is set too high. This bit stays high until the user clears it. The bit is cleared by writing a 0 to it. Attempting to write a 1 to this bit does nothing.
7	R/W	POWER_DOWN	This bit is used to put the chip into a power down (standby) mode. In this mode the chip is put into a static powerdown mode. All control register settings are preserved, but the output data will be invalid.

The READY signal is used to capture output samples and to read them into an external processor. The user captures outputs by setting the READY bit and then waiting for the bit to be cleared by the chip. When the bit goes low the processor can read the samples out of the I and Q output registers described in section 3.9. The processor can wait for READY to go low by either continuously reading this register, or it can use the interrupt output **$\overline{\text{INT}}$** to tell it when the sample is ready. To use the interrupt output mode the user must tie the **$\overline{\text{INT}}$** output pin from the chip to an interrupt input of the processor. The processor can then capture samples by setting READY and then setting INT_ENABLE (INT_ENABLE should be set after READY in order to avoid a spurious interrupt due to the interrupt being enabled before READY has settled to its high state). The processor will be interrupted when READY goes low again. When it is interrupted the processor can turn off INT_ENABLE, read the I/Q outputs, and then start over again.

The MISSED flag is provided to let the processor know if it has taken too long to read the I/Q samples before rearming the READY bit. If the processor wants to use the MISSED flag it should clear the flag the first time it sets the READY bit and then check it after setting the READY bit thereafter. The READY bit is set and the MISSED bit cleared by writing a 01(hex) to this register. The READY bit is set and the MISSED bit is left alone by writing a 03(hex) to this register.

NOTE: The READY bit will not be cleared if the sample is captured while the user is setting the READY bit. This will cause the READY bit to stay high after the output is captured and will not allow the chip to capture any more samples until the bit is cleared and set again. The user can detect this incorrect "ready" state by always clearing the MISSED bit when setting the READY bit. The incorrect state is detected if MISSED goes high when READY is high. The work-around to guarantee capturing an output sample is to always clear READY before setting it.

3.7 ONE SHOT ADDRESS

The one shot pulse is generated on the **$\overline{OS}$** pin by writing to address 10. This is a write-only address and the data written to it is irrelevant.

ADDRESS 10: ONE SHOT

3.8 CHECKSUM REGISTER

This read-only register stores the checksums generated in the diagnostic mode.

ADDRESS 11: CHECKSUM

BIT	TYPE	NAME	DESCRIPTION
0-7	R	CHECK[0:7]	The 8 bit checksum. The checksum is generated as a non-linear feedback accumulation of the **BS**, **FS**, **I**, and **Q** output bits. The current checksum is stored in this register and the checksum generator is cleared whenever the internal sync goes low (see SS_MUX in Section 3.2 for the modes of the internal sync).

3.9 I AND Q OUTPUT REGISTERS

These registers are used to capture output samples.

ADDRESS 12: I-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[0:7]**	Least significant 8 bits of the **I** output.

ADDRESS 13: I-Output Byte 1

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**I[8:15]**	Most significant 8 bits of the **I** output.

ADDRESS 14: Q-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**Q[0:7]**	Least significant 8 bits of the **Q** output.

ADDRESS 15: Q-Output Byte 0

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**QI[8:15]**	Most significant 8 bits of the **Q** output.

The user reads the **I** and **Q** outputs through these read-only registers. The captured samples can be used for gain control, analysis, display, or diagnostics.

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4.0 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Table 1: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	4.0	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.7	V_{CC}+0.7	V	
Storage Temperature	T_{STG}	-65	150	°C	
Lead Soldering Temperature (10 seconds)			300	°C	
Clock Rate	F_{CK}	1		KHz	1

Notes:

1. Below 1 KHz the clock loss detect circuit will power down the chip. If the clock loss detect circuit is disabled (bit 5, address 7) and the clock is stopped, the chip may draw up to one Amp of power supply current for approximately 10 seconds. After 10 seconds the current will go down to below 50 mAmps.

4.2 RECOMMENDED OPERATING CONDITIONS

Table 2: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	3.0	3.6	V	
Temperature Ambient, no air flow	T_A	-40	+85	°C	1
Junction Temperature	T_J		125	°C	1

Notes:

1. Thermal management is required to keep T_J below MAX for full rate operation. See Table 3 below.

4.3 THERMAL CHARACTERISTICS

Table 3: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	GC1012B-PQ			UNITS
		2 Watts	4 Watts	6 Watts	
Theta Junction to Ambient	θja	18	11	10	°C/W
Theta Junction to Case	θjc	4	4	4	°C/W

Note: Air flow will reduce **θja** and is highly recommended.

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4.4 DC CHARACTERISTICS

All parameters are industrial temperature range of 0 to 85 ^{o}C ambient unless noted.:

Table 4: DC Operating Conditions

PARAMETER	SYMBOL	Vcc = 3.3V		UNITS	NOTES
		MIN	MAX		
Voltage input low	V_{IL}		0.8	V	1
Voltage input high	V_{IH}	2.0		V	2
Input current (V_{IN} = 0V)	I_{IN}	Typical +/- 50		uA	2
Voltage output low (I_{OL} = 2mA)	V_{OL}		0.5	V	2
Voltage output high (I_{OH} = -2mA)	V_{OH}	2.4	3.3	V	2
Data input capacitance (All inputs except **CK** and **C[0:15]**)	C_{IN}	Typical 4		pF	1
Clock input capacitance (**CK** input)	C_{CK}	Typical 10		pF	1
Control data capacitance (**C[0:15]** I/O pins)	C_{CON}	Typical 6		pF	1

Notes:

1. Controlled by design and process and not directly tested. Verified on initial parts evaluation.
2. Each part is tested at 85^{o}C for the given specification.

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4.5 AC CHARACTERISTICS

Table 5: AC Characteristics (0 TO +85^{o}C Ambient, unless noted)

PARAMETER	SYMBOL	3.3V +/- 5%		UNITS	NOTES
		MIN	MAX		
Clock Frequency	F_{CK}	0.01	100	MHz	2, 3, 4
Clock low period (Below V_{IL})	t_{CKL}	4		ns	1
Clock high period (Above V_{IH})	t_{CKH}	4		ns	1
Data setup before **CK** goes high (**X, SS, AS** or **GS**)	t_{SU}	4		ns	1
Data hold time after **CK** goes high	t_{HD}	2		ns	1
Data output delay from rising edge of **CK**. (**I, Q, WS, IFLAG, OS, OFLOW, SO**	t_{DLY}	0	8	ns	1, 5
Data to tristate delay (**I** or **Q** to hiZ from **OEI** or **OEQ**)	t_{DZ}	2	5		1
Tristate to data output delay (**I** or **Q** valid from **OEI** or **OEQ**)	t_{ZD}	3	8	ns	1, 5
Control Setup before **CS** goes low (**A**, **R/W** during read, and **A**, **R/W**, **C** during write)	t_{CSU}	5		ns	1
Control hold after **CS** goes high (**A**, **R/W** during read, and **A**, **R/W**, **C** during write)	t_{CHD}	5		ns	1
Control strobe (**CS**) pulse width (Write operation)	t_{CSPW}	20		ns	1,6
Control output delay **CS** low to **C** (Read Operation)	t_{CDLY}		20	ns	1,6
Control tristate delay after **CS** goes high	t_{CZ}		5	ns	1
Quiescent supply current (V_{IN}=0 or V_{CC}, F_{CK} = 1KHz)	I_{CCQ}		200	uA	1
Supply current (F_{CK} =100MHz)	I_{CC}		400	mA	1, 7

Notes:

1. Controlled by design and process and not directly tested. Verified on initial part evaluation.
2. Each part is tested at 85 deg C for the given specification.
3. Temperature range is verified by lot sampling.
4. The chip may not operate properly at clock frequencies below MIN and MAX.
5. Current load is 2ma. Delays are measured from the rising edge of the clock to the output level rising above V_{IH} or Falling below V_{IL}.
6. Capacitive output load is 80pf.
7. Current changes linearly with voltage and clock speed. Icc (MAX) $= \left(\frac{VCC}{5}\right)\left(\frac{F_{CK}}{100M}\right)400mA$

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5.0 APPLICATION NOTES

5.1 POWER AND GROUND CONNECTIONS

The GC1012B chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC} and GND pins. If possible the GC1012B chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 and 0.1 μf) adjacent to each GC1012B chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors adjacent to each V_{CC} and GND pair.

IMPORTANT

The GC1012B chip may not operate properly if these power and ground guidelines are violated.

5.2 STATIC SENSITIVE DEVICE

The GC1012B chip is fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments.

5.3 100 MHZ OPERATION

Care must be taken in generating the clock when operating the GC1012B chip at its full 100 MHz clock rate. The user must insure that the clock is above 2 volts for at least 4 nanoseconds and is below 0.8 volts for at least 4 nanoseconds. At 1000 MHz the clock period is only 10 nanoseconds so that the clock must have a duty cycle of exactly 50%, and the rise and fall times can only be 1 nanosecond each. One must also be careful to prevent clock undershoot below ground. An ideal clock at 100 MHz would be a square wave with a low voltage of 0.5 volts and a high voltage of 2.5 volts.

5.4 REDUCED VOLTAGE OPERATION

The power consumed by the GC1012B chip can be greatly reduced by operating the chip at the lowest V_{CC} voltage which will meet the application's timing requirements. When operating at a reduced voltage, GRAYCHIP recommends driving the GC1012B chip inputs with 5 volt to 3 volt interface chips.

5.5 SYNCHRONIZING MULTIPLE GC1012B CHIPS

A system containing a bank of GC1012B chips will need to be synchronized so that the output frames from each chip are aligned, and, if desired, so that their frequency accumulators are running synchronously. The GC1000 Input Switch chip has built in sync counters which are designed specifically for this purpose. If the GC1000 chip is not used, then the one-shot strobe (see Section 3.7) can be used. The bank of chips should be interconnected so that the **$\overline{\text{OS}}$** pin of one GC1012B chip is tied to the **$\overline{\text{SS}}$** input of all of the chips. The one-shot strobe mode can then be used to simultaneously synchronize all of the chips. The **$\overline{\text{OS}}$** pin of a second GC1012B chip should be tied to the **$\overline{\text{AS}}$** input of all of the chips. The one-shot mode of the second chip can be used to synchronize the frequency accumulators whenever the tuning frequency has been changed.

5.6 PROCESSING COMPLEX DATA

Two GC1012B chips can be used to process complex input data by using one chip to process the I-input data and the other to process the Q-input data. If the two chips are synchronized as discussed above, then the complex output stream can be reconstructed by adding and subtracting the I and Q outputs of the two chips. A programmable gate array chip such as from XILINX would be ideal for this post-processing. The configuration for processing complex data is illustrated in Figure 6.

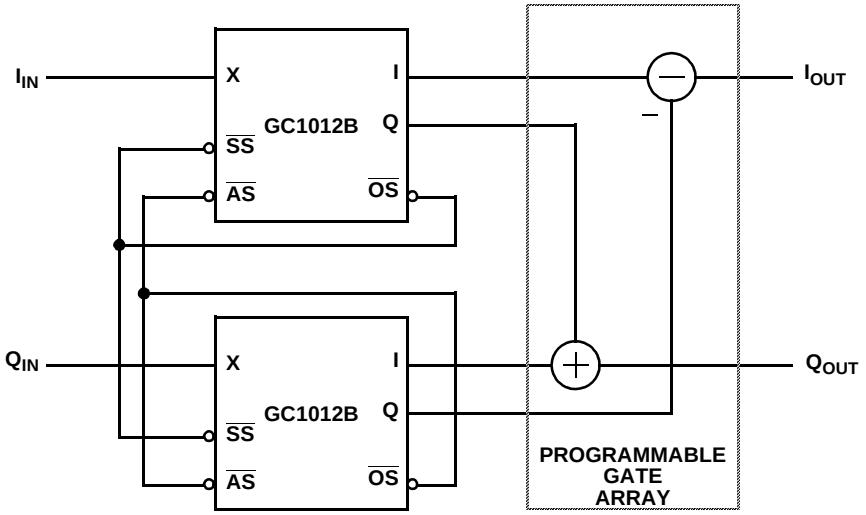


Figure 6. Processing Complex Input Data

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5.7 EXAMPLE RECEIVER ARCHITECTURE

An example digital receiver architecture using the GC1012B chip is shown in Figure 7.

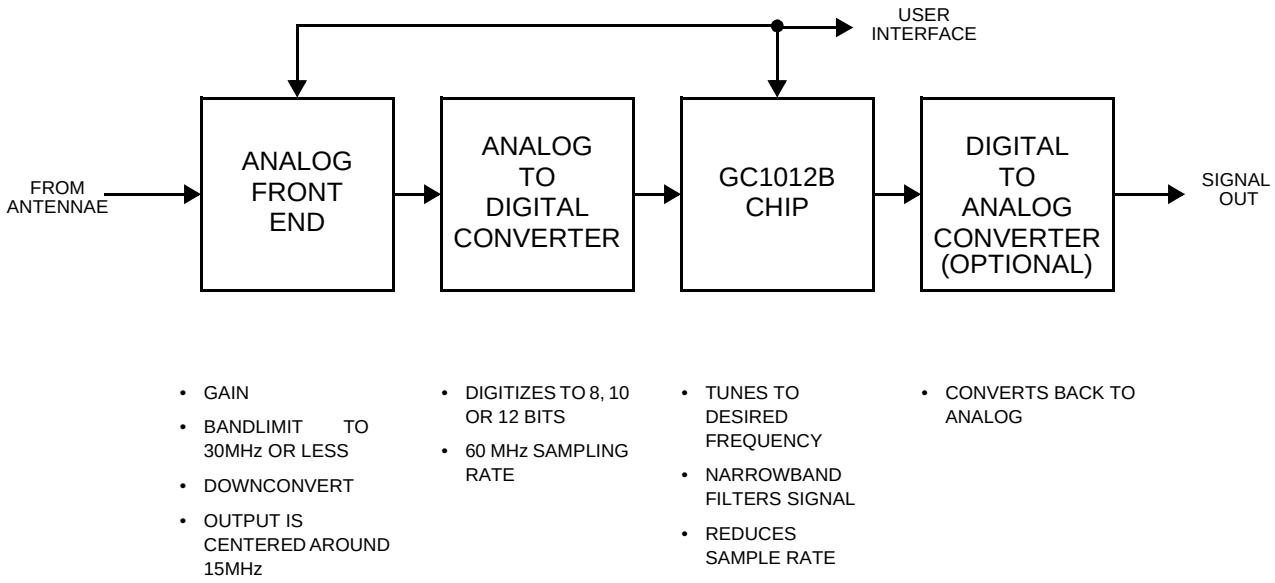


Figure 7. Example Digital Receiver Architecture

The receiver contains an analog front end which downconverts up to 30MHz of radio spectrum to an IF frequency around 15MHz[1]. It also adjusts the gain of the signal so that it fills the dynamic range of the analog to digital converter (ADC). The ADC digitizes the signal using up to 12 bits of resolution at a sampling rate up to 60 MHZ. The GC1012B chip tunes, downconverts, and narrowband filters desired frequencies from within the 30 MHz band. The GC1012B output can either be converted back to analog or kept in its digital state for subsequent signal processing.

1. Note that the HF spectrum (1 to 30MHz) can be digitized directly.

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5.8 LATENCY THROUGH THE GC1012B

Two latencies are of interest, the latency from a step function in to a step function out (midpoint), and the latency from a step function until the end of the “ringing” in the step function output (endpoint). These latencies are:

Table 6: Latency

Output Mode	Midpoint	Endpoint	Values of D (decimation)
Real	41 + 20D	41 + 40D	1, 2, 4, 8, 16 and 32
Complex	35 + 10D	35 + 20D	2, 4, 8, 16, 32 and 64

Another latency of interest is the delay from SS input to stable WS. The WS strobe becomes stable and is low after 9 clocks, before 9 clocks the WS is unknown and may go high at any time. The delay until the first valid high WS is a function of decimation. For decimate by 2 the delay from SS is 10 clocks, for 4 the delay is 12 clocks, for 8 the delay is 16 clocks and for decimation ratios of 16, 32 and 64 the delay is 24 clocks. WS is high at clock 24 for all decimations.

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